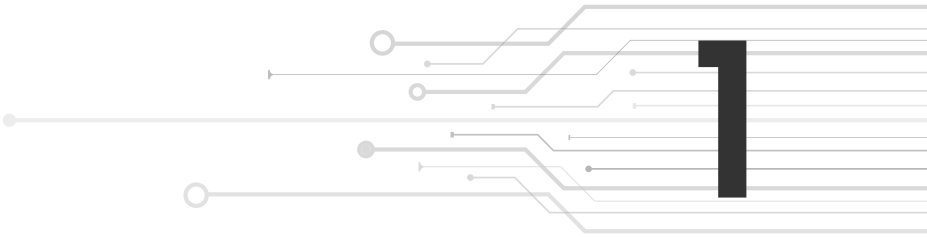

1 Introduction

This thesis shall introduce the creation of a Universal Verification Component (UVC), which inherits the aspects of re-usability, scalability and stability in order to be used in later designs and further projects. The UVC includes a digital model of an analog functionality as well as an environment connected to it, which provides all abilities needed to correctly interfere with the digital pendant in the same way as one would with the analog device. This specific UVC shall represent the functionality of Low Dropout Voltage Regulators (LDO), specifically those used in Dialog Semiconductors Power Management Integrated Circuits (PMIC).

1.1 Motivation

The development or progression of an electronic device of such a high level class brings together many different teams, time-lines and objectives. To deliver a fully functional and tested device at Tape-Out, early debugging and verification has to be done. In order to accomplish this with various stages of finished and in-progress blocks and to highly minimize simulation time, analog blocks tend to be represented as digital code - mostly in Module or Register Transfer (RTL) level. Those representations have to implement all functionality with the same in- and output signals given by the real device (pin accurate), which means that no or only minor adaptations have to be done in the existing digital layers that would or will later connect to the analog interfaces. When developing such UVC's, the designer has to choose a fitting level of abstraction for the model and provide an as generic as possible code, so the UVC can be used in many different flavors.

1.2 Objectives

The main objectives for this thesis are creating a RTL representation of LDO's used in a specific and currently in progress PMIC, implementing all the functionality given in the scope of that specific PMIC as well as reasonable features that might be needed in future or similar projects. Further, a Universal Verification Methodology (UVM) environment shall be created to interfere with the created model - this leads to reusable verification methods and easier integration when used in future projects to simulate analog behavior. After the verification of the finished UVC and created testbench, it shall be embedded into the Dialog Semiconductor work-flow for later reuse.

1.3 Outline

This thesis is divided into three parts: First, a background in digital development, as well as the history of Hardware Description Languages (HDL) and the further progress towards reusable verification methods such as UVM is given. Secondly, the analog functionality of LDO's is evaluated, transformed into digital blocks and implemented as a single module. This module is further embedded into the UVM Environment and verified using various test-scenarios together with the rest of the digital environment. After the successful verification, the coverage report is generated and discussed. Finally, the UVC will be integrated into the existing work-flow. The last part draws a conclusion on the done process and outlines possible further developments in this area.