CS 33301-01

Fall 2021

Project 2: Input (Interrupt) Tutorial

Project 2. Write a program with Appropriate Comments. Input switch should be working with the interrupt.

HW Connection: Using External Interrupt 0 for input switch (normal state is high and pushed state is low) and Port C bit 3 for output LED (On is pin high and off is pin low)

1. Initial state: LED OFF → External LED

After 1 second - when the button is pushed. → LED ON

After 1 second - Push again → LED OFF

After 1 second - Push again → LED ON

…

2. initial state: internal LED ON and external LED OFF with optimal delayed value

a. After 1 second - when the pushed button is off (rising edge). → External LED ON with optimal delayed value and internal LED OFF
b. After 1 second - Push (Falling edge) again → External LED OFF and internal LED ON with optimal delayed value
c. After 1 second - Push (Low status) again → External LED ON with optimal delayed value and internal LED OFF
d. After 1 second - Push (Any Change) again → External LED OFF and internal LED ON with optimal delayed value
… (Repeat a – d)

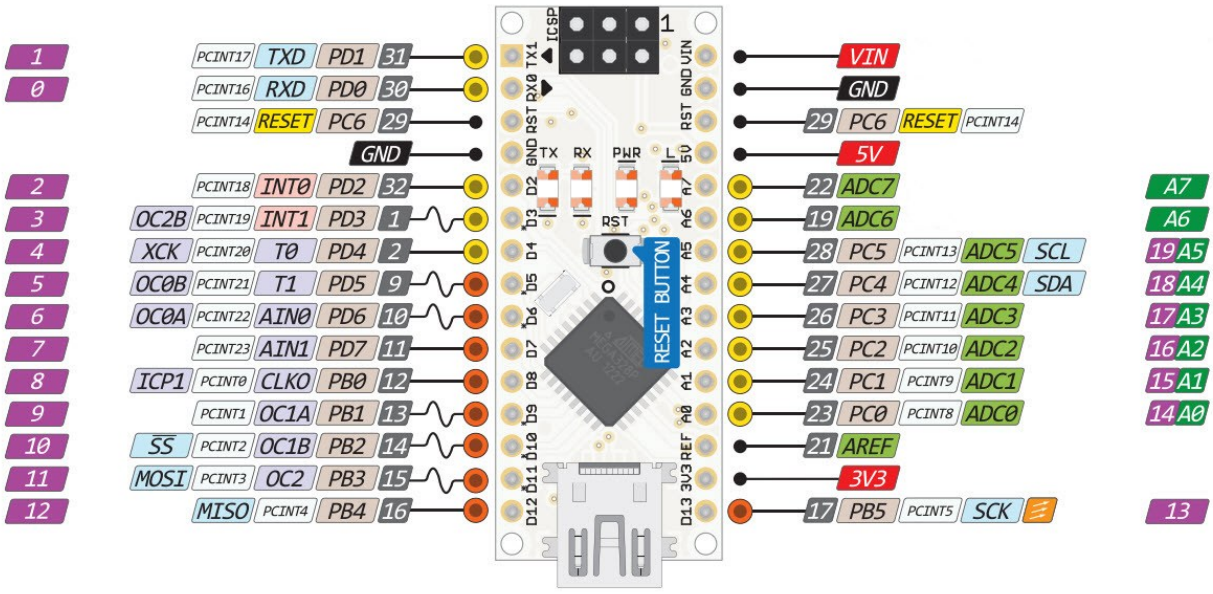
% You should not use any Arduino function.

% Any code from Arduino library is found, it will be directly zero point.

% We will not accept any H/W issues on due date and one day before. If you have H/W issues, please contact the GA as soon as possible.

```
// Sample Code for External Interrupt


int main(void)
{
   unsigned char *portD;
   portD = (unsigned char *) 0x2B;

   // Enable the pull-up resistor on PD2 using the Port D
   // Data Register (PORTD)
   *portD |= 0x04; // b 0000 0100

   // Configure external interrupt 0 to generate an interrupt request on any
   // logical change using External Interrupt Control Register A (EICRA)
   unsigned char *AT328_EICRA;
   AT328_EICRA = (unsigned char *) 0x69;
   *AT328_EICRA |= 0x01;  // b 0000 0001 --> b xxxx xx11 --> Any change for INT 0

   // Enable external interrupt 0 using the External Interrupt Mask Register
   // (EIMSK)
   unsigned char *AT328_EIMSK;
   AT328_EIMSK = (unsigned char *) 0x3D;
   *AT328_EIMSK |= 0x01; // b 0000 0001 --> b xxxx xxx1 --> INT0 enable

   // Configure PB5 as an output using the Port B Data Direction Register
   // (DDRB)
   unsigned char *portDDRB;
   portDDRB = (unsigned char *) 0x24;
   *portDDRB |= 0x20;  // PORTB bit 5 as output (bit --> 1) --> b 0010 0000 --> b xx1x xxxx

   // Enable interrupts using SREG
   unsigned char *ptrSREG;
   ptrSREG = (unsigned char *) 0x5F;
   *ptrSREG |= 0x80; // b 1000 0000 == 0x80 --> b 1xxx xxxx

   //sei();
   // Loop forever
   while (1)
   {
      // Nothing to do here
      // All work is done in the ISR
   }
}
```

```
ISR(INT0_vect)
{
   unsigned char *portPinD;
   portPinD = (unsigned char *) 0x29;
   unsigned char *portB;
   portB = (unsigned char *) 0x25;

   // Read PD2 using the Port D Pin Input Register (PIND)
   if (*portPinD & 0x04)
   {
      // PD2 is high, so button is released
      // Set PB5 low using the Port B Data Register (PORTB)
      *portB &= ~0x20;
   }
   else
   {
      // PD2 is low, so button is pressed
      // Set PB5 high using the Port B Data Register (PORTB)
      *portB |= 0x20;
   }
}
```



6.4.1 PORTB - THE PORT B DATA REGISTER

Bit	7	6	5	4	3	2	1	0
0x25	PORTB7	PORTB6	PORTB5	PORTB4	PORTB3	PORTB2	PORTB1	PORTB0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

- PORTB7-0: GPIO data value stored in bit *n*.

6.4.2 DDRB - THE PORT B DATA DIRECTION REGISTER

Bit	7	6	5	4	3	2	1	0
0x24	DDRB7	DDRB6	DDRB5	DDRB4	DDRB3	DDRB2	DDRB1	DDRB0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

- DDRB7-0: selects the direction of pin *n*. If DDRB*n* is written '1', then PORTB*n* is configured as an output pin. If DDRB*n* is written '0', then PORTB*n* is configured as an input pin.

6.4.3 PINB - THE PORT B INPUT PINS ADDRESS

Bit	7	6	5	4	3	2	1	0
0x23	PINB7	PINB6	PINB5	PINB4	PINB3	PINB2	PINB1	PINB0
Read/Write	R	R	R	R	R	R	R	R
Default	-	-	-	-	-	-	-	-

- PINB7-0: logic value present on external pin *n*.

11.4.8 PORTD – The Port D Data Register

Bit	7	6	5	4	3	2	1	0	
0x0B (0x2B)	PORTD7	PORTD6	PORTD5	PORTD4	PORTD3	PORTD2	PORTD1	PORTD0	PORTD
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

11.4.9 DDRD – The Port D Data Direction Register

Bit	7	6	5	4	3	2	1	0	
0x0A (0x2A)	DDD7	DDD6	DDD5	DDD4	DDD3	DDD2	DDD1	DDD0	DDRD
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

11.4.10 PIND – The Port D Input Pins Address

Bit	7	6	5	4	3	2	1	0	
0x09 (0x29)	PIND7	PIND6	PIND5	PIND4	PIND3	PIND2	PIND1	PIND0	PIND
Read/Write	R	R	R	R	R	R	R	R	
Initial Value	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	

10.2 Register Description

10.2.1 EICRA – External Interrupt Control Register A

The External Interrupt Control Register A contains control bits for interrupt sense control.

Bit	7	6	5	4	3	2	1	0	
(0x69)	–	–	–	–	ISC11	ISC10	ISC01	ISC00	EICRA
Read/Write	R	R	R	R	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- **Bit 7..4 – Res: Reserved Bits**

These bits are unused bits in the ATmega48P/88P/168P/328P, and will always read as zero.

- **Bit 3, 2 – ISC11, ISC10: Interrupt Sense Control 1 Bit 1 and Bit 0**

The External Interrupt 1 is activated by the external pin INT1 if the SREG I-flag and the corresponding interrupt mask are set. The level and edges on the external INT1 pin that activate the interrupt are defined in Table 10-1. The value on the INT1 pin is sampled before detecting edges. If edge or toggle interrupt is selected, pulses that last longer than one clock period will generate an interrupt. Shorter pulses are not guaranteed to generate an interrupt. If low level interrupt is selected, the low level must be held until the completion of the currently executing instruction to generate an interrupt.

Table 10-1. Interrupt 1 Sense Control

ISC11	ISC10	Description
0	0	The low level of INT1 generates an interrupt request.
0	1	Any logical change on INT1 generates an interrupt request.
1	0	The falling edge of INT1 generates an interrupt request.
1	1	The rising edge of INT1 generates an interrupt request.

- **Bit 1, 0 – ISC01, ISC00: Interrupt Sense Control 0 Bit 1 and Bit 0**

The External Interrupt 0 is activated by the external pin INT0 if the SREG I-flag and the corresponding interrupt mask are set. The level and edges on the external INT0 pin that activate the interrupt are defined in Table 10-2. The value on the INT0 pin is sampled before detecting edges. If edge or toggle interrupt is selected, pulses that last longer than one clock period will generate an interrupt. Shorter pulses are not guaranteed to generate an interrupt. If low level interrupt is selected, the low level must be held until the completion of the currently executing instruction to generate an interrupt.

Table 10-2. Interrupt 0 Sense Control

ISC01	ISC00	Description
0	0	The low level of INT0 generates an interrupt request.
0	1	Any logical change on INT0 generates an interrupt request.
1	0	The falling edge of INT0 generates an interrupt request.
1	1	The rising edge of INT0 generates an interrupt request.

10.2.2 EIMSK – External Interrupt Mask Register

Bit	7	6	5	4	3	2	1	0	
0x1D (0x3D)	–	–	–	–	–	–	INT1	INT0	EIMSK
Read/Write	R	R	R	R	R	R	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- **Bit 7..2 – Res: Reserved Bits**

These bits are unused bits in the ATmega48P/88P/168P/328P, and will always read as zero.

- **Bit 1 – INT1: External Interrupt Request 1 Enable**

When the INT1 bit is set (one) and the I-bit in the Status Register (SREG) is set (one), the external pin interrupt is enabled. The Interrupt Sense Control1 bits 1/0 (ISC11 and ISC10) in the External Interrupt Control Register A (EICRA) define whether the external interrupt is activated on rising and/or falling edge of the INT1 pin or level sensed. Activity on the pin will cause an interrupt request even if INT1 is configured as an output. The corresponding interrupt of External Interrupt Request 1 is executed from the INT1 Interrupt Vector.

- **Bit 0 – INT0: External Interrupt Request 0 Enable**

When the INT0 bit is set (one) and the I-bit in the Status Register (SREG) is set (one), the external pin interrupt is enabled. The Interrupt Sense Control0 bits 1/0 (ISC01 and ISC00) in the External Interrupt Control Register A (EICRA) define whether the external interrupt is activated on rising and/or falling edge of the INT0 pin or level sensed. Activity on the pin will cause an interrupt request even if INT0 is configured as an output. The corresponding interrupt of External Interrupt Request 0 is executed from the INT0 Interrupt Vector.