COD HW 4

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4.16

4.16 In this exercise, we examine how pipelining affects the clock cycle time of the processor. Problems in this exercise assume that individual stages of the datapath have the following latencies:

IF	ID	EX	MEM	WB
250 ps	350 ps	150 ps	300 ps	200 ps

Also, assume that instructions executed by the processor are broken down as follows:

ALU/Logic	Jump/Branch	Load	Store
45%	20%	20%	15%

4.16.1 [5] <§4.5> What is the clock cycle time in a pipelined and non-pipelined processor?
4.16.2 [10] <§4.5> What is the total latency of an `ld` instruction in a pipelined and non-pipelined processor?
4.16.3 [10] <§4.5> If we can split one stage of the pipelined datapath into two new stages, each with half the latency of the original stage, which stage would you split and what is the new clock cycle time of the processor?

4.16.1 对于单周期处理器，时钟周期为最长指令时长。本题中取 lw 指令，则总时长为 250 + 350 + 150 + 300 + 200 = 1250ps；

对于流水线处理器，时钟周期为最长流水段时长。本题中为 ID 段，为 350ps。

4.16.2 ld 指令在单周期处理器中耗时 1250ps， 在流水线处理器中耗时 350 x 5 = 1750ps。

4.16.3 将 ID 段进行分裂。此时流水段最长耗时为 MEM 段的 300ps，所以流水线处理器的时钟周期为 300ps。

4.23

4.23 If we change load/store instructions to use a register (without an offset) as the address, these instructions no longer need to use the ALU. (See Exercise 4.15.) As a result, the MEM and EX stages can be overlapped and the pipeline has only four stages.

4.23.1 [10] <§4.5> How will the reduction in pipeline depth affect the cycle time?

4.23.2 [5] <§4.5> How might this change improve the performance of the pipeline?

4.23.3 [5] <§4.5> How might this change degrade the performance of the pipeline?

4.23.1 由于 MEM 与 EX 段合并，原先的 MEM 段耗时不再影响流水线时钟周期。此时时钟周期为 IF ID EX_{new} WB 段的最长用时。但是合并后 EX_{new} 段耗时依然为 max{MEM, EX_{old}}，所以 CPU 时钟周期保持不变。

4.23.2 对于 load 指令，当其与后续指令发生数据相关时，流水线不再需要停顿，因为在 EX 段 load 指令即可取到目标值，通过数据前递即可在下一周期将数据传递给 EX 段的后续指令。所以流水线停顿次数会减少。

4.23.3 load 与 store 指令的目标地址均需要提前存入寄存器中，这为汇编程序编写带来了一定的麻烦。换而言之，在 load 和 store 指令前都需要增加额外的运算指令，使得程序更为复杂。