WT013261-S5 Series Datasheet

Version 1.0

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Revision History

Version	Date	Developed/ Changed Content	Modifier By	Auditor
V1.0	2025-7-9	First Creation	Pail	Louie

Contents

1. Overview

1.1.Products Introduction

WT013261-S5 series module is an integrated Wi-Fi & BLE module designed based on Espressif ESP32-C61 series chipset launched by Wireless-Tag Technology Co.,Limited.The WT013261-S5 supports 2.4 Wi-Fi6 (802.11ax), Bluetooth®5 (LE), and is powerful with a rich set of peripheral interfaces supporting PCB antenna or I-PEX (Generation 3) RF coaxial connectors, and is designed for Internet of Things (IoT), industrial automation, healthcare, andconsumer electronics applications.

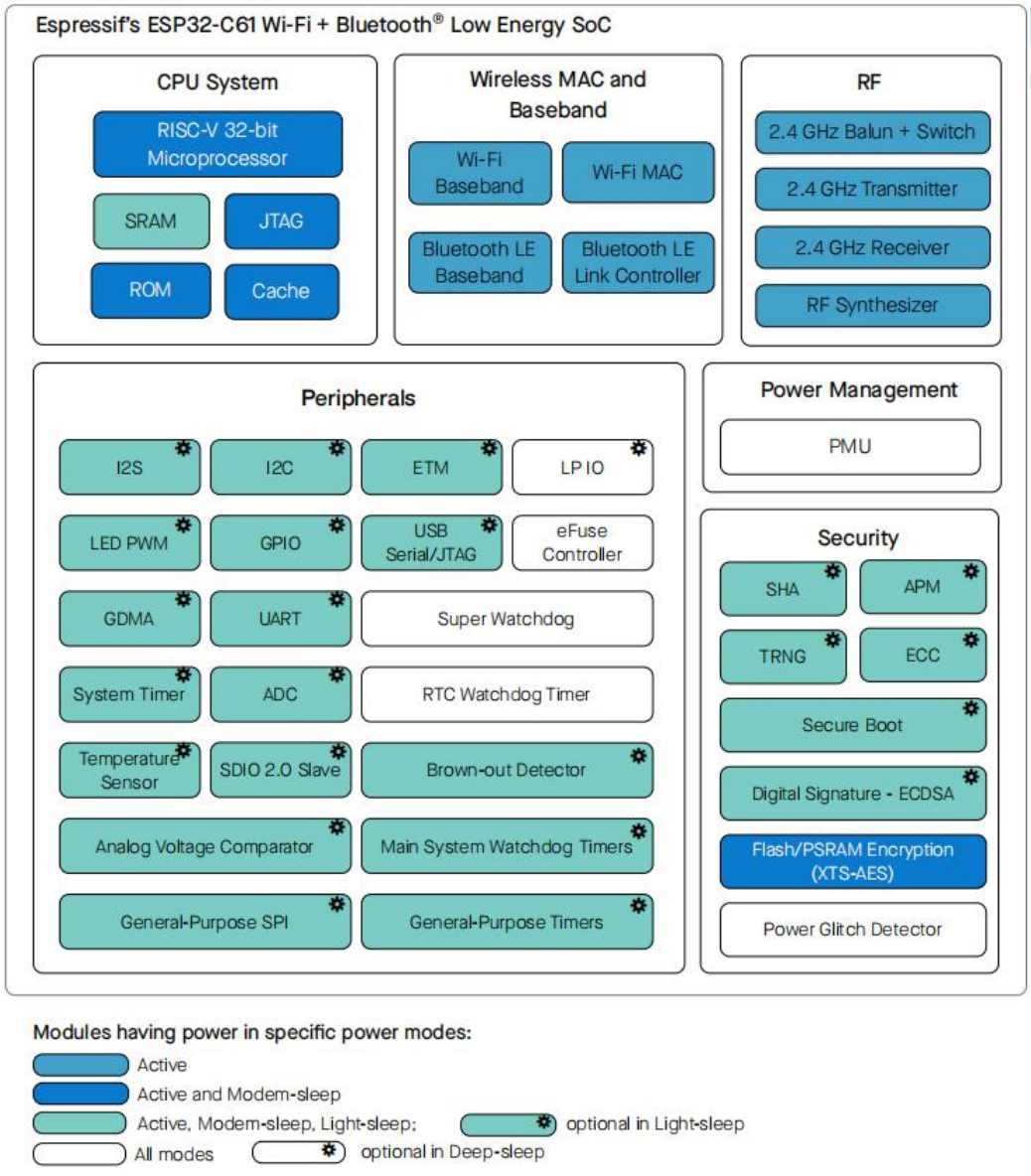

Figure 1: Main Chip Architecture Diagram

The WT013261-S5 utilizes a PCB mounted antenna and the WT013261-S5U utilizes a connector to attach an external antenna. Both modules are available in a variety of models,see the table below for more information.

WT013261-S5 Series Model Number Comparison

Part Number	Flash	PSRAM	Module Size (mm)
WT013261-S5-N4	4MB	/	24.00*16.00
WT013261-S5-N8	8MB	/	
WT013261-S5-N4R2	4MB	2MB	
WT013261-S5-N8R2	8MB	2MB	
WT013261-S5-N4R8	4MB	8MB	
WT013261-S5-N8R8	8MB	8MB	

WT013261-S5U Series Model Number Comparison

Part Number	Flash	PSRAM	Module Size (mm)
WT013261-S5U-N4	4MB	/	24.00*16.00
WT013261-S5U-N8	8MB	/	
WT013261-S5U-N4R2	4MB	2MB	
WT013261-S5U-N8R2	8MB	2MB	
WT013261-S5U-N4R8	4MB	8MB	
WT013261-S5U-N8R8	8MB	8MB	

1.2.Product Features

- RISC-V 32-bit single-core processor at 160 MHz
- RISC-V MCU supporting 2.4GHz Wi-Fi6, BLE5
- supports PCB antenna or I-PEX RF coaxial connector.
- Mature software support, based on Espressif's ESP-IDF IoT development framework.
- Complete security mechanism, including secure boot, flash encryption and hardware encryption gas pedal.

1.3.Product Pictures

Figure 2:WT013261-S5(front)

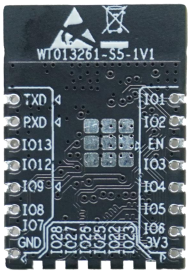

Figure 3:WT013261-S5 (back)

Figure 4:WT013261-S5U(front)

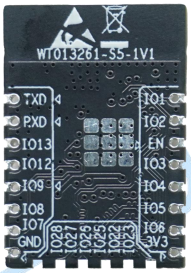

Figure 5:WT013261-S5U(back)

1.4.Application Scenarios

- Smart Home
- Industrial Automation
- Consumer Electronics
- HMI Human Machine Interaction
- Healthcare
- Mobile Pay

2. Product Specification

2.1.Block Diagram

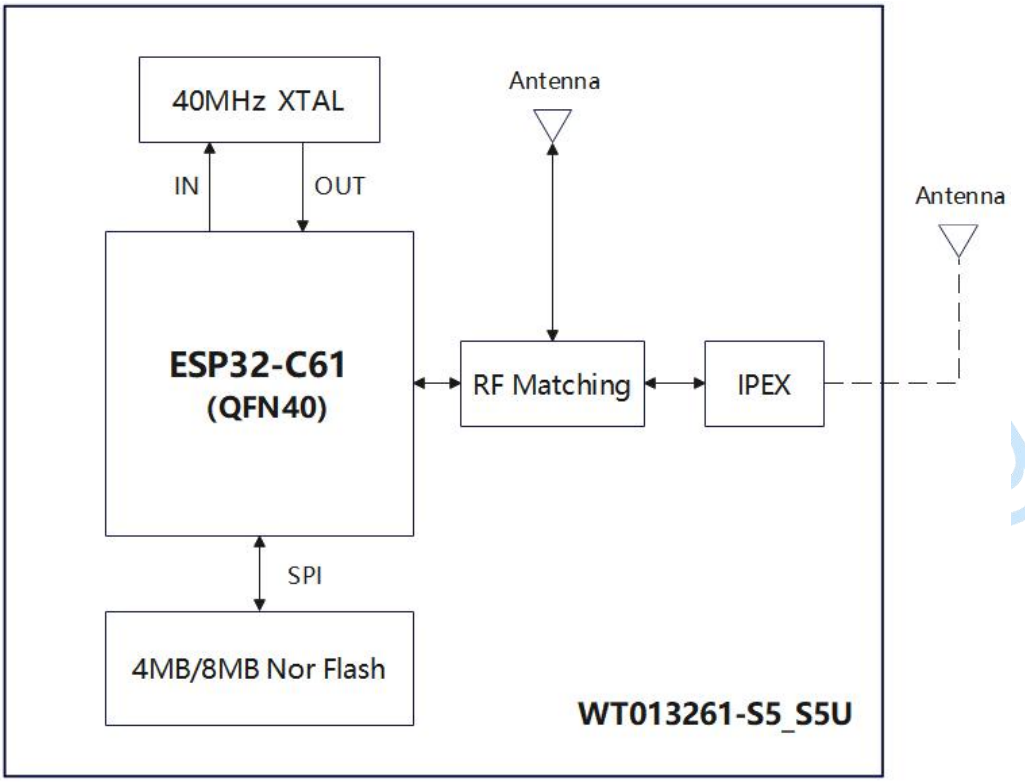

Figure 6: Block diagram of WT013261-S5

2.2.Hardware Parameters

CPU	Core	32-bit RISC-V dual-core
	Main Frequency	160 MHz
Memory	ROM	256 KB
	SRAM	320 KB
	Flash	4/8 MB
Peripheral Interface	GPIO	17
	SPI	1
	UART	3
	I2C	1
	I2S	1
	SDIO Slave	1

	LED PWM	1
	12-bit multi-channel ADC	1
	Temperature sensor	1

3. Pin Definitions

3.1.Pin Layout

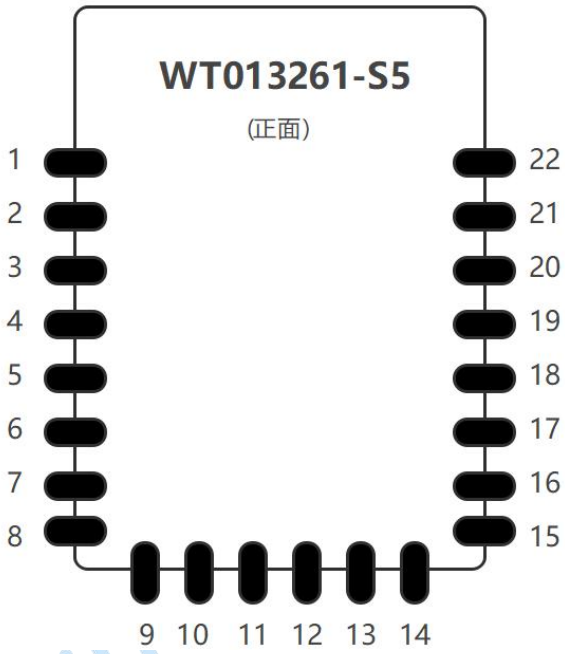

Figure 7:WT013261-S5 Pin Layout

3.2.Pin Description

Pin Definitions

No.	Name	Function
1	GPIO1	GPIO1，LP_GPIO1, XTAL_32K_N, ADC1_CHO
2	GPIO2	GPIO2，LP_GPIO2，FSPIQ
3	CHIP_EN	High: on,enable the chip; Low: off,the chip powers off; Note: Do not leave the EN pin floating.（internal 10K pull-up）
4	GPIO3	GPIO3，LP_GPIO3，MTMS，ADC1_CH1，FSPIHD
5	GPIO4	GPIO4，LP_GPIO4，MTDI，ADC1_CH2，FSPIWP
6	GPIO5	GPIO5，LP_GPIO5，MTCK，ADC1_CH3
7	GPIO6	GPIO6，LP_GPIO6，MTDO，FSPICLK

8	VCC_3V3	3.3V power in
9	GPIO23	GPIO23，SDIO_DATA3
10	GPIO22	GPIO22，SDIO_DATA2
11	GPIO25	GPIO25，SDIO_CMD
12	GPIO26	GPIO26，SDIO_CLK
13	GPIO27	GPIO27，SDIO_DATA0
14	GPIO28	GPIO28，SDIO_DATA1
15	GND	Ground
16	GPIO7	GPIO7，FSPID
17	GPIO8	GPIO8，FSPICS0，ZCD0（internal 10K pull-up）
18	GPIO9	GPIO9，ZCD1
19	GPIO12	GPIO12，USB_D-
20	GPIO13	GPIO13，USB_D+
21	U0RXD	GPIO10，U0RXD
22	U0TXD	GPIO11，U0TXD

3.3.Startup Item Configuration

3.3.1. Strapping Pins

The chip allows for configuring the following boot parameters through strapping pins and eFuse bits at power-up or a hardware reset, without microcontroller interaction.

- **Chip Boot Mode**

– Strapping pin: GPIO8 and GPIO9

- **SDIO sampling and driving clock edge**

– Strapping pin: MTDI and MTMS

- **ROM Message Printing**

– Strapping pin: GPIO8

– eFuse parameter:

EFUSE_UART_PRINT_CONTROL and EFUSE_DIS_USB_SERIAL_JTAG_ROM_PRINT

- **JTAG Signal Source**

– Strapping pin: GPIO7

– eFuse parameter:

EFUSE_DIS_PAD_JTAG, EFUSE_DIS_USB_JTAG, and EFUSE_JTAG_SEL_ENABLE

The default values of all the above eFuse parameters are 0, which means that they are not burnt. Given that eFuse is one-time programmable, once programmed to 1, it can never be reverted to 0.

The default values of the strapping pins, namely the logic levels, are determined by pins'internal weak pull-up/pull-down resistors at reset if the pins are not connected to any circuit, or connected to an external high-impedance circuit.

Default Configuration of Strapping Pin

Strapping Pin	Default Configuration	Value
MTMS	Floating	-
MTDI	Floating	-
GPIO7	Floating	-
GPIO8	Floating	-
GPIO9	Pull-up	1

To change the bit values, the strapping pins should be connected to external pull-down/pull-up resistors.

All strapping pins have latches. At system reset, the latches sample the bit values of their respective strapping pins and store them until the chip is powered down or shut down. The states of latches cannot be changed in any other way. It makes the strapping pin values available during the entire chip operation, and the pins are freed up to be used as regular IO pins after reset.

The timing of signals connected to the strapping pins should adhere to the *setup time* and *hold time* specifications in Table and Figure 8.

Description of Timing Parameters for the Strapping Pins

Parameter	Description	Min(ms)

t_{SU}	*Setup time* is the time reserved for the power rails to stabilize before the CHIP_PU pin is pulled high to activate the chip.	0
t_H	*Hold time* is the time reserved for the chip to read the strapping pin values after CHIP_PU is already high and before these pins start operating as regular IO pins.	3

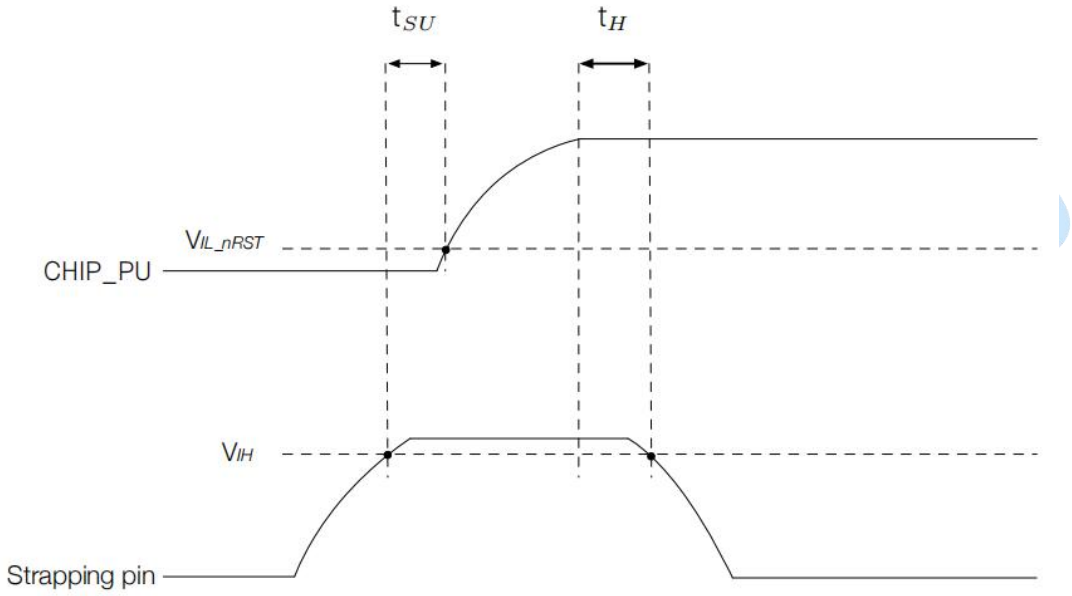

Figure 8: Visualization of Timing Parameters for the Strapping Pins

3.3.2. Chip Boot Mode Control

GPIO8 and GPIO9 control the boot mode after the reset is released.

Boot Mode	GPIO8	GPIO9
SPI Boot*	Any value	1
Joint Download Boot[1]	1	0

*marks the default value and configuration.

[1]Joint Download Boot mode supports the following download methods:

- USB-Serial-JTAG Download Boot
- UART Download Boot
- SDIO Slave 2.0 Download Boot

In SPI Boot mode, the ROM bootloader loads and executes the program from SPI flash to boot thesystem.

In Joint Download Boot mode, users can download binary files into flash using UART0, USB or SDIO Slaveinterfaces and execute it in SPI Boot mode.

In Joint Download Boot mode,, it is also possible to download binary files into SRAM using UART0, USB or SDIO Slave interfaces and execute it from SRAM.

3.3.3. SDIO Sampling and Driving Clock Edge Control

The strapping pin MTMS and MTDI can be used to decide on which clock edge to sample signals and drive output lines.

Edge behavior	MTMS	MTDI
Falling edge sampling, falling edge output	0	0
Falling edge sampling, rising edge output	0	1
Rising edge sampling, falling edge output	1	0
Rising edge sampling, rising edge output	1	1

MTMS and MTDI are floating by default, so above are not default configurations.

3.3.4. ROM Messages Printing Control

During the boot process, the messages by the ROM code can be printed to:

- **(Default) UART0 and USB Serial/JTAG controller**
- USB Serial/JTAG controller
- UART0

EFUSE_UART_PRINT_CONTROL and GPIO27 control ROM messages printing to **UART0** as shown in Table.

UART0 ROM Code Printing	EFUSE_UART_PRINT_CONTROL	GPIO8	Register[1]
Always enabled*	0*	Ignored	0
Enabled	1	0	
Disabled		1	
Disabled	2	0	
Enabled		1	

Always enabled	3	Ignored	
Disabled	Ignored	Ignored	1

*marks the default value and configuration.

[1]Register: LP_AON_STORE4_REG[0]

EFUSE_DIS_USB_SERIAL_JTAG_ROM_PRINT controls the printing to USB Serial/JTAG controller as shown in Table.

USB Serial/JTAG ROM Message Printing Control	LP_AON_STORE4_REG[0]	EFUSE_DIS_USB_SERIAL_JTAG_ROM_PRINT
Enabled*	0*	0*
Disabled	0	1
	1	Ignored

*marks the default value and configuration.

3.3.5. JTAG Signal Source Control

The strapping pin GPIO7 can be used to control the source of JTAG signals during the early boot process. This pin does not have any internal pull resistors and the strapping value must be controlled by the external circuit that cannot be in a high impedance state.

GPIO7 is used in combination with EFUSE_DIS_PAD_JTAG,EFUSE_DIS_USB_JTAG, and EFUSE_JTAG_SEL_ENABLE.

JTAG Signal Source	eFuse 1[1]	eFuse 2[2]	eFuse 3[3]	GPIO7
USB Serial/JTAG Controller[*5]	0*	0*	0*	X[4]
			1	1
JTAG pins MTDI, MTCK, MTMS, and MTDO				0
	0	x	x	x
	0	1	x	x
USB Serial/JTAG Controller	1	0	x	x
JTAG is disabled	1	1	x	x
	1	x	x	x

*marks the default value and configuration.

[1]eFuse 1：EFUSE_DIS_PAD_JTAG

[2]eFuse 2：EFUSE_DIS_USB_JTAG

[3]eFuse 3：EFUSE_JTAG_SEL_ENABLE

[4]x: x indicates that the value has no effect on the result and can be ignored

4. Electrical Characteristics

4.1.Absolute Maximum Limit Value

Exceeding the absolute maximum ratings may result in permanent damage to the device. This is an emphasized rating only and does not address the functional operation of the device under these or other conditions beyond those indicated in these specifications. Prolonged exposure to absolute maximum rating conditions may affect module reliability.

4.2.Power Consumption Characteristics

update soon

4.3.Recommended Working Conditions

Parameter	Description	Min	Typ	Max	Unit
VCC	Power pin voltage	3	3.3	3.6	V
I_{VCC}	Supply current from external power supply	0.5	-	-	A
T_A	Operating Temperature	-40	-	85	℃

5. WT013261-S5 Schematic

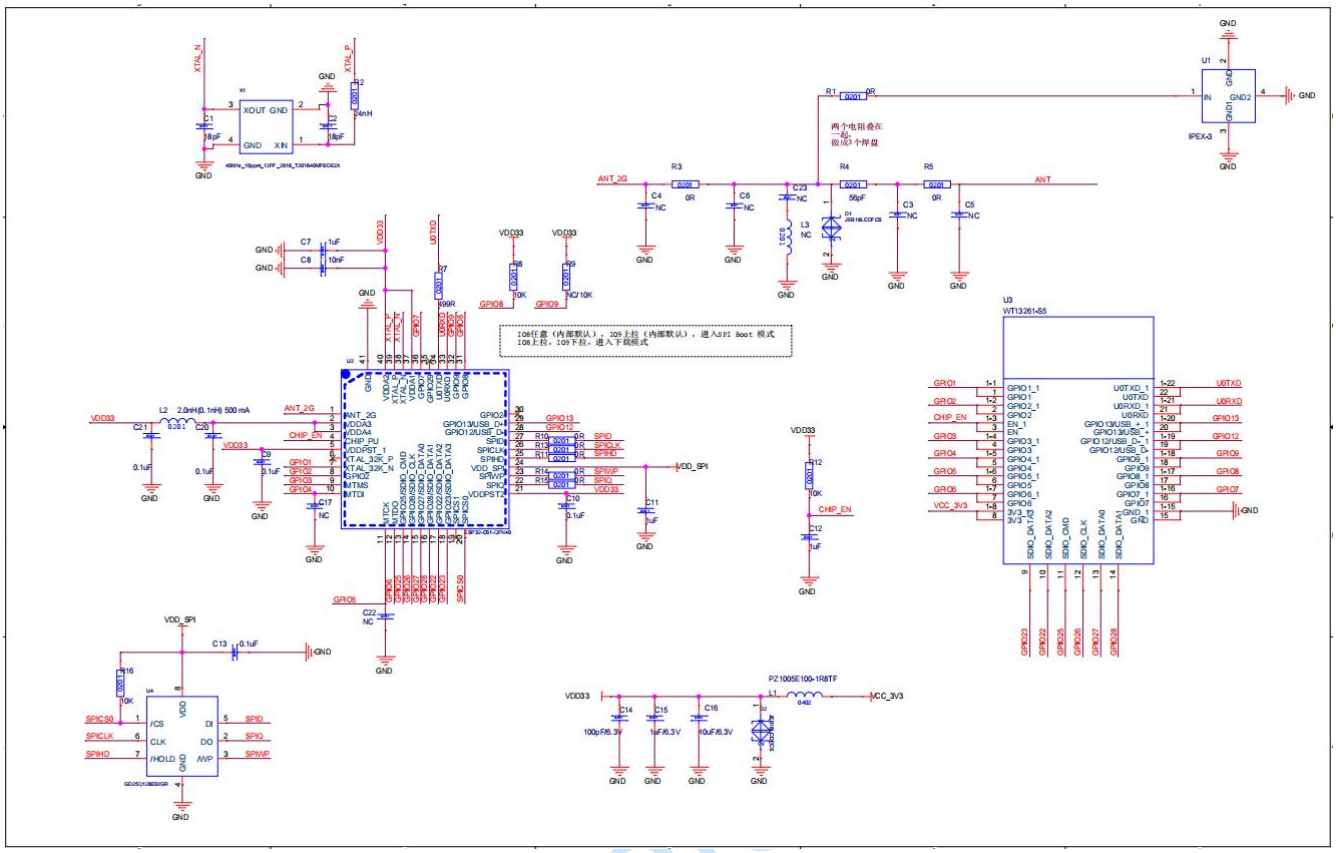

Figure 9: WT013261-S5 Schematic

6. WT013261-S5 Dimensions

The following figure shows the top view and front view of WT013261-S5 with a tolerance of ±0.2 mm.

Unit:mm

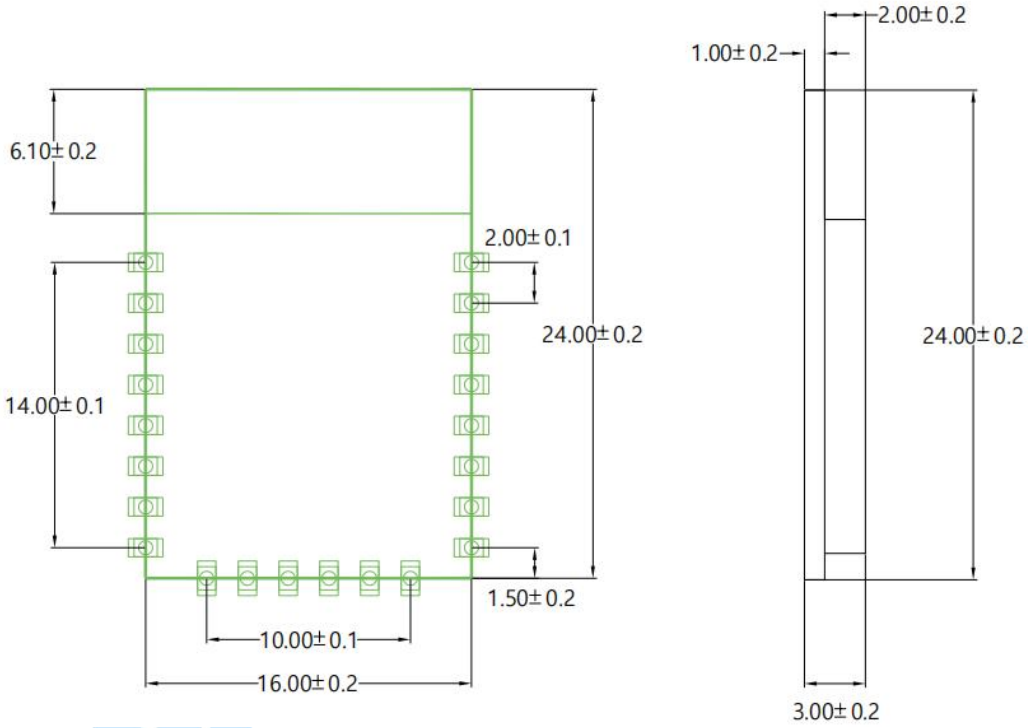

Figure 10: Dimension figure of WT013261-S5

7. Storage Condition

Prerequisite	Parameters
Storage condition	Non-condensing atmosphere < 40℃ /90 %RH in sealed MBBs
Conditions of use	168 hours at 25 ± 5℃ , 60 % RH.
Moisture sensitivity	3 levels

8. Reflow Soldering Curve

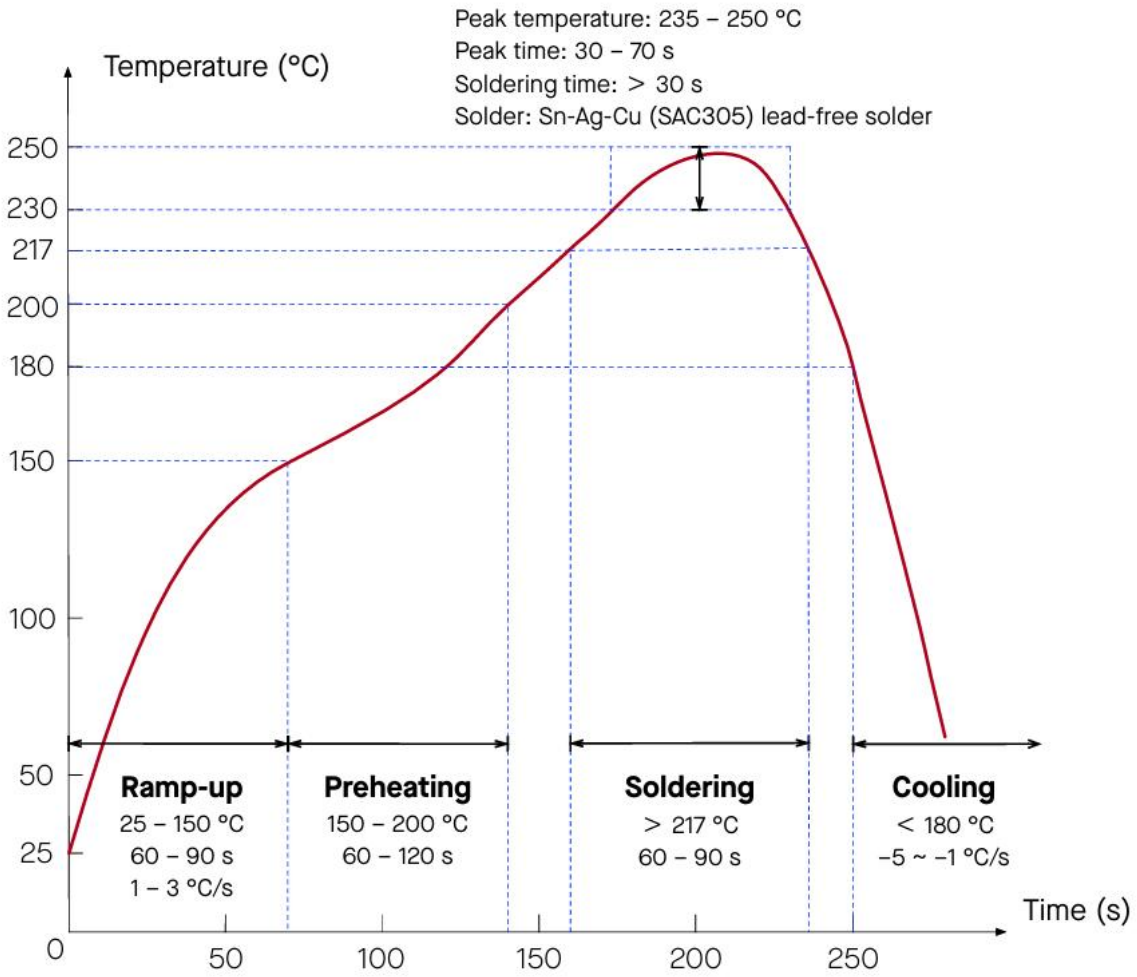

Figure 11: Reflow Soldering Temperature Curve

9. Contact Us

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