WT018684-S5 series Datasheet

Version V1.0.4

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Wireless-Tag

2.4GHz Wi-Fi(802.11b/g/n)+Bluetooth 5(LE) module
Built-in ESP8684 series chip, single-core 32-bit RISC-V processor
Flash up to 4MB
Rich peripheral on-board PCB antenna and external antenna connectors

Ordering Model	built-in chip	Flash (MB)	PSRAM (MB)	connection with high-ranking officials
WT018684-S5-N2	ESP8684	2	0	PCB
WT018684-S5-N2X	ESP8684	2	0	PCB
WT018684-S5-N4	ESP8684	4	0	PCB
WT018684-S5-N4X	ESP8684	4	0	PCB
WT018684-S5U-N2	ESP8684	2	0	IPEX
WT018684-S5U-N2X	ESP8684	2	0	IPEX
WT018684-S5U-N4X	ESP8684	4	0	IPEX

About this document

This document provides user specifications for WT018684-S5 Series.

Document version

Please download the latest version of the document from the Qiming website

revision history (of a document, web page etc)

Please go to the document revision page to view the revision history

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instructions

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Revision History

No.	Version	Changes	Notes	Editor	Date
1	V1.0.0	C	Creating Documents	GUO	2022-4-25
2	V1.0.1	M	Erratum, corrigendum 5.1	GUO	2022-7-8
3	V1.0.2	A	Add Pin Descriptions	Zeng	2023-8-3
4	V1.0.3	A	Add pin descriptions and physical diagrams	Zeng	2023-10-26
5	V1.0.4	M	1. Updated the pinout and module physical diagram 2. Updated the ordering part numbers 3. Updated the module dimension drawing	Wang	2025-11-26

*Changes：C——create，A——add，M——modify，D——delete

CONTENTS

1. Module Overview

1.1 Characteristics

MCU

- Built-in ESP8684 series chip, 32-bit RISC-V single-core processor, support up to 120 MHz clock frequency
- 576 KB ROM
- 272 KB SRAM (16 KB dedicated to cache)
- SIP flash
- Flash controllers that introduce a cache mechanism
- Support flash in circuit becomes (ICP)

Wi-Fi

- Supports IEEE 802.11 b/g/n protocols
- Supports 20 MHZ bandwidth in the 2.4GHZ band
- Supports 1T1R mode with data rate up to 72.2Mbps
- Data rates up to 72.2 Mbps in 802.11n mode
- Frame Aggregation (TX/RX A-MPDU, TX/RX A-MSDU)
- Immediate Block ACK (Immediate Block Acknowledgement)
- Fragmentation and defragmentationaion
- Transmit opportunity (TXOP)
- Automatic Beacon monitoring (hardware TSF)
- Wireless Multimedia (WMM)
- 3 x virtual Wi-Fi ports
- Antenna subplot
- Support for external power amplifiers
- Simultaneously supports Infrastructure BSS Station mode, SoftAP mode, Station + SoftAP mode, and hybrid mode.

  Please note that when the ESP8684 series is scanning in Station mode, the SoftAP channel will change at the same time.

bluetooth

- Bluetooth LE (Low Power): Bluetooth 5
- High Power Mode
- Rate support 125kbps, 500kbps, 1Mbps, 2Mbps
- Advertising Extensions
- Multiple Broadcasts (Multiple Advertisement Sets)
- Channel Selection (Channel Selection Algorithm #2)
- Wi-Fi and Bluetooth coexist, share the same antenna

software

- Peripheral interfaces: 14 GPIO ports, 3xSPI, 2xUART, I2C host, LED PWM controller with up to six channels, general purpose DMA controller (GDMA), one receive channel and one transmit channel
- Analogue interface: 1x 12-bit SAR analogue/digital converter. Up to 5 channels, 1x temperature sensor
- Timer: 1x54-bit general-purpose timer, 2x watchdog timers, 1x52-bit system timer

1.2 Description

The two module core processor chips, WT018684-S5 and WT018684-S5U, ESP8684, are highly integrated, low-power Wi-Fi and Bluetooth System-on-Chips (SoCs) designed for Internet of Things (IoT), mobile devices, wearable electronics, and smart home applications, such as wake word detection and voice command recognition, face detection and recognition, smart home, smart home appliances, smart control panels, smart speakers, and more. The ESP8684 chip features industry-leading low-power and RF performance and supports Wi-Fi IEEE802.11b/g/n protocol and BLE 5.0. The chip is equipped with a RISC-V 32-bit single-core processor with an operating frequency of up to 120MHz, which allows the user to turn off the

CPU and use the low-power co-processor to monitor the status of peripheral devices or whether certain analogue quantities exceed thresholds. The user can switch off the CPU and use the low-power co-processor to monitor the status change of peripherals or whether certain analogue quantities exceed the threshold. Supports secondary development without using other microcontrollers or processors. The chip supports a variety of low-power operating states to meet the power requirements of various application scenarios. The chip's unique features such as fine clock gating, dynamic voltage clock frequency adjustment, and adjustable RF output power can achieve the best balance between communication distance, communication rate and power consumption.The WT018684-S5 and WT018684-S5U modules provide a rich set of peripheral interfaces, including UART, SPI, I2C, ADC, temperature sensor, GPIOs, LED PWM controllers, GDMA, analogue-to-digital converters, temperature sensors, general-purpose timers and watchdogs.

The WT018684-S5 and WT018684-S5U modules feature a variety of unique hardware security mechanisms and hardware cryptographic accelerators that support AES, SHA and RSA algorithms. The RNG, HMAC and Digital Signature modules provide additional security features. Other security features include Flash encryption and se-cure boot signature verification. The complete security mechanism makes the chip perfect for a variety of cryptographic products.The WT8684-S5 module supports low-power Bluetooth: Bluetooth5, Bluetooth mesh.Bluetooth rate support: 125Kbps, 500Kbps, 1Mbps, 2Mbps.Support for Broadcast Extension, Multi-broadcasting, Channel Selection WT018684-S5 and WT018684-S5. WT018684-S5U is a general-purpose Wi-Fi + low-power Bluetooth MCU module, equipped with ESP8684 series chips.

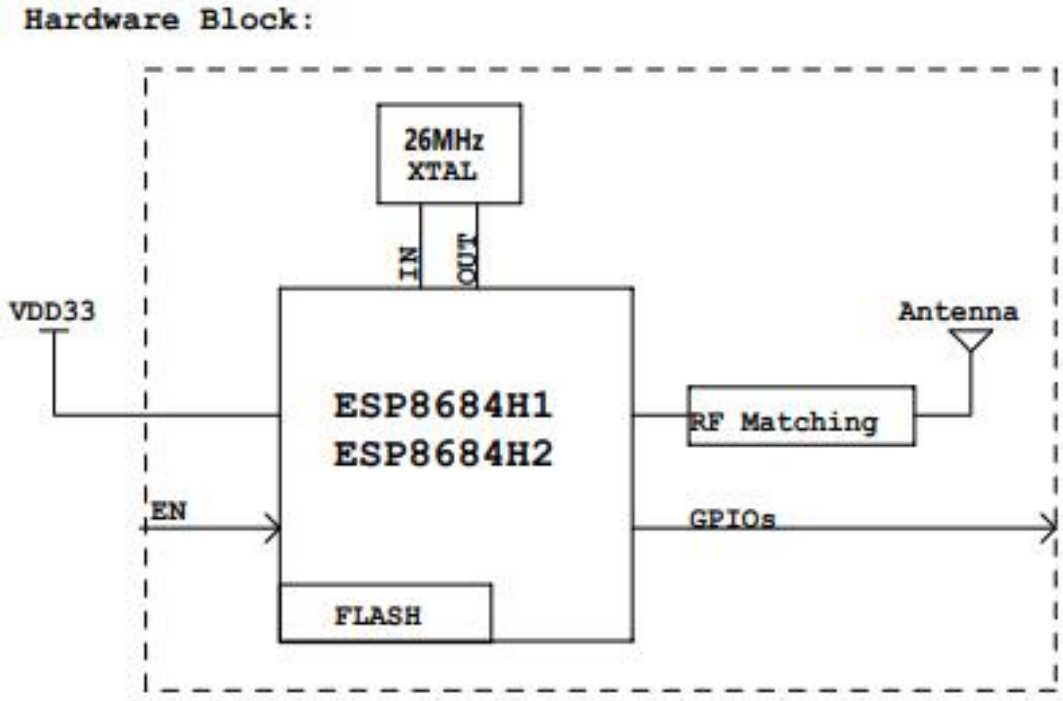
1.3 Applications

- General Purpose Low Power IoT Sensor Hub
- General Purpose Low Power IoT Data Logger
- Camera Video Streaming
- OTT TV box/set-top box

- equipment
- speech recognition
- image recognition
- Mesh Networks
- home automation
- Smart Home Control Board
- Smart Buildings
- industrial automation
- intelligent agriculture
- sound card
- Health/medical/nursing
- Wi-Fi toys
- Wearable Electronics
- Retail & Catering
- Smart POS Applications
- Intelligent door locks

2. hardware block diagram

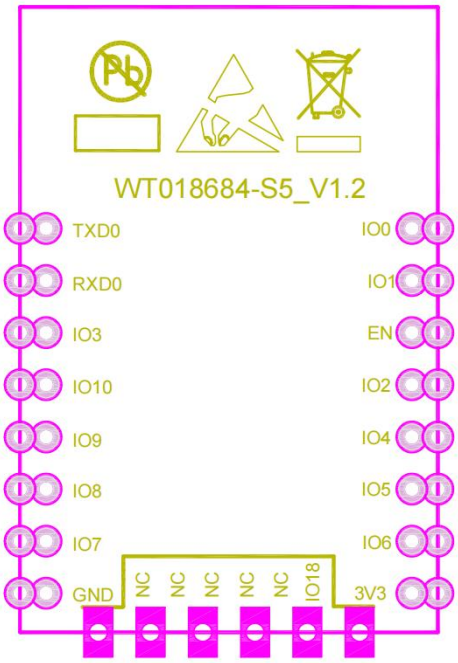
Figure 1 Hardware block diagram



3. Pin Definitions

3.1 Pin Layout

Figure 2 Pin Layout



3.2 Module Physical Drawing

Figure 3 WT8684-S5 Physical Drawing

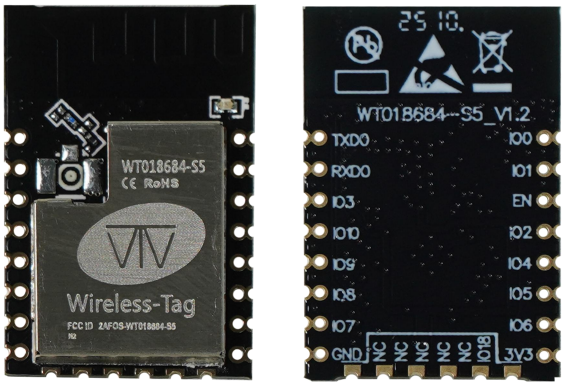
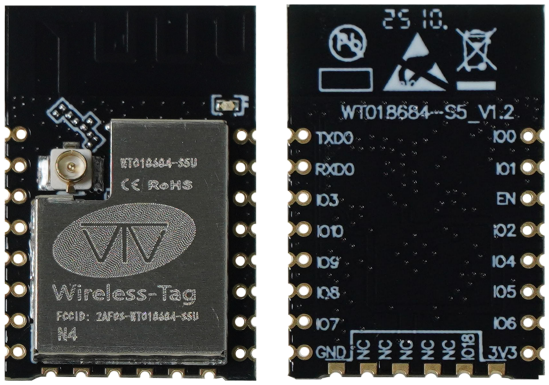


Figure 4 WT8684-S5U Physical Drawing



3.3 Pin Description

Table 1 Pin Definitions and Descriptions

serial number	name (of a thing)	typology	power domain	functionality
1	IO0	I/O/T	VDD3P3_RTC	GPIO0,ADC1_CHO
2	IO1	I/O/T	VDD3P3_RTC	GPIO1,ADC1_CH1
3	EN	I	VDD3P3_RTC	High: Chip enable Low: Chip off Be careful not to leave the CHIP_EN pin floating!
4	IO2	I/O/T	VDD3P3_RTC	GPIO2,ADC1_CH2, FSPIQ
5	IO4	I/O/T	VDDP3_CPU	GPIO4,ADC1_CH4,FSPIHD,MTMS
6	IO5	I/O/T	VDDP3_CPU	GPIO5,FSPIWP,MTDI
7	IO6	I/O/T	VDDP3_CPU	GPIO6,FSPICLK,MTCK
8	3V3	PA	-	analogue power supply
9	IO18	I/O/T	VDD3P3_CPU	GPIO18
10	NC	I/O/T	-	Overhanging pins
11	NC	-	-	pin empty (of piping)
12	NC	-	-	pin empty (of piping)
13	NC	-	-	pin empty (of piping)
14	NC	-	-	pin empty (of piping)
15	GND	G	-	earth (electric connection)
16	IO7	I/O/T	VDDP3_CPU	GPIO7,FSPID,MTDP
17	IO8	I/O/T	VDDP3_CPU	GPIO8
18	IO9	I/O/T	VDDP3_CPU	GPIO9
19	IO10	I/O/T	VDDP3_CPU	GPIO10,FSPICSO
20	IO3	I/O/T	VDDP3_CPU	GPIO3,ADC1_CH3
21	RXDO	I/O/T	VDDP3_CPU	GPIO19,U0RXD
22	TXDO	I/O/T	VDDP3_CPU	GPIO20,U0TXD

Table 2 Factory Default AT Command Communication Pins

serial number	name (of a thing)	functionality
7	GPIO6	RX
12	GPIO7	TX

PA:Analogue power supply
PD:Digital IO power supply
I:Input
O:Output
T: can be set to high resistance
The pin functions in this table only refer to some fixed settings, the signals that can be input and output through GPIO matrix are not limited by this table.

3.4 Strapping Pins

There are two Strapping pins on the ESP8684 family of chips.

- GPIO8
- GPIO9

The software can read the GPIO_STRAPPING field of the GPIO_STRAP_REG register to get the values of GPIO8 and GPIO9. During the system reset of the chip, the Strapping pin samples the level on its own pin and stores it in a latch with a value of "0" or "1" and keeps it until the chip is powered down or turned off.
There are several types of system resets:

- Power-on reset
- RTC Watchdog Reset
- Undervoltage reset
- Analogue Super Watchdog reset

GPIO9 is connected to internal weak pull-up by default, if there is no external connection on this pin or the connected external line is in high impedance state, the latch value is "1".
To change the value of Strapping, you can apply an external pull-down or pull-up resistor, or you can apply the host MCU's GPIOs to control the level of the Strapping pin during power-on reset of the ESP8684 series chips.
After reset release, the Strapping pin functions the same as the normal pin.
Refer to Table 3 for detailed startup modes for configuring Strapping pins.

Table 3 Strapping Pins

system boot mode			
pin	default (setting)	SPI boot mode	Download Launch Mode
GPIO8	not have	irrelevant item	1
GPIO9	Internal weak pull-up	1	0
Control ROM Code printing during system startup			
pin	default (setting)	functionality	
GPIO8	not have	When the EFUSE_UART_PRINT_CONTROL field of eFuse is 0 (initial default value), power-on printing is normal and not controlled by GPIO8. 1, if GPIO8 is 0, power-on normal printing; if GPIO8 is 1, power-on no printing. 2, if GPIO8 is 0, power-on does not print; if GPIO8 is 1, power-on prints normally. When 3, power-up does not print and is not controlled by GPIO8.	

GPIO8=0 and GPIO9=0 is not available.

Figure 3 shows the build time and hold time of the Strapping pin before and after power-up of CHIP_EN, with each parameter shown in Table 3.

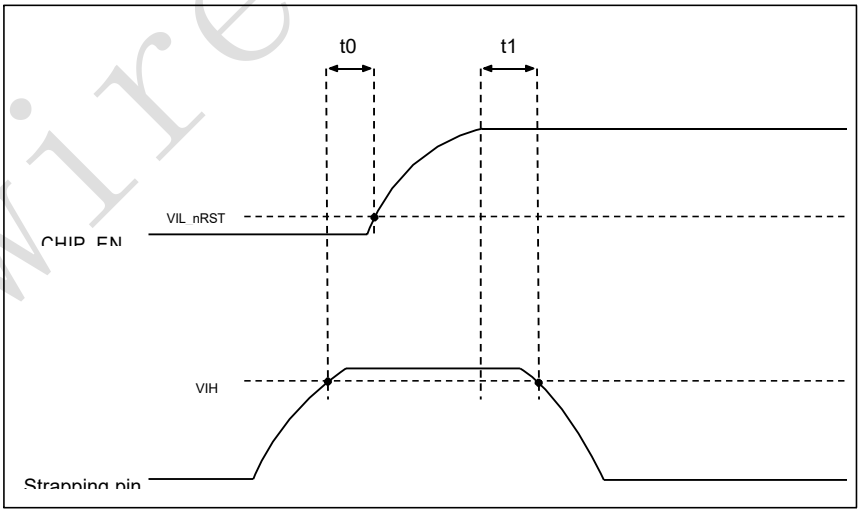


Table 4 Parameter descriptions of build-up and hold times for Strapping pins

parametric	instructions	Minimum (ms)

t_0	CHIP_EN Establishment time before power-up	0
t_1	CHIP_EN Hold time after power up	3

4. Electrical Characteristics

4.1 Absolute maximum ratings

Exceeding the absolute maximum ratings may result in permanent damage to the device, this is an emphasised rating and does not relate to the functional operation of the device.

Table 5 Absolute maximum ratings

notation	**parametric**	**minimum value**	**maximum values**	**unit (of measure)**
VDDA3P3, VDDA, VDD3P3_RTC, VDD3P3_CPU	**Power Pin Voltage**	**-0.3**	**3.6**	**V**
TSTORE	**Storage temperature**	**-40**	**150**	℃

4.2 Recommended working conditions

Table 6 Recommended working conditions

notation	parametric	minimum value	typical value	maximum values	unit (of measure)
vdda3p3,vdda,vdd3p3_rtc,vdd3p3_cpu	Power Pin Voltage	3.0	3.3	3.6	V
IVDD 2	Supply current from external power supply	0.5	-	-	A
TA	Working environment temperature	-40	-	105	℃

VDD3P3_CPU should not exceed 3.3v when writing eFuse.

When using a single power supply, the output current needs to be 500mA and above.

5. Application Notes

5.1 Module Size

Fig. 5 Module size (back view)

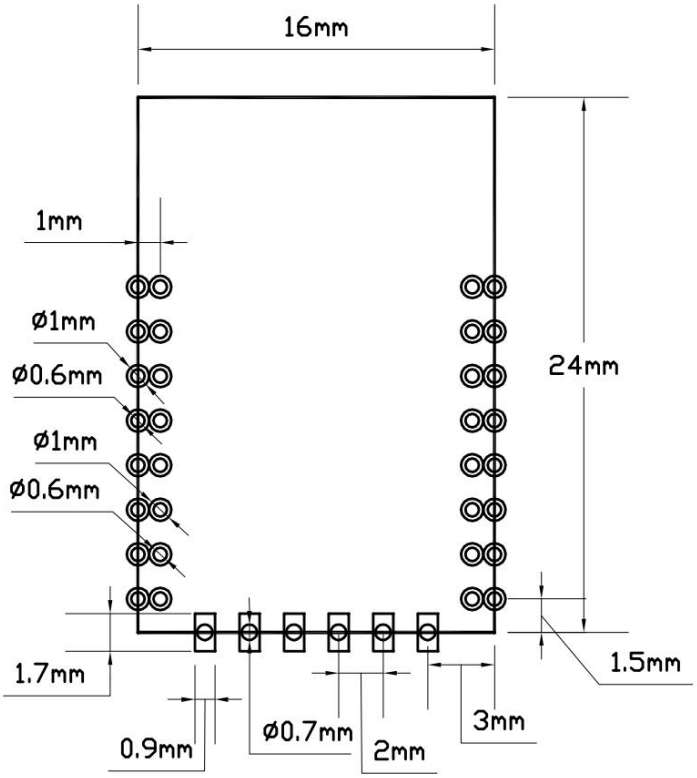
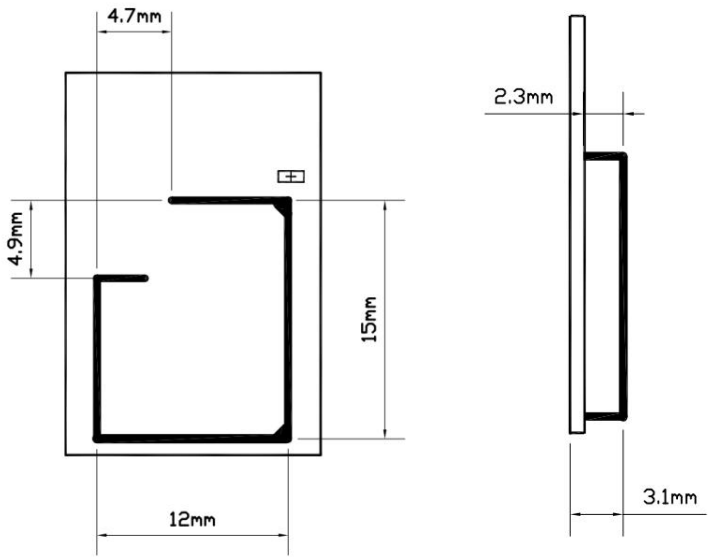
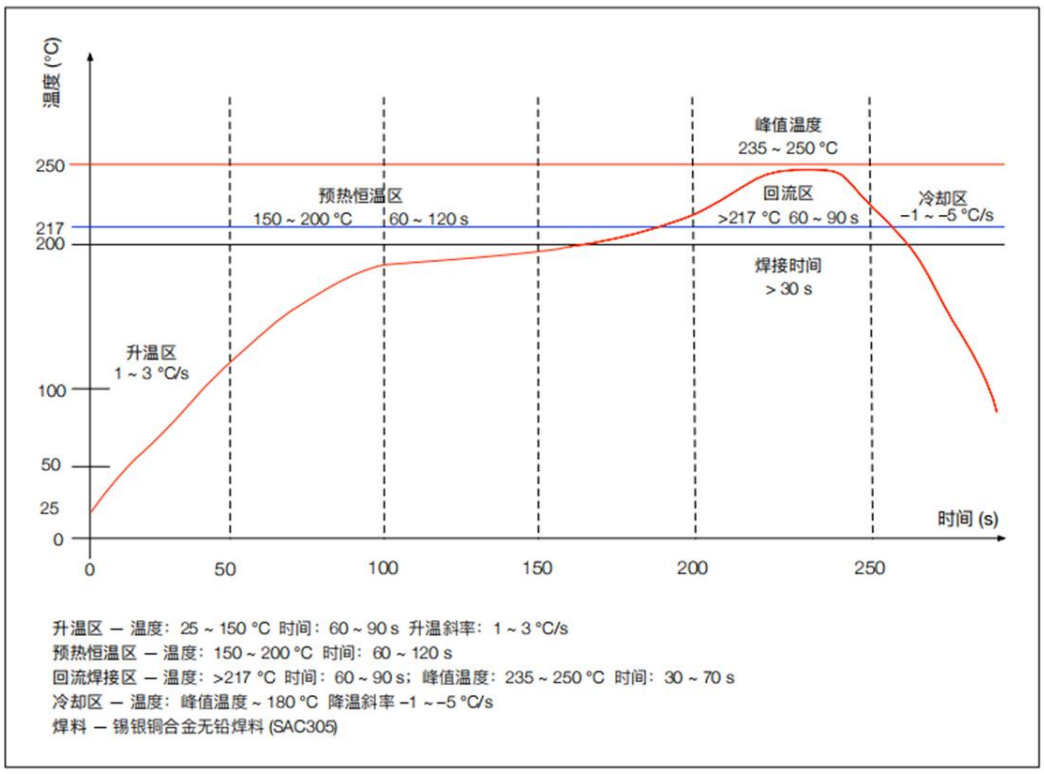


Fig. 6 Module size (front view) Figure 7: Side View



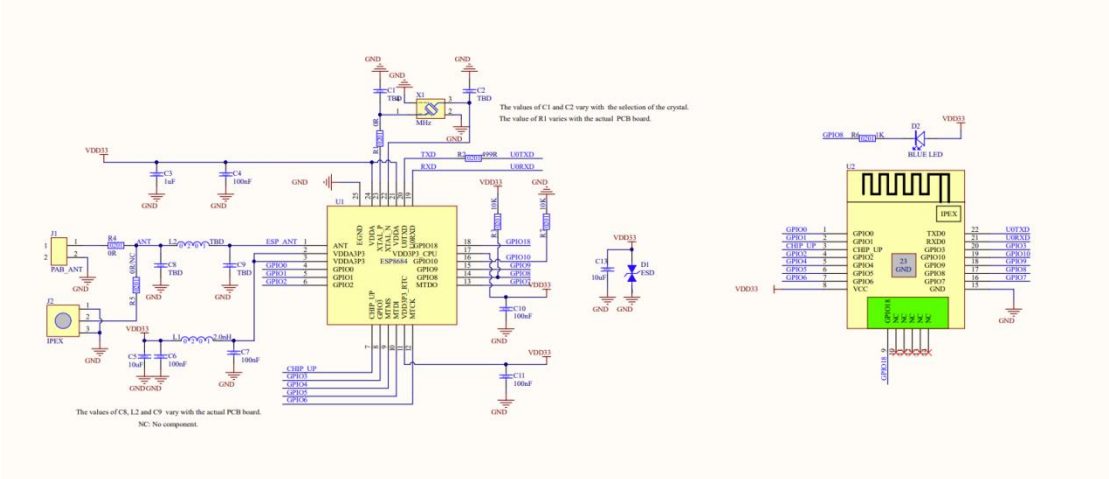
5.2 Reflow Profile

Fig. 8 Reflow profile



5.3 Module Schematic

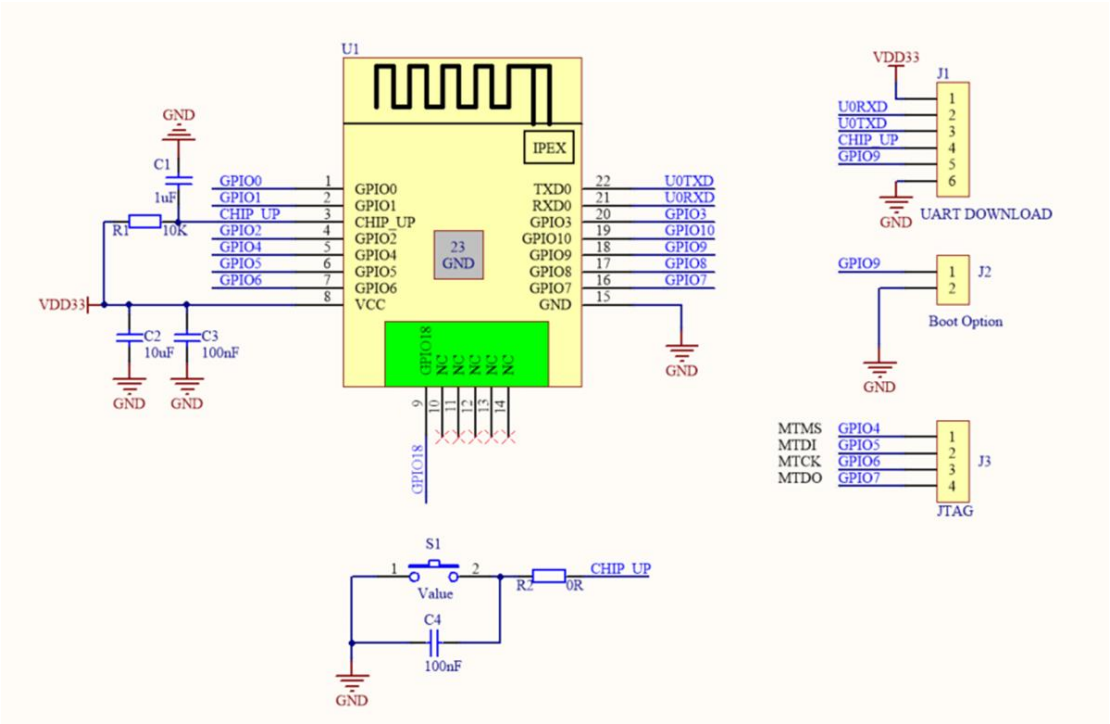
Fig. 9 Module schematic diagram



5.4 Peripheral Design Schematic

Application circuit diagram for connecting the module to peripheral devices (e.g. reset button, JTAG interface, UART interface, etc.).

Fig. 10 Schematic diagram of peripheral design



6. Product Trial

-Sales email: sales@wireless-tag.com

-Technical support email: technical@wireless-tag.com