WT0132C5-S6/WT0132C5-S6U

Datasheet

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Revision History

Version	Modifier By	Date	Reason	Main changes
V1.0	Pail	2024.8.15	Creation	Creat Document

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1. Overview

WT0132C5-S6 series module is an integrated dual-band Wi-Fi & BLE module designed based on Espressif ESP32-C5 series chipset launched by Wireless-Tag Technology Co.,Limited.WT0132C5-S6 supports 2.4 & 5G dual-band Wi-Fi6 (802.11ax), Bluetooth® 5 (LE), Zigbee and Thread (802.15.4), with powerful features, rich peripheral interfaces, and antenna support for on-board PCB antenna or I-PEX (3rd generation) RF coaxial connector, designed for Internet of Things (IoT), industrial automation, healthcare, and consumer electronics applications.

The WT0132C5-S6 utilizes a PCB mounted antenna and the WT0132C5-S6U utilizes a connector to attach an external antenna. Both modules are available in a variety of models, as shown in Tables 1 and 2.

Table 1: WT0132C5-S6 Series Model Comparison

Module Model	Flash	PSRAM	Module Size (mm)
WT0132C5-S6-N4	4 MB	-	27.00*16.00
WT0132C5-S6-N8	8 MB	-	
WT0132C5-S6-N16	16 MB	-	
WT0132C5-S6-N4R4	4 MB	4 MB	
WT0132C5-S6-N8R4	8 MB	4 MB	
WT0132C5-S6-N16R4	16 MB	4 MB	

Table 2: WT0132C5-S6U Series Model Comparison

Module Model	Flash	PSRAM	Module Size (mm)
WT0132C5-S6U-N4	4 MB	-	27.00*16.00
WT0132C5-S6U-N8	8 MB	-	
WT0132C5-S6U-N16	16 MB	-	
WT0132C5-S6U-N4R4	4 MB	4 MB	
WT0132C5-S6U-N8R4	8 MB	4 MB	
WT0132C5-S6U-N16R4	16 MB	4 MB	

CPU and On-Chip Memory

- Built-in ESP32-C5 series chip, 32-bit RISC-V single-core processor, supporting 240MHz clock frequency
- 320KB ROM
- 384KB HP SRAM
- 16KB LP SRAM
- SIP flash

Wi-Fi

- Operates in 2.4 & 5 GHz Dual Band, 1T1R
- Operating channel center frequency range: 2412 ~ 2484 MHz, 5160 ~ 5885 MHz
- Compatible with IEEE 802.11ax protocol: 20MHz non-access point mode of operation only
- Compatible with IEEE 802.11ac protocol: supports 20MHz bandwidth
- Fully compatible with IEEE 802.11a/b/g/n protocols: supports 20 MHz and 40 MHz bandwidths with 150 Mbps data rate

Please note that when the ESP32-C5 series is scanning in Station mode, the SoftAP channel will change at the same time.

Bluetooth®

- Bluetooth Low Power (Bluetooth LE): Bluetooth 5
- BLE Mesh
- High power mode (20 dBm)
- Rate support 125 kbps, 500 kbps, 1 Mbps, 2 Mbps
- Broadcast Extension
- multibroadcast
- channel selection
- power control
- Bluetooth and 2.4GHz WiFi coexist and share the same antenna

IEEE 802.15.4

- Compatible with IEEE802.15.4-2015 protocols

- Operates in 2.4GHz band, supports OQPSK PHY
- Data rate: 250 Kbps
- Support for Thread 1.3
- Supports Zigbee 3.0

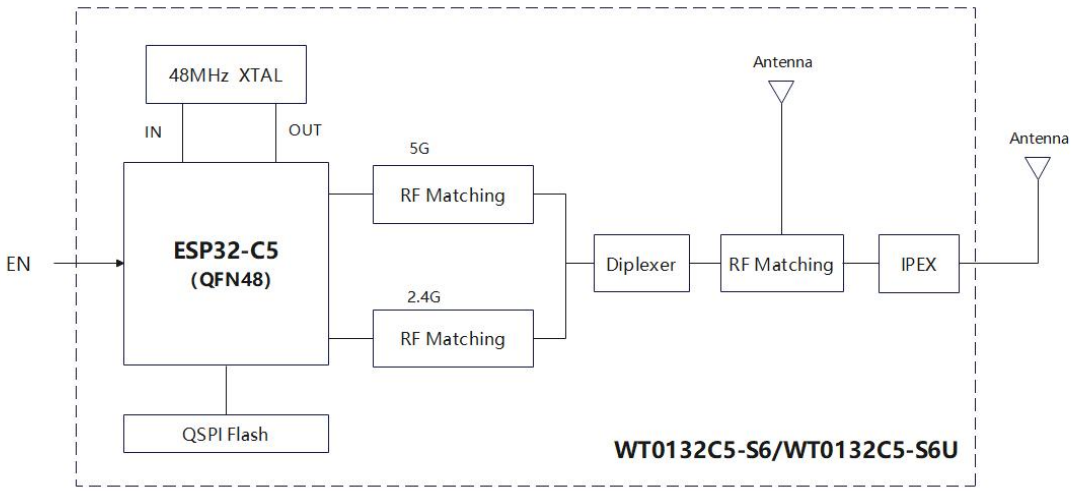
Peripherals

- GPIO, SPI, Parallel IO, UART, I2C, I2S, RMT, LED PWM, ADC, USB Serial/JTAG Controller, etc.

Antenna

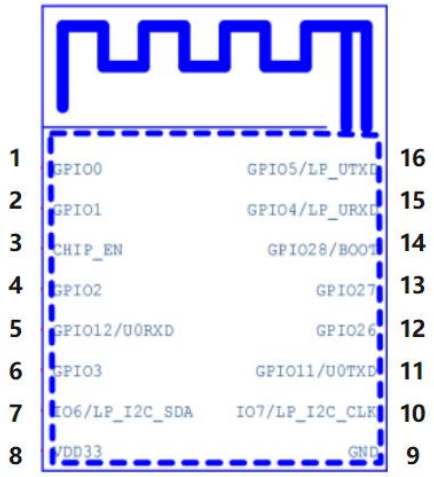
- On-board PCB antenna or external antenna with connectors

2. Functional Block Diagram



3. Hardware Specifications

3.1 WT0132C5-S6/WT0132C5-S6U Pinout & Description



Pinout	Name	Function
1	IO0	GPIO0, XTAL_32K_P, LP_GPIO0, LP_UART_DTRN
2	IO1	GPIO1, XTAL_32K_N, LP_GPIO1, LP_UART_DSRN, ADC1_CH0
3	EN	High: on,enable the chip; Low: off,the chip powers off; Note: Do not leave the EN pin floating.
4	IO2	GPIO2, MTMS, LP_GPIO2, LP_UART_RTSN, ADC1_CH1, FSPIQ
5	RXD0/IO12	U0RXD, GPIO12
6	IO3	GPIO3, MTDI, LP_GPIO3, LP_UART_CTSN, ADC1_CH2
7	LP_I2C/IO6	LP_I2C_SDA, LP_GPIO6, GPIO6, ADC1_CH5, FSPICLK
8	3V3	electricity supply
9	GND	grounding
10	LP_I2C/IO7	LP_I2C_SCL, LP_GPIO7, GPIO7, FSPID
11	TXD0/IO11	U0TXD, GPIO11
12	IO26	GPIO26
13	IO27	GPIO27
14	BOOT/IO28	GPIO28
15	LP_RXD/IO4	LP_UART_RXD, LP_GPIO4, GPIO4, MTCK, ADC1_CH3, FSPIHD
16	LP_TXD/IO5	LP_UART_TXD, LP_GPIO5, GPIO5, MTDO, ADC1_CH4, FSPIWP

3.2 Strapping Pins

At each startup or reset, a module requires some initial configuration parameters, such as in which boot mode to load the module, voltage of flash memory, etc. These parameters are passed over via the strapping pins. After reset, the strapping pins operate as regular IO pins.

The parameters controlled by the given strapping pins at module reset are as follows:

- **Chip boot mode** - GPIO27 and GPIO28
- **ROM messages printing** - GPIO27
- **JTAG signal source** - GPIO7

- **Crystal frequency selection** - MTMS (only available in Joint Download Boot mode)

GPIO28 connects to the chip's internal weak pull-up resistor during chip reset. If the GPIO28 pin has no external connection or the connected external line is in high impedance state, the internal weak pull-up will determine the default value of GPIO28.

Strapping Pin Default Configuration

Strapping Pins	Default Configuration	Bit Value
GPIO27	Floating	-
GPIO28	Pull-up	1
GPIO7	Floating	-
MTMS	Floating	-

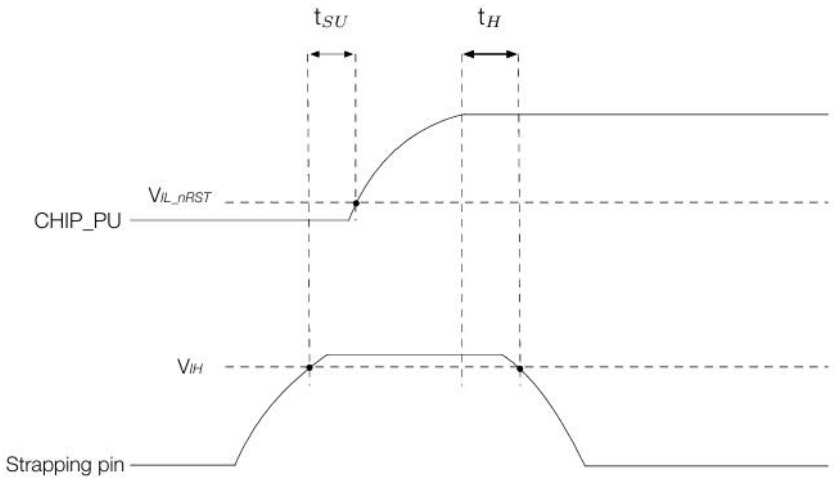
To change the value of the strapping pin, connect an external pull-down/pull-up resistor.

All strapping pins have latches. Upon system reset, the latches sample and store the values of the strapping pins and hold them until the chip is powered down or turned off. The state of the latch cannot be changed in any other way. Therefore, the value of the strapping pin is always readable while the chip is in operation and can be used as a normal IO pin after a chip reset.

The signal timing of the strapping pins needs to follow the build-up and hold times shown in the table below and in the figure below.

Parameters	Description	Min(ms)
t_{SU}	Establishment time, the time it takes for the power rails to stabilize before pulling up CHIP_PU to activate the chip	0
t_{H}	Holding time, i.e., the time when the value of the strapping pin can be read before CHIP_PU is pulled high and the strapping pin is changed to a normal IO	3

	pin.	



3.3 Chip Boot Mode Control

GPIO27 and GPIO28 control the boot mode after the reset is released. See the following table for details.

Boot Mode	GPIO27	GPIO28
default configuration	-(Floating)	1 (Pull-up)
SPI Boot (default)	Any value	1
Joint Download Boot	1	0

Joint Download Boot mode supports the following download methods:

- USB-Serial-JATG Download Boot
- UART Download Boot
- SPI Slave Download Boot

In SPI Boot mode, the ROM bootloader boots the system by reading the program from the SPI flash.

In Joint Download Boot mode, users can download the binary file to flash via UART0, USB or SPI Slave interface, or download the binary file to SRAM and run the program in SRAM.

4. Peripheral Application Design and Considerations

The WT0132C5-S6 module needs to be used to meet basic operating

requirements. This chapter describes how to perform each functional interface circuit design, precautions, and provides a design reference.

4.1 Power Interface

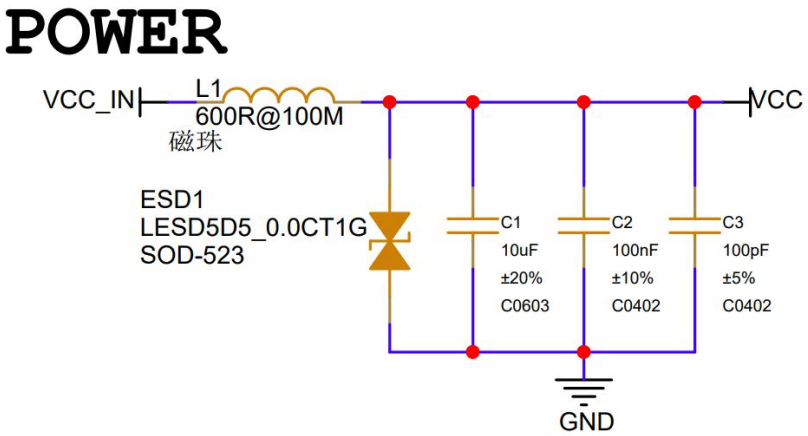
Power supply circuit design and layout, is a very important part of the whole product design, power supply design good or bad affect the performance of the whole product. Please read the power supply design requirements carefully and follow the correct power supply design principles to ensure optimal circuit performance.

Power connector

Pin Name	Pin Number	Functional Description	note
VCC	8	Module power input	3.0-3.6V (Default: 3.3V)
GND	9	Module power supply input ground	Make sure all ground pins are well grounded!

4.2 Power Supply Design

The WT0132C5-S6 power supply power supply supports 3.0-3.6V power input (3.3V typical). The power supply recommended design suggestions are shown below:



Power Supply Design Considerations :

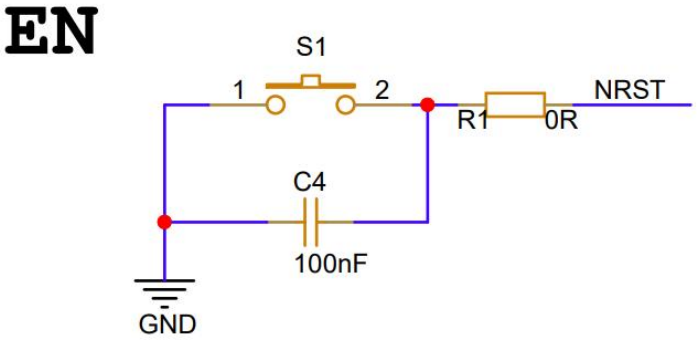
- It is recommended to place a magnetic bead L1 on the power input

to filter out power supply high frequency noise.

- Module power supply maximum input voltage 3.6V, typical value is 3.3V; VCC recommended alignment width ⩾ 0.5mm or more.
- It is recommended to increase the ESD tube at the module power supply, ESD clamp operating voltage VRWM = 5V, need to be placed close to the power input interface to ensure that the power supply surge voltage into the back-end circuits before that is clamped, to protect the back-end devices and modules;
- C1 can choose 10uF aluminum electrolytic capacitor or ceramic capacitor, can improve the power supply instantaneous high-current current capacity, capacitance withstand voltage value should be greater than the input power supply voltage of more than 1.5 times;
- Place low ESR bypass capacitors C2 and C3 near the module position to filter out high frequency interference in the power supply;

4.3 Enabling Interfaces

The enable EN pin of the module is 3 pins, which is connected to the chip CHIP_PU, and the module has an internal 10K pull-up, which can also be used to realize reset through the enable pin. After the module is powered on, the EN pin is enabled high by default, and the module can be reset when the EN pin input is low under the normal working condition of the module. If you need to press the key to reset, please refer to the following figure, it is recommended to connect a 100nF capacitor in parallel with the key to filter out the level jitter after the key is triggered.



4.4 Peripheral Interfaces

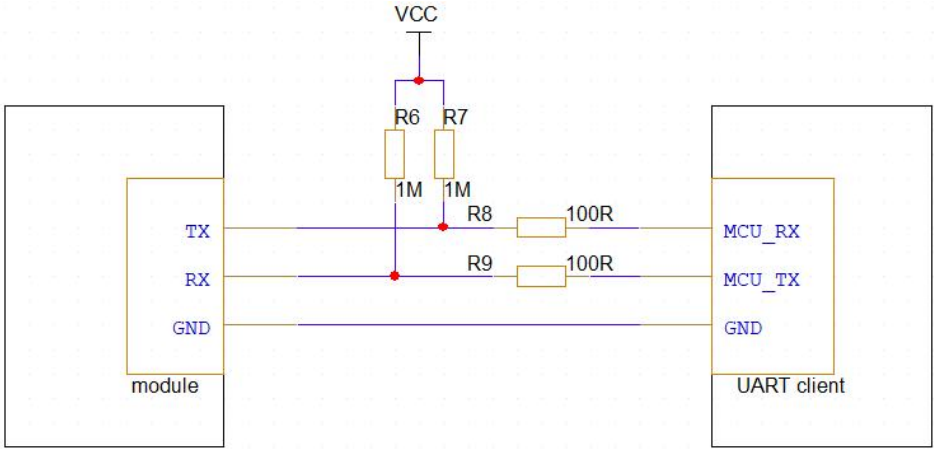
Module provides a variety of commonly used peripheral interfaces

Serial Port Interface

Pin Name	Pin Number	Functional Description	note
RXD0	5	serial port reception	Firmware Download
TXD0	11	serial port sending	Firmware Download
LP_RXD/IO4	15	serial port reception	Low Power Serial Port
LP_TXD/IO5	16	serial port sending	Low Power Serial Port

The module can realize data communication and debugging and other functions through the serial port. Customers can choose to use it according to their needs. The recommended serial port connection circuit is shown in Figure 5. It is recommended to reserve the pull-up resistor to prevent the chip from insufficient serial communication drive capability, and it is recommended to connect 100 ohm current limiting resistors in series with RXD and TXD signal lines to prevent pulse current and burn the chip.

Serial Connection Reference Design



Serial Port Schematic Design Considerations:

- Note the correspondence of the signal flow to the connection.
- Module serial port level is 3.3V, if the UART and MCU logic level does not match, you need to do level conversion

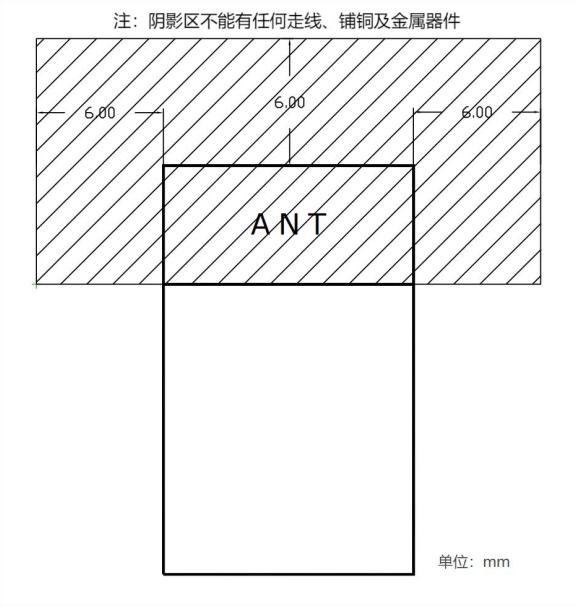
4.5 RF Design Considerations

The WT0132C5-S6 module uses an on-board PCB antenna, and the WT0132C5-S6U module uses an antenna connector with a third-generation IPEX base, both of which are in an area outside the shield. The module antenna area should be near the edge of the product.

The on-board antenna will be affected by the customer's base plate, resulting in resonance frequency shift, if the communication distance requirements are very high, the customer needs to prepare a finished product that has already been finalized with modules, and submit it to our company for testing and verification. The reference layout is shown in the figure below:

RF Reference Layout Diagram 1

RF Reference Layout Diagram 2



5. Electrical Characteristics

5.1 Absolute Maximum Ratings

Exceeding the absolute maximum ratings may result in permanent damage to the device. This is an emphasized rating only and does not address the functional operation of the device under these or other conditions that exceed the recommended operating conditions specifications. Prolonged exposure to absolute maximum rating conditions may affect module reliability.

notation	parameters	minimum value	maximum values	unit (of measure)
VDD33	Power Pin Voltage	-0.3	3.6	V
T_{STORE}	Storage temperature	-40	85	℃

5.2 Recommended Working Conditions

notation	parameters	minimum value	typical value	maximum values	unit (of measure)
VDD33	Power Pin Voltage	3.0	3.3	3.6	V
I_{VDD}	Supply current from	0.5	-	-	A

	external power supply				
T_A	Operating Temperature	-40	-	85	℃

5.3 Wi-Fi Radio Frequency

5.3.1 2.4G Wi-Fi RF Transmitter and Receiver (TX/RX) Specifications

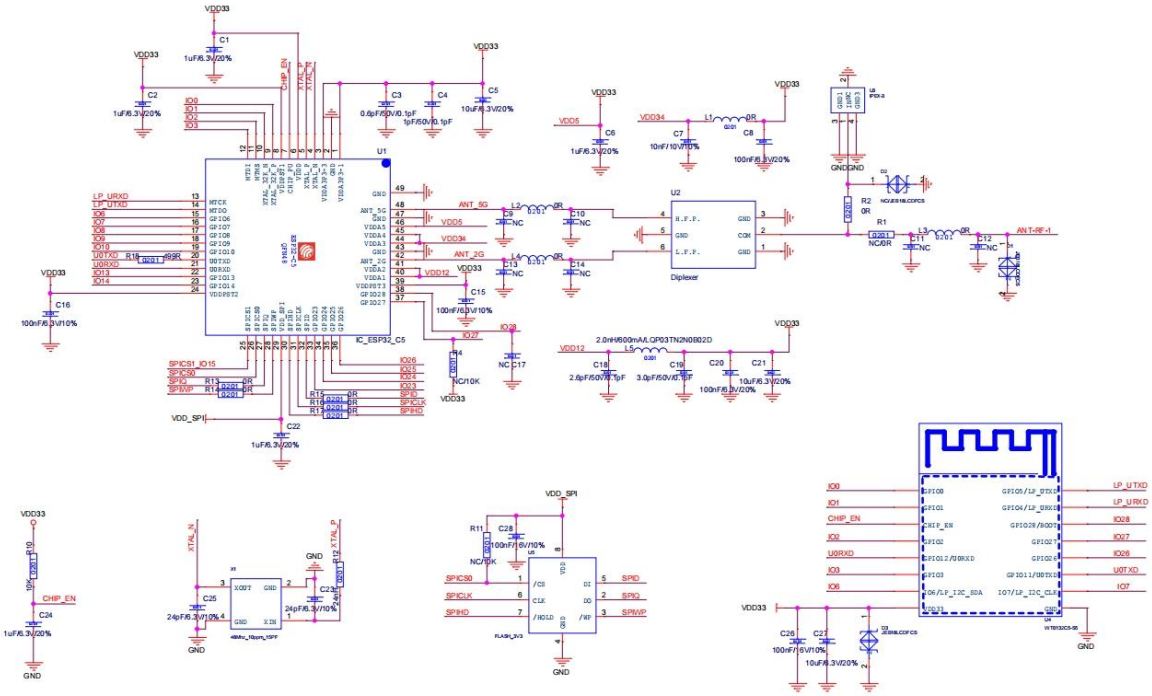
Mode/Rate	Power/dBm	Emission	Receiving
802.11b, 1 Mbps	18.83	-30.95	-100
802.11b, 11 Mbps	18.79	-29.55	-91
802.11g, 6 Mbps	18.7	-23.56	-95
802.11g, 54 Mbps	17.4	-26.21	-78
802.11n, HT20, MCS 0	18.05	-21.33	-95
802.11n, HT20, MCS 7	16.5	-29.17	-78
802.11n, HT40, MCS 0	17.6	-21.67	-93
802.11n, HT40, MCS 7	15.83	-28.79	-75

5.3.2 5G Wi-Fi RF Transmitter and Receiver (TX/RX) Specifications

Mode/Rate	Power/dBm	Emission	Receiving
802.11a, 6 Mbps	15	-23.73	-93
802.11a, 54 Mbps	14.3	-26.12	-76
802.11n, 20M, MCS 0	15.6	-24.55	-93
802.11n, 20M, MCS 7	13.5	-29.88	-73
802.11n, 40M, MCS 0	14.1	-24.97	-90
802.11n, 40M, MCS 7	12.6	-27.67	-72

6. Schematic

6.1 Peripheral Application Circuits



7. Module Dimension Drawing

7.1 Module WT0132C5-S6/WT0132C5-S6U Dimension Drawing