

WTDP4C5-S1

Development Board Guide

Version 1.0

Disclaimer and Copyright Notice

Information in this document, including the URL addresses for reference, is subject to change without notice.

This document is provided "as is" without warranty of any kind, including any warranty of merchantability, fitness for a particular purpose, or non-infringement, and any warranty that any proposal, specification, or sample is referred to elsewhere. This document disclaims all liability, including liability for infringement of any patent, arising out of the use of the information in this document. This document does not grant any license, express or implied, by estoppel or otherwise, to use any intellectual property.

The Wi-Fi Alliance member logo is owned by the Wi-Fi Alliance.

All trade names, trademarks and registered trademarks mentioned herein are the property of their respective owners and are hereby acknowledged.

Notice

The content of this manual is subject to change due to product version upgrade or other reasons. WIRELESS-TAG Technology Co.,limited reserves the right to modify the contents of this manual without any notice or prompting. Ltd. makes every effort to provide accurate information in this manual, but WIRELESS-TAG Technology Co.,limited does not ensure that the contents of the manual are completely free of errors, and all statements, information and recommendations in this manual do not constitute any express or implied warranty.

Revision History

Version	Date	Developed/changed content	Modifier By	Auditor
V1.0	2025-8-27	Creating Documents	Pail	Louie

Contents

1. Development Board Introduction	5
1.1. Development Board Overview	5
1.2. Development Board Pictures	5
1.3. Product Characteristics	5
1.4. Component Introduction	6
1.5. Interface Packaging	8
2. Hardware Reference	8
2.1. Block Diagram	8
2.2. Header Block	8
3. Getting Started	14
3.1. Preliminary	14
3.2. Hardware Setup	14
3.3. Software Setup	14
4. Related Documents	16
5. Contact Us	16

1. Development Board Introduction

1.1. Development Board Overview

The WTDP4C5-S1 development board is designed by Wireless-tag Technology Co., Limited. based on the WT01P4C5-S1 core board. The WT01P4C5-S1 core board integrates Espressif ESP32-P4 and ESP32-C5 chips, featuring a dual-core 360 MHz RISC-V processor and supporting dual-band 2.4G & 5G Wi-Fi 6 (802.11ax). The development board supports USB 2.0, MIPI-CSI, MIPI-DSI, and DC 12V power interfaces, making it ideal for cost-effective, low-power multimedia product development.

Most pins of the core board are routed to headers, allowing developers to easily connect external peripherals via jumpers or use the board on a breadboard.

1.2. Development Board Pictures



Figure 1: WTDKP4C5-S1 Development Board (front)

Figure 2: WTDKP4C5-S1 Development Board (back)

1.3. Product Characteristics

- RISC-V 32-bit dual-core processor with 360 MHz main frequency
 - Core board equipped with Espressif ESP32-P4 and ESP32-C5 dual chips
 - Full-pin development board for ESP32-P4 and ESP32-C5 chips

- Supports dual-band Wi-Fi 6 at 2.4GHz & 5GHz
- Mature Software support, based on ESP-IDF IoT development framework

1.4. Component Introduction

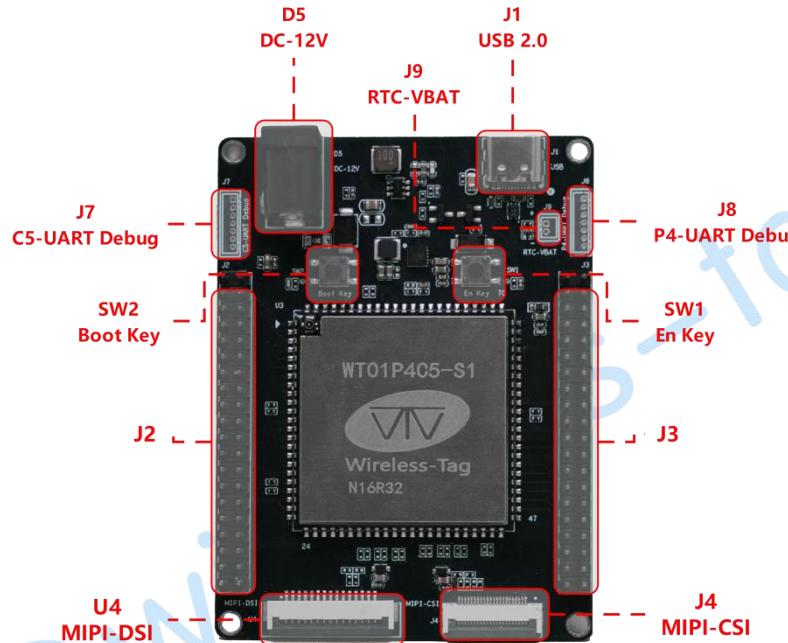


Figure 3: WTDPK4C5-S1 Development Board Component Description

The key components of the board are described in a clockwise direction.

Key Component	Position	Description
DC-12V	D5	DC 12V Power in
RTC-VBAT (NC)	J9	Clock Power Interface (NC)
USB 2.0	J1	The USB 2.0 Port connected to the USB 2.0 OTG High-Speed interface of the ESP32-P4 chip on the WTDPK4C5-S1 core board. When communicating with other devices via this port, ESP32-P4 acts as a USB device connecting to a USB host, which can also be used as the power supply interface of the development board.

P4-UART Debug	J8	P4-UART Debug Interface connects to the ESP32-P4 on the core board via UART. When used with the Wireless-tag programming tool, it enables viewing operational logs or download firmware to the ESP32-P4 chip.
En Key	SW1	Reset key
J3	J3	Part of available GPIO pins are broken out to the header block J3 for easy interfacing. For more details, see Header Block .
MIPI-CSI	J4	MIPI CSI FPC connector is used for connecting external camera module to enable image transmission. FPC specifications: 1.0 mm pitch, 0.3 mm pin width, 0.3 mm thickness, 15 pins.
MIPI-DSI	U4	MIPI DSI FPC connector is used for connecting displays. FPC specifications: 0.5 mm pitch, 0.3 mm pin width, 0.3 mm thickness, 30 pins.
J2	J2	Part of available GPIO pins are broken out to the header block J2 for easy interfacing. For more details, see Header Block .
Boot Key	SW2	The boot mode control button. Press the EN Key while holding down the Boot Key to reset WT01P4C5-S1 and enter firmware download mode. Firmware can then be downloaded to ESP32-P4 via the USB 2.0 Port.
C5-UART Debug	J7	C5-UART Debug Interface connects to the ESP32-C5 on the core board via UART. When used with the Wireless-tag programming tool, it enables viewing operational logs or download firmware to the ESP32-C5 chip.

1.5. Interface Packaging

Interface Description	Package
J7	1.25mm 1x7P
J8	1.25mm 1x7P
J2	2.54mm L11.5 2x20P
J3	2.54mm L11.5 2x20P
MIPI-CSI	FPC 22P spacing 0.5mm
MIPI-DSI	FPC 15P spacing 1.0mm

2. Hardware Reference

2.1. Block Diagram

The block diagram below shows the components of WTDP4C5-S1 and their interconnections.

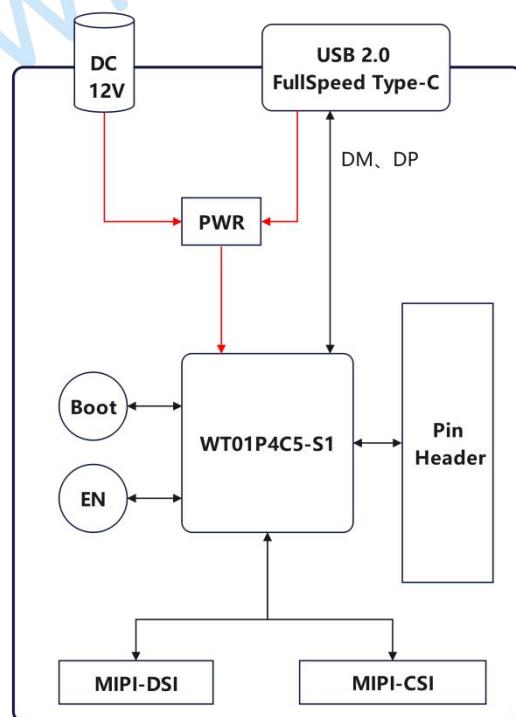


Figure 4: WTDP4C5-S1 Block Diagram

2.2. Header Block

The tables below provide the Name and Function of the pin or pin header(J2、J3、J7、J8).

Detailed Functional Description of J2

No.	Name	Function
1	VCC_3V3	3.3V Power in
2	C5_IO1	GPIO1, LP_GPIO1, XTAL_32K_N, LP_UART_DSRN, ADC1_CHO
3	VCC_3V3	3.3V Power in
4	C5_IO2	GPIO1, LP_GPIO1, XTAL_32K_N, LP_UART_DSRN, ADC1_CHO
5	C5_EN	Enable ESP32-C5 Chip (Internal 10K pull-up on the core board)
6	GND	GROUND
7	C5_IO28_BOOT	GPIO28
8	GND	GROUND
9	C5_U0TXD	GPIO11, U0TXD
10	C5_IO27	GPIO27
11	C5_U0RXD	GPIO12, U0RXD
12	C5_IO26	GPIO26
13	C5_IO3	GPIO3, MTDI, LP_GPIO3, LP_UART_CTSN, ADC1_CH2
14	C5_IO25	GPIO25
15	C5_IO4	GPIO4, LP_GPIO4, LP_UART_RXD, MTCK, ADC1_CH3, FSPIHD
16	C5_IO24	GPIO24
17	C5_IO5	GPIO5, LP_GPIO5, LP_UART_TXD, MTDO, ADC1_CH4, FSPIWP
18	C5_IO23	GPIO23
19	C5_IO6	GPIO6, LP_GPIO6, LP_I2C_SDA, ADC1_CH5, FSPICLK
20	NC	/
21	NC	/
22	NC	/

23	PWR_CTRL	Core board power control pin (default high level; pull low to power down)
24	GPIO6	GPIO6, SPI2_HOLD_PAD, LP_GPIO6, TOUCH_CHANNEL4
25	GPIO0	GPIO0, LP_GPIO0, XTAL_32K_N
26	GPIO7	GPIO7, SPI2_CS_PAD, LP_GPIO7, TOUCH_CHANNEL5
27	GPIO1	GPIO1, LP_GPIO1, XTAL_32K_P
28	GPIO8	GPIO8, UART0_RTS_PAD, SPI2_D_PAD, LP_GPIO8, TOUCH_CHANNEL6
29	GPIO2	GPIO2, MTCK, LP_GPIO2, TOUCH_CHANNEL0
30	GPIO11	GPIO11, UART1_RXD_PAD, SPI2_WP_PAD, LP_GPIO11, TOUCH_CHANNEL9
31	GPIO3	GPIO3, MTDI, LP_GPIO3, TOUCH_CHANNEL1
32	GPIO20	GPIO20, ADC1_CHANNEL4
33	GPIO4	GPIO4, MTMS, LP_GPIO4, TOUCH_CHANNEL2
34	GPIO21	GPIO21, ADC1_CHANNEL5
35	GPIO9	GPIO9, UART0_CTS_PAD, SPI2_CK_PAD, LP_GPIO9, TOUCH_CHANNEL7
36	GPIO22	GPIO22, ADC1_CHANNEL6
37	GPIO10	GPIO10, UART1_TXD_PAD, SPI2_Q_PAD, LP_GPIO10, TOUCH_CHANNEL8
38	GPIO23	GPIO23, ADC1_CHANNEL7, REF_50M_CLK_PAD
39	GND	GROUND
40	GND	GROUND

Detailed Functional Description of J3

No.	Name	Function
1	DC_5V	5V Power in
2	GPIO54	GPIO54, GMAC_PHY_RXER_PAD, ADC2_CHANNEL5, ANA_COMP1

3	DC_5V	5V Power in
4	GPIO53	GPIO53, GMAC_PHY_RXD1_PAD, ADC2_CHANNEL4, ANA_COMP1
5	P4_EN	Enable ESP32-P4 Chip (Internal 10K pull-up on the core board)
6	GND	GROUND
7	GPIO35_BOOT	GPIO35, SPI2_IO5_PAD, GMAC_PHY_TXD1_PAD (Internal 10K pull-up on the core board)
8	GND	GROUND
9	IO38_UO_RXD	GPIO38, UART0_RXD_PAD, SPI2_DQS_PAD (ESP32-P4 Download Pins)
10	GPIO52	GPIO52, GMAC_PHY_RXD0_PAD, ADC2_CHANNEL3, ANA_COMP0
11	IO37_UO_TXD	GPIO37, UART0_TXD_PAD, SPI2_IO7_PAD (ESP32-P4 Download Pins)
12	GPIO51	GPIO51, GMAC_PHY_RXDV_PAD, ADC2_CHANNEL2, ANA_COMP0
13	GND	GROUND
14	GPIO50	GPIO50, GMAC_RMII_CLK_PAD, ADC2_CHANNEL1
15	GPIO36	GPIO36, SPI2_IO6_PAD, GMAC_PHY_TXER_PAD (Internal 10K pull-up on the core board)
16	GPIO49	GPIO49, GMAC_PHY_TXEN_PAD, ADC2_CHANNEL0
17	GPIO34	GPIO34, SPI2_IO4_PAD, GMAC_PHY_RXD0_PAD
18	GPIO48	GPIO48, SD1_CDATA7_PAD, GMAC_PHY_RXER_PAD
19	GPIO33	GPIO33, SPI2_WP_PAD, GMAC_PHY_TXEN_PAD
20	GPIO47	GPIO47, SD1_CDATA6_PAD,

		GMAC_PHY_RXD1_PAD
21	GPIO32	GPIO32, SPI2_HOLD_PAD, GMAC_RMII_CLK_PAD
22	GPIO46	GPIO46, SD1_CDATA5_PAD, GMAC_PHY_RXD0_PAD
23	GPIO31	GPIO31, SPI2_Q_PAD, GMAC_PHY_RXER_PAD
24	GPIO45	GPIO45, SD1_CDATA4_PAD, GMAC_PHY_RXDV_PAD
25	GPIO30	GPIO30, SPI2_CK_PAD, GMAC_PHY_RXD1_PAD
26	GPIO44	GPIO44, SD1_CCMD_PAD, GMAC_RMII_CLK_PAD
27	GPIO29	GPIO29, SPI2_D_PAD, GMAC_PHY_RXD0_PAD
28	GPIO43	GPIO43, SD1_CCLK_PAD, GMAC_PHY_TXER_PAD
29	GPIO28	GPIO28, SPI2_CS_PAD, GMAC_PHY_RXDV_PAD
30	GPIO42	GPIO42, SD1_CDATA3_PAD, GMAC_PHY_TXD1_PAD
31	GPIO27	GPIO27, USB1P1_P1
32	GPIO41	GPIO41, SD1_CDATA2_PAD, GMAC_PHY_TXD0_PAD
33	GPIO26	GPIO26, USB1P1_N1
34	GPIO40	GPIO40, SD1_CDATA1_PAD, GMAC_PHY_TXEN_PAD
35	GPIO25	GPIO25, USB1P1_P0
36	GPIO39	GPIO39, SD1_CDATA0_PAD, REF_50M_CLK_PAD
37	GPIO24	GPIO24, USB1P1_N0
38	ESP_LDO_VO4	Output POWER (Output voltage range 0.5~2.7V or 3.3V, maximum

		output current 0.2A)
39	GND	GROUND
40	GND	GROUND

Detailed Functional Description of J7

序号	名称	描述
1	GND	GROUND
2	C5_IO28_BOOT	GPIO28
3	C5_EN	Enable ESP32-C5 Chip (Internal 10K pull-up on the core board)
4	C5_U0RXD	GPIO12, U0RXD
5	C5_U0TXD	GPIO11, U0TXD
6	NC	/
7	VCC_5V	5V Power in

Detailed Functional Description of J8

序号	名称	描述
1	GND	GROUND
2	GPIO35_BOOT	GPIO35, SPI2_IO5_PAD, GMAC_PHY_TXD1_PAD (Internal 10K pull-up on the core board)
3	P4_EN	Enable ESP32-P4 Chip (Internal 10K pull-up on the core board)
4	IO38_U0_RXD	GPIO38, UART0_RXD_PAD, SPI2_DQS_PAD (ESP32-P4 Download Pins)
5	IO37_U0_TXD	GPIO37, UART0_TXD_PAD, SPI2_IO7_PAD (ESP32-P4 Download Pins)
6	NC	/
7	VCC_5V	5V Power in

3. Getting Started

3.1. Preliminary

- WTDP4C5-S1
- USB-C cables or DC 12V Power Adapter
- Computer running Windows,Linux,or macOS
- Wireless-tag Flash Tool
- LCD (Optional)
- Camera (Optional)

3.2. Hardware Setup

3.2.1. Development Board Power Supply Instructions

- Use a DC 12V power adapter connected to the DC power port on the development board for power supply
- Use a USB Type-C cable to connect to the USB Type-C port on the development board for power supply
- After connecting to either terminal at J7 or J8 using the Wireless-tag Flash Tool, use a USB Type-C cable to connect to the USB Type-C port on the programming tool for power supply

3.2.2. Development Board Download or Debug Instructions

- After connecting the Wireless-tag Flash Tool to the terminal at J7, use a USB Type-C cable to connect the USB Type-C port on the programming tool to a computer. This allows firmware to be downloaded to the ESP32-C5 chip via the serial port and debugged.
- After connecting the Wireless-tag Flash Tool to the terminal at J8, use a USB Type-C cable to connect the USB Type-C port on the programming tool to a computer. This allows firmware to be downloaded to the ESP32-P4 chip via the serial port and debugged.
- When connecting the development board's USB Type-C port to a computer via a USB Type-C cable, press and hold the Boot Key while briefly

pressing the EN Key to download the firmware to the ESP32-P4 chip via the serial port.

- If using other flash tools, ground the BOOT pin before powering on and connect it to the corresponding serial port pin. After powering on, the chip will enter download mode. Firmware can then be flashed to the corresponding chip and debugged via a computer programming tool through the serial port.

3.3. Software Setup

To set up your development environment and flash an application example onto your board, please follow the instructions in [ESP-IDF Get Started](#). Or go to [Wireless-Tag GitHub Examples](#), development board application examples have been stored, download compile and burn the application to the development board to start development.

4. Related Documents

WTDP4C5-S1 Github: <https://github.com/wireless-tag-com/WTDP4C5-S1>

5. Contact Us

Official website: www.wireless-tag.com

Contact Email: gtm@wireless-tag.com

Technical support e-mail: technical@wireless-tag.com

