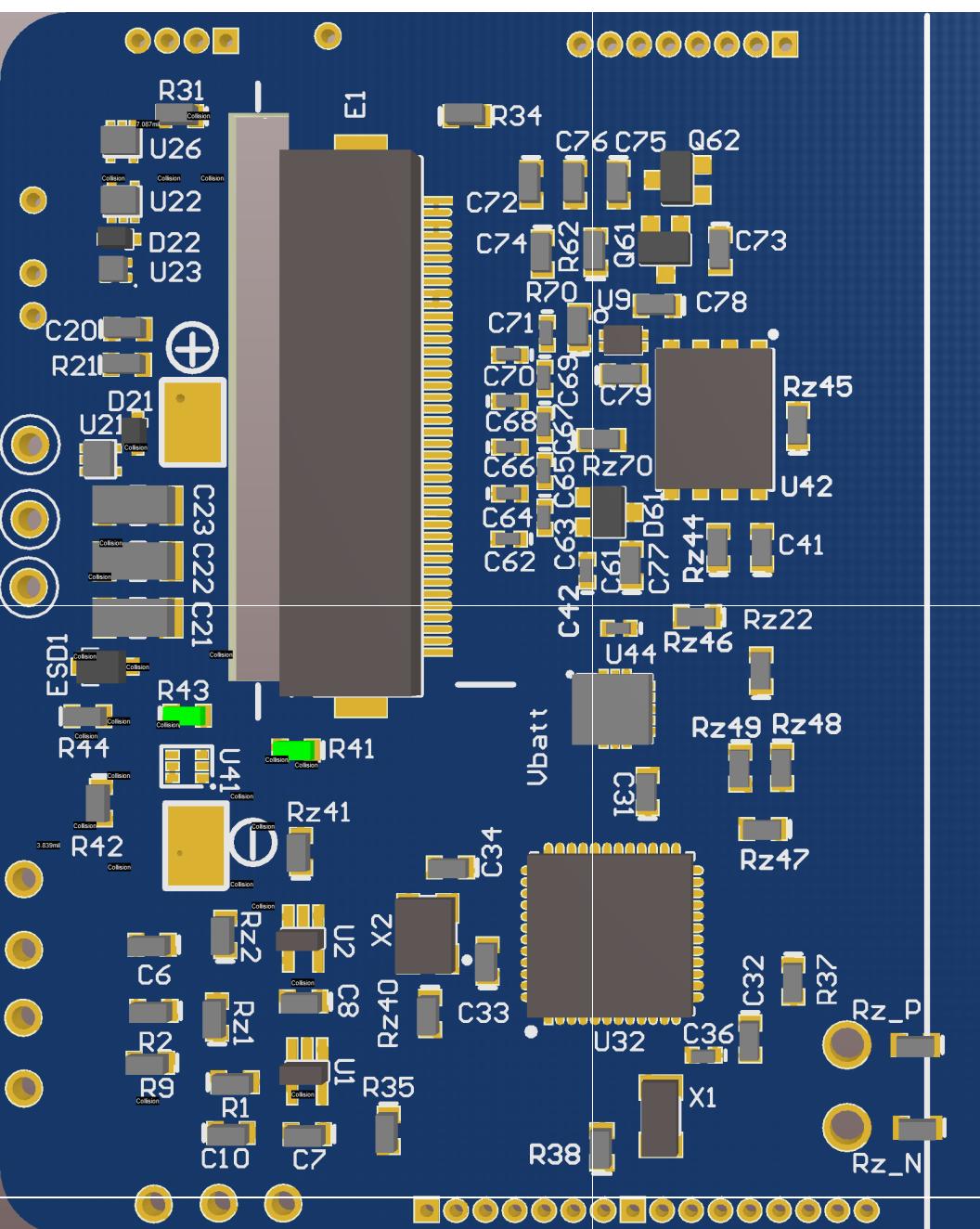
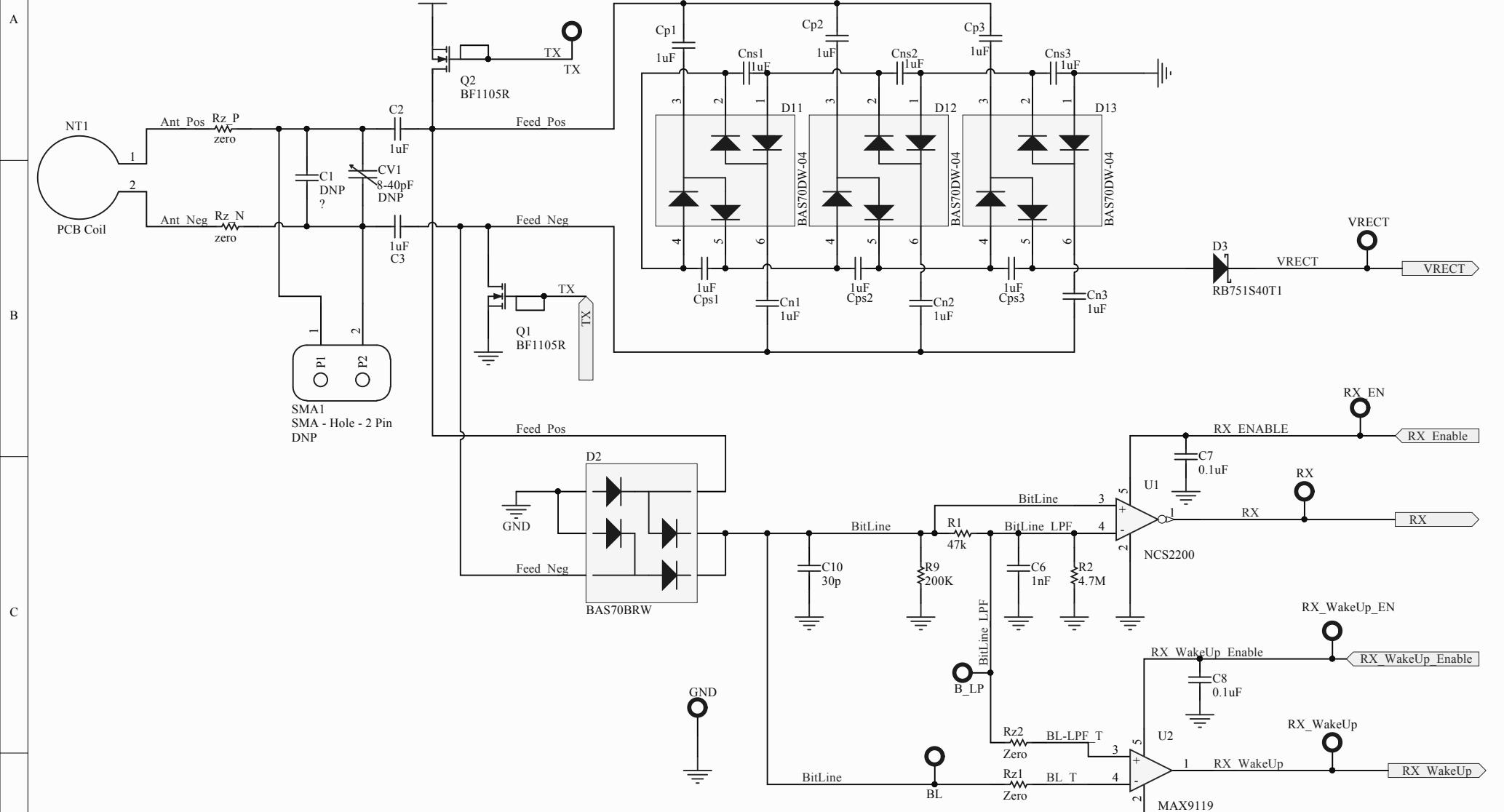


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Todo:

- 1)VNA testing is needed to determine C1
- 2)Tune C10 and R9 for demodulator
:reduce C10 and R9 will increase the bit detection threshold

*DNP => Do Not Populate

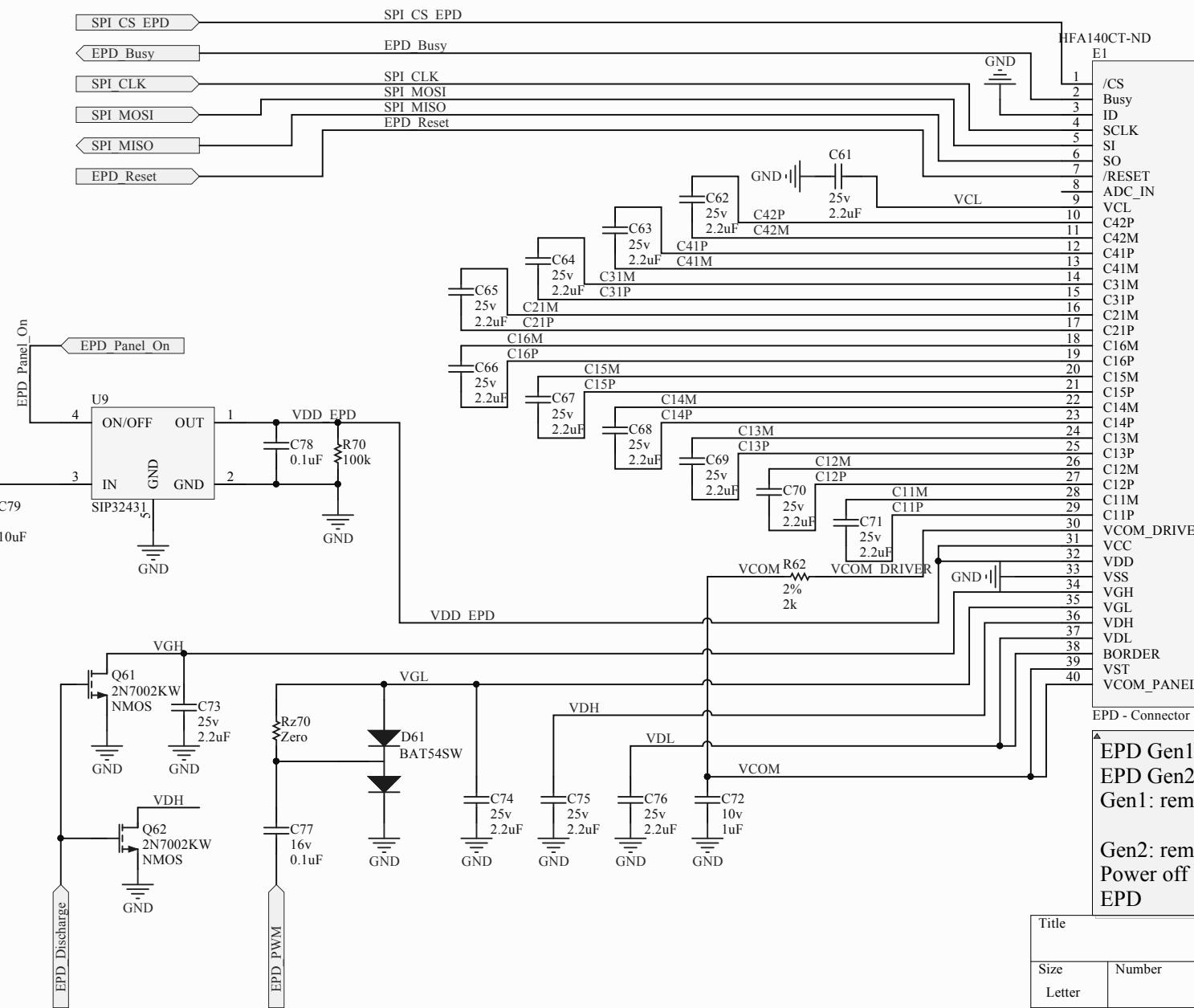
Title: *nfc-epd-afe.SchDoc*

Designed by: Yi Zhao (Eve), Alanson Sample Data: 10/25/2014

Version: NFC-WISP_1.0

File: C:\Users\evezhao\Dropbox\Disney Research\NFC_WISP_DRP\Schematic\alitium\nfc-epd-afe.SchDoc

A



EPD - Connector

EPD Gen1: EM027AS012

EPD Gen2: EM027BS012

Gen1: remove Rz70

Gen2: remove C77,C61,C62

Power off Sequence is different for Gen2 EPD

Title

Size
Letter

Number

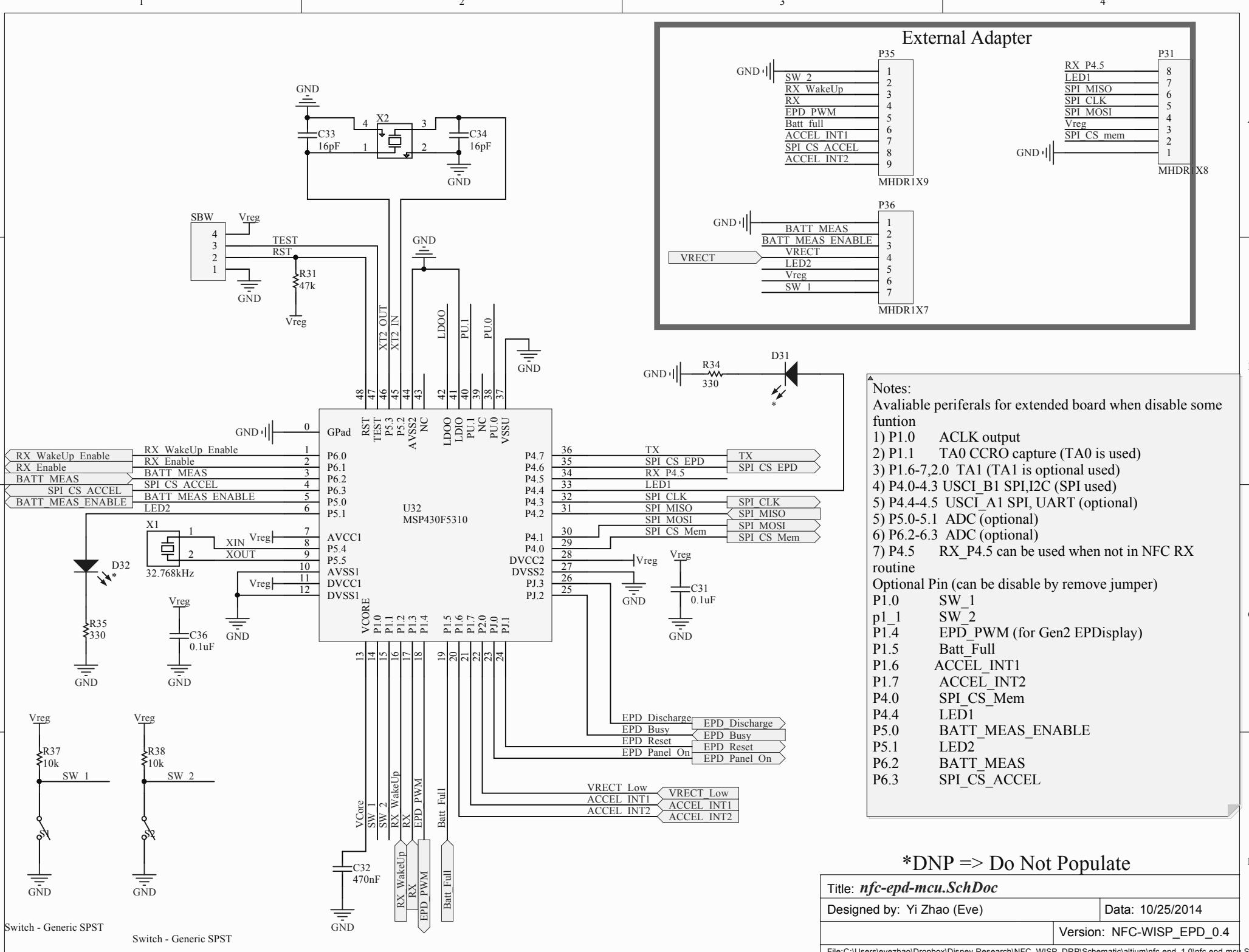
Revision

Date: 11/4/2014

Sheet of

File: C:\Users...\nfc-epd-eink.SchDoc

Drawn By:



Warning

The bottom of MEC201 (B1) is conductive and connected to the positive battery terminal. Thus, it is possible to short V+ to a trace or a via on the bottom of the PCB if there are defects in the solder mask (which is very likely with the covered vias used in layout).

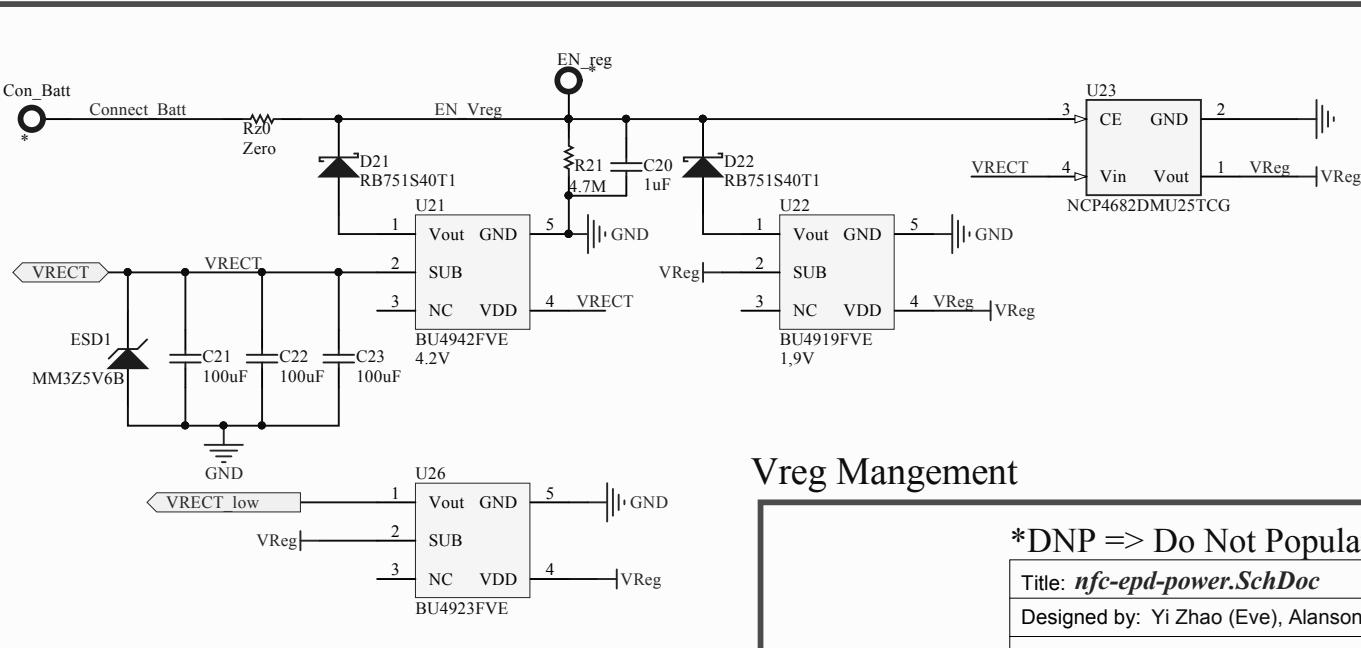
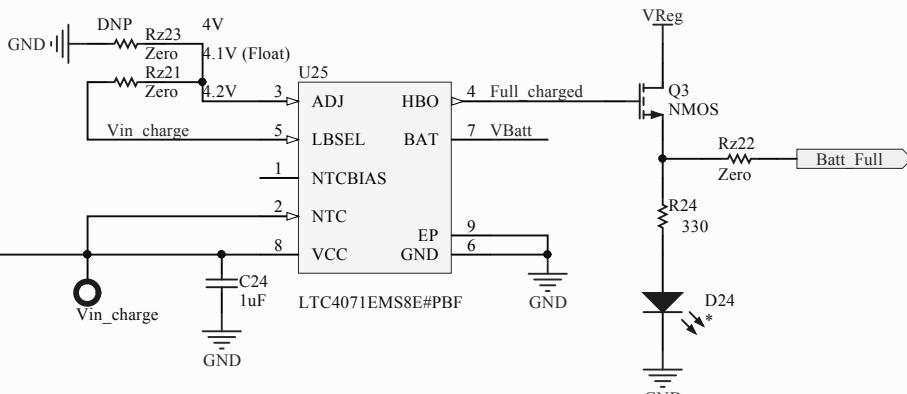
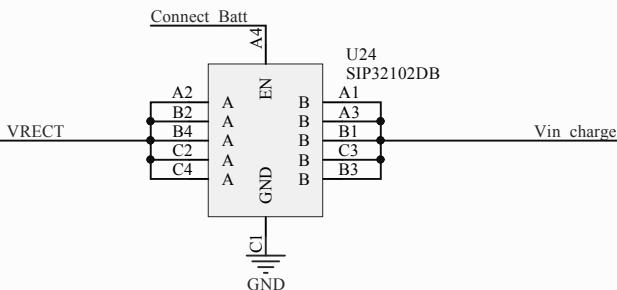
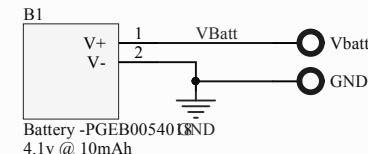
The best solution is to use double sided Kapton to insulate and affix cell to board.

Note:
Must remove Rz23 or Rz21 or both to configure the fully charged threshold

Remove 24 or Rz22 if we do not need battery full LED blinking

TODO

- 1 do we need indicate charging D24??
- 2 power-off voltage ? 1.8? or 2.5? or 2?
- 3 should we use bigger Batt?
- 4 Do we need temperature protection?



Vreg Management

*DNP => Do Not Populate

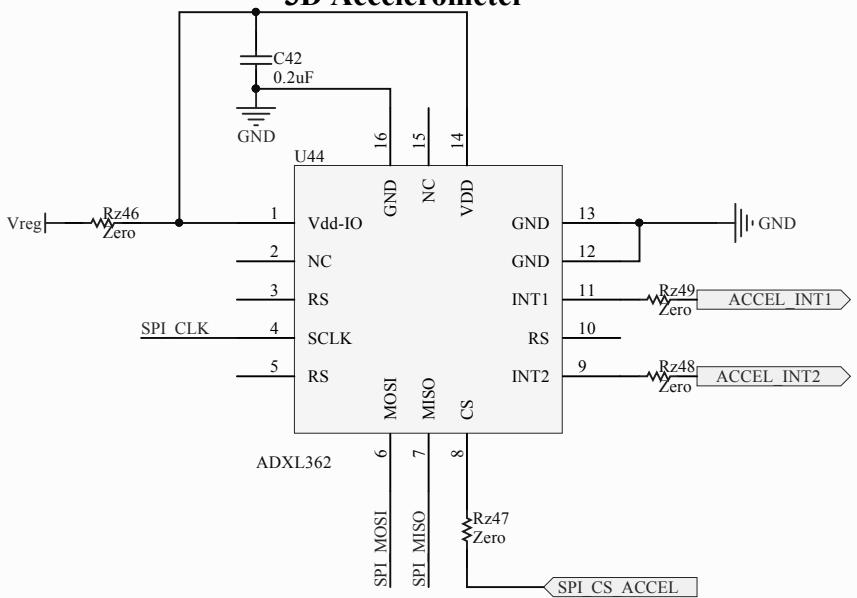
Title: *nfc-epd-power.SchDoc*

Designed by: Yi Zhao (Eve), Alanson Sample Data: 10/25/2014

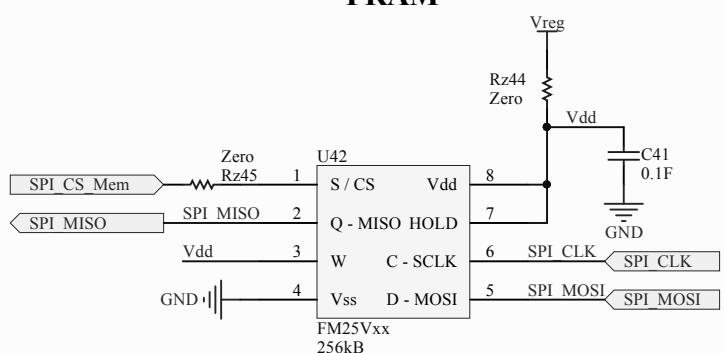
Version: NFC-WISP_EPD_1.0

File:C:\Users\lvezhao\Dropbox\Disney Research\NFC_WISP_DRP\Schematic\altium\nfc-epd_1.0\nfc-epd-power.Sch

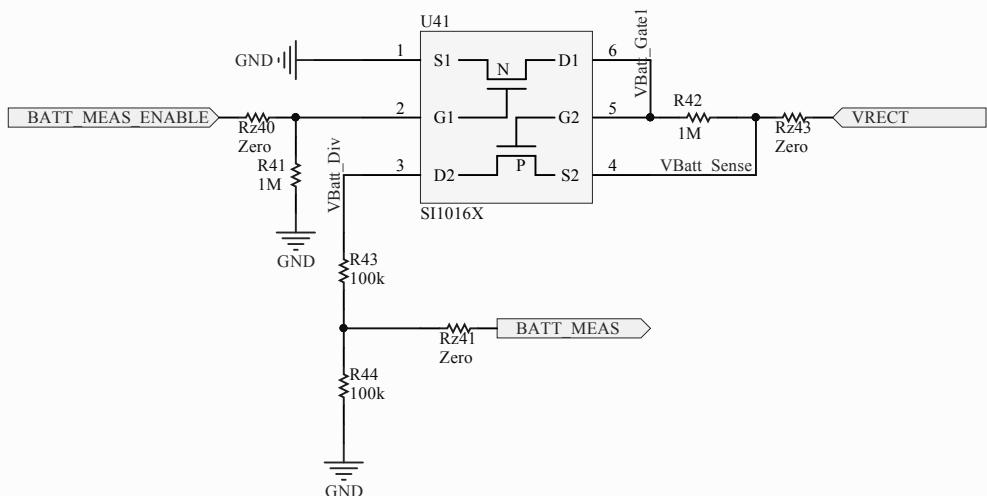
3D Accelerometer



FRAM



High-side switching for supply voltage measurement



Note:

- (1) 2MB size FRAM (U42) is not in stock now, use 256k
- (2) U41 can be disabled by remove Rz40, Rz41, Rz43 to save power or provide I/O Pin

*DNP => Do Not Populate

Title: *nfc-epd-sensors.SchDoc*

Designed by: Yi Zhao (Eve)

Data: 10/25/2014

Version: NFC-WISP_EPD_1.0

File:C:\Users\levezhao\Dropbox\Disney Research\NFC_WISP_DRP\Schematic\altium\nfc-epd_1.0\nfc-epd-sensors.SchDoc

A Public Note:

Library Requirements:

WISP_AD10.PcbLib

WISP_AD10.SchLib

Miscellaneous Connectors.IntLib

Design Rules:

nfc-epd_1.0.RUL

(see document “Altium_DesignRules_Instructions_v1.doc” for instructions importing design rules and addition information and guidelines. Design rules files used for this project are modified from the 4 layer versions:
“AltiumSSC-DFM_MLB-final.RUL”

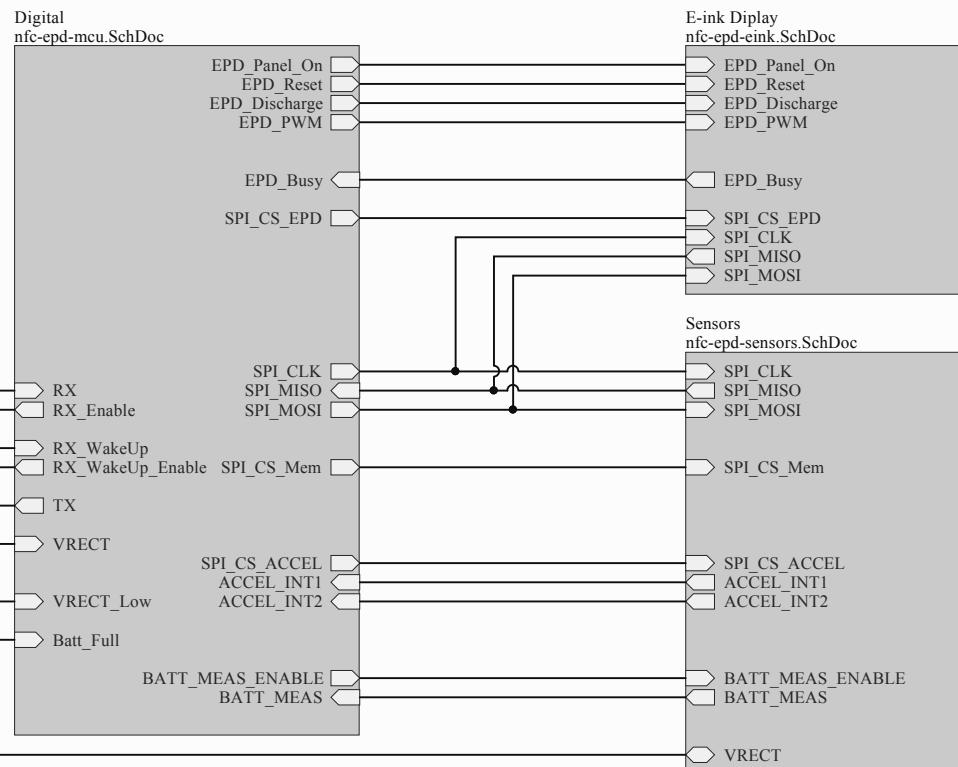
A Preliminary Release Notes:

Project and file naming convention:

Any projects/boards ending with a revision number less than 1 are considered pre-release (example: “WISP-board_0.3”). Boards that are release to be public automatically get promoted to 1.0 (example: “WISP-Board_1.0”).

Individual schematics and pcb files will be appended with a suffix “ vX” to denote file revisions (example: “WISP-board_0.3-digital_v1.SchDoc” or “WISP-board_0.3 – PCB_v6.PcbDoc”).

B



Note:
AE is intentionally not connected at this time.

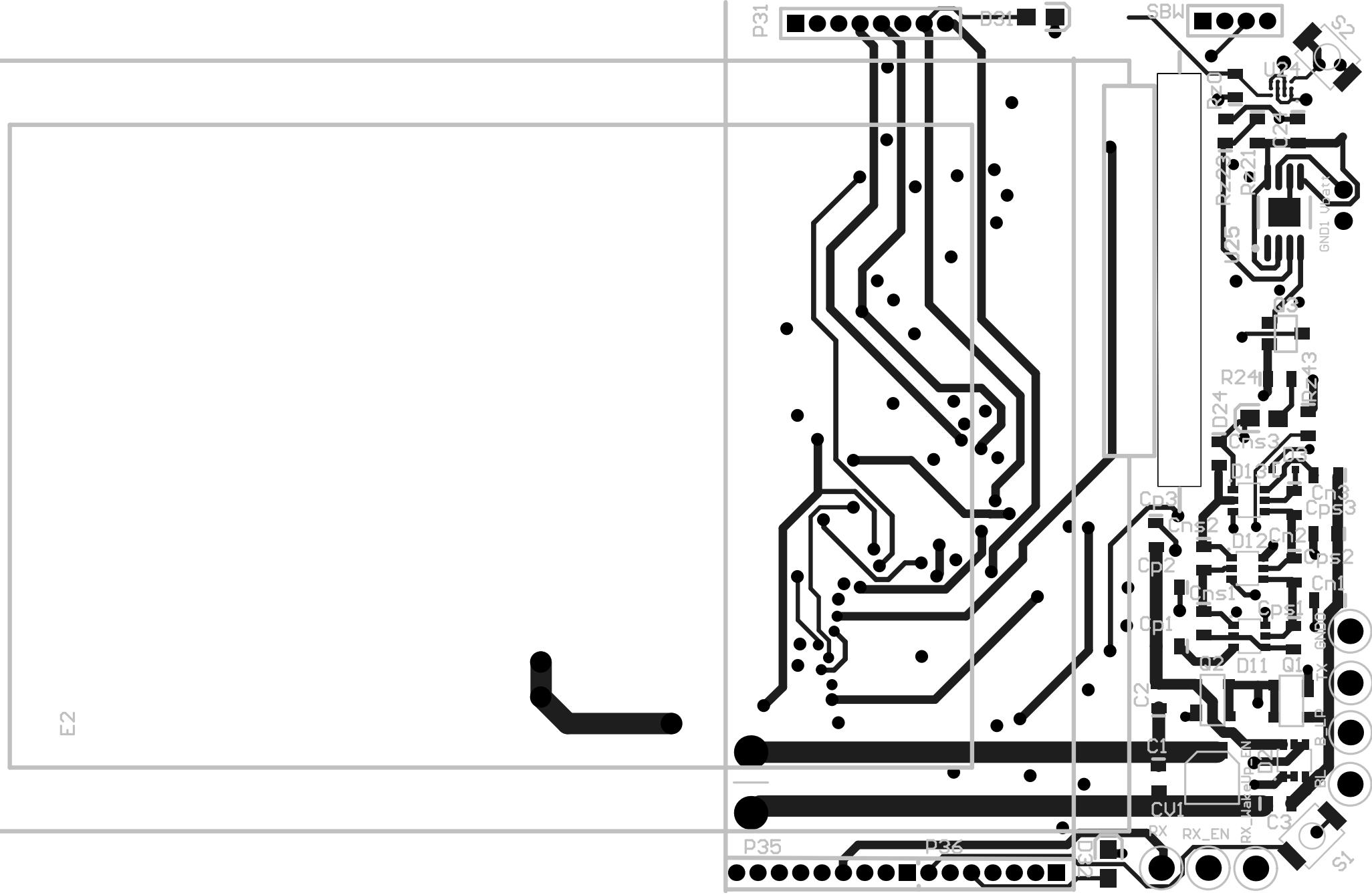
*DNP => Do Not Populate

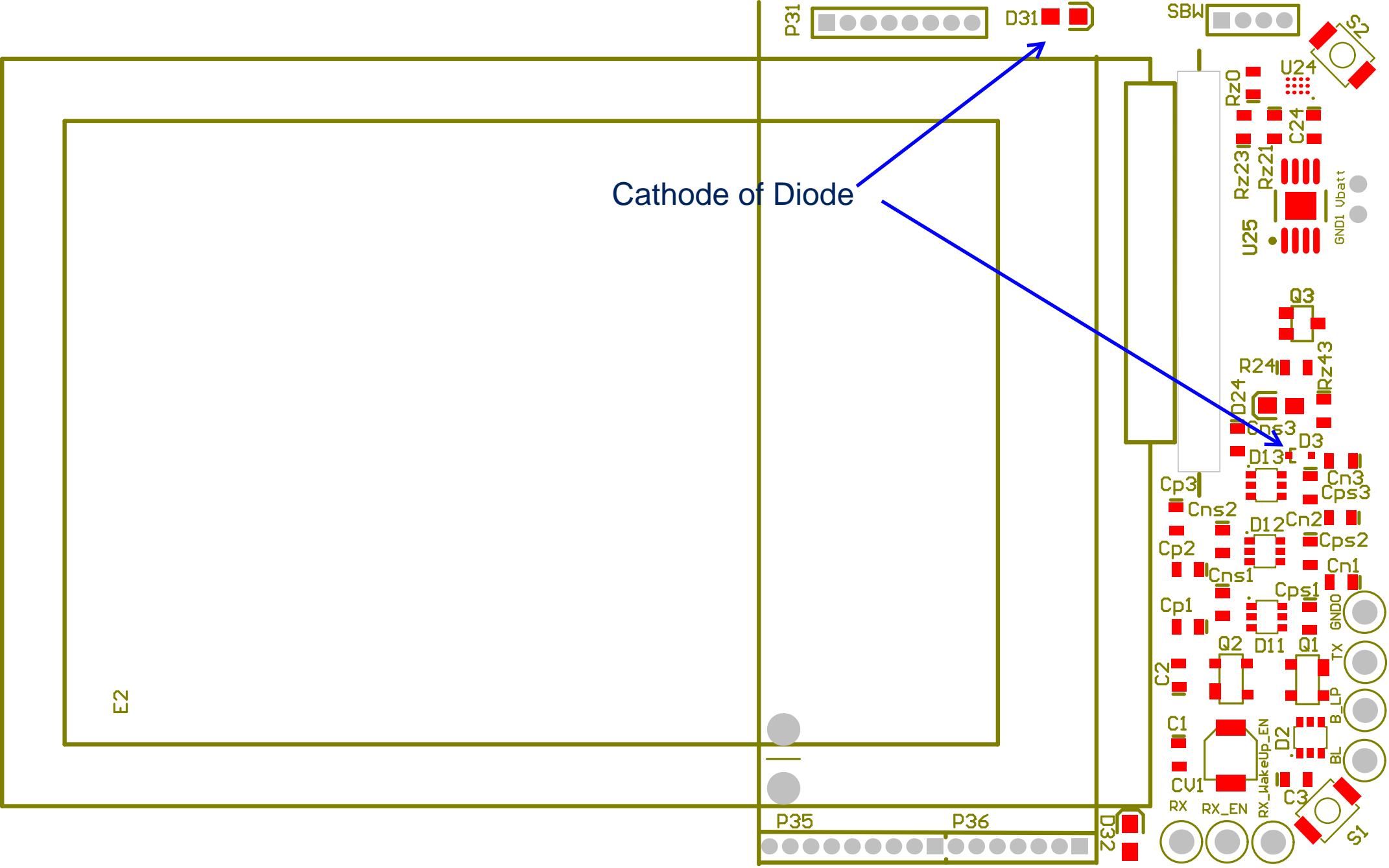
Title: *nfc-epd-top.SchDoc*

Designed by: Yi Zhao (Eve), Alanson Sample Data: 10/25/2014

Version: NFC-WISP_EPD_0.4

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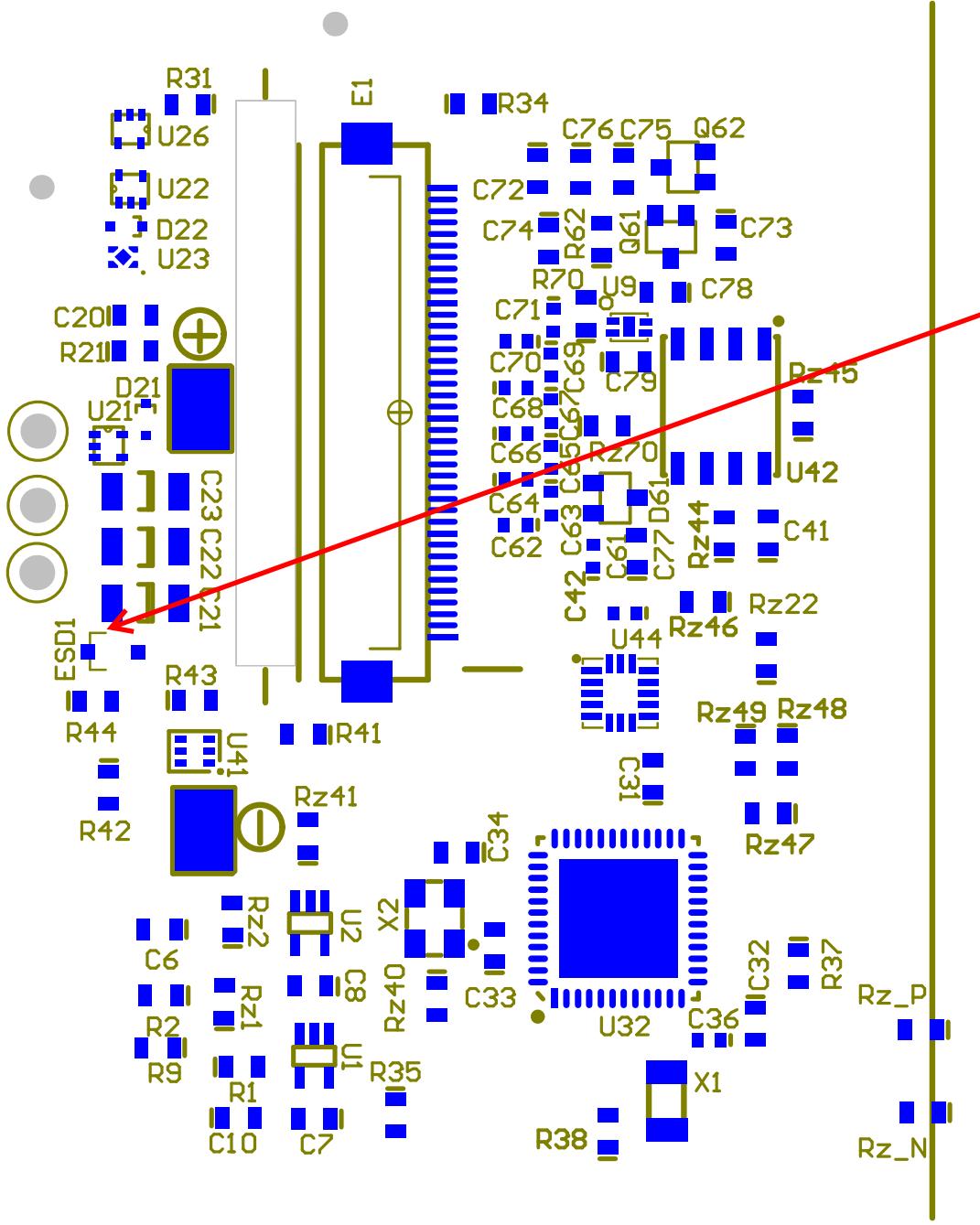


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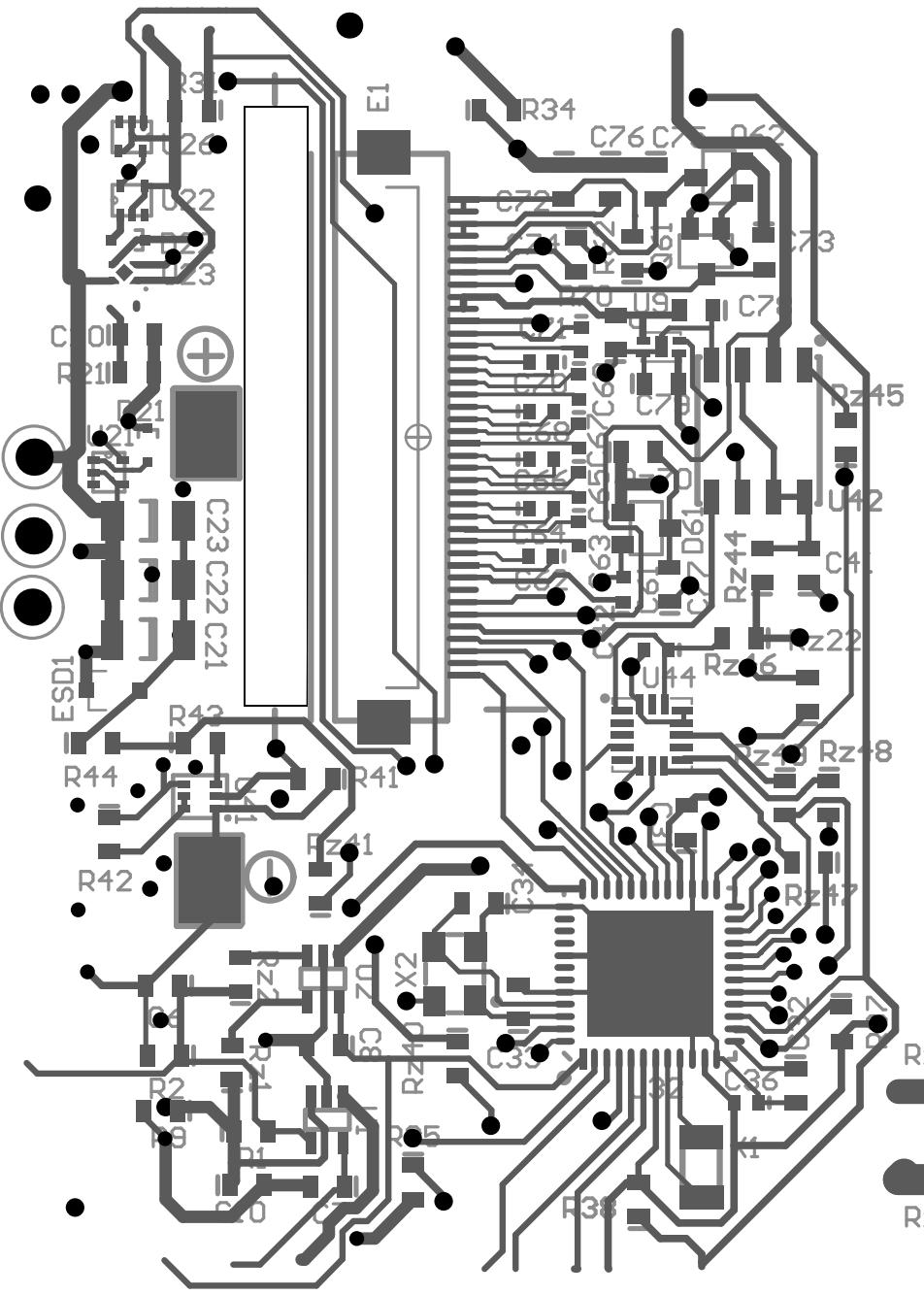
Cathode is marked as

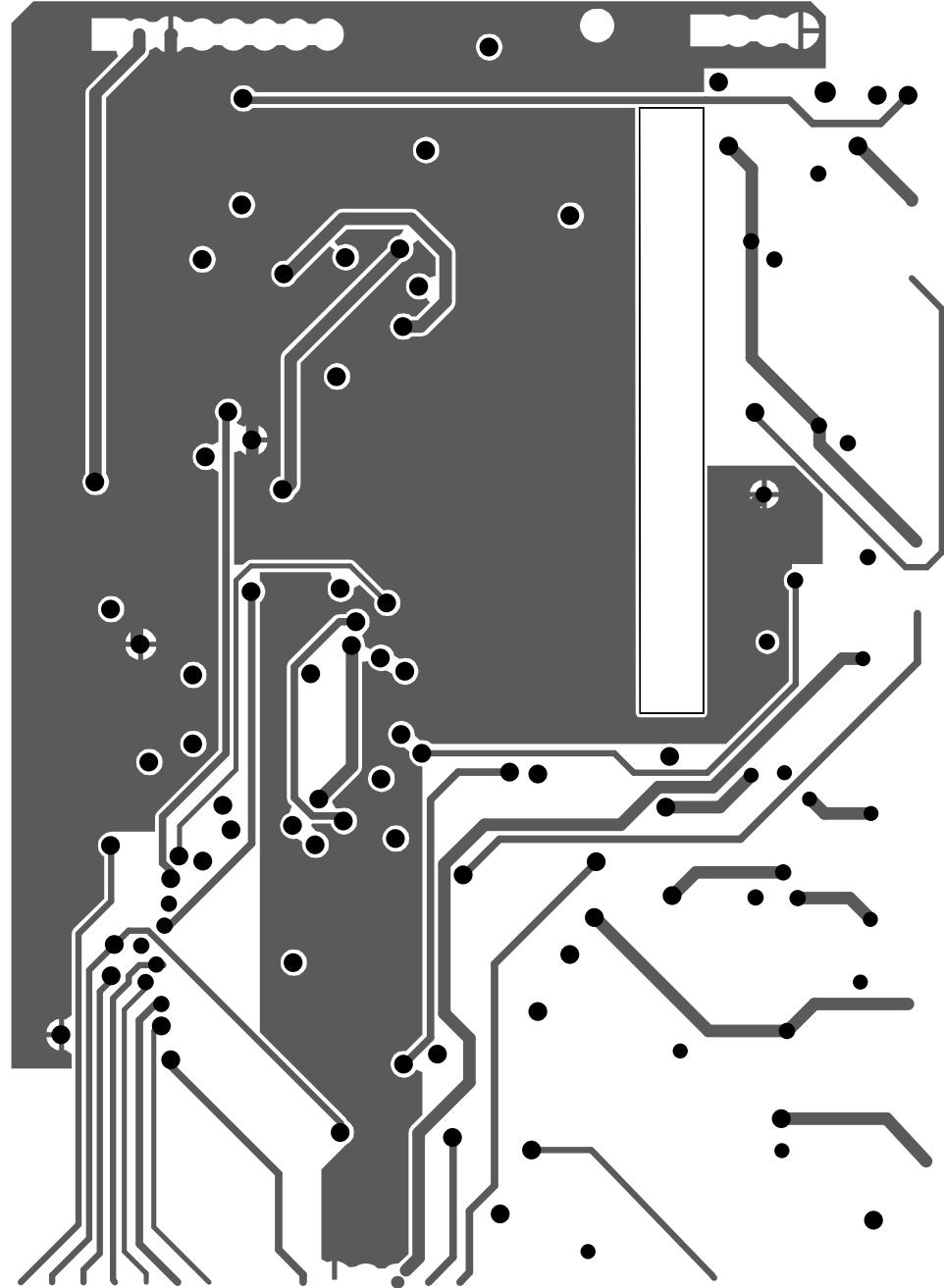


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D31

S2

E2

D32

S3

