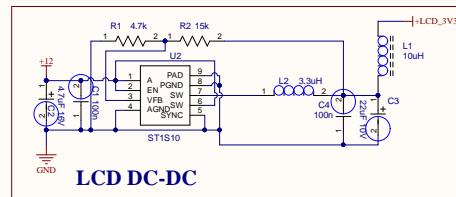


7Inch version



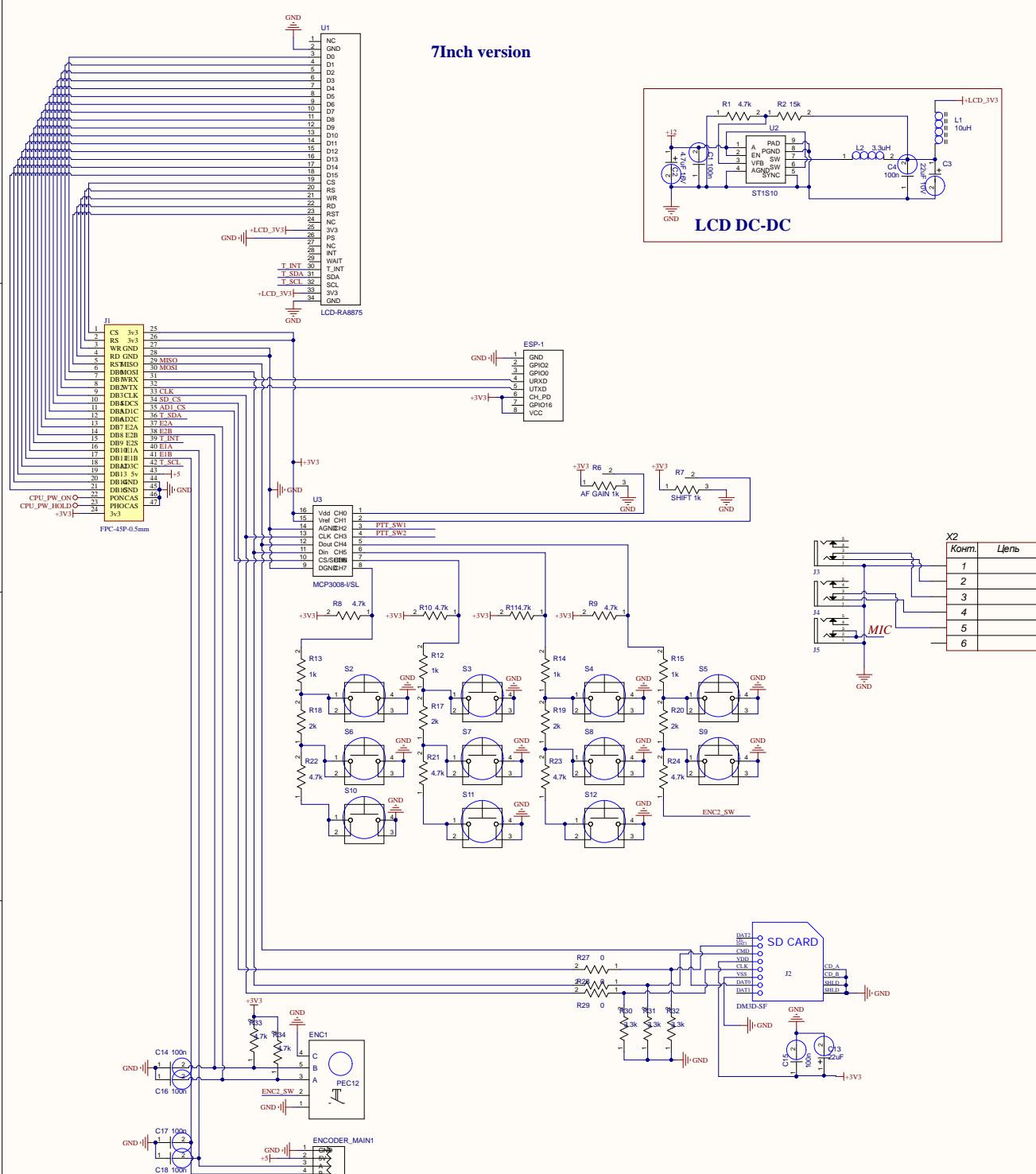
LCD DC-DC

A

B

C

D

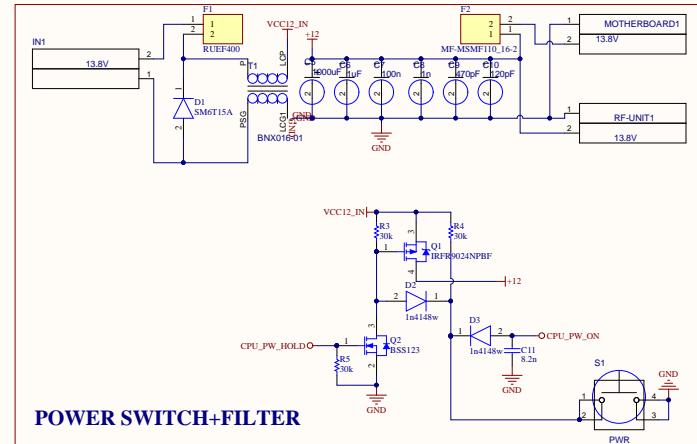


A

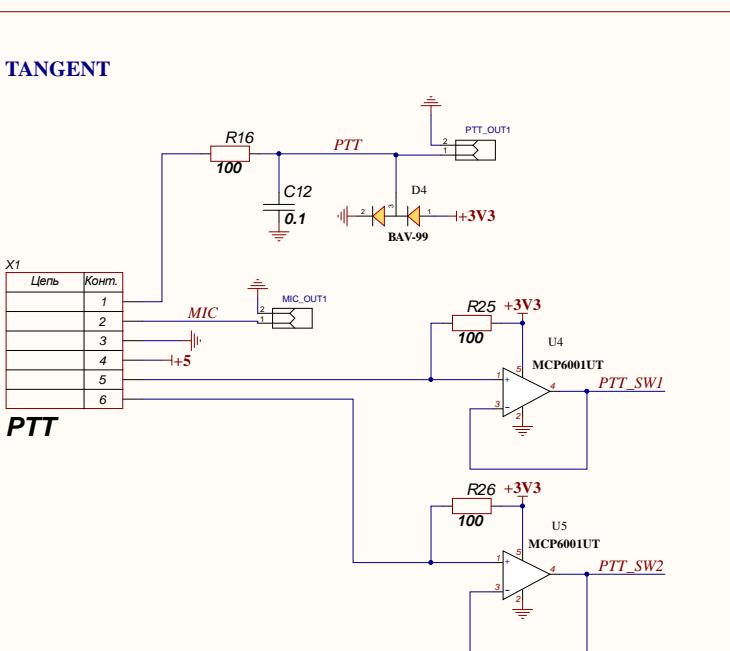
B

C

D



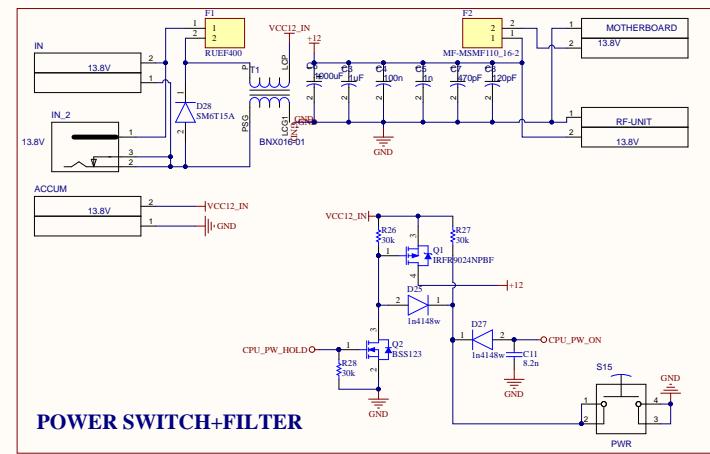
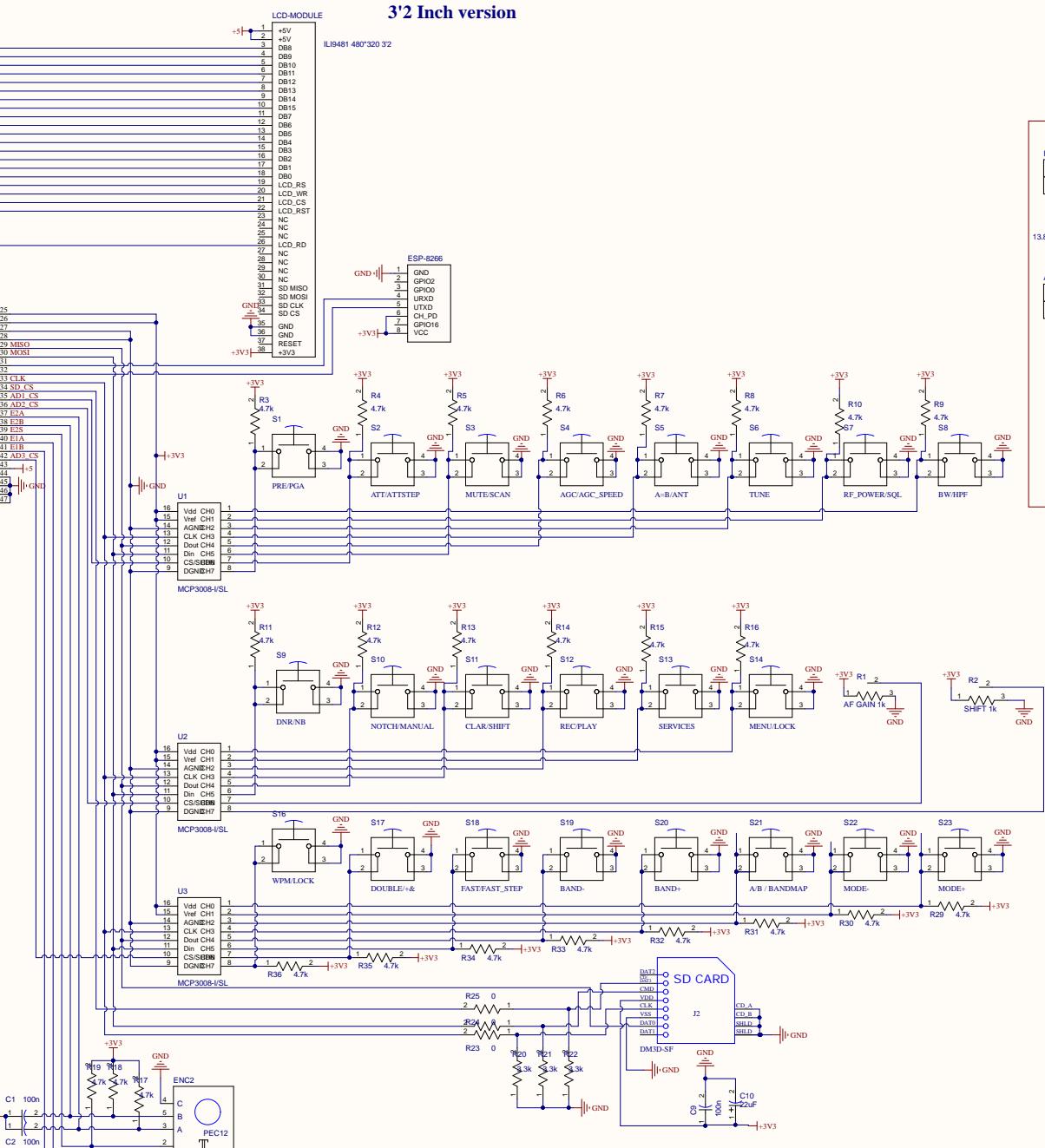
POWER SWITCH+FILTER



TANTENT

### 3'2 Inch version

ILI9481 480\*320 3'2



A

U\_POWER  
POWER.SchDoc

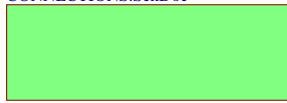


U\_CLOCK\_GENERATOR  
CLOCK\_GENERATOR.SchDoc



B

U\_CONNECTIONS  
CONNECTIONS.SchDoc



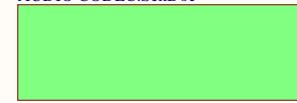
U\_FPGA  
FPGA.SchDoc



U\_STM32  
STM32.SchDoc



U\_AUDIO\_CODEC  
AUDIO\_CODEC.SchDoc



A

B

C

D

C

D

Title **MOTHERBOARD**

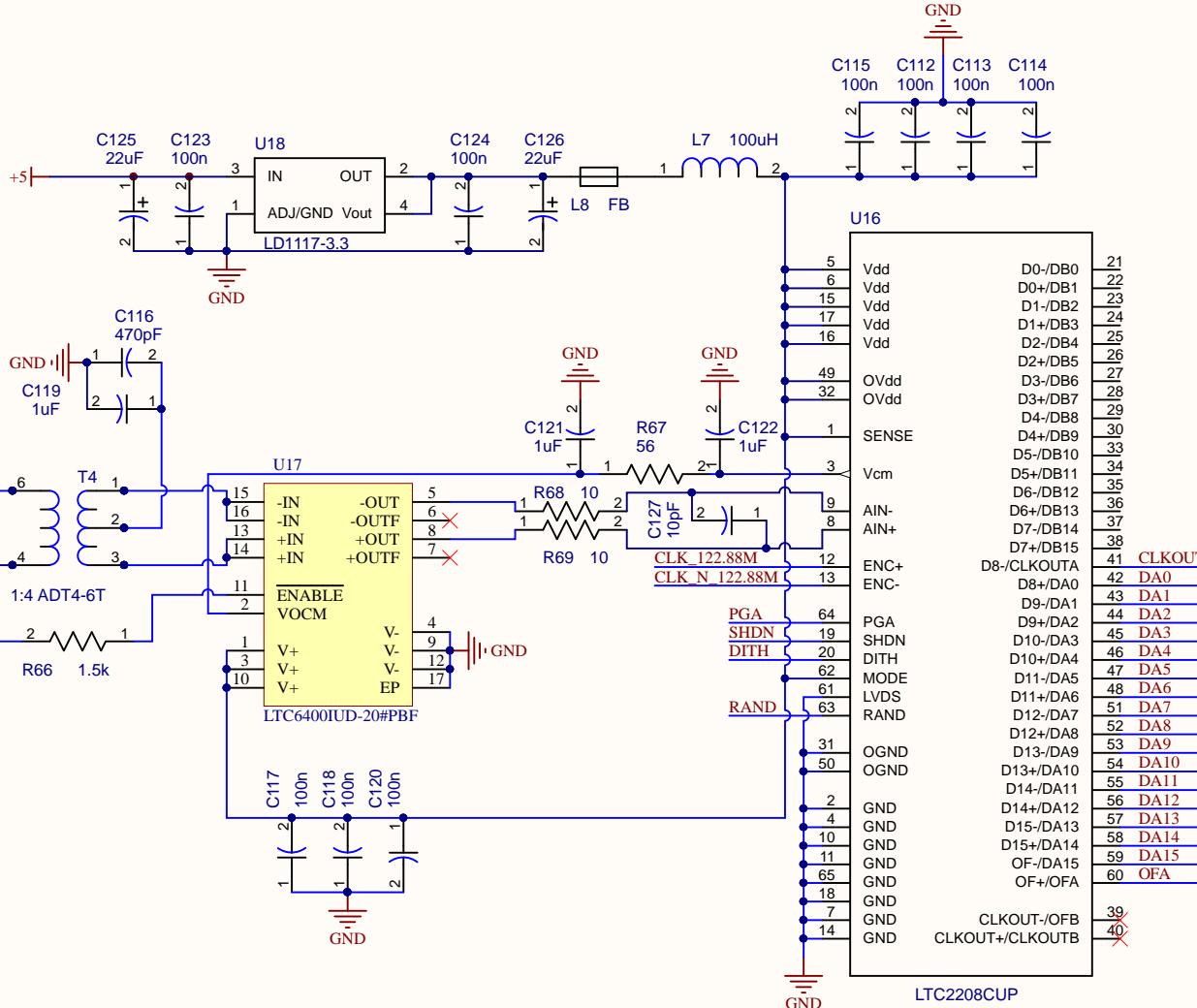
Size: A4 Number:2 Revision:2.0

Date: 06.11.2020 Time: 9:32:59 Sheet 2 of 18

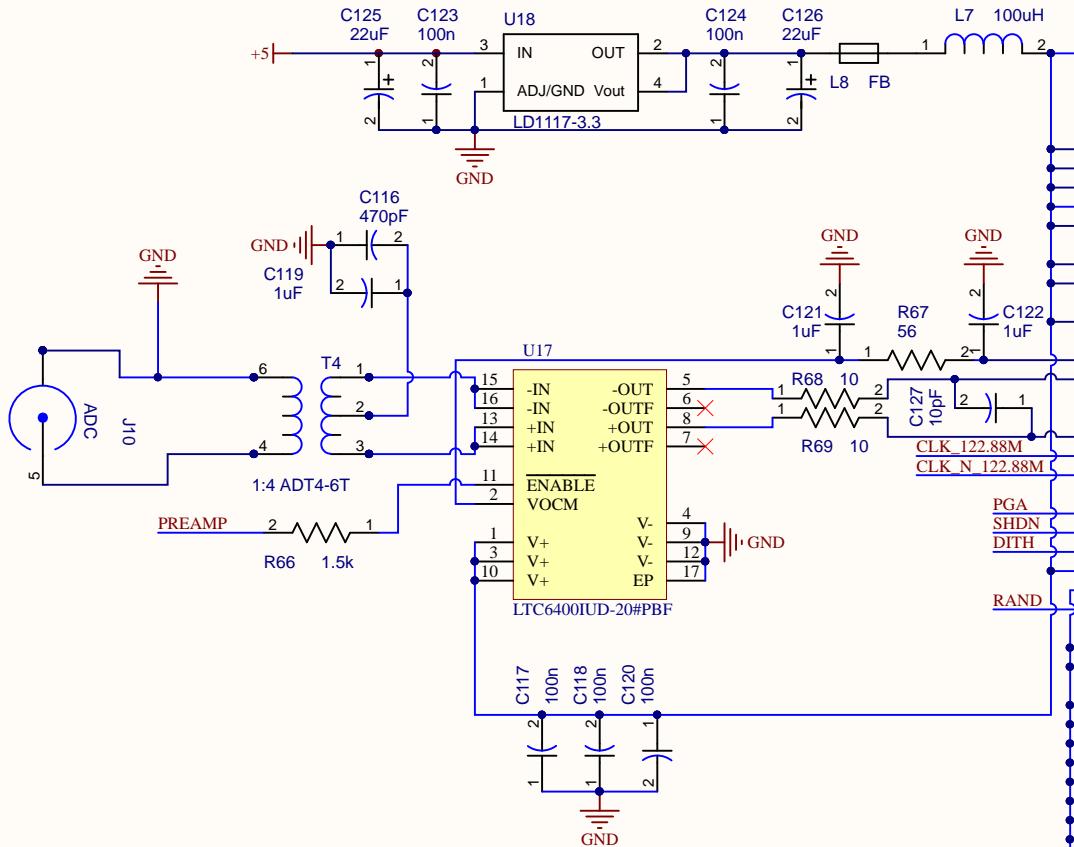
File: C:\Dropbox\Develop\Projects\WOLF\Scheme\ALTIUM\_DESIGNER\MOTHERBOARD\MOTHERBOARD.SCHDOC



A



B



C

Title <b>ADC</b>			*
Size: A4	Number:3	Revision:2.0	*
Date: 06.11.2020	Time: 9:32:59	Sheet 3 of 18	*
File: C:\Dropbox\Develop\Projects\WOLF\Schema\ALTIUM_DESIGNER\MOTHERBOARD\ADC.SchDoc			*

**Altium**

A

A

B

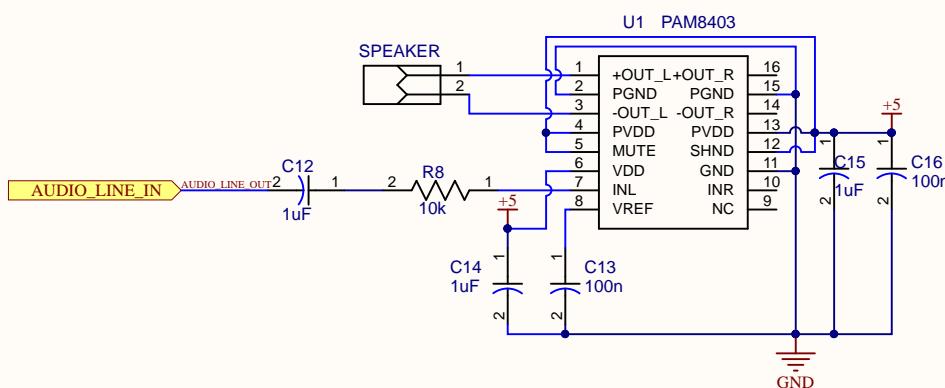
B

C

C

D

D

Title ***AF AMP***Size: **A4** Number: **4** Revision: **2.0**Date: **06.11.2020** Time: **9:33:00** Sheet **4** of **18**File: **C:\Dropbox\Develop\Projects\WOLF\Scheme\ALTIUM\_DESIGNER\MOTHERBOARD\AF AMP.SchDoc**
 \*  
 UA3REO  
 BH8CGJ  
 \*


A

B

C

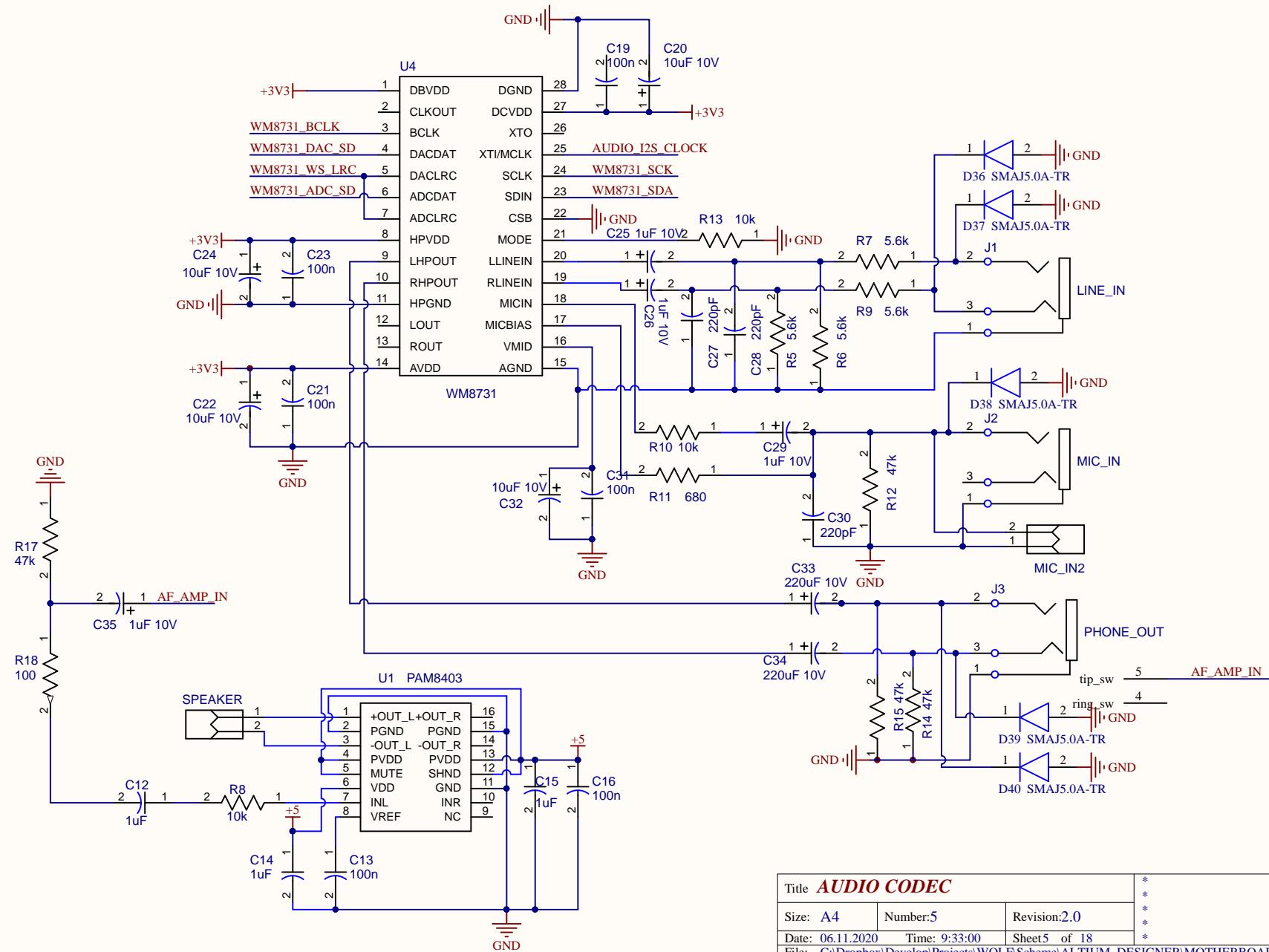
D

A

B

C

D

Title **AUDIO CODEC**

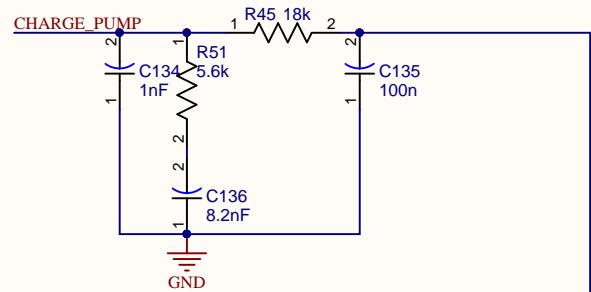
Size: A4 Number:5 Revision:2.0

Date: 06.11.2020 Time: 9:33:00 Sheet 5 of 18

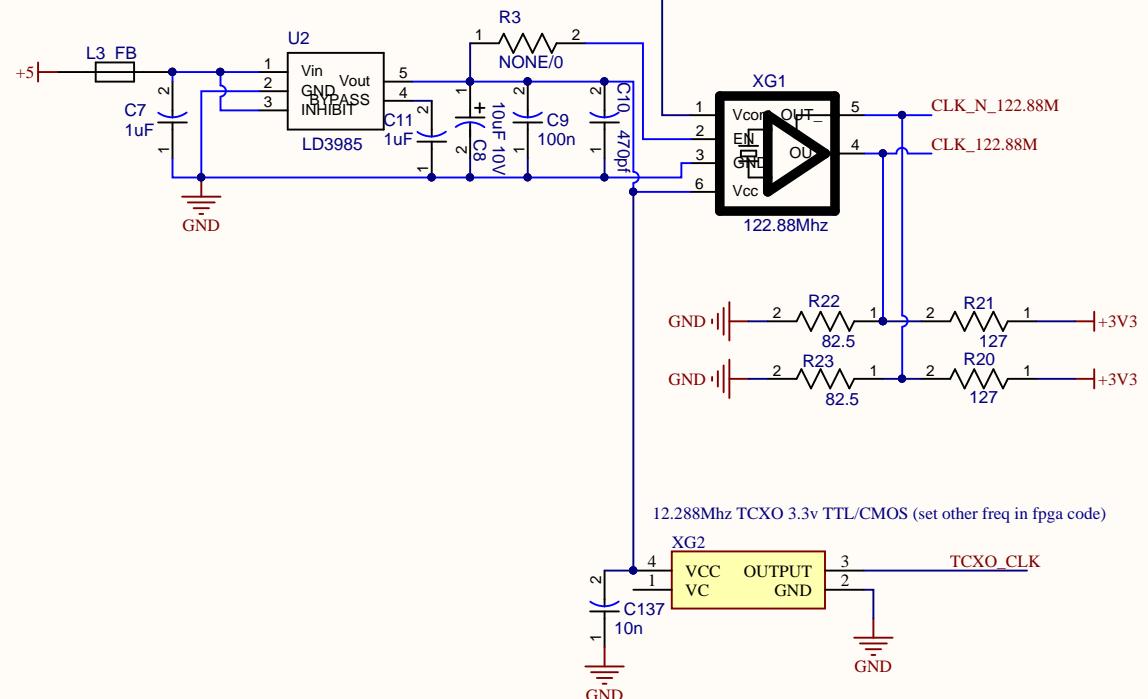
File: C:\Dropbox\Develop\Projects\WOLF\Schema\ALTIUM\_DESIGNER\MOTHERBOARD\AUDIO\_CODEC.SchDoc

**Altium**

A



B



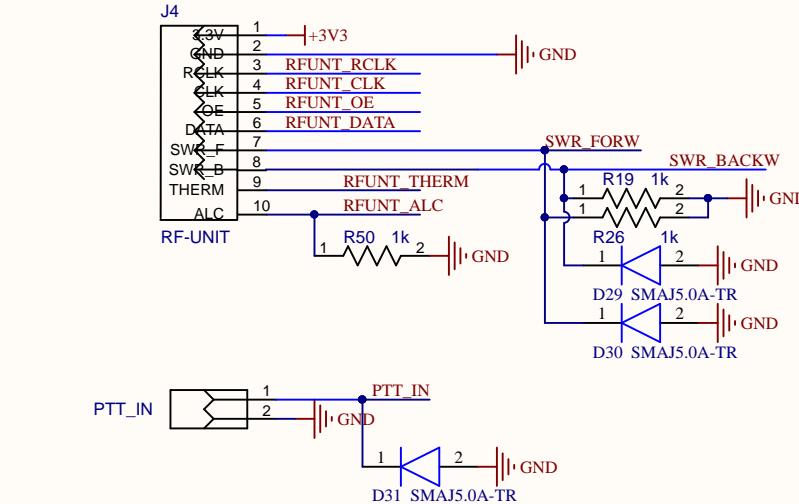
D

Title **CLOCK\_GENERATOR**

Size: A4	Number: 6	Revision: 2.0
Date: 06.11.2020	Time: 9:33:00	Sheet 6 of 18
File: C:\Dropbox\Develop\Projects\WOLF\Schema\ALTIUM_DESIGNER\MOTHERBOARD\CLOCK_GENERATOR.SchDoc		*

**Altium**

A

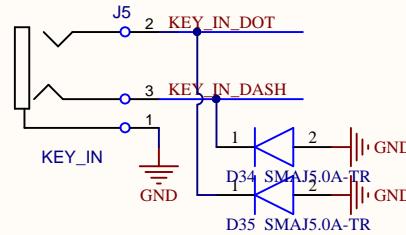


B

FMC_NE1	1	CS 3v3
FMC_A18	2	RS 3v3
FMC_NWE	3	WR GND
FMC_NOE	4	RD GND
STM_NRST	5	RST'MISO
FMC_D0	6	DB0'MOSI
FMC_D1	7	DB1'WRX
FMC_D2	8	DB2'WTX
FMC_D3	9	DB3'CLK
FMC_D4	10	DB4'DCS
FMC_D5	11	DB5'D1C
FMC_D6	12	DB6'D2C
FMC_D7	13	DB7'E2A
FMC_D8	14	DB8'E2B
FMC_D9	15	DB9'E2S
FMC_D10	16	DB10'E1A
FMC_D11	17	DB11'E1B
FMC_D12	18	DBAD3'C
FMC_D13	19	DB13'5v
FMC_D14	20	DB14'GND
FMC_D15	21	DB15'GND
PWR_ON	22	PONCAS
PWR_HOLD	23	PHOCAS
	24	3v3
	25	+3V3
	26	GND
	27	PERI_MISO
	28	PERI_MOSI
	29	ESP_1_RX
	30	PERI_SCK
	31	SD_CS
	32	AD1_CS
	33	AD2_CS
	34	ENC2_DT
	35	ENC2_CLK
	36	ENC2_SW
	37	ENC_DT
	38	ENC_CLK
	39	AD3_CS
	40	ENC_SW
	41	AD1_SW
	42	AD2_SW
	43	+5
	44	GND
	45	GND
	46	GND
	47	GND

FPC-45P-0.5mm

C

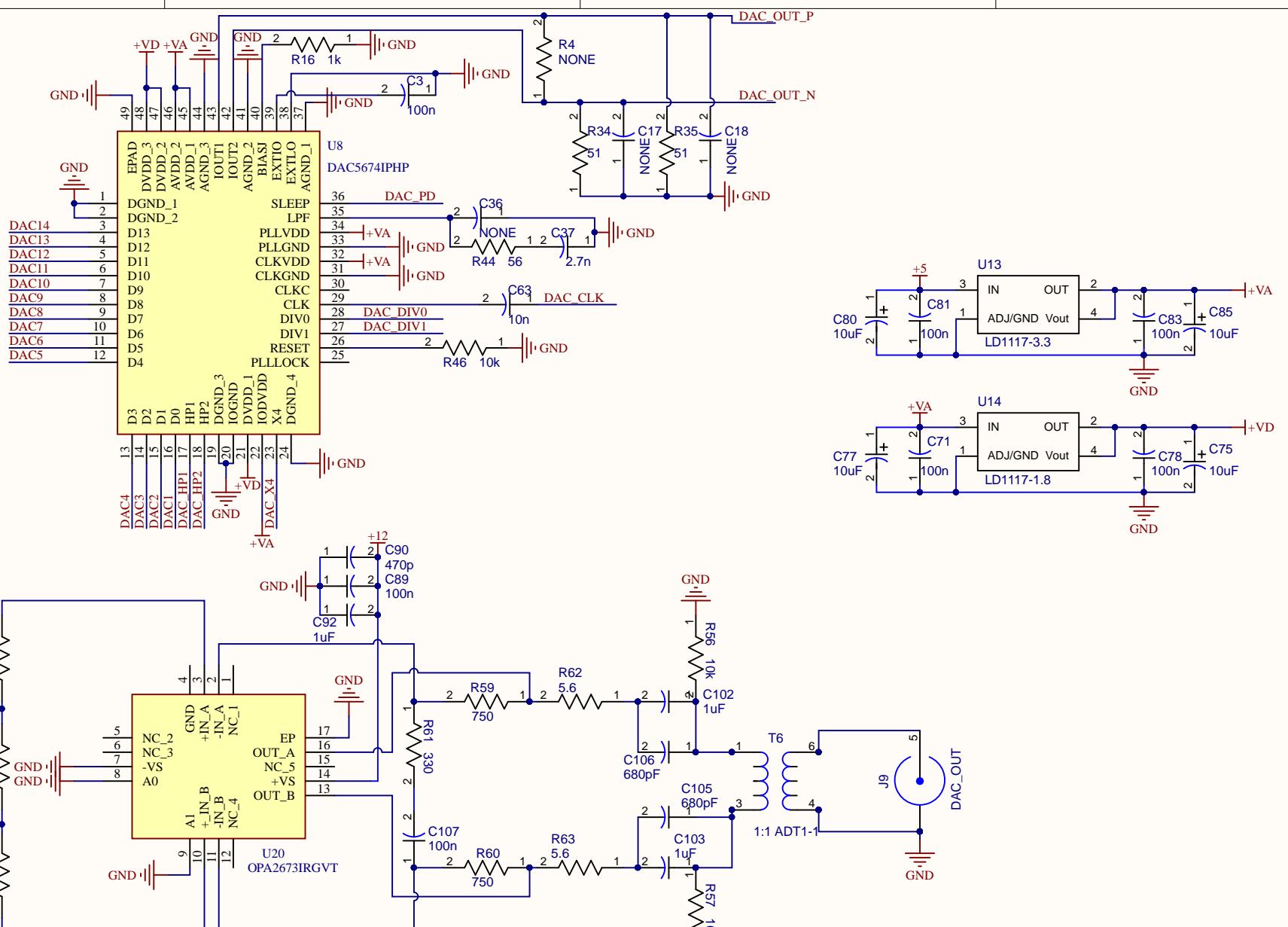


D

Title **CONNECTIONS**

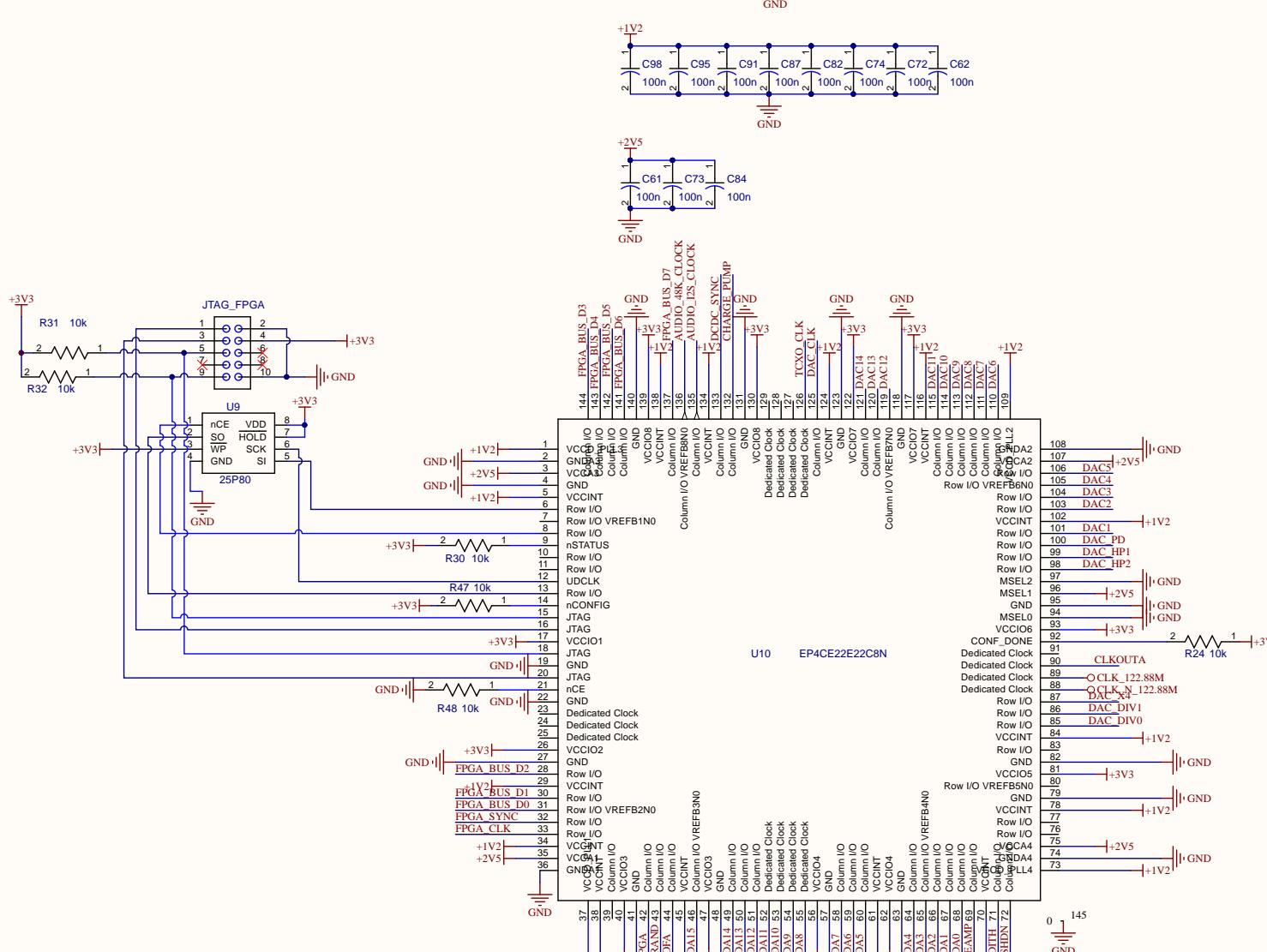
Size: A4	Number: 7	Revision: 2.0
Date: 06.11.2020	Time: 9:33:00	Sheet 7 of 18
File: C:\Dropbox\Develop\Projects\WOLF\Schema\ALTIUM_DESIGNER\MOTHERBOARD\CONNECTIONS.SchDoc		*

**Altium**

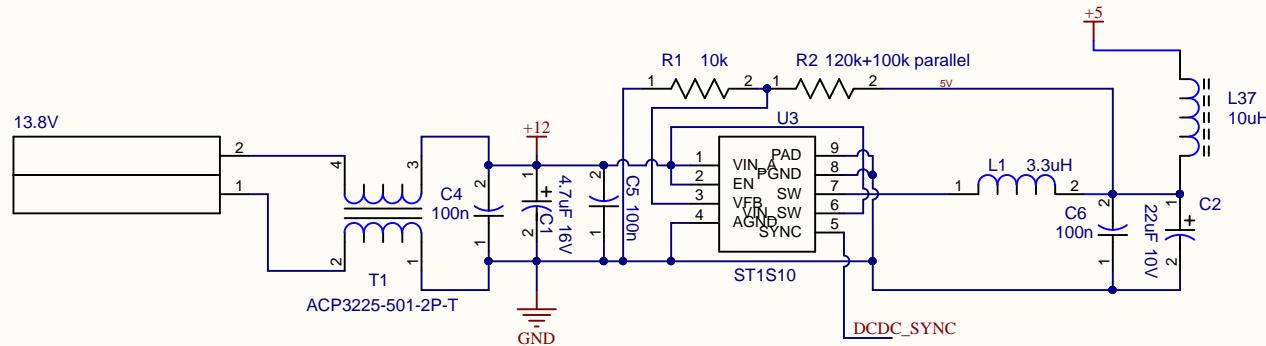


Title <b>DAC</b>		
Size: A4	Number: 8	Revision: 2.0
Date: 06.11.2020	Time: 9:33:01	Sheet 8 of 18
File: C:\Dropbox\Develop\Projects\WOLF\Schema\ALTIUM_DESIGNER\MOTHERBOARD\DAC.SchDoc		*

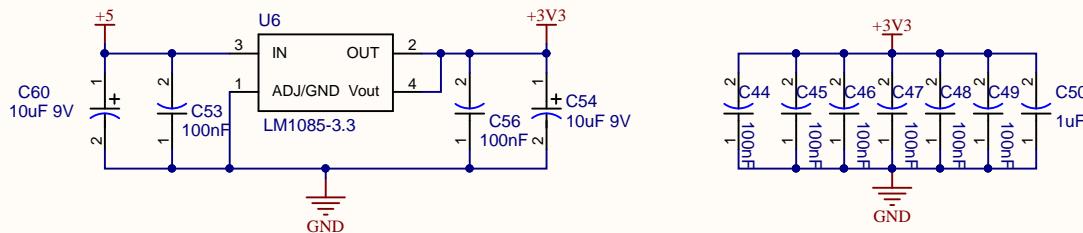
**Altium**



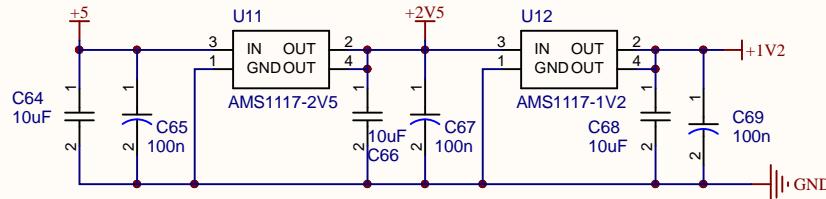
A



B



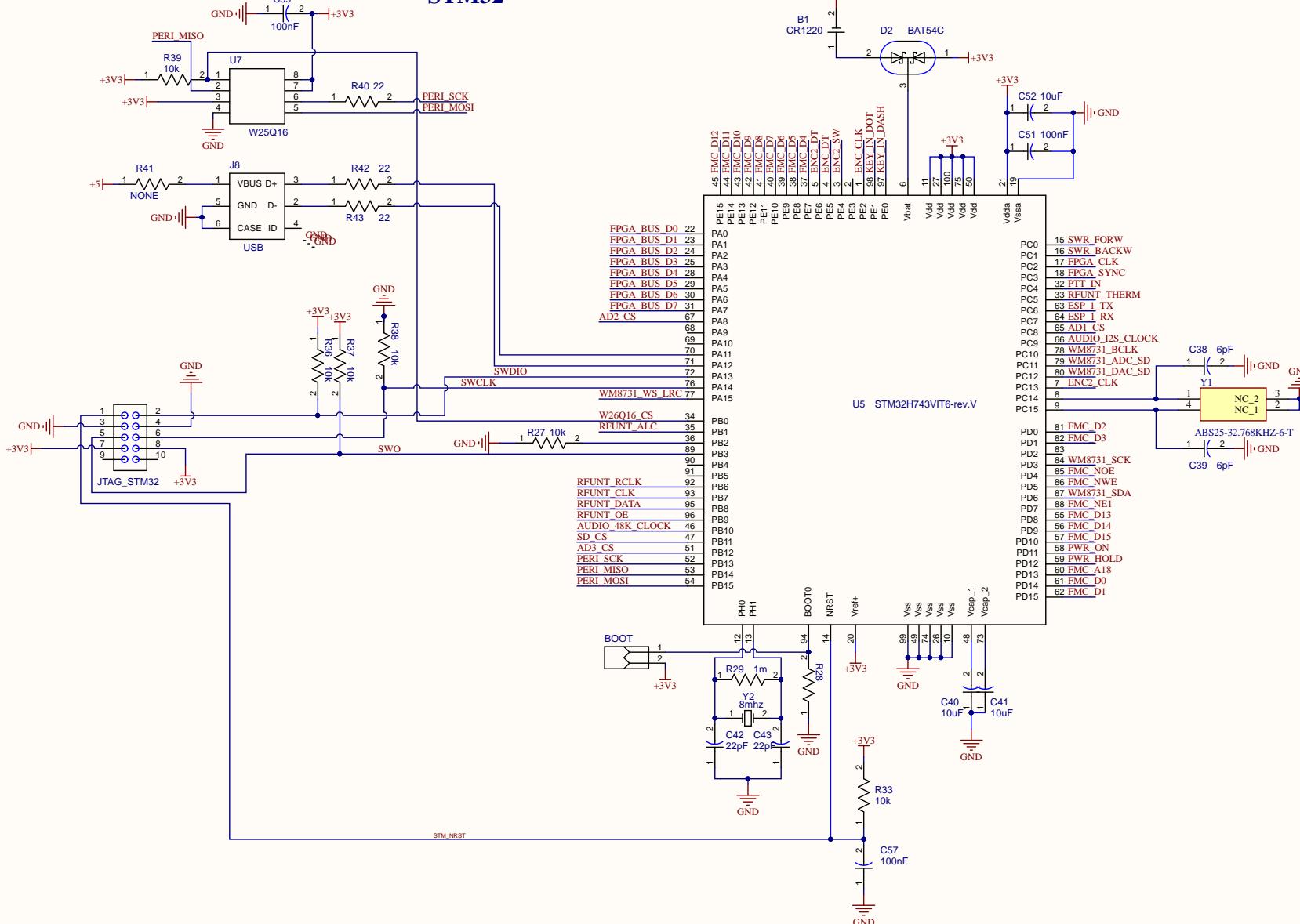
C

Title **POWER**

Size: A4	Number: 10	Revision: 2.0
Date: 06.11.2020	Time: 9:33:02	Sheet 10 of 18
File: C:\Dropbox\Develop\Projects\WOLF\Schema\ALTIUM_DESIGNER\MOTHERBOARD\POWER.SchDoc		*

**Altium**

# STM32



A

A

B

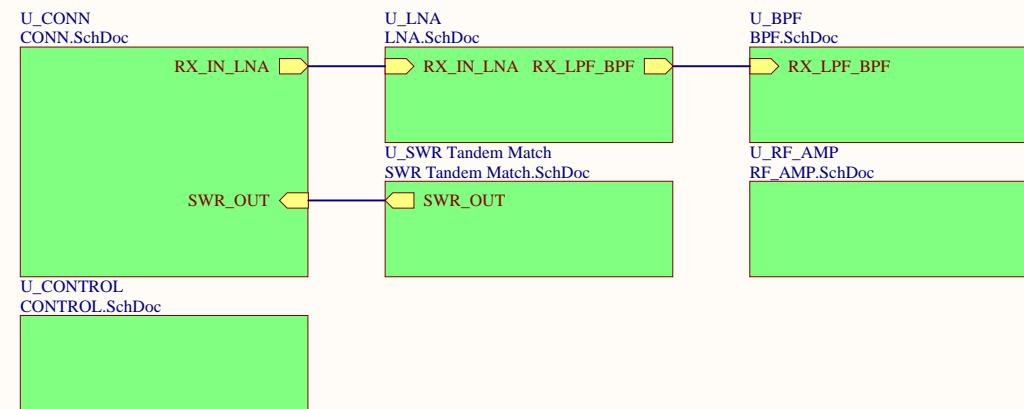
B

C

C

D

D

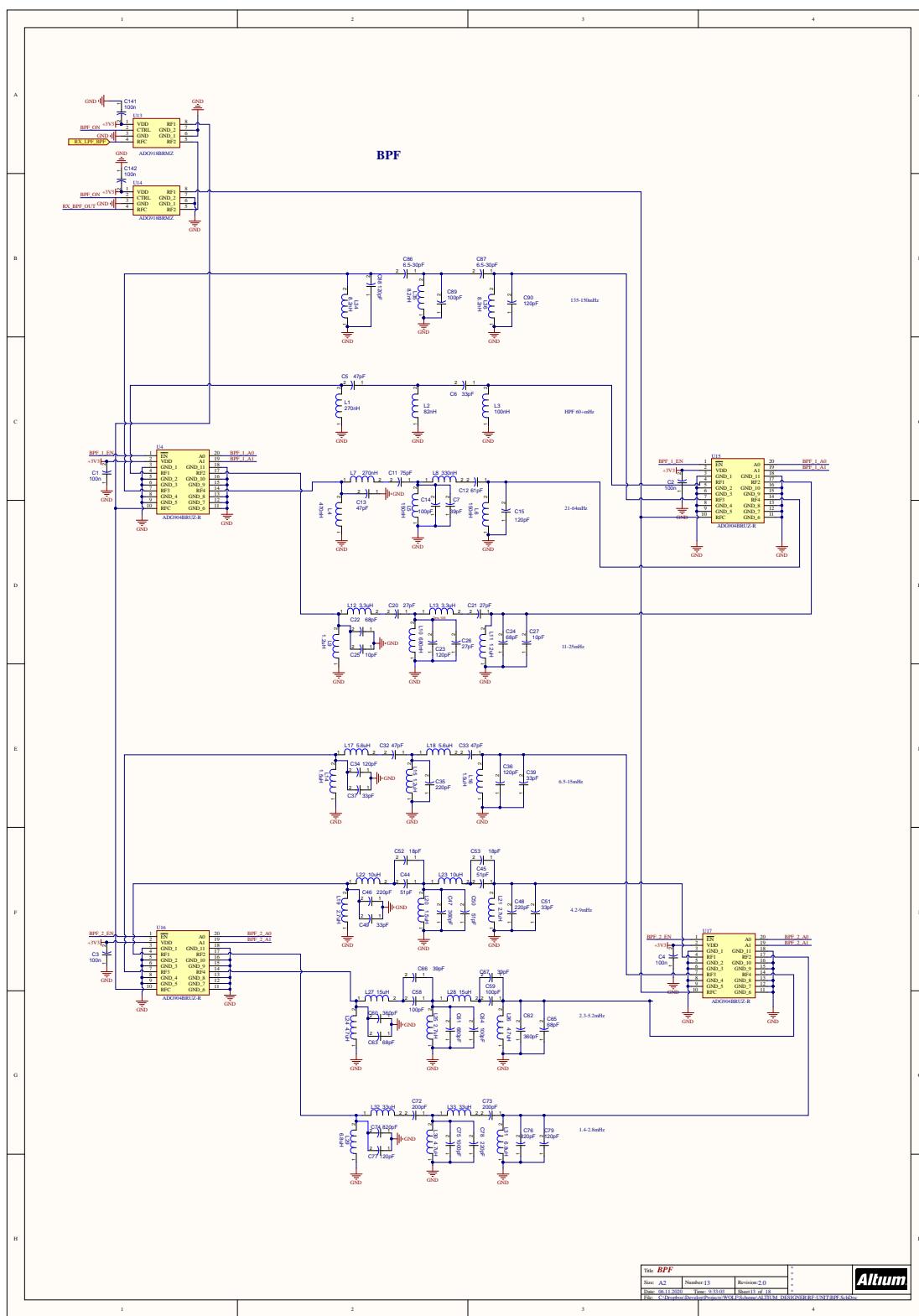
Title ***RF-UNIT***

Size: A4 Number:12 Revision:2.0

Date: 06.11.2020 Time: 9:33:02 Sheet 12 of 18

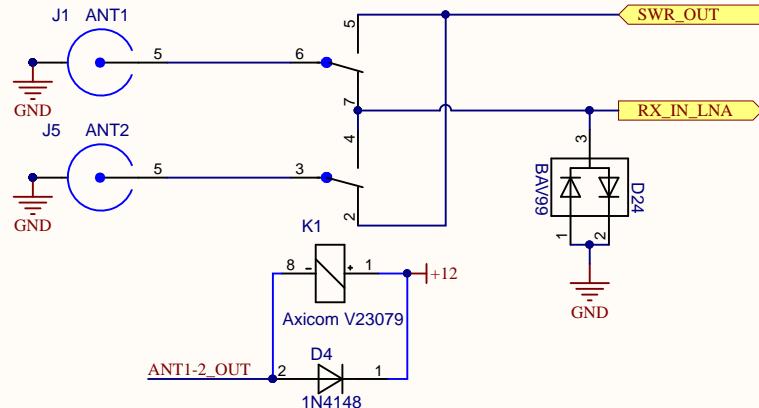
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**Altium**

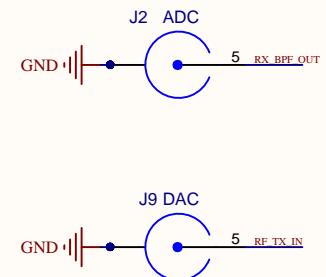


A

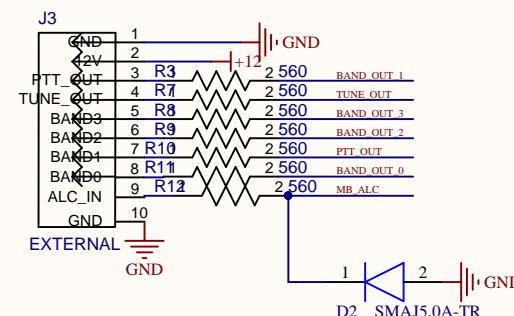
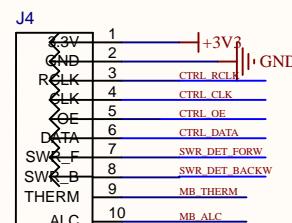
## TXRX\_COMUTATOR



## CONN



B

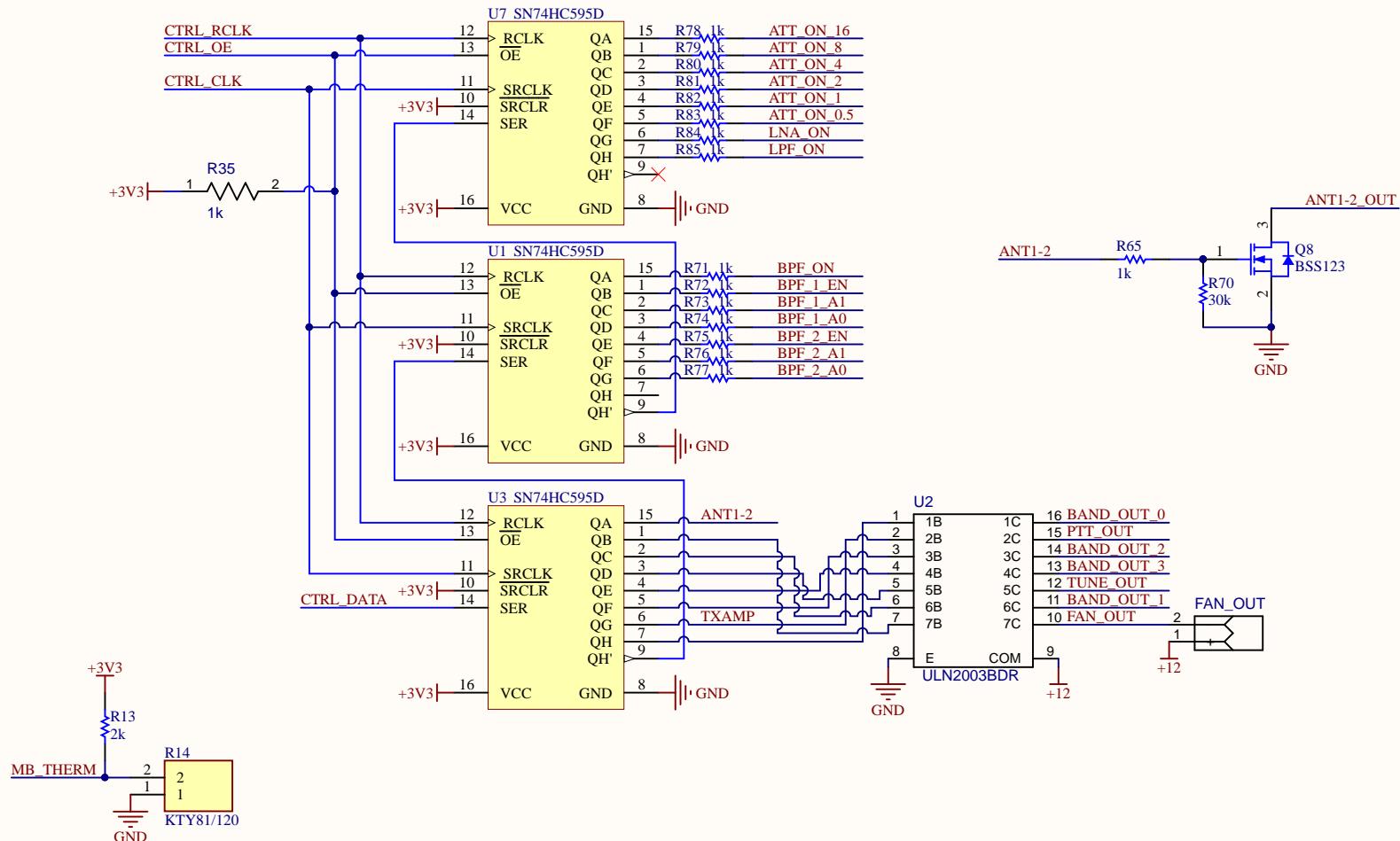


Title: CONN

Size: A4	Number: 14	Revision: 2.0
Date: 06.11.2020	Time: 9:33:03	Sheet 14 of 18
File: C:\Dropbox\Develop\Projects\WOLF\Schema\ALTIUM_DESIGNER\RF-UNIT\CONN.SchDoc		*

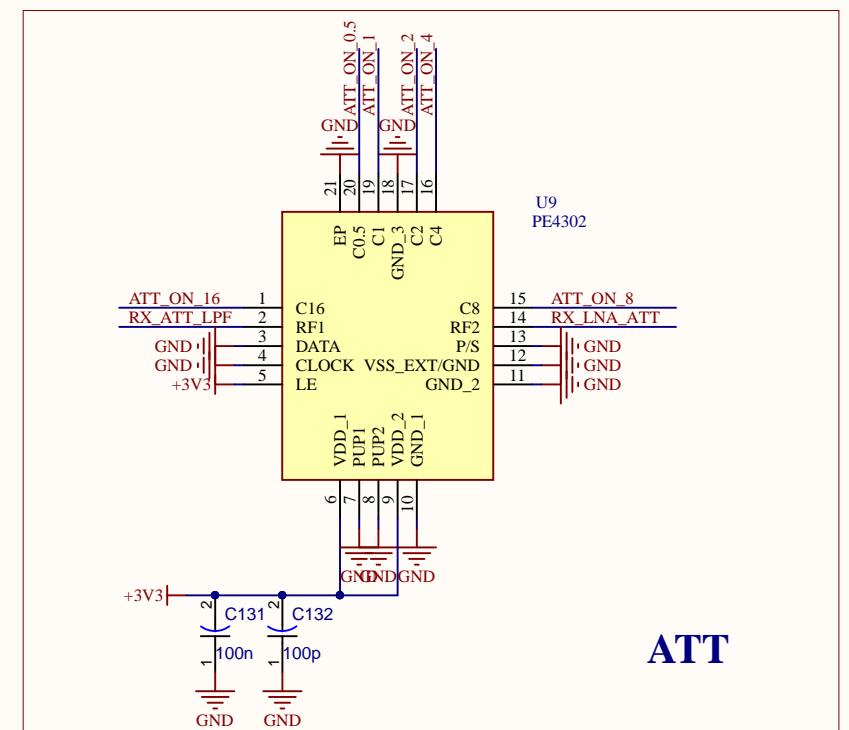
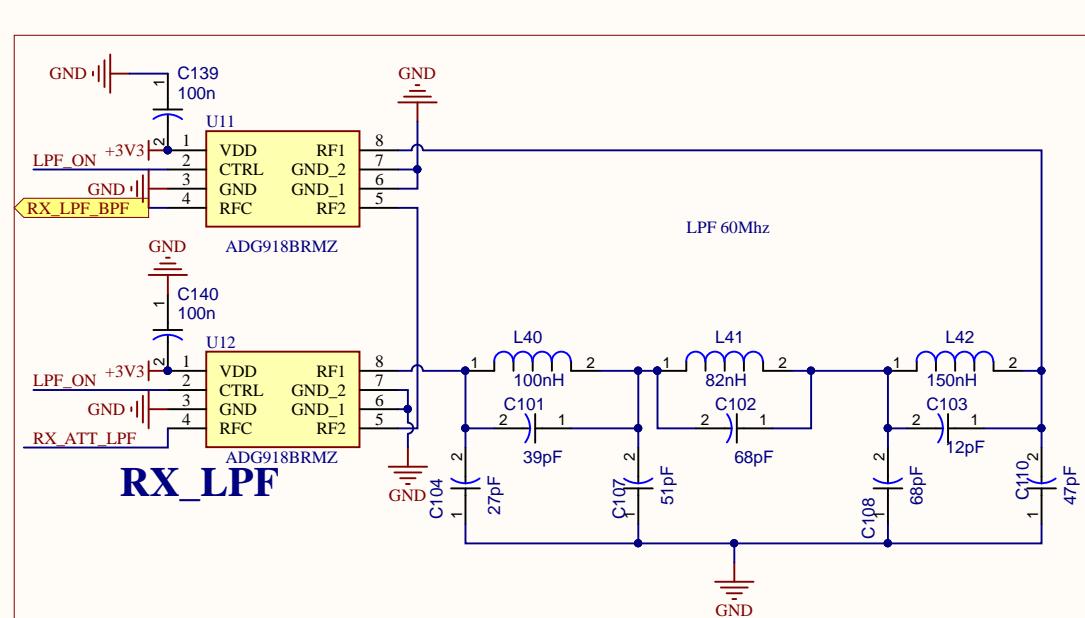
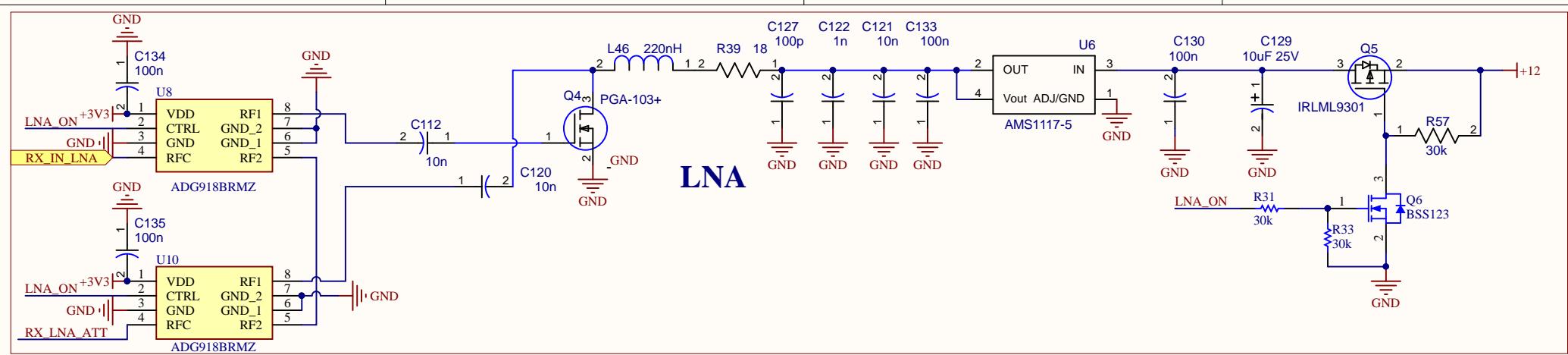
Altium®

A

Title **CONTROL**

Size: A4	Number: 15	Revision: 2.0
Date: 06.11.2020	Time: 9:33:04	Sheet 15 of 18
File: C:\Dropbox\Develop\Projects\WOLF\Schema\ALTIUM_DESIGNER\RF-UNIT\CONTROL.SchDoc		*

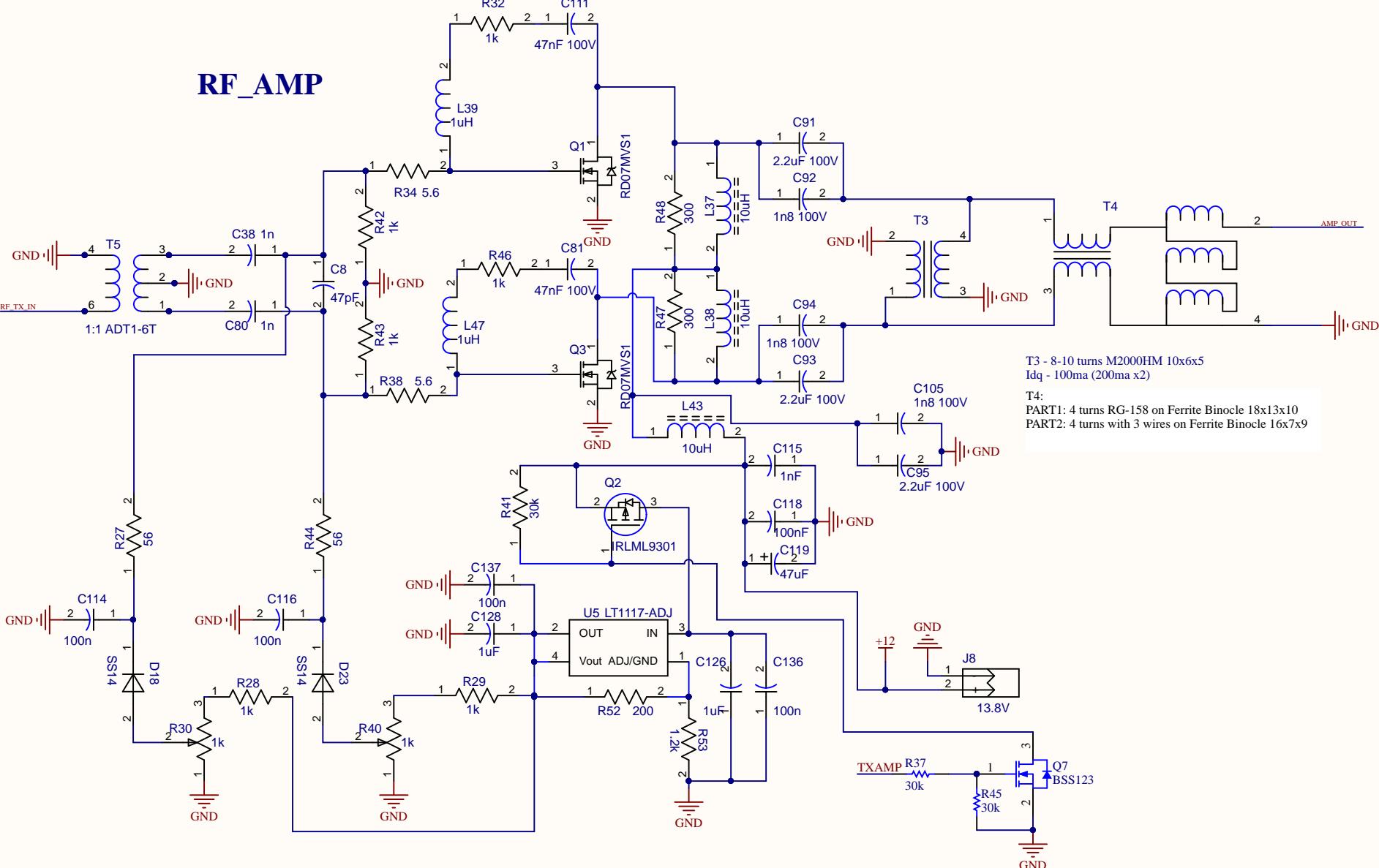
**Altium**



Title <b>LNA</b>			*
Size: A4	Number:16	Revision:2.0	*
Date: 06.11.2020	Time: 9:33:04	Sheet16 of 18	*
File: C:\Dropbox\Develop\Projects\WOLF\Schema\ALTIUM_DESIGNER\RF-UNIT\LNA.SchDoc			

**Altium**

# RF\_AMP



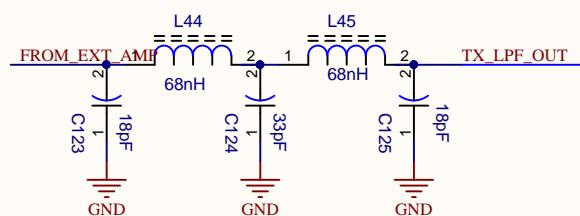
Title **RF\_AMP**

Size: A4	Number: 17	Revision: 2.0
Date: 06.11.2020	Time: 9:33:04	Sheet 17 of 18
File: C:\Dropbox\Develop\Projects\WOLF\Schema\ALTIUM_DESIGNER\RF-UNIT\RF_AMP.SchDoc		*

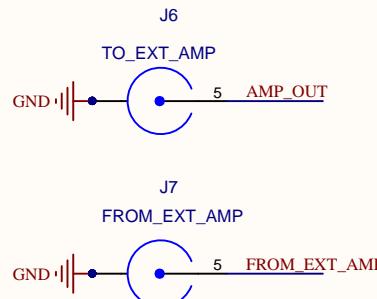
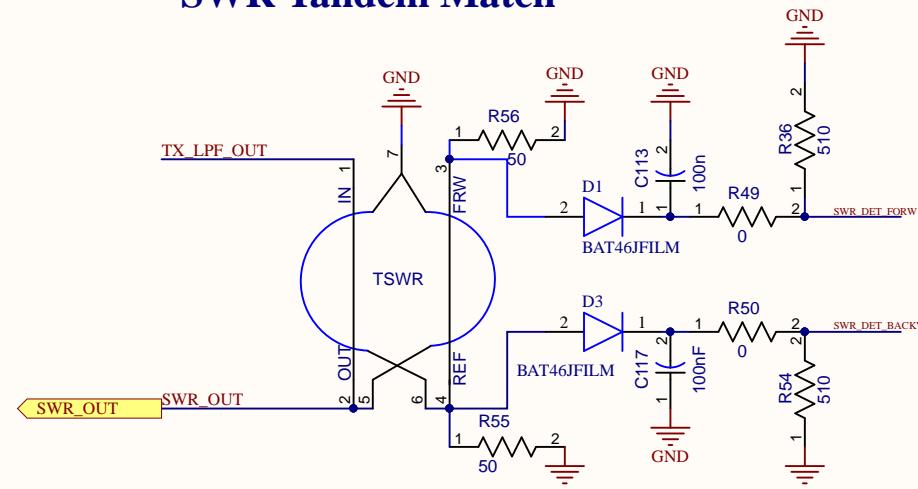


**TX\_LPF**

LPF 170Mhz



Катушки намотаны проводом 0.5мм на оправке диаметром 5мм, 3.5 витка

**SWR Tandem Match**

по диагонали пропущено и намотано по 10 витков 0.5мм

Title **SWR Tandem Match**

Size: A4 Number:18 Revision:2.0

Date: 06.11.2020 Time: 9:33:04 Sheet 18 of 18

File: C:\Dropbox\Develop\Projects\WOLF\Scheme\ALTIUM\_DESIGNER\RF-UNIT\SWR Tandem Match.SchDoc

**Altium**