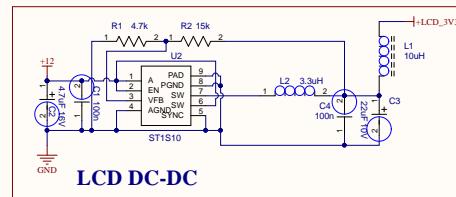


7Inch version



A

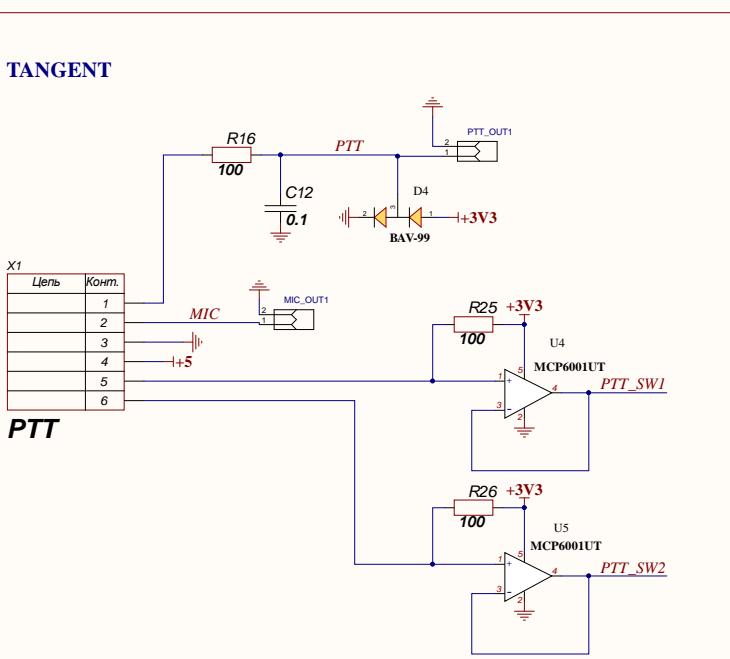
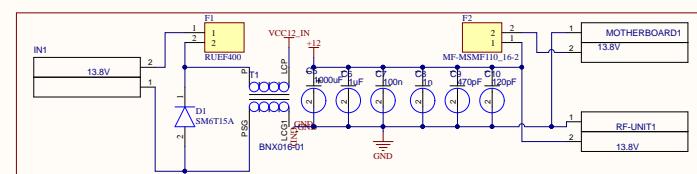
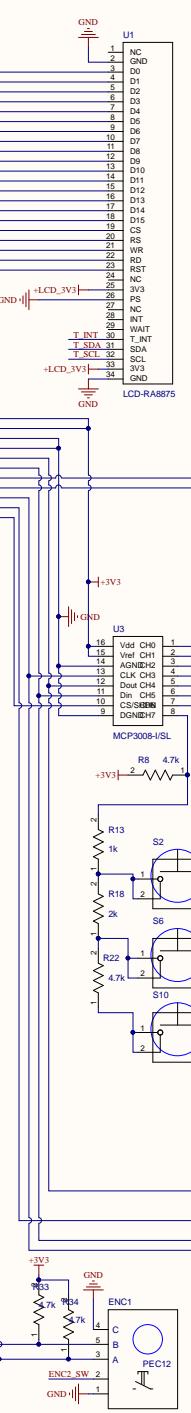
B

C

D

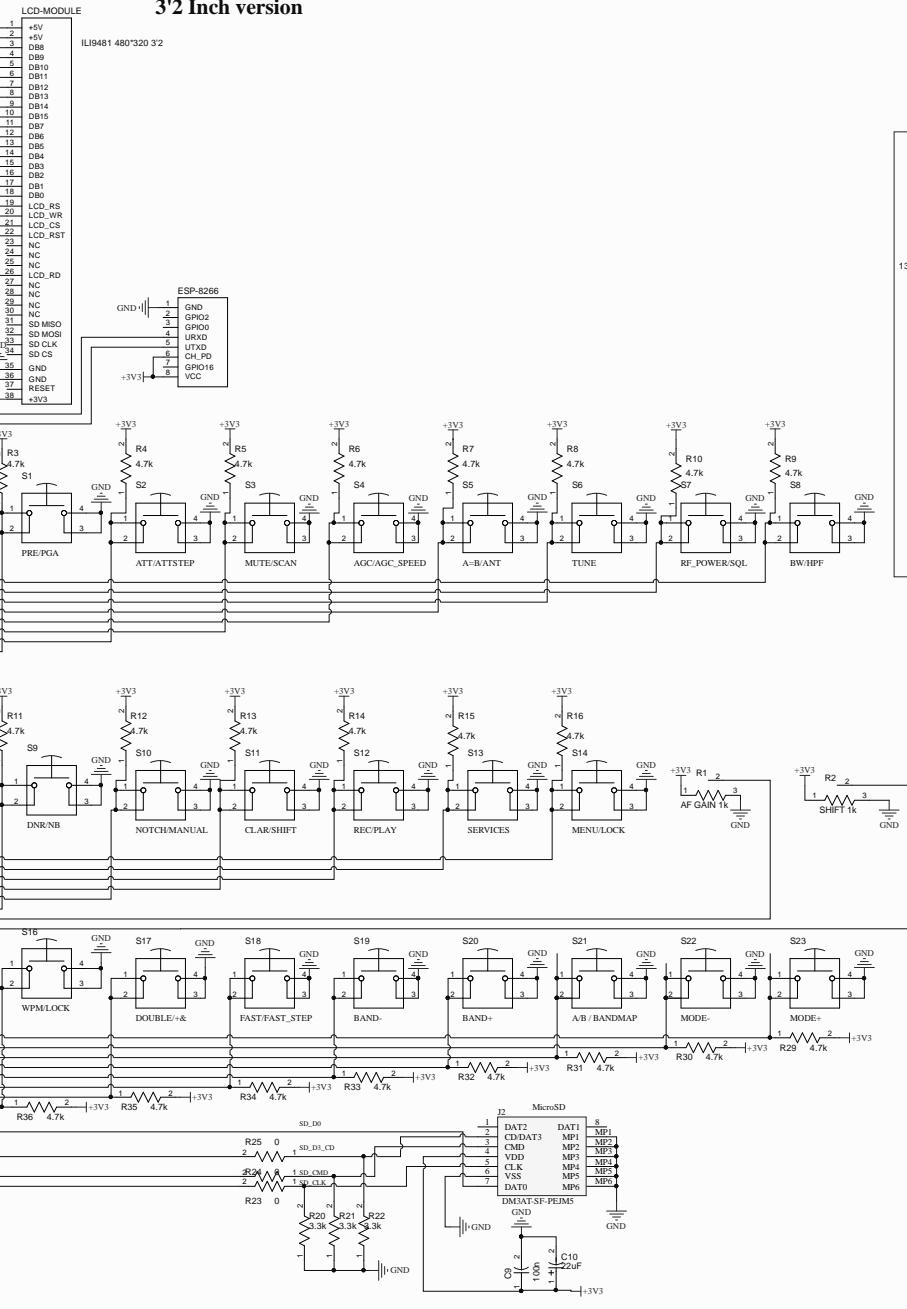
CPU_PV_ON CPU_PV_HOLD PONCAS PHOCAS

FPC-4SP-0.5mm



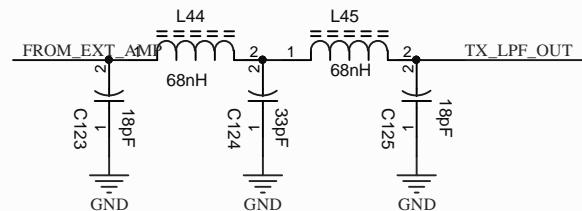
3'2 Inch version

ILI9481 480*320 3'2

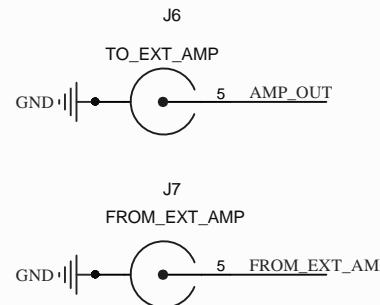
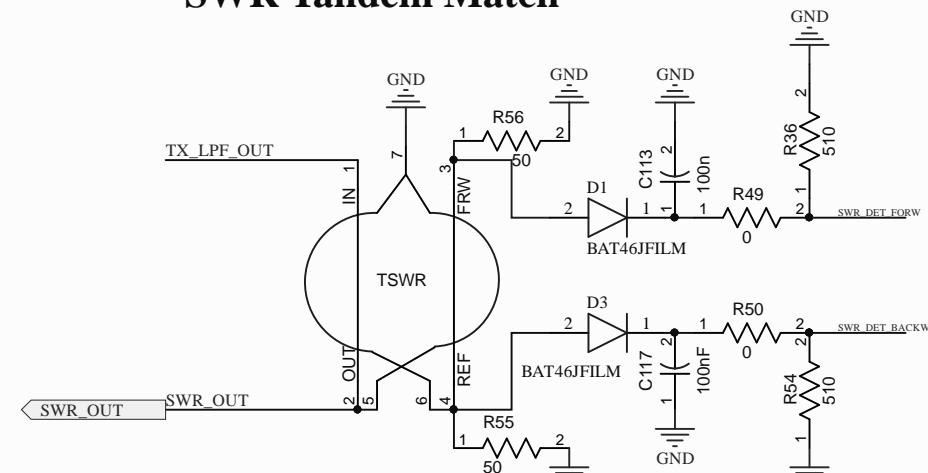


TX_LPF

LPF 170Mhz



Катушки намотаны проводом 0.5мм на оправке диаметром 5мм, 3.5 витка

**SWR Tandem Match**

2 провода 0.9мм пропущено через бинокль

по диагонали пропущено и намотано по 10 витков 0.5мм

Title **SWR Tandem Match**

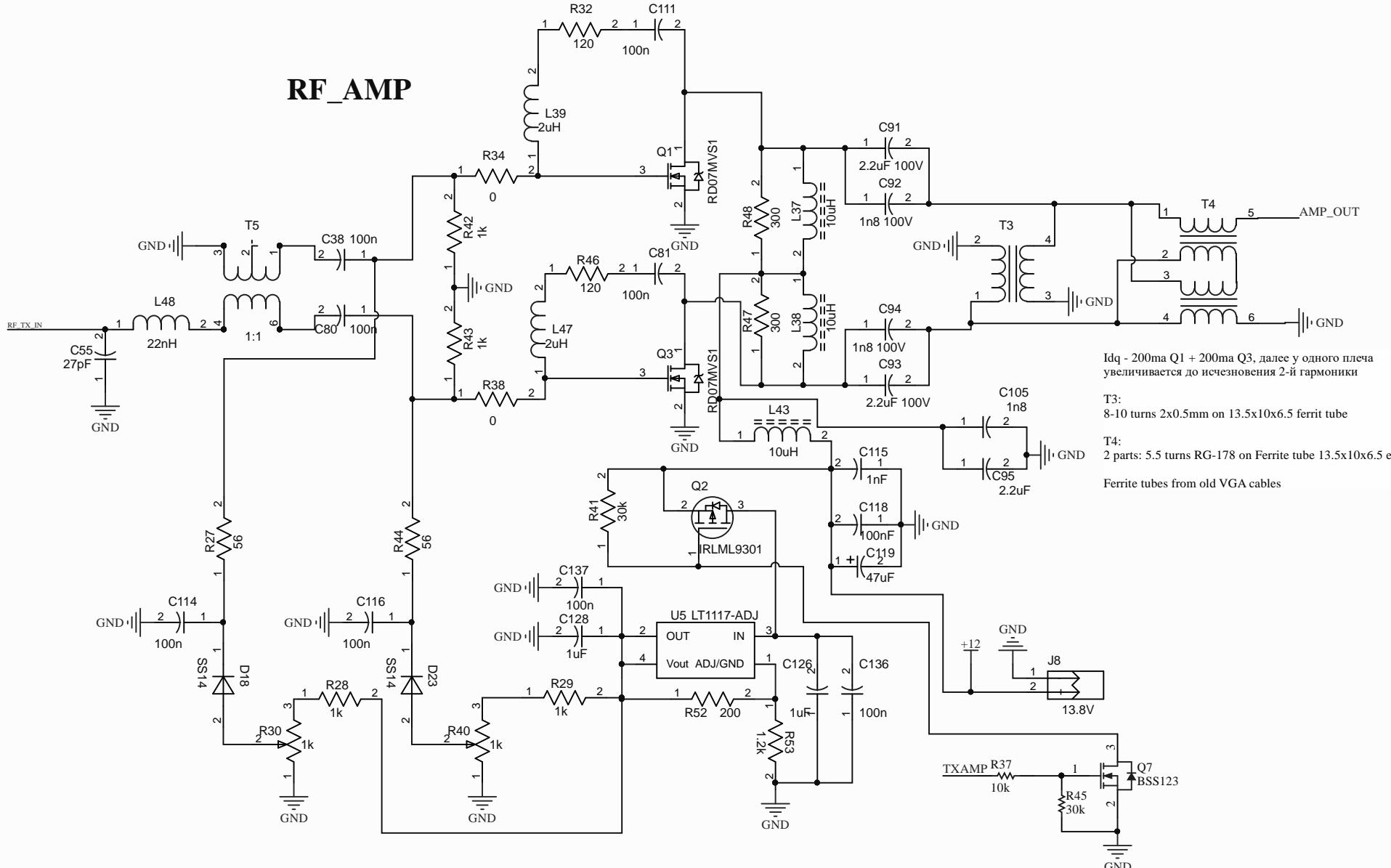
Size: A4 Number:18 Revision:2.0

Date: 20.12.2020 Time: 22:04:05 Sheet:18 of 18

File: D:\Dropbox\Develop\Projects\WOLF\Scheme\ALTIUM_DESIGNER\RF-UNIT\SWR Tandem Match.SchDoc

Altium

A

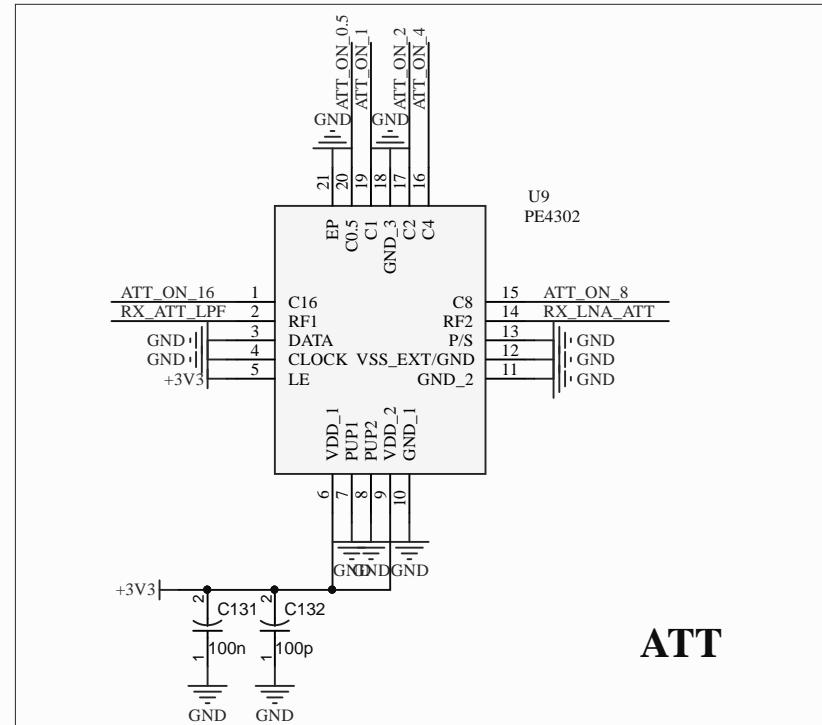
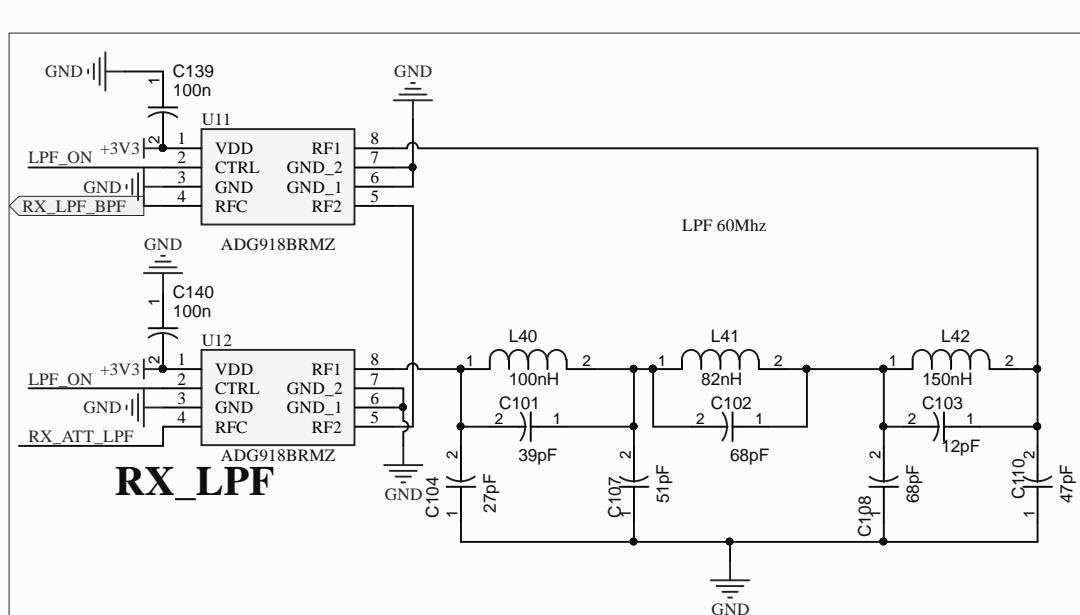
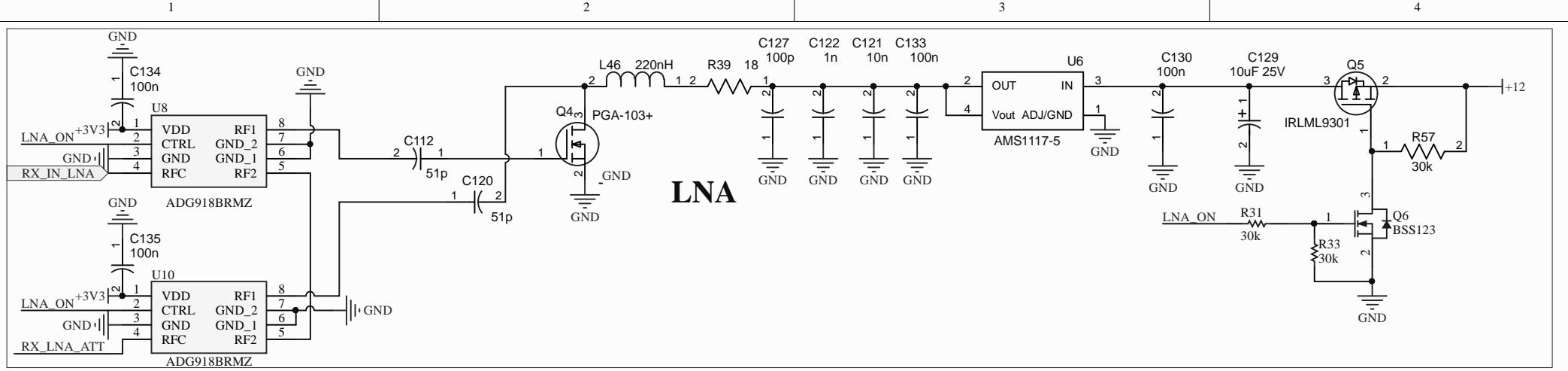
RF_AMPTitle **RF_AMP**

Size: A4 Number:17 Revision:2.0

Date: 20.12.2020 Time: 22:04:07 Sheet:17 of 18

File: D:\Dropbox\Develop\Projects\WOLF\Schema\ALTIUM_DESIGNER\RF-UNIT\RF_AMP.SchDoc

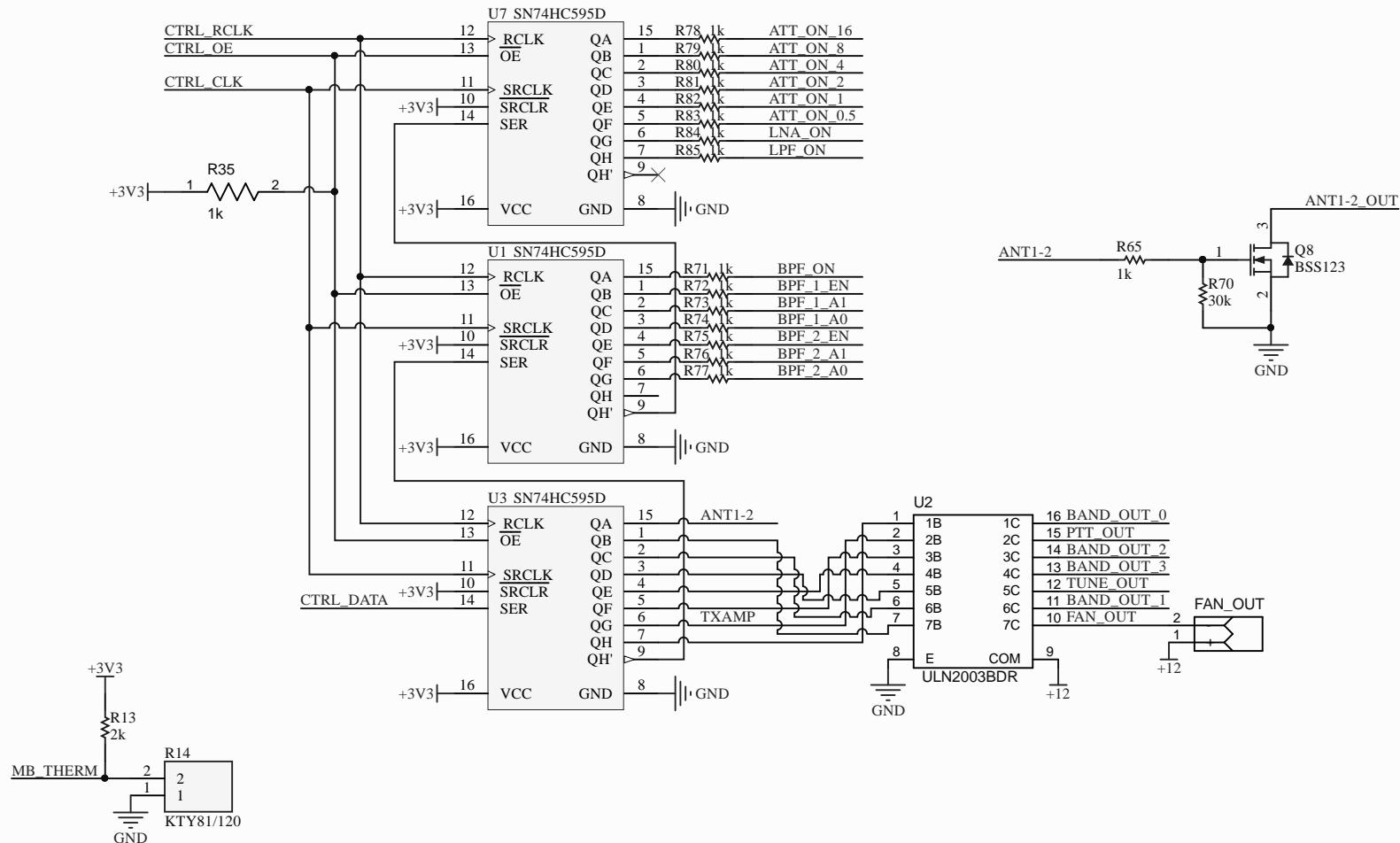
Altium



Title LNA			*
Size: A4	Number:16	Revision2.0	*
Date: 20.12.2020	Time: 22:04:09	Sheet16 of 18	*
File: D:\Dropbox\Develop\Projects\WOLF\Schema\ALTIUM_DESIGNER\RF-UNIT\LNA.SchDoc			

Altium

A

Title **CONTROL**

Size: A4 Number:15 Revision:2.0

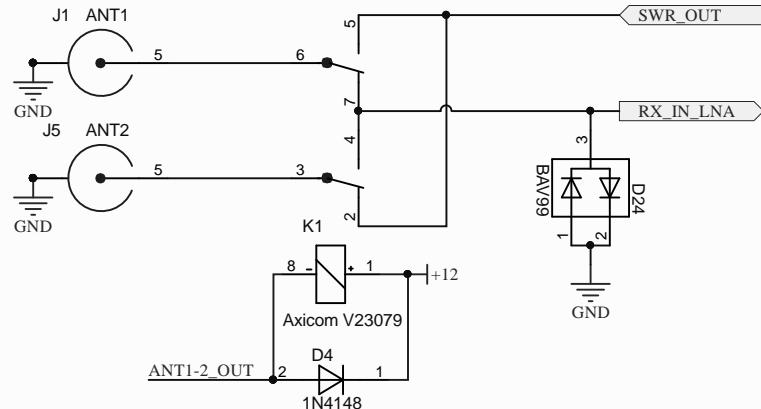
Date: 20.12.2020 Time: 22:04:11 Sheet 15 of 18

File: D:\Dropbox\Develop\Projects\WOLF\Scheme\ALTIUM_DESIGNER\RF-UNIT\CONTROL.SchDoc

Altium

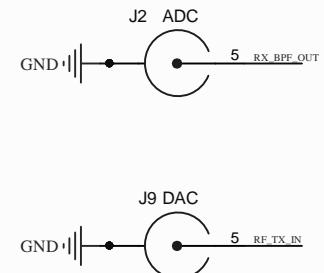
A

TXRX_COMUTATOR



B

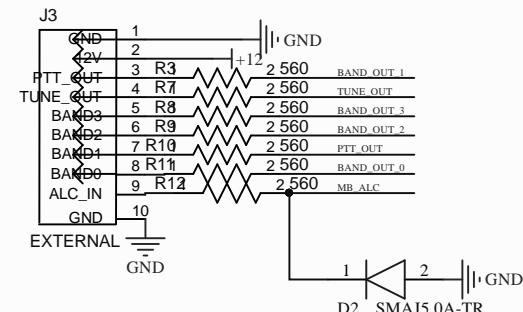
CONN



c

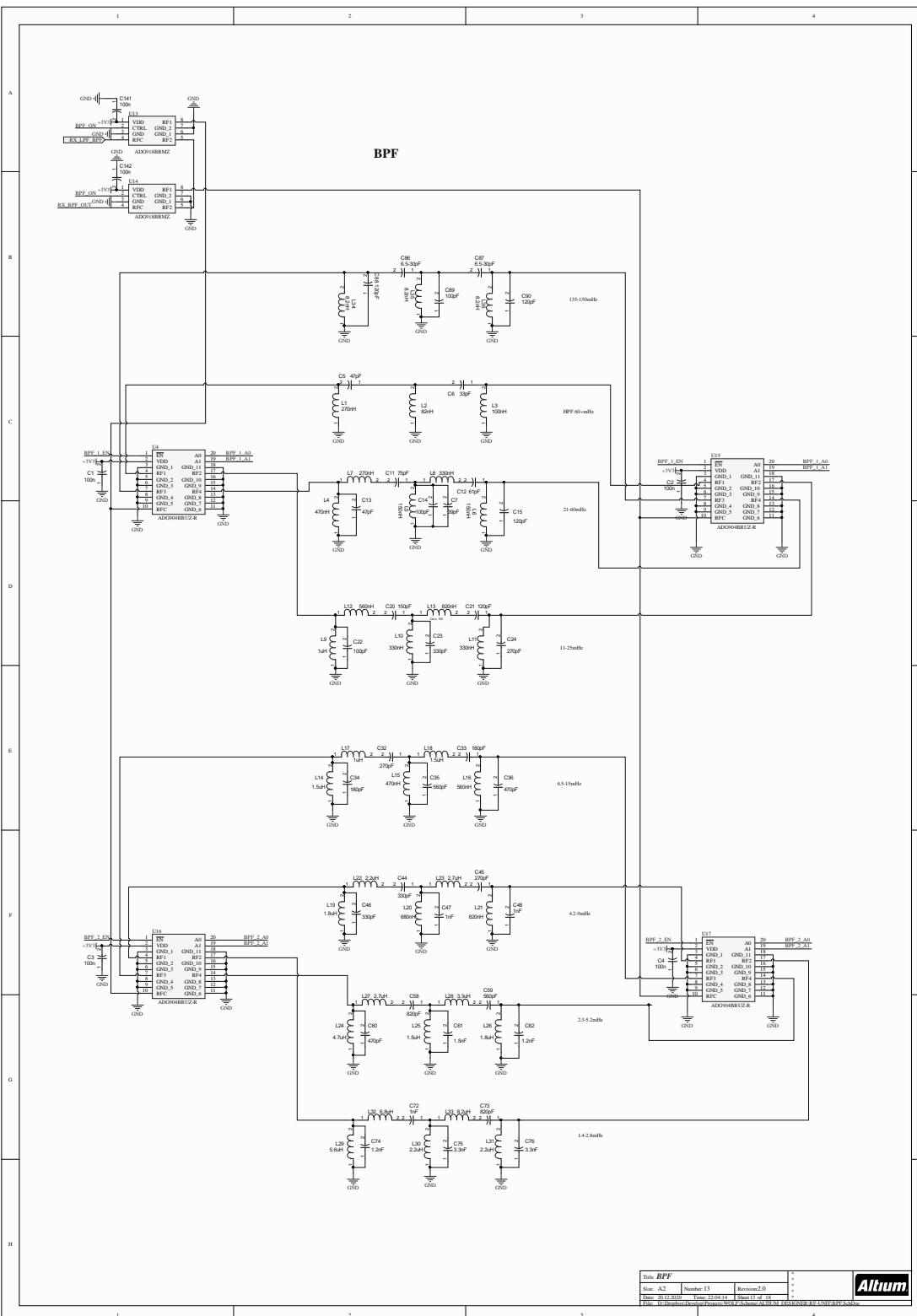
\triangle 3V	1	+3V ₃
GND	2	
RELK	3	CTRL_RELK
CLK	4	CTRL_CLK
\triangle OE	5	CTRL_OE
DATA	6	CTRL_DATA
SWR_F	7	SWR_DET_FORW
SWR_B	8	SWR_DET_BACKW
THERM	9	MB_THERM
A/LC	10	MB_A/LC

MOTHERBOARD

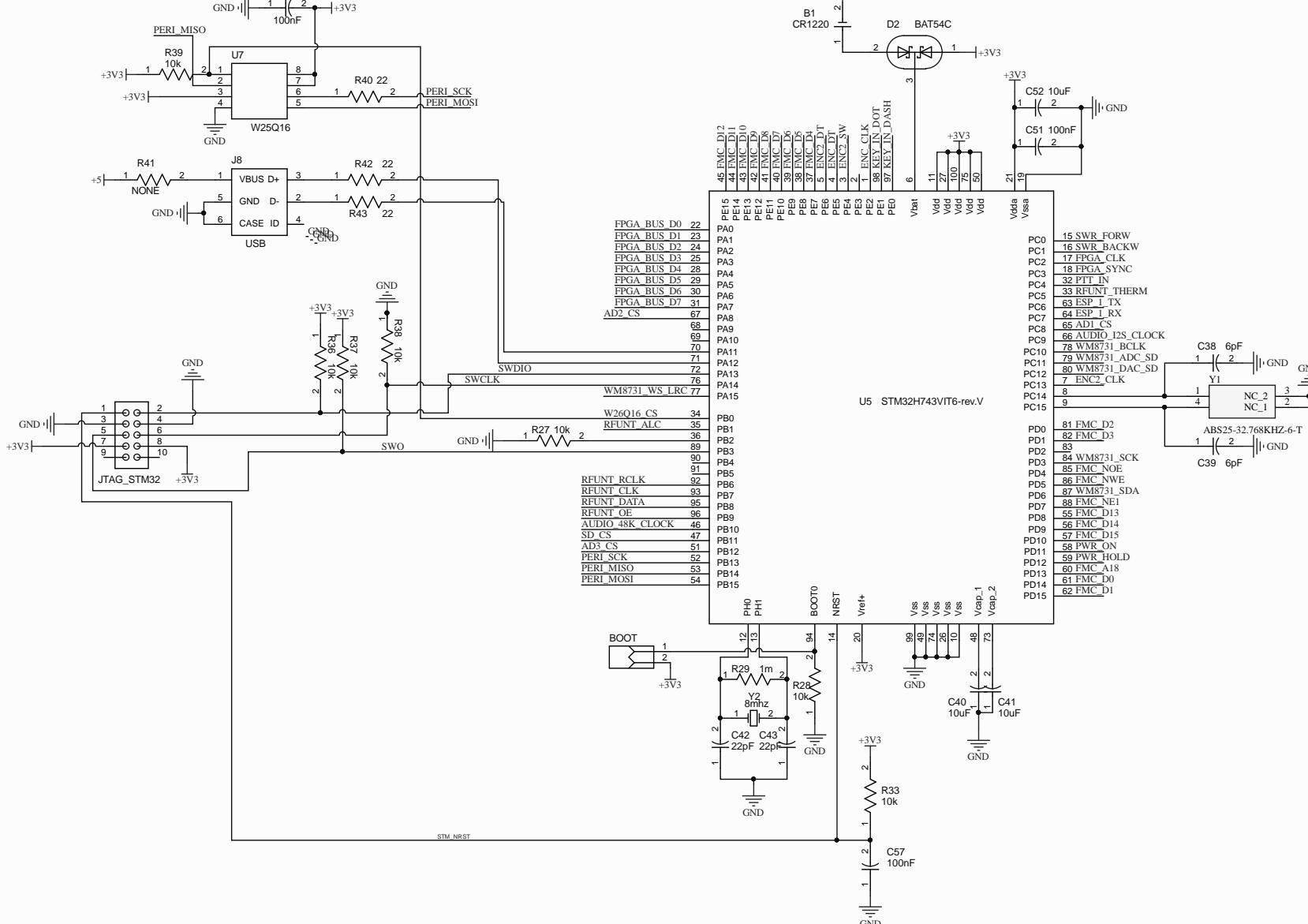


B

Title <i>CONN</i>	*		
Size: A4	Number:14		*
Revision2,0			*
Date: 20.12.2020	Time: 22:04:12		Sheet14 of 18
File: D:\Dropbox\Develop\Projects\WOLF\Scheme\ALTUIM DESIGNER\RF-UNIT\CONN.SchDoc			



STM32

Title **STM32**

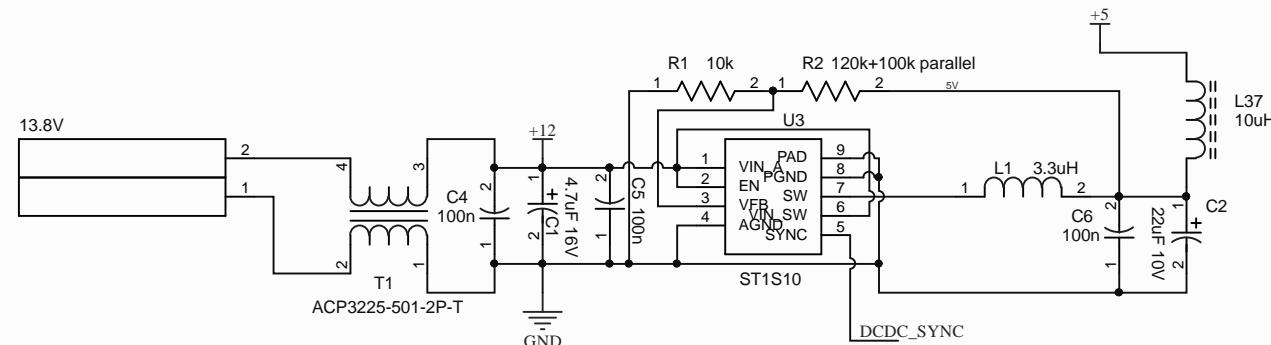
Size: A3 Number: 11 Revision: 2.0

Date: 20.12.2020 Time: 22:04:17 Sheet 11 of 18

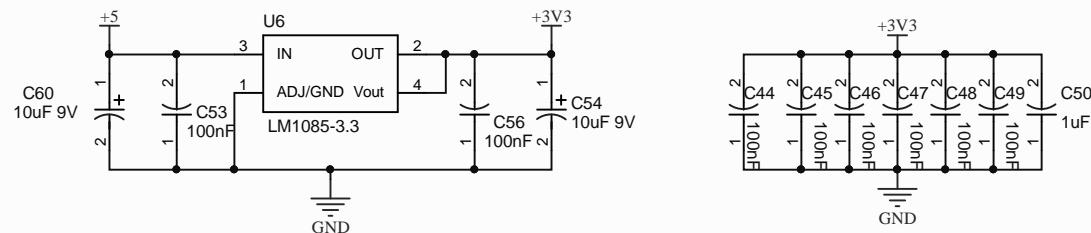
File: D:\Dropbox\Develop\Projects\WOLF\Scheme\ALTIUM DESIGNER\MOTHERBOARD\STM32.SchDoc

Altium

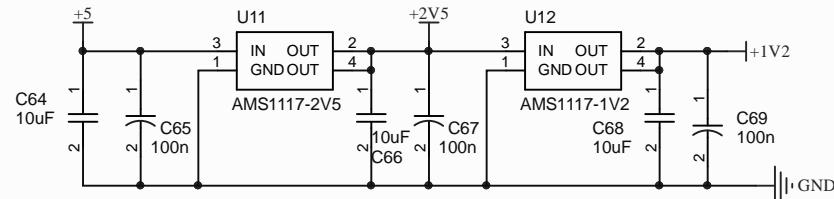
A



B



C

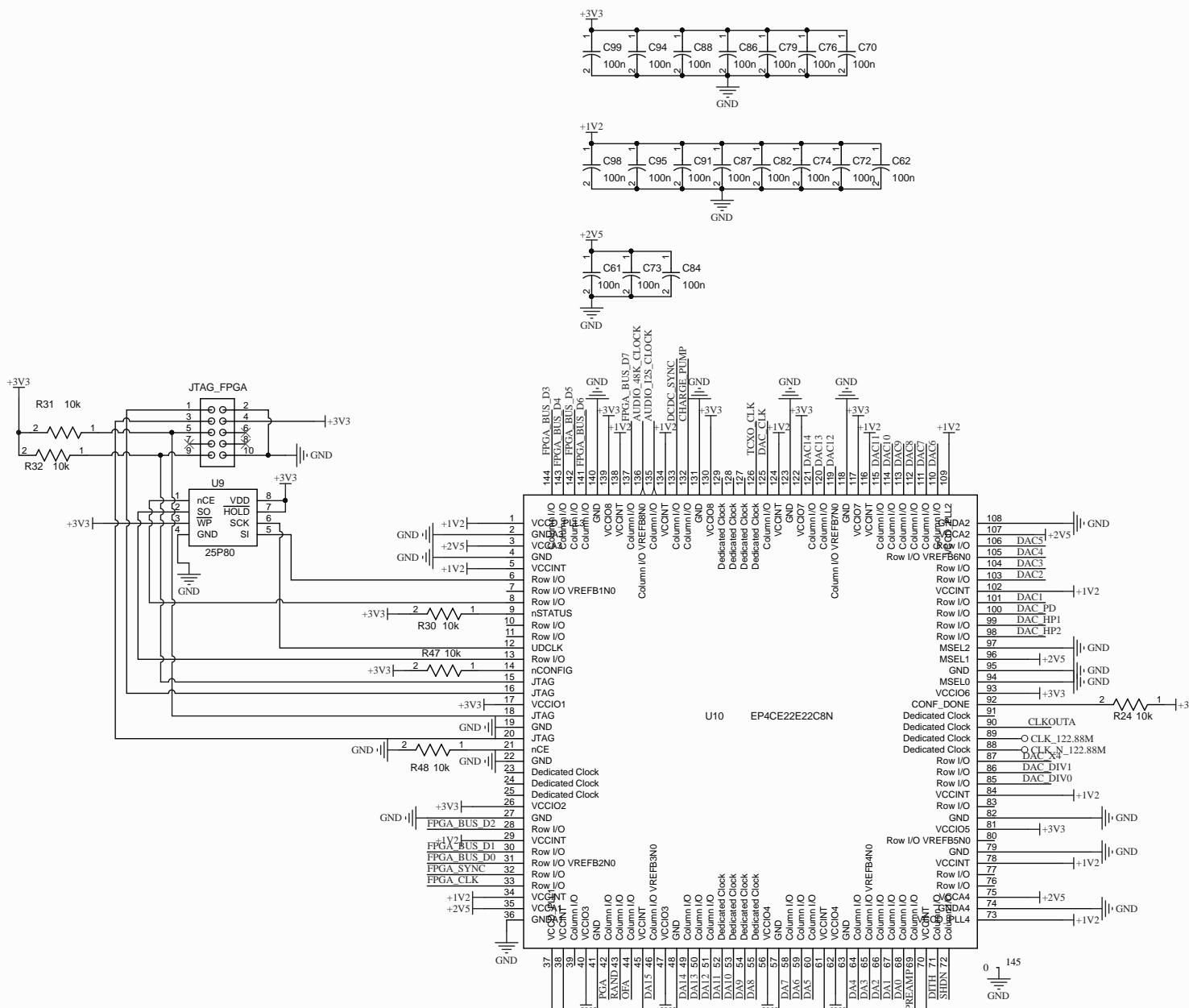
Title **POWER**

Size: A4 Number:10 Revision:2.0

Date: 20.12.2020 Time: 22:04:19 Sheet 10 of 18

File: D:\Dropbox\Develop\Projects\WOLF\Scheme\ALTIUM_DESIGNER\MOTHERBOARD\POWER.SchDoc

Altium

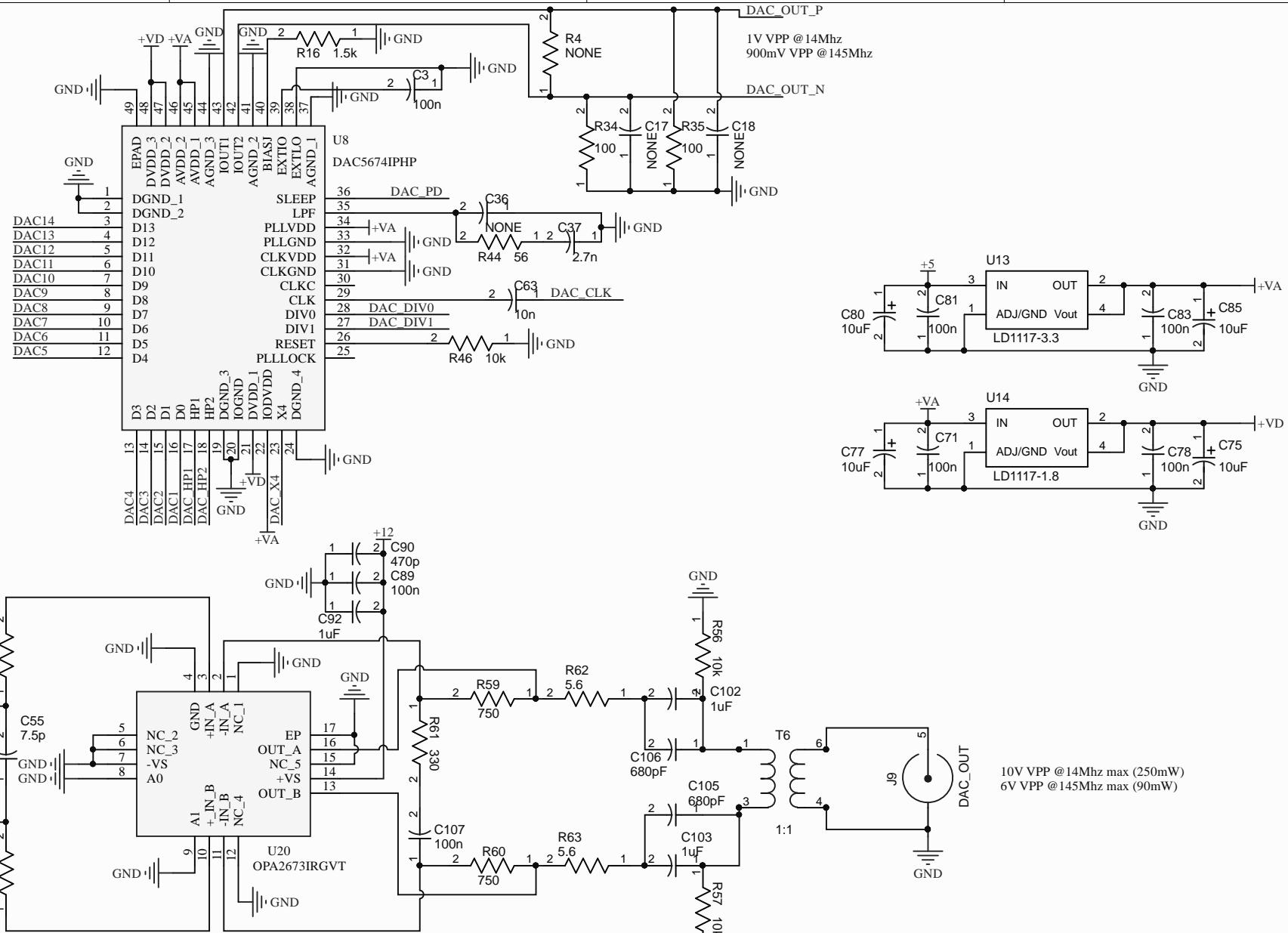


Title **FPGA**

Size: A3
Date: 20.12.20

Number:9 Revision:2.0
Time: 22:04:22 Sheet 9 of 18

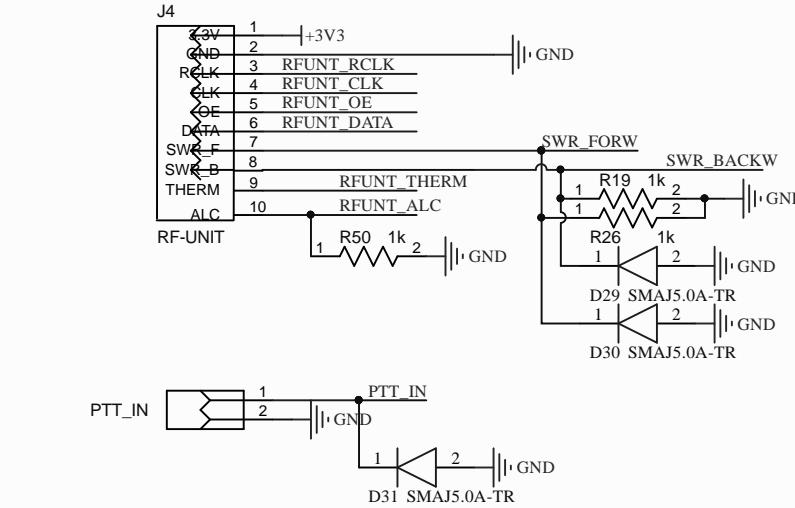
Altium



10V VPP @ 14Mhz max (250mW)
6V VPP @ 145Mhz max (90mW)

Title DAC			*	
			*	
Size: A4	Number:8	Revision:2.0	*	
Date: 20.12.2020	Time: 22:04:24	Sheet 8 of 18	*	
File: D:\Dropbox\Develop\Projects\WOLF\Scheme\ALTIUM_DESIGNER\MOTHERBOARD\DAC.SchDoc				

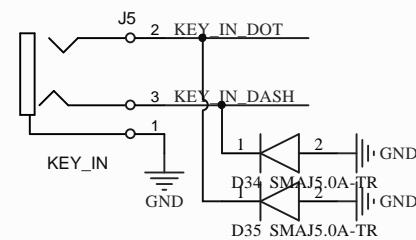
A



J6

1	CS 3v3
2	FMC_A18
3	RS 3v3
4	WR GND
5	RD GND
6	STM_NRST
7	RST_MISO
8	FMC_D1
9	FMC_D2
10	FMC_D3
11	FMC_D4
12	FMC_D5
13	FMC_D6
14	FMC_D7
15	FMC_D8
16	FMC_D9
17	FMC_D10
18	FMC_D11
19	FMC_D12
20	FMC_D13
21	FMC_D14
22	PWR_ON
23	PWR_HOLD
24	+3V3
25	PERI_MOSI
26	DB0_MOSI
27	DB1_WRX
28	DB2_WTX
29	DB3_CLK
30	DB4\$DCS
31	DB5@1C
32	DB6@2C
33	DB7_E2A
34	DB8_E2B
35	DB9_E2S
36	DB10@1A
37	DB11@1B
38	DB12@3C
39	DB13_5v
40	DB14@ND
41	DB15@ND
42	DB16@ND
43	+5
44	PONCAS
45	PHOCAS
46	3v3
47	GND

FPC-45P-0.5mm



Title **CONNECTIONS**

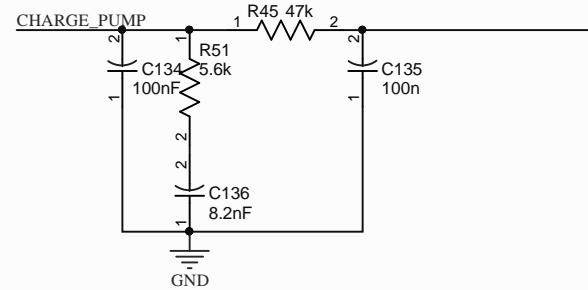
Size: A4	Number:7	Revision2.0
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Date: 20.12.2020	Time: 22:04:26	Sheet7 of 18
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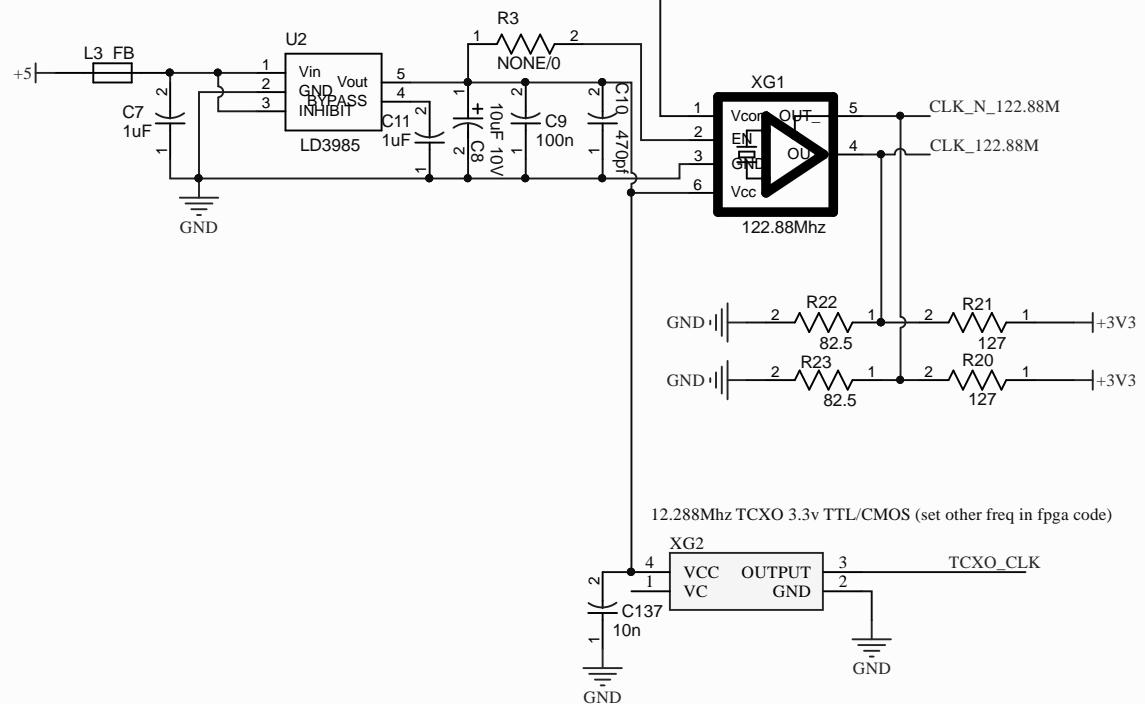
File: D:\Dropbox\Develop\Projects\WOLF\Scheme\ALTIUM_DESIGNER\MOTHERBOARD\CONNECTIONS.SchDoc	*
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Altium

A



B



C

D

Title **CLOCK_GENERATOR**

Size: A4 Number:6 Revision 2.0

Date: 20.12.2020 Time: 22:04:28 Sheet 6 of 18

File: D:\Dropbox\Develop\Projects\WOLF\Schema\ALTIUM_DESIGNER\MOTHERBOARD\CLOCK_GENERATOR.SchDoc

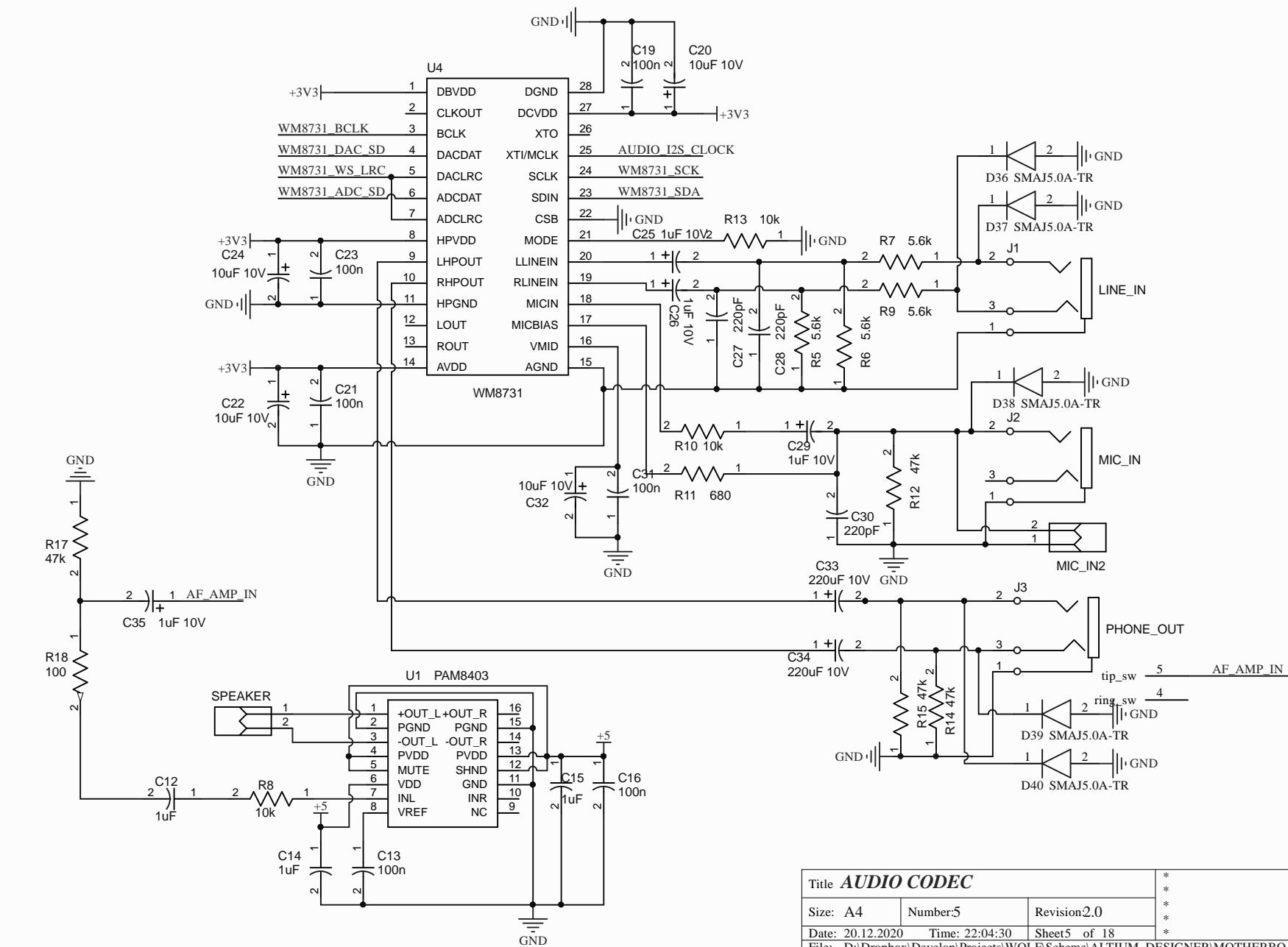
Altium

A

B

C

D

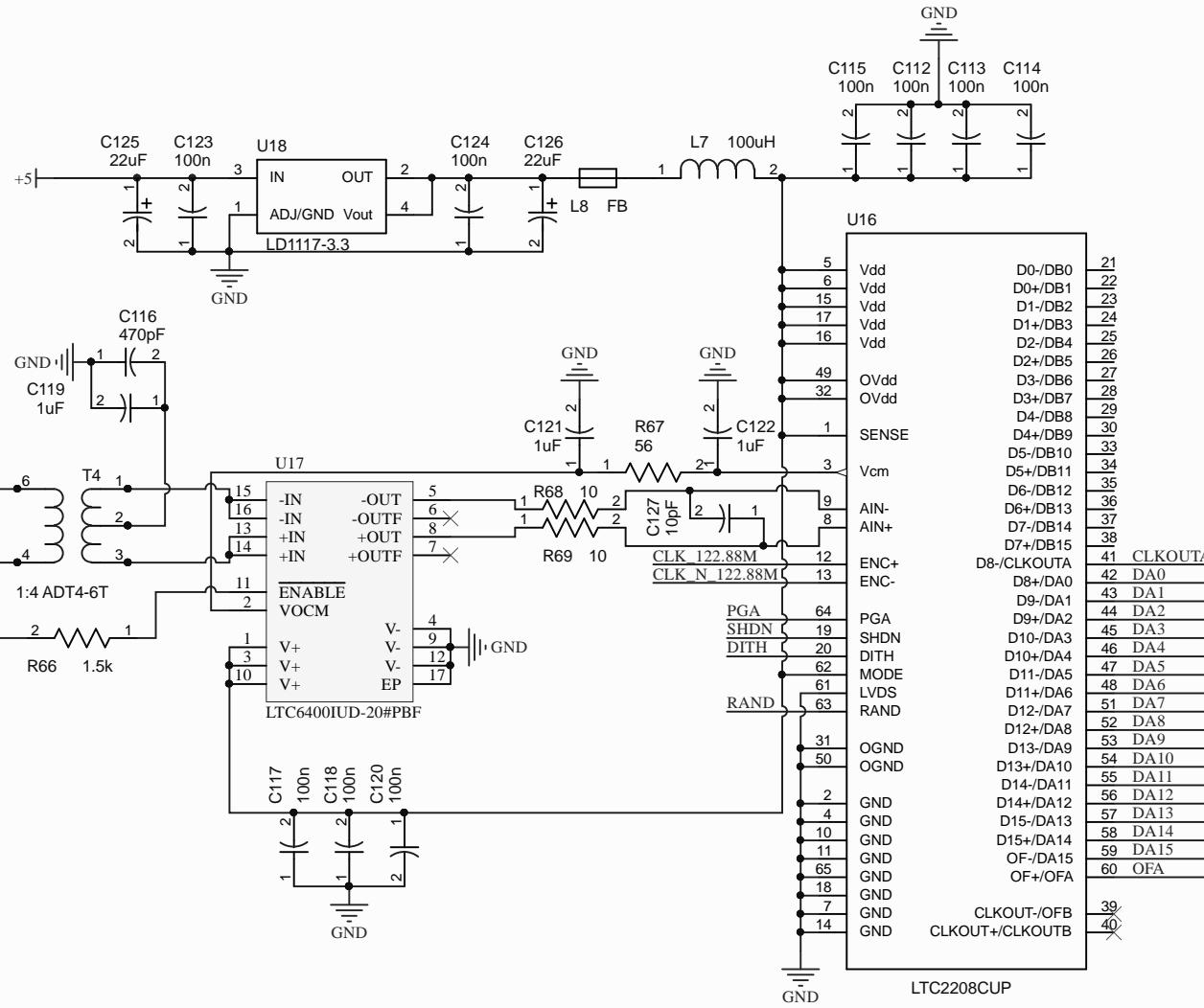
Title **AUDIO CODEC**

Size: A4 Number:5 Revision:2.0

Date: 20.12.2020 Time: 22:04:30 Sheet 5 of 18

File: D:\Dropbox\Develop\Projects\WOLF\Scheme\ALTIUM_DESIGNER\MOTHERBOARD\AUDIO_CODEC.SchDoc

Altium

Title **ADC**

Size: A4 Number:3 Revision 2.0

Date: 20.12.2020 Time: 22:04:32 Sheet 3 of 18

File: D:\Dropbox\Develop\Projects\WOLF\Scheme\ALTIUM_DESIGNER\MOTHERBOARD\ADC.SchDoc

Altium