

A

U_POWER
POWER.SchDoc

U_CLOCK_GENERATOR
CLOCK_GENERATOR.SchDoc

B

U_CONNECTIONS
CONNECTIONS.SchDoc

U_FPGA
FPGA.SchDoc

U_STM32
STM32.SchDoc

U_AUDIO_CODEC
AUDIO_CODEC.SchDoc

C

U_DAC
DAC.SchDoc

U_ADC
ADC.SchDoc

A

B

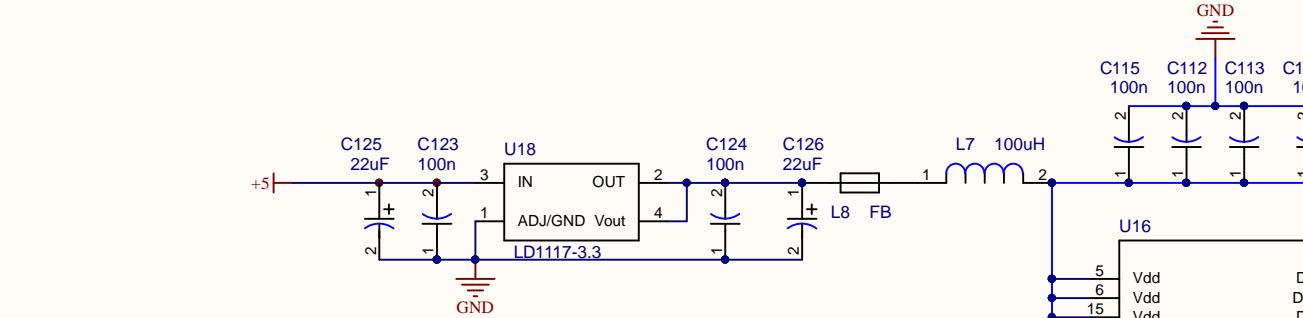
C

D

Title MOTHERBOARD			*
Size: A4	Number:2	Revision:2.0	*
Date: 10.10.2020	Time: 21:32:19	Sheet2 of 18	*
File: D:\Dropbox\Develop\Projects\UA3REO\Scheme\ALTIUM_DESIGNER\MOTHERBOARD\MOTHERBOARD.SCHDOC			*

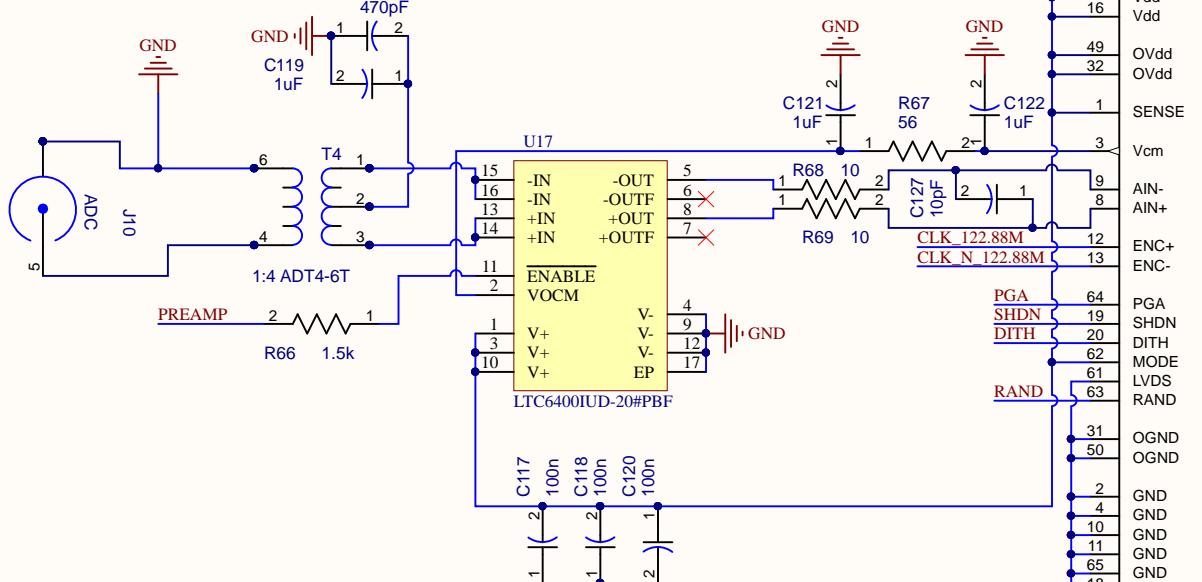
A

A



B

B



Vdd	D0-/DB0
Vdd	D0+/DB1
Vdd	D1-/DB2
Vdd	D1+/DB3
Vdd	D2-/DB4
Vdd	D2+/DB5
Vdd	D3-/DB6
Vdd	D3+/DB7
Vdd	D4-/DB8
Vdd	D4+/DB9
Vdd	D5-/DB10
Vdd	D5+/DB11
Vdd	D6-/DB12
Vdd	D6+/DB13
Vdd	D7-/DB14
Vdd	D7+/DB15
OVdd	CLKOUTA
OVdd	DA0
SENSE	DA1
Vcm	DA2
AIN-AIN+	DA3
ENC+ENC-	DA4
D8-/CLKOUTA	DA5
D8+/DA0	DA6
D9-/DA1	DA7
D9+/DA2	DA8
D10-/DA3	DA9
D10+/DA4	DA10
D11-/DA5	DA11
D11+/DA6	DA12
D12-/DA7	DA13
D12+/DA8	DA14
D13-/DA9	DA15
D13+/DA10	DA16
D14-/DA11	DA17
D14+/DA12	DA18
D15-/DA13	DA19
D15+/DA14	DA20
OF-/DA15	DA21
OF+/OFA	DA22
CLKOUT-/OFB	DA23
CLKOUT+/CLKOUTB	DA24

LTC2208CUP

Title **ADC**

Size: A4 Number:3 Revision:2.0

Date: 10.10.2020 Time: 21:32:19 Sheet 3 of 18

File: D:\Dropbox\Develop\Projects\UA3REO\Scheme\ALTIUM_DESIGNER\MOTHERBOARD\ADC.SchDoc

Altium

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B

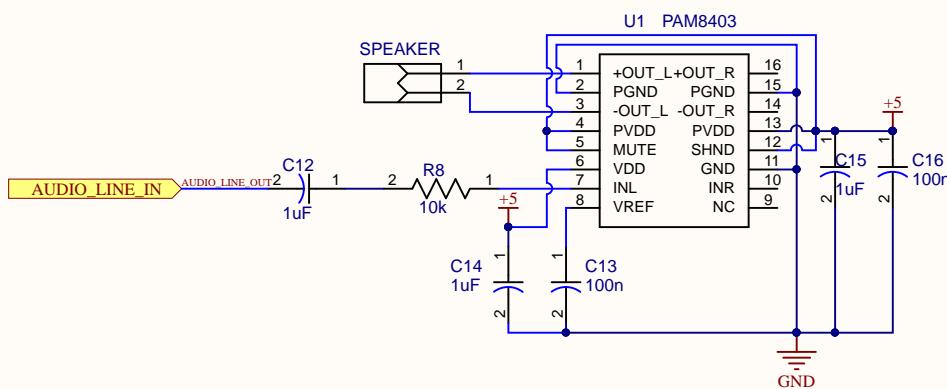
10

C

1

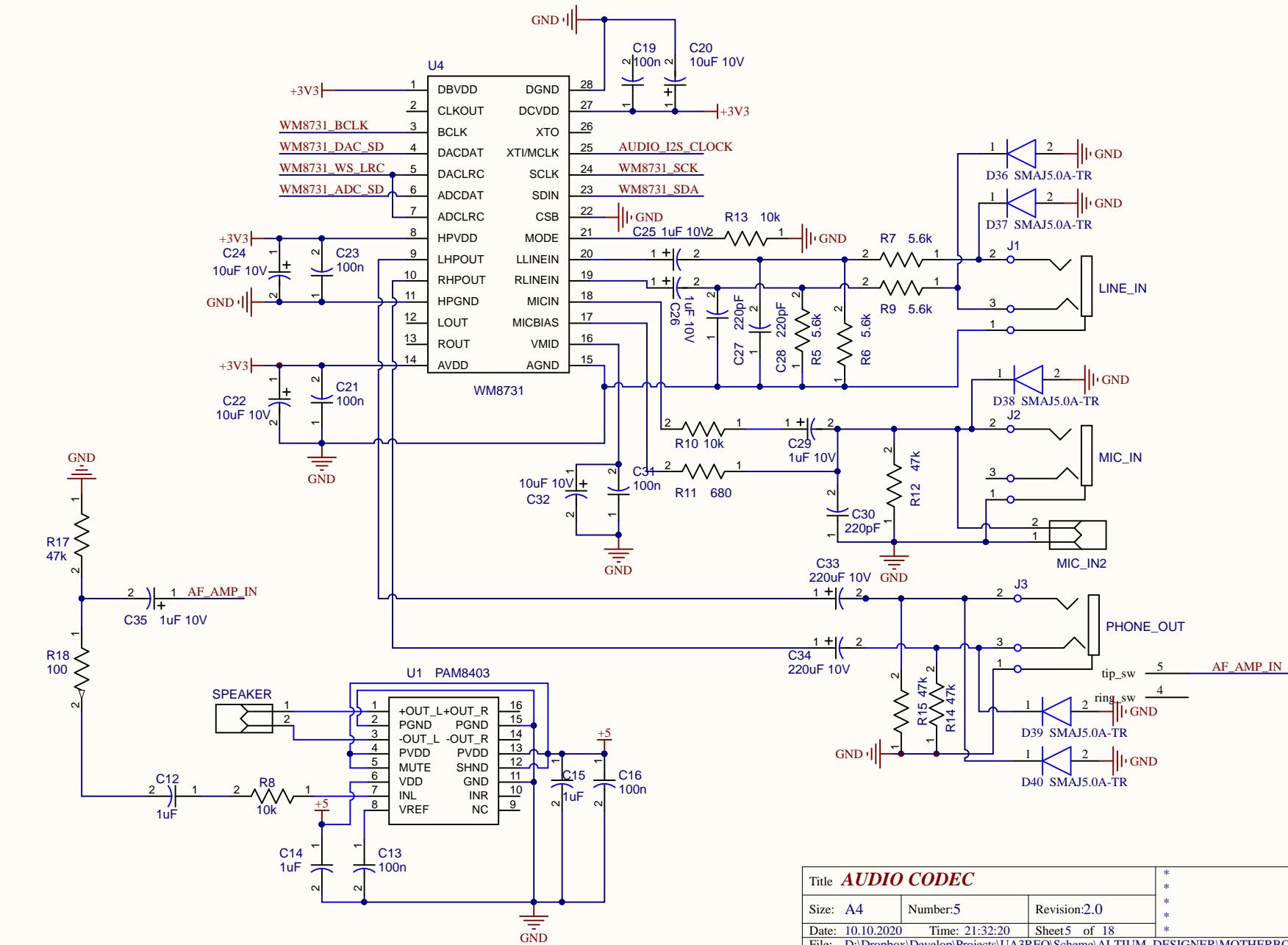
D

1



Title <i>AF AMP</i>	* <i>UA3REO</i> <i>BH8CGJ</i>	
Size: A4	Number:4	Revision:2.0
Date: 10.10.2020	Time: 21:32:19	Sheet 4 of 18
File: D:\Dropbox\Develop\Projects\UA3REO\Scheme\ALTIUM DESIGNER\MOTHERBOARD\AF AMP.SchDoc		

A

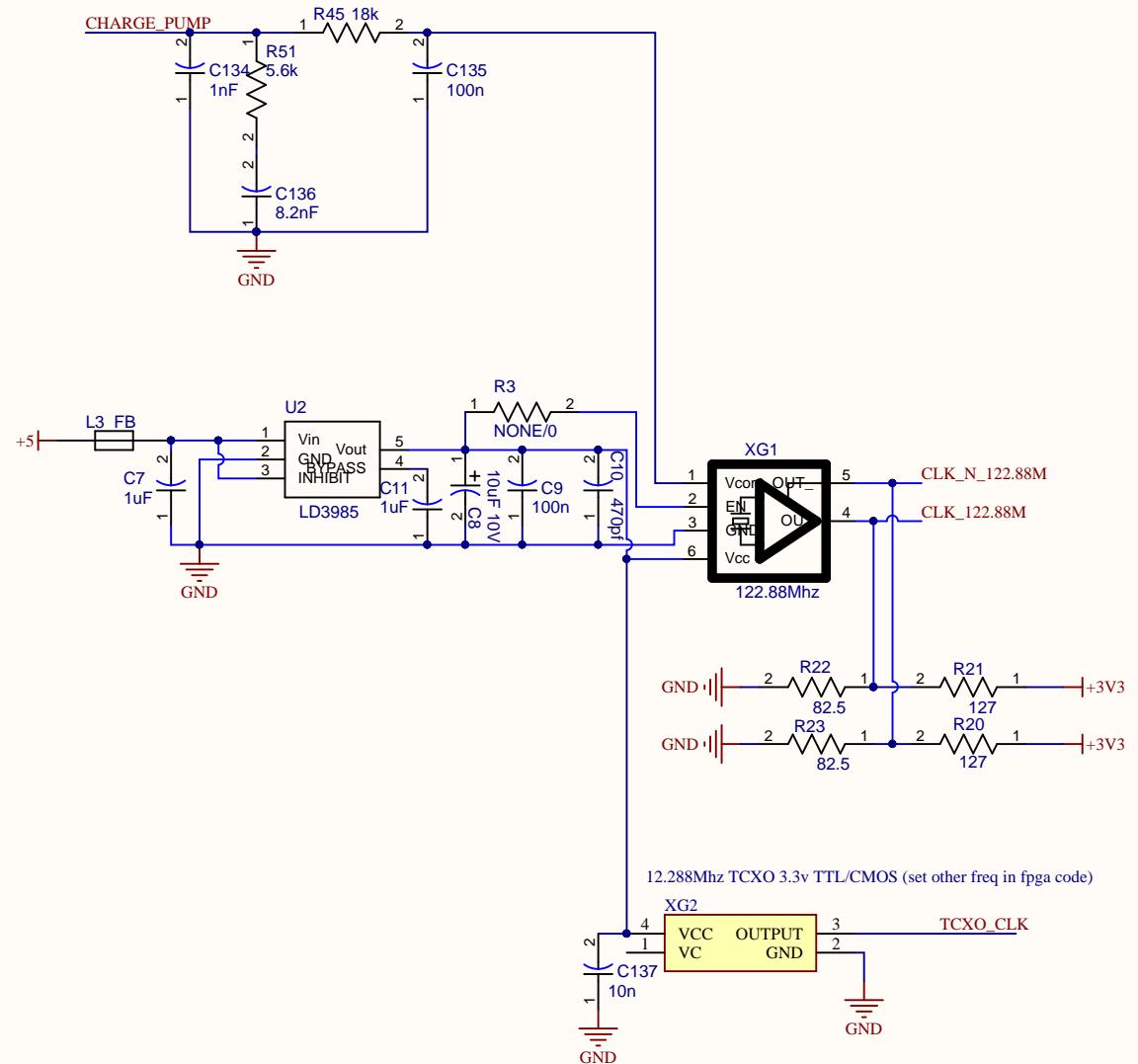
Title **AUDIO CODEC**

Size: A4 Number:5 Revision:2.0

Date: 10.10.2020 Time: 21:32:20 Sheet 5 of 18

File: D:\Dropbox\Develop\Projects\UA3REO\Scheme\ALTIUM_DESIGNER\MOTHERBOARD\AUDIO CODEC.SchDoc

Altium



Title	CLOCK GENERATOR
Size:	A4
Number:	6
Date:	10.10.2020
Time:	21:32:20
File:	D:\Dropbox\Devolon\Projects\U3A3RE

Altium

A

B

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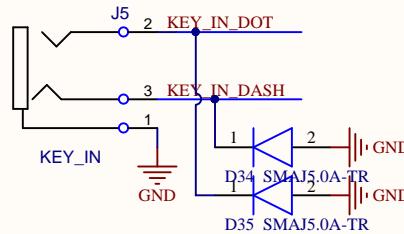
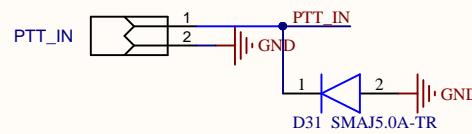
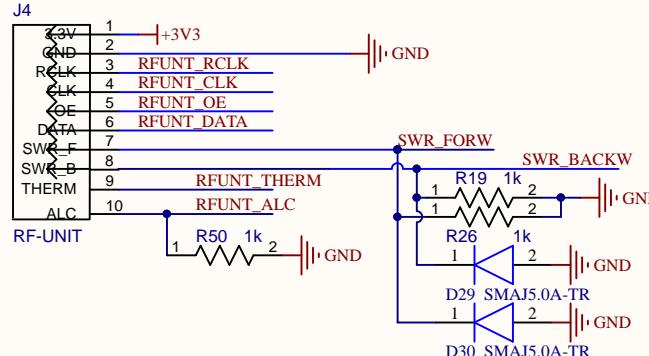
D

A

B

C

D



J6

FMC_NE1	1	CS 3v3
FMC_A18	2	RS 3v3
FMC_NWE	3	WR GND
FMC_NOE	4	RD GND
STM_NRST	5	RSTMISO
FMC_D0	6	DB0MOSI
FMC_D1	7	DB1WRX
FMC_D2	8	DB2WTX
FMC_D3	9	DB3CLK
FMC_D4	10	DB4DCS
FMC_D5	11	DB5AD1C
FMC_D6	12	DB6AD2C
FMC_D7	13	DB7E2A
FMC_D8	14	DB8E2B
FMC_D9	15	DB9E2S
FMC_D10	16	DB10E1A
FMC_D11	17	DB11E1B
FMC_D12	18	DBAD3C
FMC_D13	19	DB135v
FMC_D14	20	DB14GND
FMC_D15	21	DB15GND
PWR_ON	22	PONCAS
PWR_HOLD	23	PHOCAS
	24	3v3
	25	+3V3
	26	GND
	27	PERI_MISO
	28	PERI_MOSI
	29	ESP_1_TX
	30	ESP_1_RX
	31	PERI_SCK
	32	SD_CS
	33	AD1_CS
	34	AD2_CS
	35	ENC2_DT
	36	ENC2_CLK
	37	ENC2_SW
	38	ENC_DT
	39	ENC_CLK
	40	AD3_CS
	41	AD4_CS
	42	AD5_CS
	43	+5
	44	GND
	45	GND
	46	GND
	47	3v3

FPC-45P-0.5mm

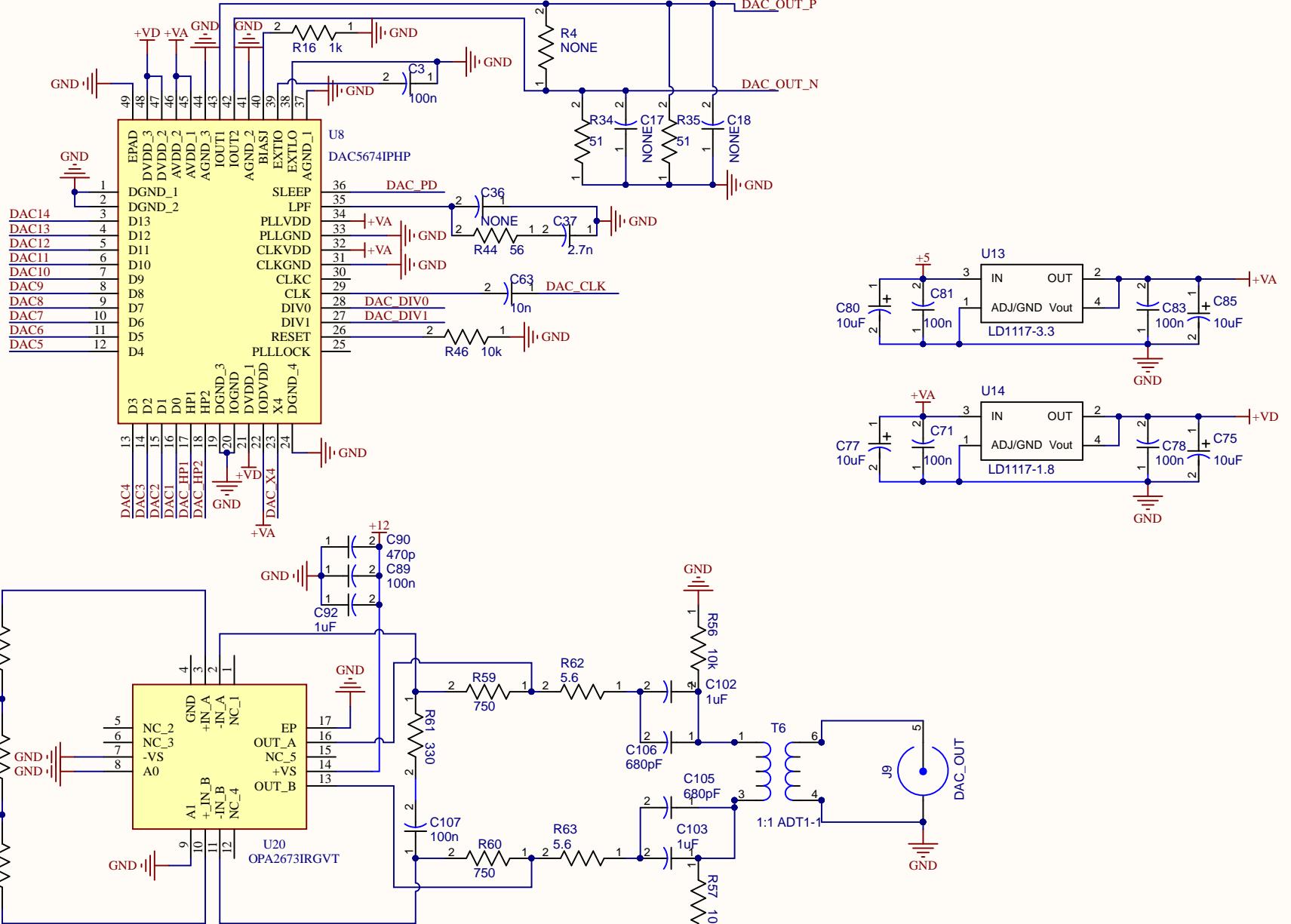
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Size: A4 Number: 7 Revision: 2.0

Date: 10.10.2020 Time: 21:32:20 Sheet 7 of 18

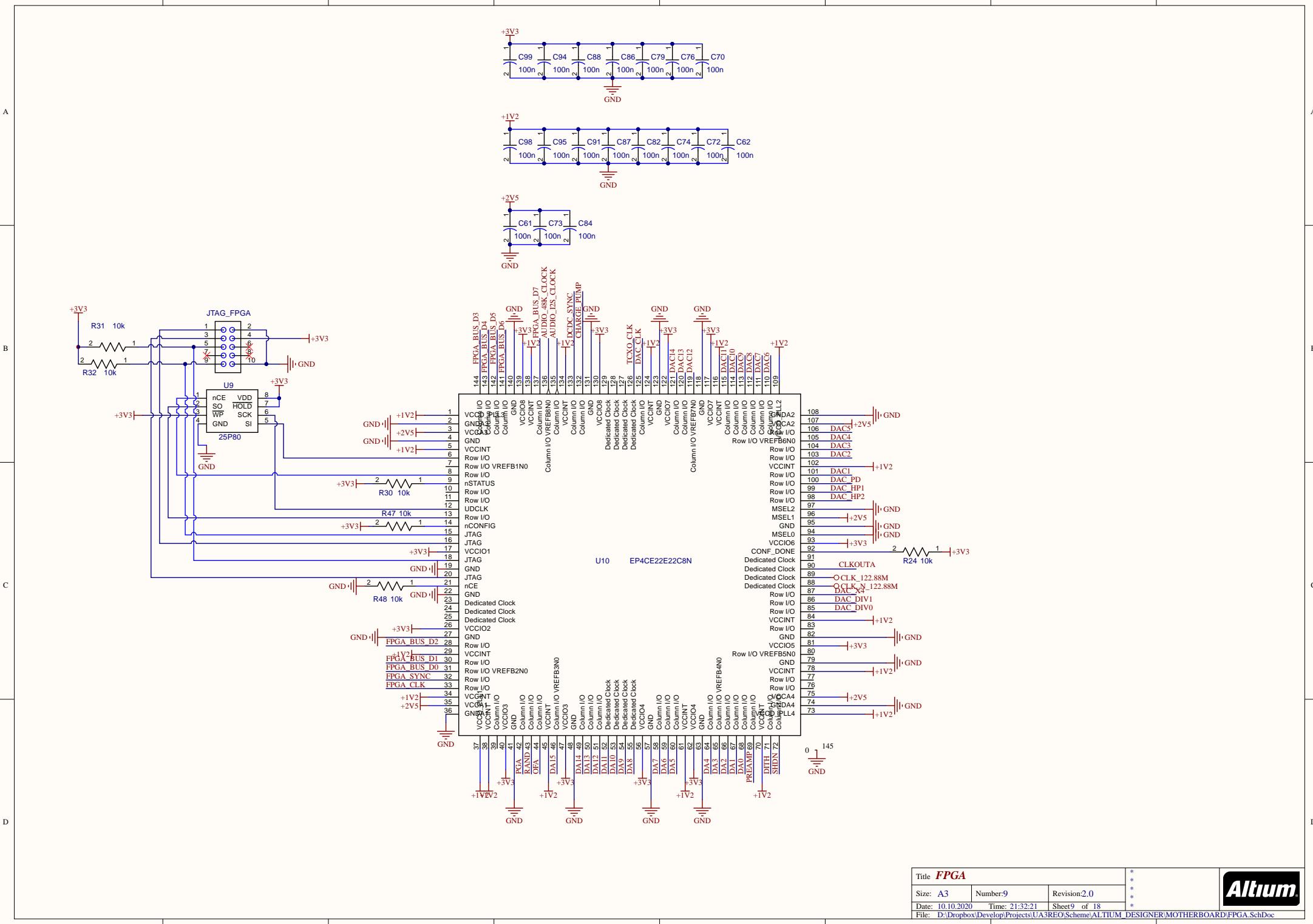
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Altium



Title DAC		
Size: A4	Number: 8	Revision: 2.0
Date: 10.10.2020	Time: 21:32:20	Sheet 8 of 18
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Title **FPGA**

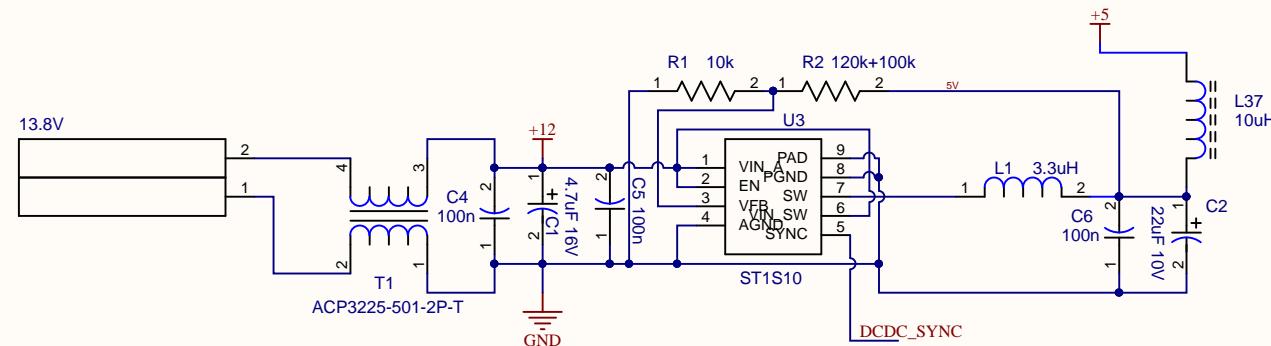
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Date: 10.10.2020 Time: 21:32:21 Sheet9 of 18

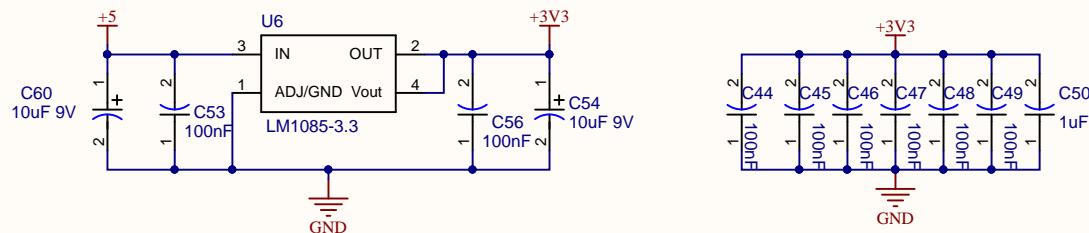
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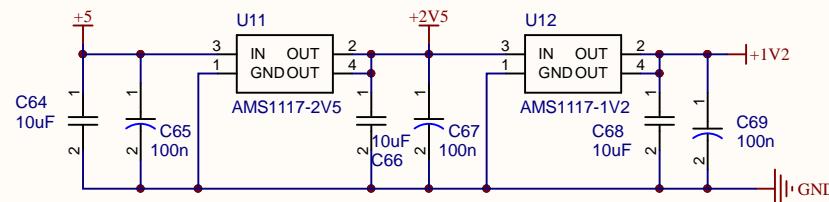
A



B



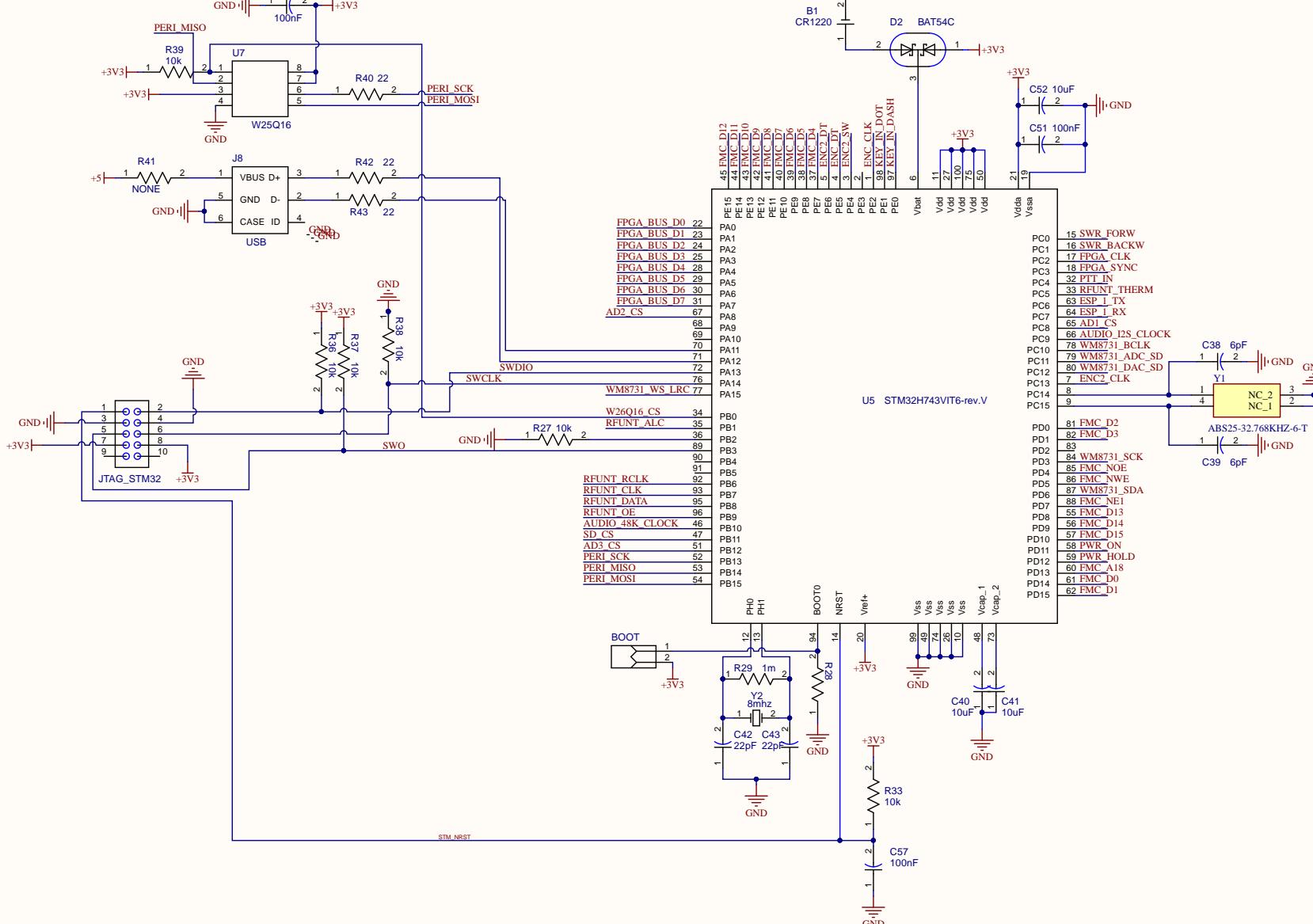
C



D

Title POWER		
Size: A4	Number:10	Revision:2.0
Date: 10.10.2020	Time: 21:32:21	Sheet 10 of 18
File: D:\Dropbox\Develop\Projects\UA3REO\Scheme\ALTIUM_DESIGNER\MOTHERBOARD\POWER.SchDoc	*	Altium

STM32

Title **STM32**

Size: A3	Number: 11	Revision: 2.0
Date: 10.10.2020	Time: 21:32:21	Sheet 11 of 18
File: D:\Dropbox\Develop\Projects\UA3REO\Scheme\ALTIUM DESIGNER\MOTHERBOARD\STM32.SchDoc		



A

A

B

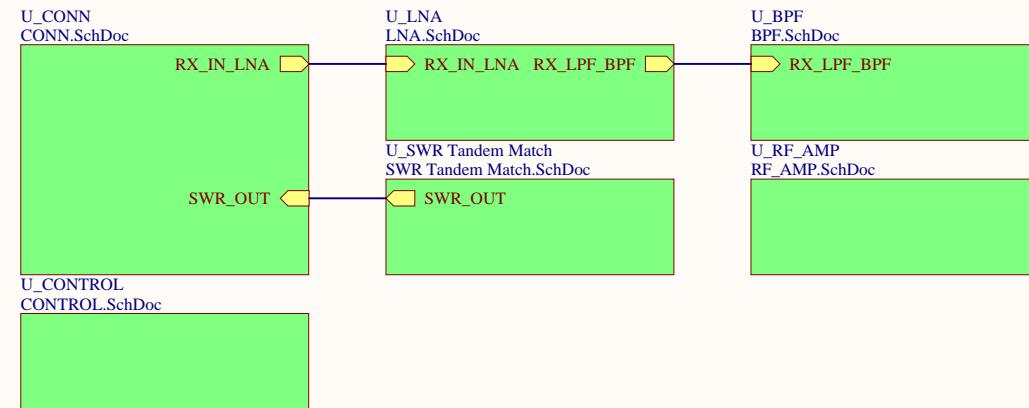
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C

C

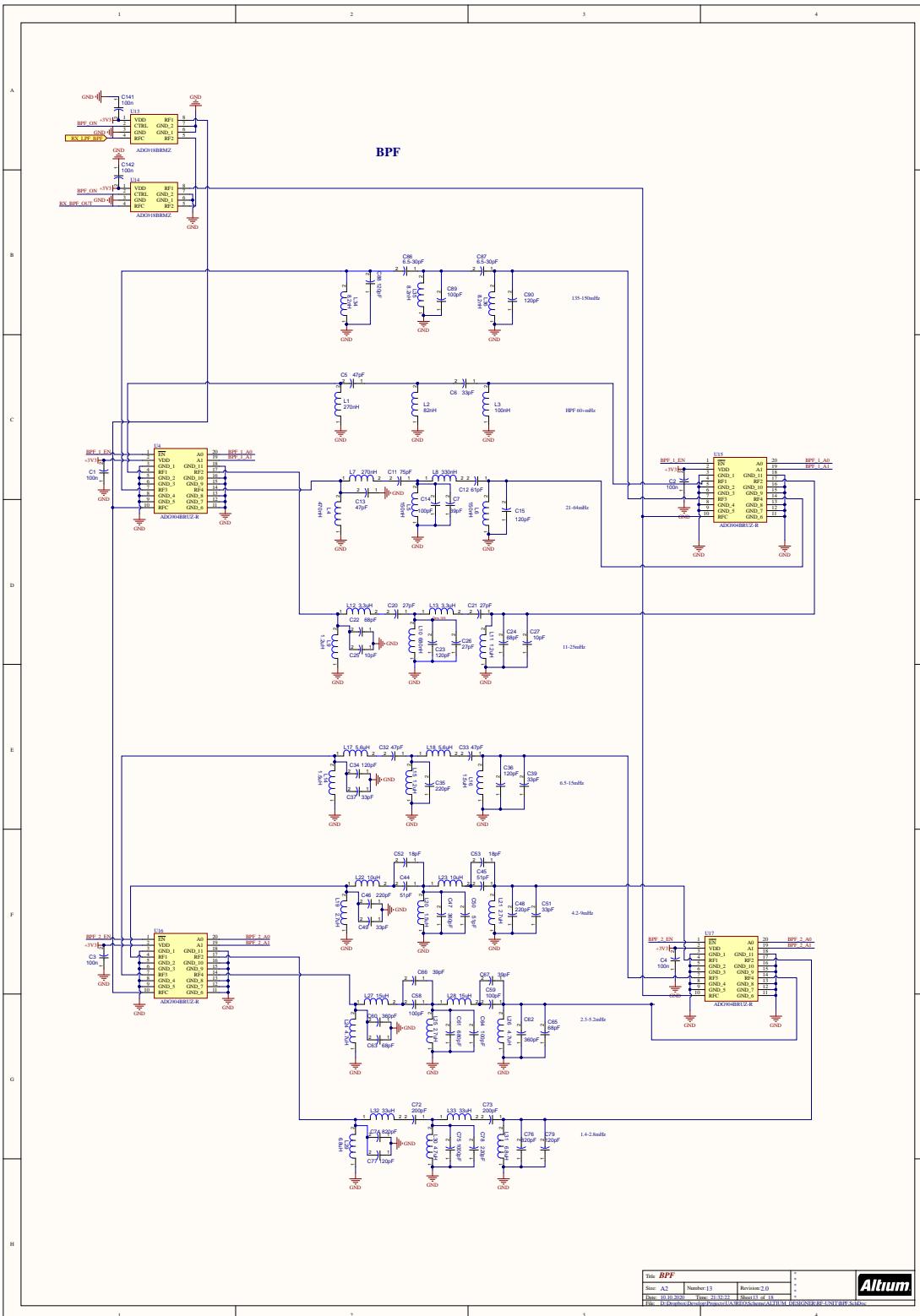
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D



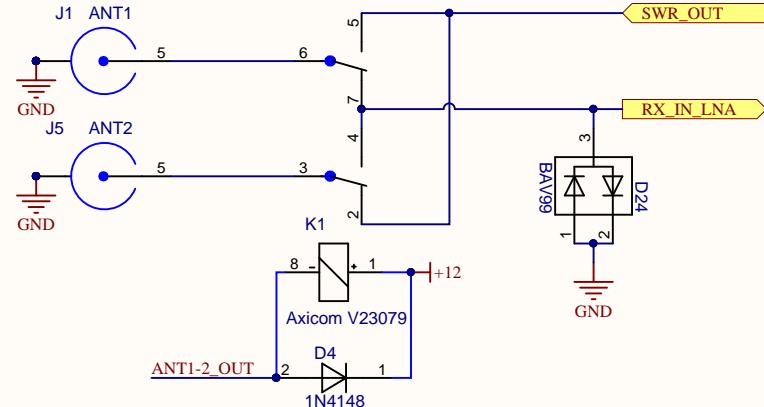
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Size: A4	Number:12	Revision:2.0	*
Date: 10.10.2020	Time: 21:32:21	Sheet 12 of 18	*
File: D:\Dropbox\Develop\Projects\UA3REO\Scheme\ALTIUM_DESIGNER\RF-UNIT\RF-UNIT.SCHDOC			*

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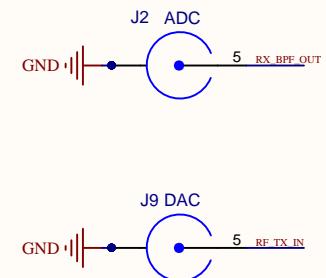


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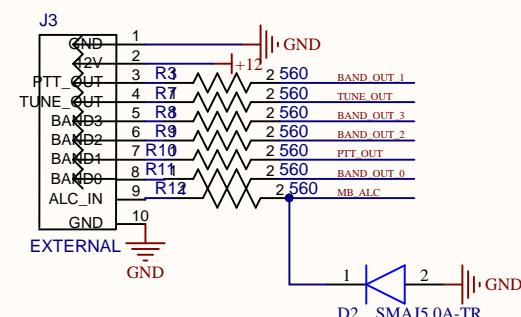
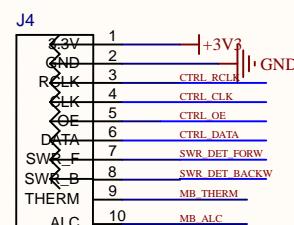
TXRX_COMUTATOR



CONN



B



C

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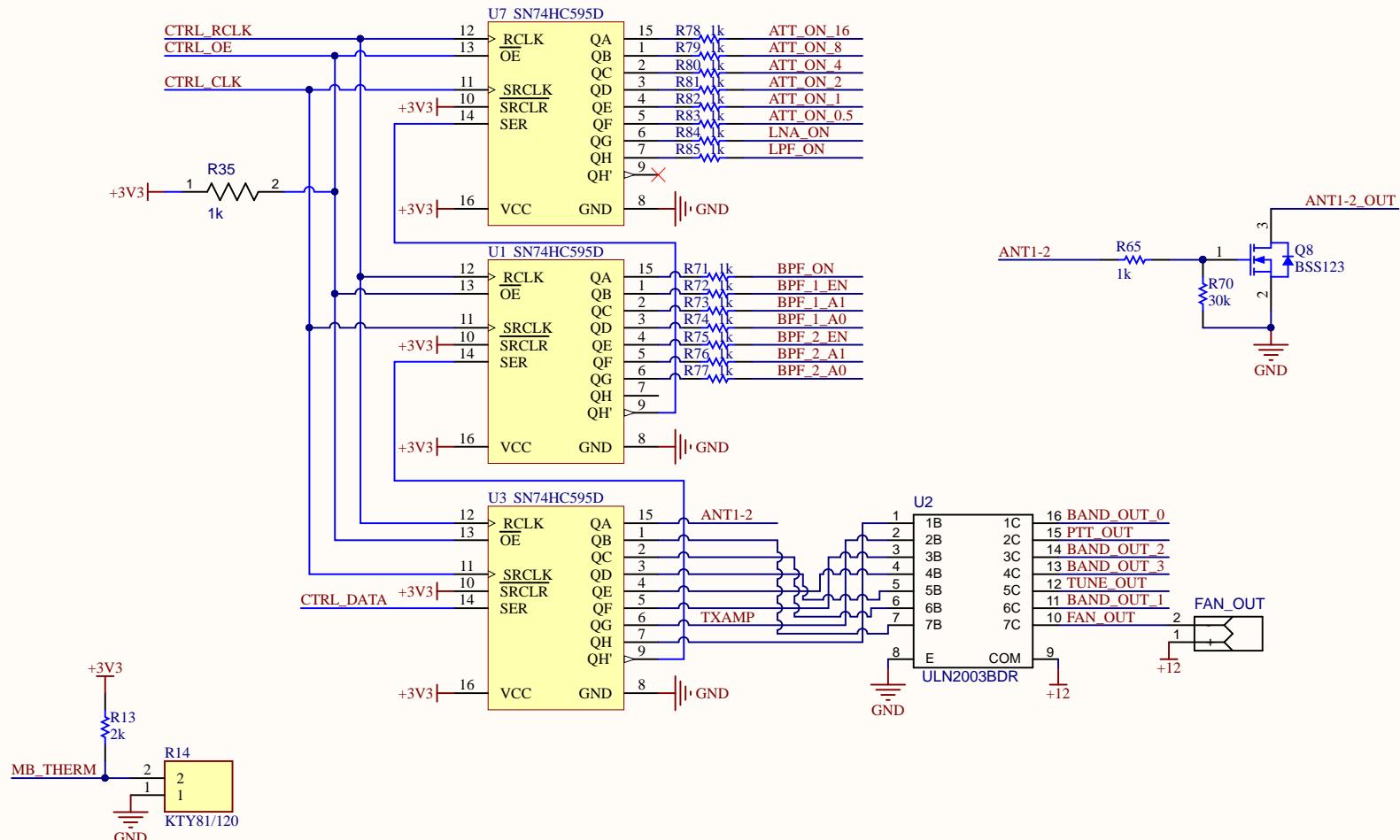
Title **CONN**

Size: A4 Number:14 Revision:2.0

Date: 10.10.2020 Time: 21:32:22 Sheet 14 of 18

File: D:\Dropbox\Develop\Projects\UA3REO\Scheme\ALTIUM_DESIGNER\RF-UNIT\CONN.SchDoc

A

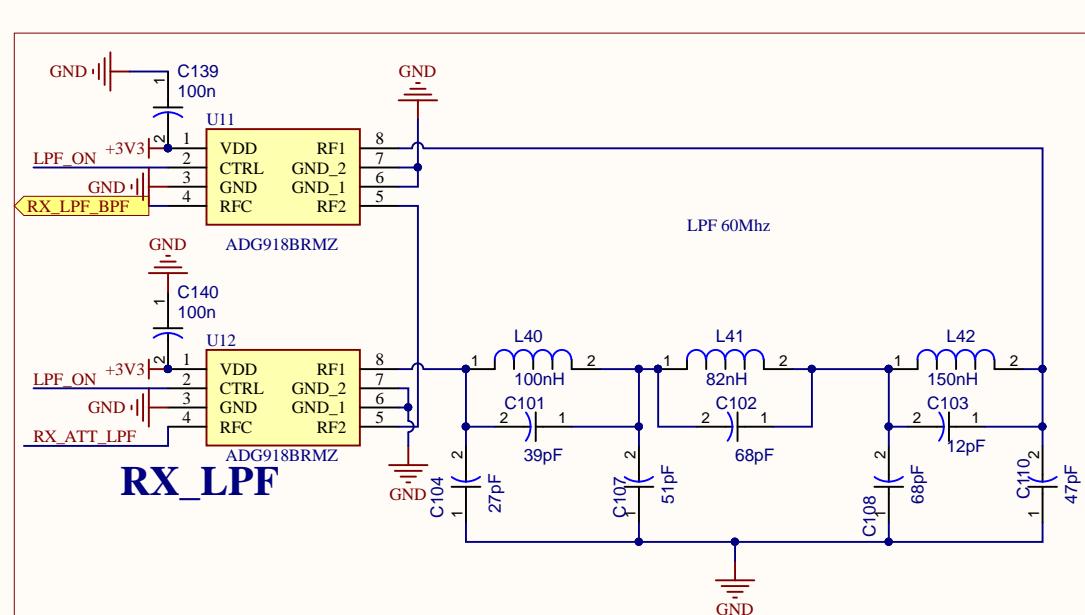
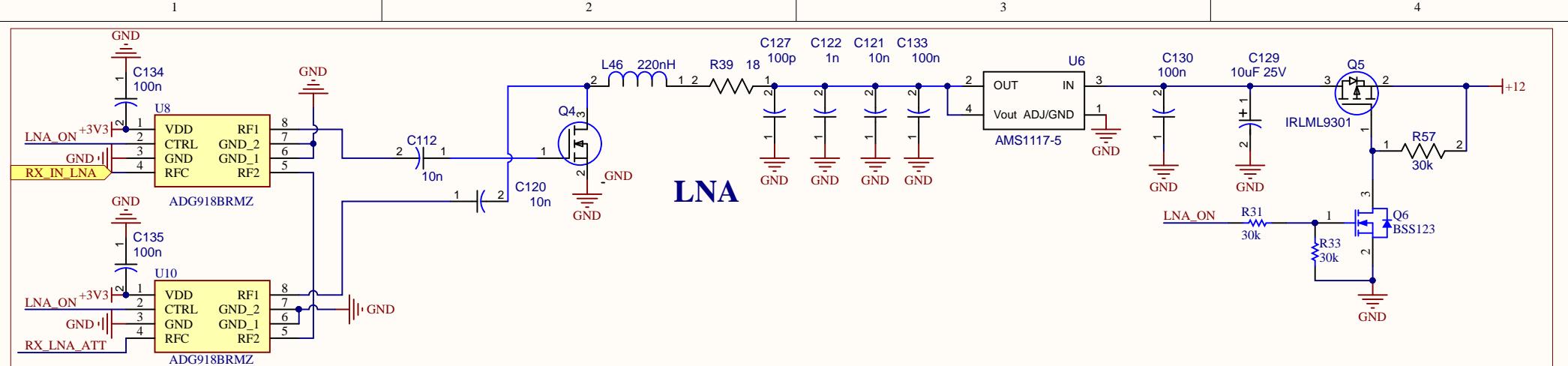
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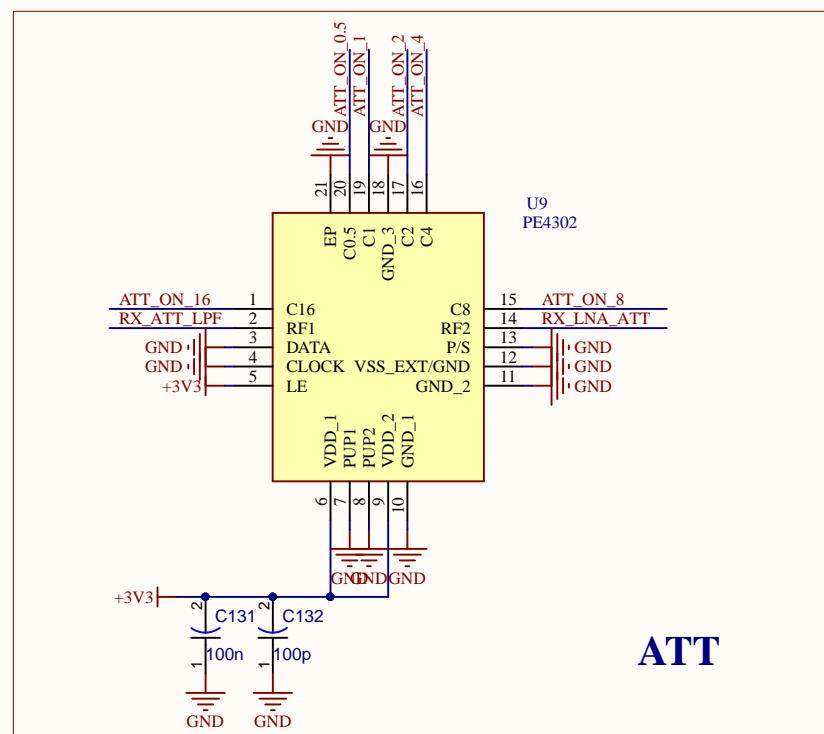
Date: 10.10.2020 Time: 21:32:22 Sheet 15 of 18

File: D:\Dropbox\Develop\Projects\UA3REO\Scheme\ALTIUM_DESIGNER\RF-UNIT\CONTROL.SchDoc

Altium



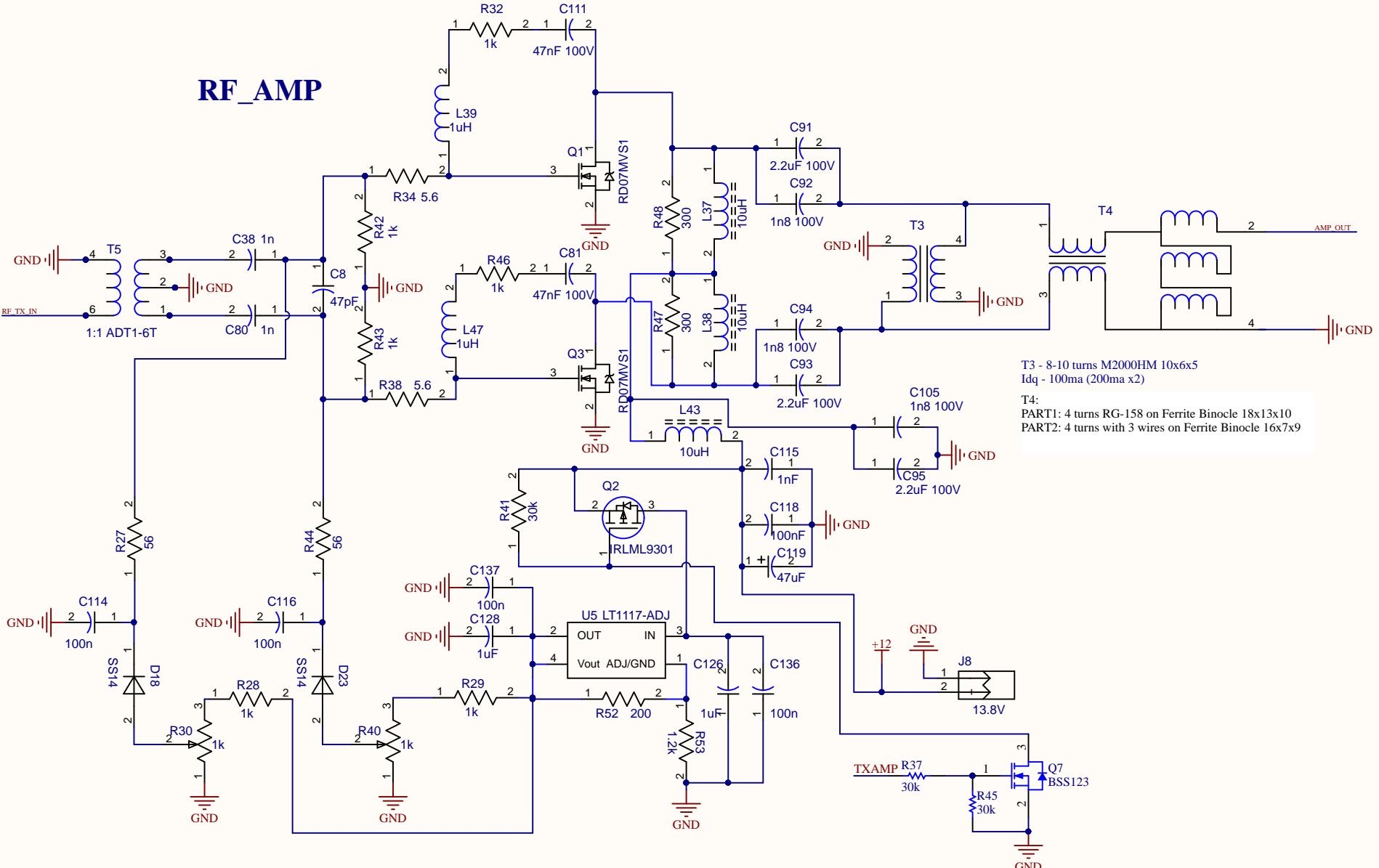
RX_LPF



Title LNA			*	*
Size: A4	Number: 16	Revision: 2.0	*	*
Date: 10.10.2020	Time: 21:32:22	Sheet 16 of 18	*	*
File: D:\Dropbox\Develop\Projects\UA3REO\Scheme\ALTIUM_DESIGNER\RF-UNIT\LNA.SchDoc			*	*

Altium

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RF_AMPTitle **RF_AMP**

Size: A4 Number: 17 Revision: 2.0

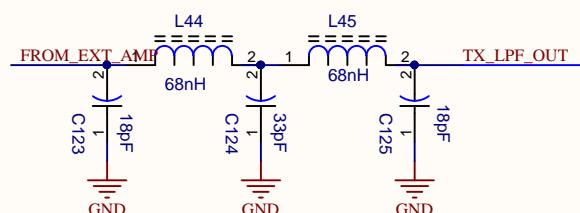
Date: 10.10.2020 Time: 21:32:23 Sheet 17 of 18

File: D:\Dropbox\Develop\Projects\UA3REO\Scheme\ALTIUM_DESIGNER\RF-UNIT\RF_AMP.SchDoc

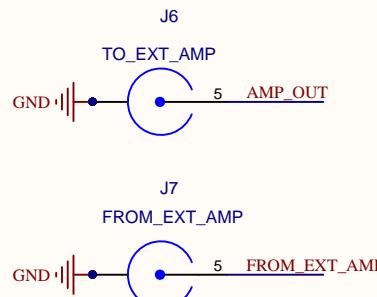
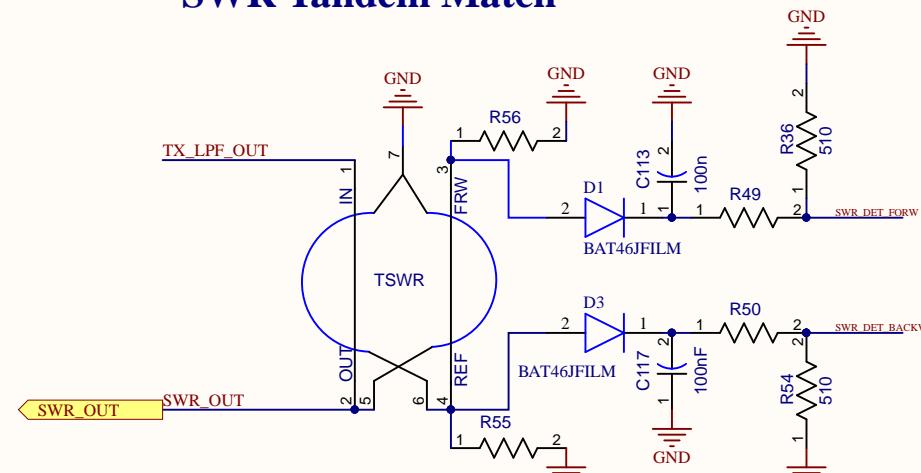
Altium

TX_LPF

LPF 170Mhz



Катушки намотаны проводом 0.5мм на оправке диаметром 5мм, 3.5 витка

**SWR Tandem Match**Title ***SWR Tandem Match***

Size: A4 Number:18 Revision:2.0

Date: 10.10.2020 Time: 21:32:23 Sheet 18 of 18

File: D:\Dropbox\Develop\Projects\UA3REO\Scheme\ALTIUM_DESIGNER\RF-UNIT\SWR Tandem Match.SchDoc

Altium