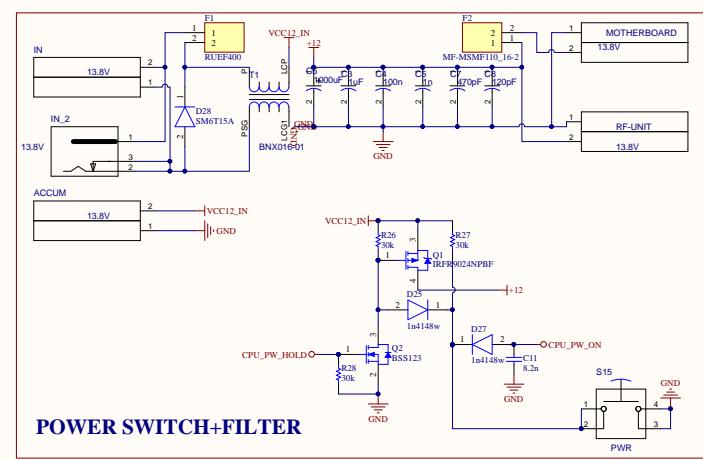
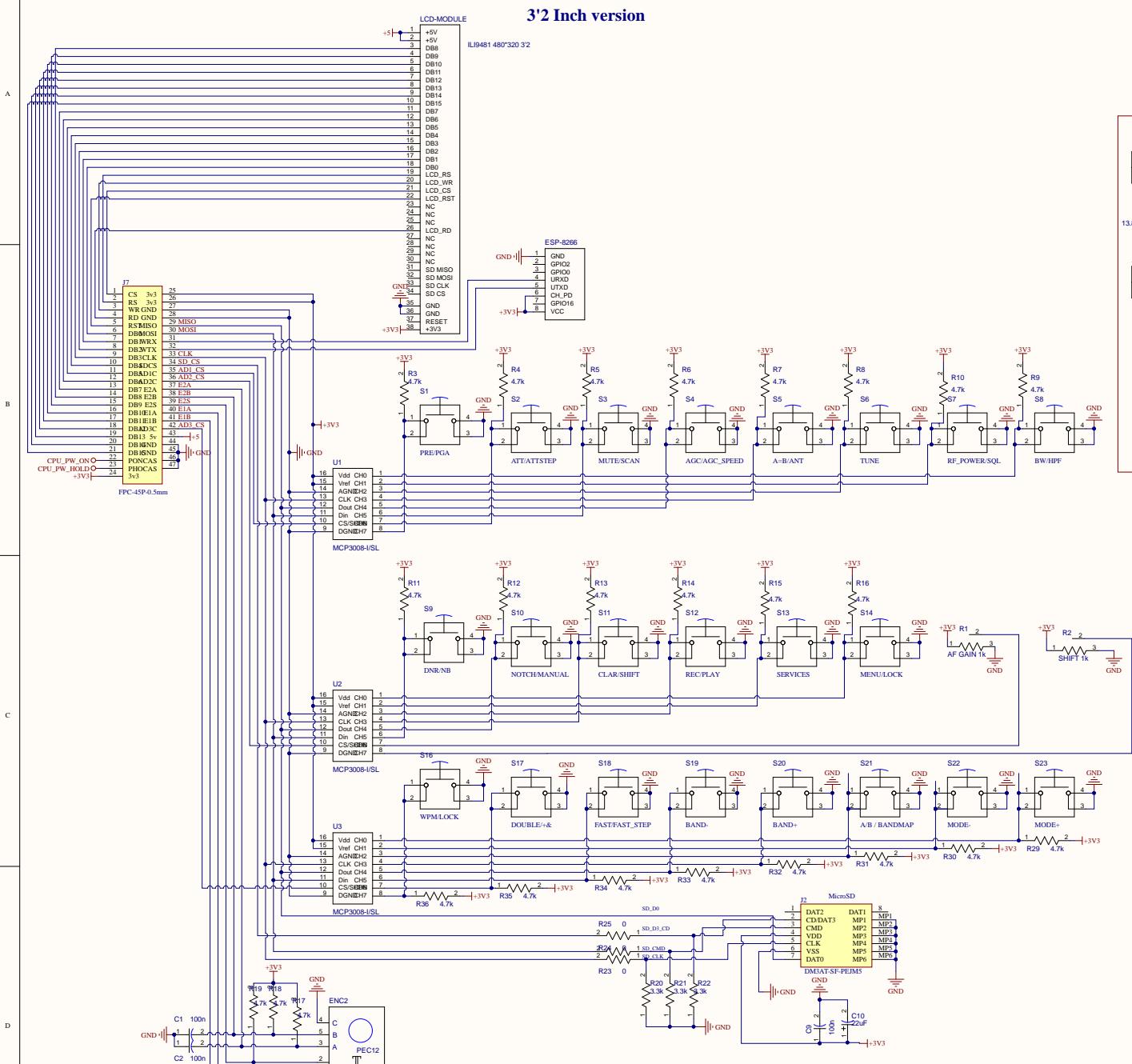


3'2 Inch version



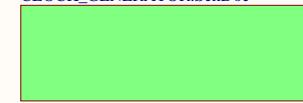
## **POWER SWITCH+FILTER**

A

U\_POWER  
POWER.SchDoc

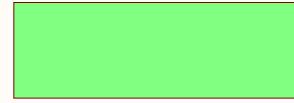


U\_CLOCK\_GENERATOR  
CLOCK\_GENERATOR.SchDoc

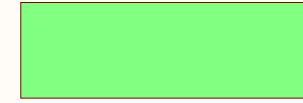


B

U\_CONNECTIONS  
CONNECTIONS.SchDoc



U\_FPGA  
FPGA.SchDoc



U\_STM32  
STM32.SchDoc



U\_AUDIO\_CODEC  
AUDIO\_CODEC.SchDoc



C

U\_DAC  
DAC.SchDoc



U\_ADC  
ADC.SchDoc



A

B

C

D

Title **MOTHERBOARD**

Size: A4	Number:2	Revision:2.0
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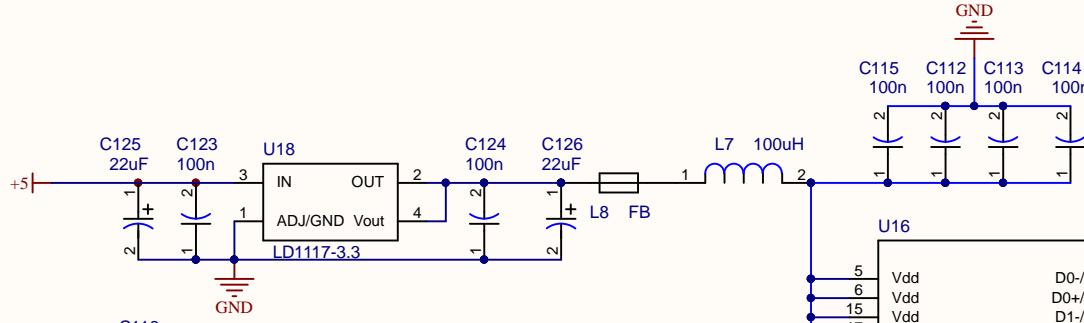
Date: 11.11.2020	Time: 20:09:40	Sheet 2 of 18
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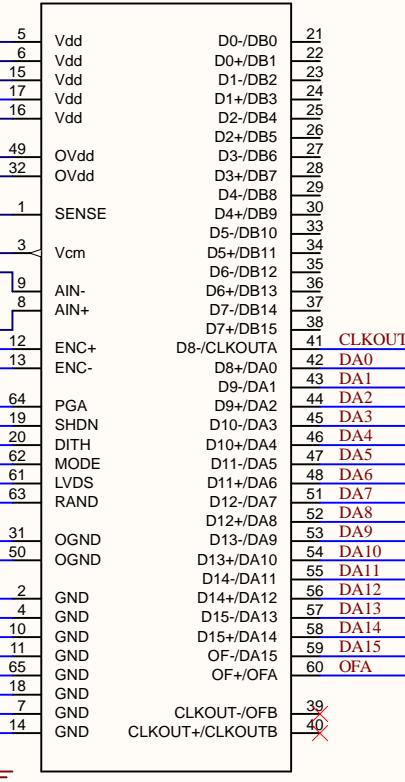
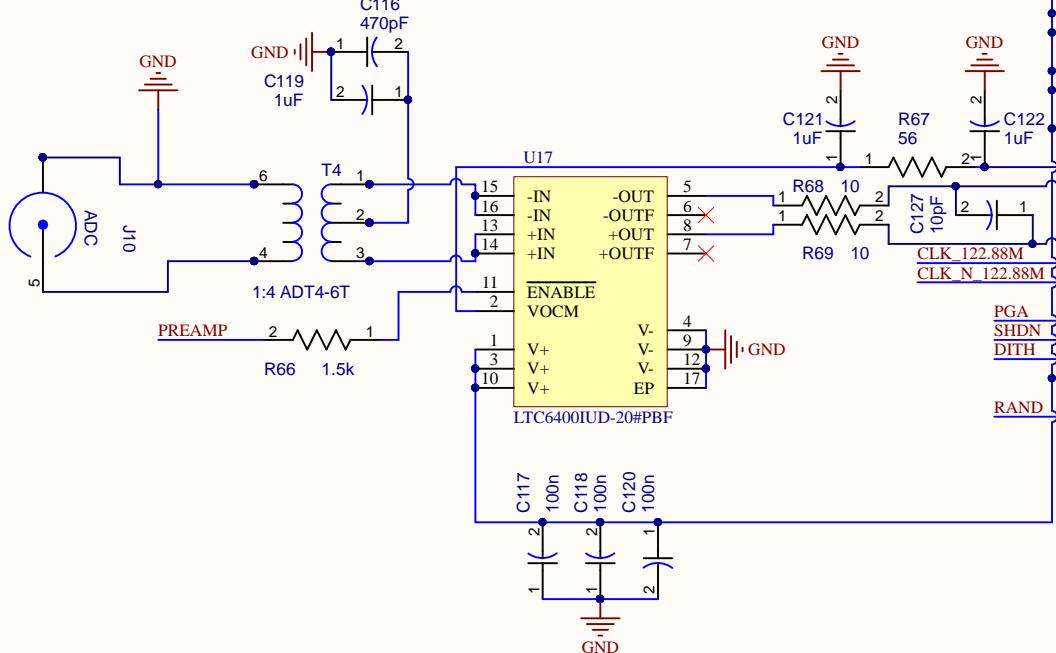
A

A



B

B

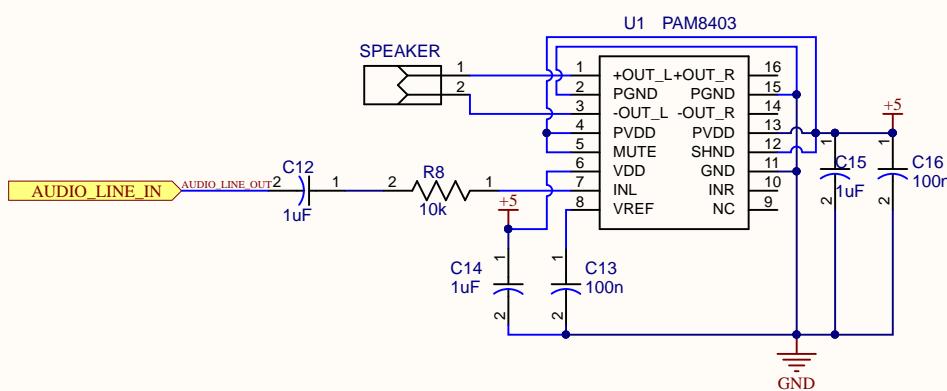
Title **ADC**

Size: A4 Number:3 Revision:2.0

Date: 11.11.2020 Time: 20:09:40 Sheet 3 of 18

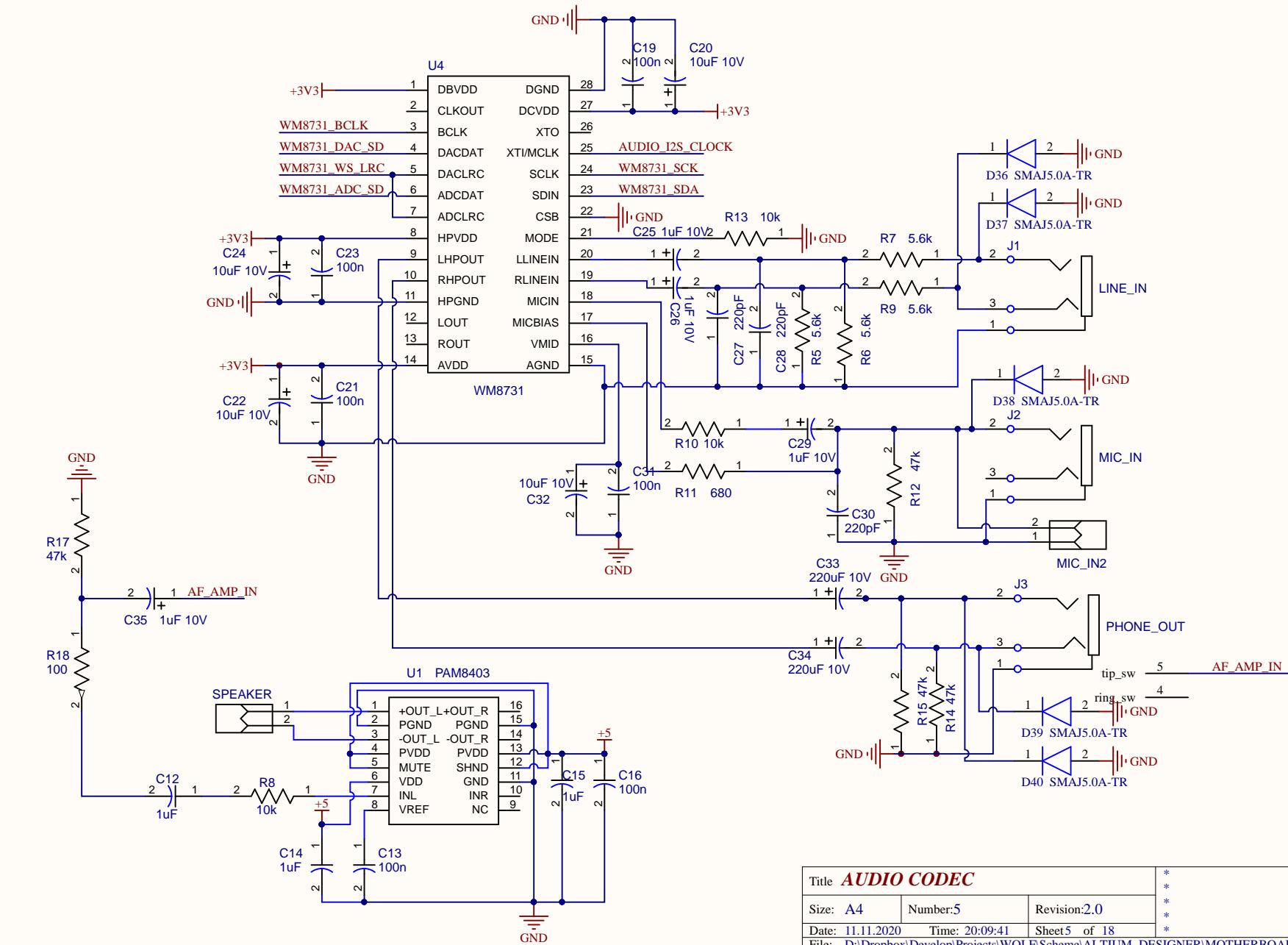
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**Altium**



Title <b>AF AMP</b>			* UA3REO BH8CGJ *
Size: A4	Number:4	Revision:2.0	
Date: 11.11.2020	Time: 20:09:41	Sheet 4 of 18	
File: D:\Dropbox\Develop\Projects\WOLF\Scheme\ALTIUM_DESIGNER\MOTHERBOARD\AF AMP.SchDoc			<b>Altium</b>

A

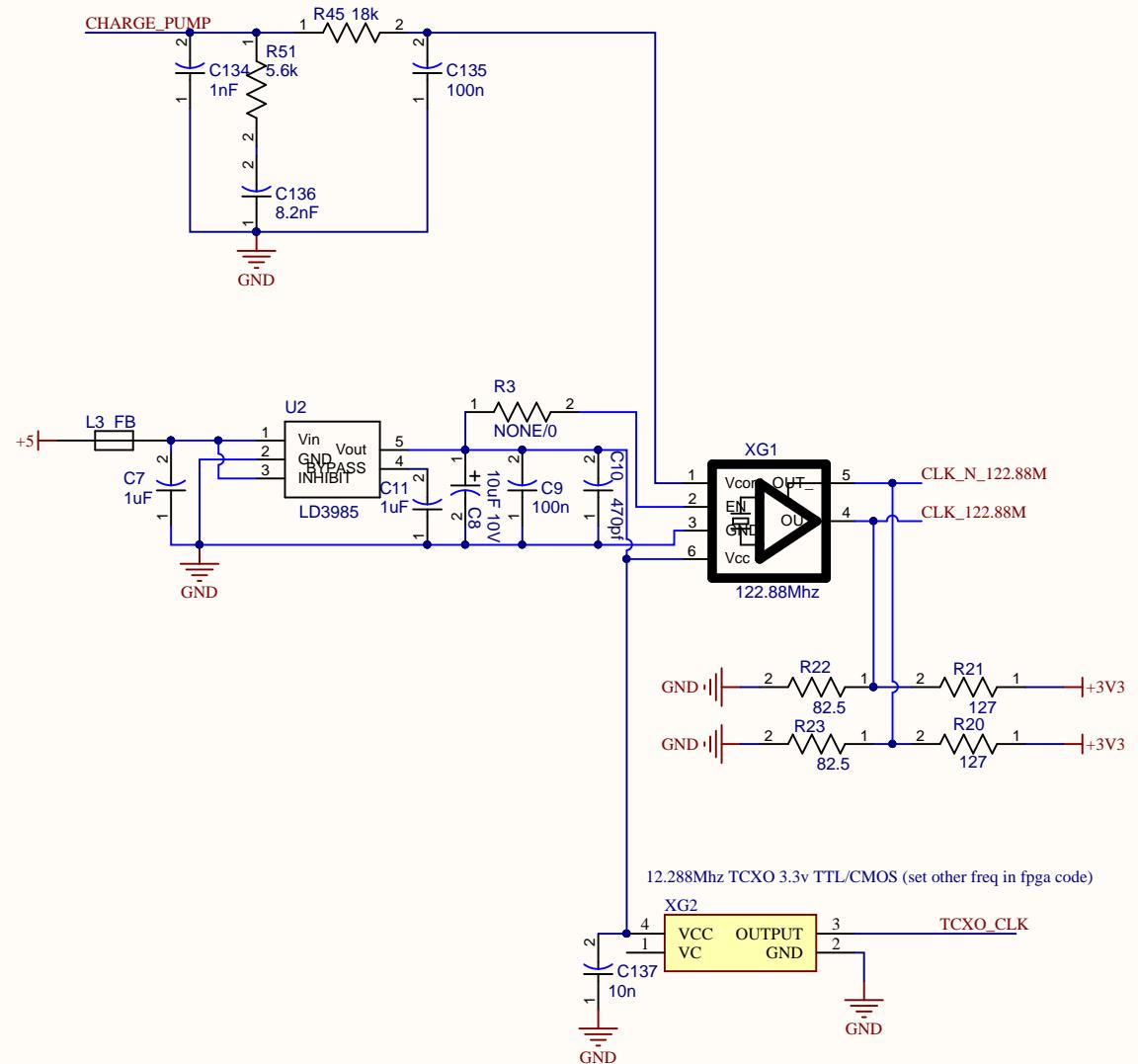
Title **AUDIO CODEC**

Size: A4 Number:5 Revision:2.0

Date: 11.11.2020 Time: 20:09:41 Sheet 5 of 18

File: D:\Dropbox\Develop\Projects\WOLF\Scheme\ALTIUM\_DESIGNER\MOTHERBOARD\AUDIO CODEC.SchDoc

**Altium**



Title	<b>CLOCK GENERATOR</b>	
Size:	A4	Number:6
Date:	11.11.2020	Time: 20:09:41
File:	D:\Dropbox\Developer\Projects\WOLF	

**Altium**

A

B

C

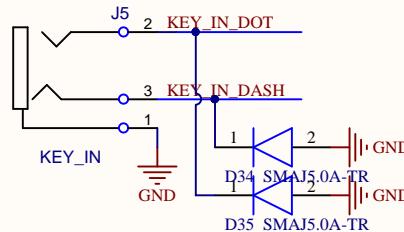
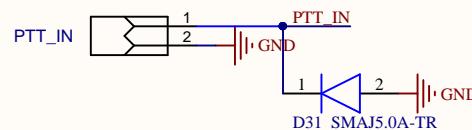
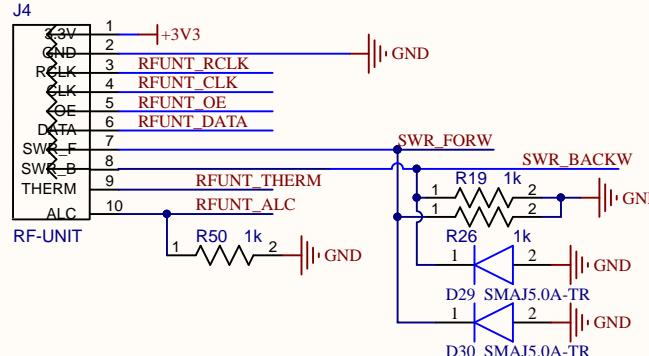
D

A

B

C

D

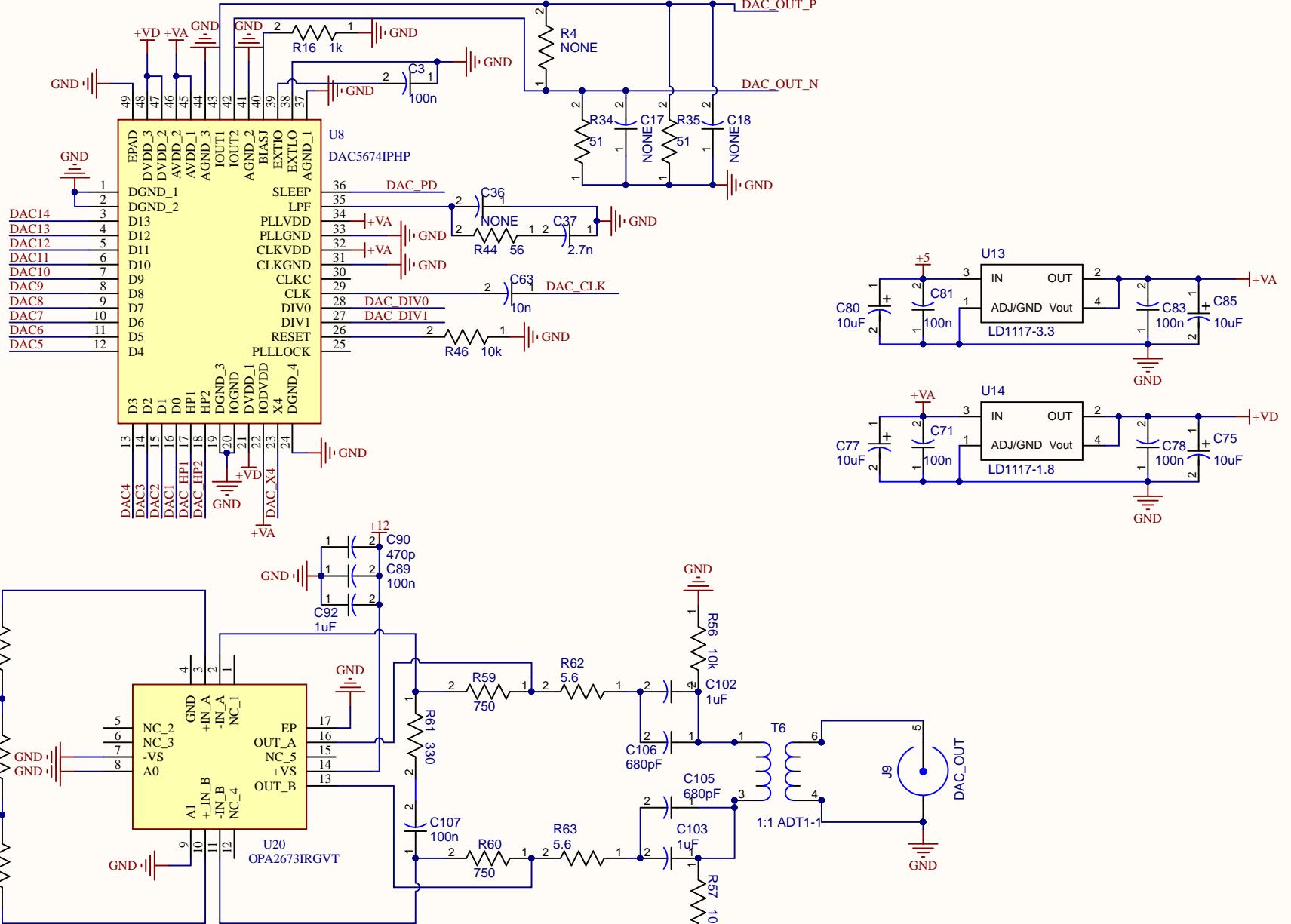


**J6**

1	CS 3v3
2	FMC_A18 3v3
3	FMC_NWE GND
4	FMC_NOE GND
5	STM_NRST GND
6	RSTMISO GND
7	FMC_D1 DB0MOSI
8	FMC_D2 DB1WRX
9	FMC_D3 DB2WTX
10	FMC_D4 DB3CLK
11	FMC_D5 DB4DCS
12	FMC_D6 DB5AD1C
13	FMC_D7 DB6AD2C
14	FMC_D8 DB7E2A
15	FMC_D9 DB8E2B
16	FMC_D10 DB9E2S
17	FMC_D11 DB1E1A
18	FMC_D12 DB1E1B
19	FMC_D13 DBAD3C
20	FMC_D14 DB13 5v
21	FMC_D15 DB1GND
22	PWR_ON DB1GND
23	PWR_HOLD PONCAS
24	+3V3 PHOCAS
25	+3V3 3v3
26	PERI_MOSI GND
27	PERI_RX GND
28	PERI_SCK GND
29	SD_CS GND
30	AD1_CS GND
31	AD2_CS GND
32	ENC2_DT GND
33	ENC2_CLK GND
34	ENC_SW GND
35	ENC_DT GND
36	ENC_CLK GND
37	AD3_CS GND
38	AD4_CS GND
39	AD5_CS GND
40	AD6_CS GND
41	AD7_CS GND
42	AD8_CS GND
43	+5 V
44	GND
45	GND
46	GND
47	GND

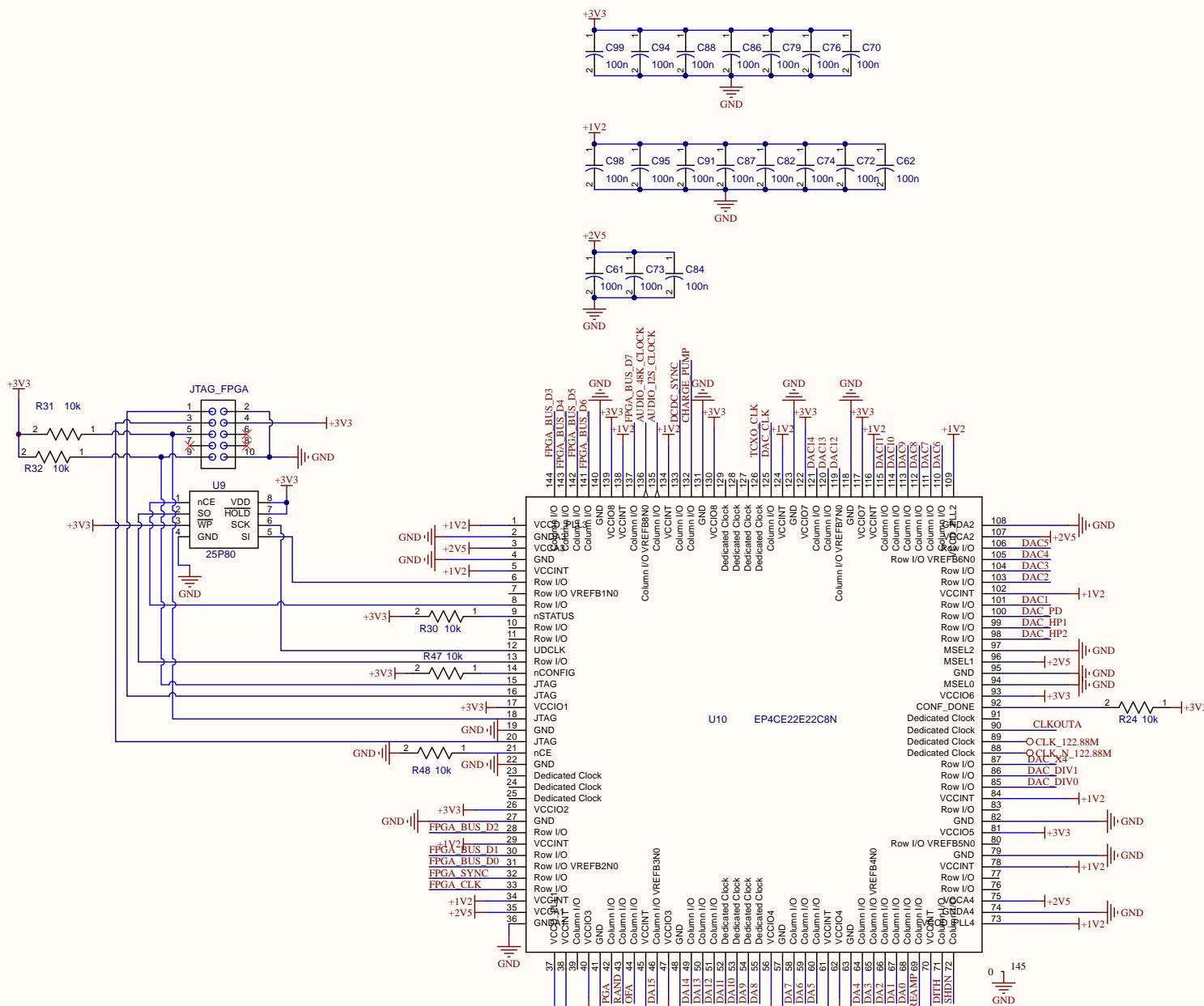
FPC-45P-0.5mm

Title **CONNECTIONS**Size: **A4** Number: **7** Revision: **2.0**Date: **11.11.2020** Time: **20:09:41** Sheet **7** of **18**File: **D:\Dropbox\Develop\Projects\WOLF\Scheme\ALTIUM\_DESIGNER\MOTHERBOARD\CONNECTIONS.SchDoc****Altium**



Title <b>DAC</b>		
Size: A4	Number: 8	Revision: 2.0
Date: 11.11.2020	Time: 20:09:41	Sheet 8 of 18
File: D:\Dropbox\Develop\Projects\WOLF\Scheme\ALTIUM_DESIGNER\MOTHERBOARD\DAC.SchDoc	*	*

**Altium**

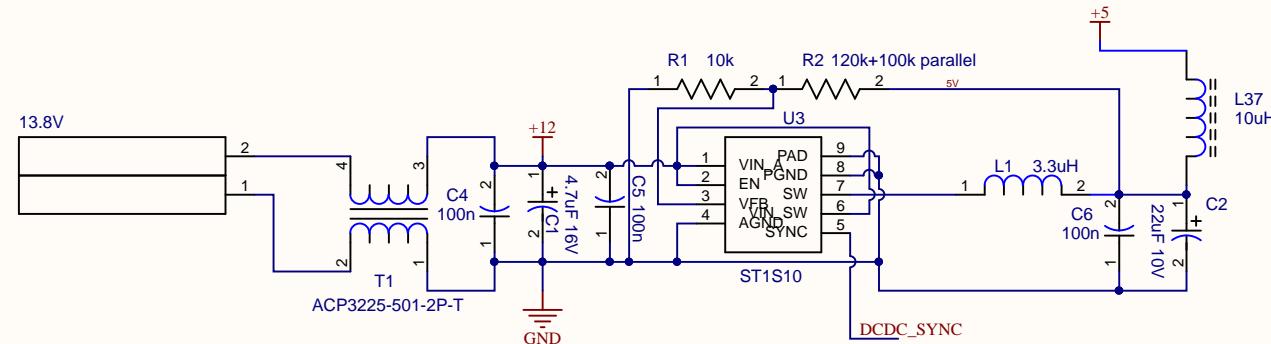


Title **FPGA**

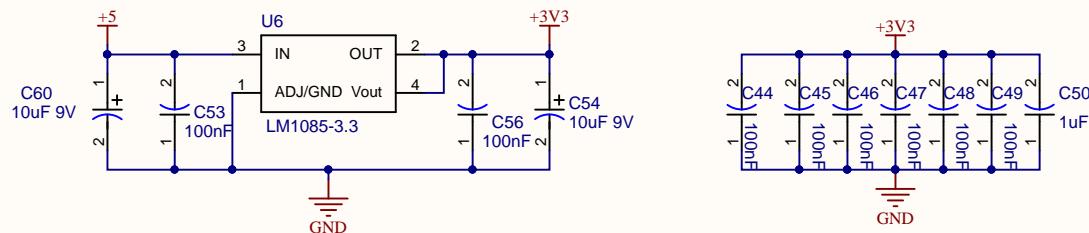
Size: A3 Number:9 Revision:2.0  
Date: 11.11.2020 Time: 20:09:41 Sheet 9 of 18  
File: D:\Dropbox\Develop\Projects\WOLF\Schema\ALTIUM DESIGN

**Altium**

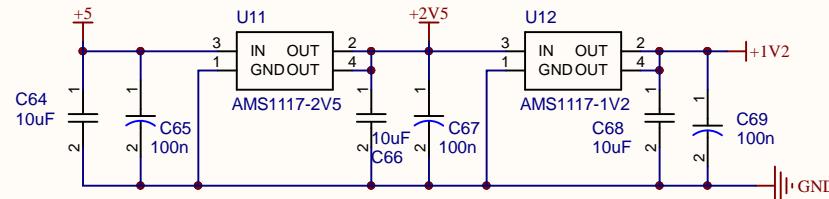
A



B



C

Title **POWER**

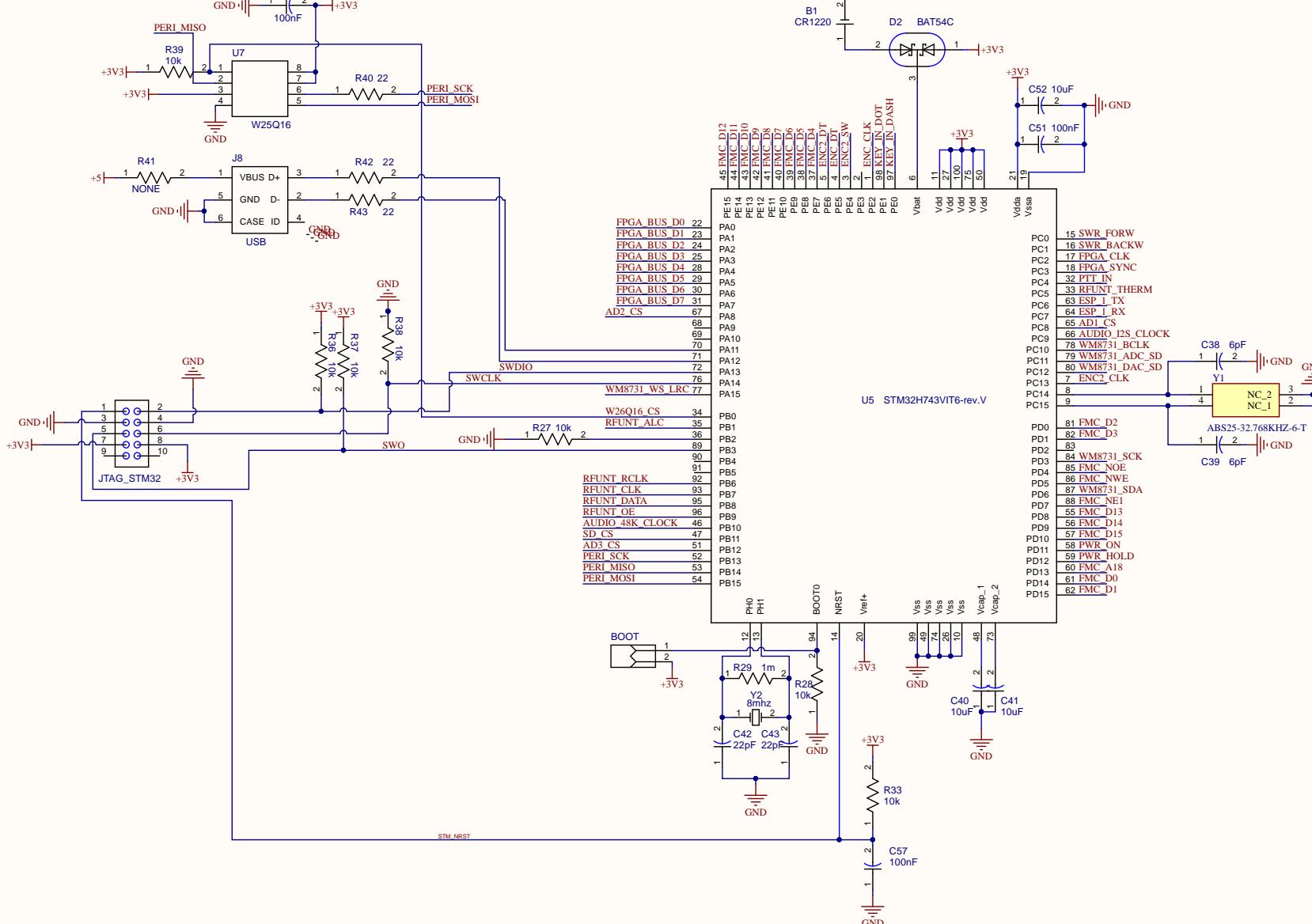
Size: A4 Number:10 Revision:2.0

Date: 11.11.2020 Time: 20:09:42 Sheet 10 of 18

File: D:\Dropbox\Develop\Projects\WOLF\Scheme\ALTIUM\_DESIGNER\MOTHERBOARD\POWER.SchDoc

**Altium**

# STM32

Title **STM32**

Size: A3 Number:11 Revision:2.0

Date: 11.11.2020 Time: 20:09:42 Sheet 11 of 18

File: D:\Dropbox\Develop\Projects\WOLF\Scheme\ALTIUM DESIGNER\MOTHERBOARD\STM32.SchDoc



A

A

B

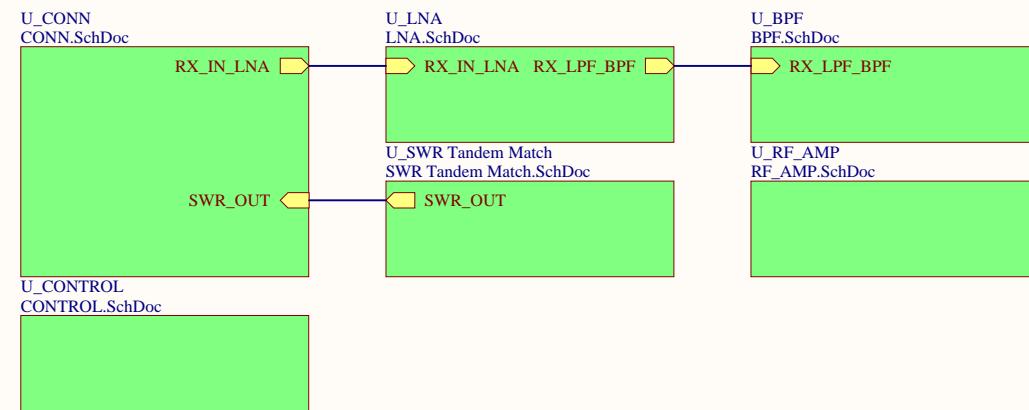
B

C

C

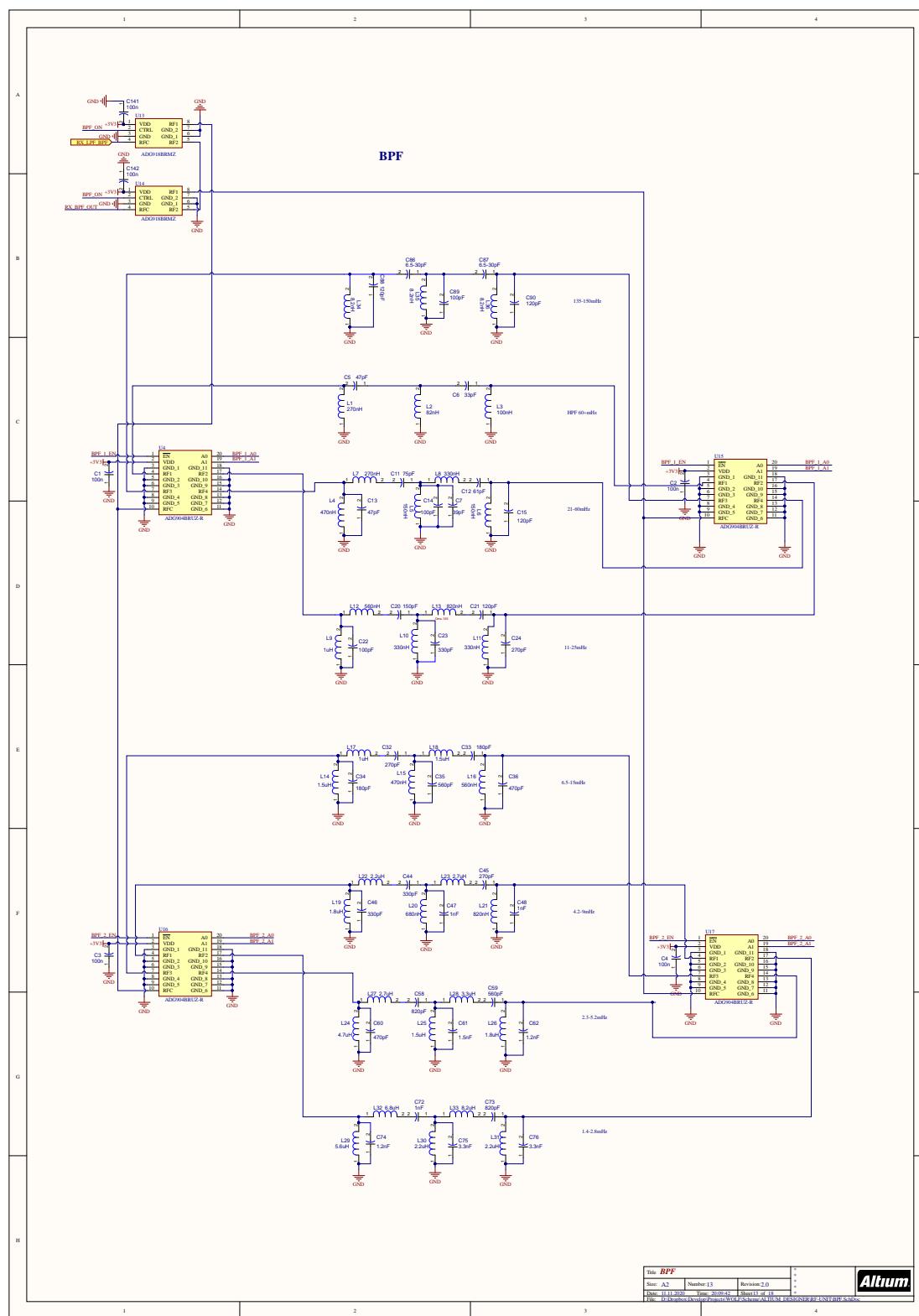
D

D



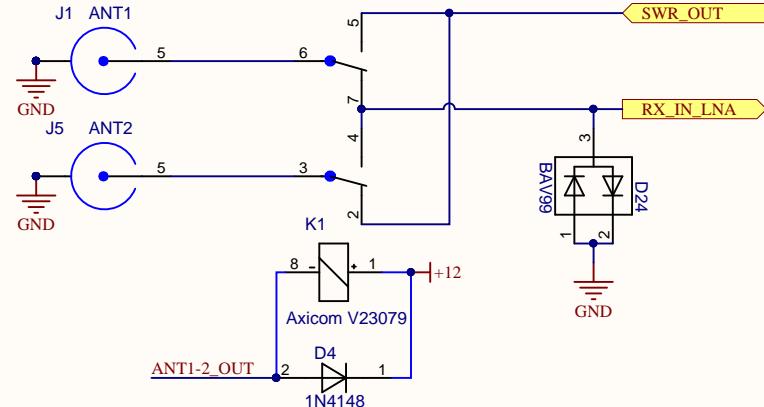
Title <b>RF-UNIT</b>			*
Size: A4	Number:12	Revision:2.0	*
Date: 11.11.2020	Time: 20:09:42	Sheet 12 of 18	*
File: D:\Dropbox\Develop\Projects\WOLF\Scheme\ALTIUM_DESIGNER\RF-UNIT\RF-UNIT.SCHDOC			*

**Altium**



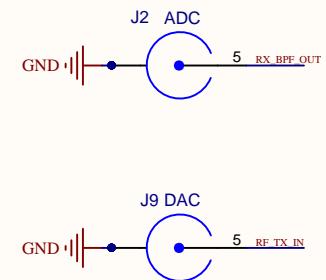
A

## TXRX\_COMUTATOR

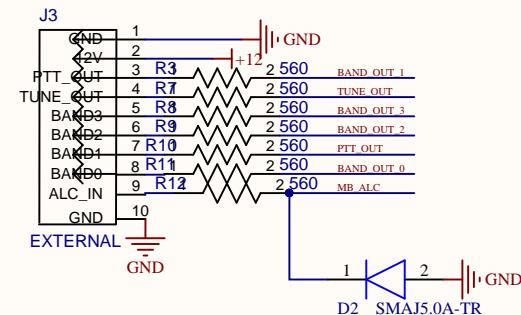
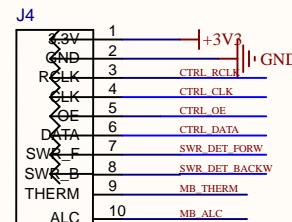


B

## CONN



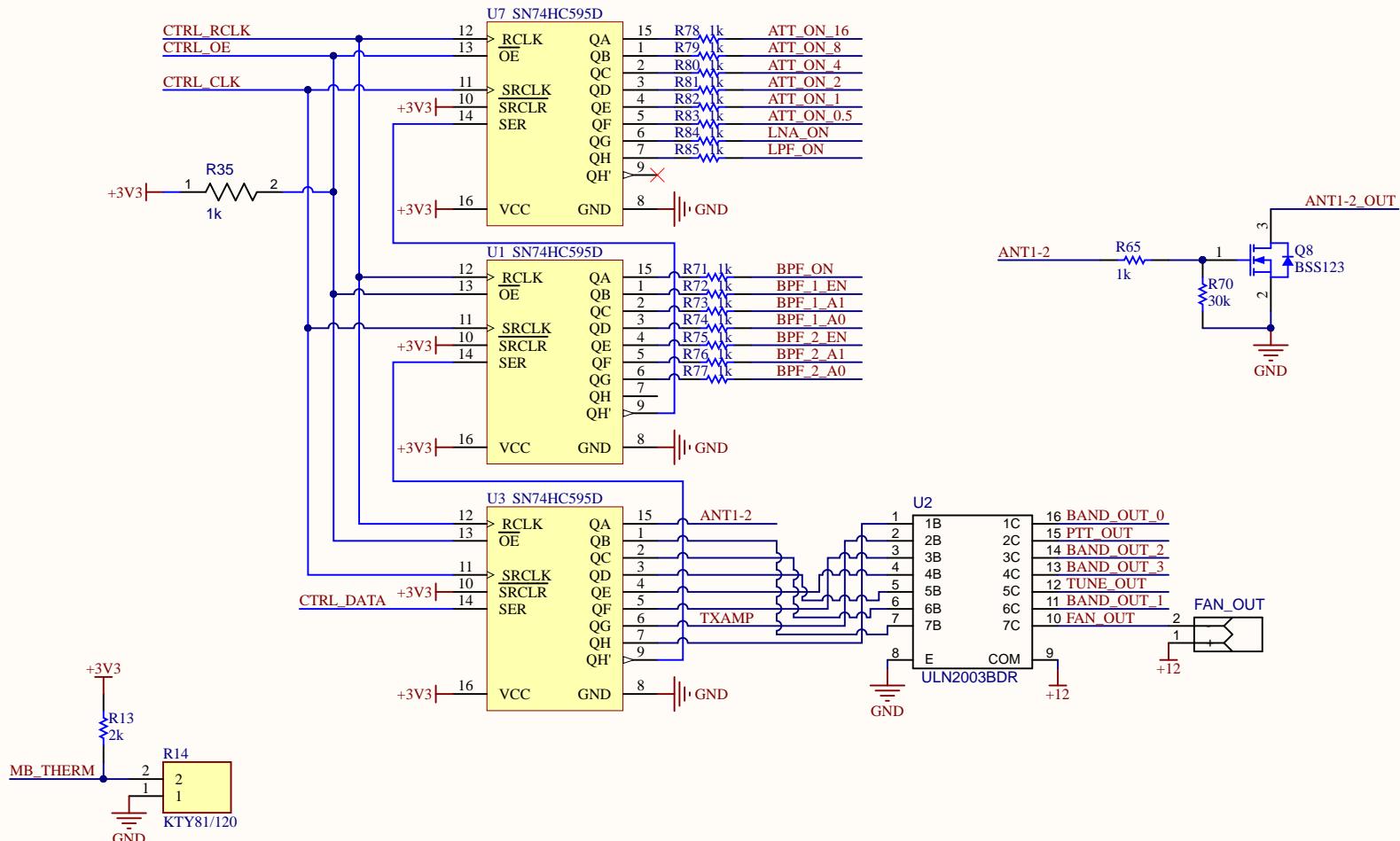
C

Title **CONN**

Size: A4 Number:14 Revision:2.0

Date: 11.11.2020 Time: 20:09:43 Sheet 14 of 18

File: D:\Dropbox\Develop\Projects\WOLF\Scheme\ALTIUM\_DESIGNER\RF-UNIT\CONN.SchDoc

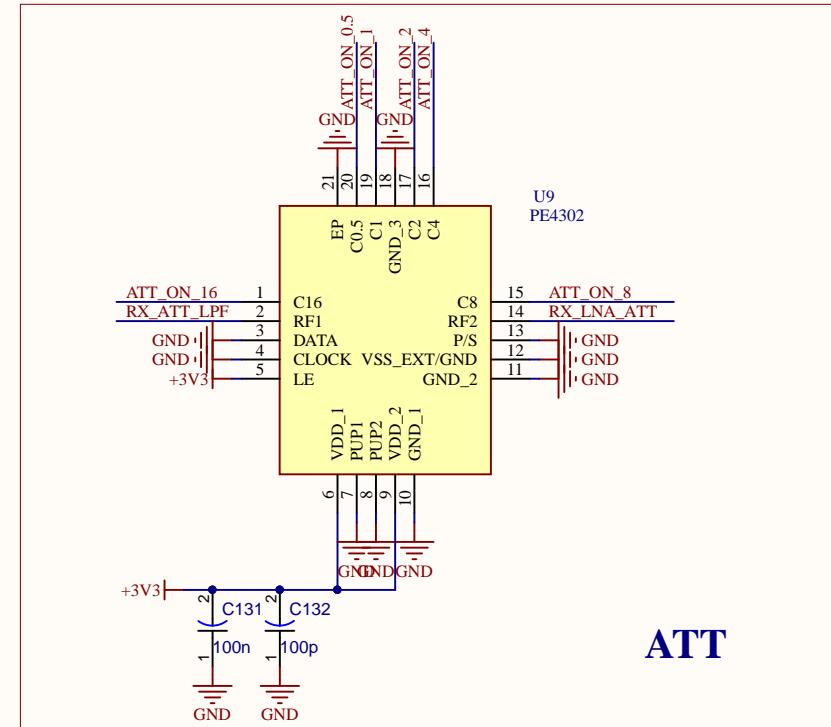
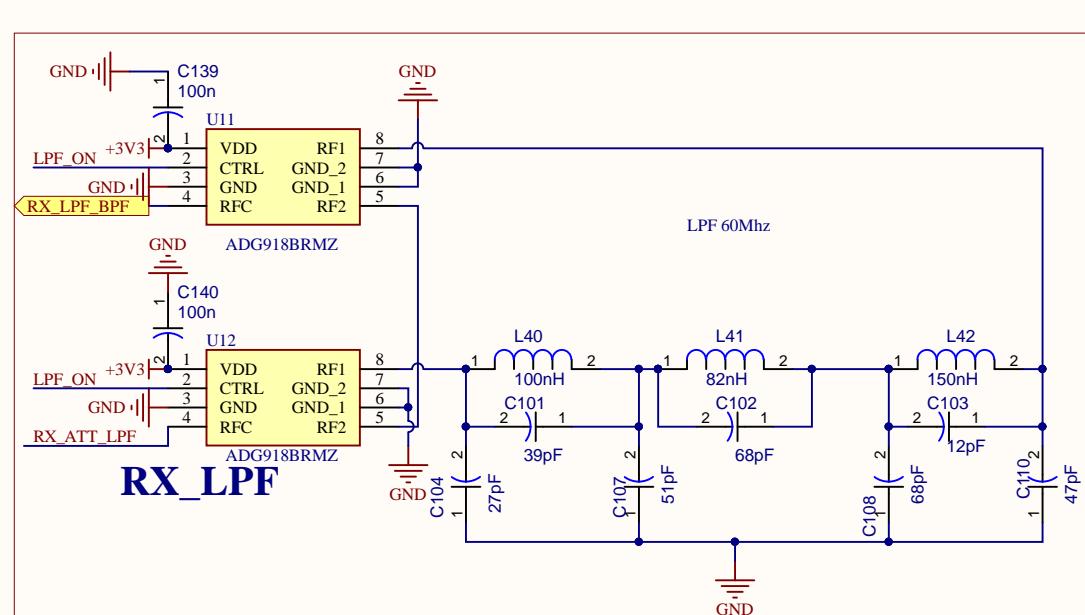
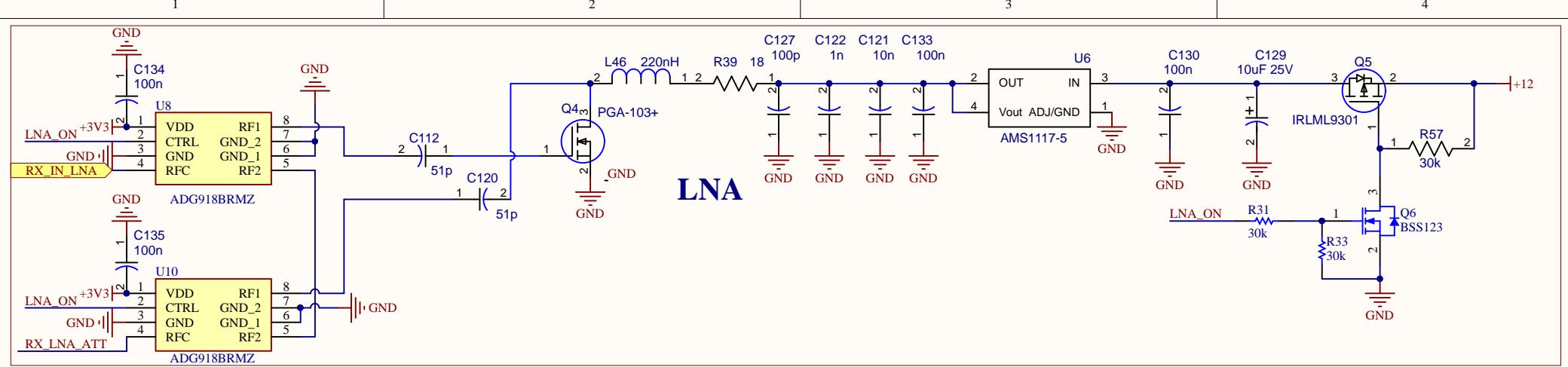
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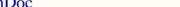
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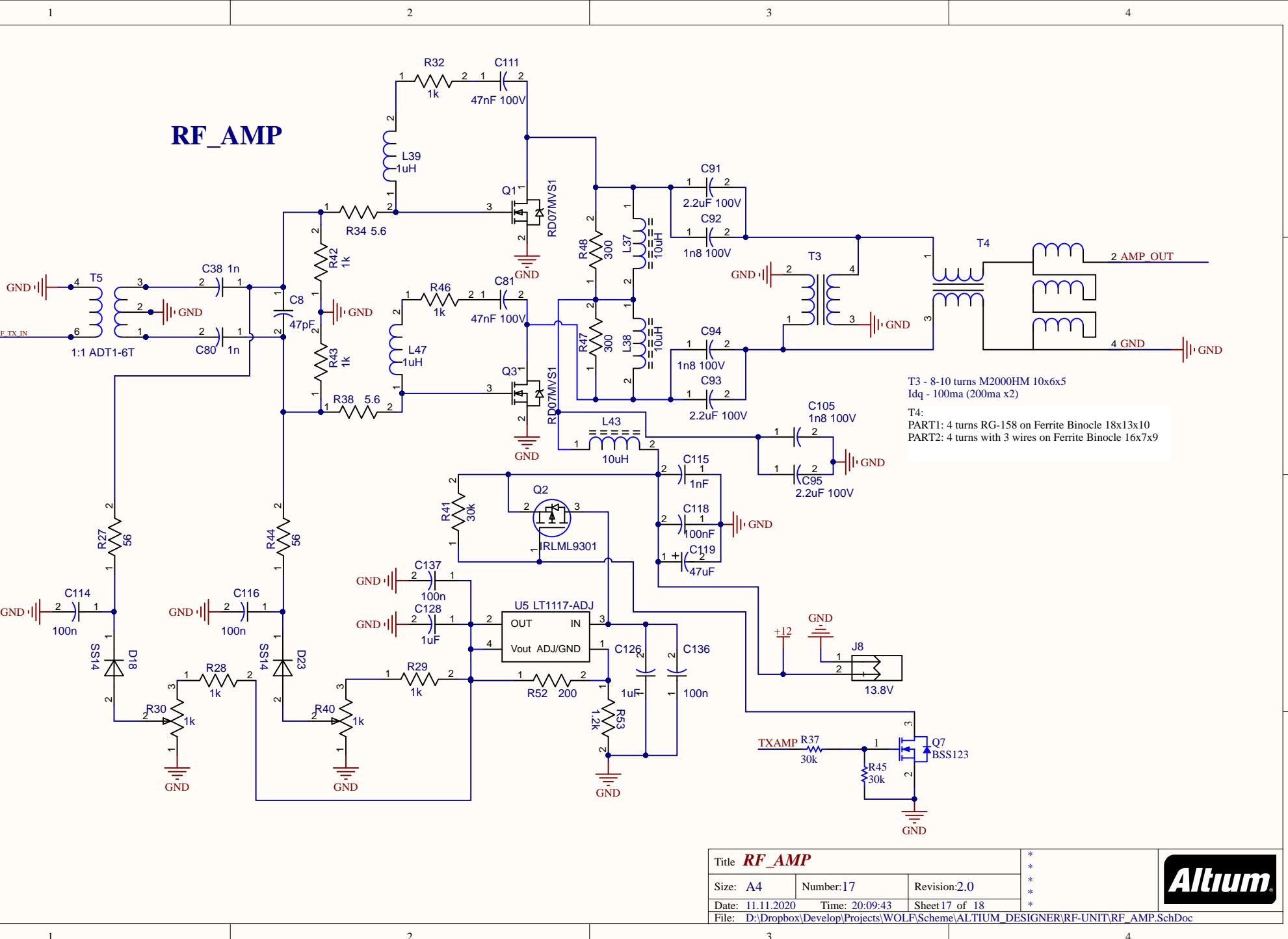
Date: 11.11.2020 Time: 20:09:43 Sheet 15 of 18

File: D:\Dropbox\Develop\Projects\WOLF\Scheme\ALTIUM\_DESIGNER\RF-UNIT\CONTROL.SchDoc

**Altium**

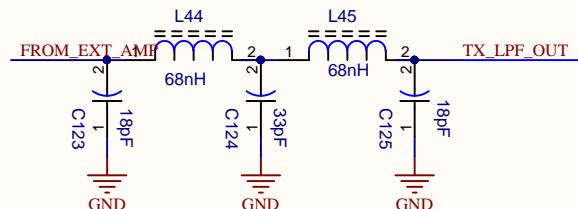


Title <b>LNA</b>	*	
Size: A4	Number:16	Revision:2.0
Date: 11.11.2020	Time: 20:09:43	Sheet 16 of 18
File: D:\Dropbox\Develop\Projects\WOLF\Scheme\ALTIUM DESIGNER\RF-UNIT\LNA.SchDoc		

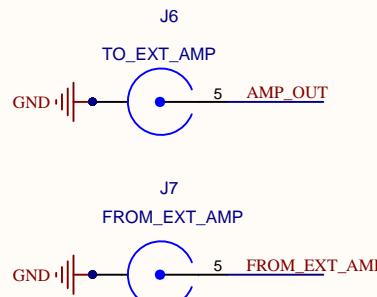
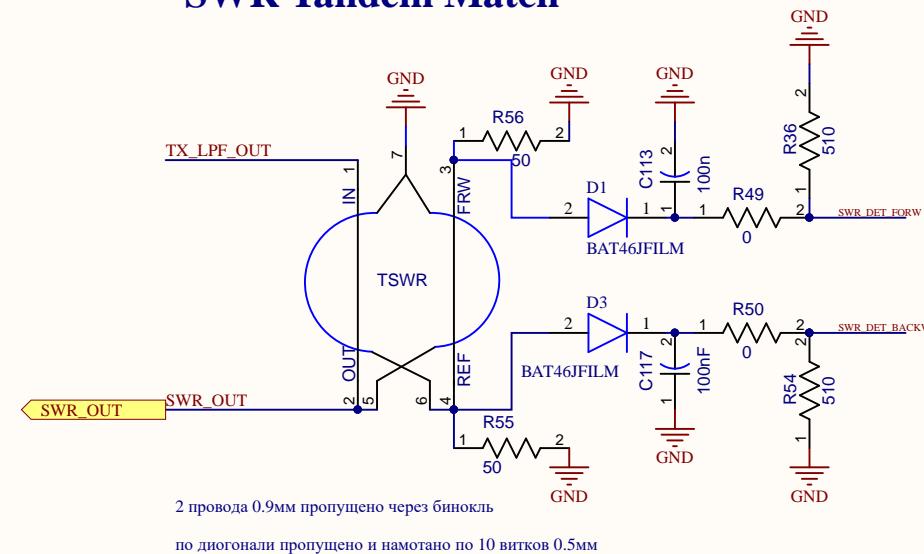


**TX\_LPF**

LPF 170Mhz



Катушки намотаны проводом 0.5мм на оправке диаметром 5мм, 3.5 витка

**SWR Tandem Match**Title ***SWR Tandem Match***

Size: A4 Number:18 Revision:2.0

Date: 11.11.2020 Time: 20:09:43 Sheet 18 of 18

File: D:\Dropbox\Develop\Projects\WOLF\Scheme\ALTIUM\_DESIGNER\RF-UNIT\SWR Tandem Match.SchDoc

**Altium**