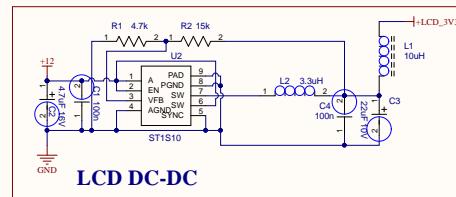


7Inch version

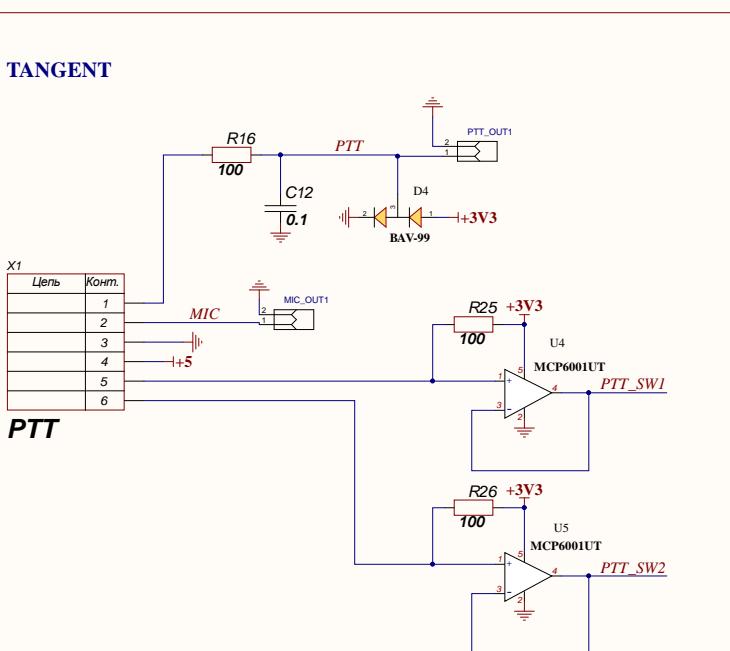
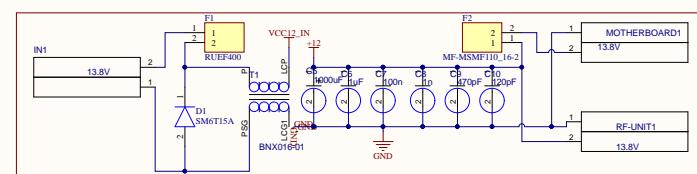
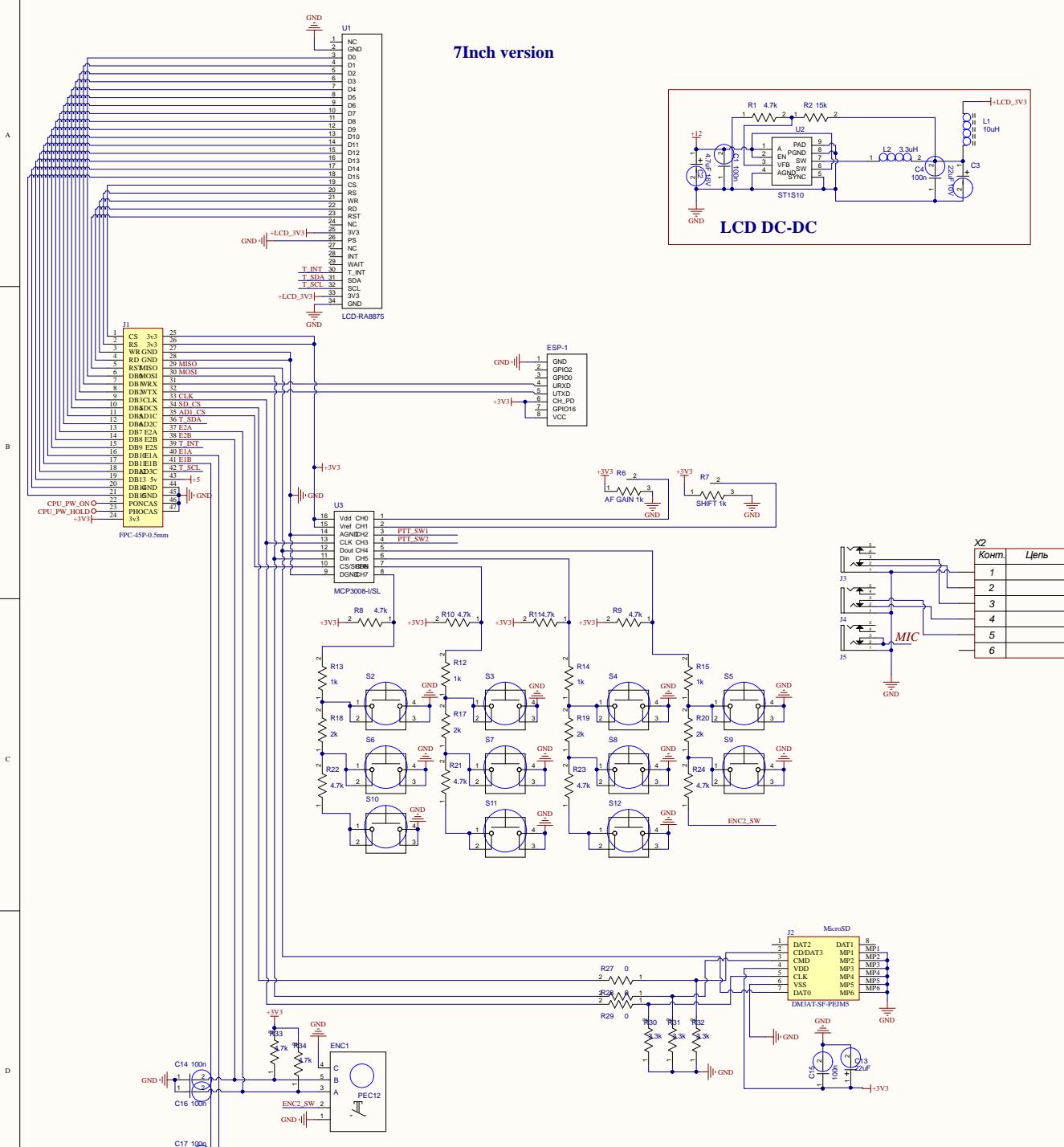


A

B

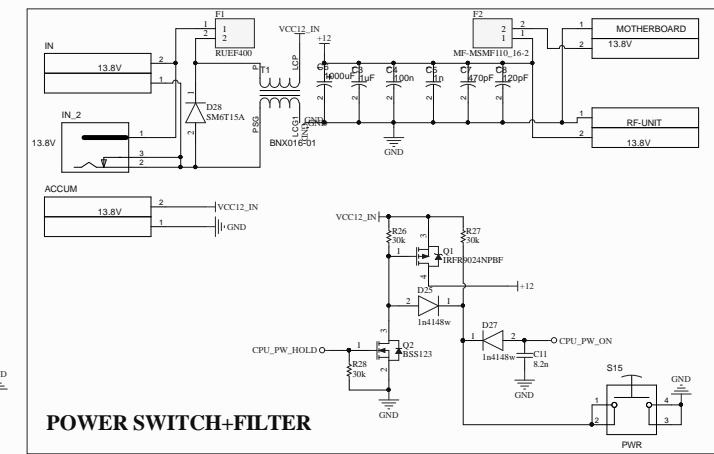
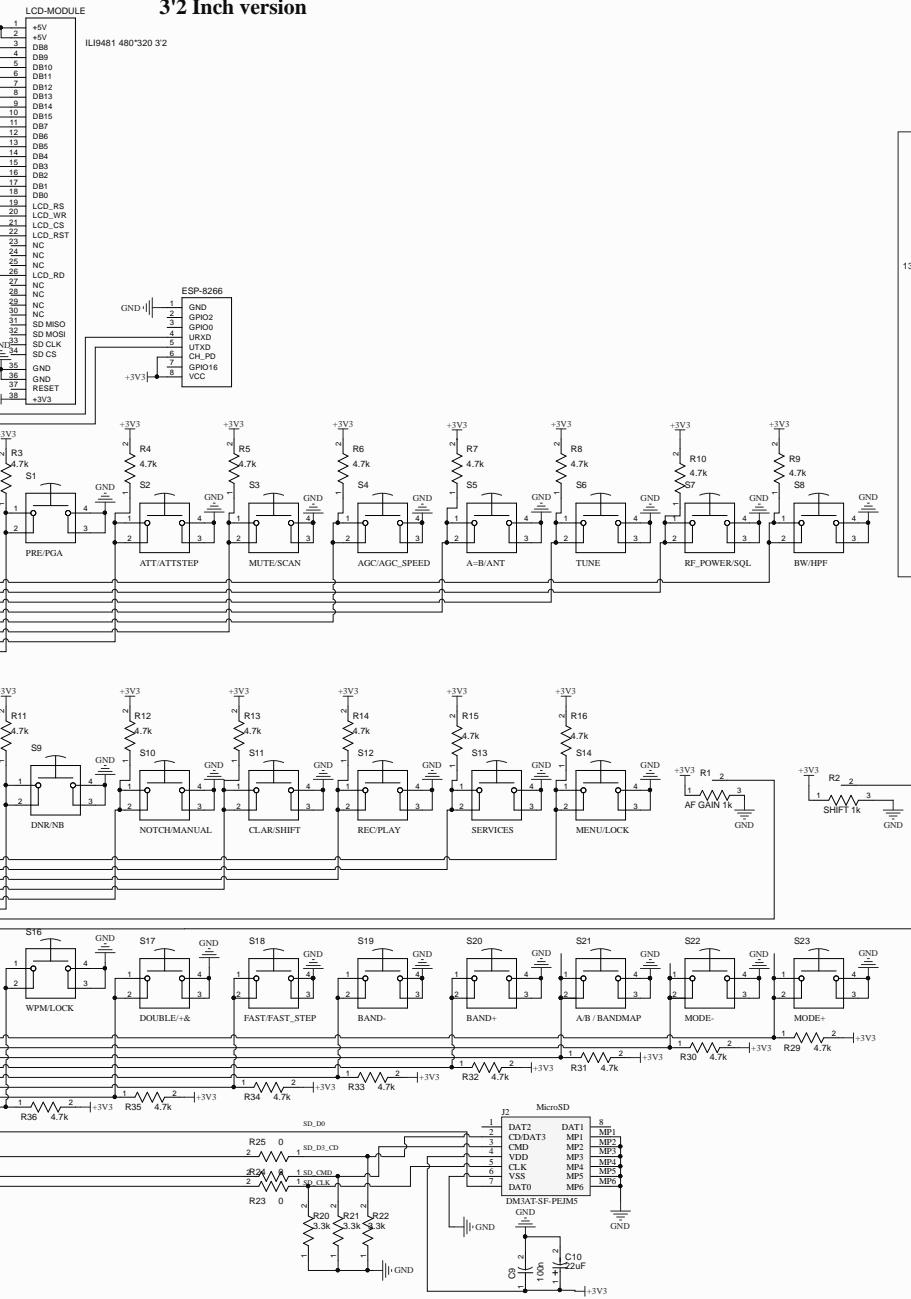
C

D



3'2 Inch version

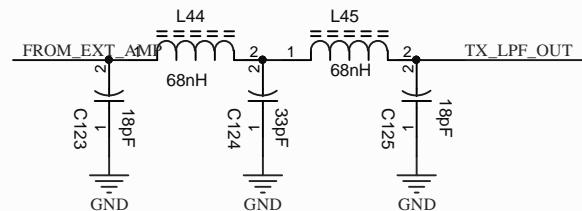
ILI9481 480*320 3'2



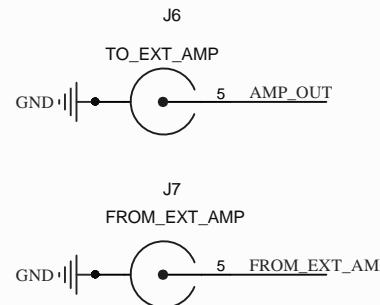
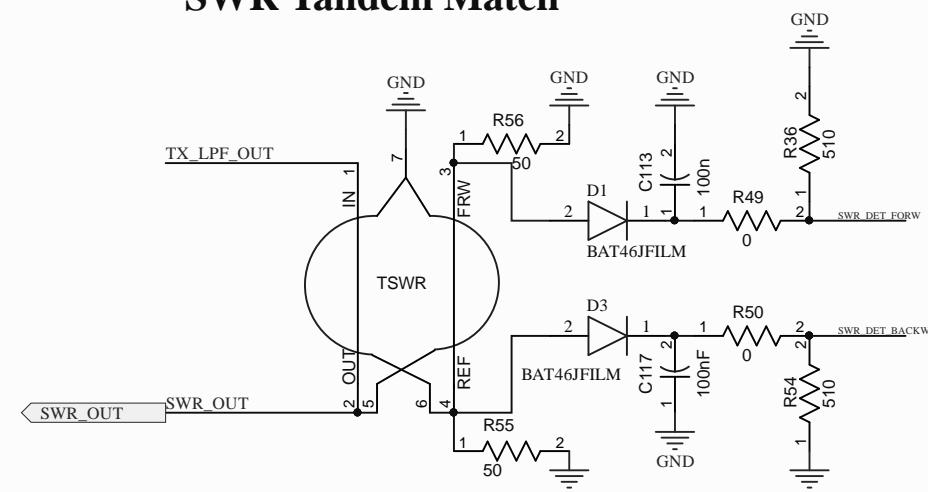
POWER SWITCH+FILTER

TX_LPF

LPF 170Mhz



Катушки намотаны проводом 0.5мм на оправке диаметром 5мм, 3.5 витка

**SWR Tandem Match**

2 провода 0.9мм пропущено через бинокль

по диагонали пропущено и намотано по 10 витков 0.5мм

Title **SWR Tandem Match**

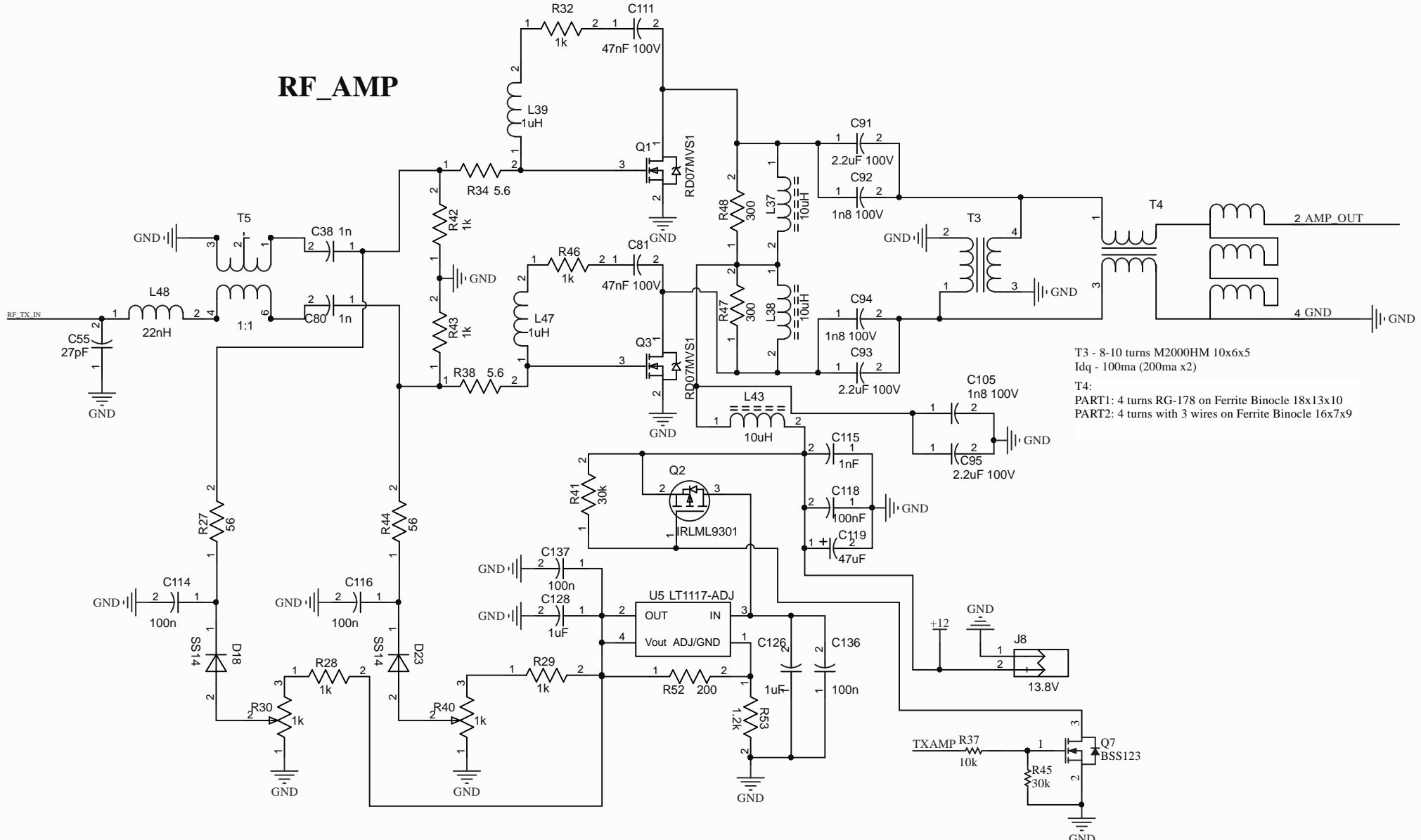
Size: A4 Number:18 Revision:2.0

Date: 07.12.2020 Time: 23:45:30 Sheet 18 of 18

File: D:\Dropbox\Develop\Projects\WOLF\Scheme\ALTIUM_DESIGNER\RF-UNIT\SWR Tandem Match.SchDoc

Altium

A

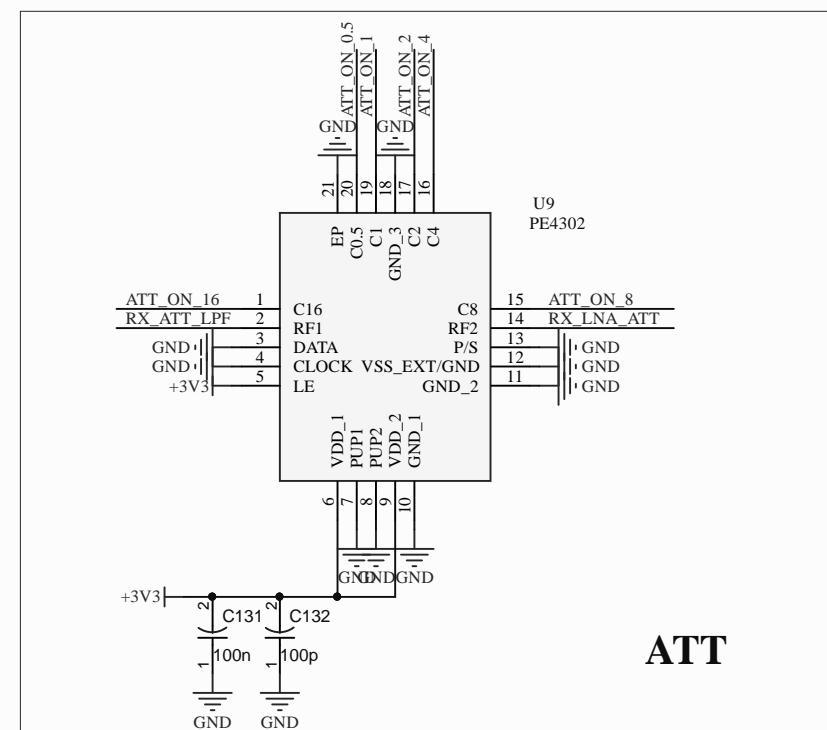
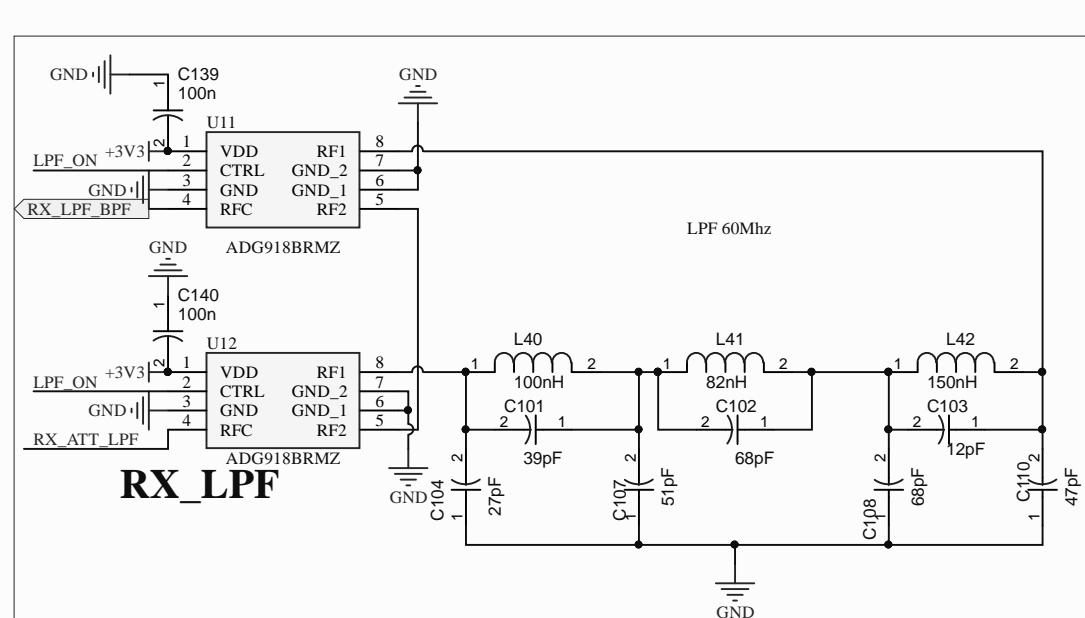
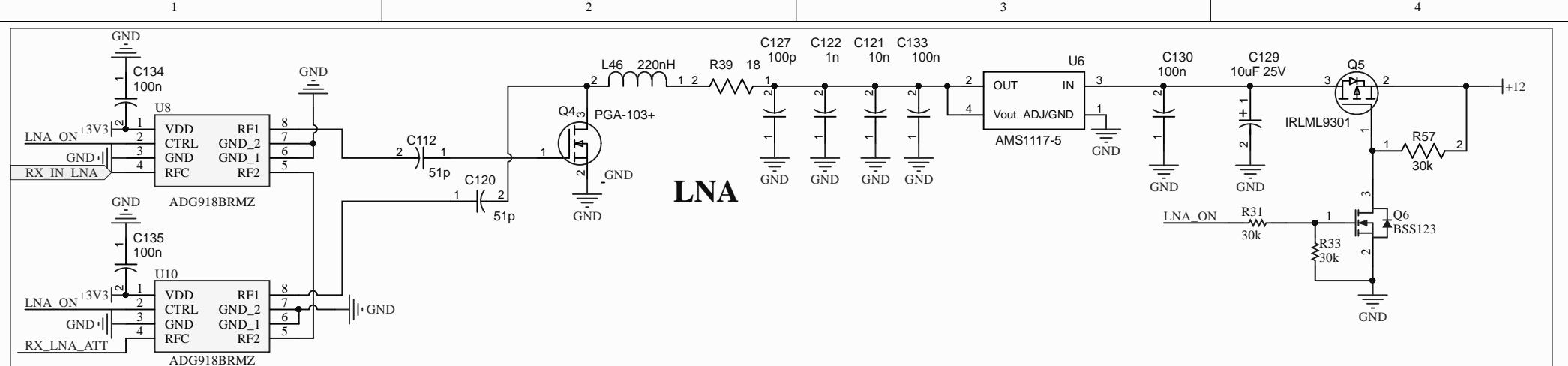
RF_AMPTitle **RF_AMP**

Size: A4 Number:17 Revision2.0

Date: 07.12.2020 Time: 23:45:32 Sheet17 of 18

File: D:\Dropbox\Develop\Projects\WOLF\Scheme\ALTIUM_DESIGNER\RF-UNIT\RF_AMP.SchDoc

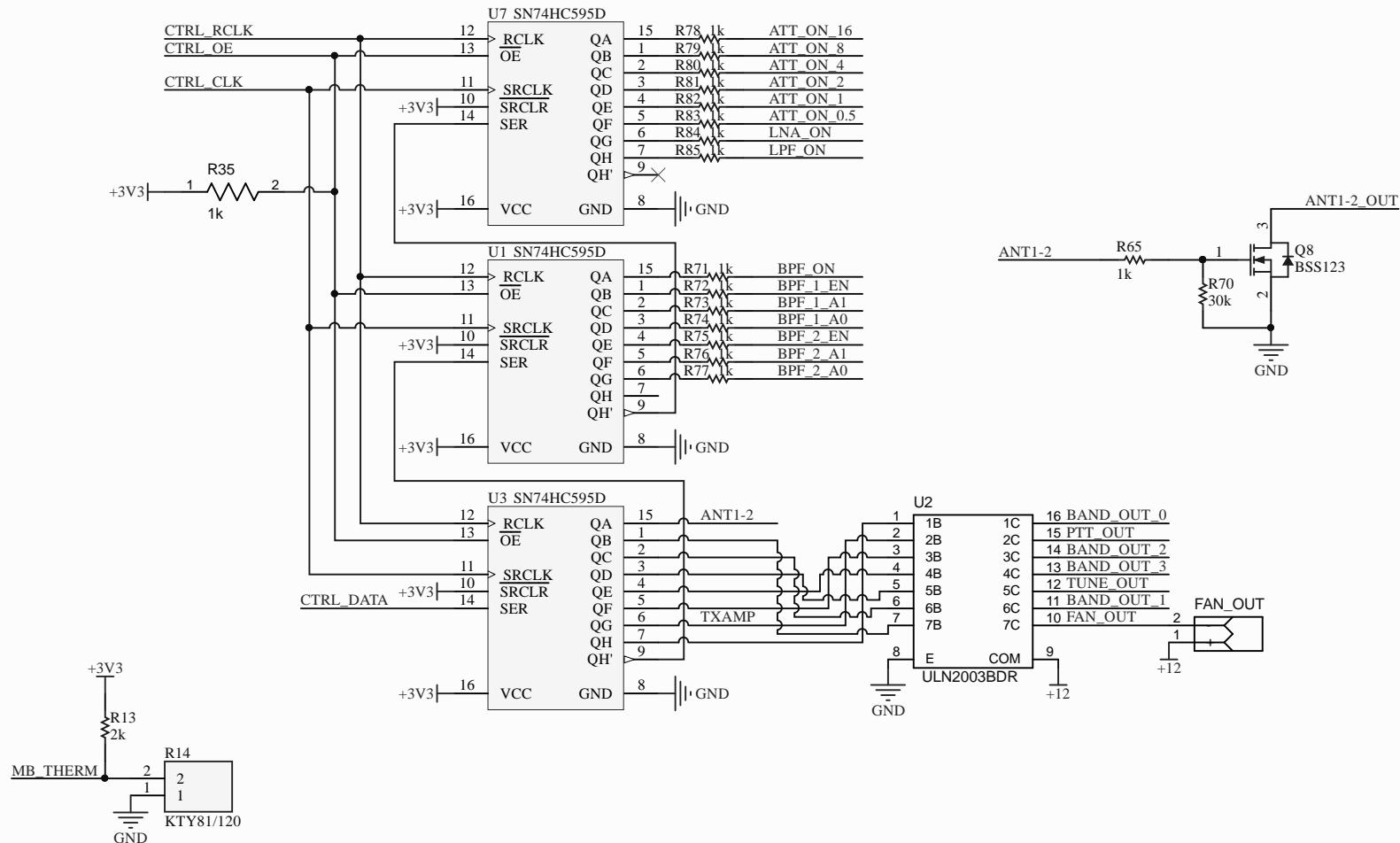
Altium



Title LNA			*
Size: A4	Number:16	Revision2.0	*
Date: 07.12.2020	Time: 23:45:33	Sheet16 of 18	*
File: D:\Dropbox\Develop\Projects\WOLF\Scheme\ALTIUM_DESIGNER\RF-UNIT\LNA.SchDoc			

Altium

A

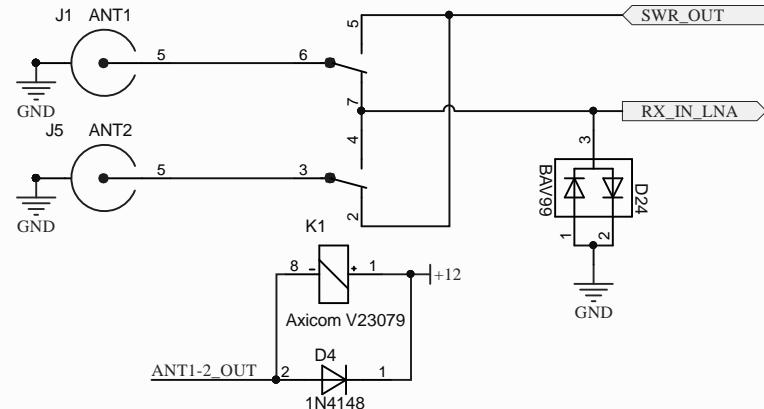
Title **CONTROL**

Size: A4	Number:15	Revision2.0
Date: 07.12.2020	Time: 23:45:35	Sheet15 of 18
File: D:\Dropbox\Develop\Projects\WOLF\Scheme\ALTIUM_DESIGNER\RF-UNIT\CONTROL.SchDoc		*

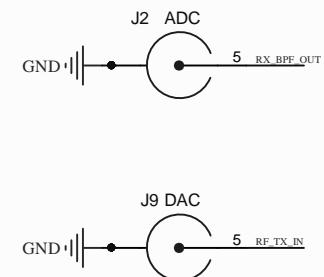
Altium

A

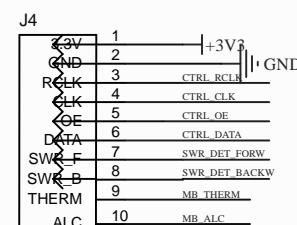
TXRX_COMUTATOR



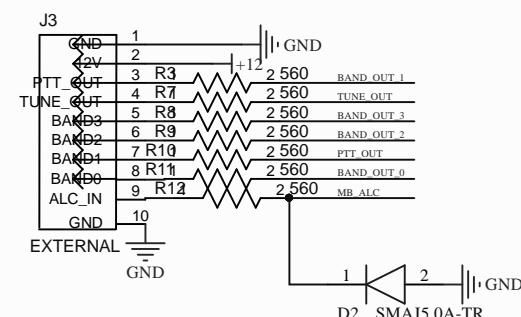
CONN



B



MOTHERBOARD



C

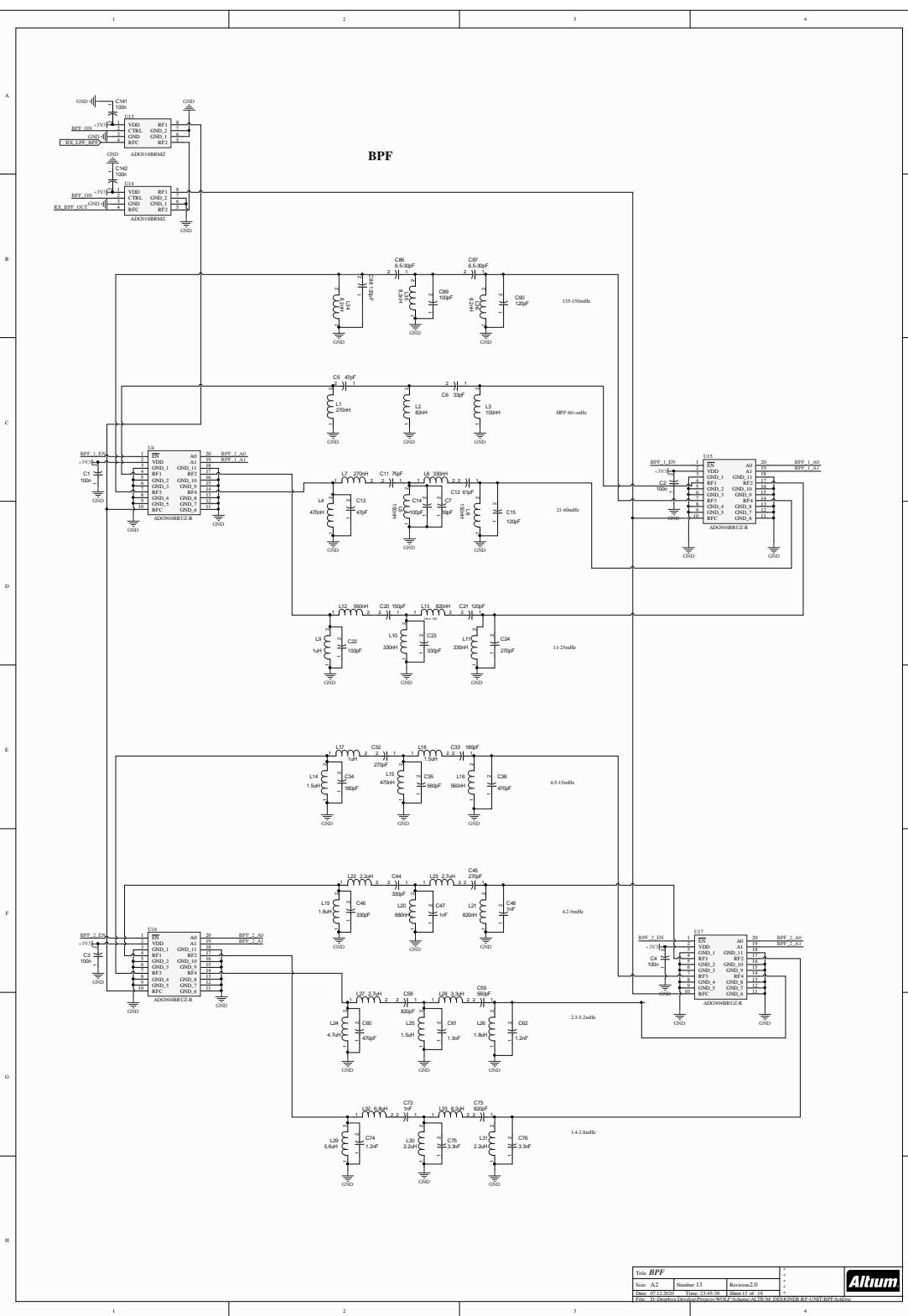
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Size: A4 Number:14 Revision2.0

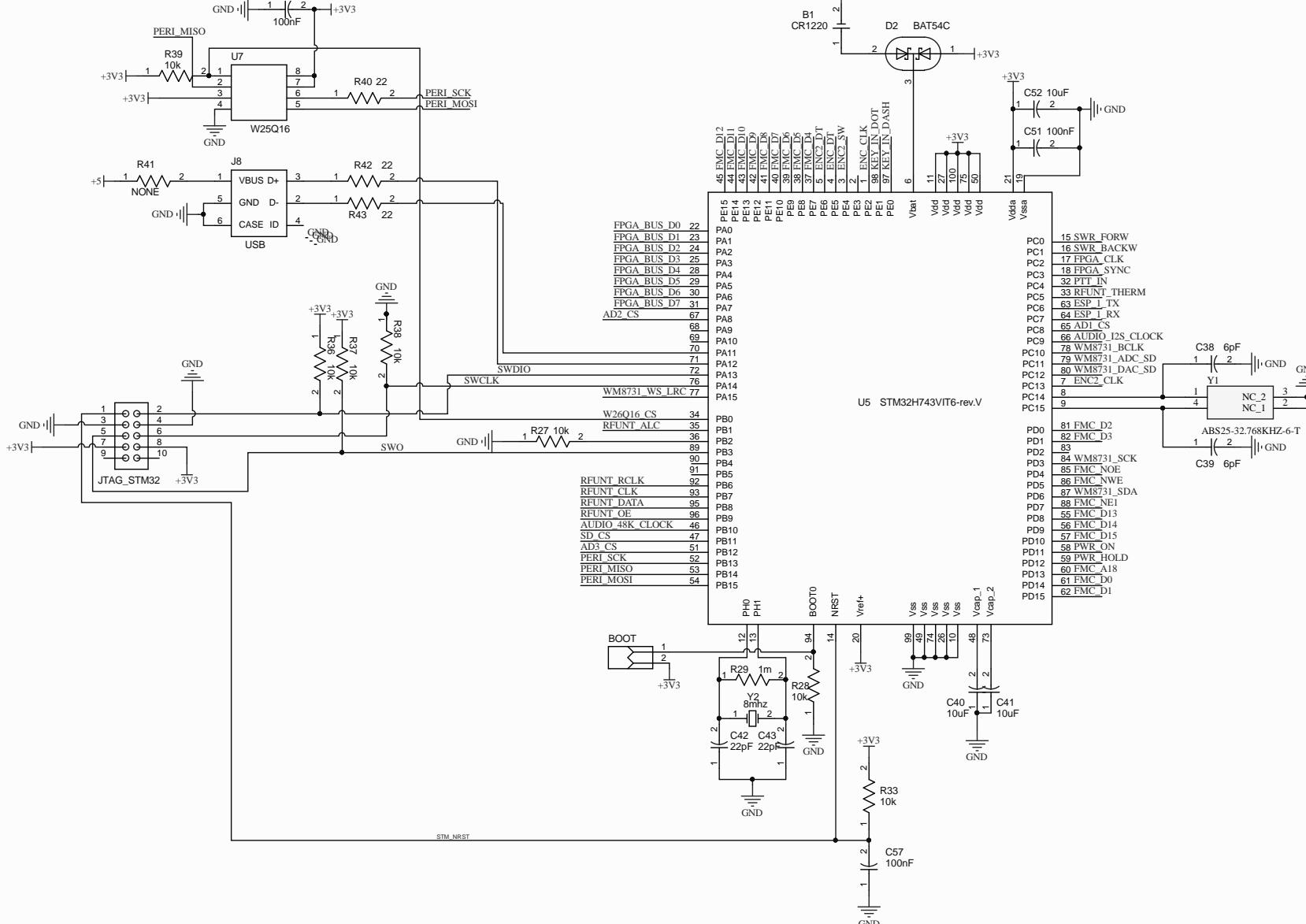
Date: 07.12.2020 Time: 23:45:36 Sheet14 of 18

File: D:\Dropbox\Develop\Projects\WOLF\Schema\ALTIUM_DESIGNER\RF-UNIT\CONN.SchDoc

D



STM32

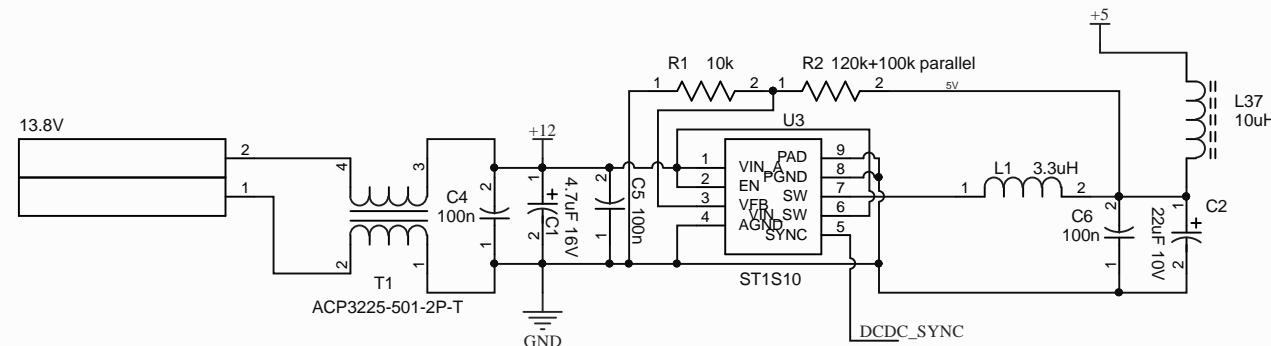
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Size: A3 Number: 11 Revision: 2.0

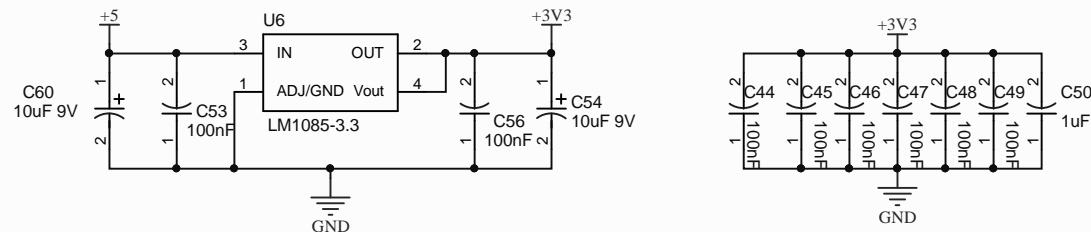
Date: 07.12.2020 Time: 23:45:40 Sheet 11 of 18

File: D:\Dropbox\Develop\Projects\WOLF\Scheme\ALTIUM DESIGNER\MOTHERBOARD\STM32.SchDoc

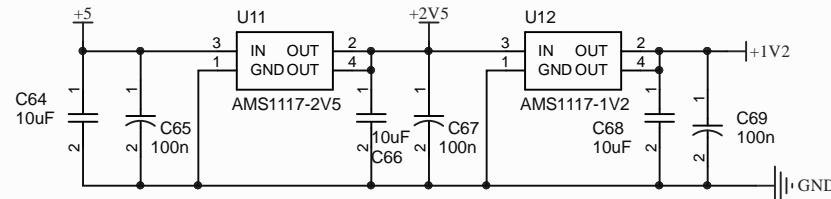
A



B

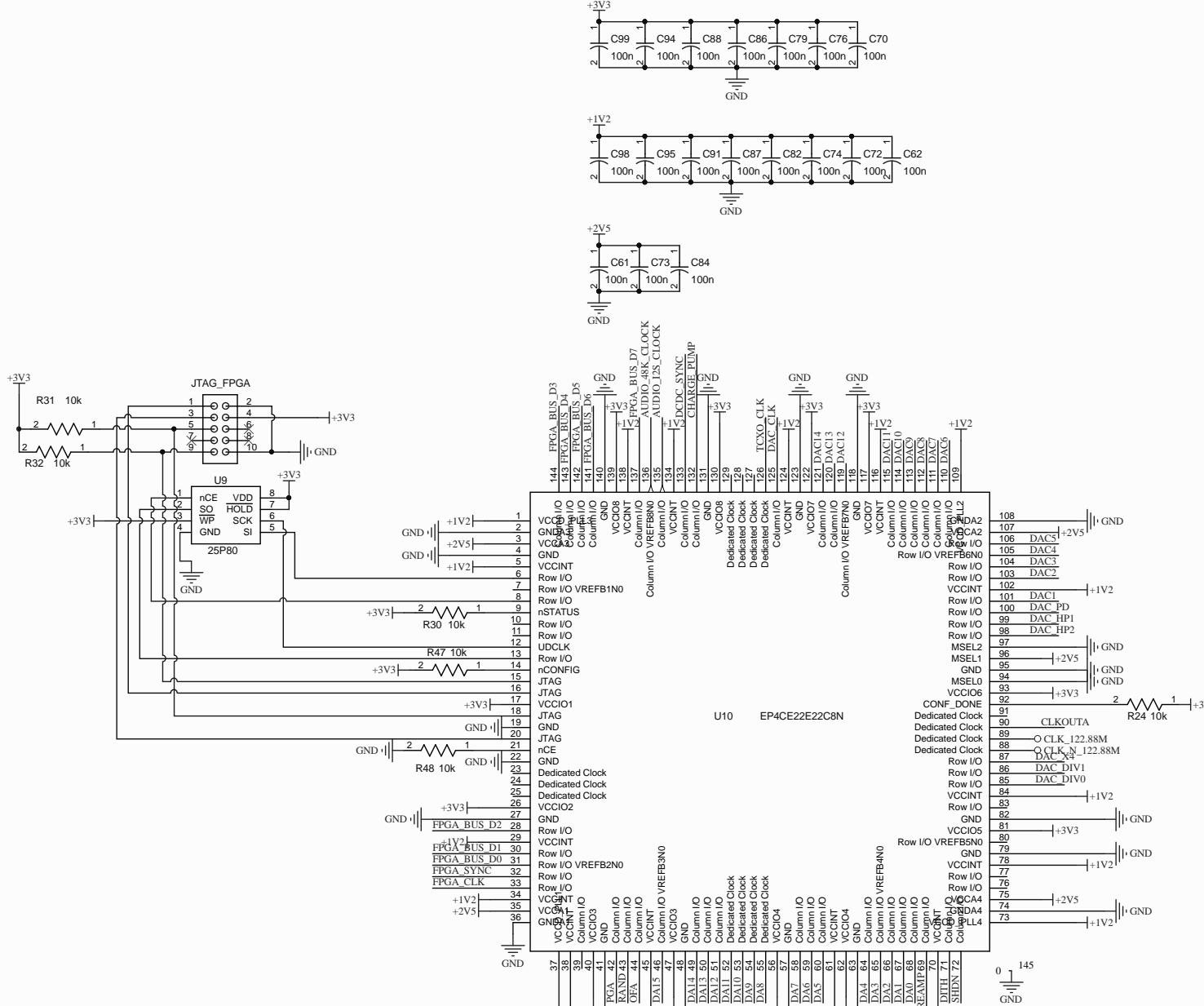


C



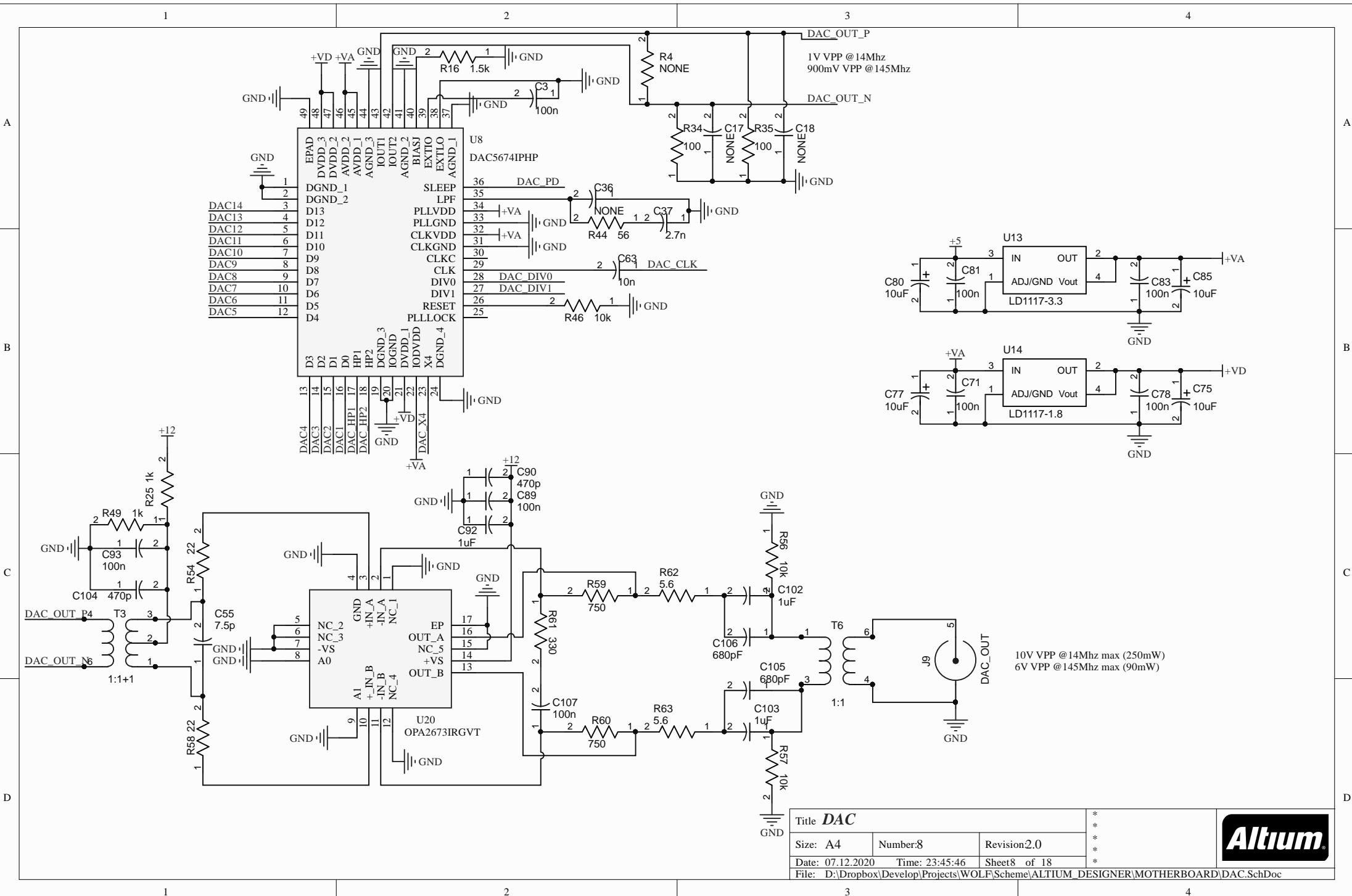
D

Title POWER			*
Size: A4	Number:10	Revision2.0	*
Date: 07.12.2020	Time: 23:45:42	Sheet10 of 18	*
File: D:\Dropbox\Develop\Projects\WOLF\Scheme\ALTIUM_DESIGNER\MOTHERBOARD\POWER.SchDoc			*

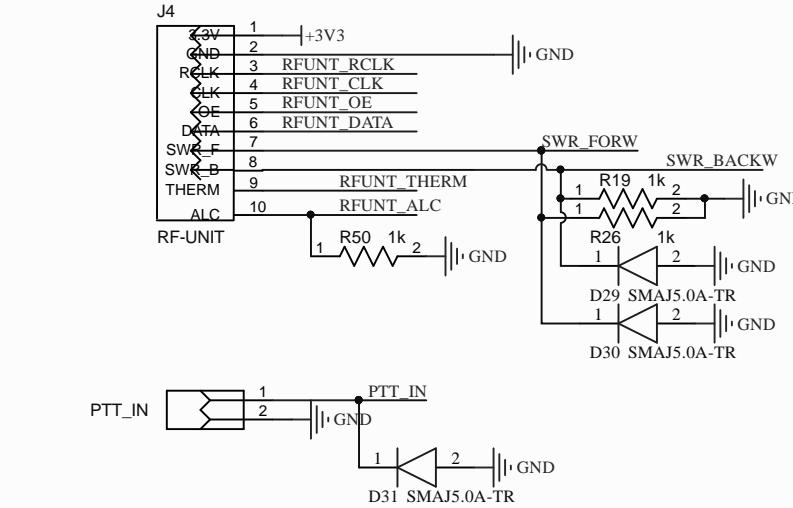
Title **FPGA**

Size: A3	Number: 9	Revision: 2.0
Date: 07.12.2020	Time: 23:45:43	Sheet 9 of 18
File: D:\Dropbox\Develop\Projects\WOLF\Scheme\ALTIUM DESIGNER\MOTHERBOARD\FPGA.SchDoc		





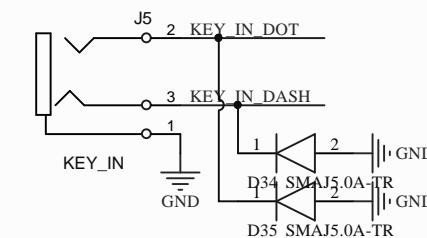
A



J6

1	CS 3v3
2	FMC_A18
3	RS 3v3
4	WR GND
5	RD GND
6	STM_NRST
7	RST_MISO
8	FMC_D1
9	FMC_D2
10	FMC_D3
11	FMC_D4
12	FMC_D5
13	FMC_D6
14	FMC_D7
15	FMC_D8
16	FMC_D9
17	FMC_D10
18	FMC_D11
19	FMC_D12
20	FMC_D13
21	FMC_D14
22	PWR_ON
23	PWR_HOLD
24	+3V3
25	PERI_MOSI
26	DB0_MOSI
27	DB1_WRX
28	DB2_WTX
29	DB3_CLK
30	DB4\$DCS
31	DB5\$AD1C
32	DB6\$AD2C
33	DB7_E2A
34	DB8_E2B
35	DB9_E2S
36	DB10\$E1A
37	DB11\$E1B
38	DB12\$AD3C
39	DB13_5v
40	DB14\$GND
41	DB15\$GND
42	DB16\$GND
43	DB17\$GND
44	+5
45	DB18\$GND
46	DB19\$GND
47	DB20\$GND

FPC-45P-0.5mm



Title **CONNECTIONS**

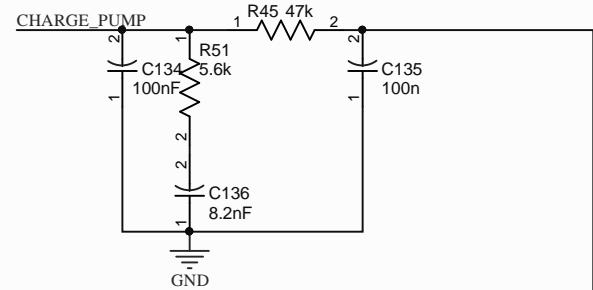
Size: A4	Number:7	Revision2.0
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Date: 07.12.2020	Time: 23:45:48	Sheet7 of 18
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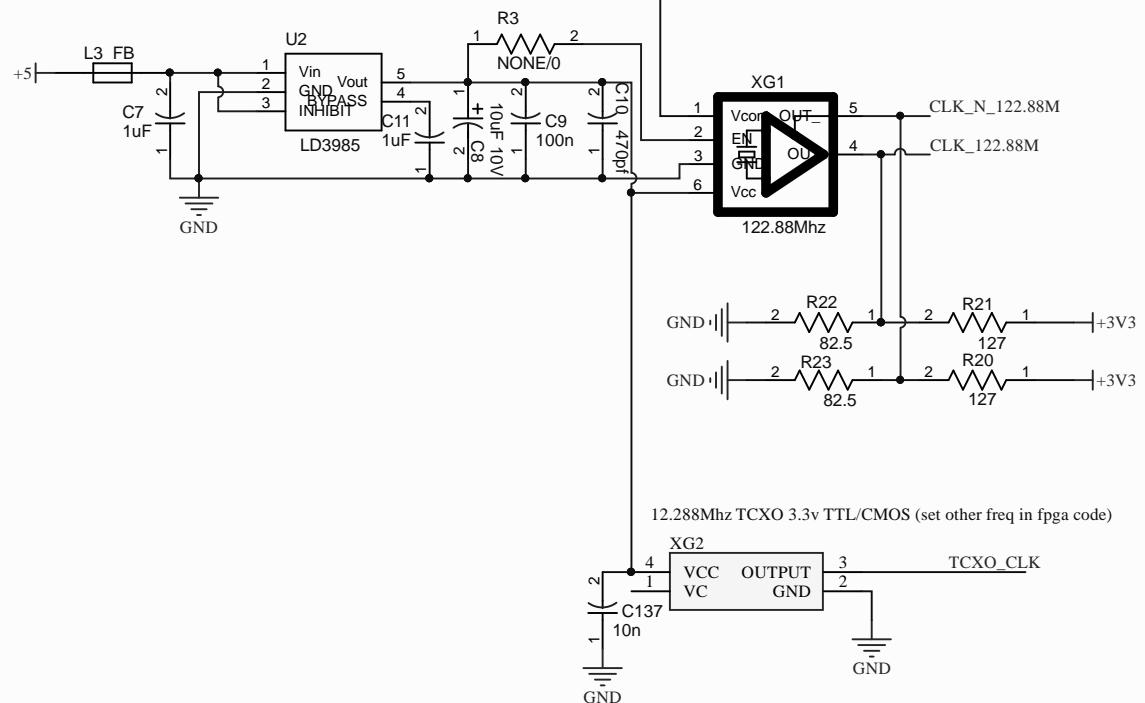
File: D:\Dropbox\Develop\Projects\WOLF\Scheme\ALTIUM_DESIGNER\MOTHERBOARD\CONNECTIONS.SchDoc	*
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Altium

A



B



C

D

Title **CLOCK_GENERATOR**

Size: A4 Number:6 Revision 2.0

Date: 07.12.2020 Time: 23:45:49 Sheet 6 of 18

File: D:\Dropbox\Develop\Projects\WOLF\Scheme\ALTIUM_DESIGNER\MOTHERBOARD\CLOCK_GENERATOR.SchDoc

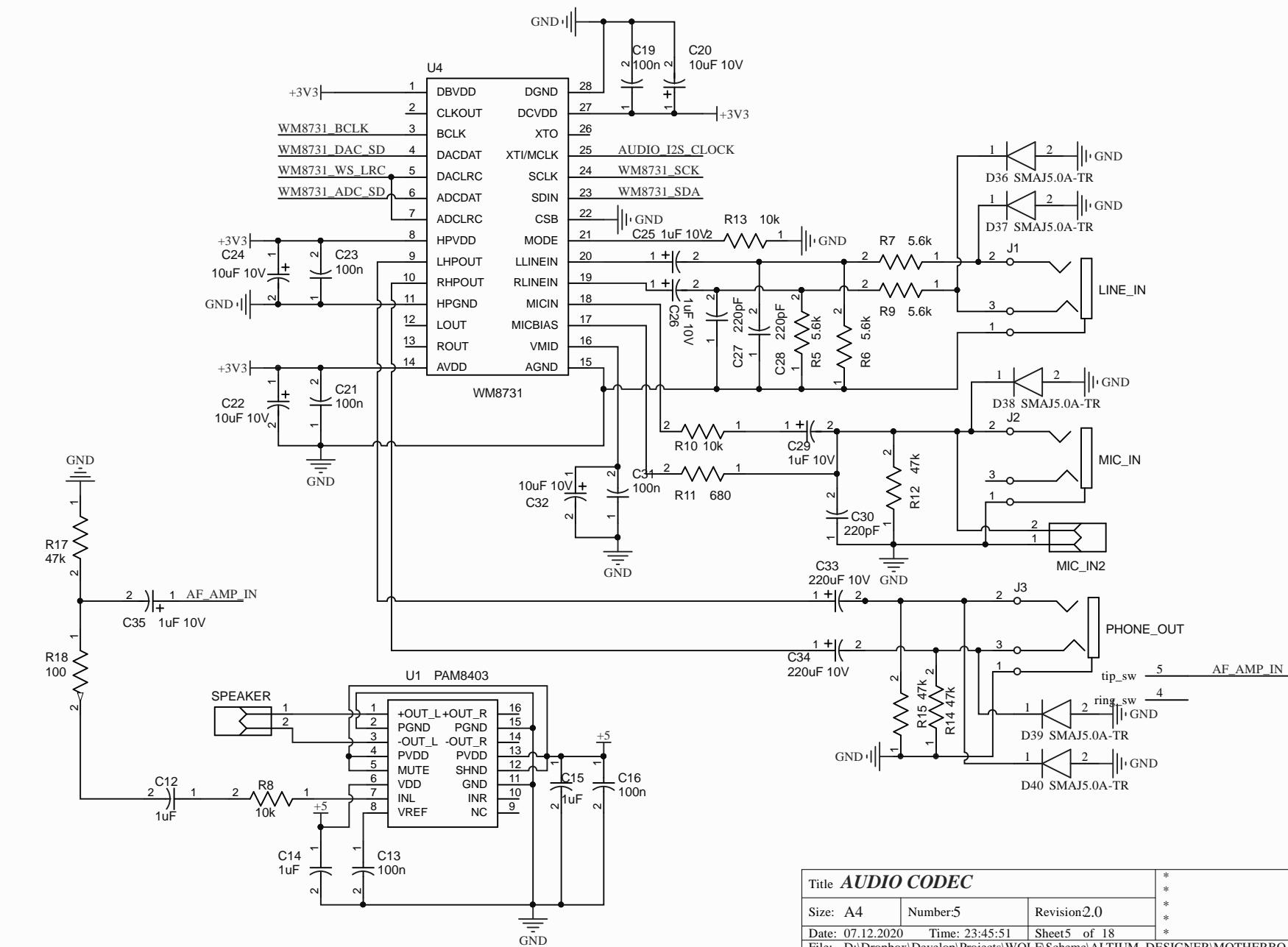
Altium

A

B

C

D

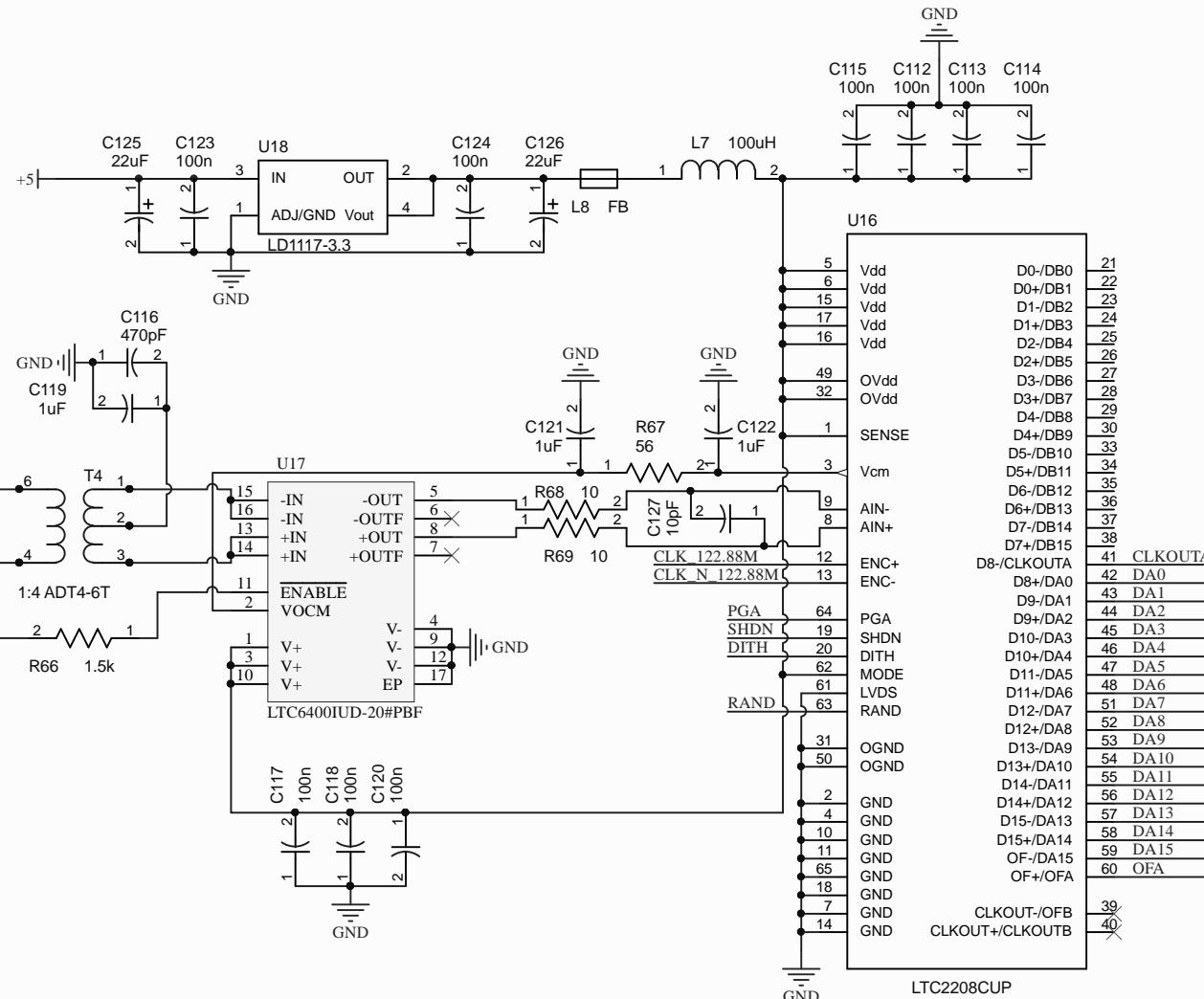
Title **AUDIO CODEC**

Size: A4 Number:5 Revision 2.0

Date: 07.12.2020 Time: 23:45:51 Sheet 5 of 18

File: D:\Dropbox\Develop\Projects\WOLF\Schema\ALTIUM_DESIGNER\MOTHERBOARD\AUDIO_CODEC.SchDoc

Altium

Title **ADC**

Size: A4 Number:3 Revision 2.0

Date: 07.12.2020 Time: 23:45:52 Sheet 3 of 18

File: D:\Dropbox\Develop\Projects\WOLF\Scheme\ALTIUM_DESIGNER\MOTHERBOARD\ADC.SchDoc

Altium