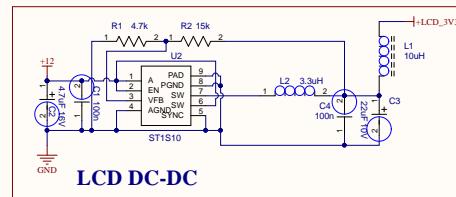


7Inch version

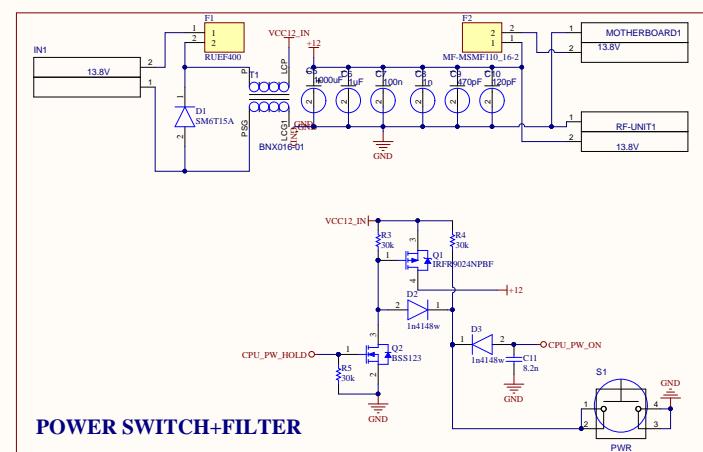
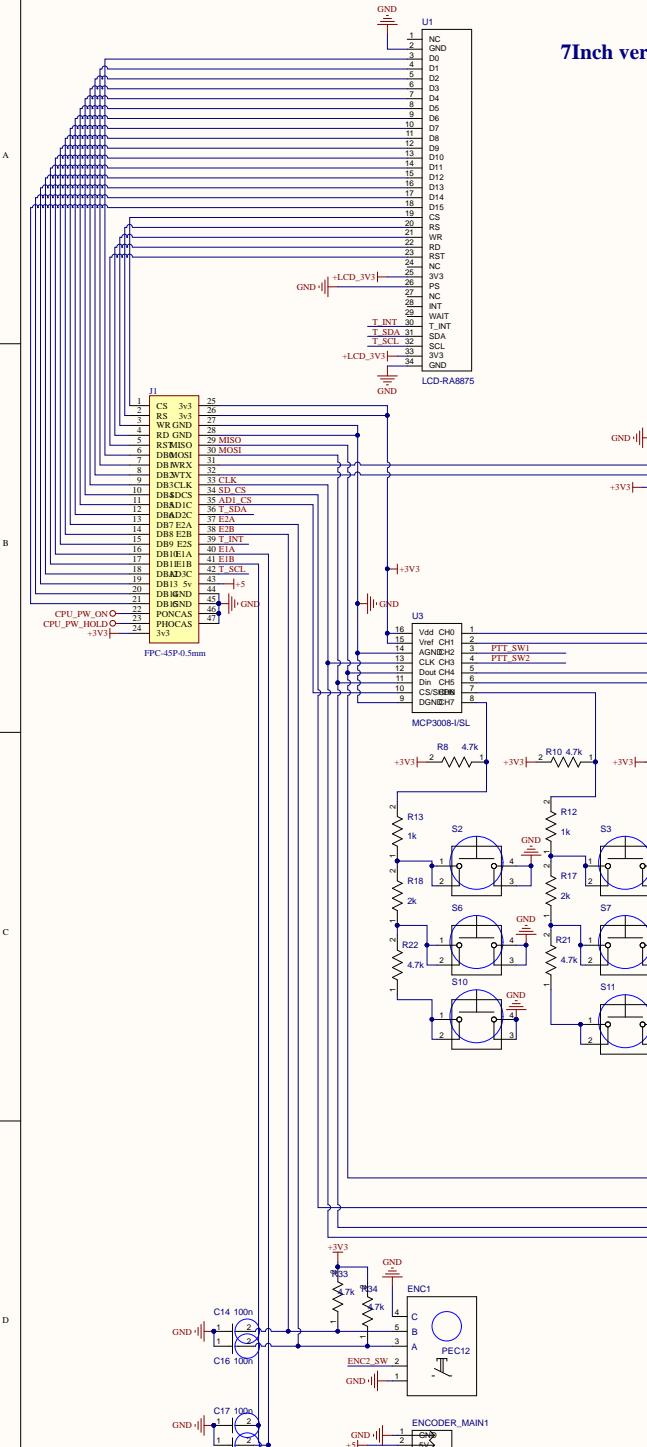


A

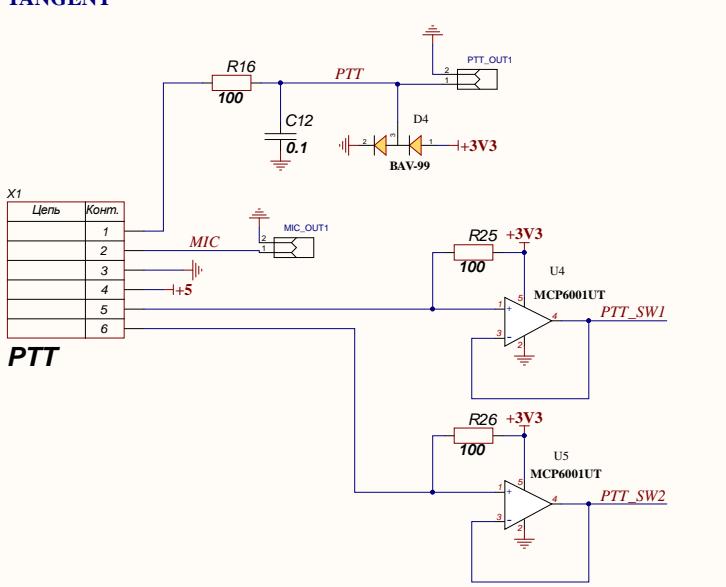
B

C

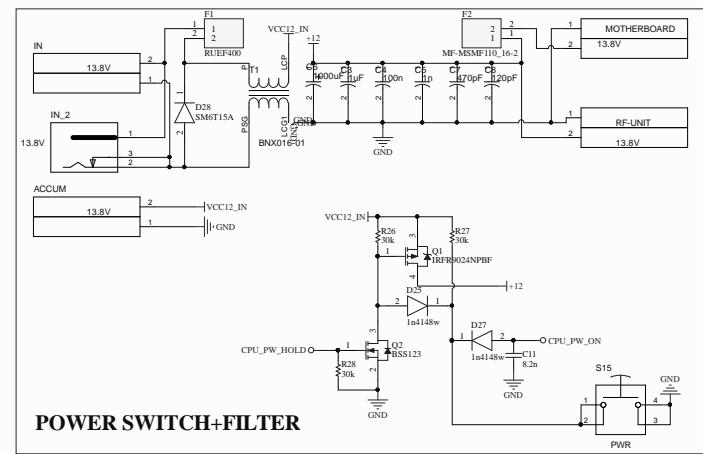
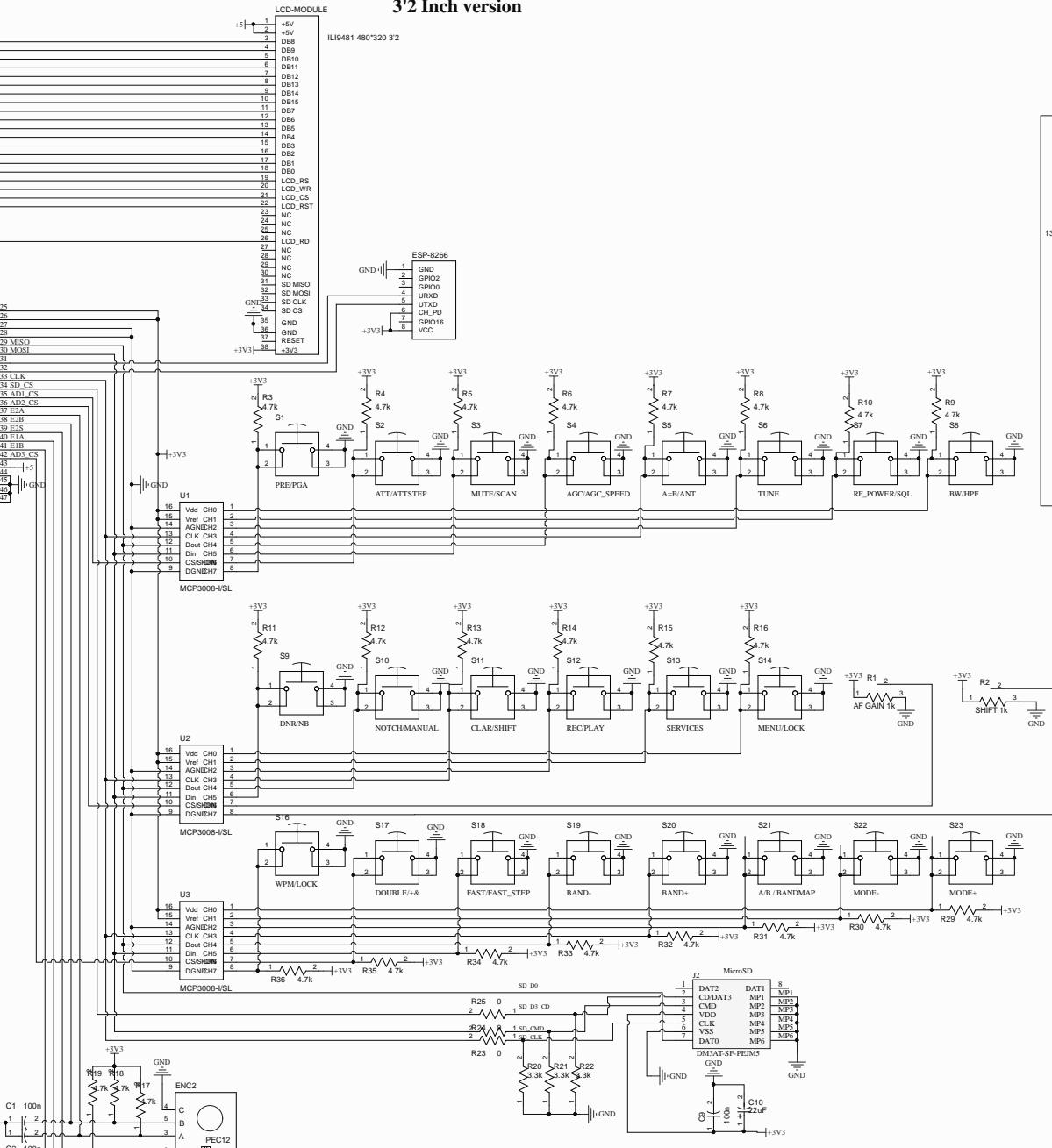
D



TANGENT

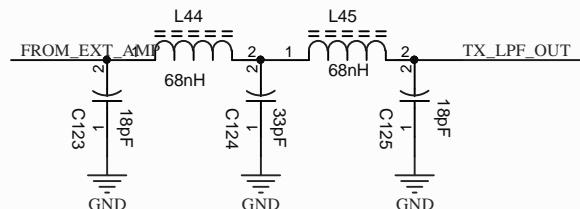


3'2 Inch version

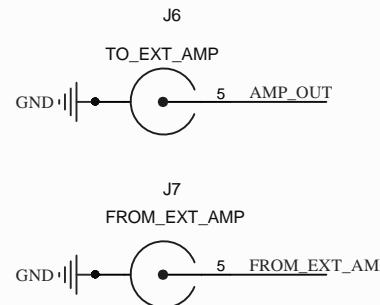
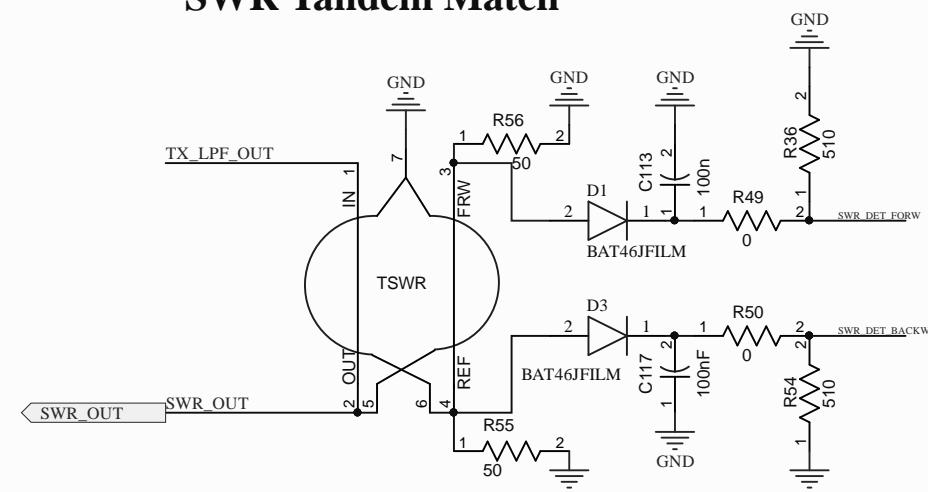


TX_LPF

LPF 170Mhz



Катушки намотаны проводом 0.5мм на оправке диаметром 5мм, 3.5 витка

**SWR Tandem Match**

2 провода 0.9мм пропущено через бинокль

по диагонали пропущено и намотано по 10 витков 0.5мм

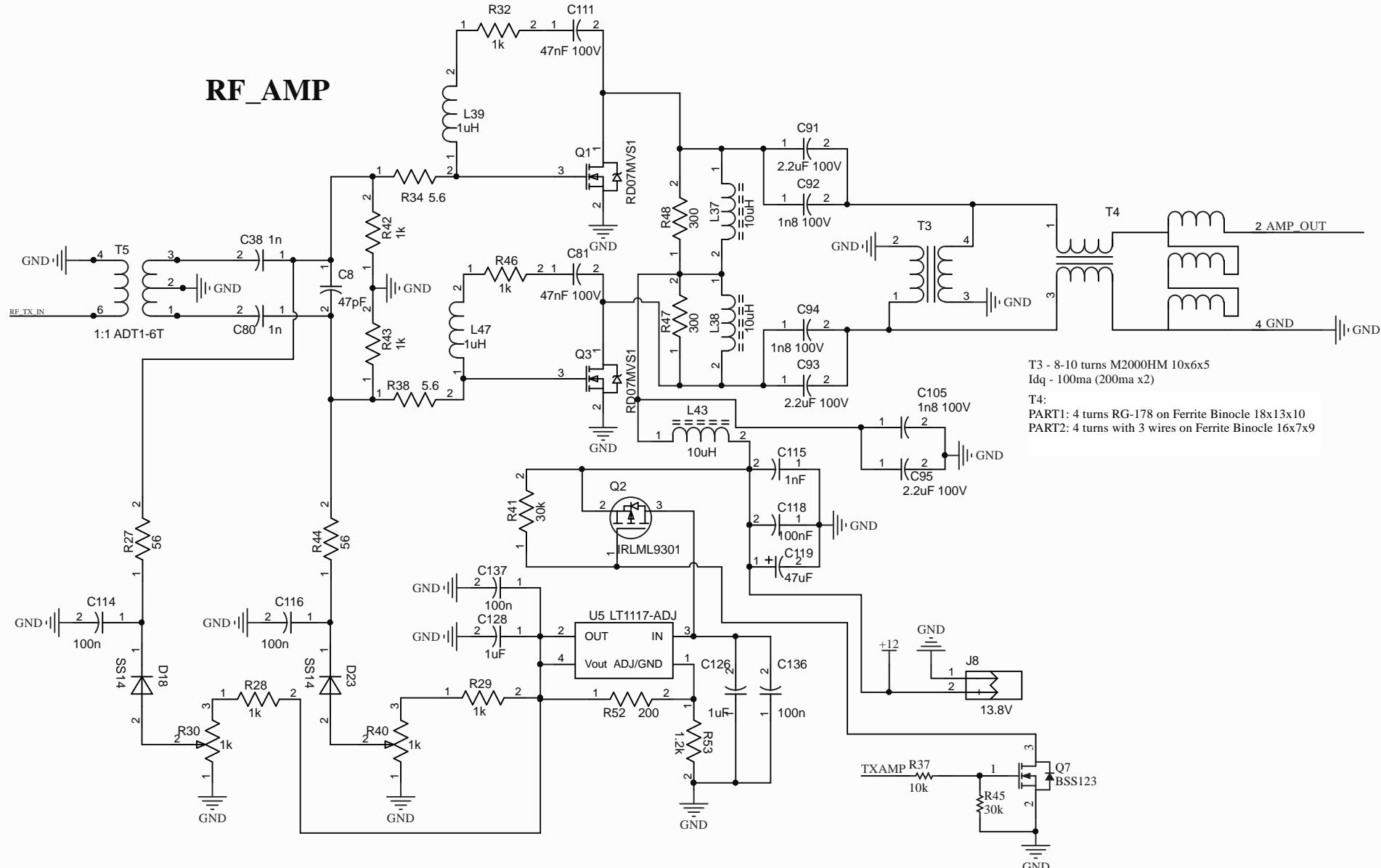
Title **SWR Tandem Match**

Size: A4 Number:18 Revision:2.0

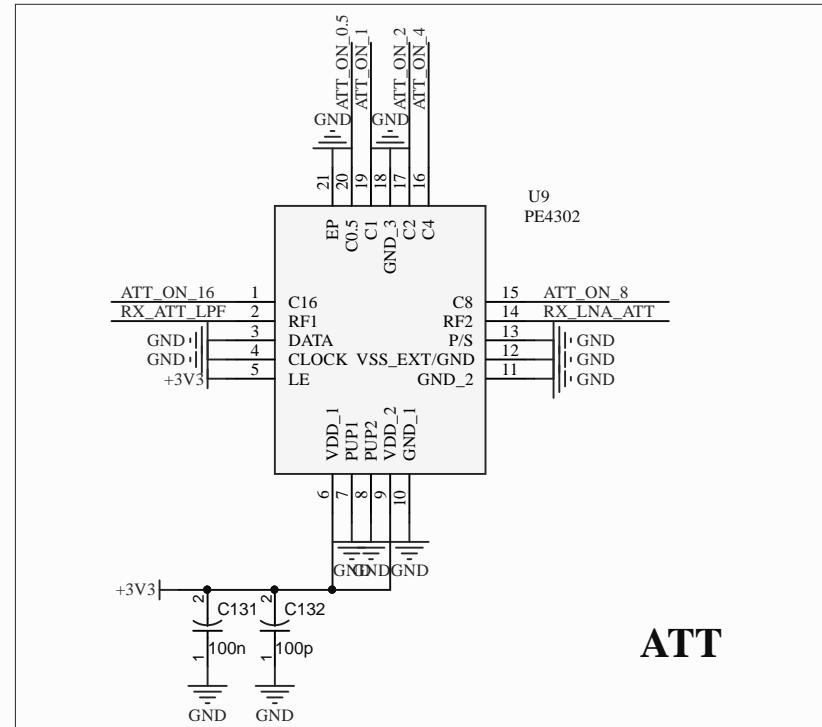
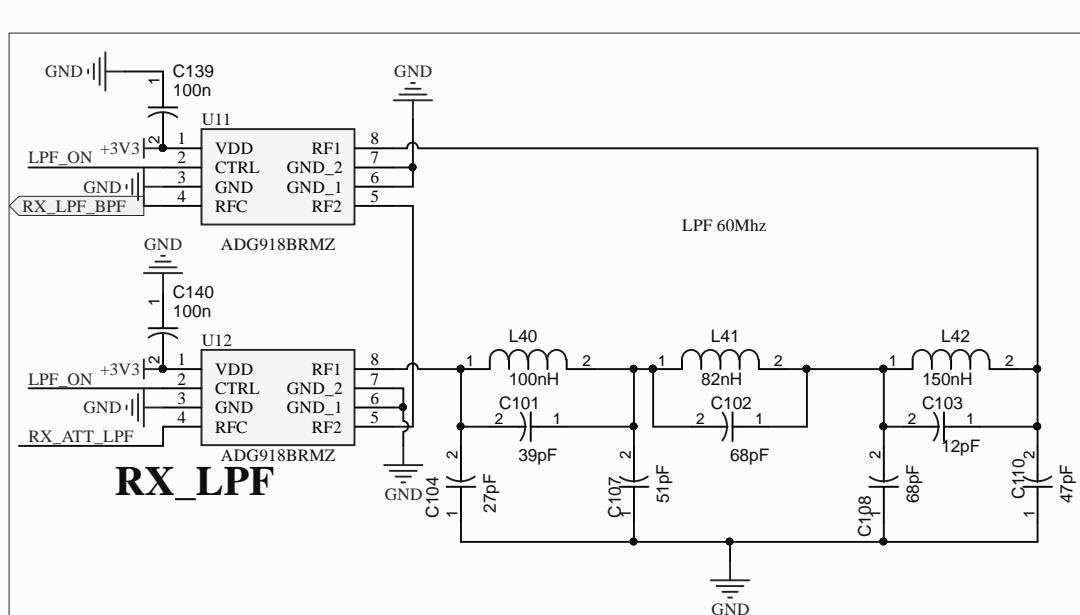
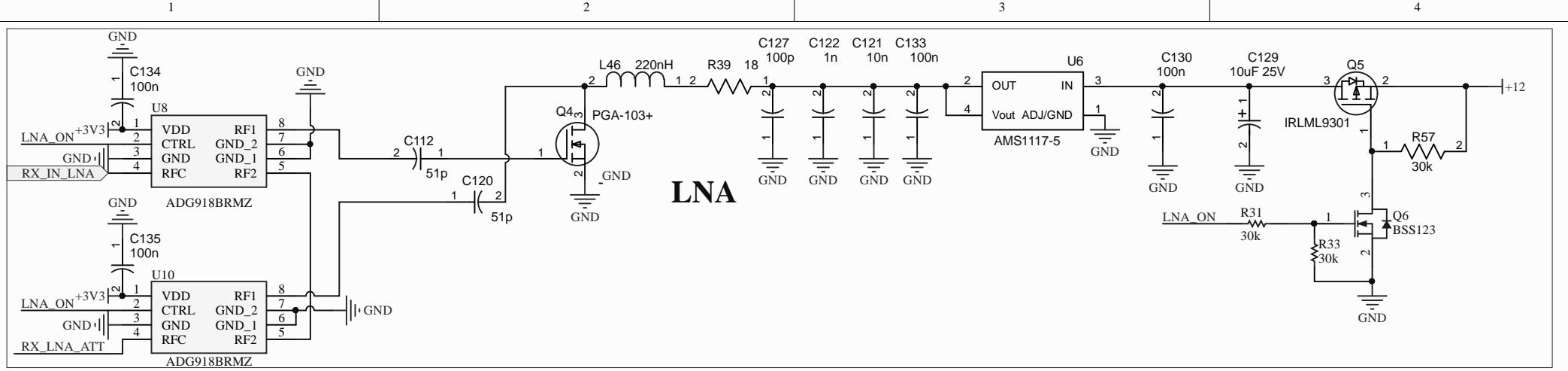
Date: 07.12.2020 Time: 23:21:31 Sheet:18 of 18

File: D:\Dropbox\Develop\Projects\WOLF\Schema\ALTIUM_DESIGNER\RF-UNIT\SWR Tandem Match.SchDoc

Altium



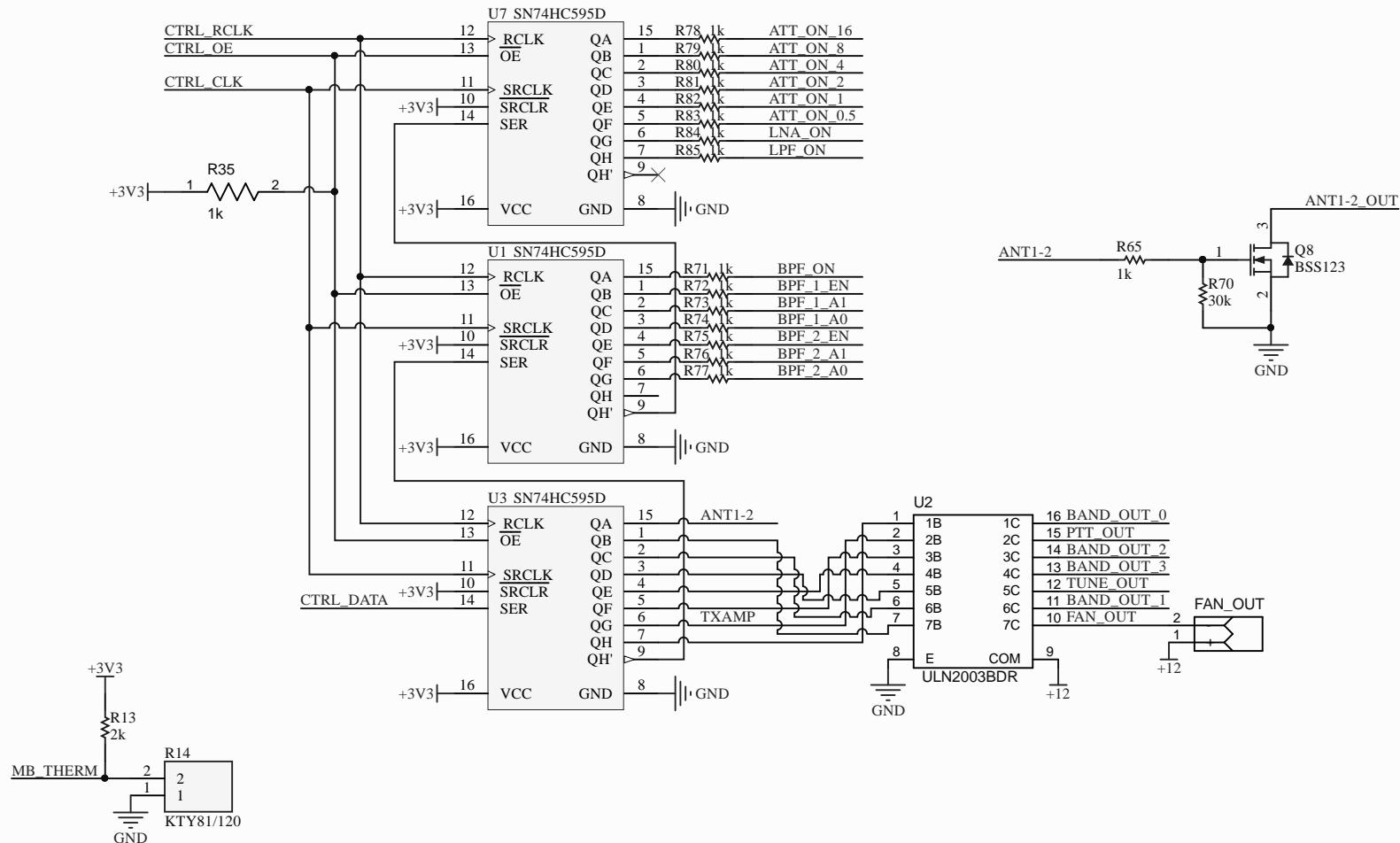
Title <i>RF_AMP</i>	*		
Size: A4	Number:17		*
Revision2.0			*
Date: 07.12.2020	Time: 23:21:32		Sheet17 of 18
File: D:\Dropbox\Develop\Projects\WOLF\Scheme\ALTUIM DESIGNER\RF-UNIT\RF_AMP.SchDoc			



Title LNA			*
Size: A4	Number:16	Revision2.0	*
Date: 07.12.2020	Time: 23:21:34	Sheet16 of 18	*
File: D:\Dropbox\Develop\Projects\WOLF\Schema\ALTIUM_DESIGNER\RF-UNIT\LNA.SchDoc			

Altium

A

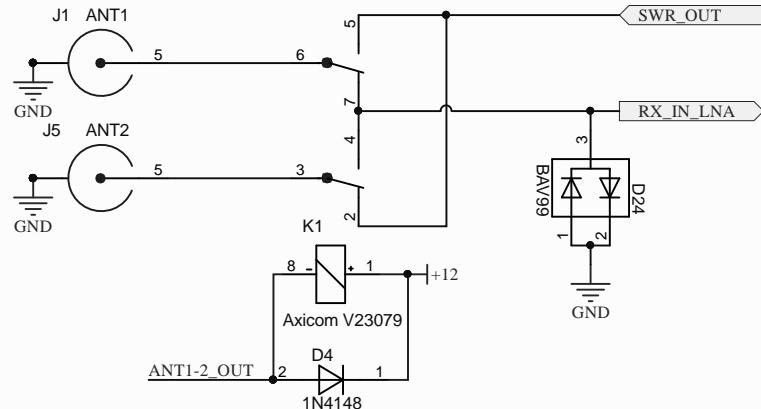
Title **CONTROL**

Size: A4	Number:15	Revision2.0
Date: 07.12.2020	Time: 23:21:36	Sheet15 of 18
File: D:\Dropbox\Develop\Projects\WOLF\Schema\ALTIUM_DESIGNER\RF-UNIT\CONTROL.SchDoc		*

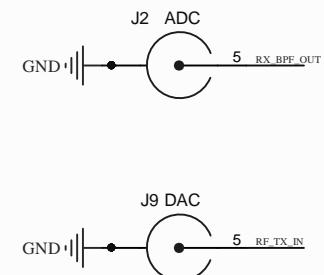
Altium

A

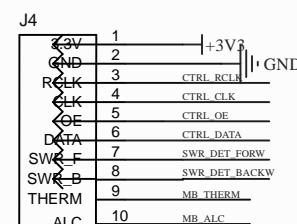
TXRX_COMUTATOR



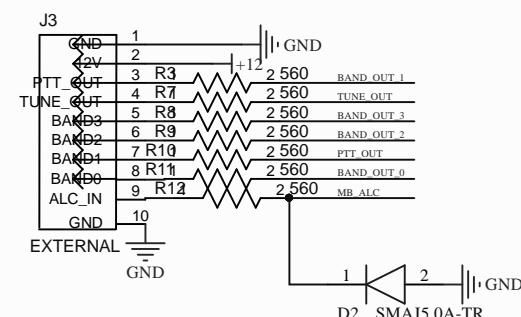
CONN



B



MOTHERBOARD



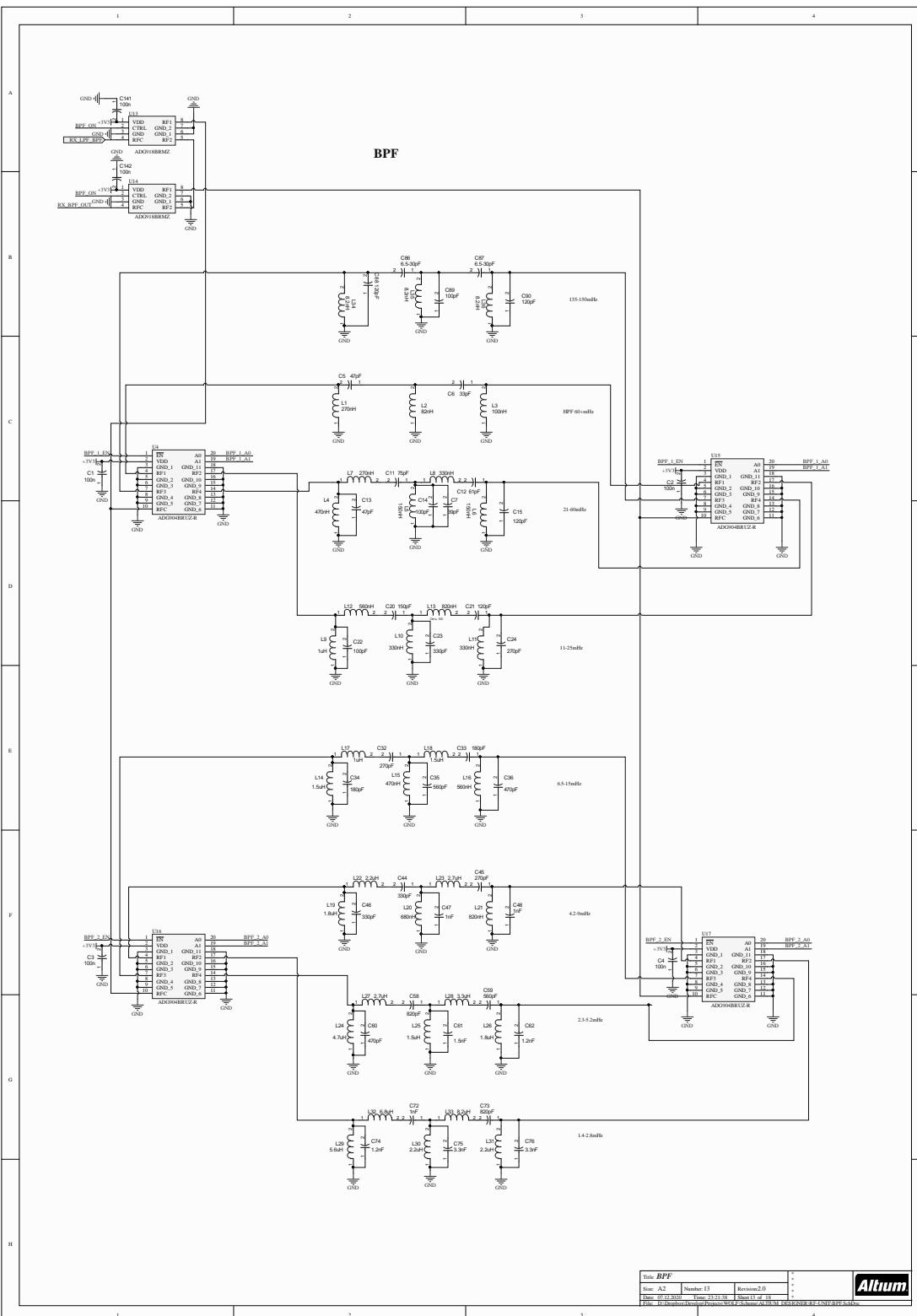
C

Title **CONN**

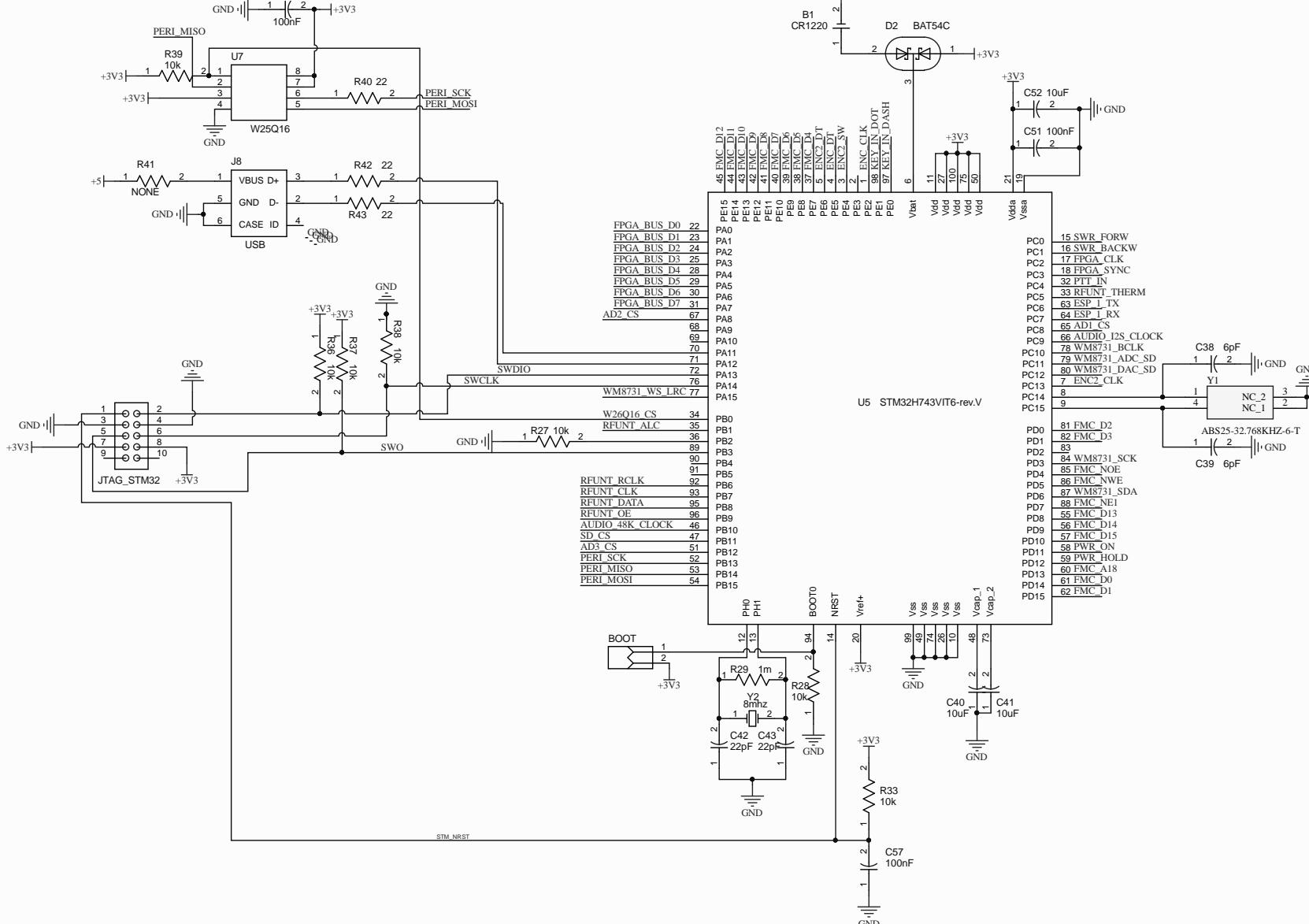
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Date: 07.12.2020 Time: 23:21:37 Sheet14 of 18

File: D:\Dropbox\Develop\Projects\WOLF\Scheme\ALTIUM_DESIGNER\RF-UNIT\CONN.SchDoc



STM32

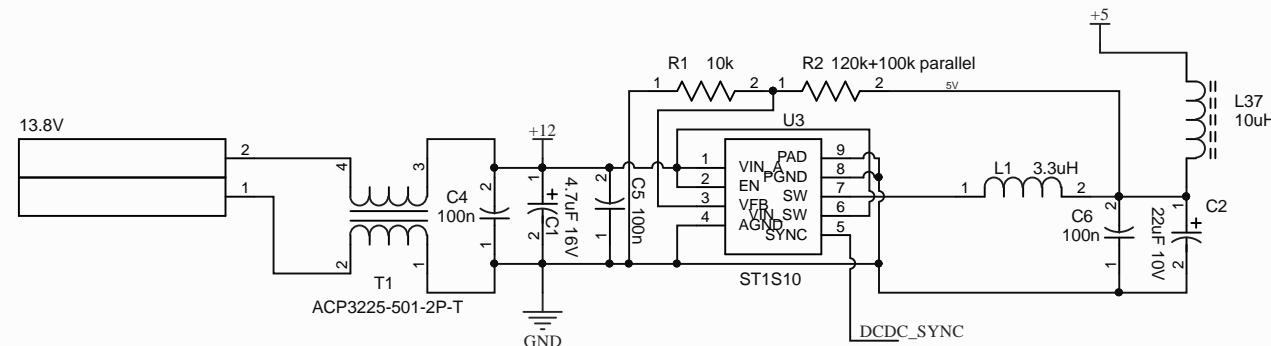


Title STM32

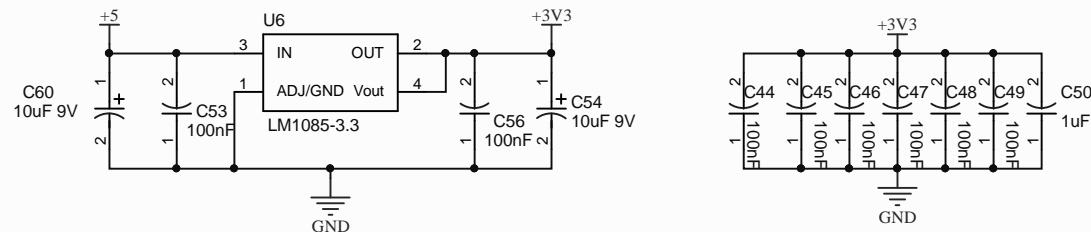
Size: A3	Number: 11	Revision 2.0
Date: 07.12.2020	Time: 23:21:40	Sheet 11 of 18
File: D:\Dropbox\Develop\Projects\WOLF\Scheme\ALTIUM_DB		

Altium

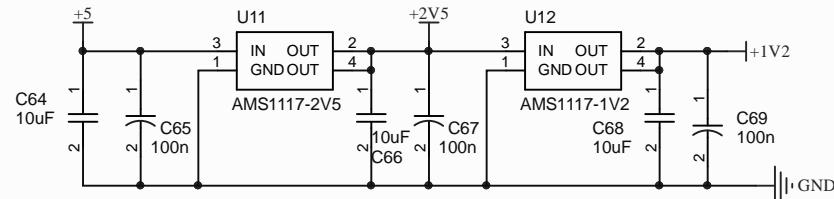
A



B



C

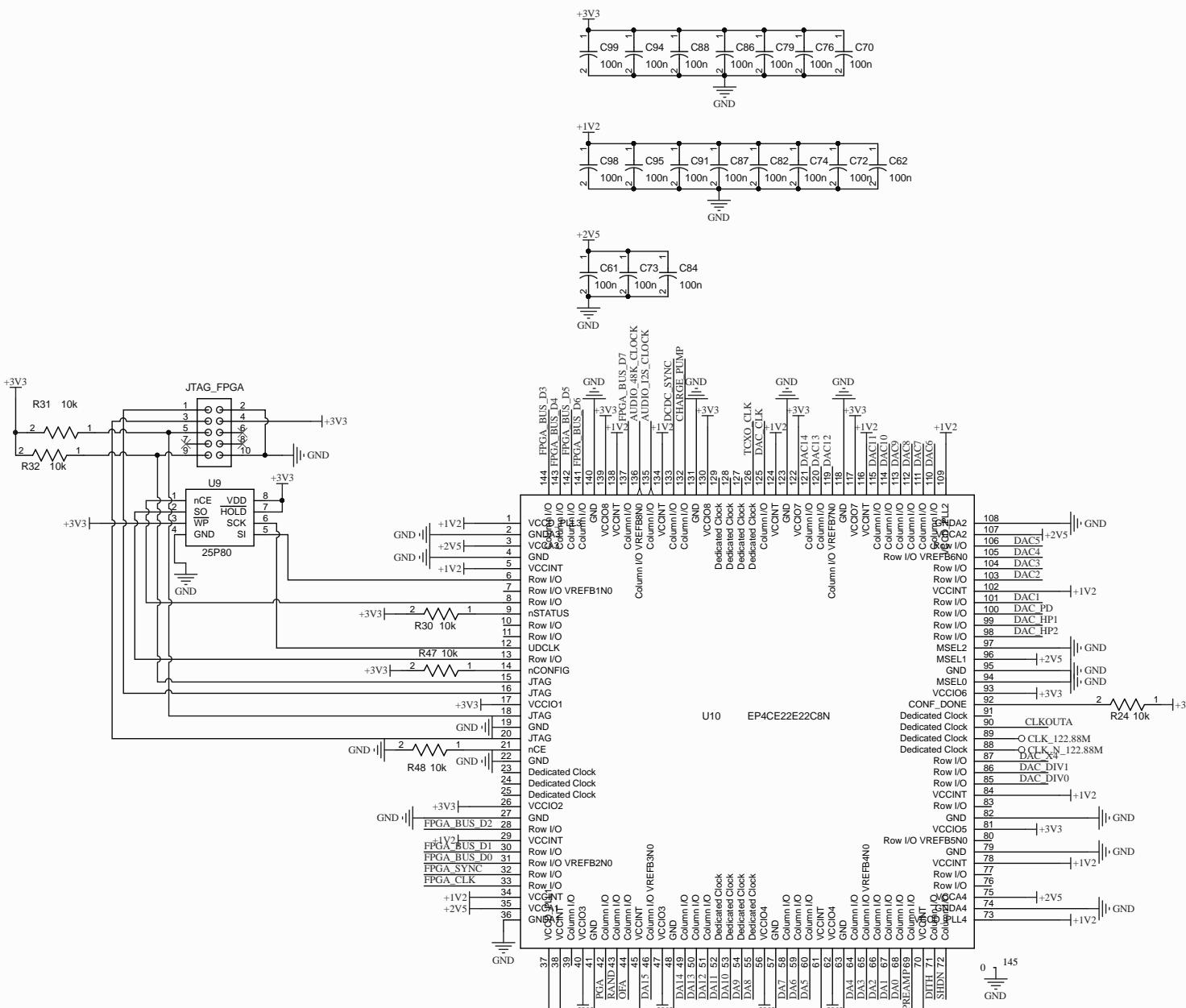
Title **POWER**

Size: A4 Number:10 Revision:2.0

Date: 07.12.2020 Time: 23:21:42 Sheet:10 of 18

File: D:\Dropbox\Develop\Projects\WOLF\Scheme\ALTIUM_DESIGNER\MOTHERBOARD\POWER.SchDoc

Altium



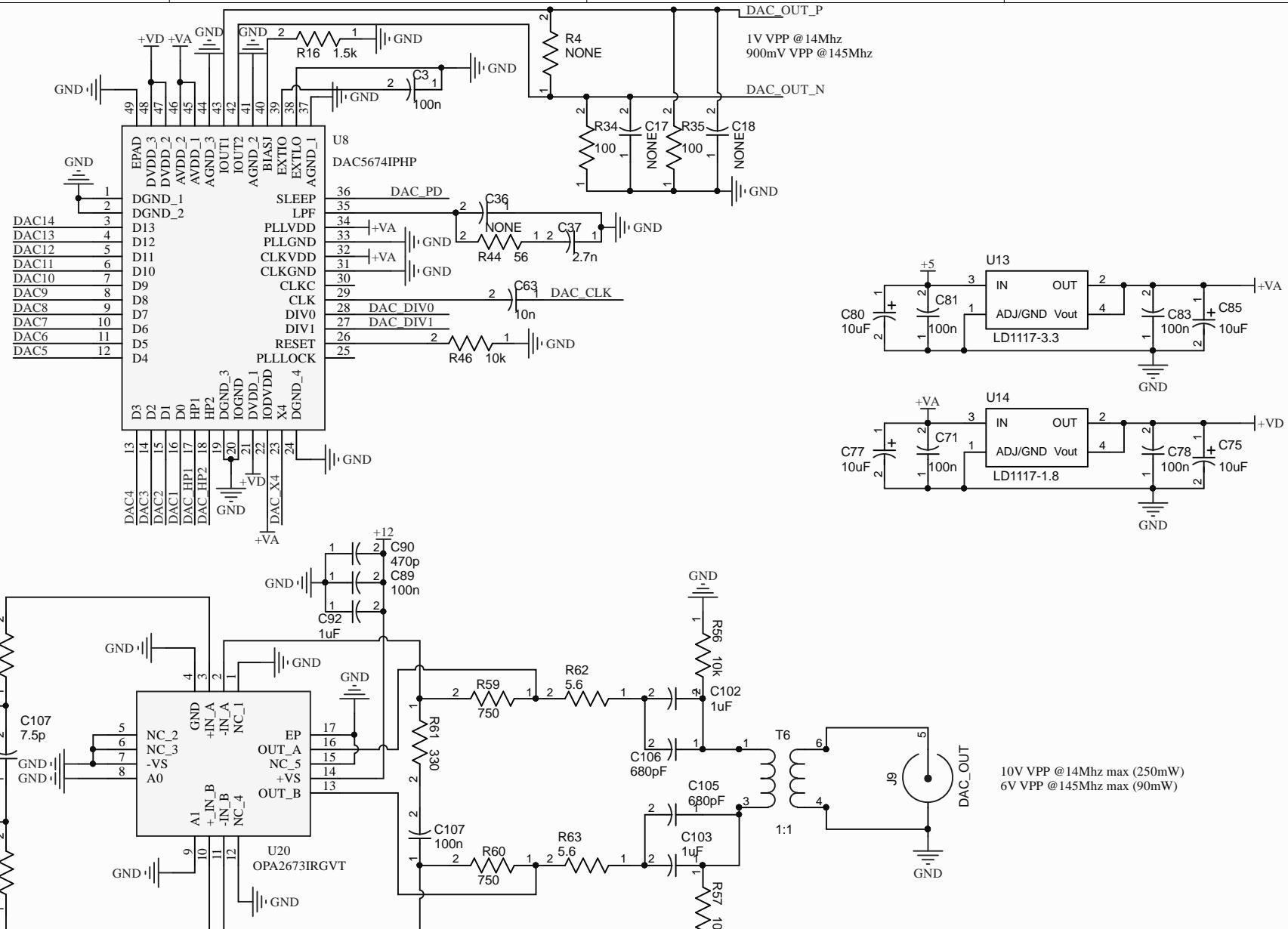
Title *FPGA*

Size: A3

Number:9
Time: 23:21:43

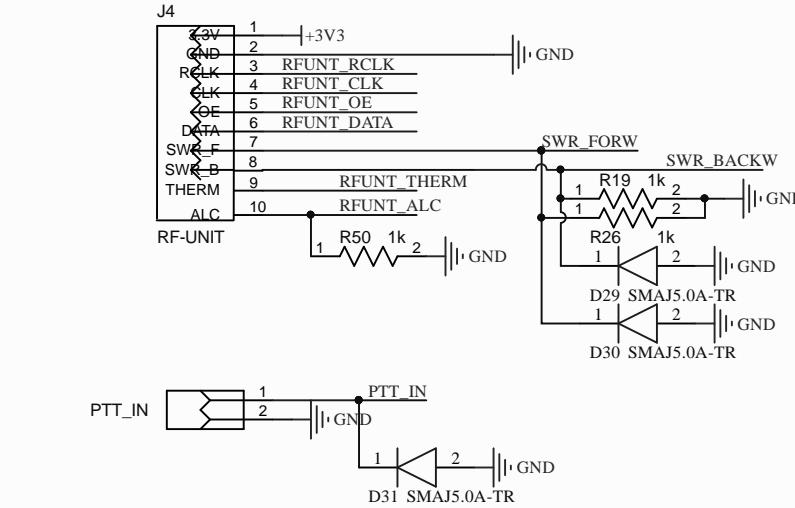
Revision 2.0
Sheet 9 of 18

Altium

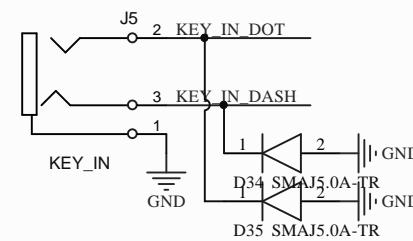


Title DAC			*	
			*	
Size: A4	Number:8	Revision:2.0	*	
Date: 07.12.2020	Time: 23:21:46	Sheet 8 of 18	*	
File: D:\Dropbox\Develon Projects\WOLF Scheme\ALTUIM DESIGNER\MOTHERBOARD\DAC.SchDoc				

A



B



C

J6

1	CS 3v3
2	FMC_A18
3	RS 3v3
4	WR GND
5	RD GND
6	STM_NRST
7	RSTMISO
8	FMC_D1
9	FMC_D2
10	FMC_D3
11	FMC_D4
12	FMC_D5
13	FMC_D6
14	FMC_D7
15	FMC_D8
16	FMC_D9
17	FMC_D10
18	FMC_D11
19	FMC_D12
20	FMC_D13
21	FMC_D14
22	PWR_ON
23	PWR_HOLD
24	+3V3
25	+3V3
26	GND
27	PERI_MOSI
28	PERI_MOSI
29	ESP_1_TX
30	ESP_1_RX
31	DBWRTX
32	DB2WTX
33	DB3CLK
34	DB\$DCS
35	SD_CS
36	AD1_CS
37	AD2_CS
38	DBAD2C
39	DB7_E2A
40	DB8_E2B
41	DB9_E2S
42	DB10E1A
43	DB11E1B
44	DBAD3C
45	DB13_5v
46	DB14GND
47	DB15GND

FPC-45P-0.5mm

D

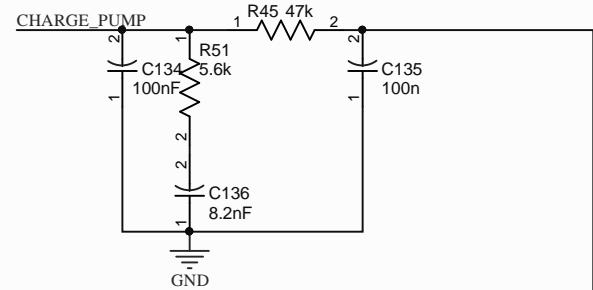
D

Title **CONNECTIONS**

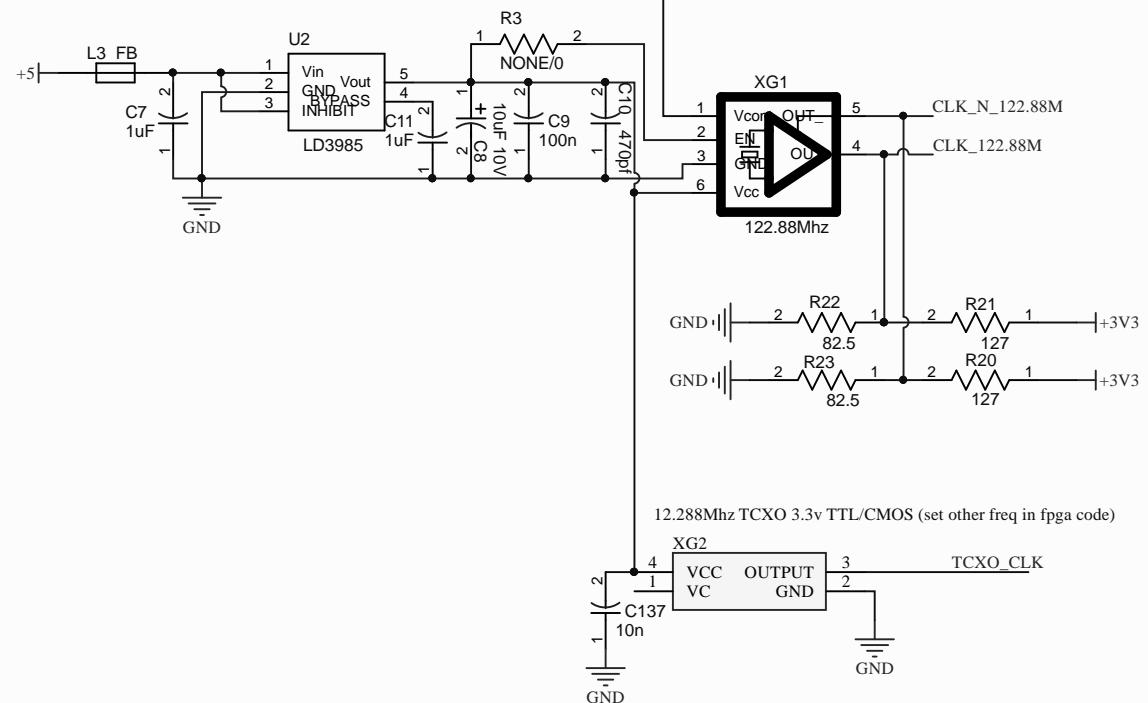
Size: A4	Number:7	Revision2.0	*
Date: 07.12.2020	Time: 23:21:48	Sheet7 of 18	*
File: D:\Dropbox\Develop\Projects\WOLF\Scheme\ALTIUM_DESIGNER\MOTHERBOARD\CONNECTIONS.SchDoc			

Altium

A



B



C

D

Title **CLOCK_GENERATOR**

Size: A4 Number:6 Revision 2.0

Date: 07.12.2020 Time: 23:21:49 Sheet 6 of 18

File: D:\Dropbox\Develop\Projects\WOLF\Schema\ALTIUM_DESIGNER\MOTHERBOARD\CLOCK_GENERATOR.SchDoc

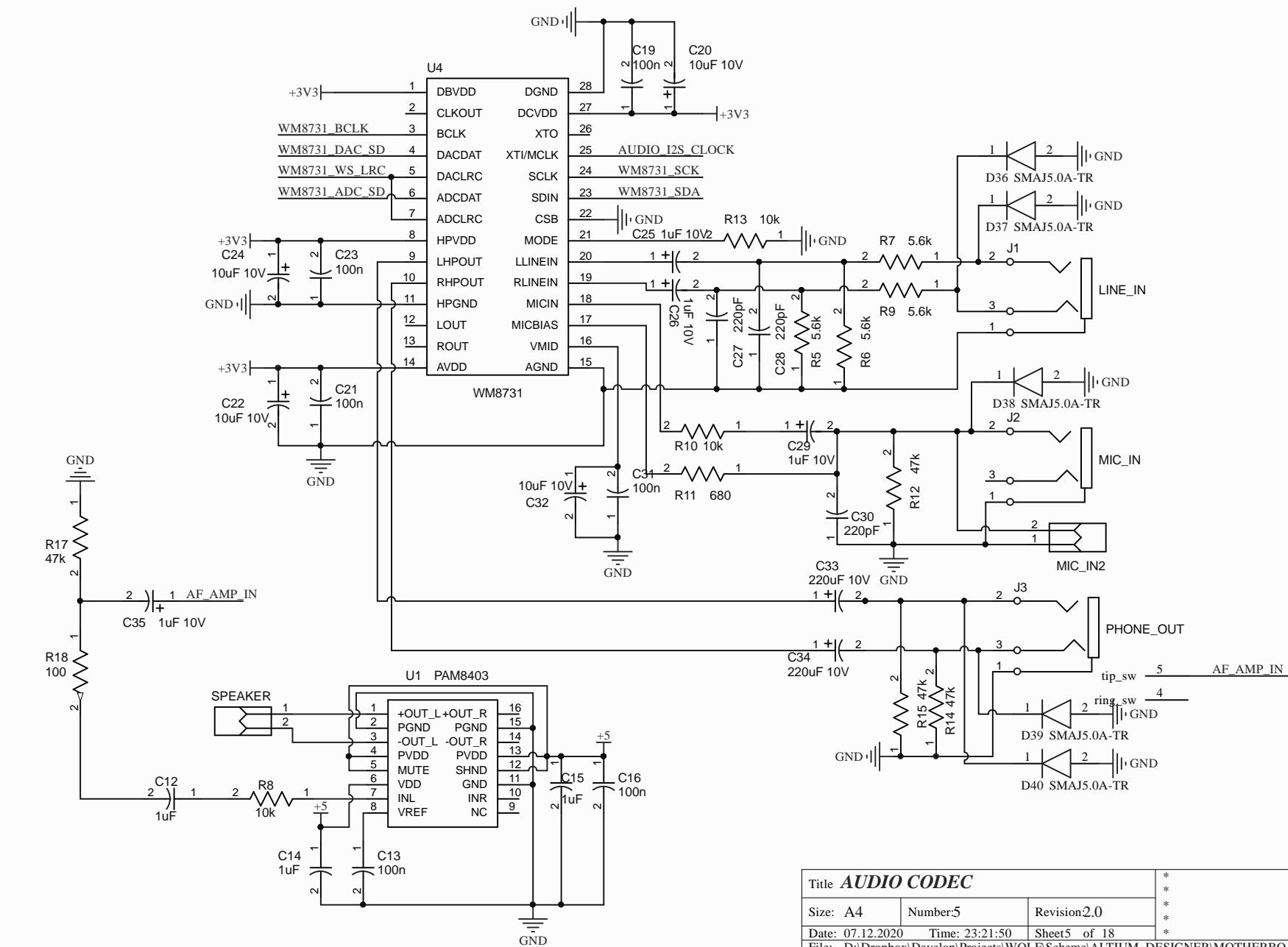
Altium

A

B

C

D

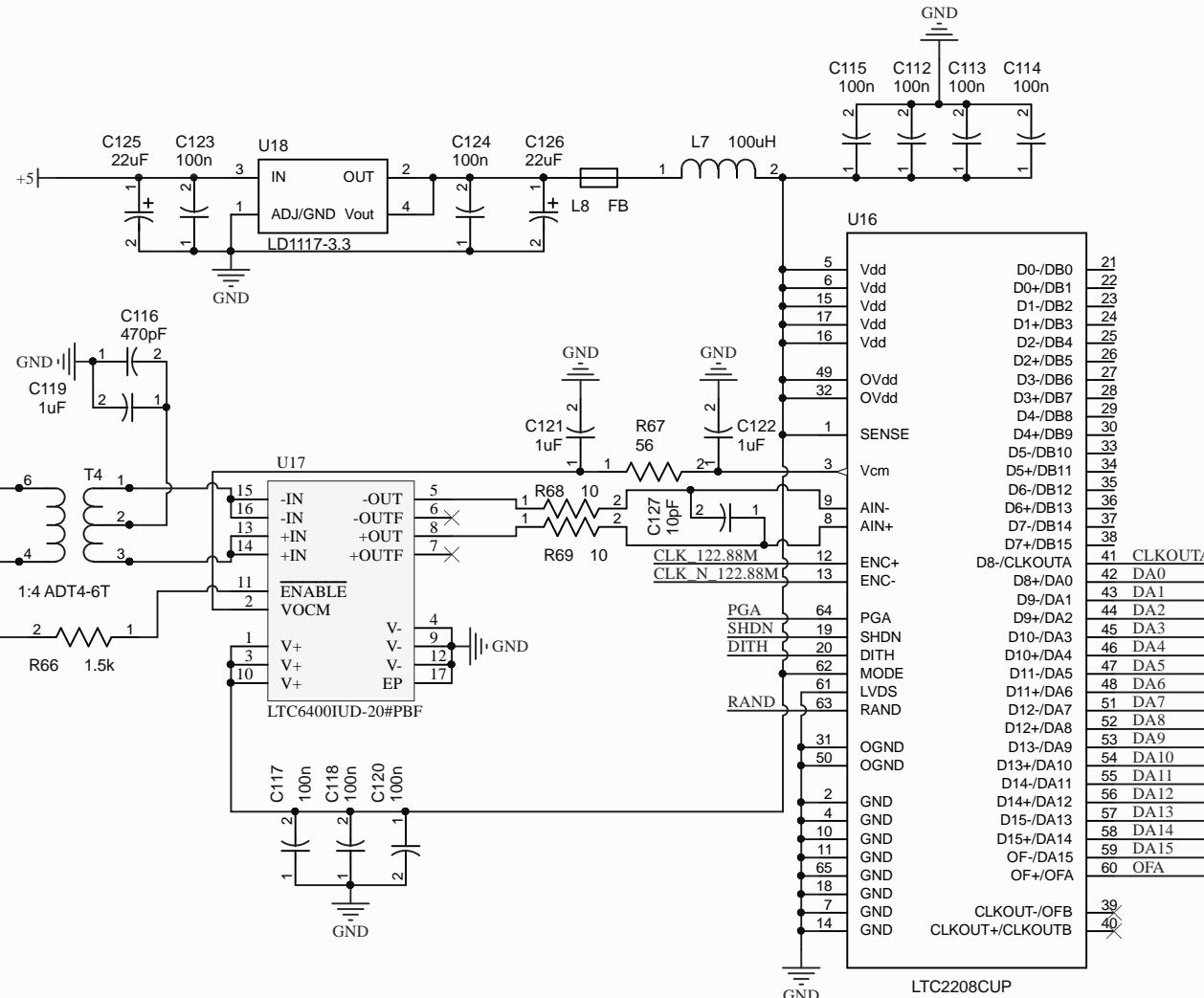
Title **AUDIO CODEC**

Size: A4 Number:5 Revision2.0

Date: 07.12.2020 Time: 23:21:50 Sheet5 of 18

File: D:\Dropbox\Develop\Projects\WOLF\Schema\ALTIUM_DESIGNER\MOTHERBOARD\AUDIO_CODEC.SchDoc

Altium

Title **ADC**

Size: A4 | Number:3 | Revision 2.0

Date: 07.12.2020 Time: 23:21:53 Sheet 3 of 18

File: D:\Dropbox\Develop\Projects\WOLF\Scheme\ALTIUM_DESIGNER\MOTHERBOARD\ADC.SchDoc

Altium