

A

U_POWER
POWER.SchDoc

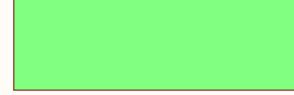


U_CLOCK_GENERATOR
CLOCK_GENERATOR.SchDoc

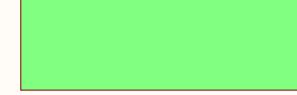


B

U_CONNECTIONS
CONNECTIONS.SchDoc



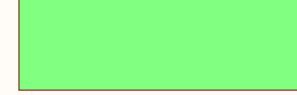
U_FPGA
FPGA.SchDoc



U_STM32
STM32.SchDoc



U_AUDIO_CODEC
AUDIO_CODEC.SchDoc



A

B

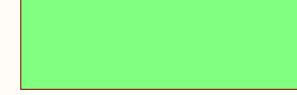
C

D

U_DAC
DAC.SchDoc



U_ADC
ADC.SchDoc



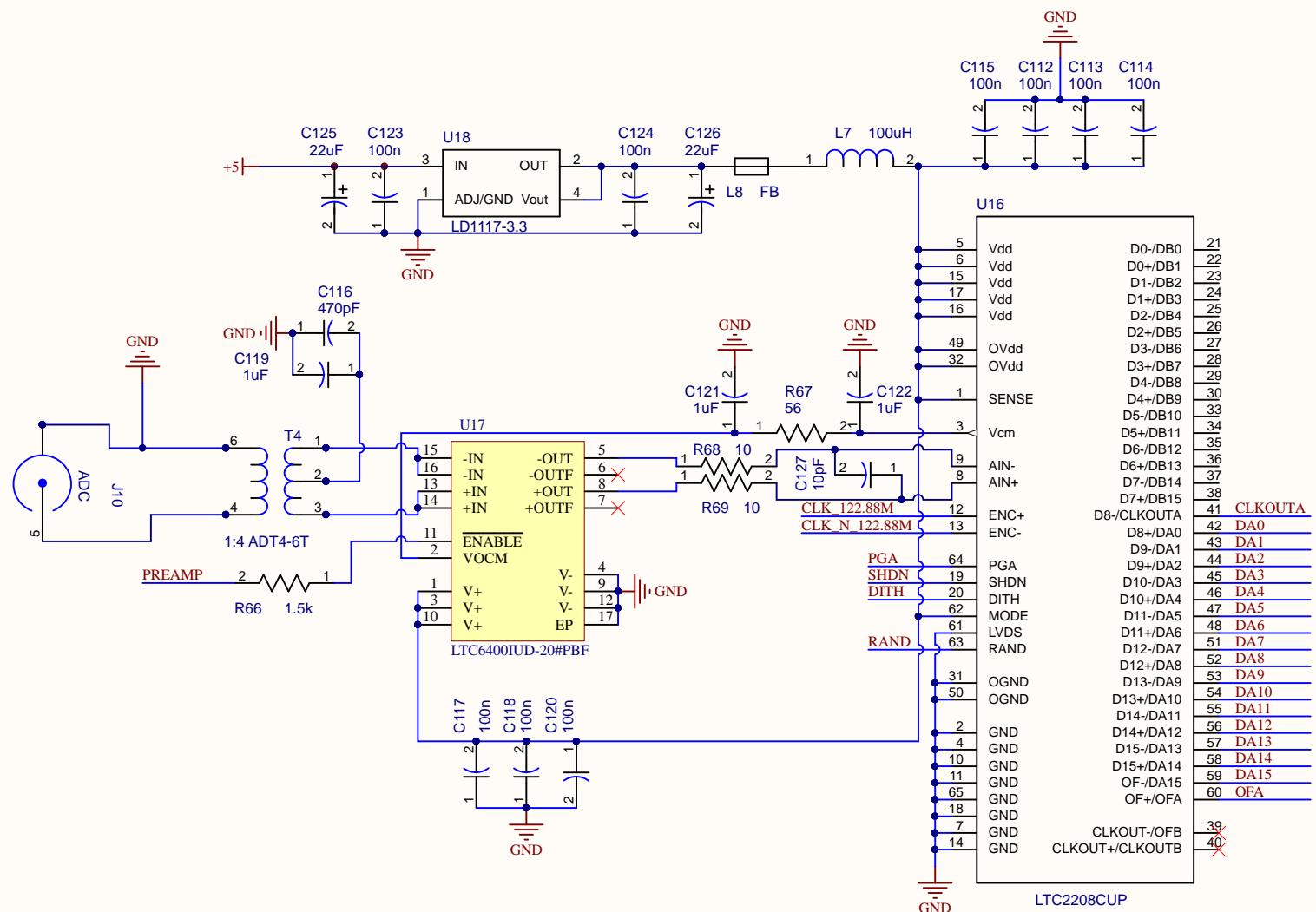
Title **MOTHERBOARD**

Size: A4	Number:2	Revision:1.9
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Date: 01.10.2020	Time: 0:16:39	Sheet 2 of 18
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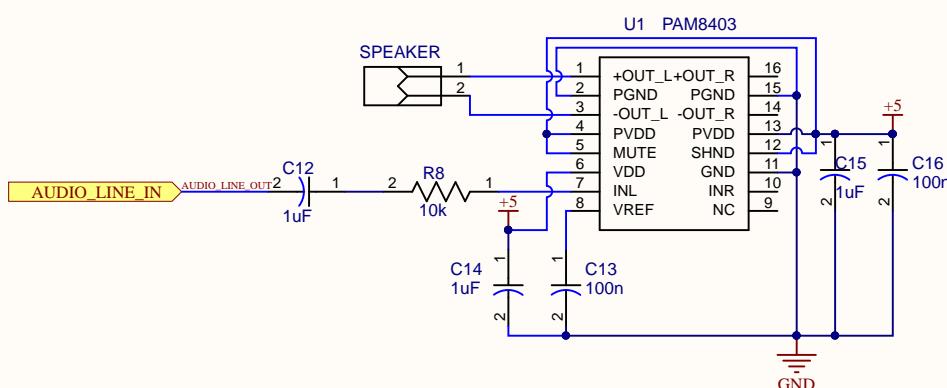
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Title **ADC** *
 Size: A4 Number:3 Revision:1.9 *
 Date: 01.10.2020 Time: 0:16:39 Sheet 3 of 18 *
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Title ***AF AMP***

Size: A4 Number:4 Revision:1.9

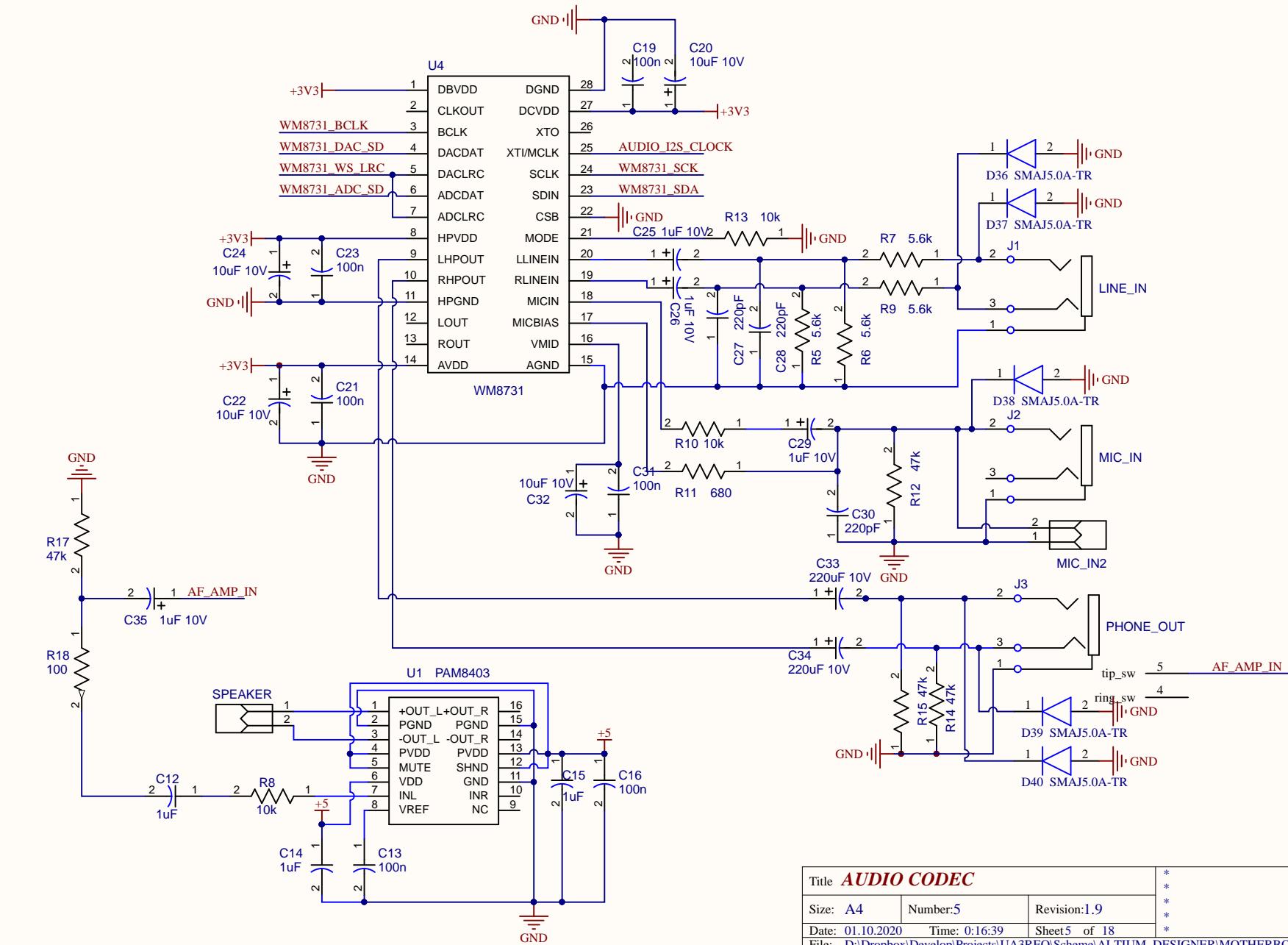
Date: 01.10.2020 Time: 0:16:39 Sheet 4 of 18

File: D:\Dropbox\Develop\Projects\UA3REO\Scheme\ALTIUM_DESIGNER\MOTHERBOARD\AF AMP.SchDoc

*
UA3REO
BH8CGJ
*

Altium

A

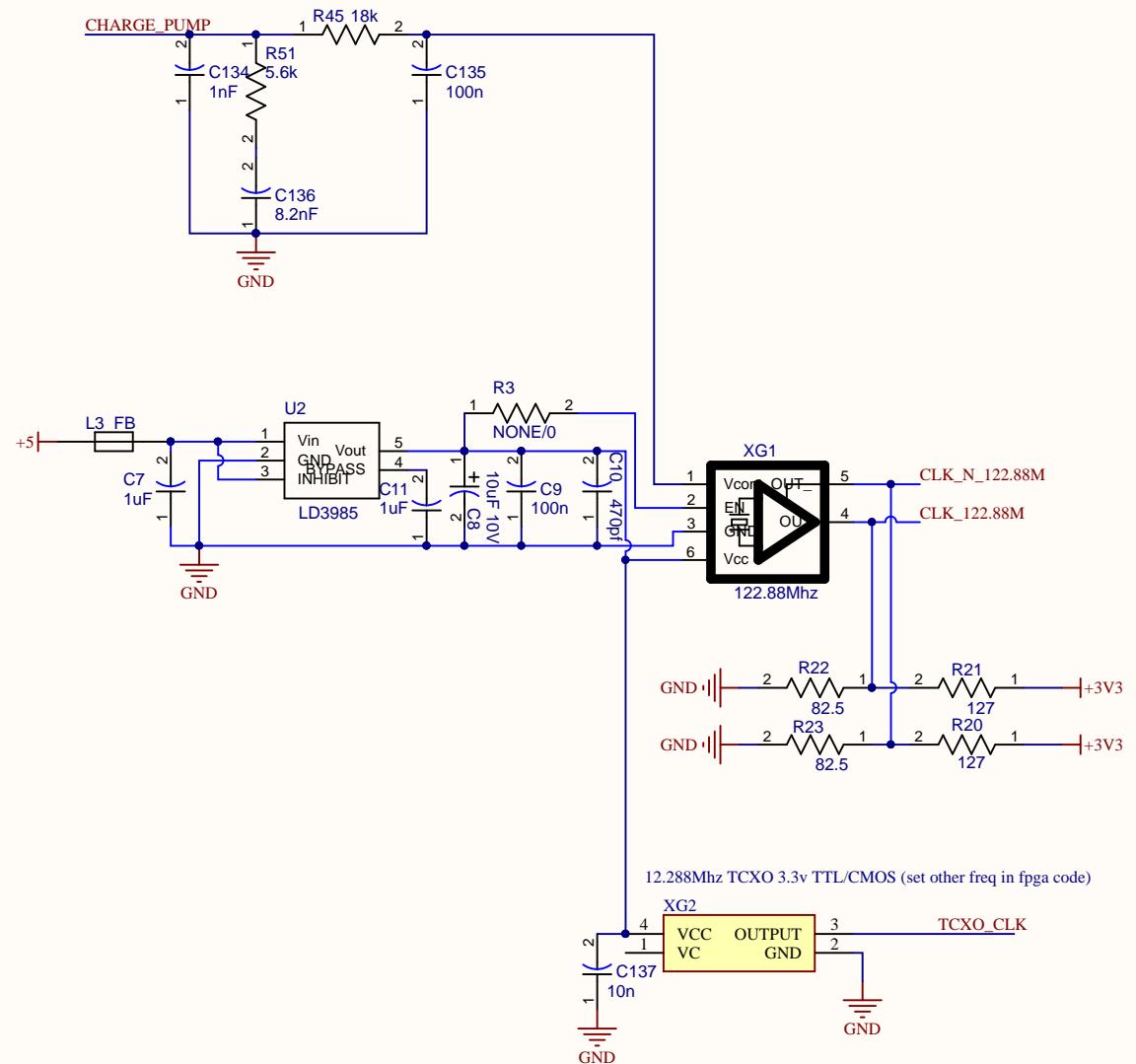
Title **AUDIO CODEC**

Size: A4 Number:5 Revision:1.9

Date: 01.10.2020 Time: 0:16:39 Sheet 5 of 18

File: D:\Dropbox\Develop\Projects\UA3REO\Scheme\ALTIUM_DESIGNER\MOTHERBOARD\AUDIO CODEC.SchDoc

Altium



Title	CLOCK GENERATOR	
Size:	A4	Number:6
Date:	01.10.2020	Time: 0:16:39
File:	D:\Dropbox\Developer\Projects\UAR3RF	

Altium

A

B

C

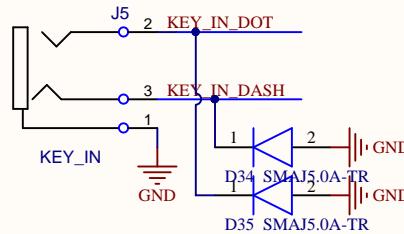
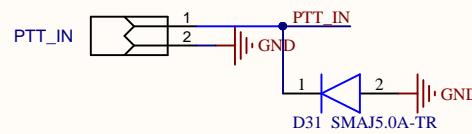
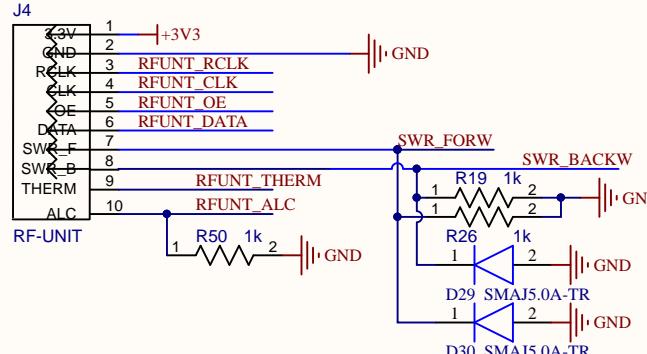
D

A

B

C

D



J6

FMC_NE1	1	CS 3v3
FMC_A18	2	RS 3v3
FMC_NWE	3	WR GND
FMC_NOE	4	RD GND
STM_NRST	5	RSTMISO
FMC_D0	6	PERI_MOSI
FMC_D1	7	DB0MOSI
FMC_D2	8	DB1WRX
FMC_D3	9	DB2WTX
FMC_D4	10	DB3CLK
FMC_D5	11	DB4DCS
FMC_D6	12	DB5AD1C
FMC_D7	13	DB6AD2C
FMC_D8	14	DB7E2A
FMC_D9	15	DB8E2B
FMC_D10	16	DB9E2S
FMC_D11	17	DB1E1A
FMC_D12	18	DB1E1B
FMC_D13	19	DBAD3C
FMC_D14	20	DB135v
FMC_D15	21	DB1GND
PWR_ON	22	DB16GND
PWR_HOLD	23	PONCAS
	24	PHOCAS
		3v3

FPC-45P-0.5mm

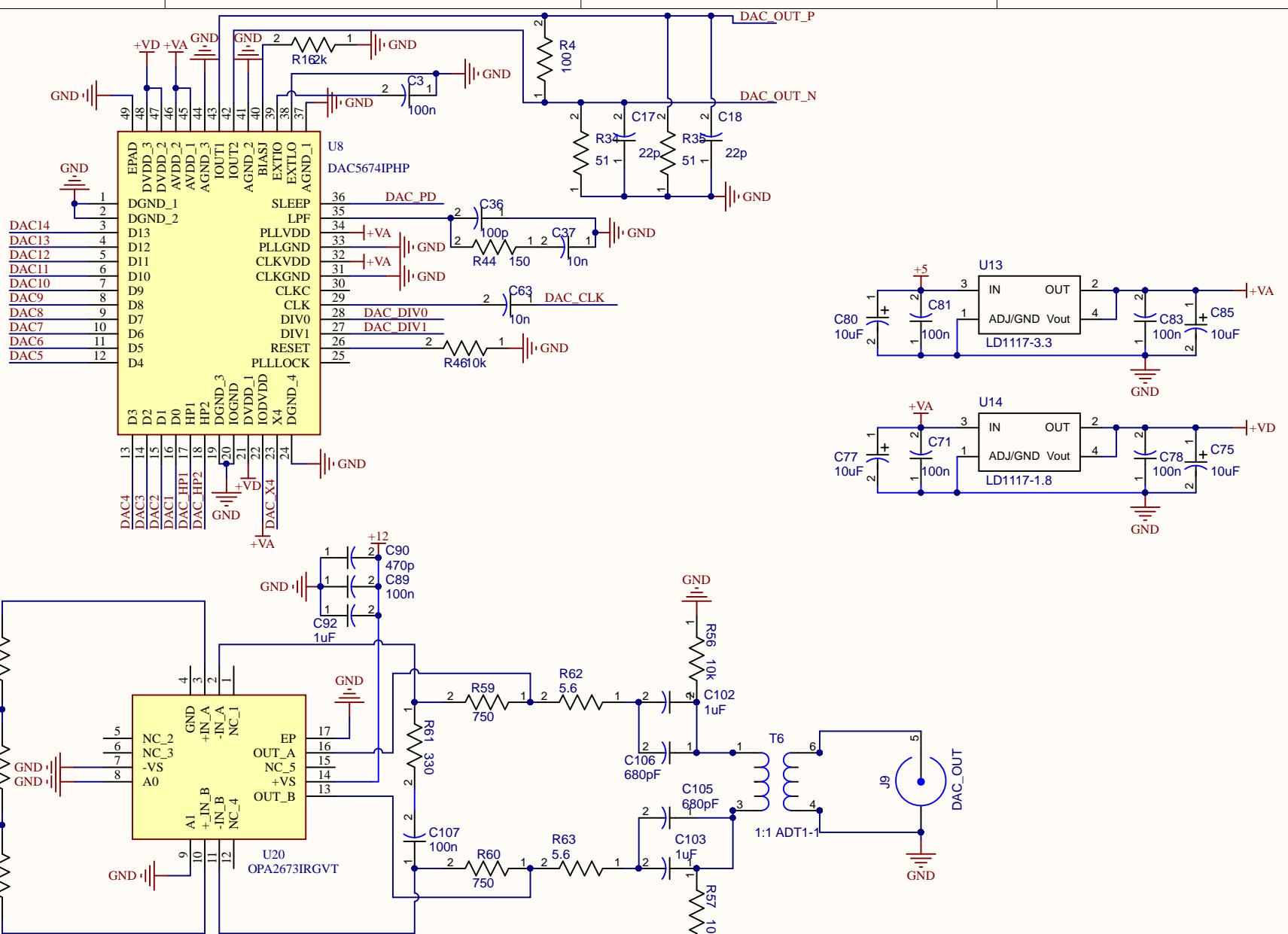
Title CONNECTIONS

Size: A4 Number: 7 Revision: 1.9

Date: 01.10.2020 Time: 0:16:39 Sheet 7 of 18

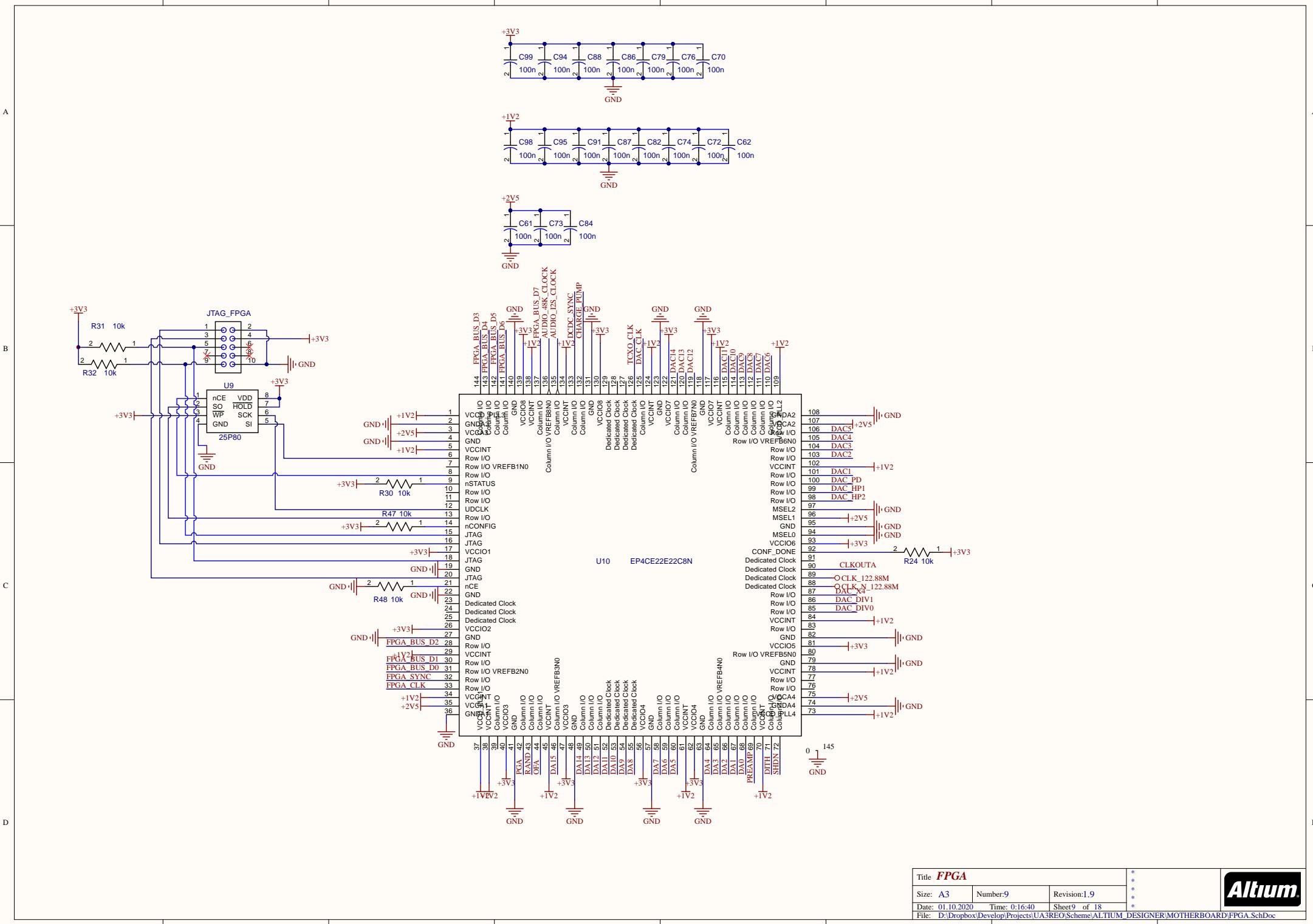
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Altium



Title DAC		
Size: A4	Number: 8	Revision: 1.9
Date: 01.10.2020	Time: 0:16:40	Sheet 8 of 18
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Altium

**Title *FPGA***

Size: A3

Number:9

Revision:1.9

Date: 01.10.2020

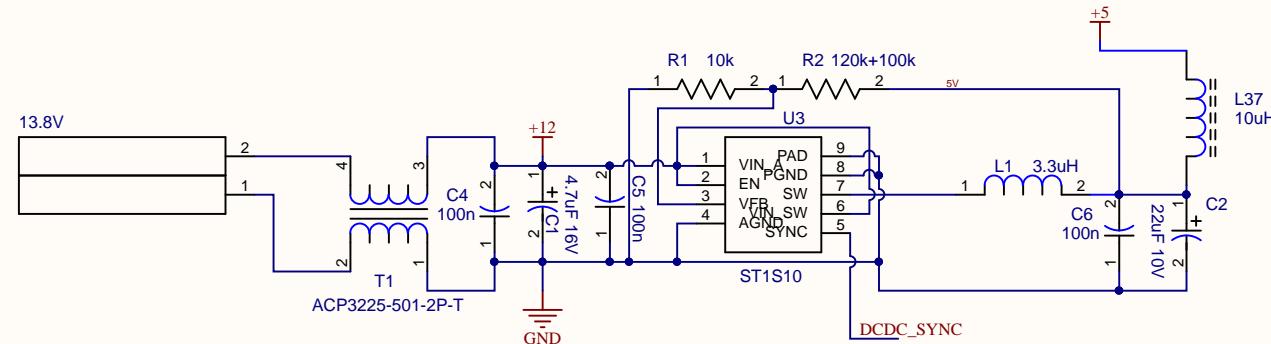
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Sheet9 of 18

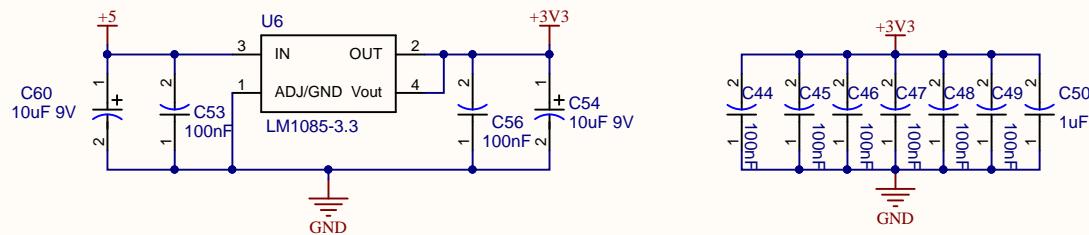
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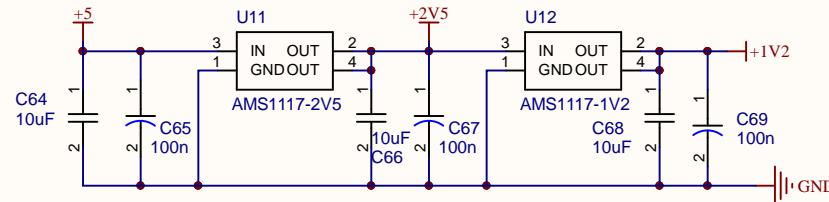
A



B



C

Title **POWER**

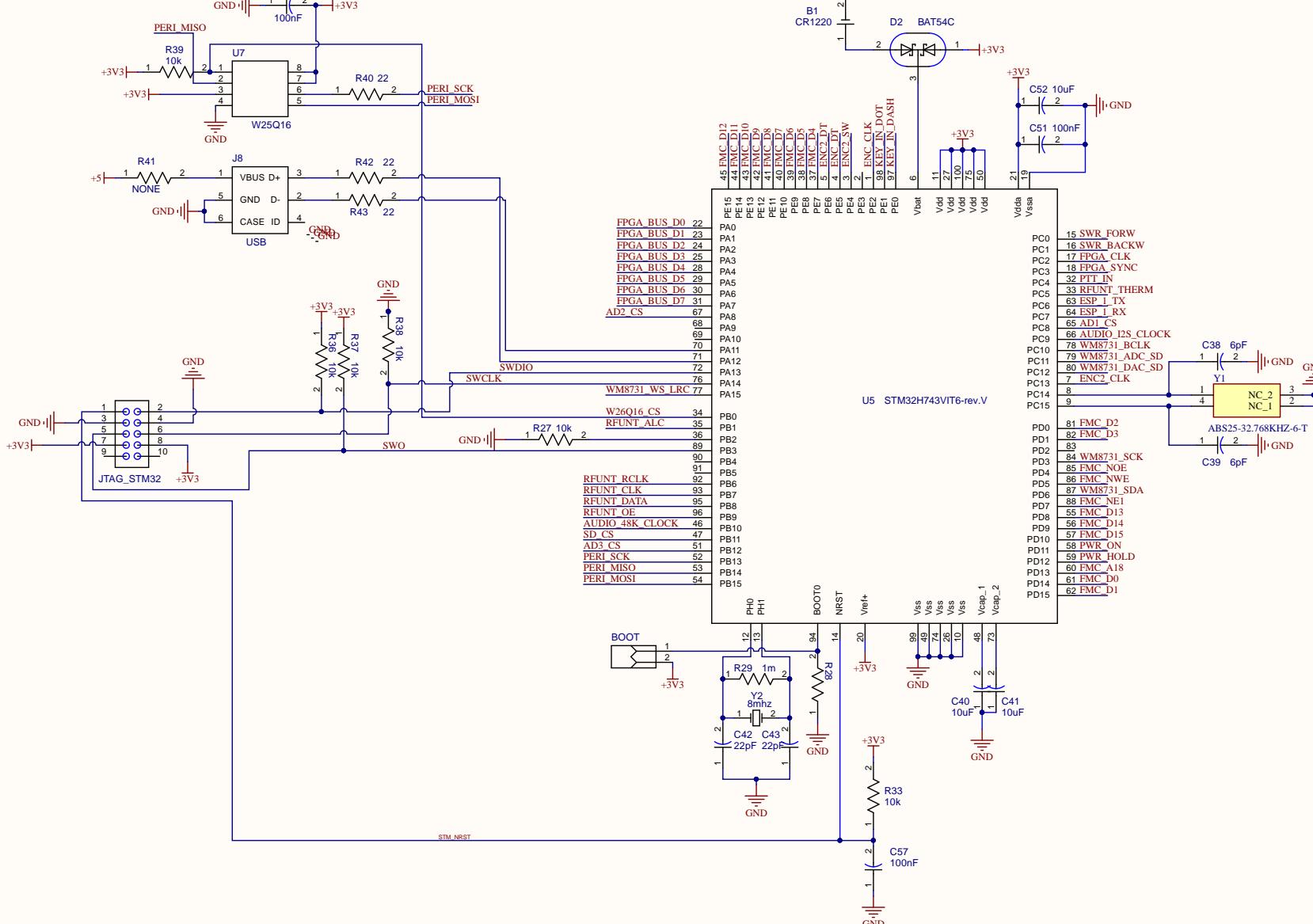
Size: A4 Number:10 Revision:1.9

Date: 01.10.2020 Time: 0:16:40 Sheet 10 of 18

File: D:\Dropbox\Develop\Projects\UA3REO\Scheme\ALTIUM_DESIGNER\MOTHERBOARD\POWER.SchDoc

Altium

STM32

Title **STM32**

Size: A3	Number:11	Revision:1.9
Date: 01.10.2020	Time: 0:16:40	Sheet 11 of 18
File: D:\Dropbox\Develop\Projects\UA3REO\Scheme\ALTIUM DESIGNER\MOTHERBOARD\STM32.SchDoc		



A

A

B

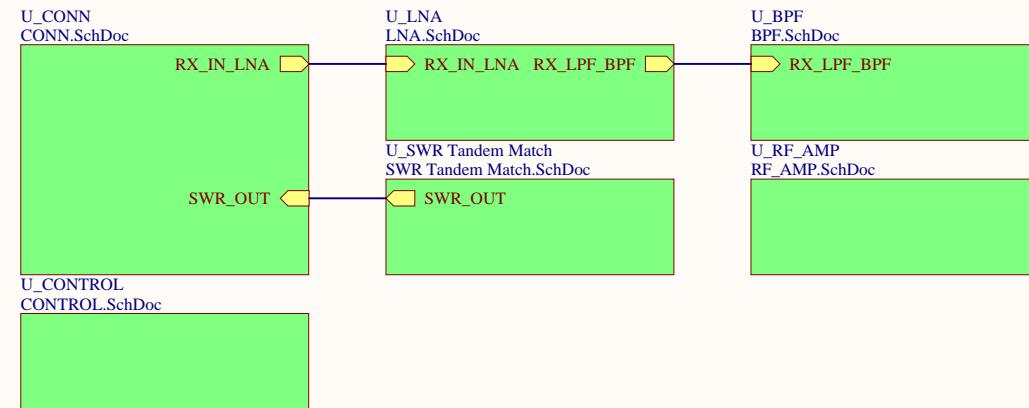
B

C

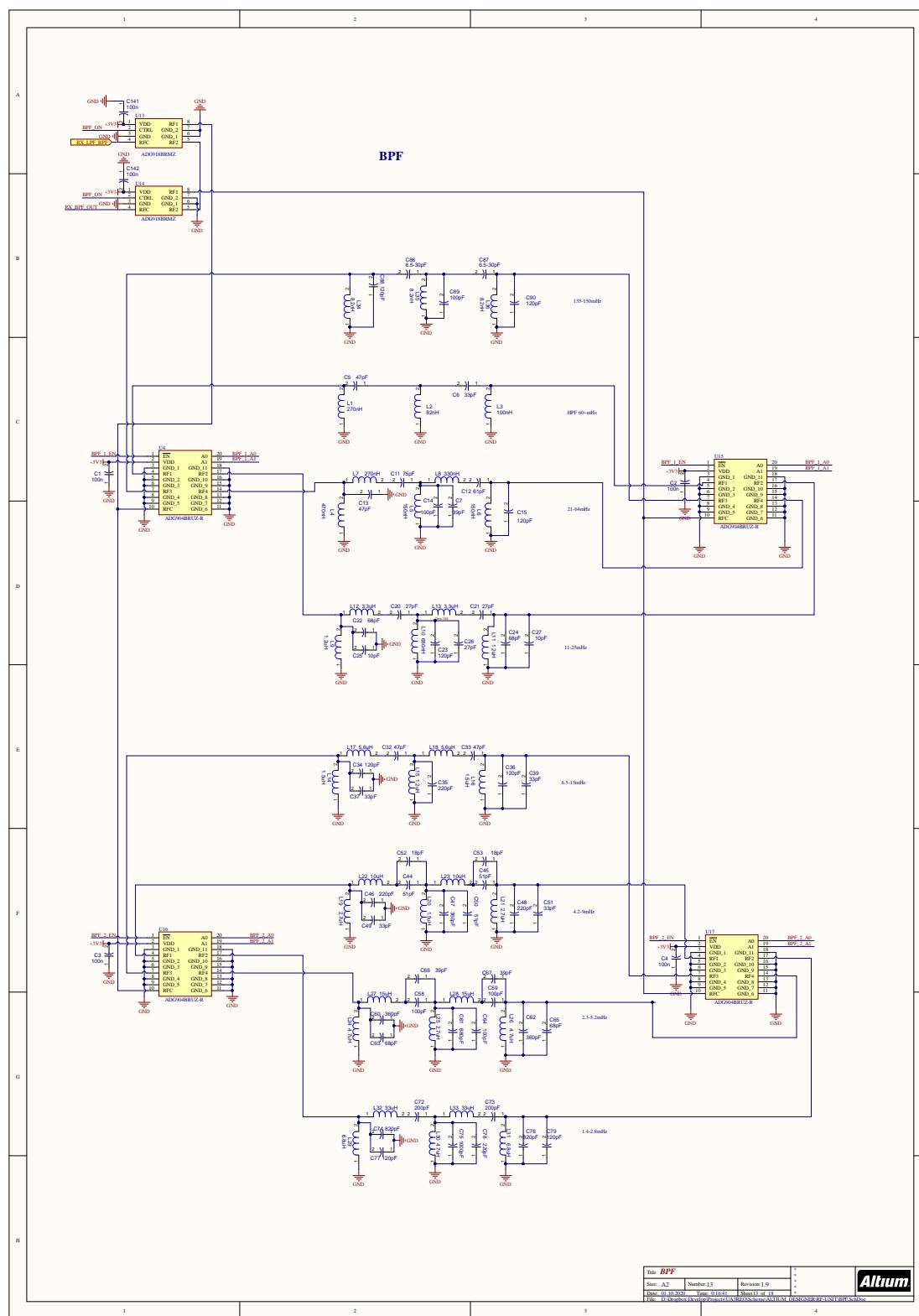
C

D

D

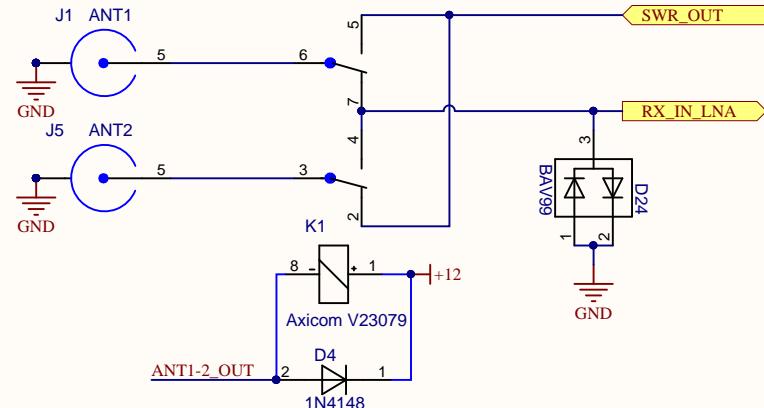


Title RF-UNIT			*
Size: A4	Number:12	Revision:1.9	*
Date: 01.10.2020	Time: 0:16:41	Sheet 12 of 18	*
File: D:\Dropbox\Develop\Projects\UA3REO\Scheme\ALTIUM_DESIGNER\RF-UNIT\RF-UNIT.SCHDOC			Altium®

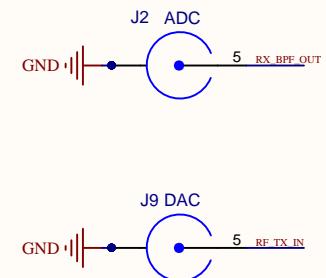


A

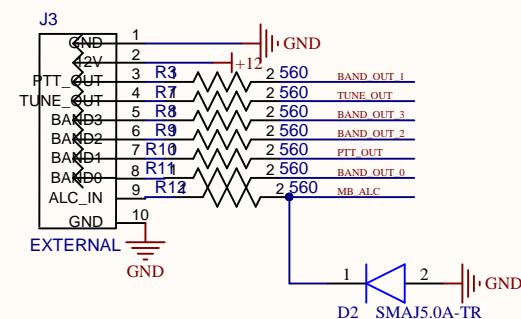
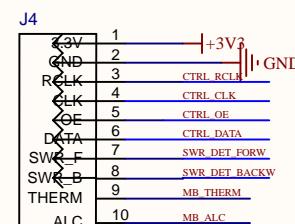
TXRX_COMUTATOR



CONN



B



C

Title **CONN**

Size: A4 Number:14 Revision:1.9

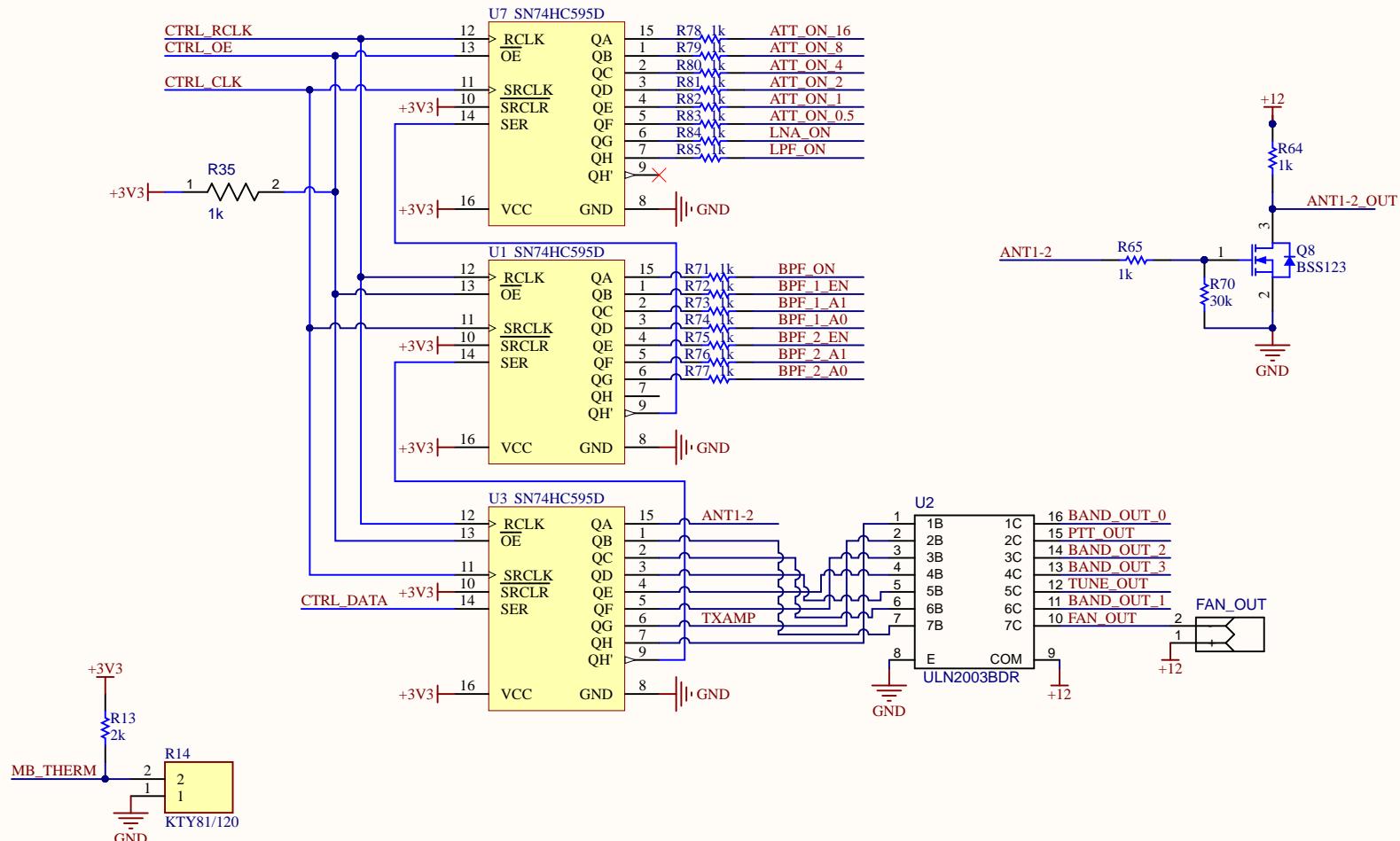
Date: 01.10.2020 Time: 0:16:41 Sheet 14 of 18

File: D:\Dropbox\Develop\Projects\UA3REO\Scheme\ALTIUM_DESIGNER\RF-UNIT\CONN.SchDoc

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A

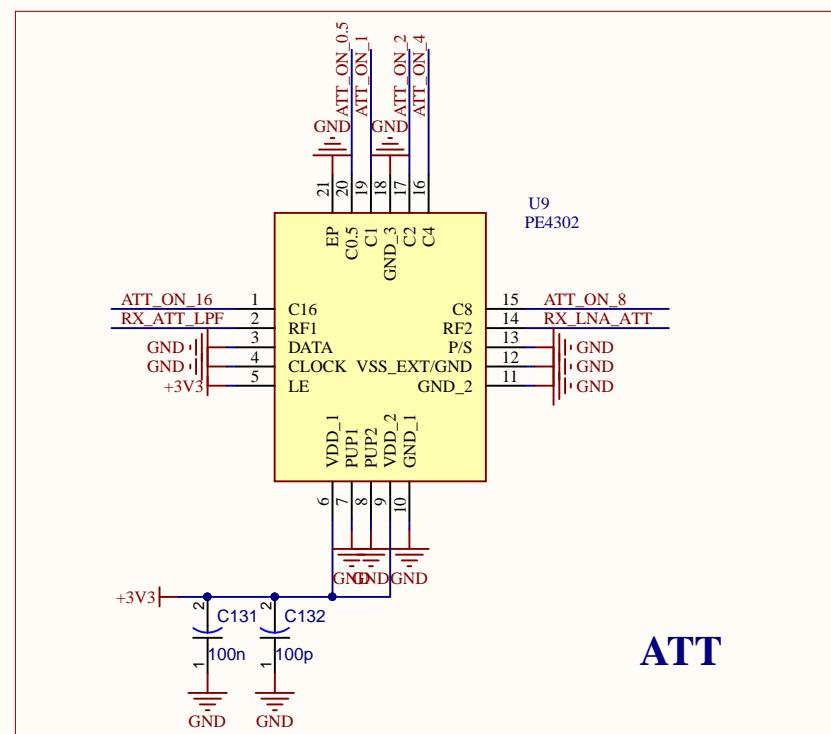
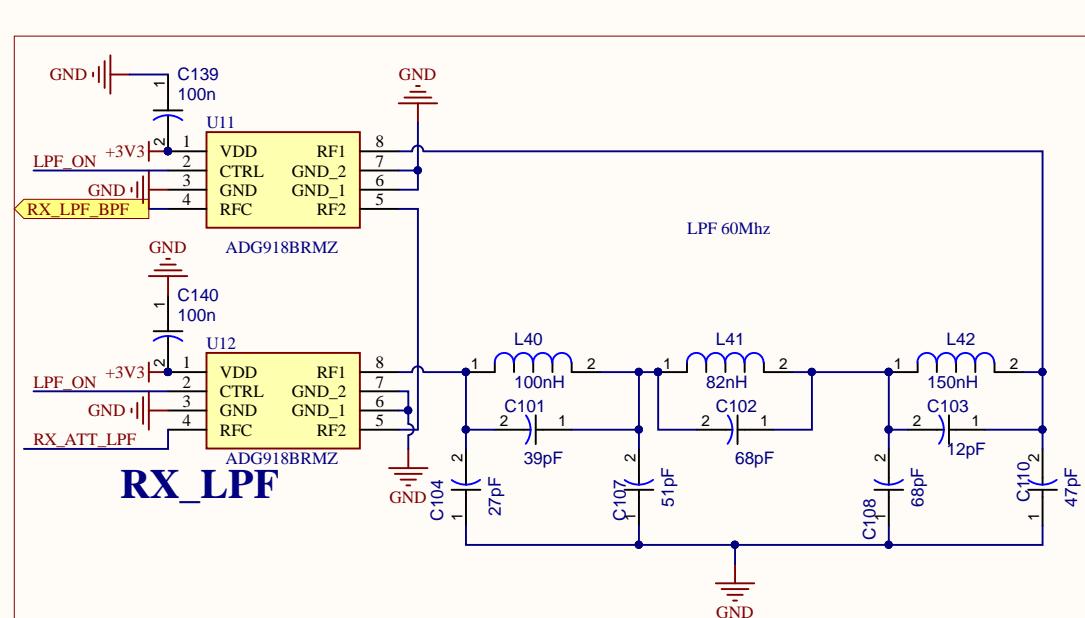
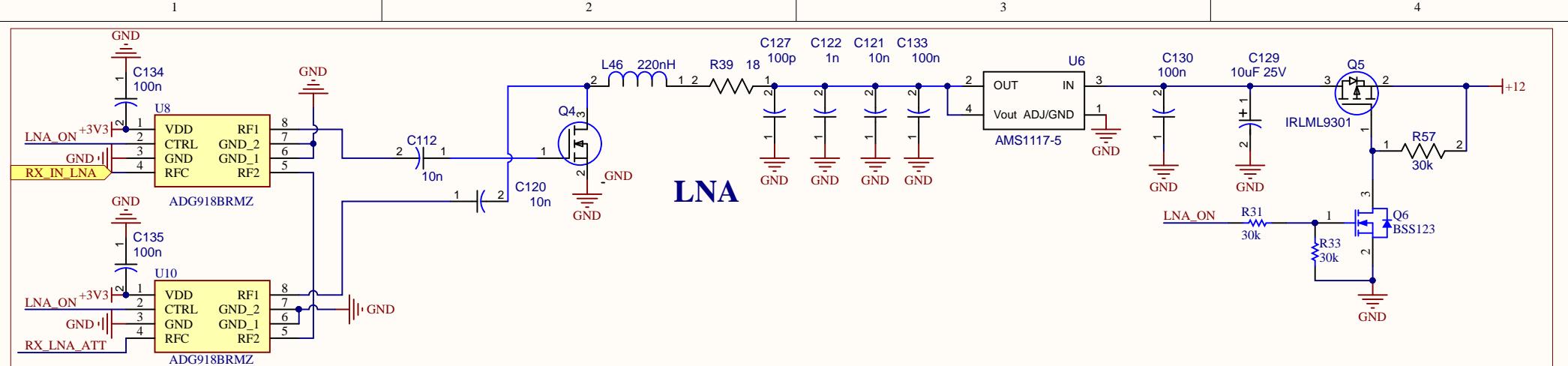
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Size: A4 Number:15 Revision:1.9

Date: 01.10.2020 Time: 0:16:41 Sheet 15 of 18

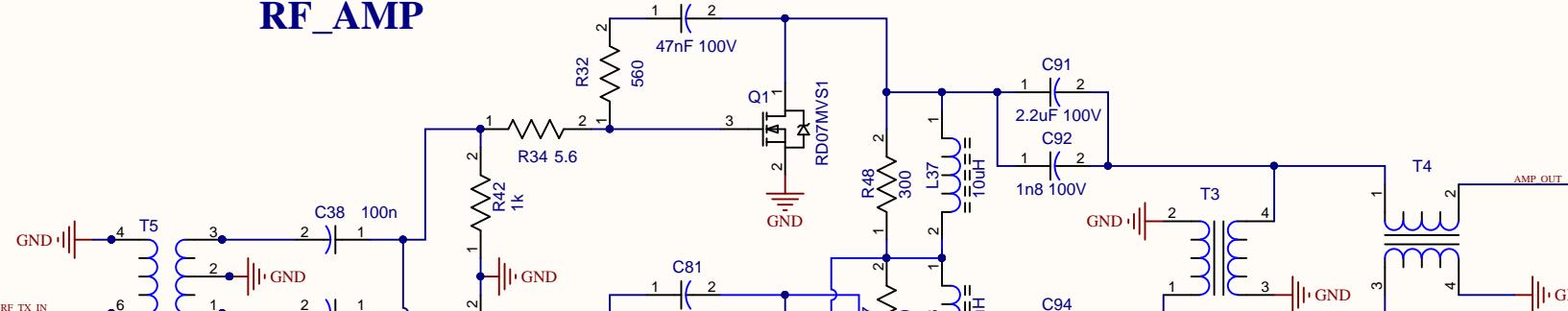
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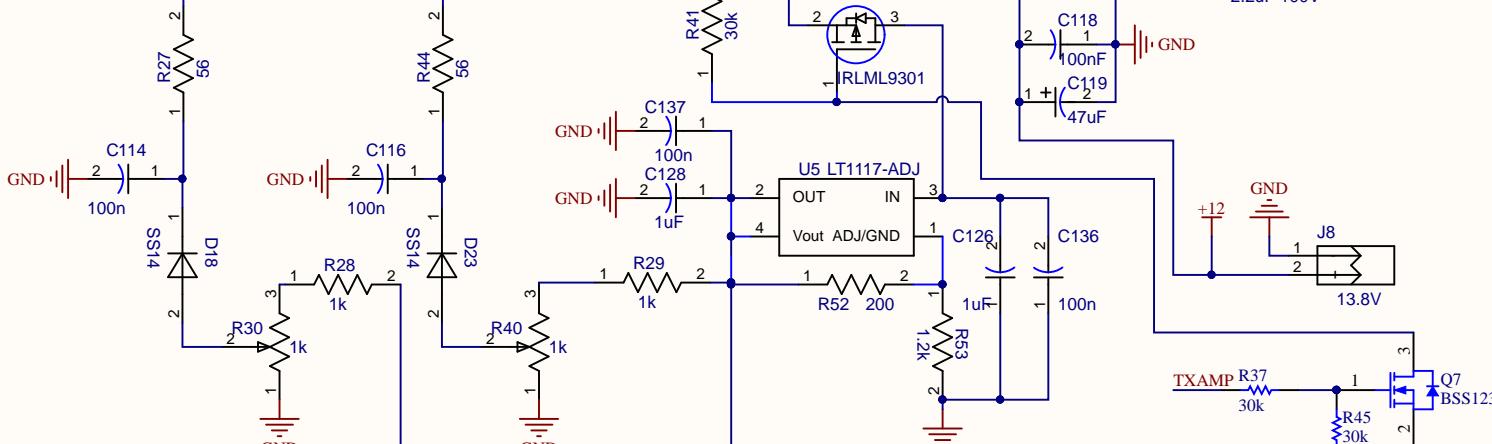
Title LNA			*	*
Size: A4	Number: 16	Revision: 1.9	*	*
Date: 01.10.2020	Time: 0:16:41	Sheet 16 of 18	*	*
File: D:\Dropbox\Develop\Projects\UA3REO\Scheme\ALTIUM_DESIGNER\RF-UNIT\LNA.SchDoc				

A

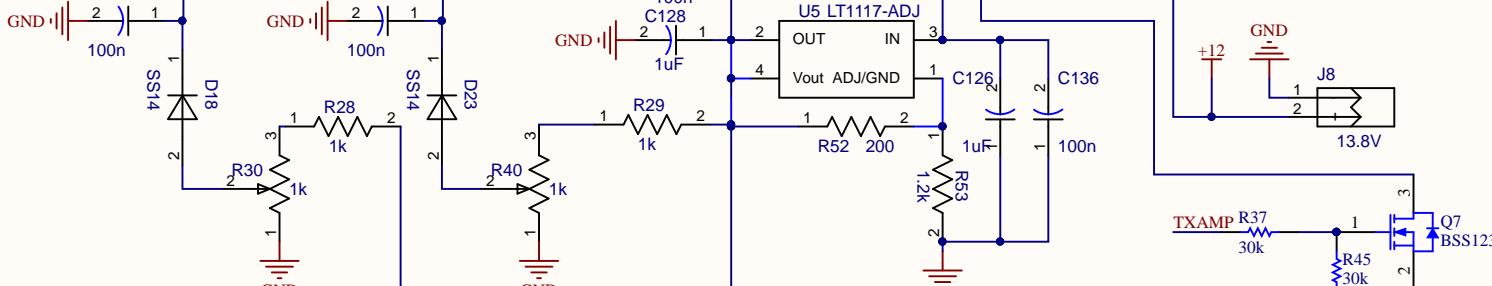
RF_AMP

T3 - 8-10 turns M2000HM 10x6x5
T4 - 3-4 turns RG-158 on Ferrite Ring 10x5x5 (or binocle)

B



C

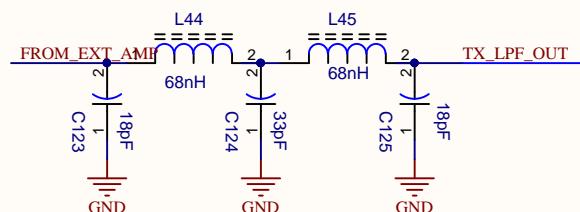


D

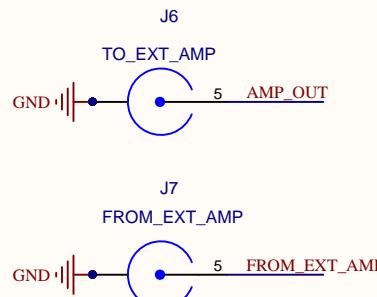
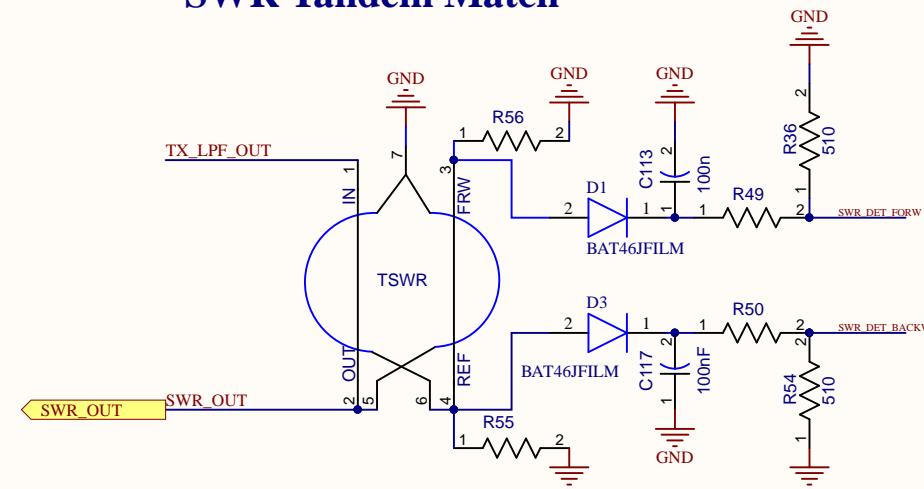
Title RF_AMP			*
Size: A4	Number: 17	Revision: 1.9	*
Date: 01.10.2020	Time: 0:16:42	Sheet 17 of 18	*
File: D:\Dropbox\Develop\Projects\UA3REO\Scheme\ALTIUM_DESIGNER\RF-UNIT\RF_AMP.SchDoc			Altium®

TX_LPF

LPF 170Mhz



Катушки намотаны проводом 0.5мм на оправке диаметром 5мм, 3.5 витка

**SWR Tandem Match**

2 провода 0.9мм пропущено через бинокль

по диагонали пропущено и намотано по 10 витков 0.5мм

Title **SWR Tandem Match**

Size: A4 Number:18 Revision:1.9

Date: 01.10.2020 Time: 0:16:42 Sheet 18 of 18

File: D:\Dropbox\Develop\Projects\UA3REO\Scheme\ALTIUM_DESIGNER\RF-UNIT\SWR Tandem Match.SchDoc

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