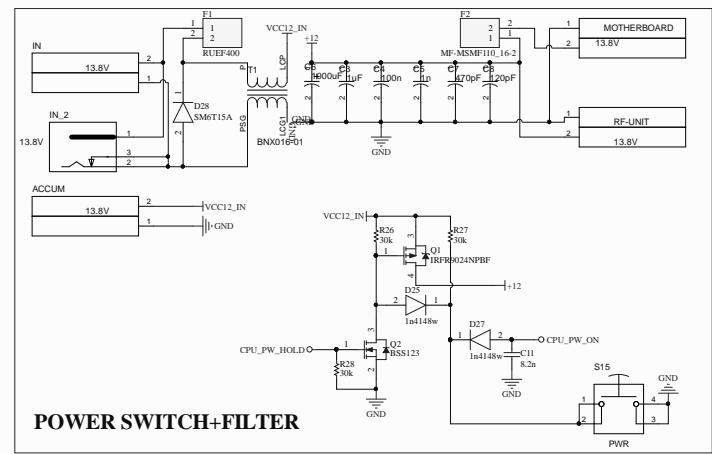
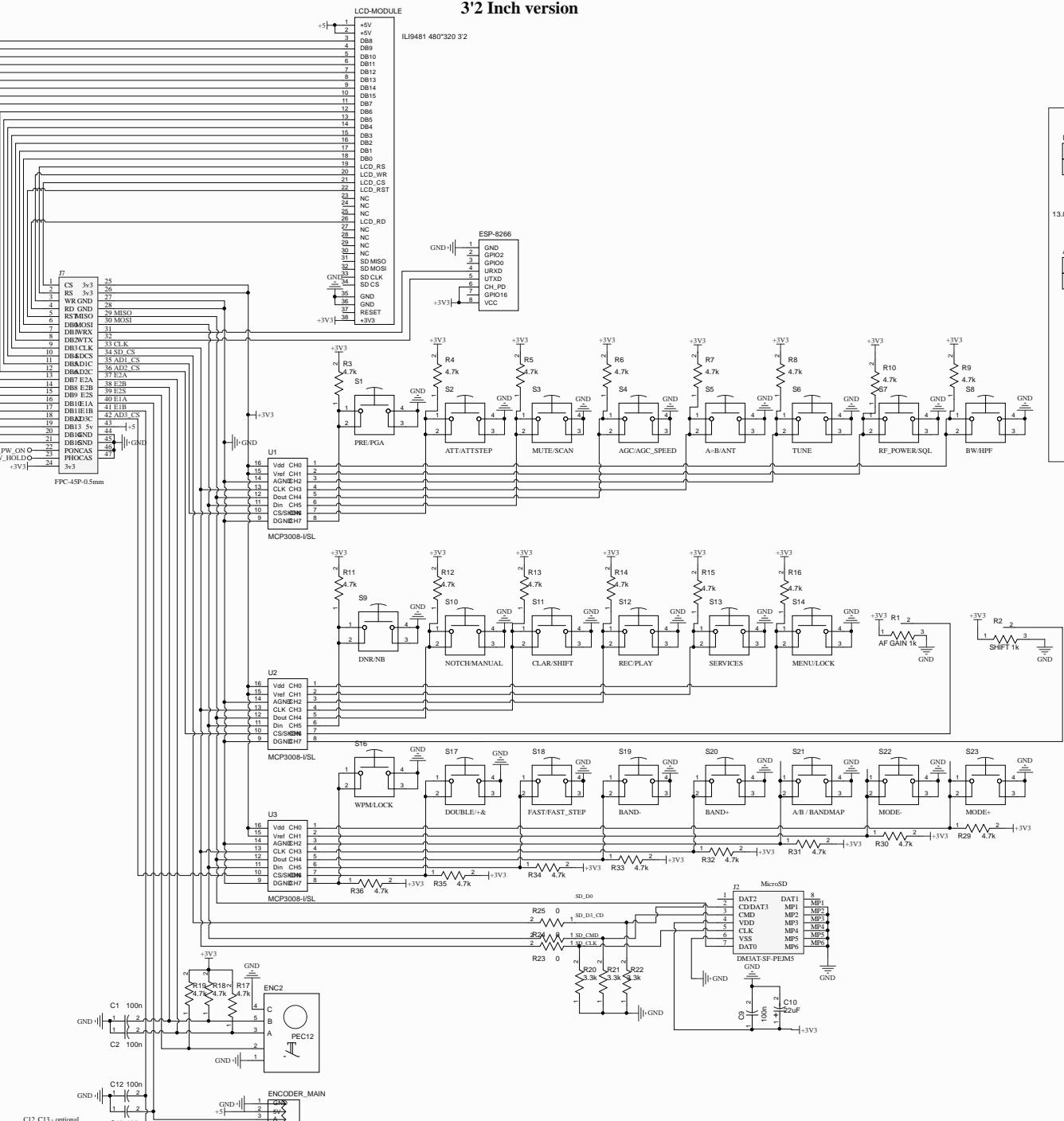


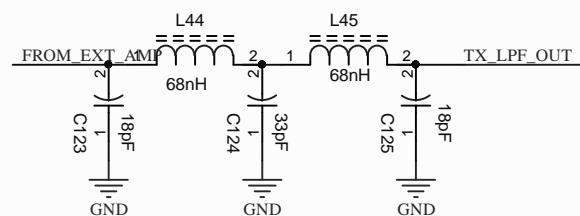
3'2 Inch version



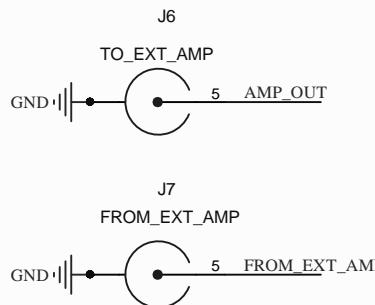
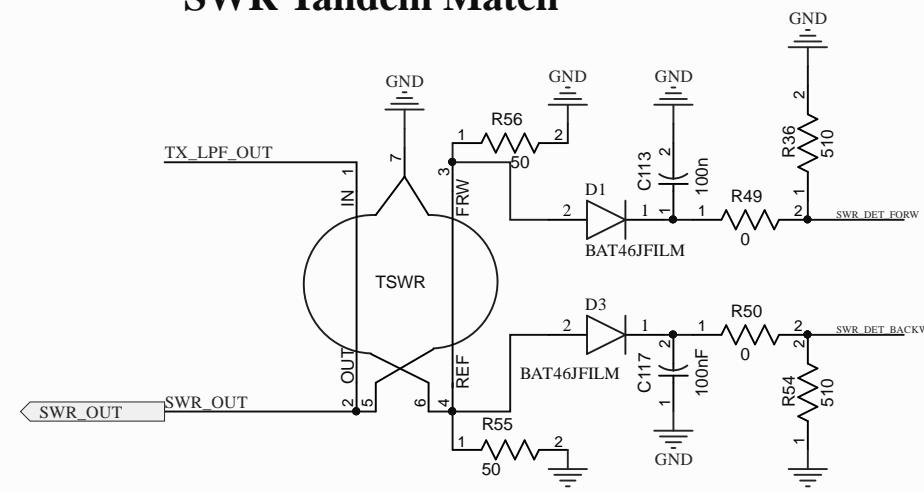
#### **POWER SWITCH+FILTER**

**TX\_LPF**

LPF 170Mhz



Катушки намотаны проводом 0.5мм на оправке диаметром 5мм, 3.5 витка

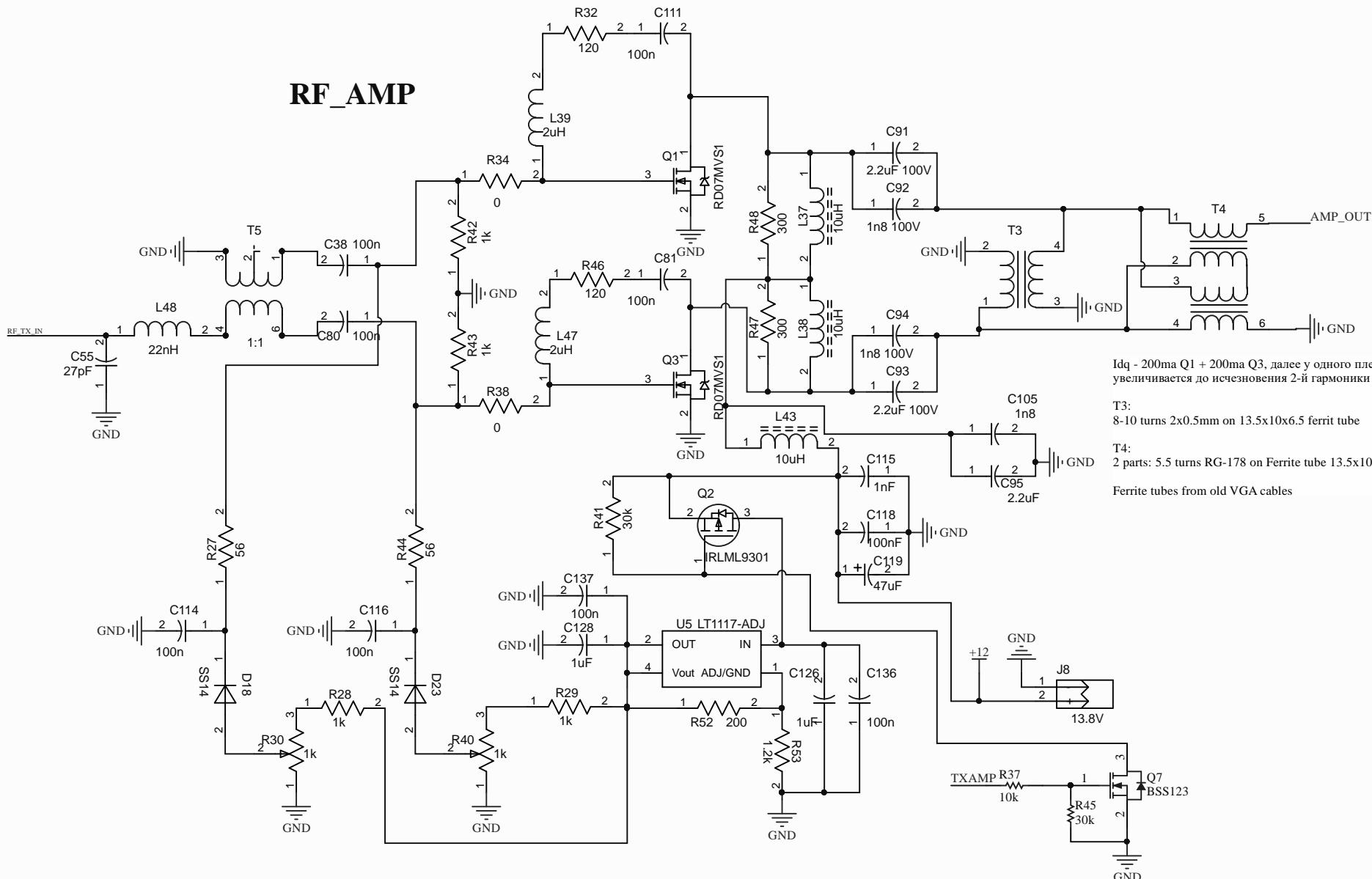
**SWR Tandem Match**Title **SWR Tandem Match**

Size: A4 Number:18 Revision:2.0

Date: 13.01.2021 Time: 9:18:11 Sheet:18 of 18

File: C:\Dropbox\Develop\Projects\WOLF\Scheme\ALTIUM\_DESIGNER\RF-UNIT\SWR Tandem Match.SchDoc

A

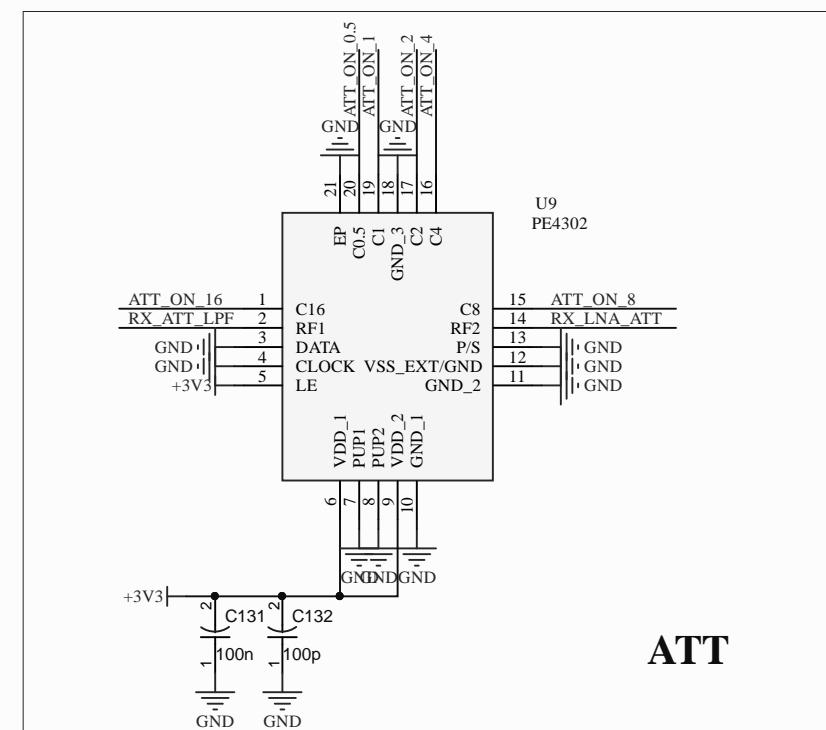
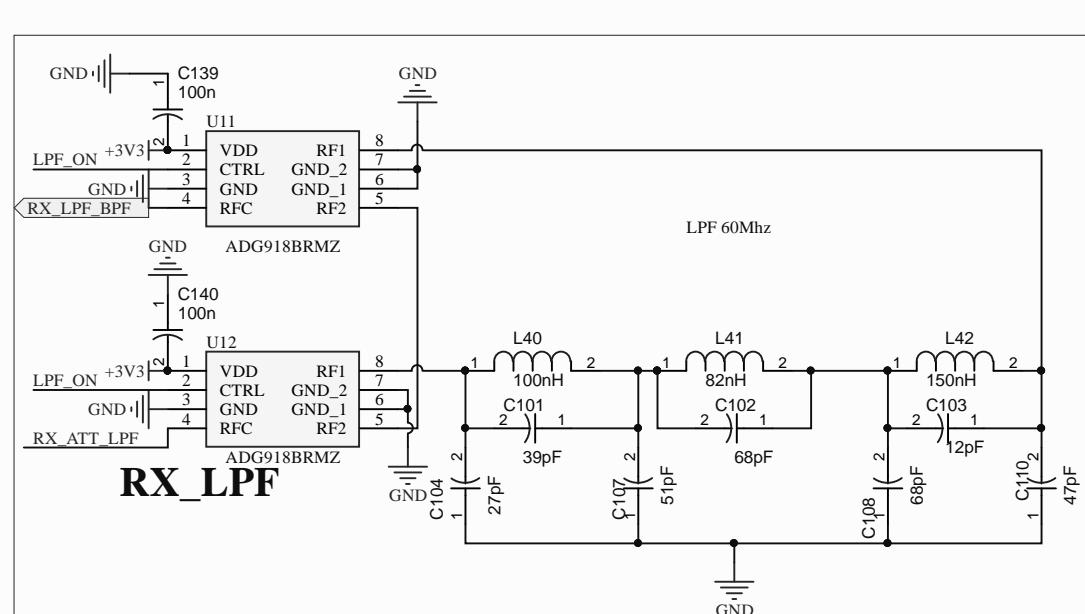
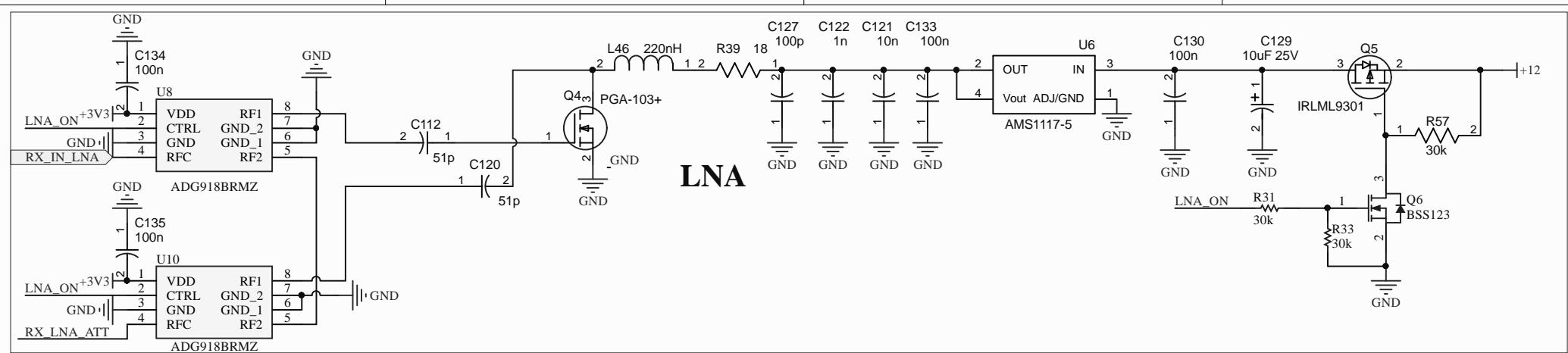
**RF\_AMP**Title **RF\_AMP**

Size: A4 Number:17 Revision 2.0

Date: 13.01.2021 Time: 9:18:14 Sheet 17 of 18

File: C:\Dropbox\Develop\Projects\WOLF\Schema\ALTIUM\_DESIGNER\RF-UNIT\RF\_AMP.SchDoc

**Altium**

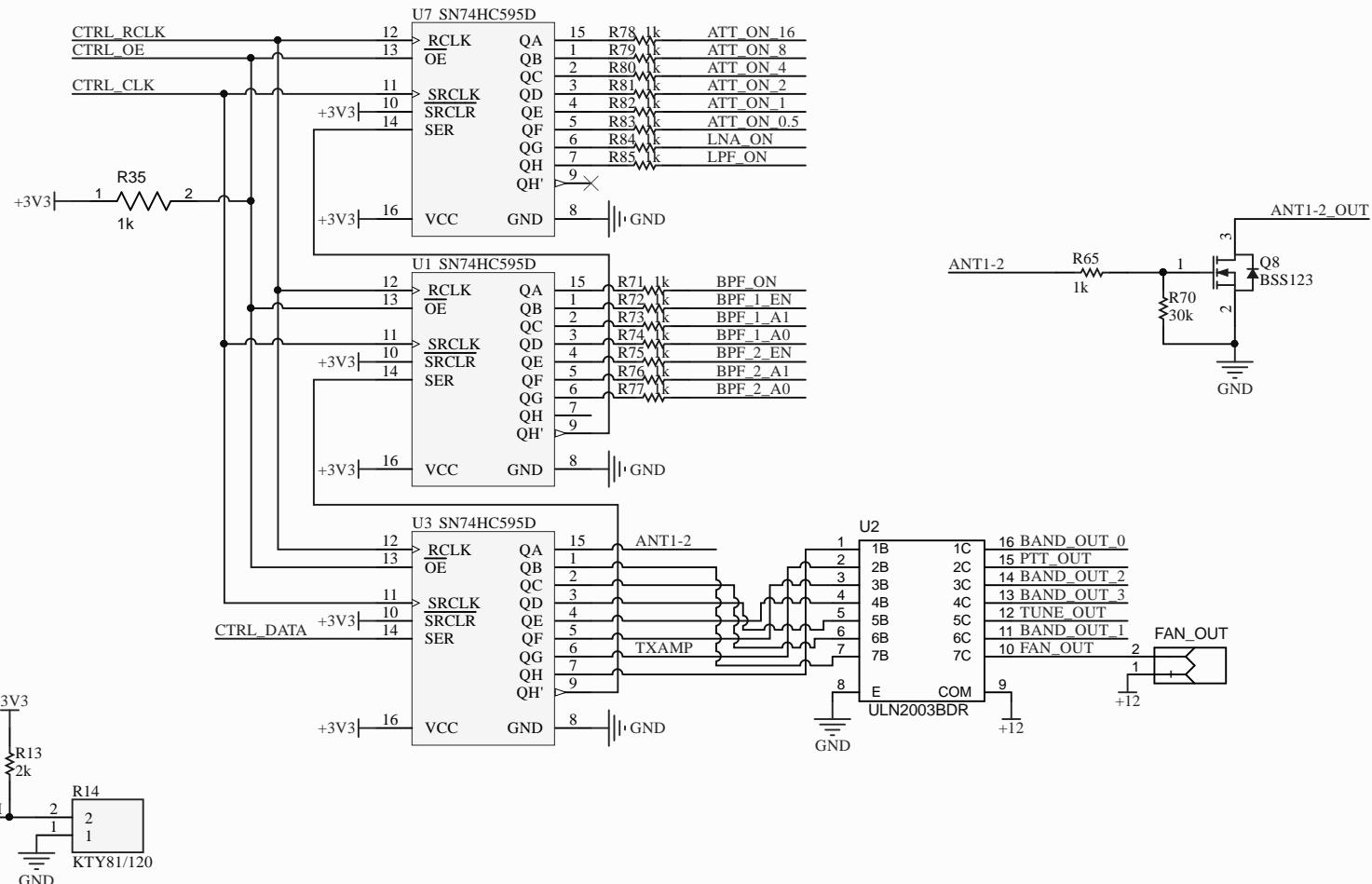


Title <b>LNA</b>			*
Size: A4	Number:16	Revision2.0	*
Date: 13.01.2021	Time: 9:18:16	Sheet16 of 18	*
File: C:\Dropbox\Develop\Projects\WOLF\Scheme\ALTIUM_DESIGNER\RF-UNIT\LNA.SchDoc			

**Altium**

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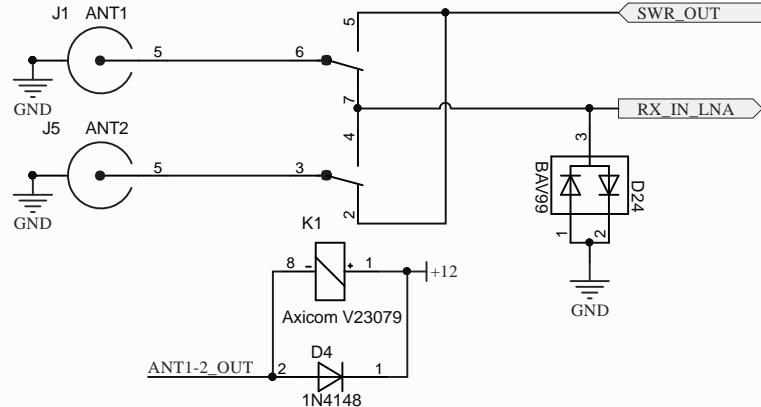
Title **CONTROL**

Size: A4	Number: 15	Revision 2.0
Date: 13.01.2021	Time: 9:18:19	Sheet 15 of 18
File: C:\Dropbox\Develop\Projects\WOLF\Scheme\ALTIUM_DESIGNER\RF-UNIT\CONTROL.SchDoc		*

**Altium**

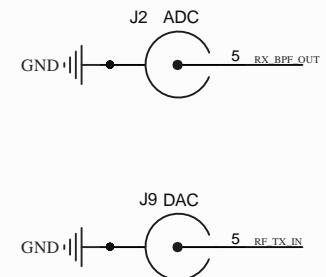
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## TXRX\_COMUTATOR

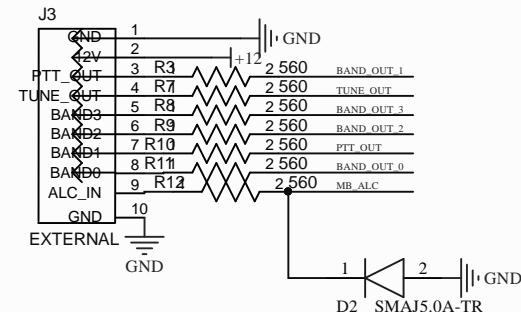
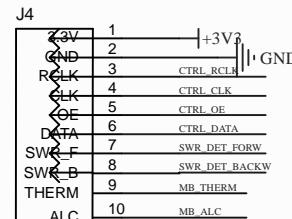


B

## CONN



C

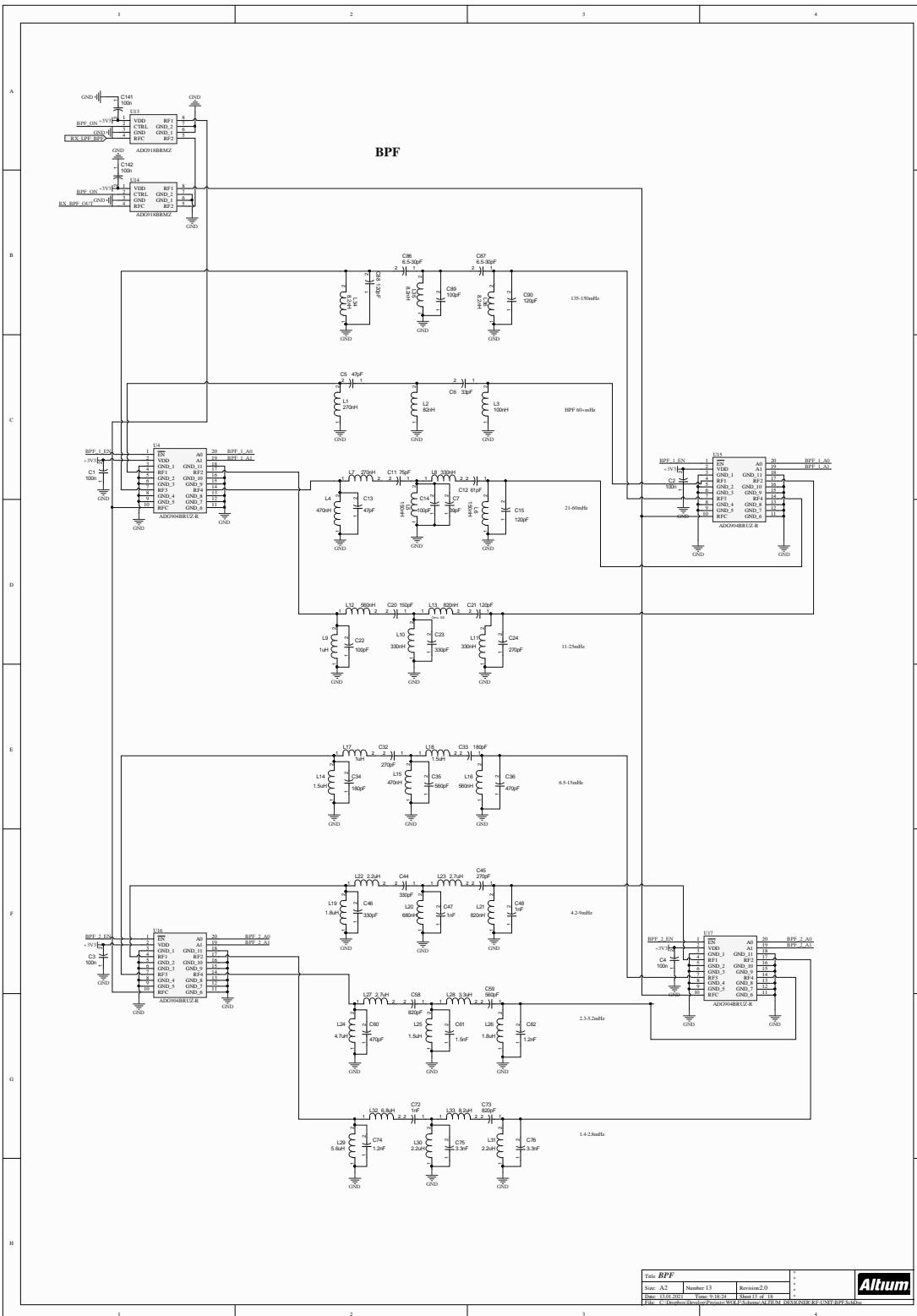


D

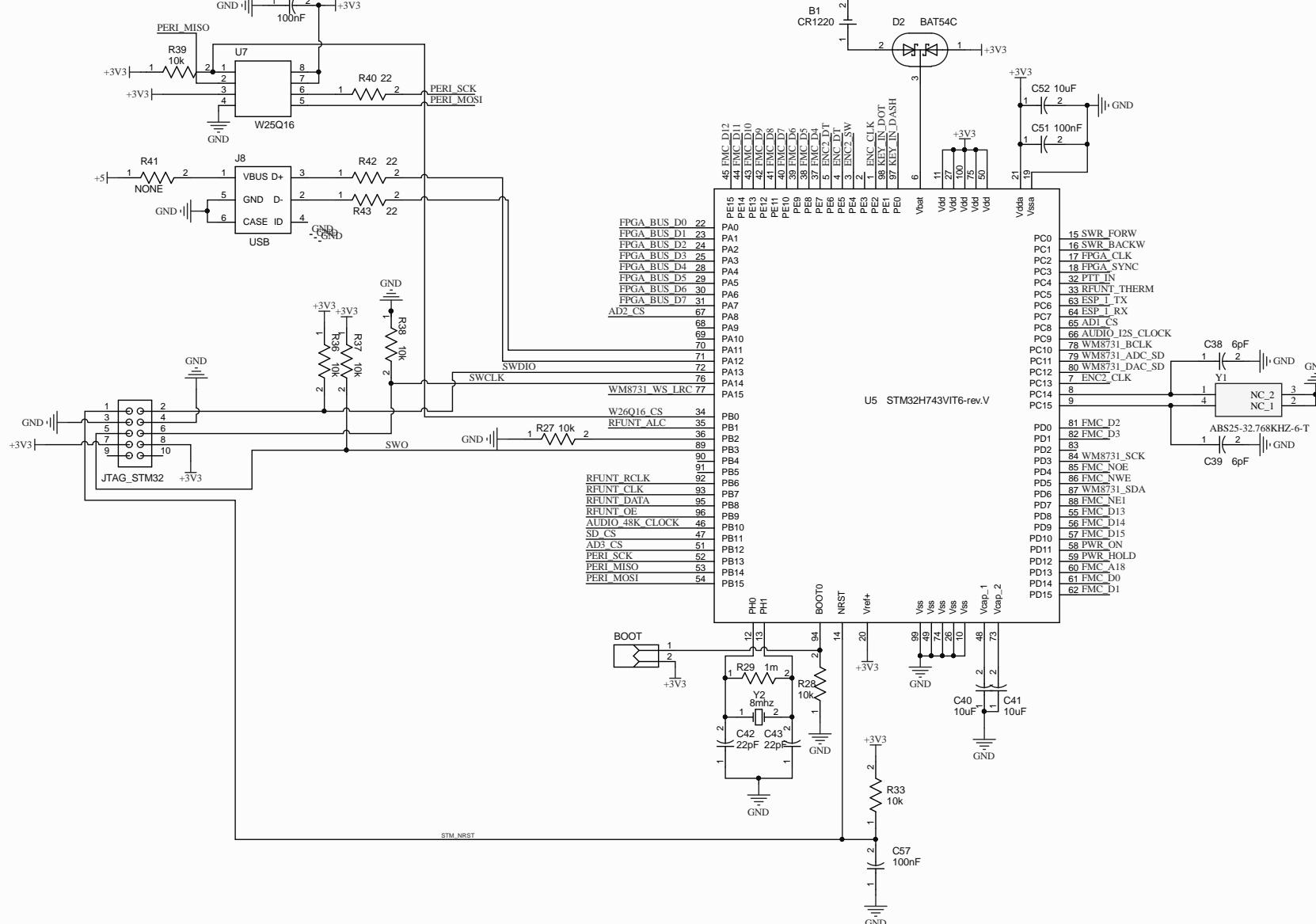
Title **CONN**

Size: A4	Number:14	Revision2.0
Date: 13.01.2021	Time: 9:18:21	Sheet14 of 18
File: C:\Dropbox\Develop\Projects\WOLF\Scheme\ALTIUM_DESIGNER\RF-UNIT\CONN.SchDoc		*

**Altium**

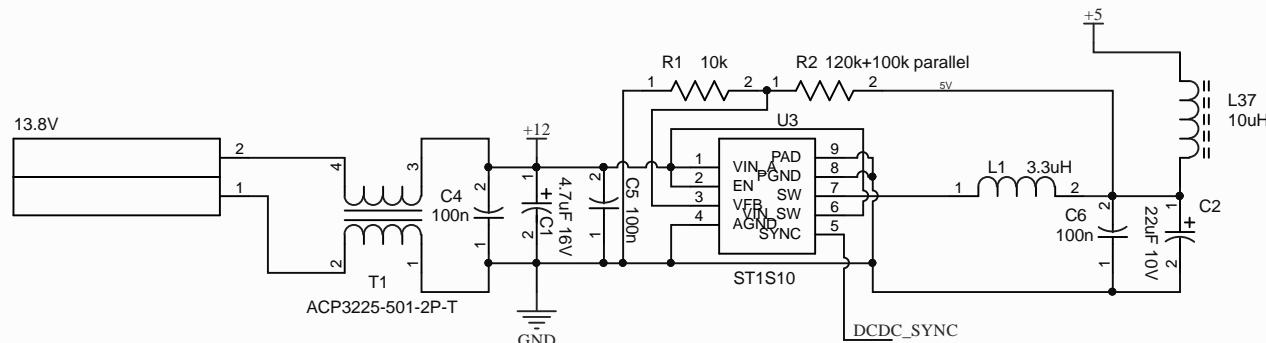


STM32



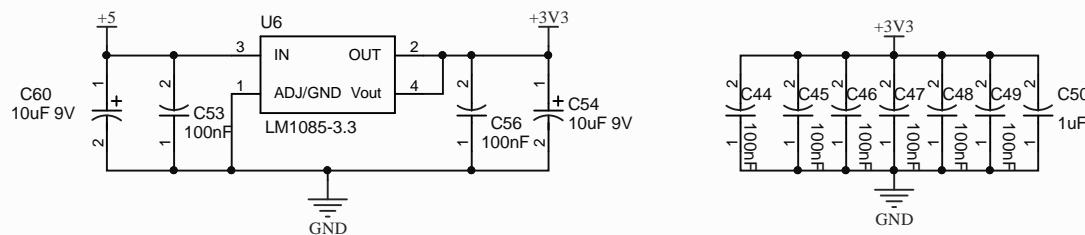
Title	<b>STM32</b>	*	
Size:	A3	*	
Number:	11	*	
Revision:	2.0	*	
Date:	13.01.2021	Time: 9:18:27	Sheet 11 of 18
File:	C:\Droron\Development\Projects\WOLFEScheme\Altium\DESIGNER\MOTHERBOARD\STM32.SchDoc		

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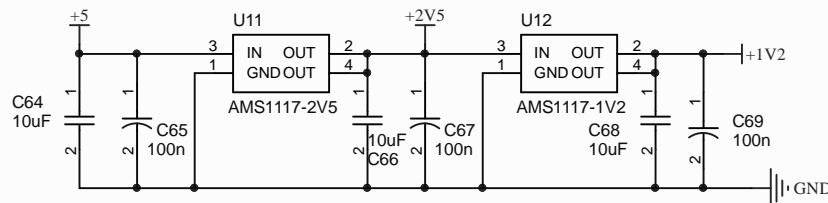
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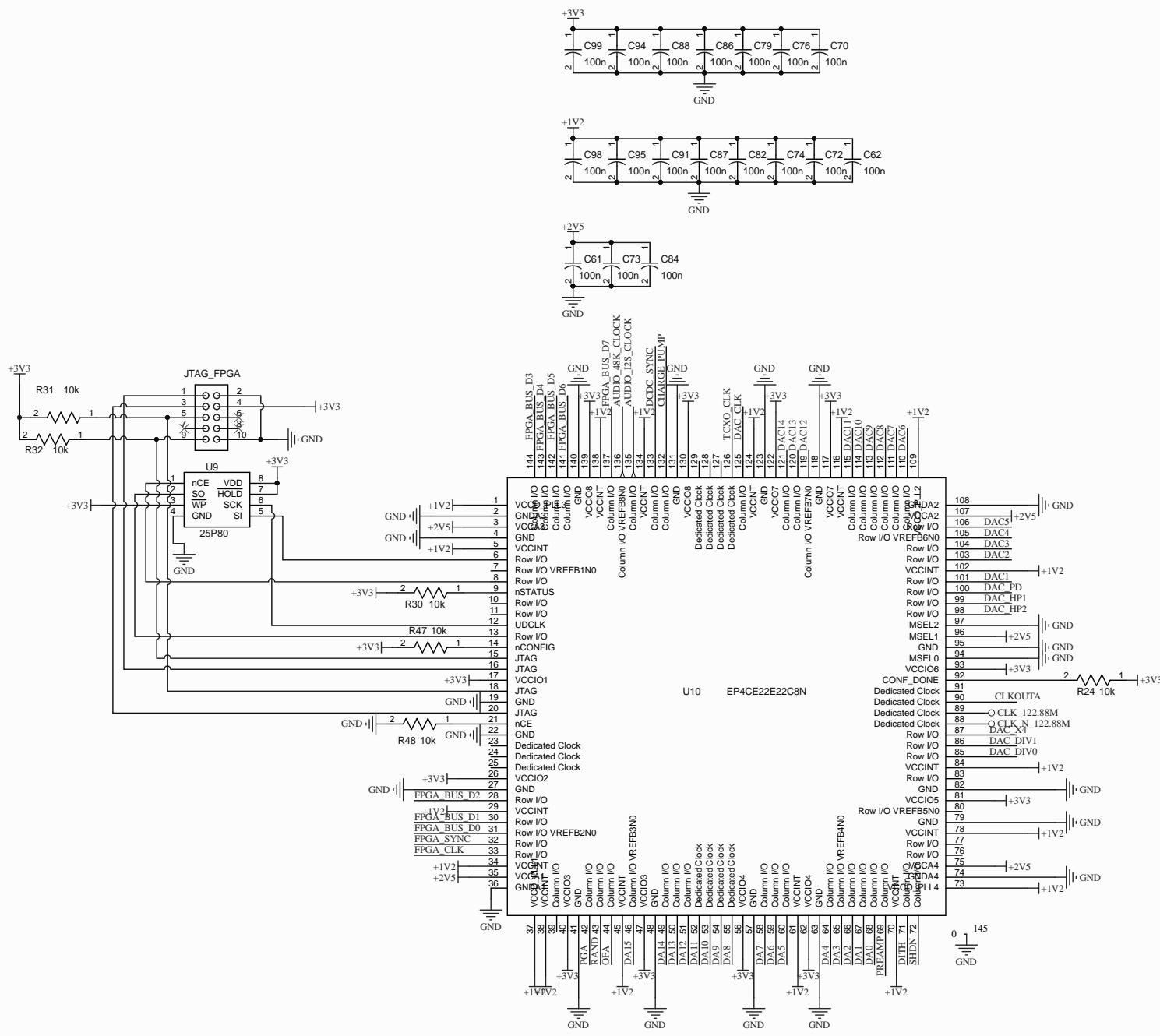
C

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Title **POWER**

Size: A4	Number:10	Revision2.0
Date: 13.01.2021	Time: 9:18:30	Sheet10 of 18
File: C:\Dropbox\Develop\Projects\WOLF\Scheme\ALTIUM_DESIGNER\MOTHERBOARD\POWER.SchDoc		*

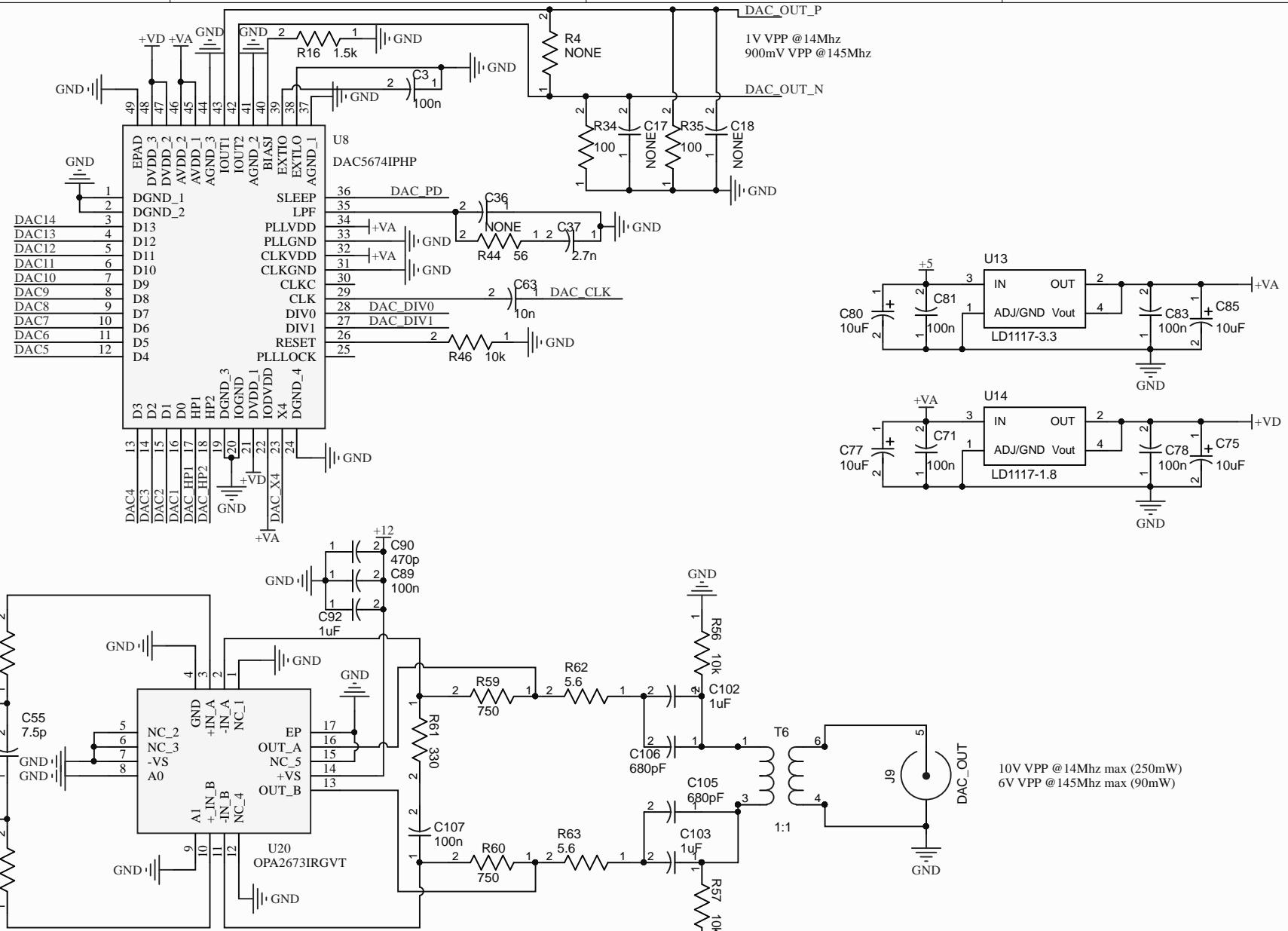
**Altium**



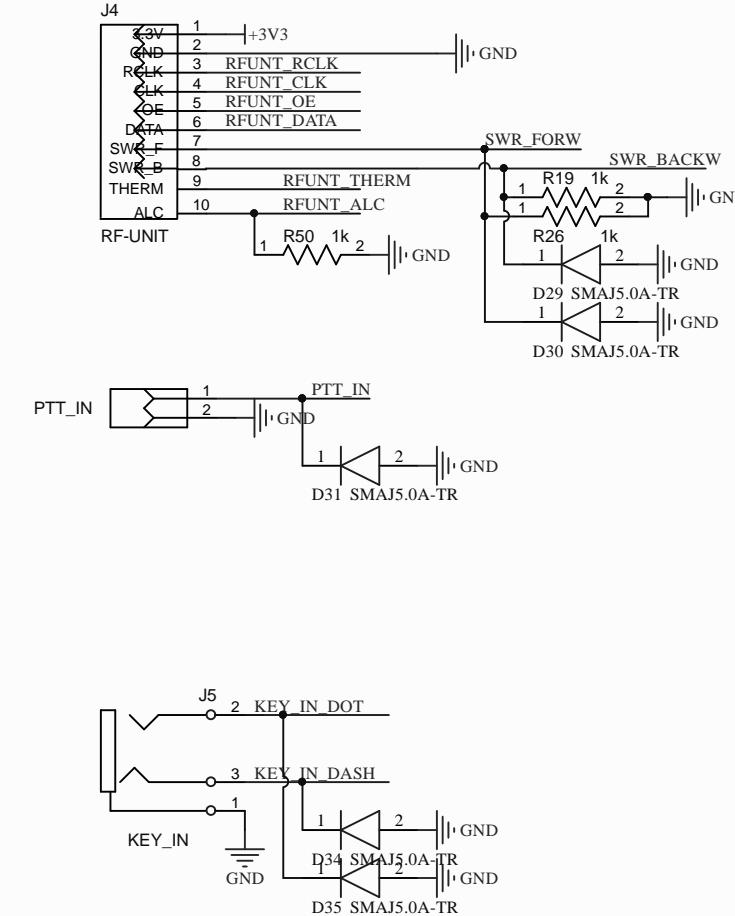
Title **FPGA**

Size: A3 Number:9 Rev: 1  
Date: 13.01.2021 Time: 9:18:34 Sheet: 1  
File: C:\Dropbox\Develop\Projects\WOLFS

**Altium**



Title **DAC** \*  
 Size: A4 Number:8 Revision:2.0 \*  
 Date: 13.01.2021 Time: 9:18:37 Sheet 8 of 18 \*  
 File: C:\Dropbox\Develop\Projects\WOLF\Scheme\ALTIUM DESIGNER\MOTHERBOARD\DAC.SchDoc \*  

**J6**

FMC_NE1	1	CS 3v3
FMC_A18	2	RS 3v3
FMC_NWE	3	WR GND
FMC_NOE	4	RD GND
STM_NRST	5	RST#MISO
FMC_D0	6	DB#MOSI
FMC_D1	7	DB#WRX
FMC_D2	8	DB#WTX
FMC_D3	9	DB#3CLK
FMC_D4	10	DB#SDCS
FMC_D5	11	DB#AD1_CS
FMC_D6	12	DB#AD2_CS
FMC_D7	13	DB#E2A
FMC_D8	14	DB#E2B
FMC_D9	15	DB#E2S
FMC_D10	16	DB#E1A
FMC_D11	17	DB#E1B
FMC_D12	18	DB#AD3_CS
FMC_D13	19	DB#5v
FMC_D14	20	DB#GND
FMC_D15	21	DB#GND
PWR_ON	22	PONCAS
PWR_HOLD	23	PHOCAS
	24	3v3
	25	+3V3
	26	GND
	27	
	28	
	29	PERI_MISO
	30	PERI_MOSI
	31	ESP_1_TX
	32	ESP_1_RX
	33	PERI_SCK
	34	SD_CS
	35	AD1_CS
	36	AD2_CS
	37	ENC2_DT
	38	ENC2_CLK
	39	ENC2_SW
	40	ENC_DT
	41	ENC_CLK
	42	AD3_CS
	43	
	44	+5
	45	GND
	46	GND
	47	

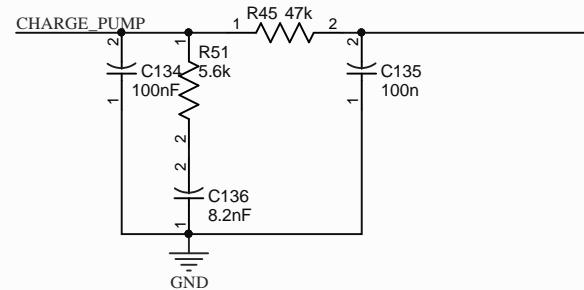
FPC-45P-0.5mm

Title **CONNECTIONS**

Size: A4	Number:7	Revision2.0
Date: 13.01.2021	Time: 9:18:40	Sheet7 of 18
File: C:\Dropbox\Develop\Projects\WOLF\Scheme\ALTIUM_DESIGNER\MOTHERBOARD\CONNECTIONS.SchDoc		*

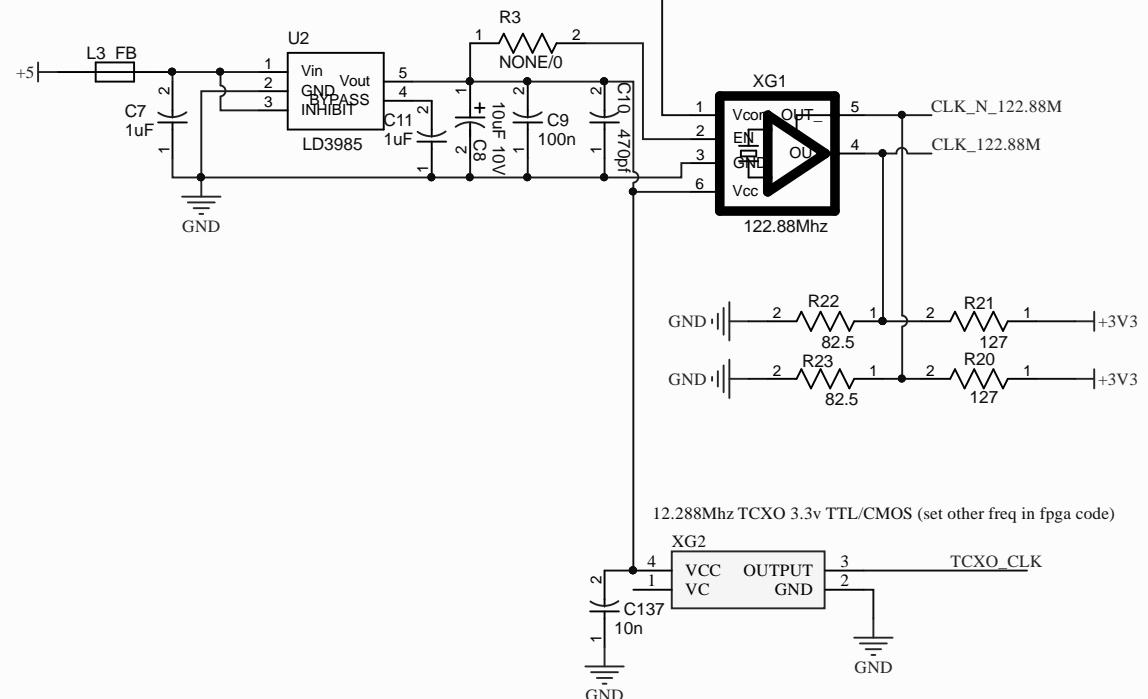
**Altium**

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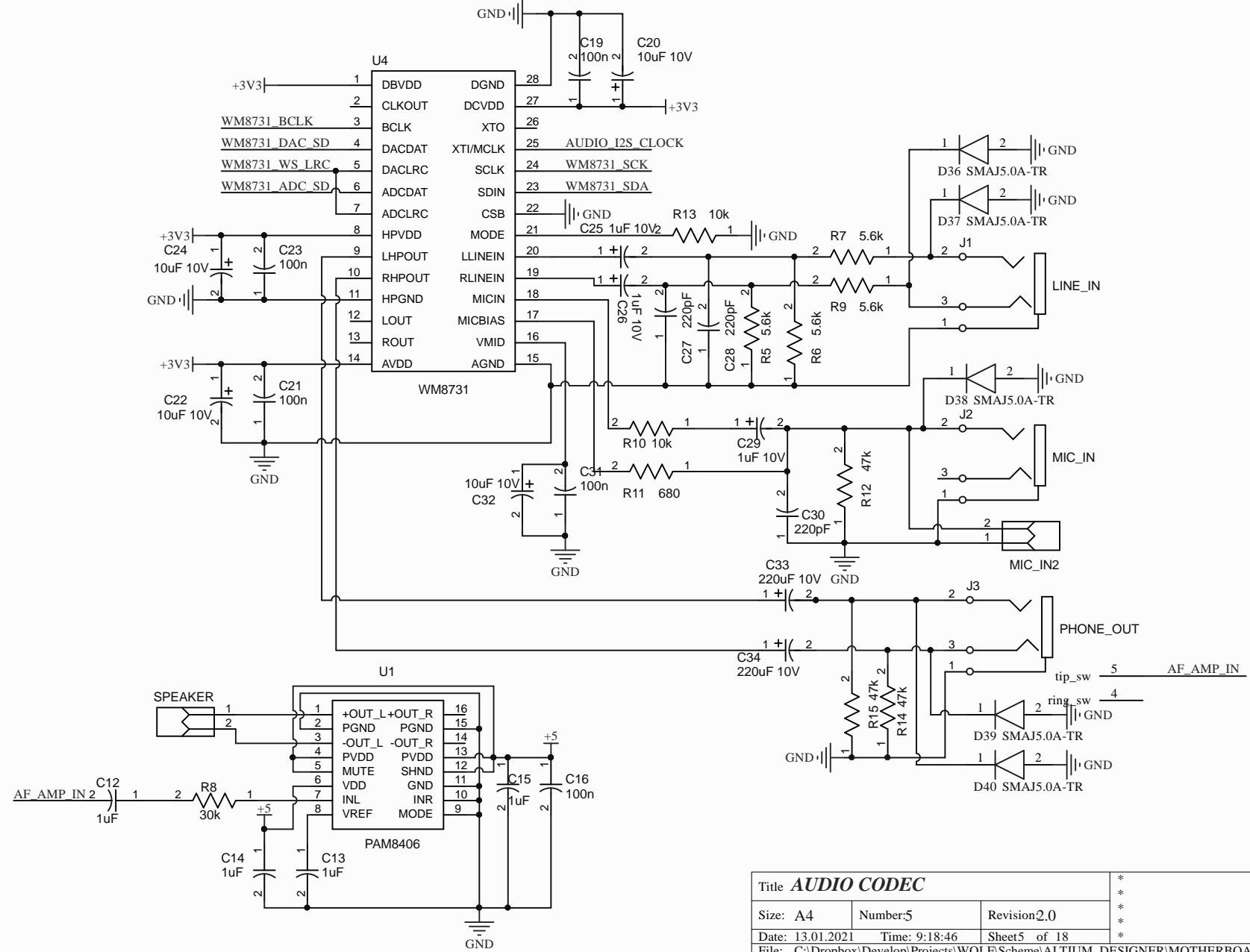
D

Title **CLOCK\_GENERATOR**

Size: A4	Number:6	Revision2.0
Date: 13.01.2021	Time: 9:18:43	Sheet6 of 18
File: C:\Dropbox\Develop\Projects\WOLF\Scheme\ALTIUM_DESIGNER\MOTHERBOARD\CLOCK_GENERATOR.SchDoc		*

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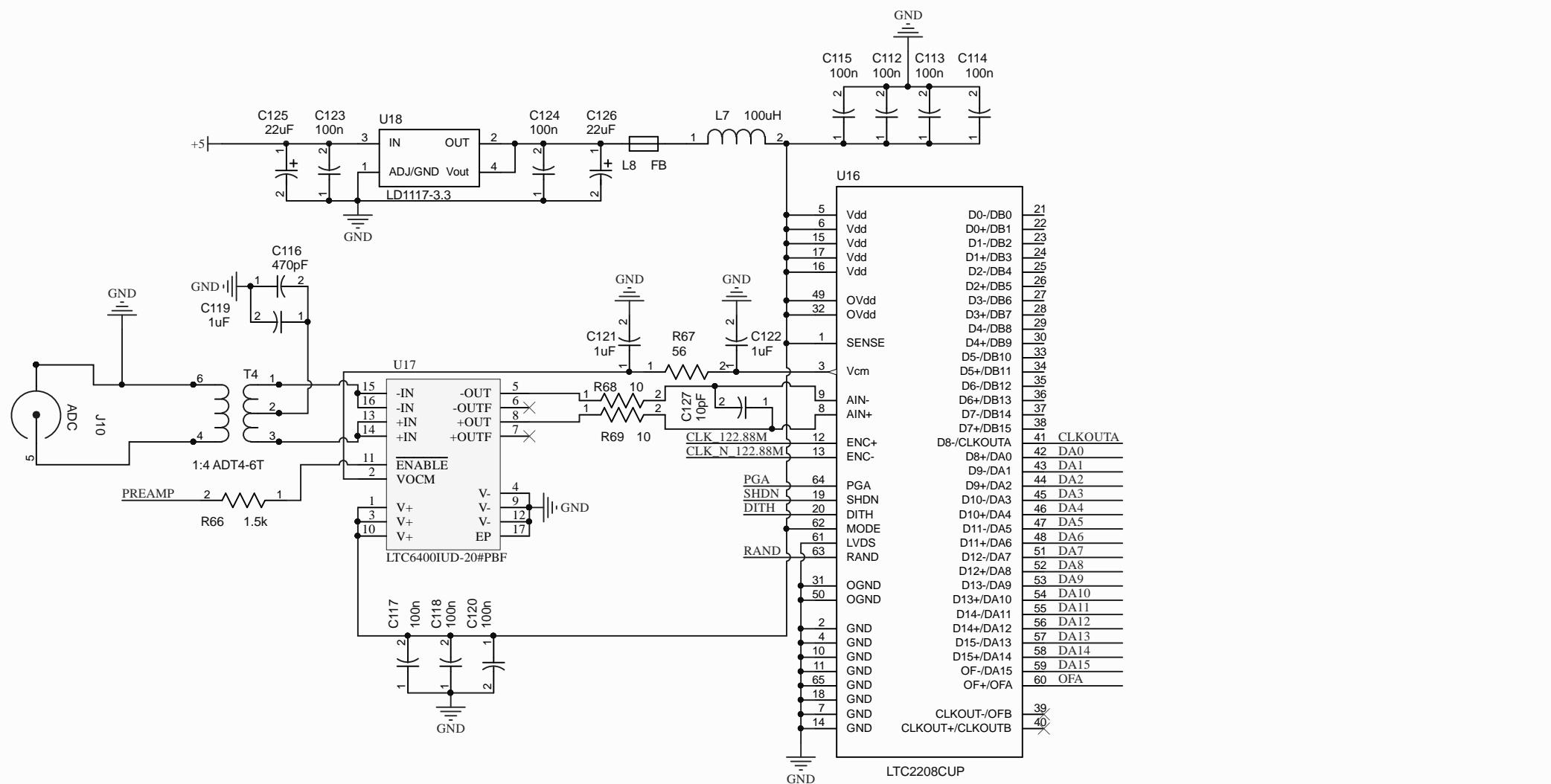
Title **AUDIO CODEC**

Size: A4 Number:5 Revision:2.0

Date: 13.01.2021 Time: 9:18:46 Sheet 5 of 18

File: C:\Dropbox\Develop\Projects\WOLF\Schema\ALTIUM\_DESIGNER\MOTHERBOARD\AUDIO\_CODEC.SchDoc

**Altium**



Title **ADC** \*  
 Size: A4 Number:3 Revision 2.0 \*  
 Date: 13.01.2021 Time: 9:18:49 Sheet 3 of 18 \*  
 File: C:\Dropbox\Development\Projects\WOLF\Scheme\ALTIUM DESIGNER\MOTHERBOARD\ADC.SchDoc \*



