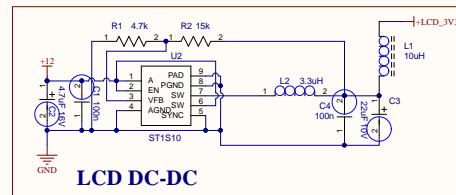
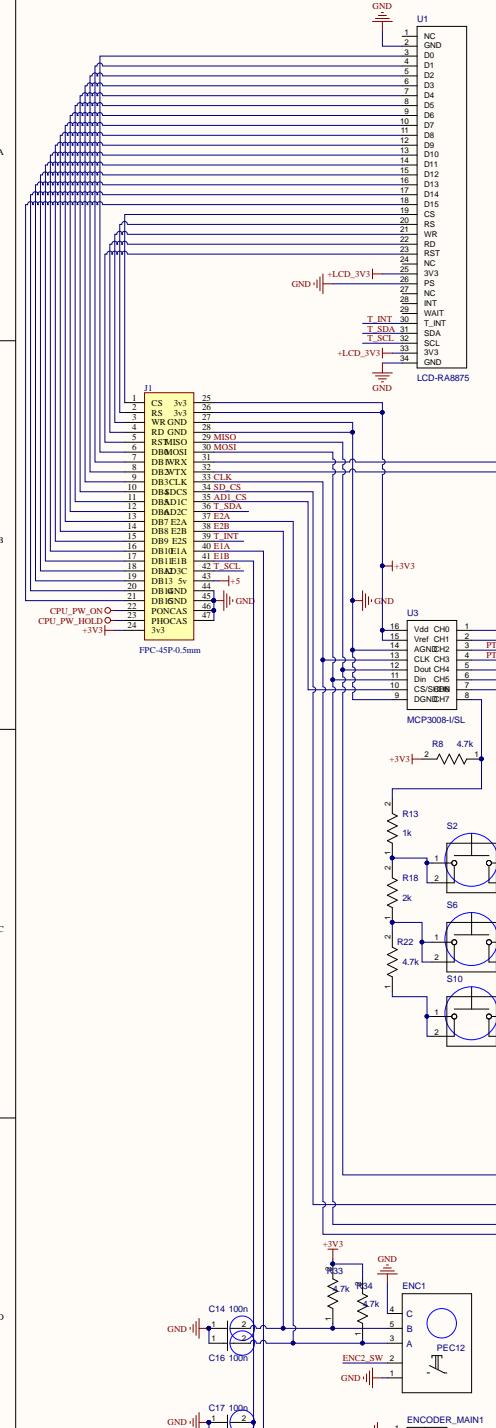


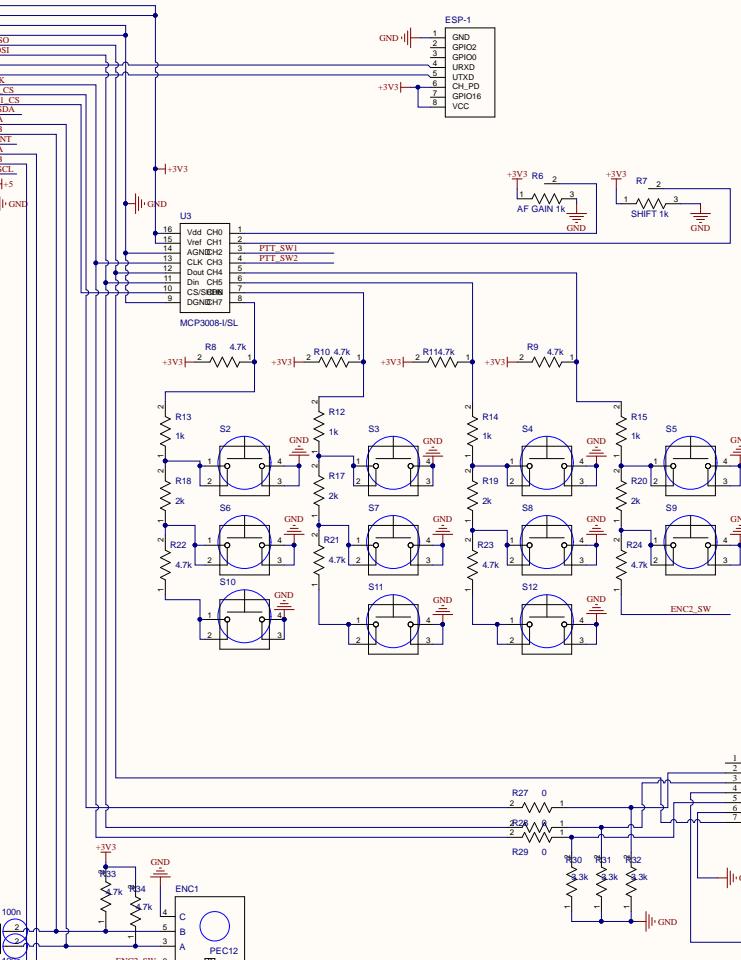
7Inch version



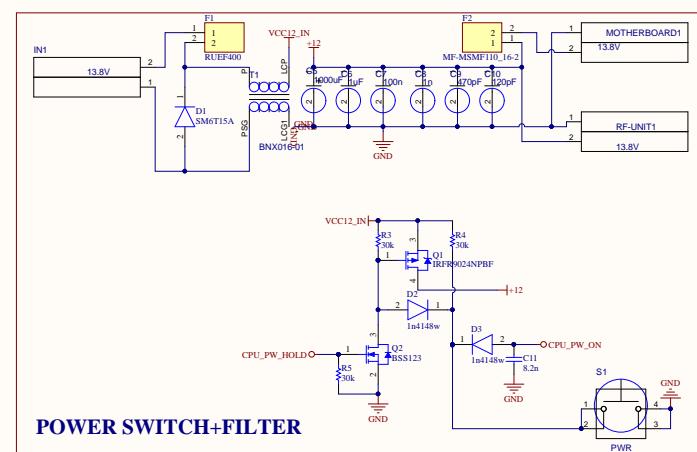
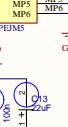
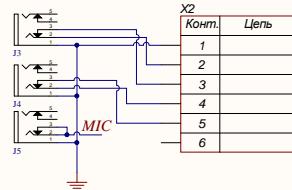
A



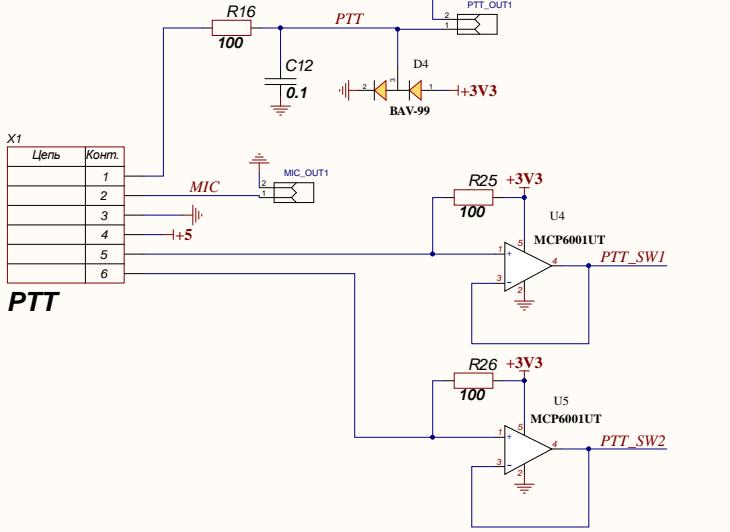
B



C

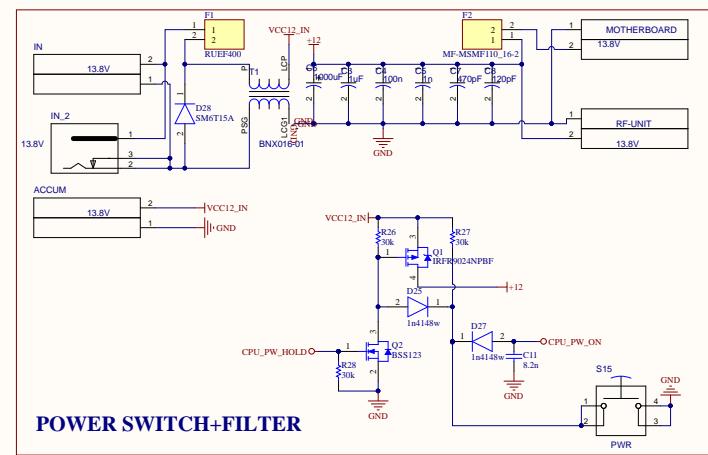
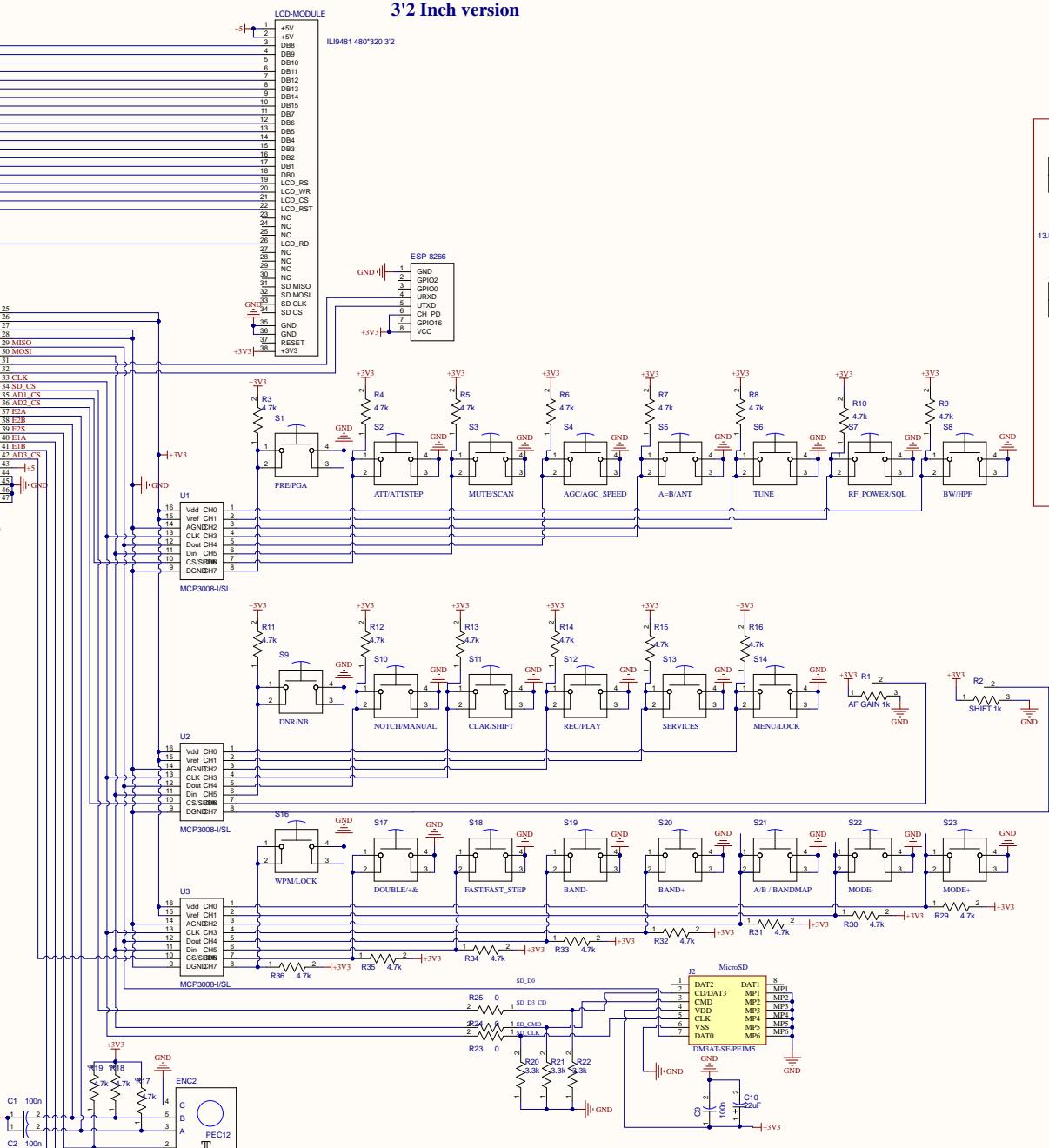


TANTEN



3'2 Inch version

ILI9481 480*320 3'2

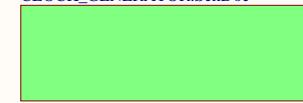


A

U_POWER
POWER.SchDoc

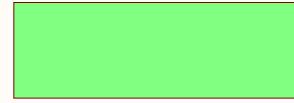


U_CLOCK_GENERATOR
CLOCK_GENERATOR.SchDoc

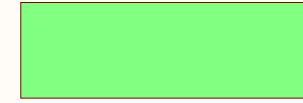


B

U_CONNECTIONS
CONNECTIONS.SchDoc



U_FPGA
FPGA.SchDoc



U_STM32
STM32.SchDoc



U_AUDIO_CODEC
AUDIO_CODEC.SchDoc



A

B

C

D

U_DAC
DAC.SchDoc



U_ADC
ADC.SchDoc



Title **MOTHERBOARD**

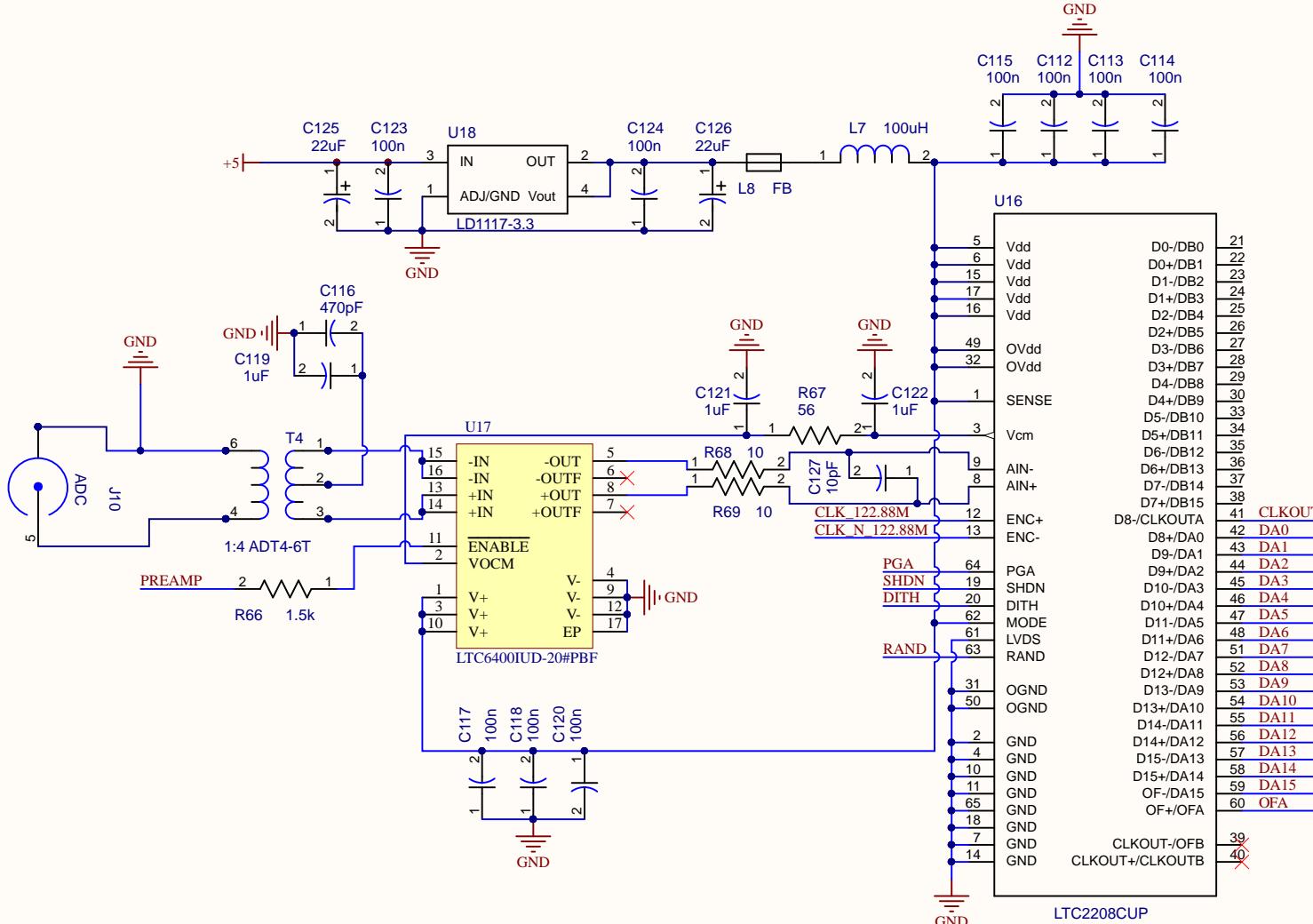
Size: A4	Number:2	Revision:2.0
----------	----------	--------------

Date: 09.11.2020	Time: 20:27:01	Sheet 2 of 18
------------------	----------------	---------------

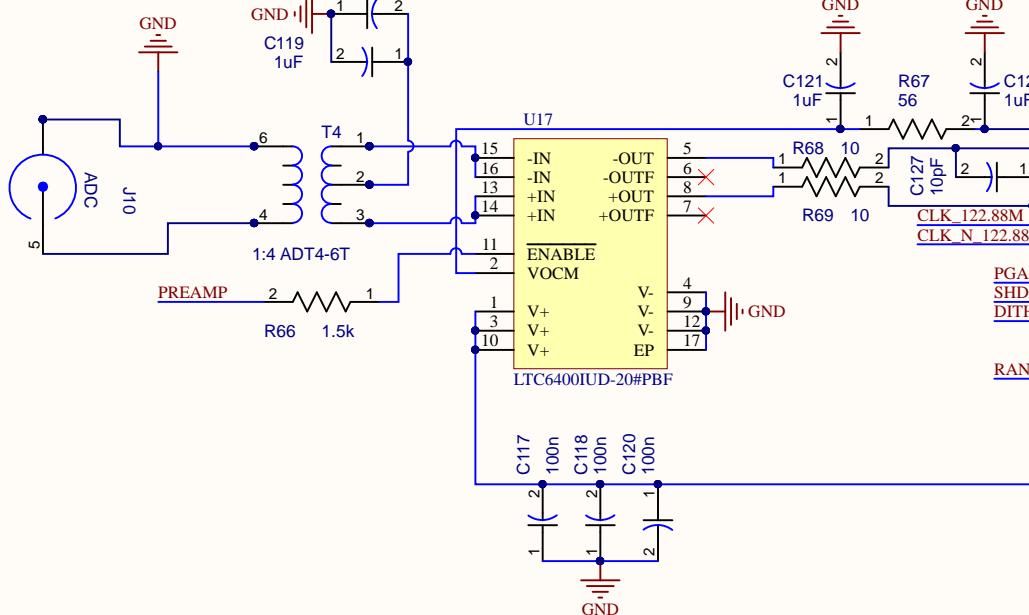
File: D:\Dropbox\Develop\Projects\WOLF\Scheme\ALTIUM_DESIGNER\MOTHERBOARD\MOTHERBOARD.SCHDOC	*	*	*	*
--	---	---	---	---



A



B



	D0-/DB0	21
	D0+/DB1	22
	D1-/DB2	23
	D1+/DB3	24
	D2-/DB4	25
	D2+/DB5	26
	D3-/DB6	27
	D3+/DB7	28
	D4-/DB8	29
	D4+/DB9	30
	D5-/DB10	33
	D5+/DB11	34
	D6-/DB12	35
	D6+/DB13	36
	D7-/DB14	37
	D7+/DB15	38
	CLKOUTA	41
	DA0	42
	DA1	43
	DA2	44
	DA3	45
	DA4	46
	DA5	47
	DA6	48
	DA7	51
	DA8	52
	DA9	53
	DA10	54
	DA11	55
	DA12	56
	DA13	57
	DA14	58
	DA15	59
	OFA	60
	CLKOUT-/OFB	39
	CLKOUT+/CLKOUTB	40

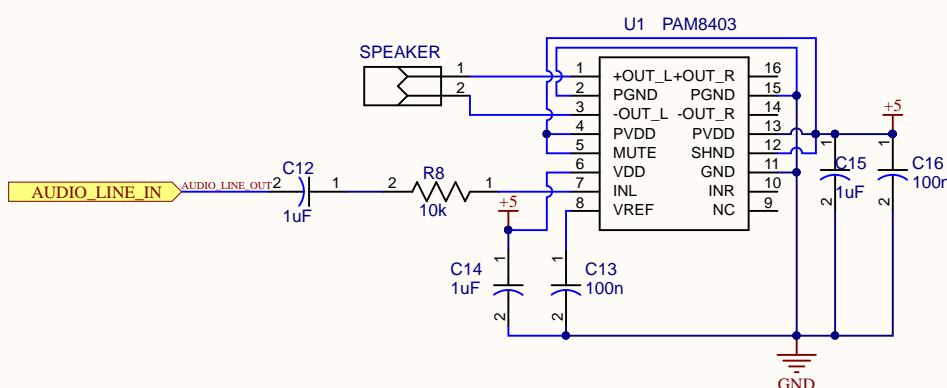
Title **ADC**

Size: A4 Number:3 Revision:2.0

Date: 09.11.2020 Time: 20:27:01 Sheet 3 of 18

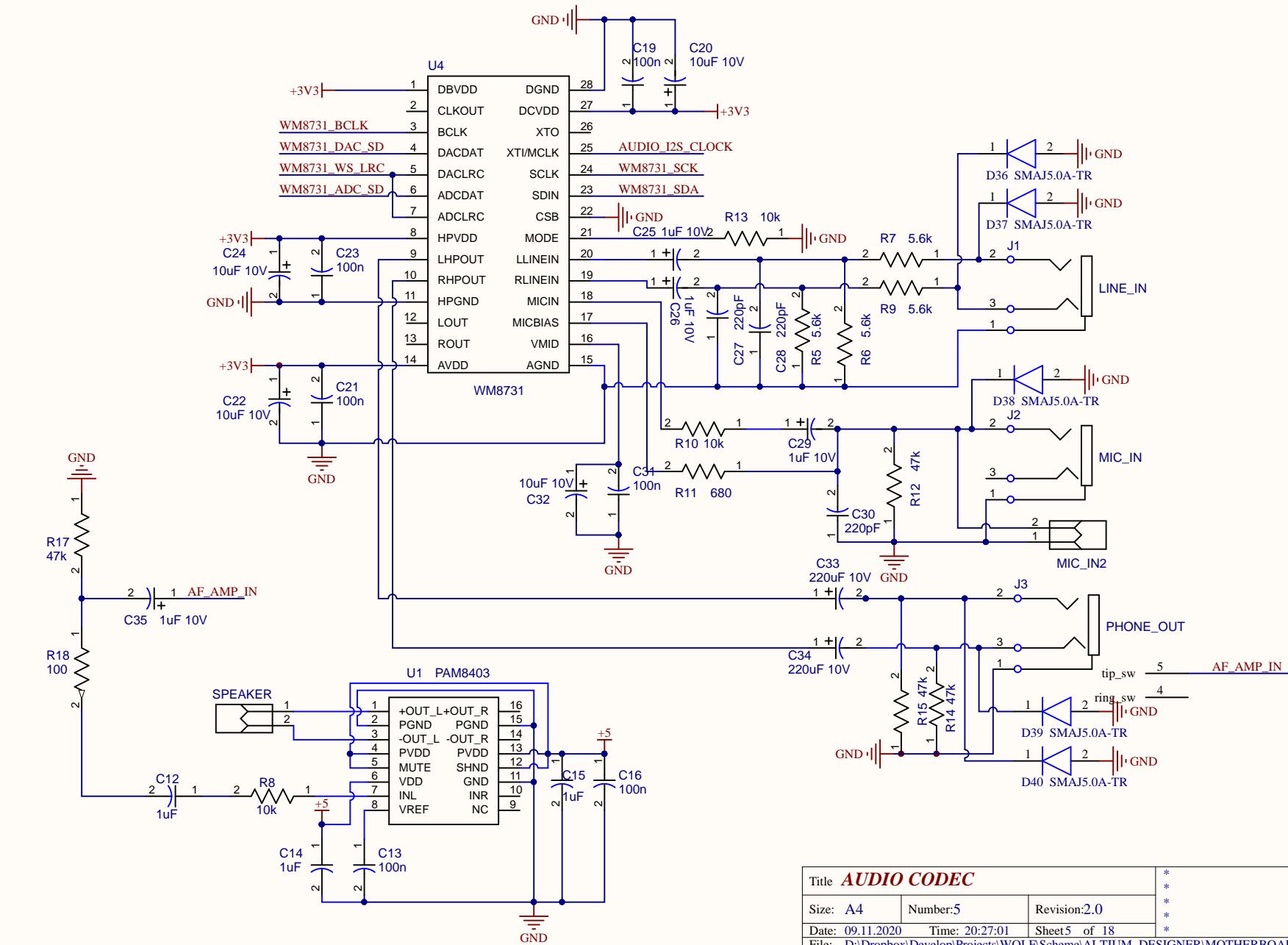
File: D:\Dropbox\Develop\Projects\WOLF\Scheme\ALTIUM_DESIGNER\MOTHERBOARD\ADC.SchDoc

Altium



Title AF AMP			* UA3REO
Size: A4	Number:4	Revision:2.0	BH8CGJ
Date: 09.11.2020	Time: 20:27:01	Sheet 4 of 18	*
File: D:\Dropbox\Develop\Projects\WOLF\Scheme\ALTIUM_DESIGNER\MOTHERBOARD\AF AMP.SchDoc			Altium

A

Title **AUDIO CODEC**

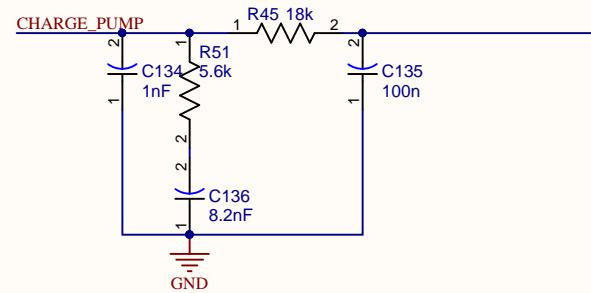
Size: A4 Number:5 Revision:2.0

Date: 09.11.2020 Time: 20:27:01 Sheet 5 of 18

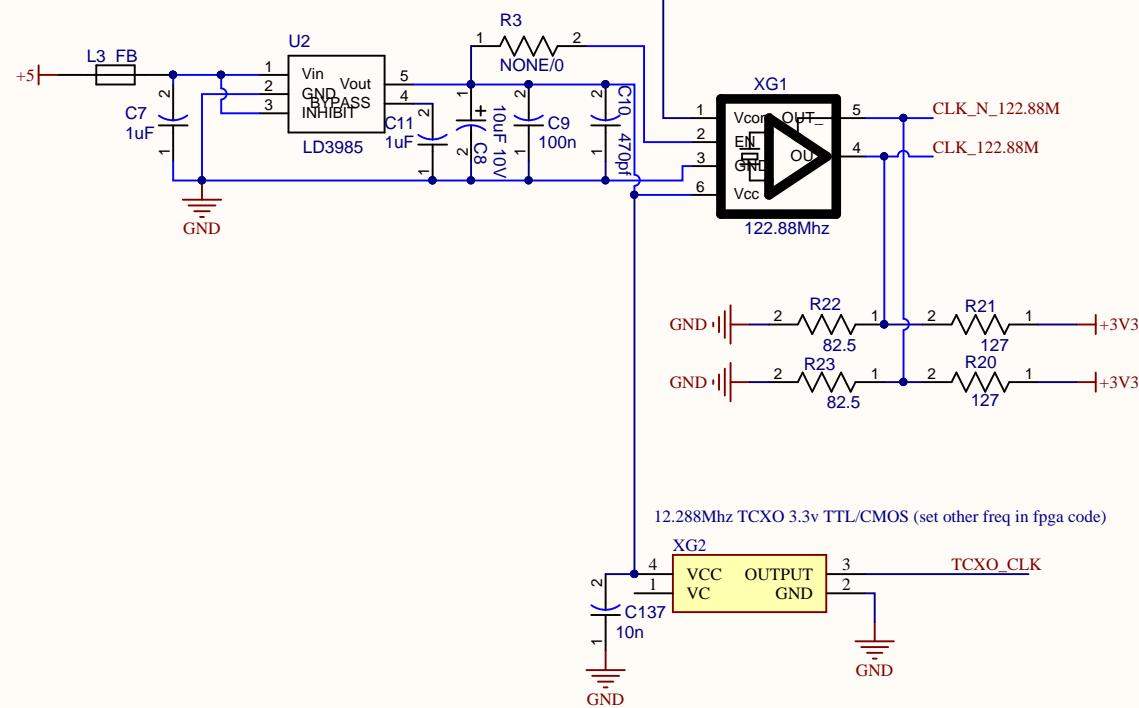
File: D:\Dropbox\Develop\Projects\WOLF\Scheme\ALTIUM_DESIGNER\MOTHERBOARD\AUDIO_CODEC.SchDoc

Altium

A



B



C

D

Title **CLOCK_GENERATOR**Size: **A4** Number:**6** Revision:**2.0**Date: **09.11.2020** Time: **20:27:01** Sheet**6** of **18**File: **D:\Dropbox\Develop\Projects\WOLF\Scheme\ALTIUM_DESIGNER\MOTHERBOARD\CLOCK_GENERATOR.SchDoc****Altium**

A

B

C

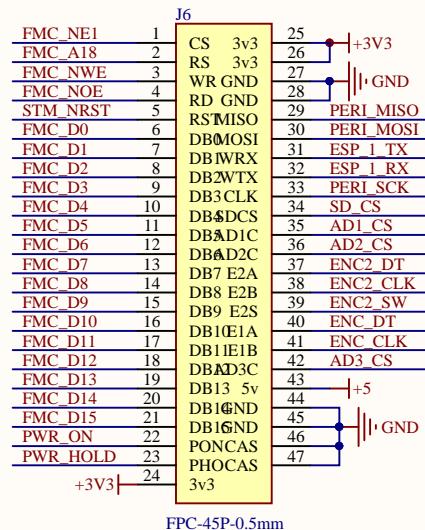
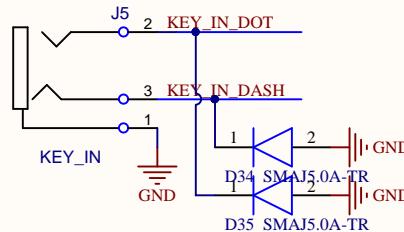
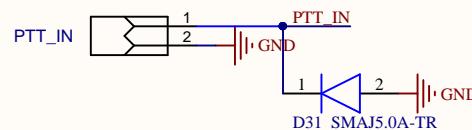
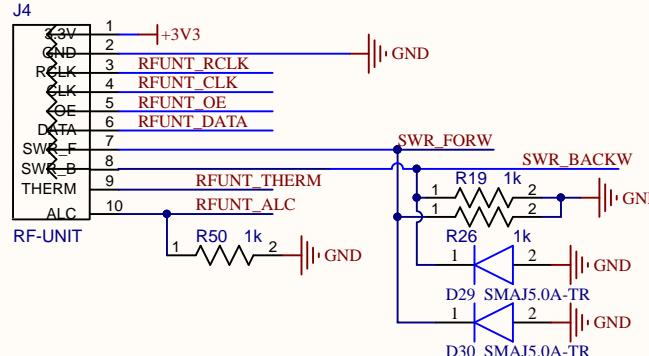
D

A

B

C

D

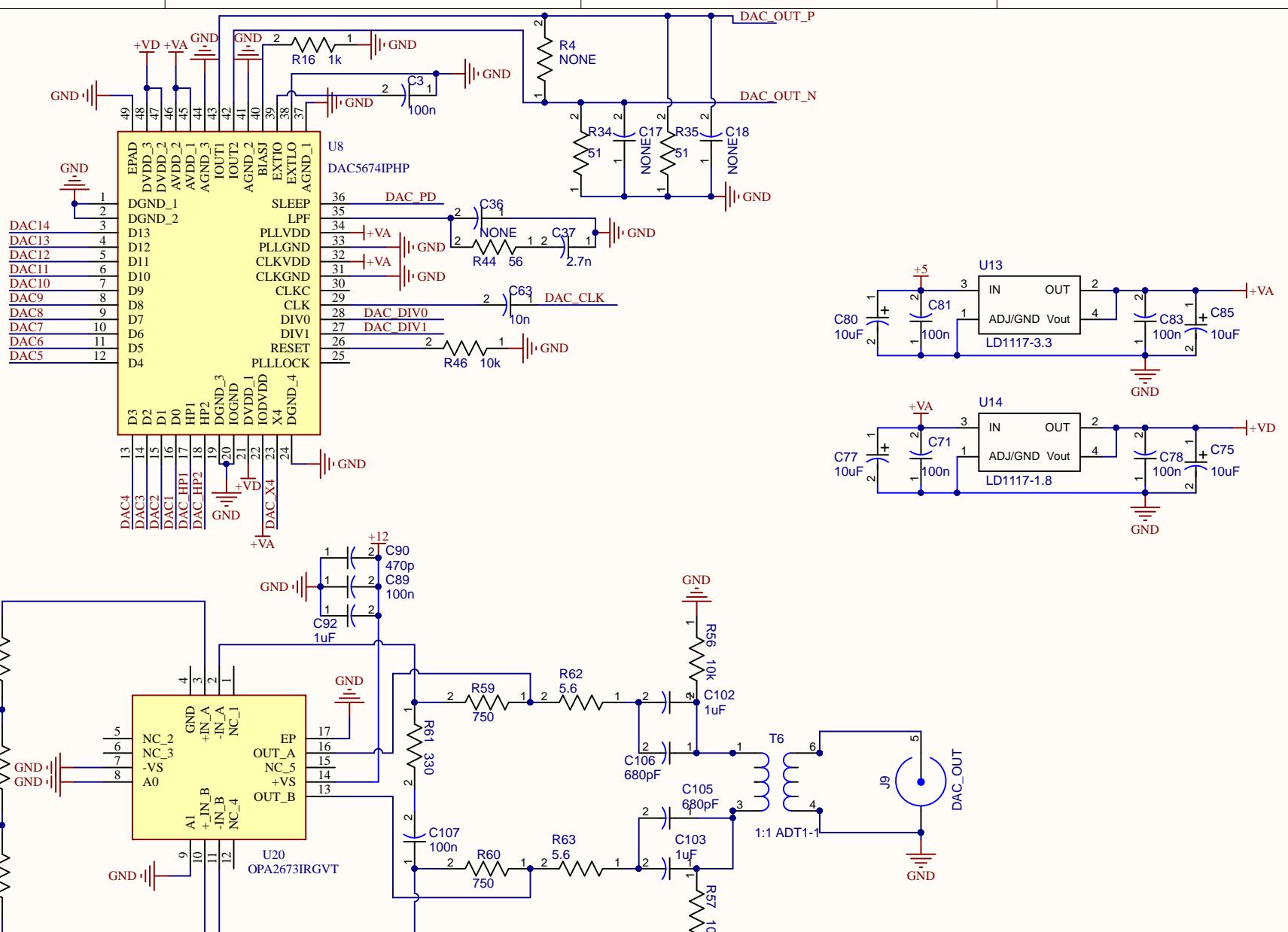
Title **CONNECTIONS**

Size: A4 Number: 7 Revision: 2.0

Date: 09.11.2020 Time: 20:27:01 Sheet 7 of 18

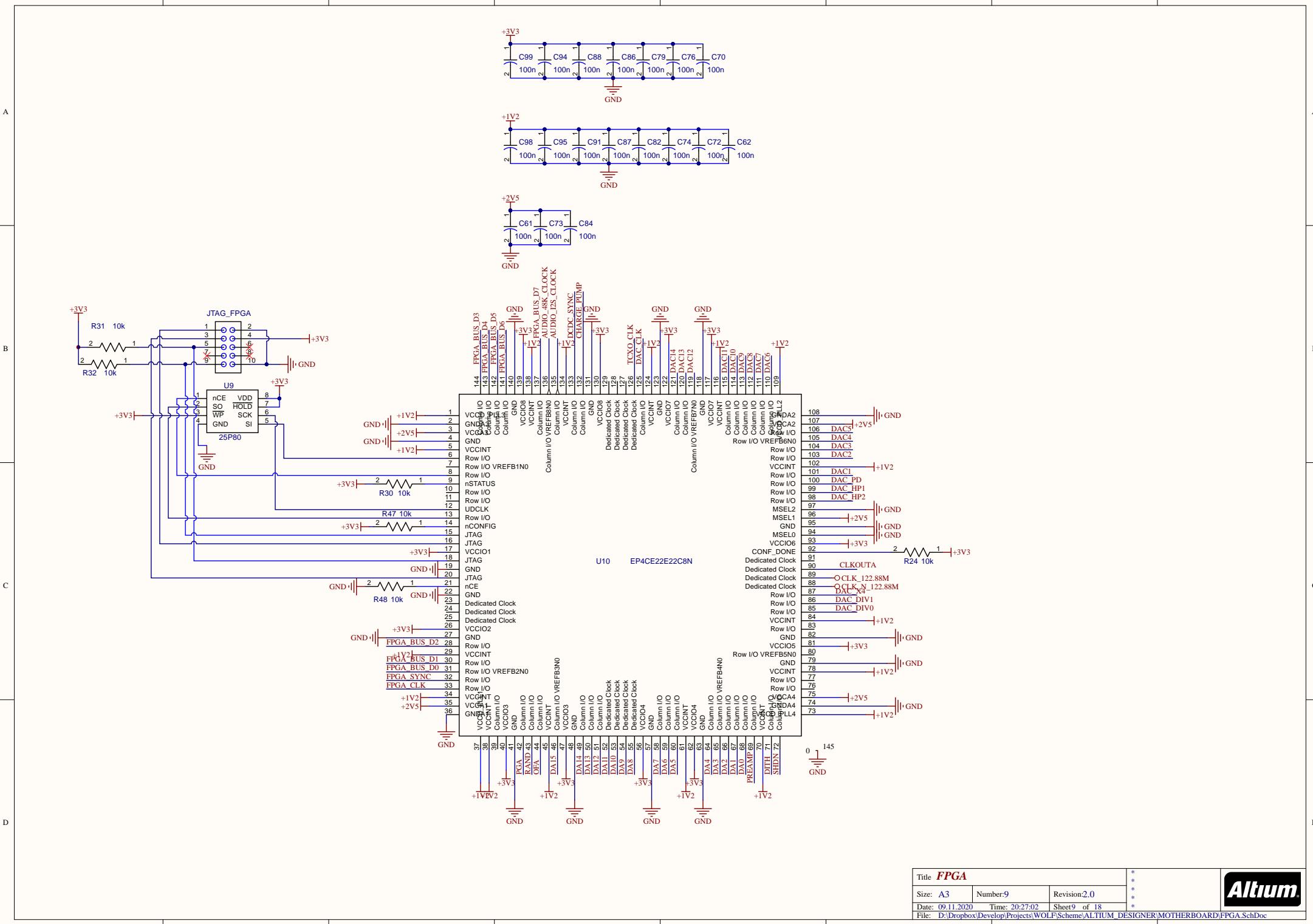
File: D:\Dropbox\Develop\Projects\WOLF\Scheme\ALTIUM_DESIGNER\MOTHERBOARD\CONNECTIONS.SchDoc

Altium



Title DAC		
Size: A4	Number: 8	Revision: 2.0
Date: 09.11.2020	Time: 20:27:01	Sheet 8 of 18
File: D:\Dropbox\Develop\Projects\WOLF\Scheme\ALTIUM_DESIGNER\MOTHERBOARD\DAC.SchDoc	*	*

Altium

Title **FPGA**

Size: A3

Number: 9

Revision: 2.0

Date: 09.11.2020

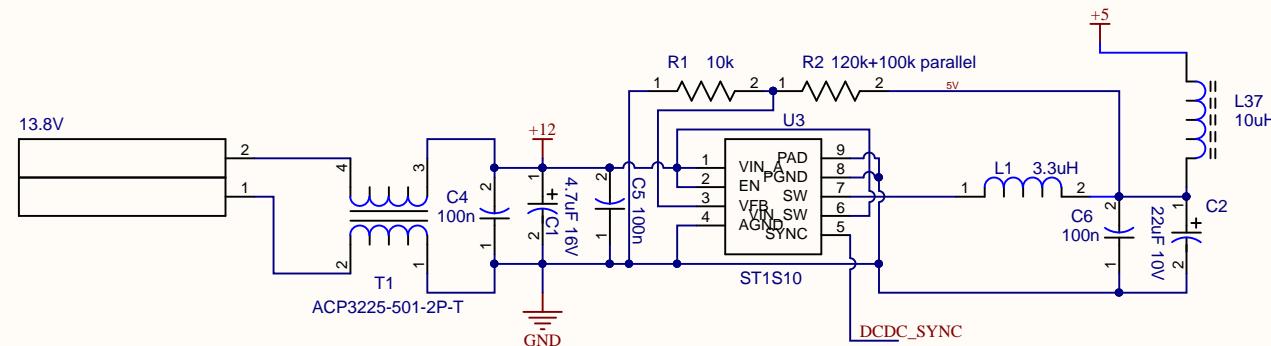
Time: 20:27:02

Sheet: 9 of 18

File: D:\Dropbox\Develop\Projects\WOLF\Scheme\ALTIUM DESIGNER\MOTHERBOARD\FPGA.SchDoc

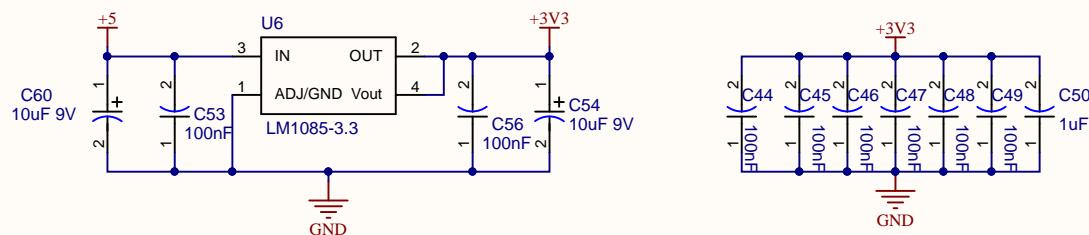


A



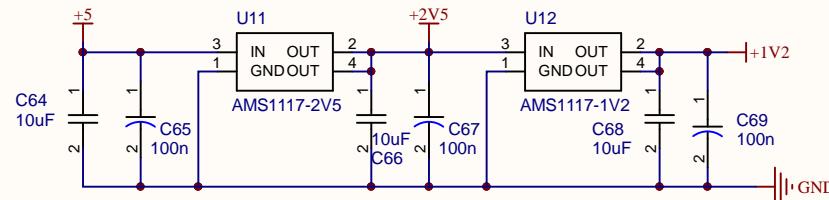
A

B



B

C



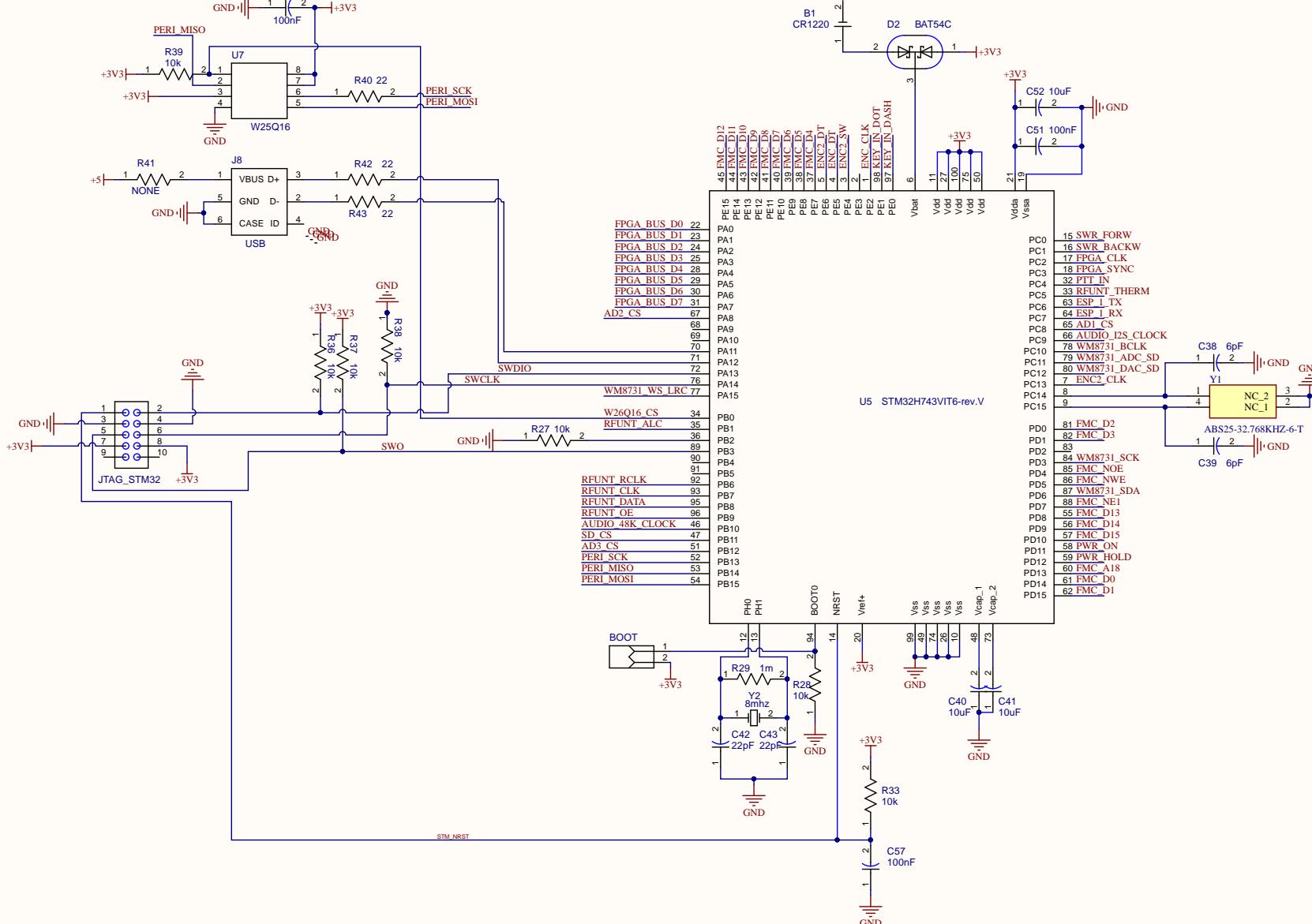
C

D

Title POWER		
Size: A4	Number: 10	Revision: 2.0
Date: 09.11.2020	Time: 20:27:02	Sheet 10 of 18
File: D:\Dropbox\Develop\Projects\WOLF\Scheme\ALTIUM_DESIGNER\MOTHERBOARD\POWER.SchDoc	*	*



STM32

Title **STM32**

Size: A3 Number:11 Revision:2.0

Date: 09.11.2020 Time: 20:27:02 Sheet 11 of 18

File: D:\Dropbox\Develop Projects\WOLF\Scheme\ALTIUM DESIGNER\MOTHERBOARD\STM32.SchDoc



A

A

B

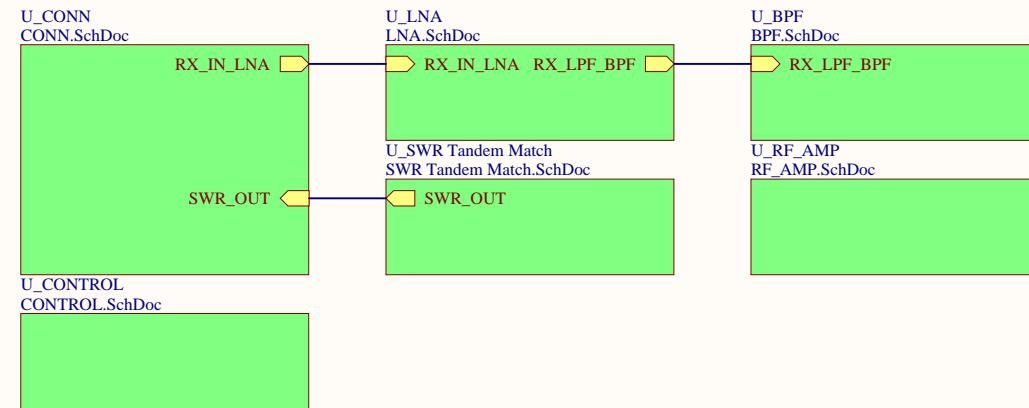
B

C

C

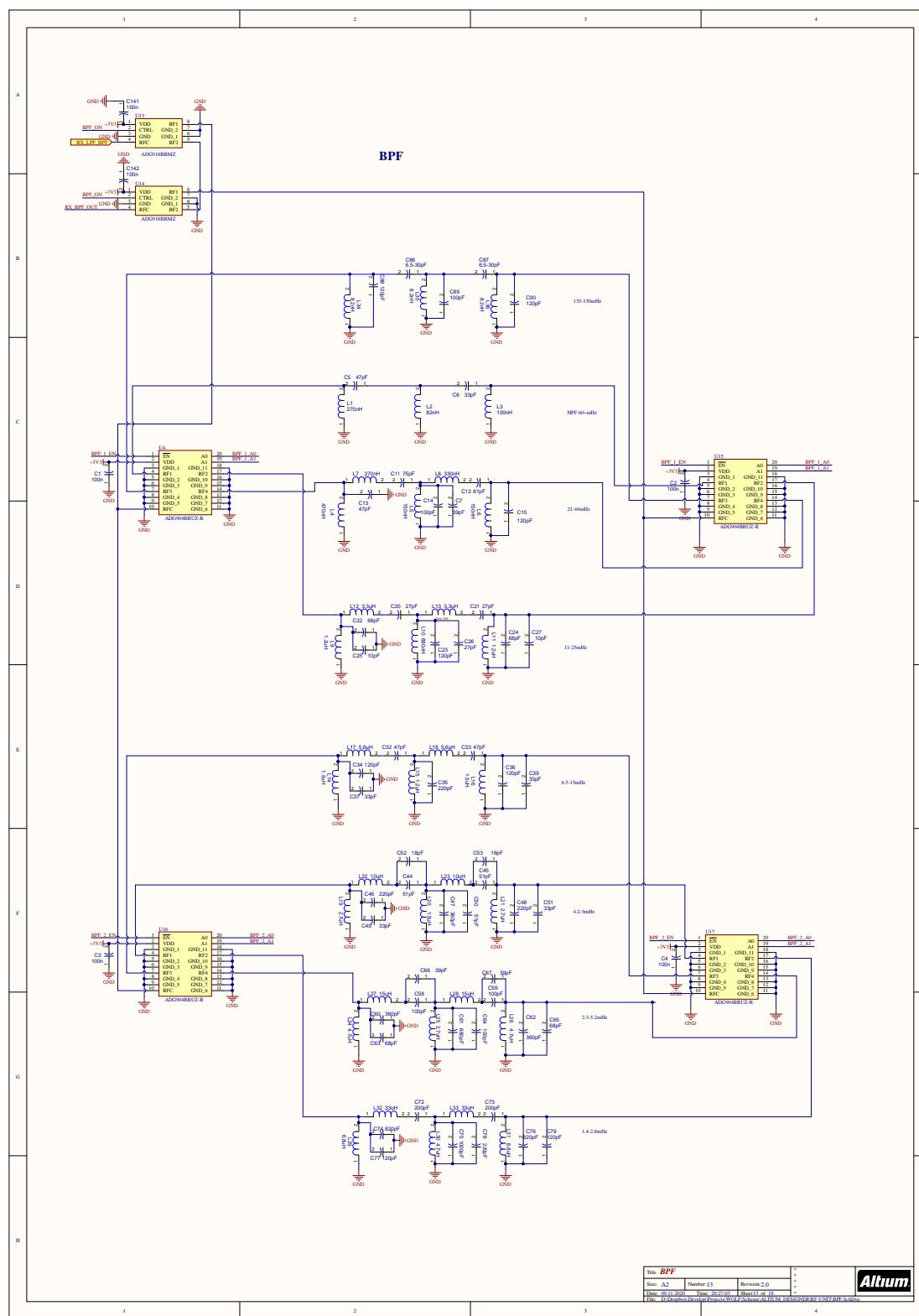
D

D



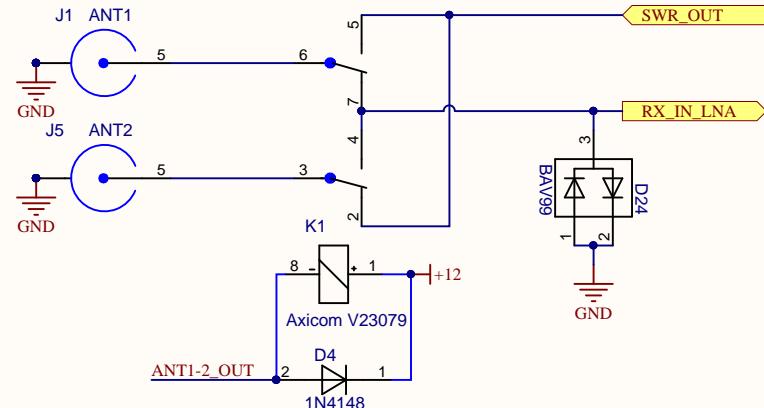
Title RF-UNIT			*
Size: A4	Number:12	Revision:2.0	*
Date: 09.11.2020	Time: 20:27:02	Sheet 12 of 18	*
File: D:\Dropbox\Develop\Projects\WOLF\Scheme\ALTIUM_DESIGNER\RF-UNIT\RF-UNIT.SCHDOC			*

Altium



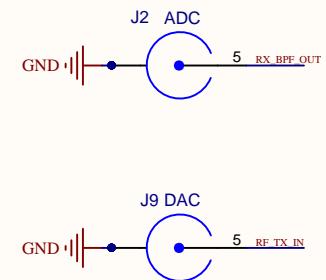
A

TXRX_COMUTATOR

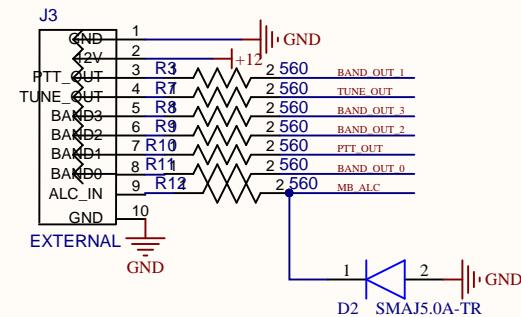
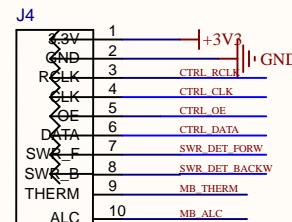


B

CONN



C



D

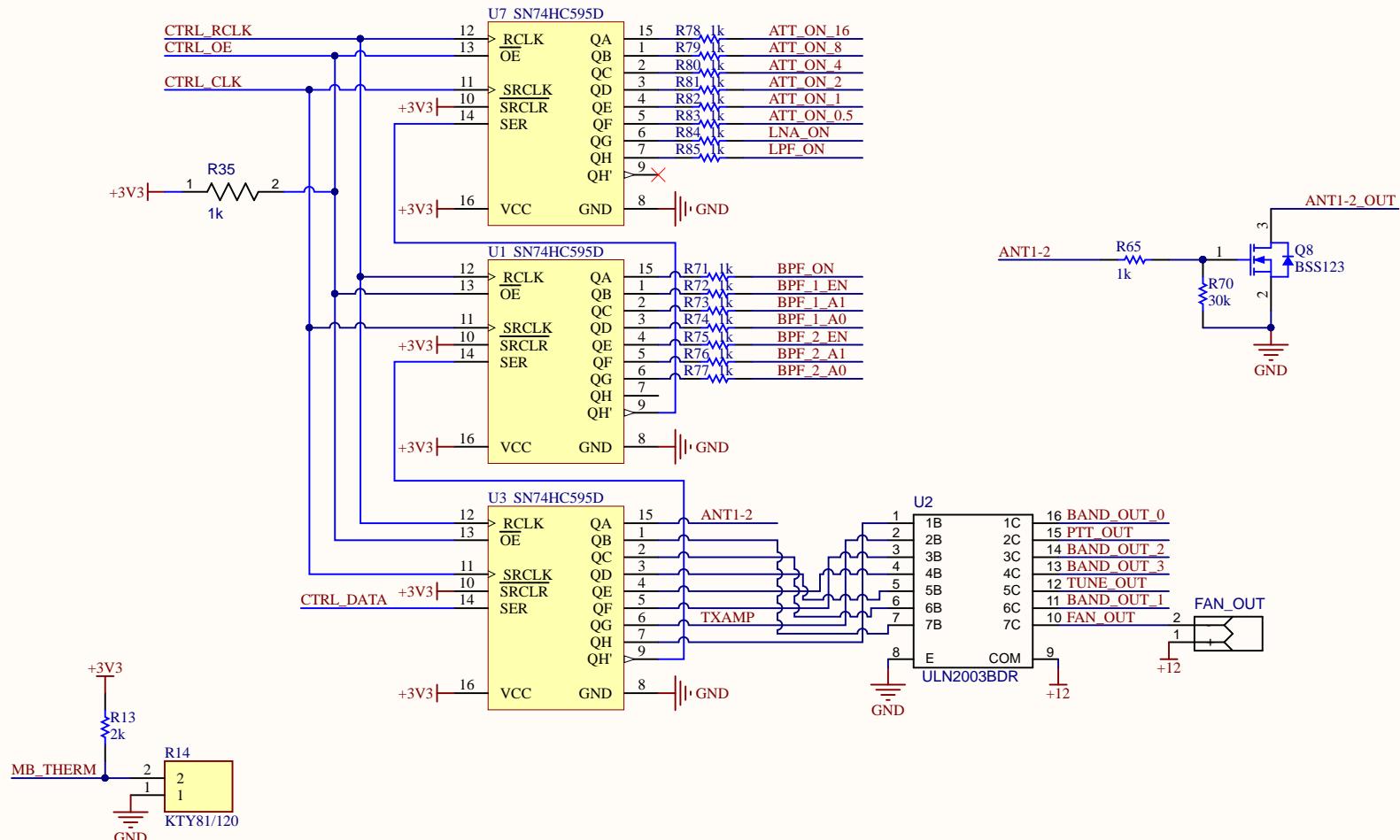
Title **CONN**

Size: A4 Number:14 Revision:2.0

Date: 09.11.2020 Time: 20:27:03 Sheet 14 of 18

File: D:\Dropbox\Develop\Projects\WOLF\Scheme\ALTIUM_DESIGNER\RF-UNIT\CONN.SchDoc

A

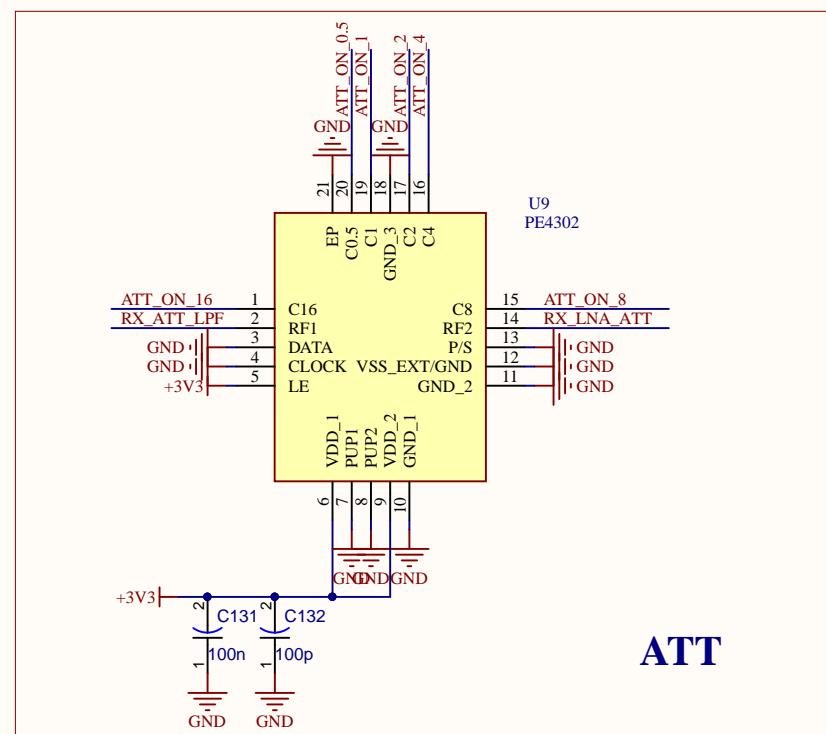
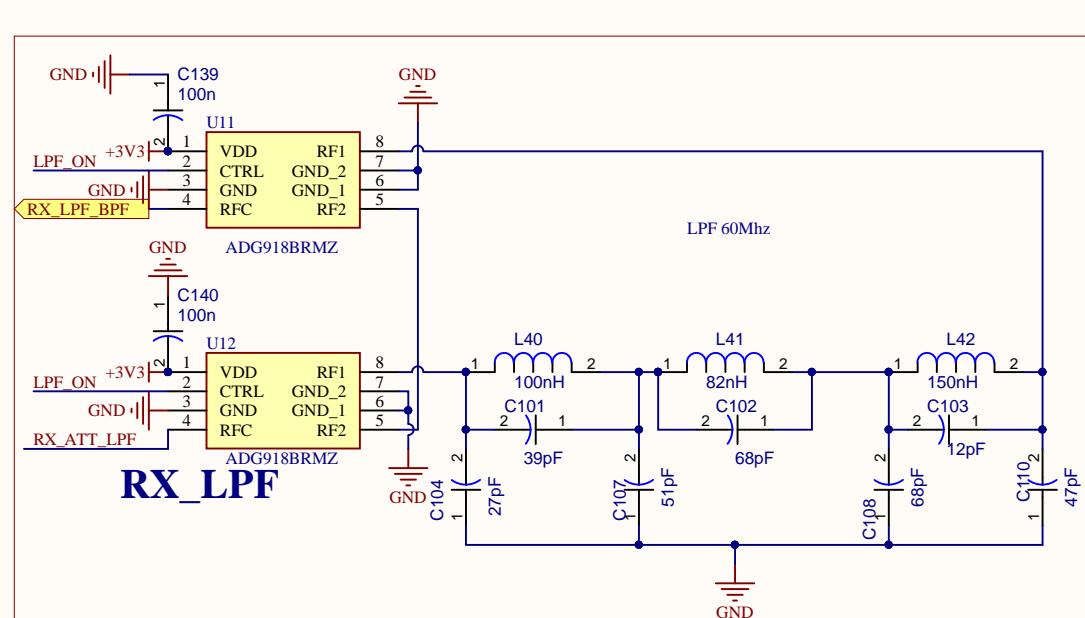
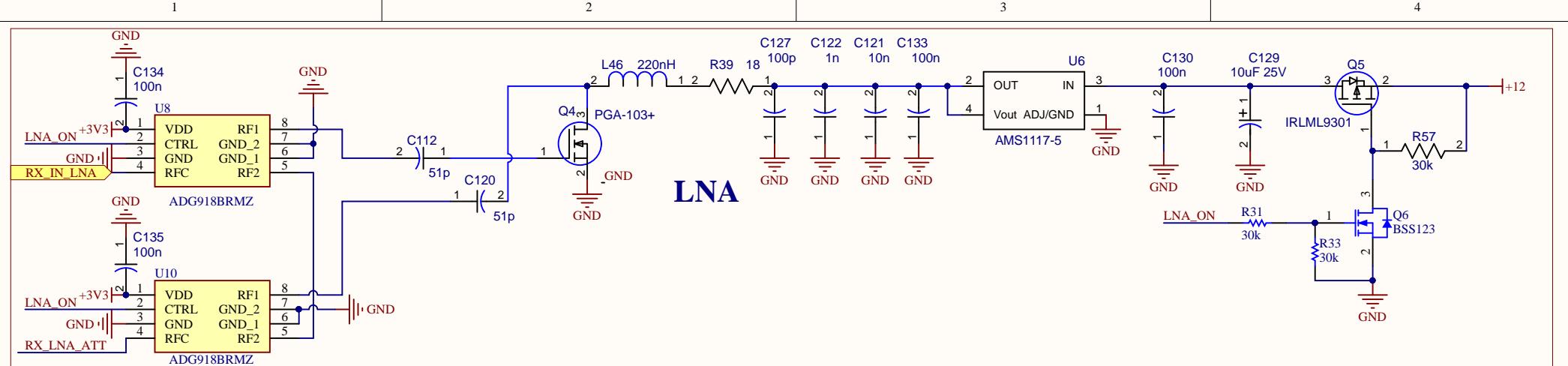
Title **CONTROL**

Size: A4 Number:15 Revision:2.0

Date: 09.11.2020 Time: 20:27:03 Sheet 15 of 18

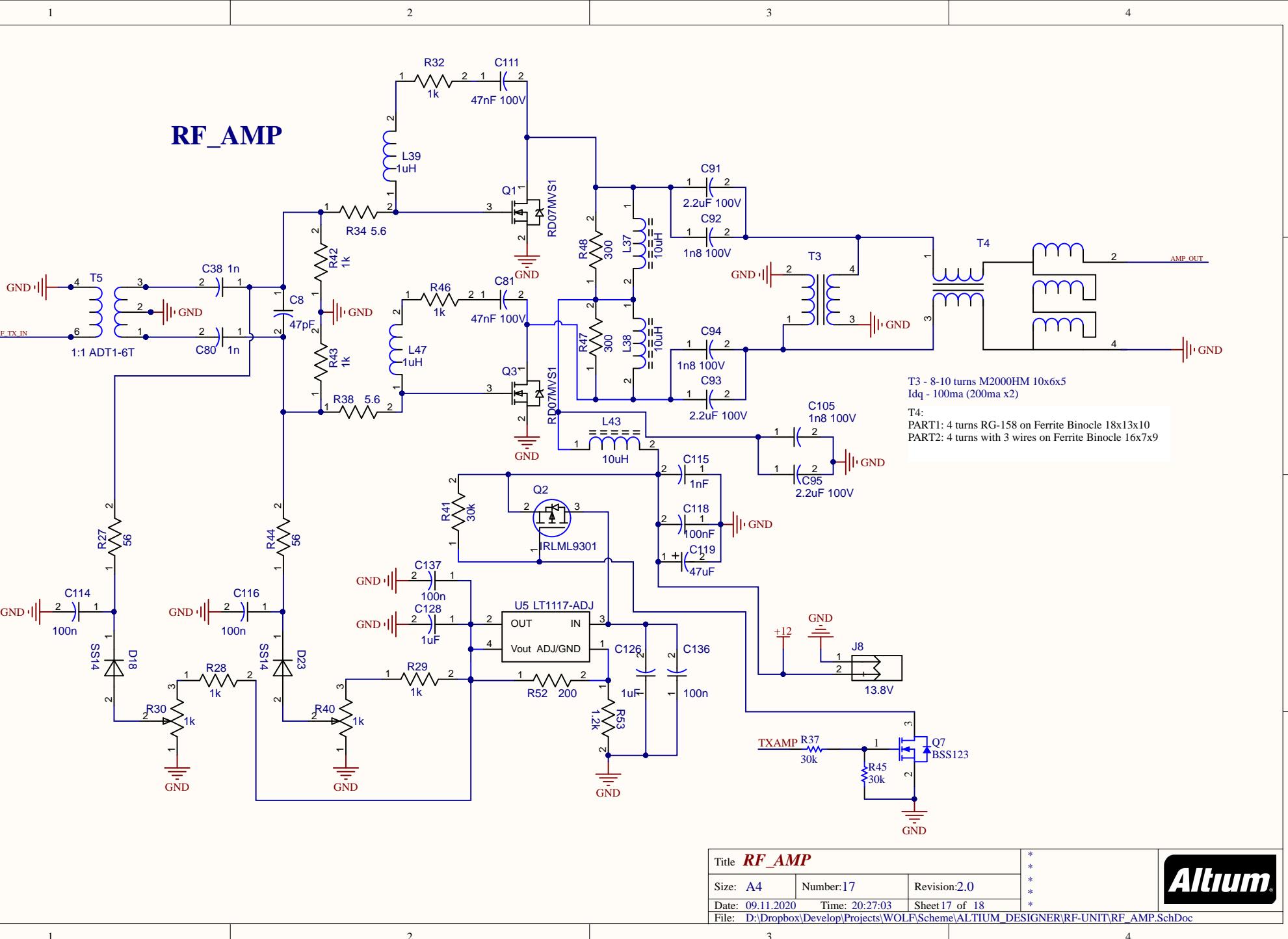
File: D:\Dropbox\Develop\Projects\WOLF\Scheme\ALTIUM_DESIGNER\RF-UNIT\CONTROL.SchDoc

Altium



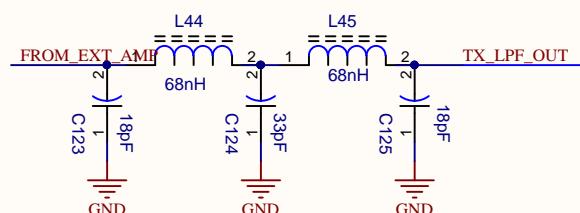
Title LNA			*	*
Size: A4	Number: 16	Revision: 2.0	*	*
Date: 09.11.2020	Time: 20:27:03	Sheet 16 of 18	*	*
File: D:\Dropbox\Develop\Projects\WOLF\Scheme\ALTIUM_DESIGNER\RF-UNIT\LNA.SchDoc			*	

Altium

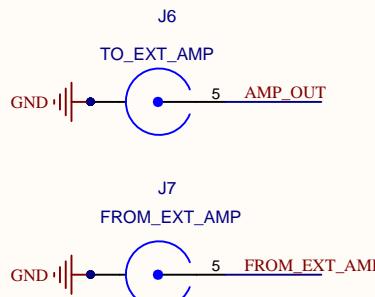
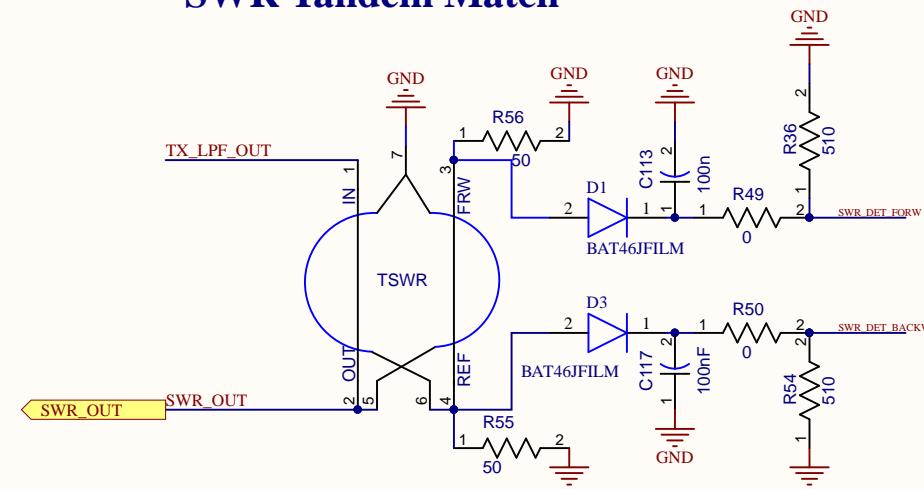


TX_LPF

LPF 170Mhz



Катушки намотаны проводом 0.5мм на оправке диаметром 5мм, 3.5 витка

**SWR Tandem Match**Title ***SWR Tandem Match***

Size: A4 Number:18 Revision:2.0

Date: 09.11.2020 Time: 20:27:04 Sheet 18 of 18

File: D:\Dropbox\Develop\Projects\WOLF\Scheme\ALTIUM_DESIGNER\RF-UNIT\SWR Tandem Match.SchDoc

Altium