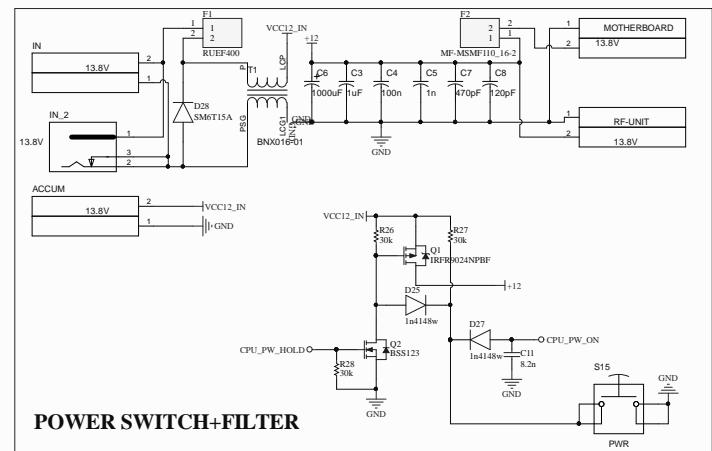
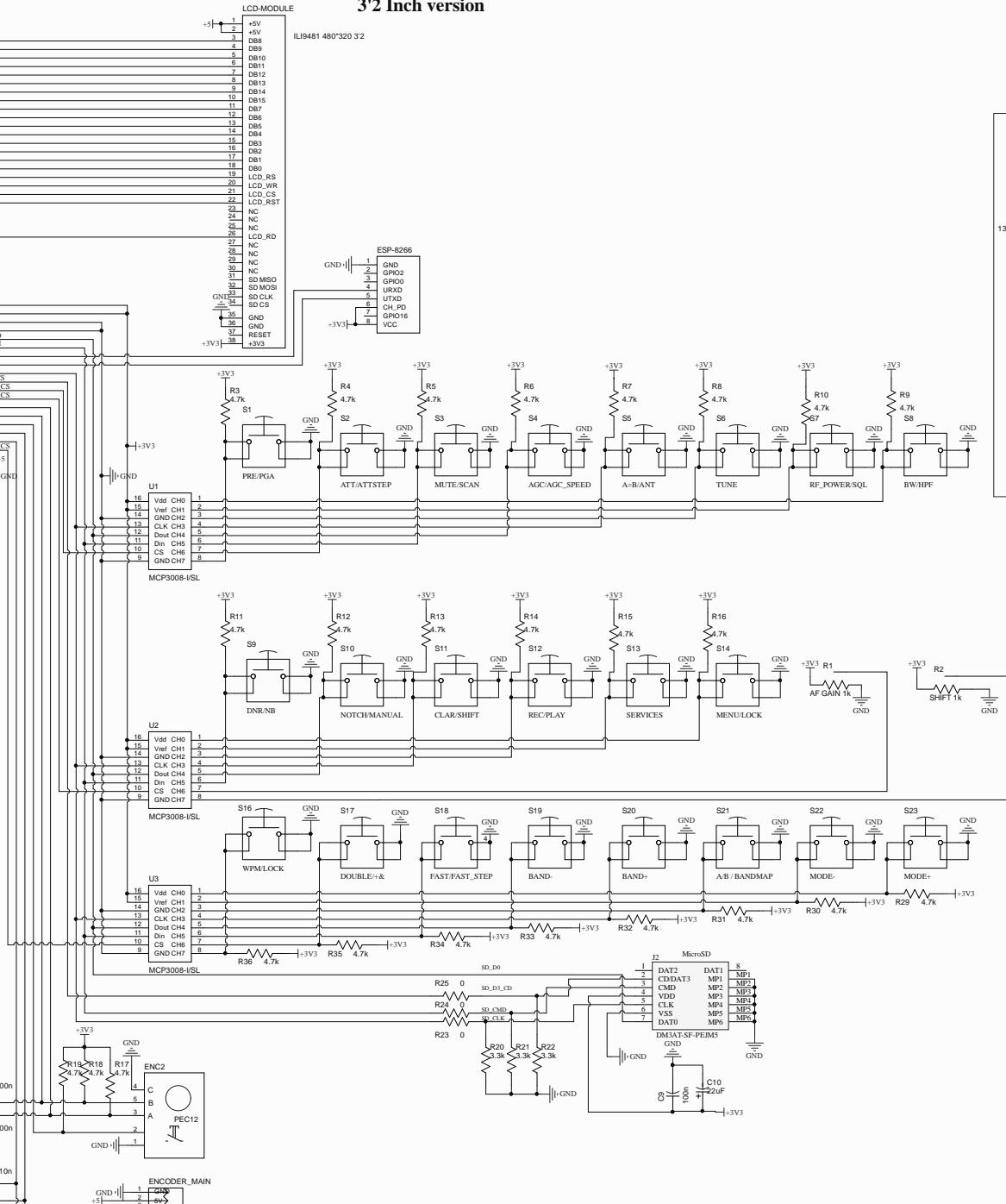


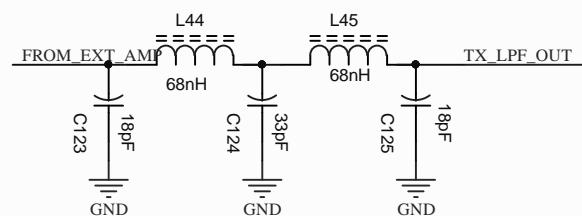
3'2 Inch version



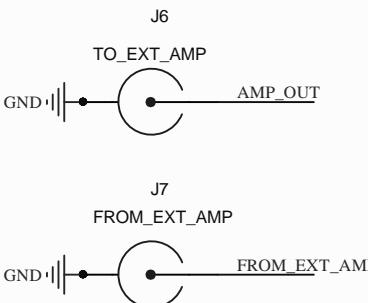
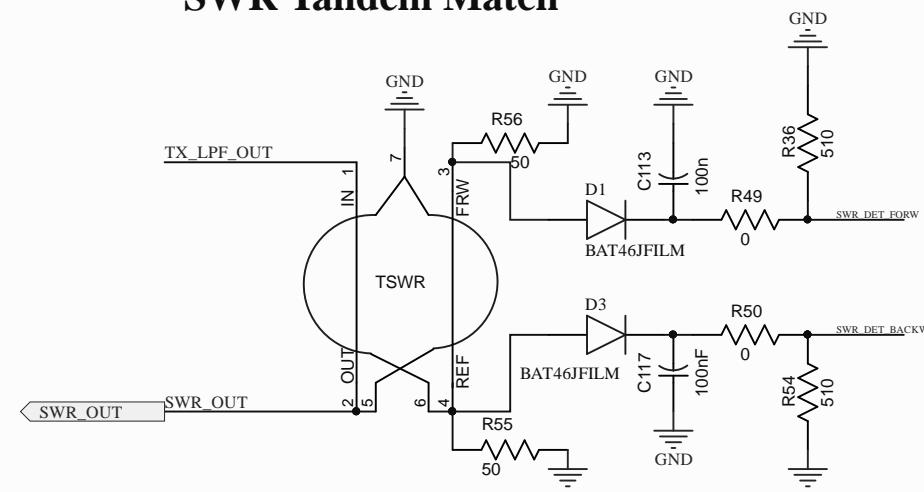
## POWER SWITCH+FILTER

**TX\_LPF**

LPF 170Mhz



Катушки намотаны проводом 0.5мм на оправке диаметром 5мм, 3.5 витка

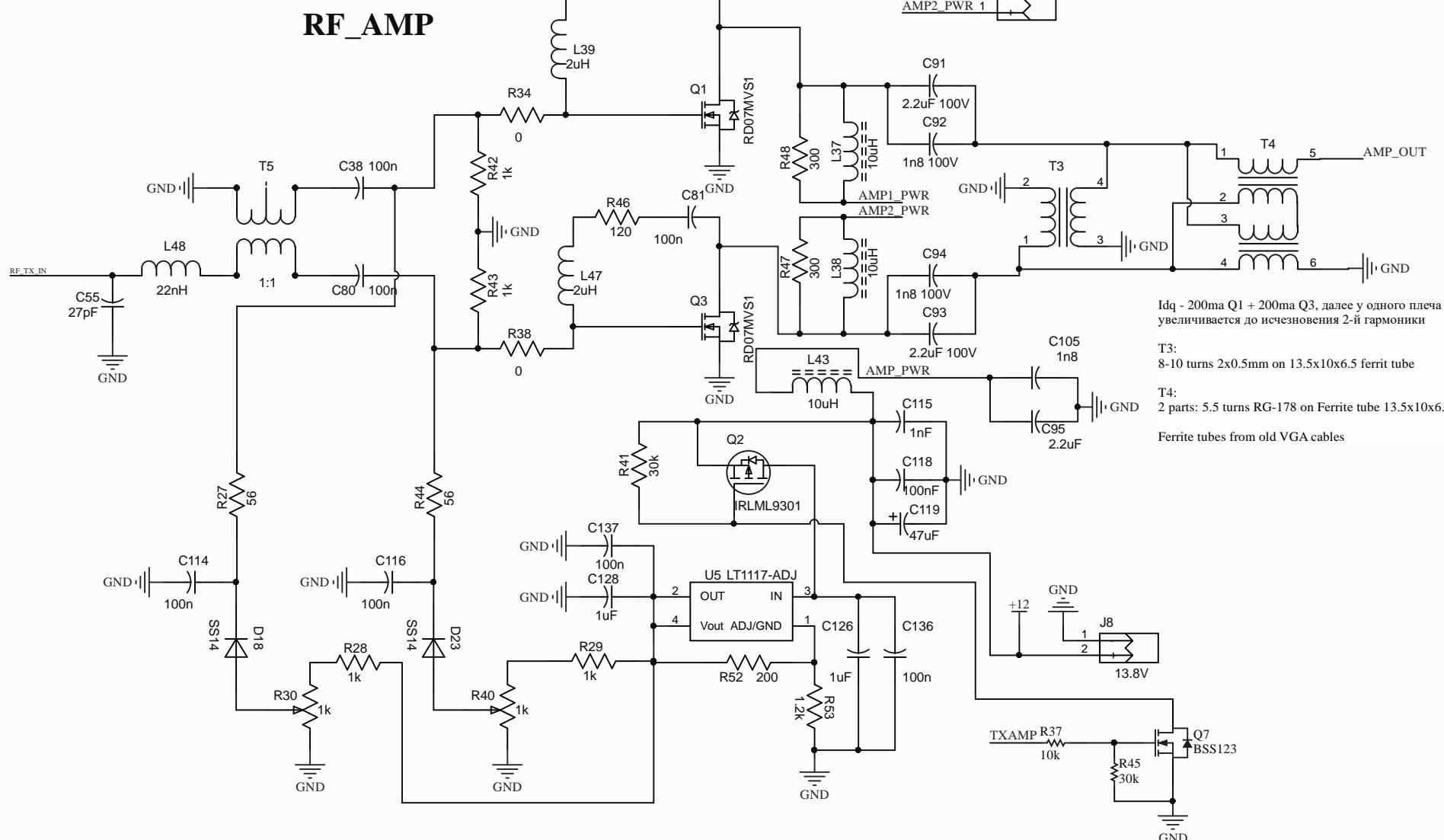
**SWR Tandem Match**Title **SWR Tandem Match**

Size: A4 Number:18 Revision:2.0

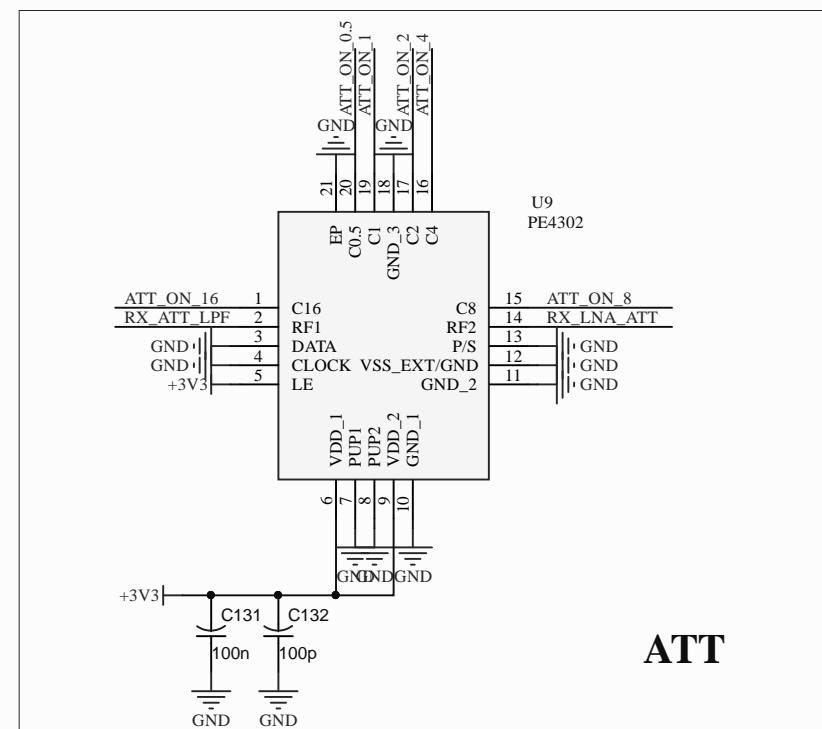
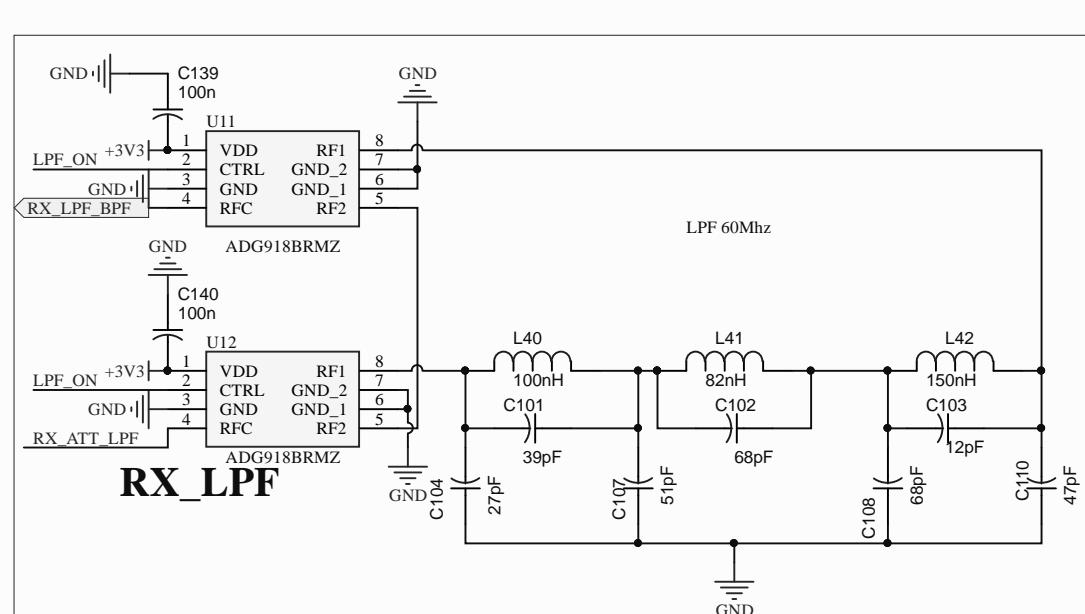
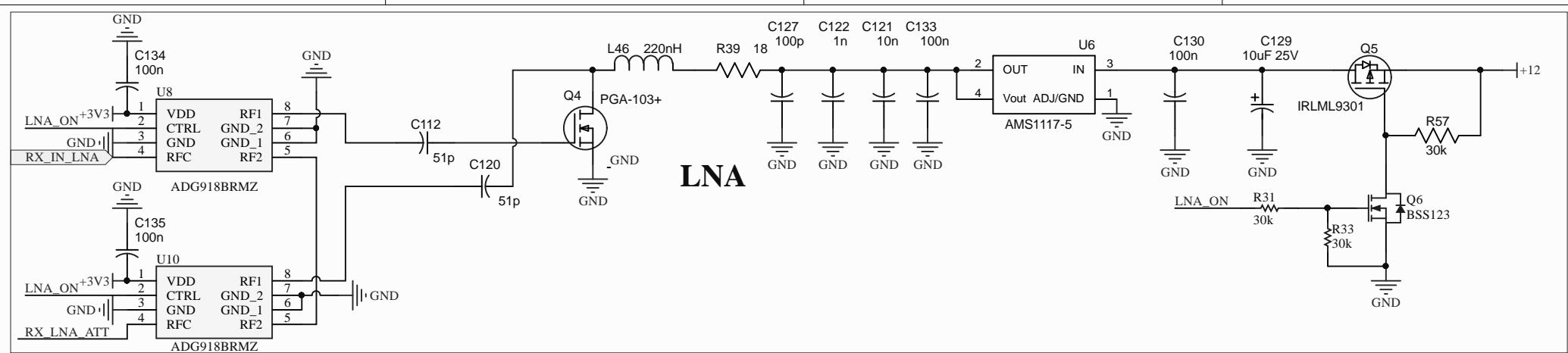
Date: 18.02.2021 Time: 19:30:56 Sheet:18 of 18

File: C:\Dropbox\Develop\Projects\WOLF\Scheme\ALTIUM\_DESIGNER\RF-UNIT\SWR Tandem Match.SchDoc

A

**RF\_AMP**Title **RF\_AMP**

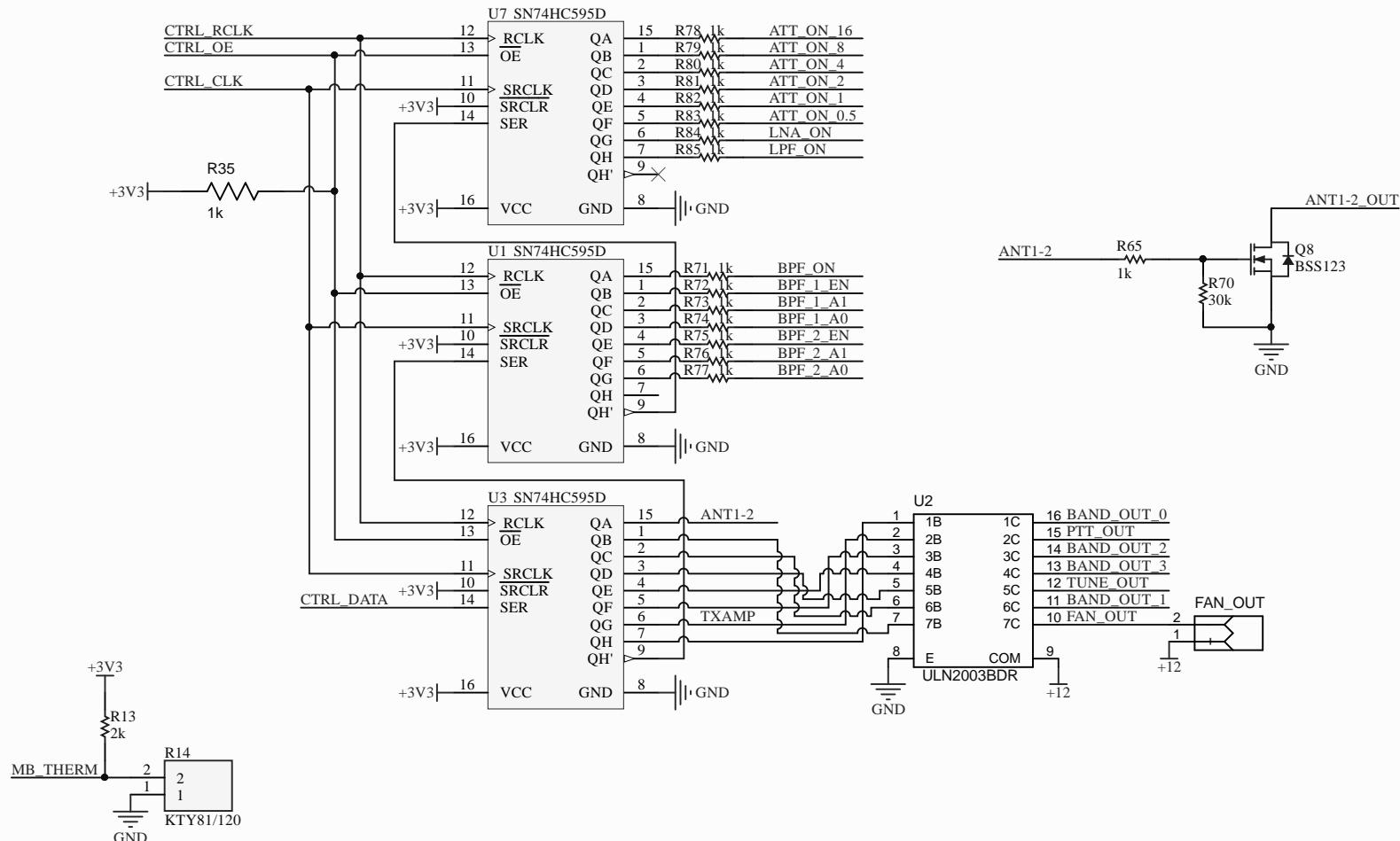
Size: A4	Number: 17	Revision 2.0
Date: 18.02.2021	Time: 19:30:58	Sheet 17 of 18
File: C:\Dropbox\Develop\Projects\WOLF\Schema\ALTIUM_DESIGNER\RF-UNIT\RF_AMP.SchDoc		*



Title <b>LNA</b>			*
Size: A4	Number:16	Revision2.0	*
Date: 18.02.2021	Time: 19:31:00	Sheet16 of 18	*
File: C:\Dropbox\Develop\Projects\WOLF\Scheme\ALTIUM_DESIGNER\RF-UNIT\LNA.SchDoc			

**Altium**

A

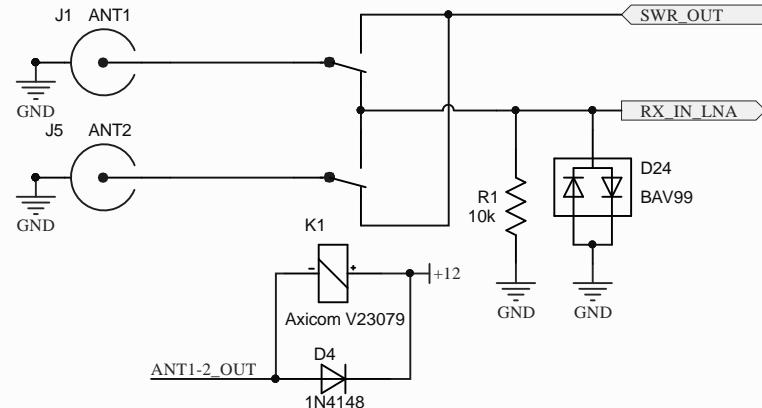
Title **CONTROL**

Size: A4	Number:15	Revision2.0
Date: 18.02.2021	Time: 19:31:02	Sheet15 of 18
File: C:\Dropbox\Develop\Projects\WOLF\Scheme\ALTIUM_DESIGNER\RF-UNIT\CONTROL.SchDoc		*

**Altium**

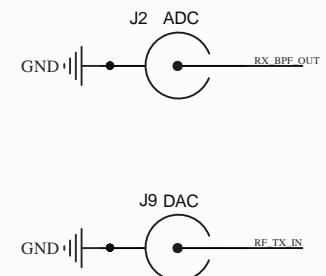
A

## TXRX\_COMUTATOR

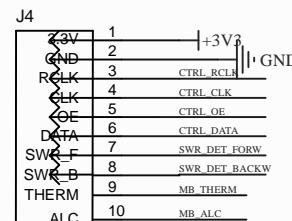


B

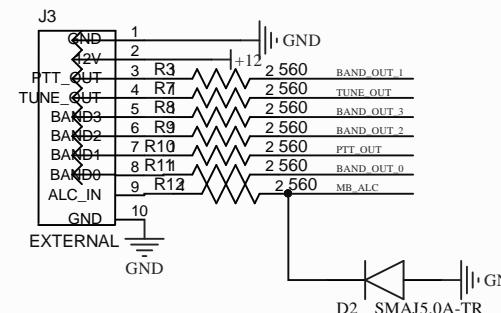
## CONN



C



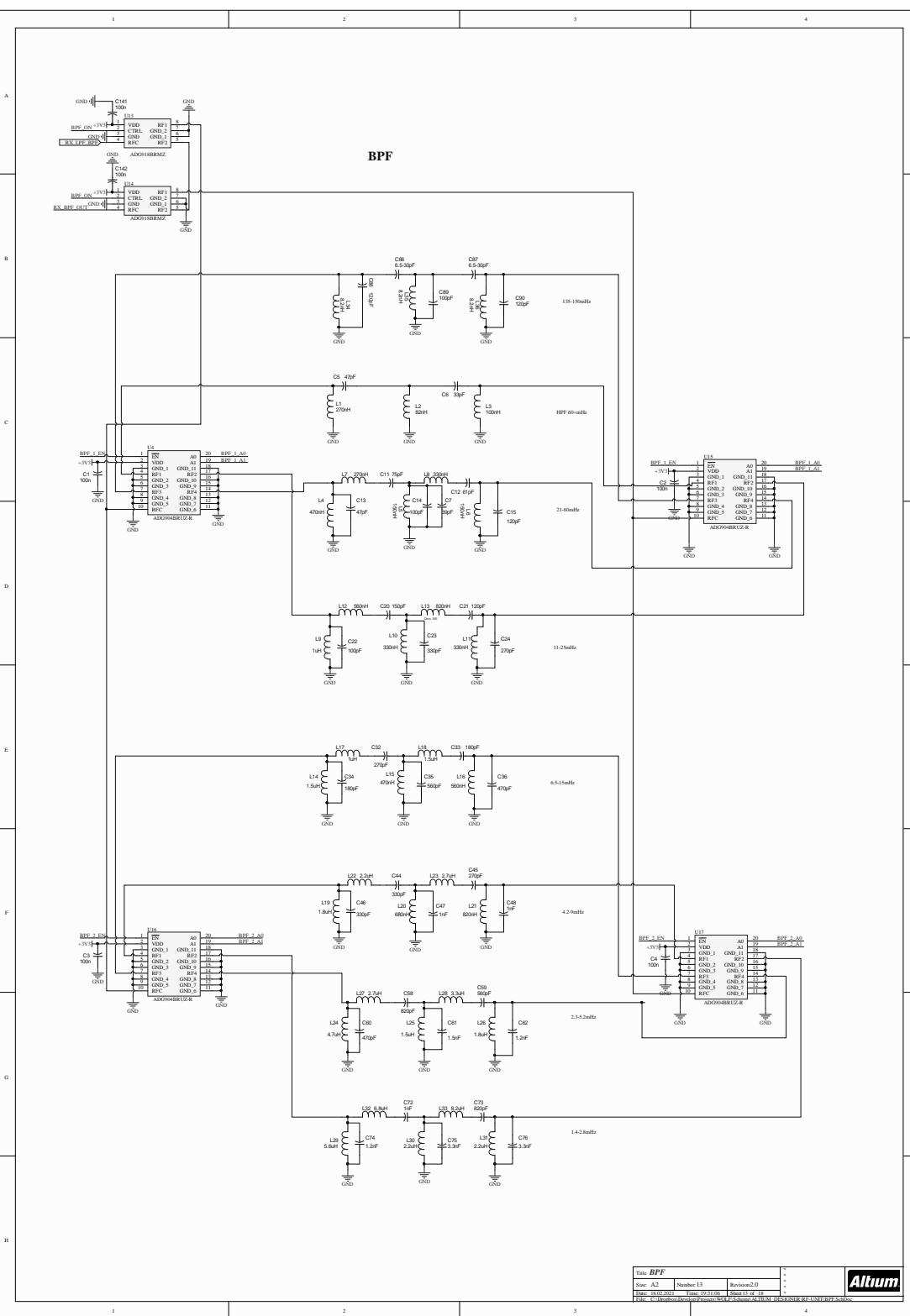
MOTHERBOARD



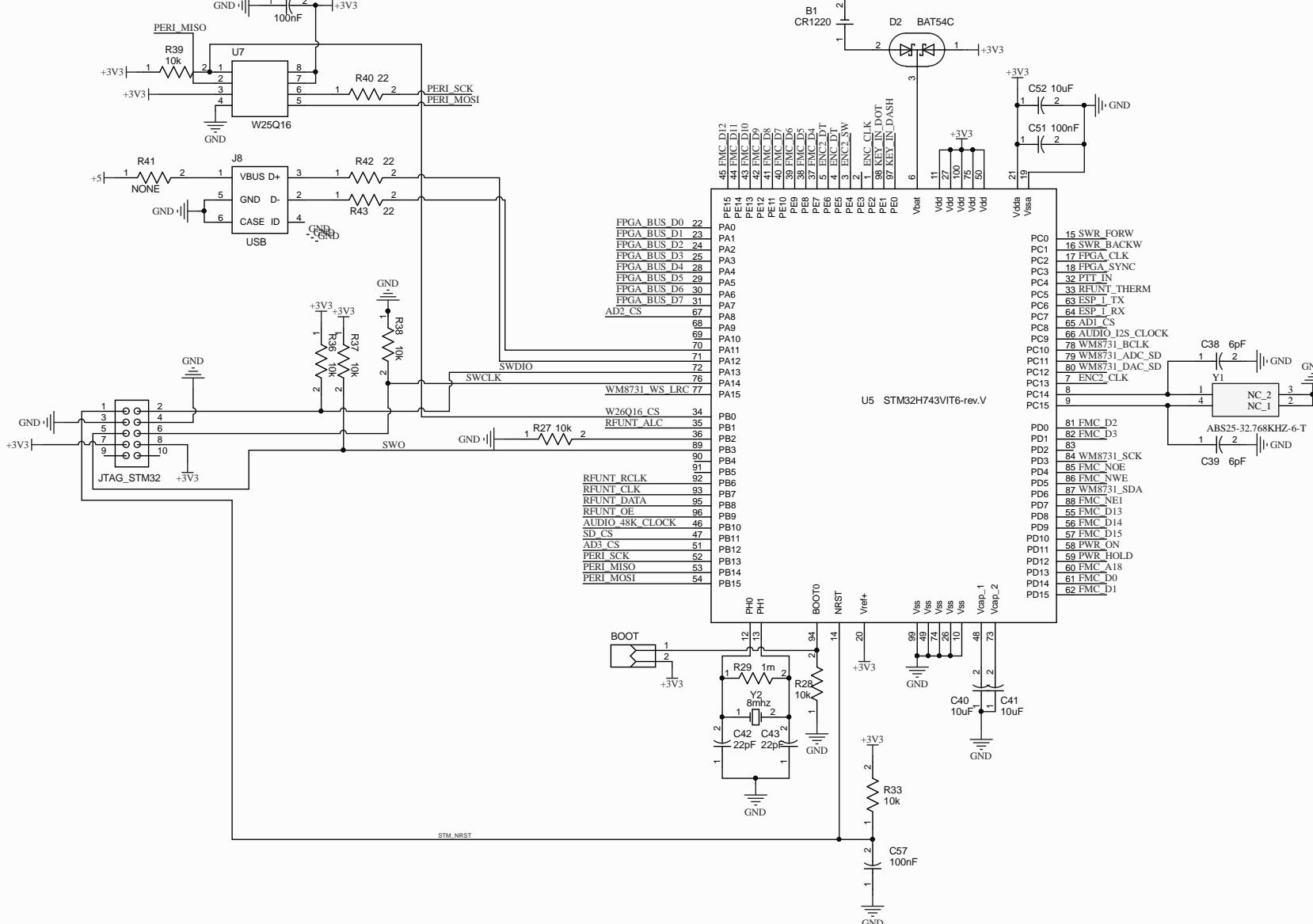
D

Title **CONN**

Size: A4	Number:14	Revision2.0
Date: 18.02.2021	Time: 19:31:04	Sheet14 of 18
File: C:\Dropbox\Develop\Projects\WOLF\Scheme\ALTIUM_DESIGNER\RF-UNIT\CONN.SchDoc		



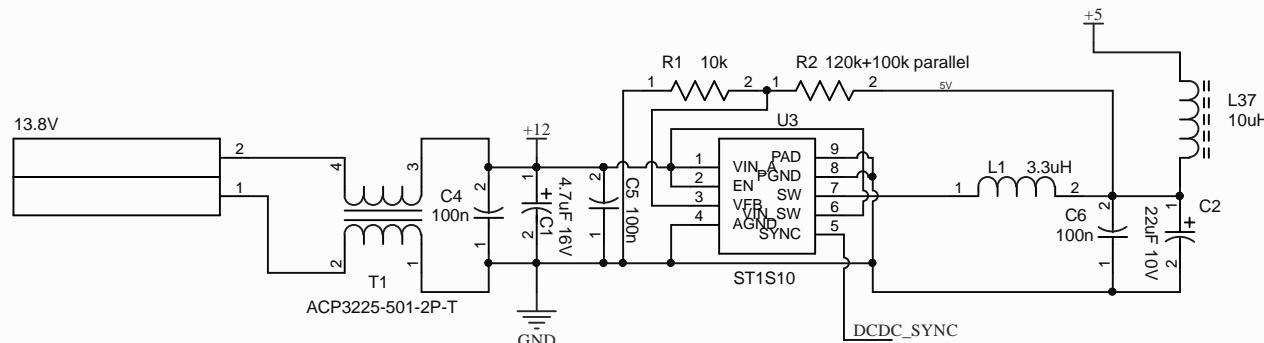
# STM32

Title **STM32**

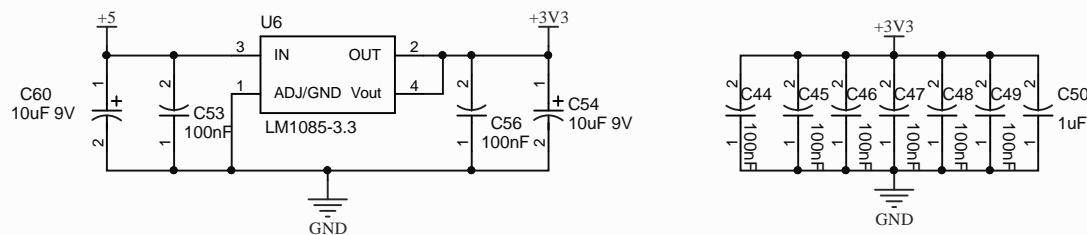
Size: A3	Number: 11	Revision: 2.0
Date: 18.02.2021	Time: 19:31:09	Sheet 11 of 18
File: C:\Dropbox\Develop\Projects\WOLF\Scheme\ALTIUM DESIGNER\MOTHERBOARD\STM32.SchDoc		



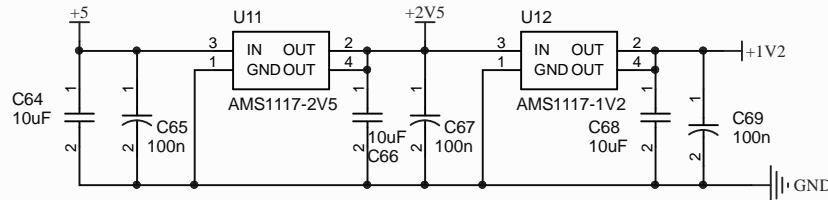
A



B



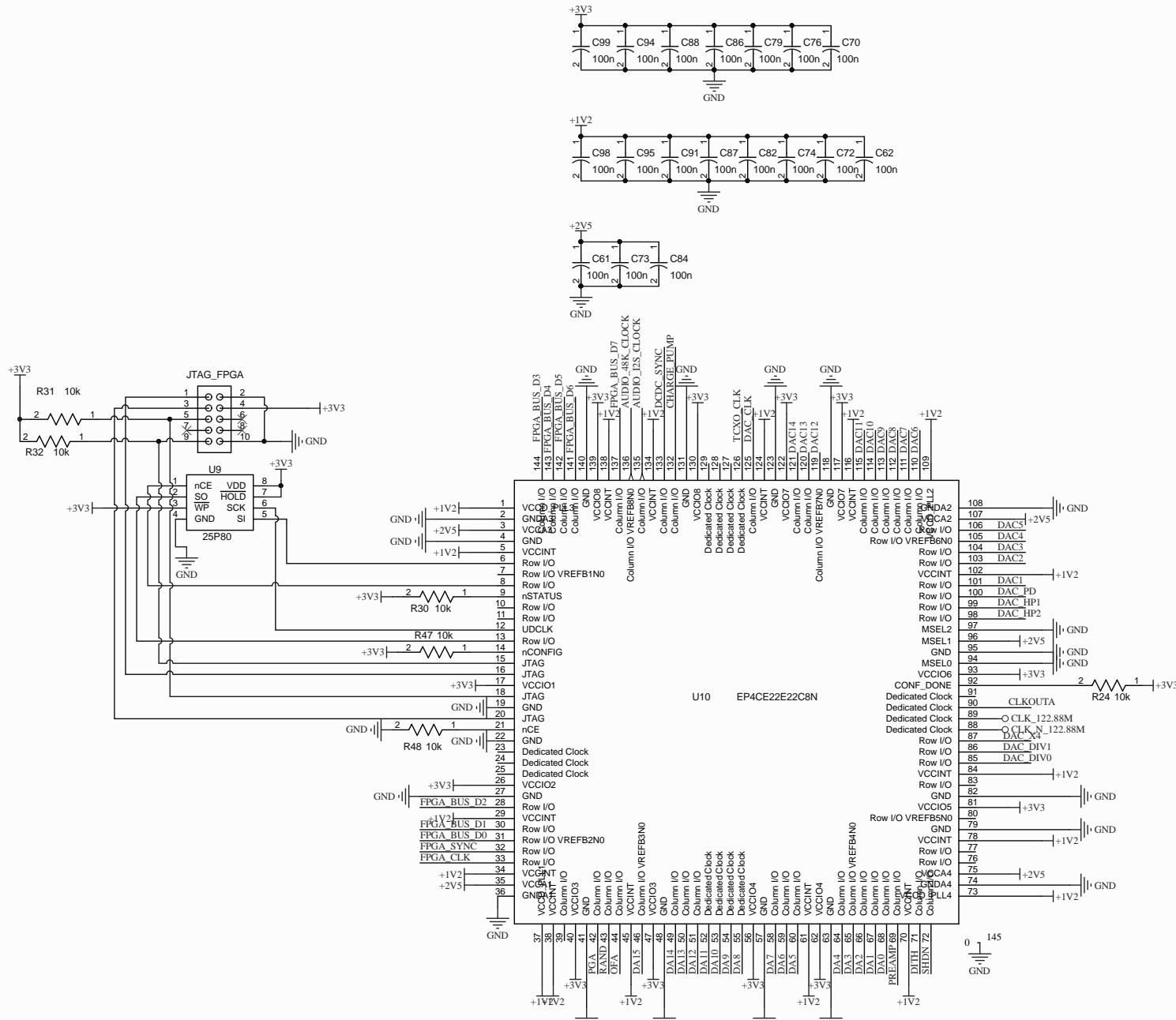
C



D

Title **POWER**

Size: A4	Number:10	Revision2.0
Date: 18.02.2021	Time: 19:31:13	Sheet10 of 18
File: C:\Dropbox\Develop\Projects\WOLF\Scheme\ALTIUM_DESIGNER\MOTHERBOARD\POWER.SchDoc		*

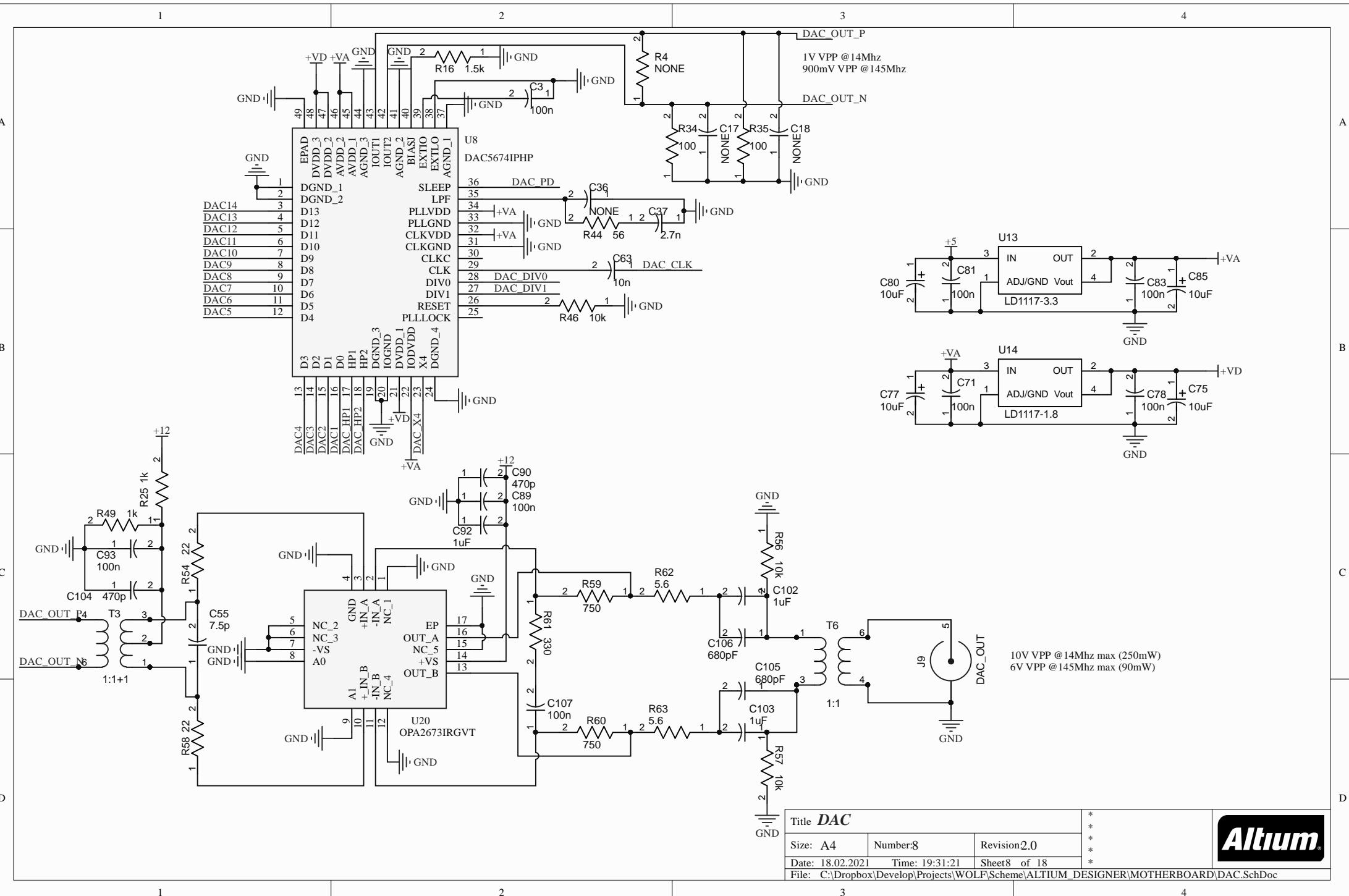
Title **FPGA**

Size: A3 Number:9 Revision2.0

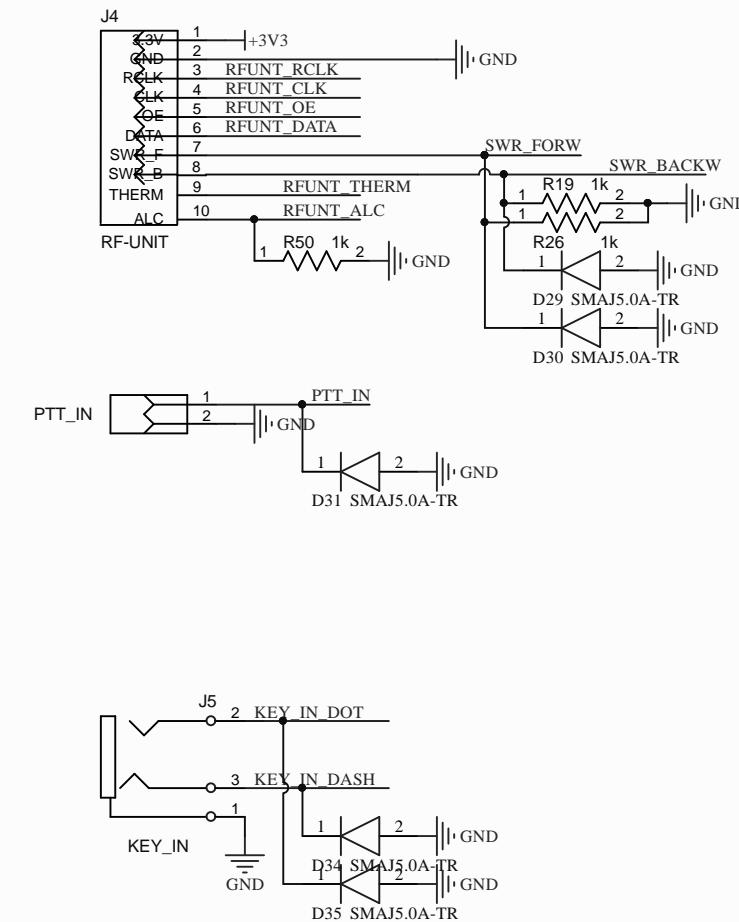
Date: 18.02.2021 Time: 19:31:16 Sheet9 of 18

File: C:\Dropbox\Develop\Projects\WOLF\Scheme\ALTIUM DESIGNER\MOTHERBOARD\FPGA.SchDoc





**Altium**



**J6**

FMC_NE1	1	CS 3v3
FMC_A18	2	RS 3v3
FMC_NWE	3	WR GND
FMC_NOE	4	RD GND
STM_NRST	5	RST#MISO
FMC_D0	6	DB#MOSI
FMC_D1	7	DB#WRX
FMC_D2	8	DB#WTX
FMC_D3	9	DB3CLK
FMC_D4	10	DB\$DCS
FMC_D5	11	DB#AD1 CS
FMC_D6	12	DB#AD2 CS
FMC_D7	13	DB#AD2C
FMC_D8	14	DB#E2A
FMC_D9	15	DB#E2B
FMC_D10	16	DB#E2S
FMC_D11	17	DB1#E1A
FMC_D12	18	DB1#E1B
FMC_D13	19	DB#AD3C
FMC_D14	20	DB13 5v
FMC_D15	21	DB1#GND
PWR_ON	22	DB1#GND
PWR_HOLD	23	PONCAS
	24	PHOCAS
	25	+3V3
	26	
	27	
	28	GND
	29	PERI_MISO
	30	PERI_MOSI
	31	ESP_1_TX
	32	ESP_1_RX
	33	PERI_SCK
	34	SD_CS
	35	AD1_CS
	36	AD2_CS
	37	ENC2_DT
	38	ENC2_CLK
	39	ENC2_SW
	40	ENC_DT
	41	ENC_CLK
	42	AD3_CS
	43	
	44	+5
	45	
	46	GND
	47	

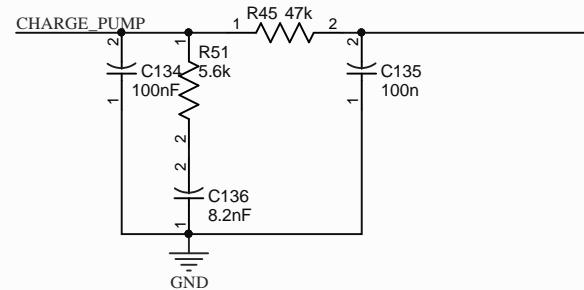
FPC-45P-0.5mm

Title **CONNECTIONS**

Size: A4	Number:7	Revision2.0
Date: 18.02.2021	Time: 19:31:25	Sheet7 of 18
File: C:\Dropbox\Develop\Projects\WOLF\Scheme\ALTIUM_DESIGNER\MOTHERBOARD\CONNECTIONS.SchDoc		*

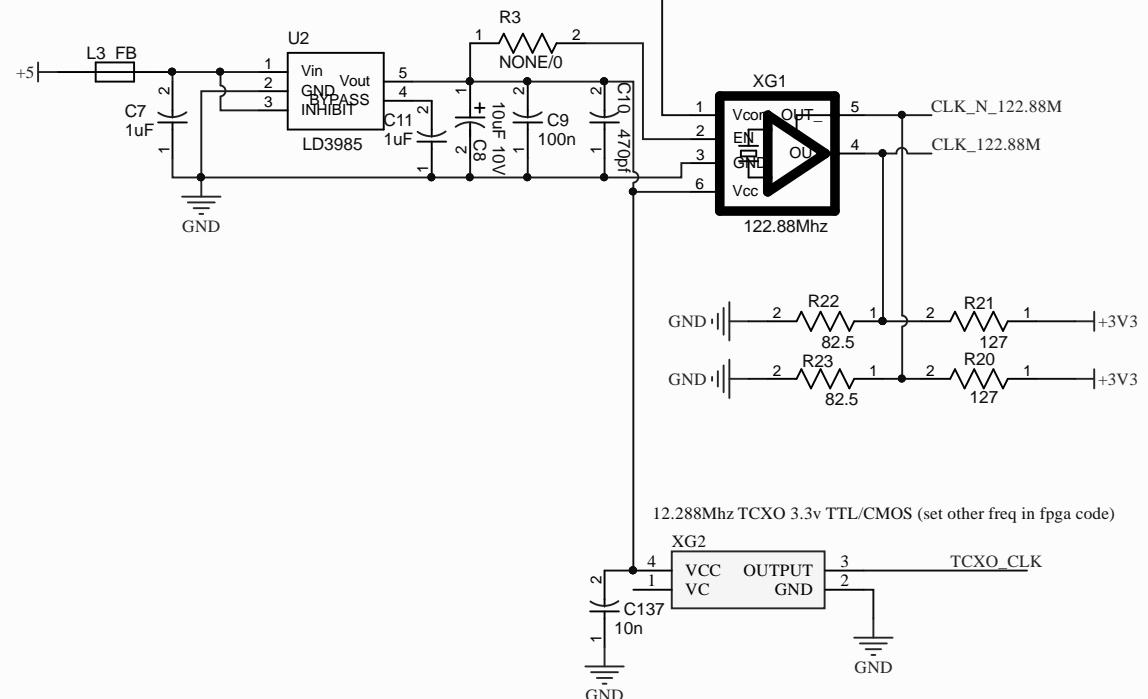
**Altium**

A



A

B



B

C

C

D

D

Title **CLOCK\_GENERATOR**

Size: A4 Number:6 Revision2.0

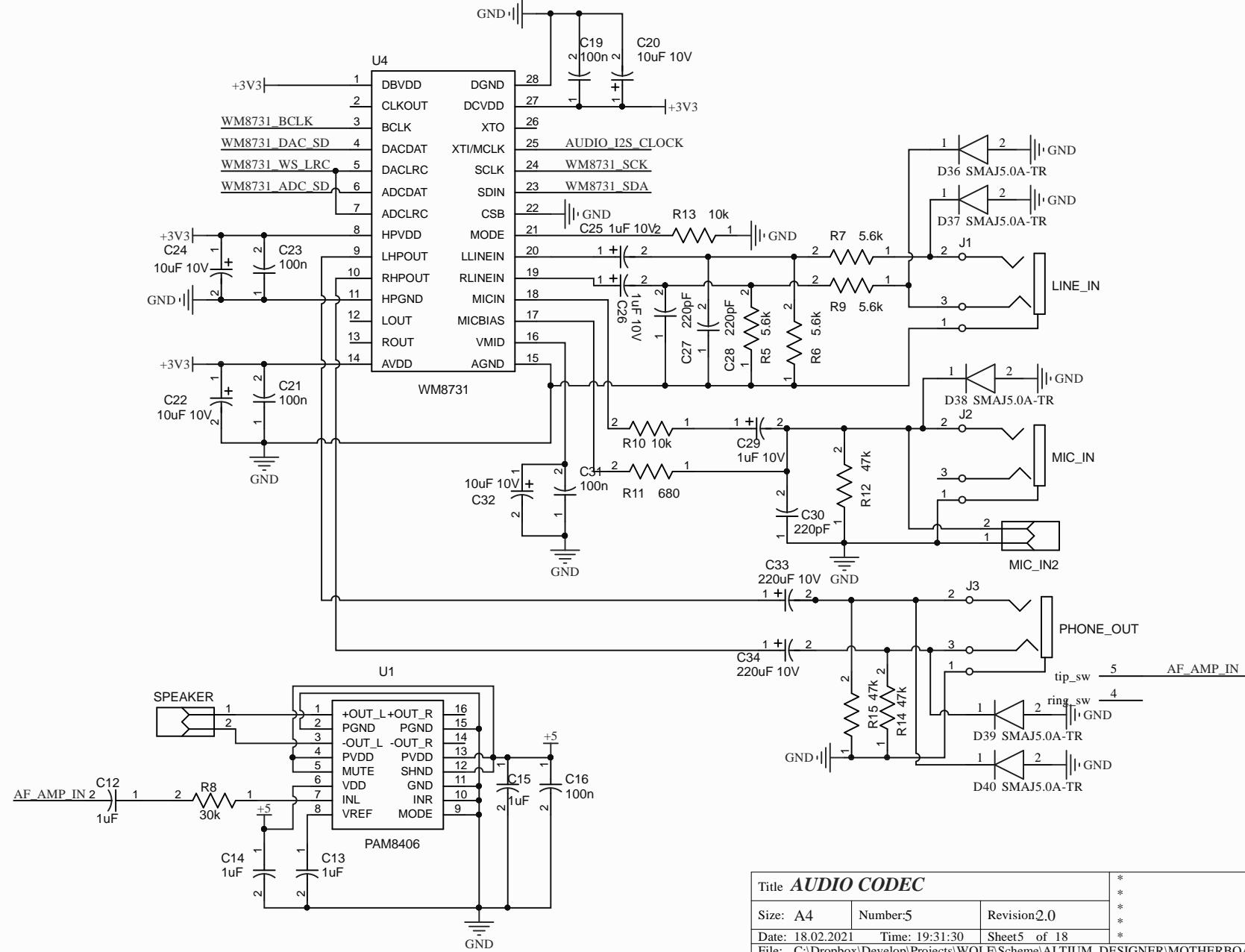
Date: 18.02.2021 Time: 19:31:27 Sheet6 of 18

File: C:\Dropbox\Develop\Projects\WOLF\Scheme\ALTIUM\_DESIGNER\MOTHERBOARD\CLOCK\_GENERATOR.SchDoc

**Altium**

A

A

Title **AUDIO CODEC**

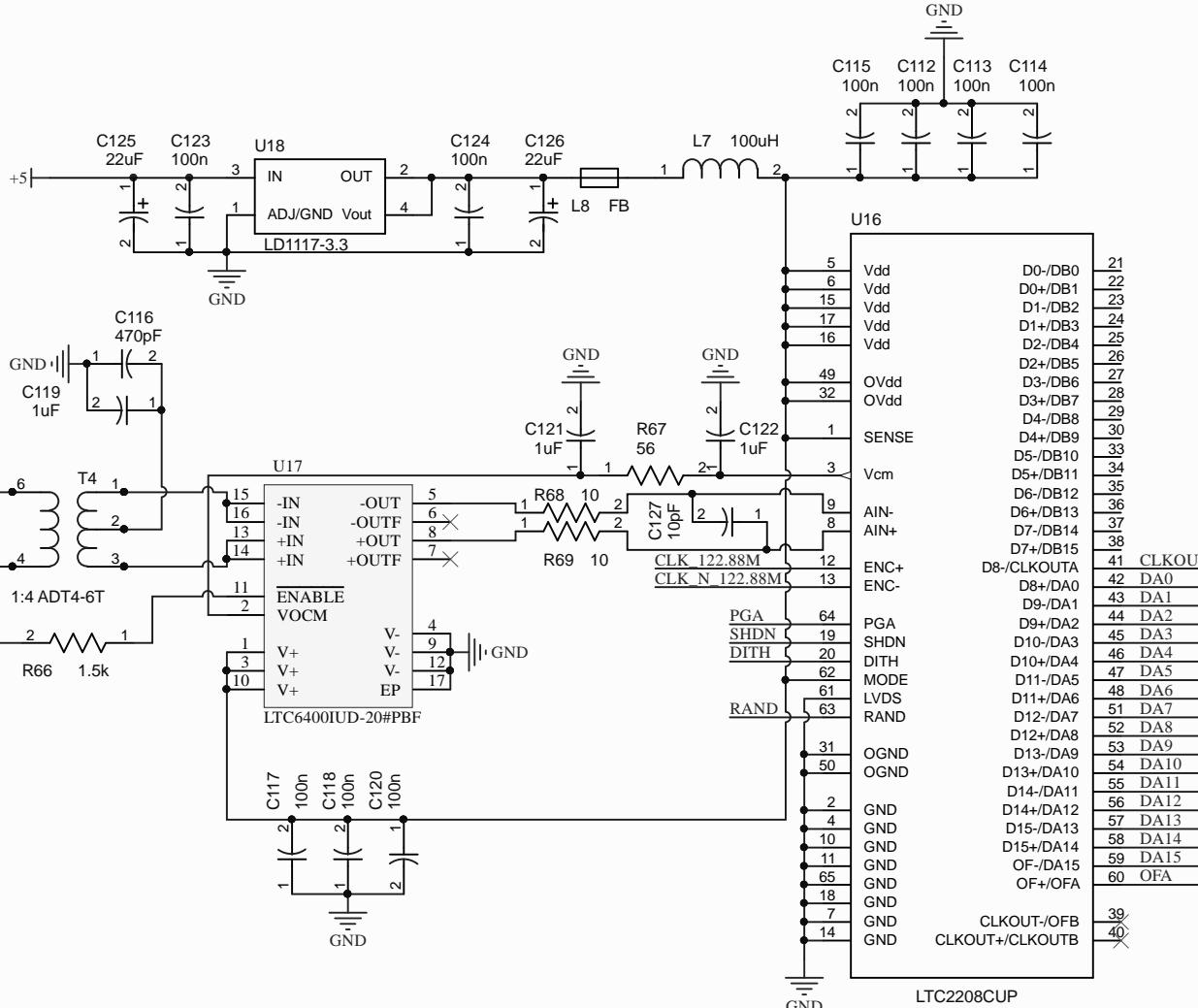
Size: A4 Number:5 Revision:2.0

Date: 18.02.2021 Time: 19:31:30 Sheet: 5 of 18

File: C:\Dropbox\Develop\Projects\WOLF\Schema\ALTIUM\_DESIGNER\MOTHERBOARD\AUDIO\_CODEC.SchDoc

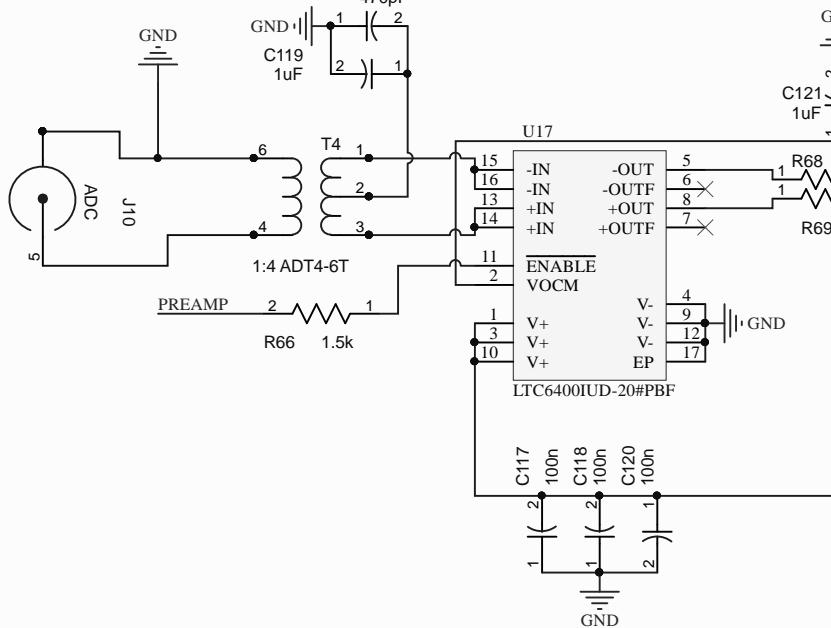
**Altium**

A



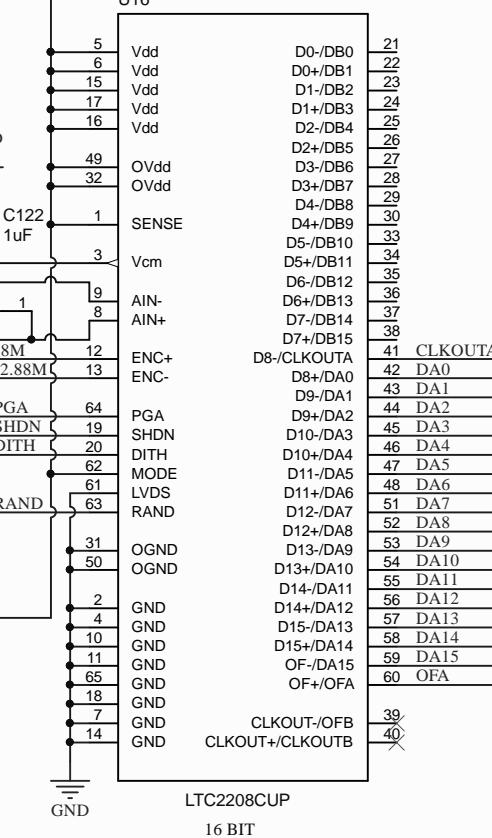
A

B



B

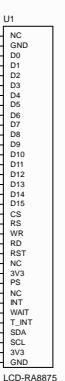
C



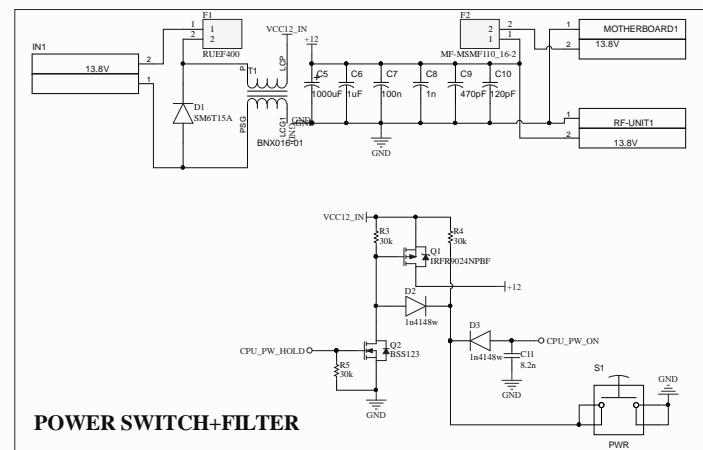
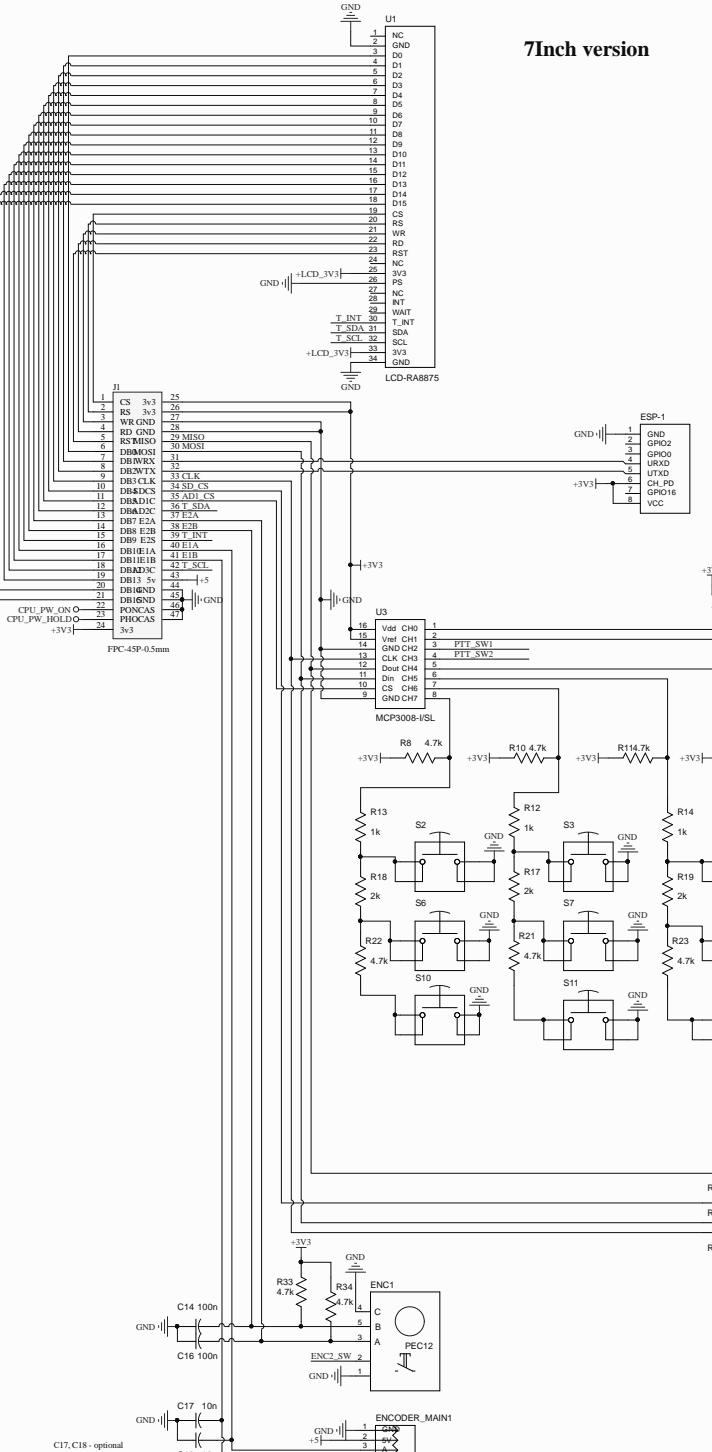
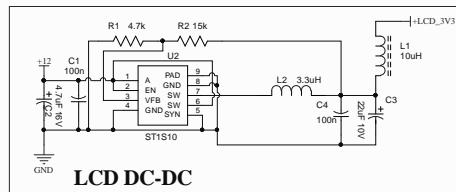
C

D

Title <b>ADC</b>			*
Size: A4	Number:3	Revision 2.0	*
Date: 18.02.2021	Time: 19:31:34	Sheet 3 of 18	*
File: C:\Dropbox\Develop\Projects\WOLF\Scheme\ALTIUM_DESIGNER\MOTHERBOARD\ADC.SchDoc			*



7Inch version



TANGENT

