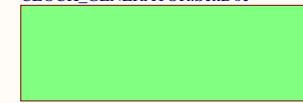


A

U\_POWER  
POWER.SchDoc



U\_CLOCK\_GENERATOR  
CLOCK\_GENERATOR.SchDoc



B

U\_CONNECTIONS  
CONNECTIONS.SchDoc



U\_FPGA  
FPGA.SchDoc



U\_STM32  
STM32.SchDoc



U\_AUDIO\_CODEC  
AUDIO\_CODEC.SchDoc



A

B

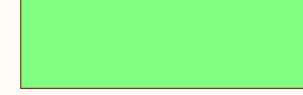
C

D

U\_DAC  
DAC.SchDoc



U\_ADC  
ADC.SchDoc



Title **MOTHERBOARD**

Size: A4	Number:2	Revision:2.0
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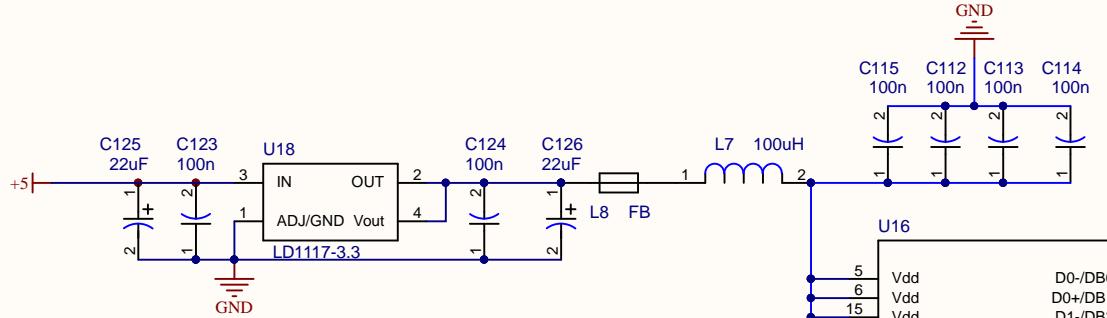
Date: 04.10.2020	Time: 18:19:59	Sheet2 of 18
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File: D:\Dropbox\Develop\Projects\UA3REO\Scheme\ALTIUM_DESIGNER\MOTHERBOARD\MOTHERBOARD.SCHDOC	*
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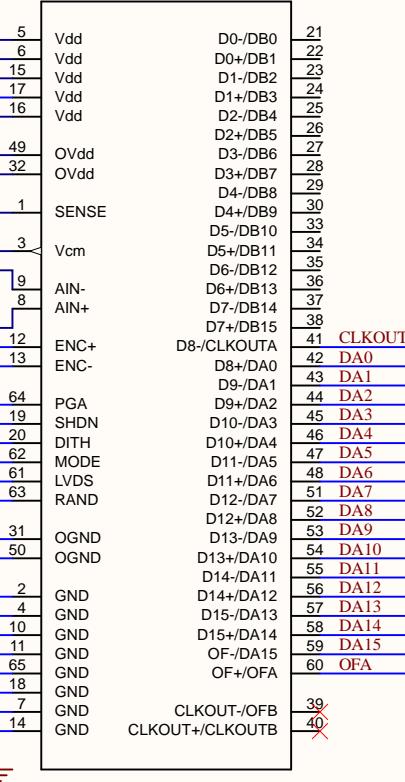
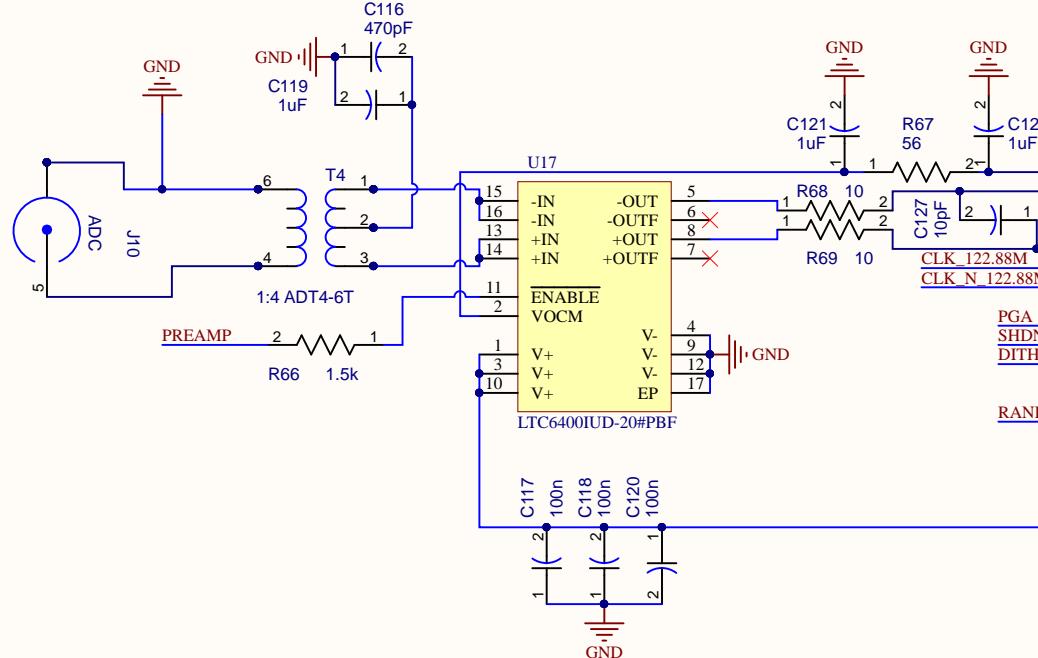
A

A



B

B



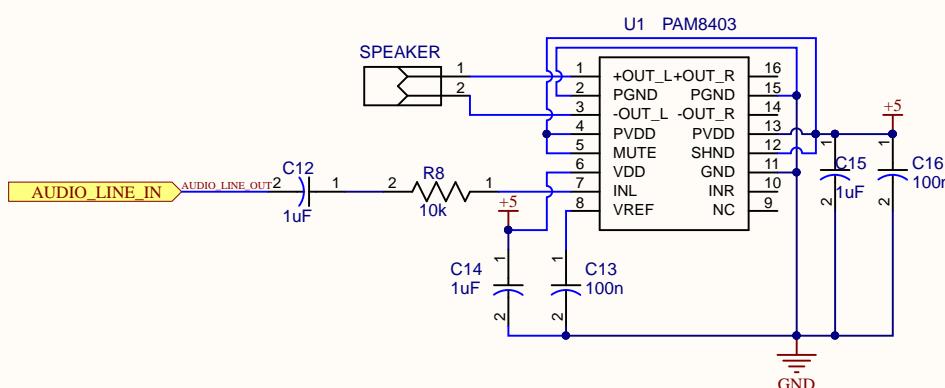
C

C

D

D

Title **ADC**Size: **A4** Number: **3** Revision: **2.0**Date: **04.10.2020** Time: **18:19:59** Sheet **3** of **18**File: **D:\Dropbox\Develop\Projects\UA3REO\Scheme\ALTIUM\_DESIGNER\MOTHERBOARD\ADC.SchDoc****Altium**



Title ***AF AMP***

Size: A4	Number:4	Revision:2.0
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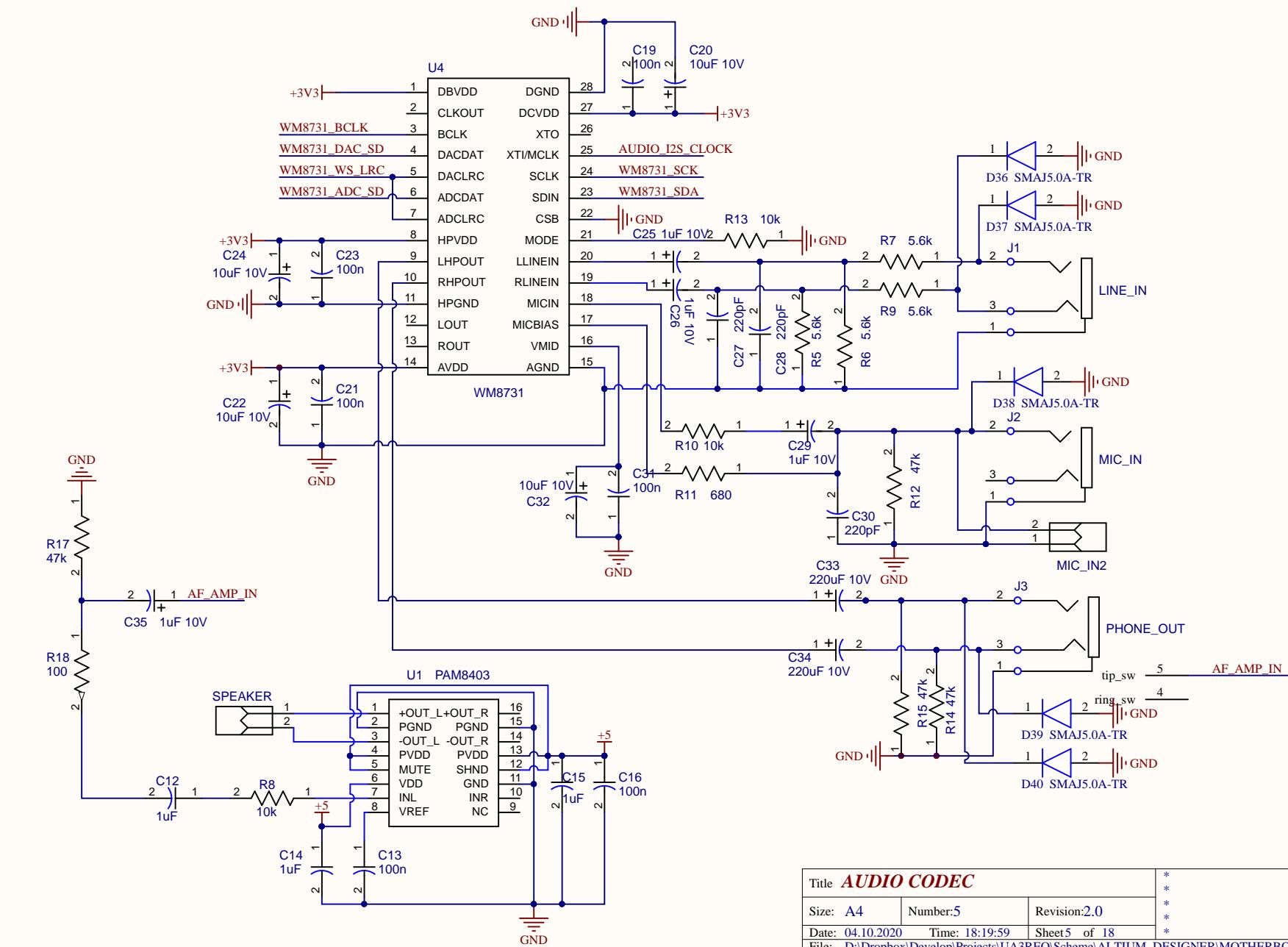
Date: 04.10.2020	Time: 18:19:59	Sheet 4 of 18
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File: D:\Dropbox\Develop\Projects\UA3REO\Scheme\ALTIUM_DESIGNER\MOTHERBOARD\AF AMP.SchDoc	*	UA3REO
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*	BH8CGJ	*
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*	Altium	*
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A

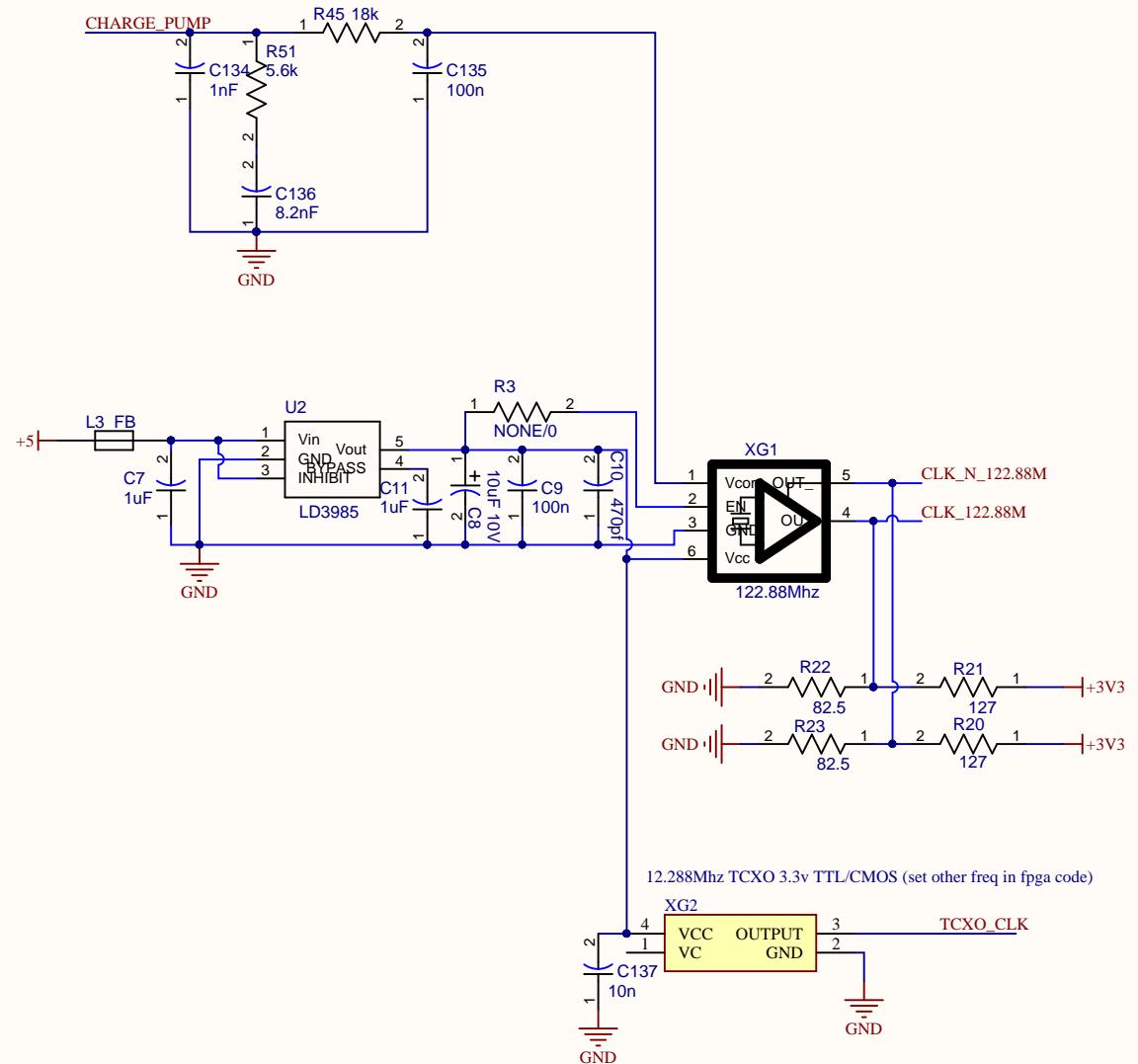
Title **AUDIO CODEC**

Size: A4 Number:5 Revision:2.0

Date: 04.10.2020 Time: 18:19:59 Sheet 5 of 18

File: D:\Dropbox\Develop\Projects\UA3REO\Scheme\ALTIUM\_DESIGNER\MOTHERBOARD\AUDIO CODEC.SchDoc

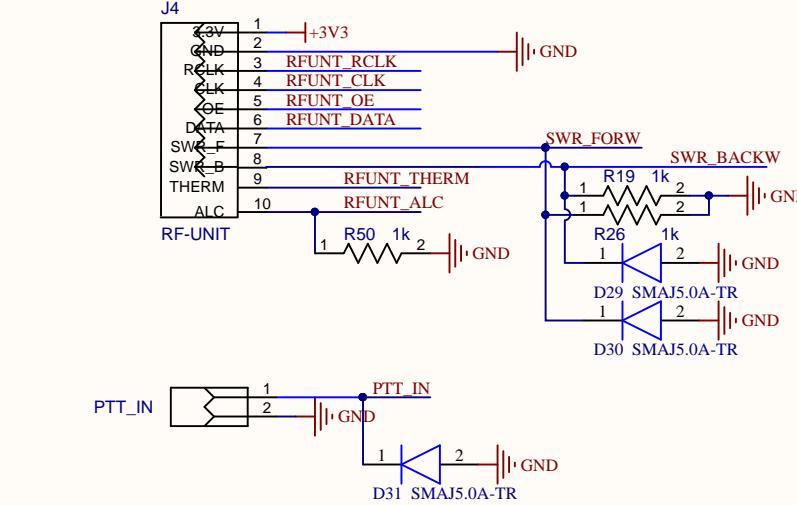
**Altium**



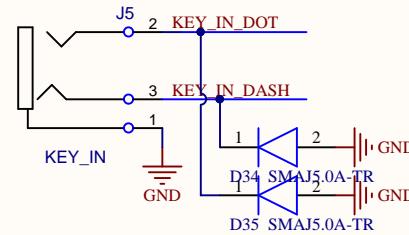
Title	<b>CLOCK GENERATOR</b>		
Size:	A4	Number:	6
Date:	04.10.2020	Time:	18:19:59
File:	D:\Dropbox\Devolon\Projects\UA3RE		

**Altium**

A



B



C

**J6**

1	CS 3v3
2	FMC_A18 3v3
3	FMC_NWE GND
4	FMC_NOE GND
5	STM_NRST
6	RSTMISO
7	FMC_D1 DB0MOSI
8	FMC_D2 DB1WRX
9	FMC_D3 DB2WTX
10	FMC_D4 DB3CLK
11	FMC_D5 DB4DCS
12	FMC_D6 DB5AD1C
13	FMC_D7 DB6AD2C
14	FMC_D8 DB7E2A
15	FMC_D9 DB8E2B
16	FMC_D10 DB9E2S
17	FMC_D11 DB1E1A
18	FMC_D12 DB1E1B
19	FMC_D13 DBAD3C
20	FMC_D14 DB13 5v
21	FMC_D15 DB1GND
22	PWR_ON DB1GND
23	PWR_HOLD PONCAS
24	+3V3 PHOCAS
25	+3V3 3v3
26	PERI_MOSI
27	PERI_MOSI
28	PERI_SCK
29	SD_CS
30	AD1_CS
31	AD2_CS
32	ENC2_DT
33	ENC2_CLK
34	ENC_SW
35	ENC_DT
36	ENC_CLK
37	AD3_CS
38	ENC2_DT
39	ENC2_CLK
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42	ENC_CLK
43	+5
44	AD3_CS
45	ENC_DT
46	ENC_CLK
47	ENC_SW

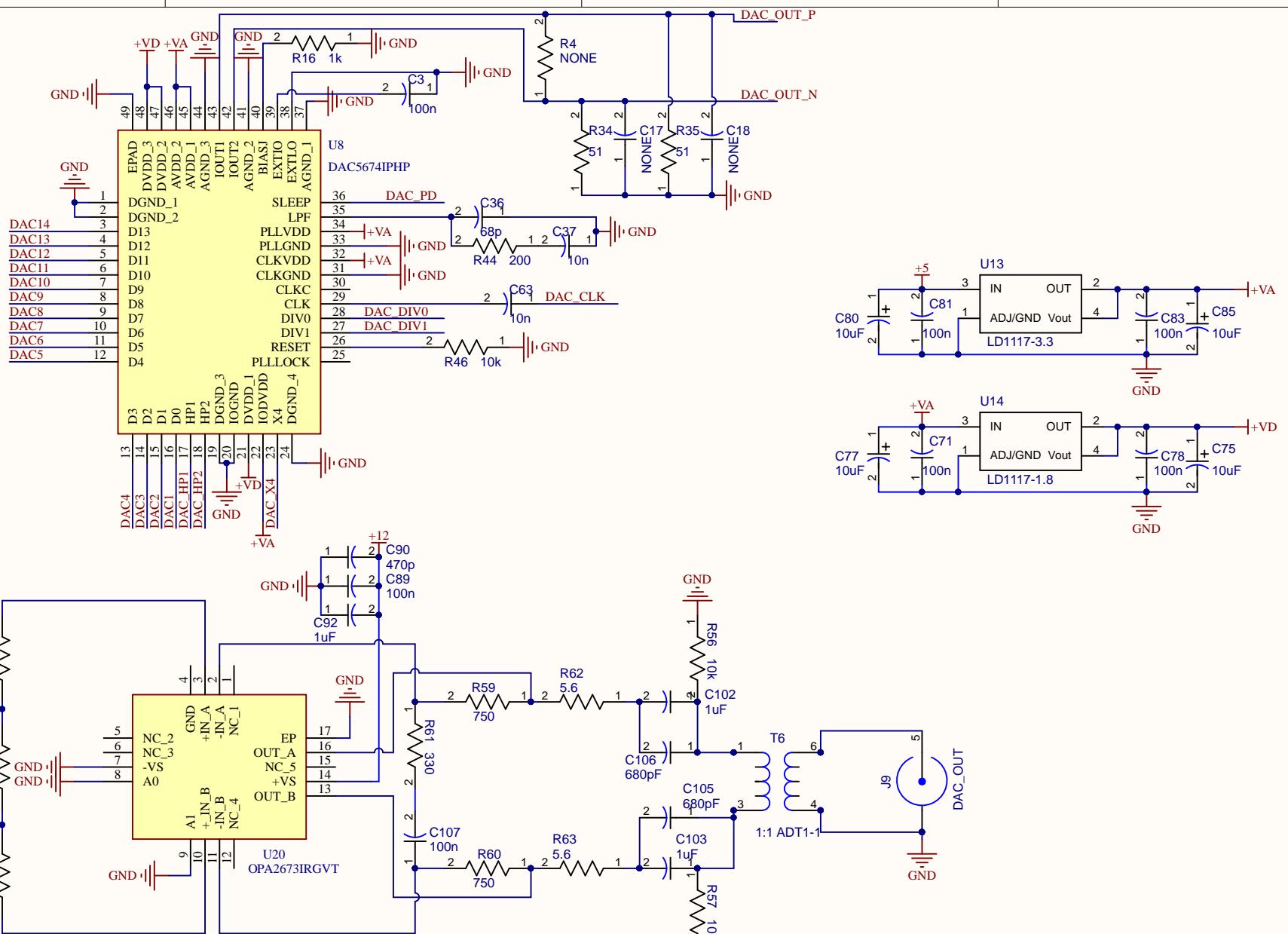
FPC-45P-0.5mm

D

Title **CONNECTIONS**

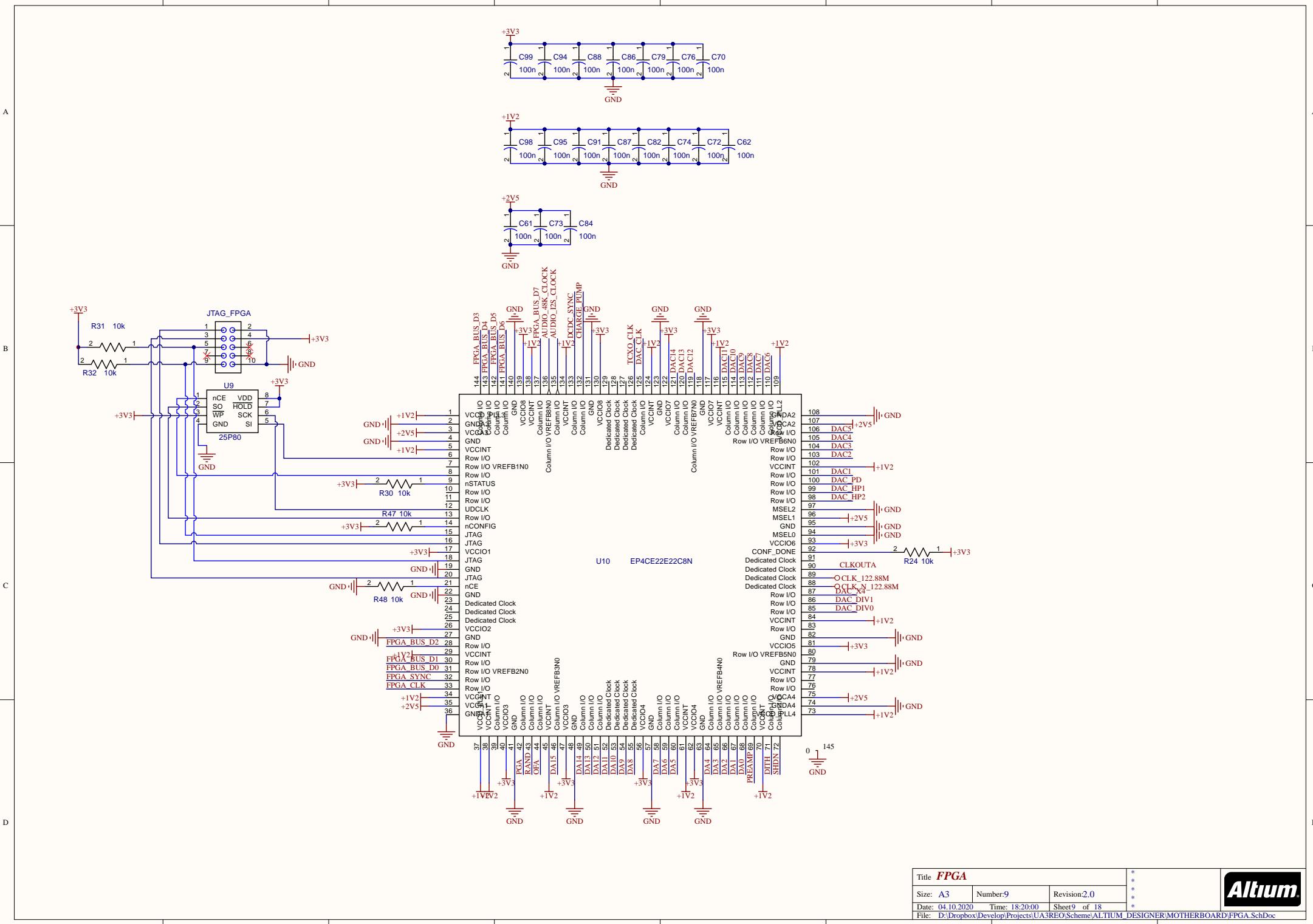
Size: A4	Number: 7	Revision: 2.0
Date: 04.10.2020	Time: 18:19:59	Sheet 7 of 18
File: D:\Dropbox\Develop\Projects\UA3REO\Scheme\ALTIUM_DESIGNER\MOTHERBOARD\CONNECTIONS.SchDoc		

**Altium**



Title <b>DAC</b>		
Size: A4	Number: 8	Revision: 2.0
Date: 04.10.2020	Time: 18:20:00	Sheet 8 of 18
File: D:\Dropbox\Develop\Projects\UA3REO\Scheme\ALTIUM_DESIGNER\MOTHERBOARD\DAC.SchDoc	*	*

**Altium**

**Title *FPGA***

Size: A3

Number:9

Revision:2.0

Date: 04.10.2020

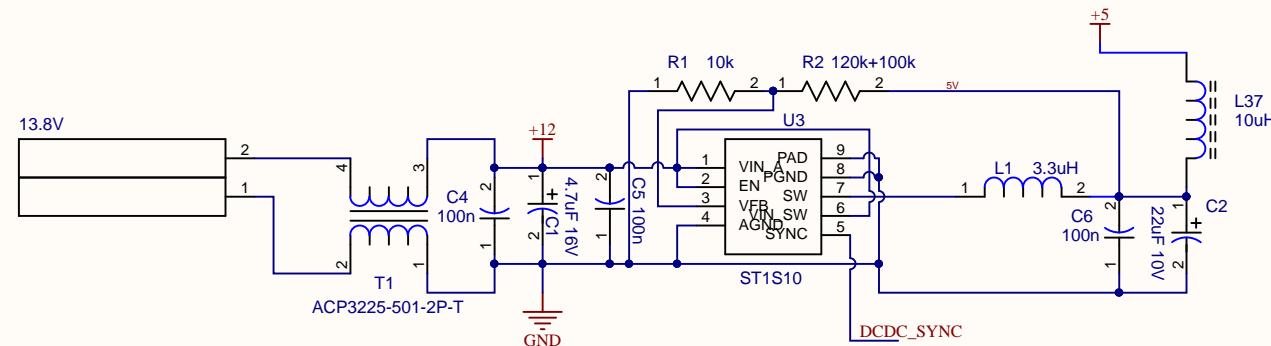
Time: 18:20:00

Sheet9 of 18

File: D:\Dropbox\Develop\Projects\UA3REO\Scheme\ALTIUM DESIGNER\MOTHERBOARD\FPGA.SchDoc

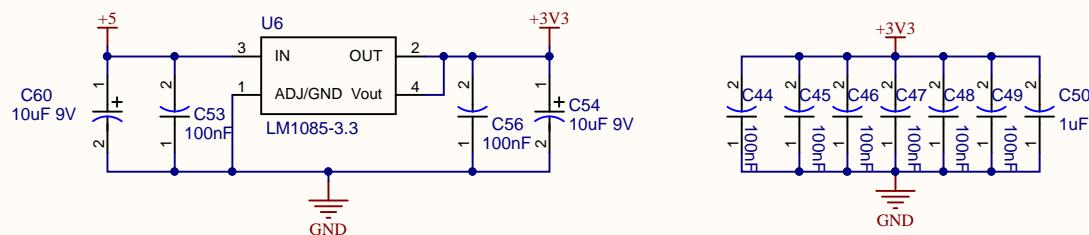


A



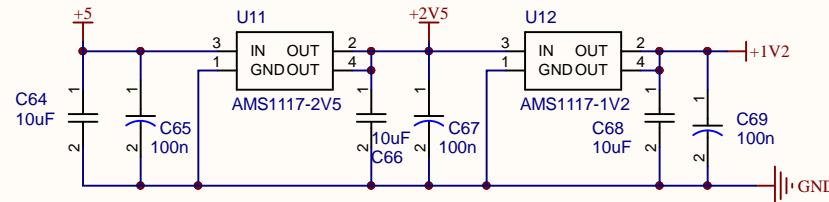
A

B



B

C

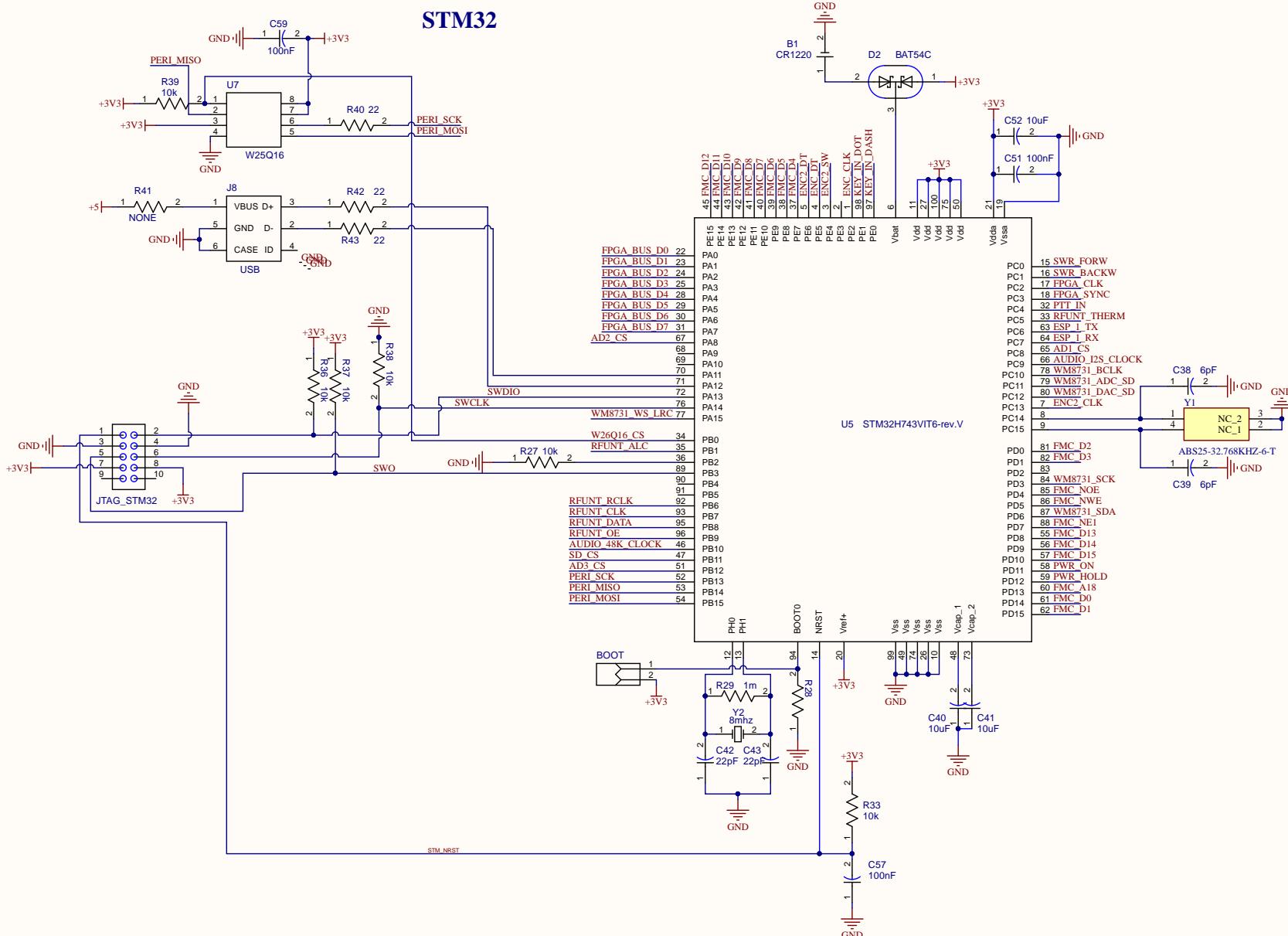


C

D

Title <b>POWER</b>		
Size: A4	Number:10	Revision:2.0
Date: 04.10.2020	Time: 18:20:00	Sheet10 of 18
File: D:\Dropbox\Develop\Projects\UA3REO\Scheme\ALTIUM_DESIGNER\MOTHERBOARD\POWER.SchDoc	*	*





Title STM32

Size: A3 Number:11 Date: 04.10.2020 Time: 18:20:00 Sh



A

A

B

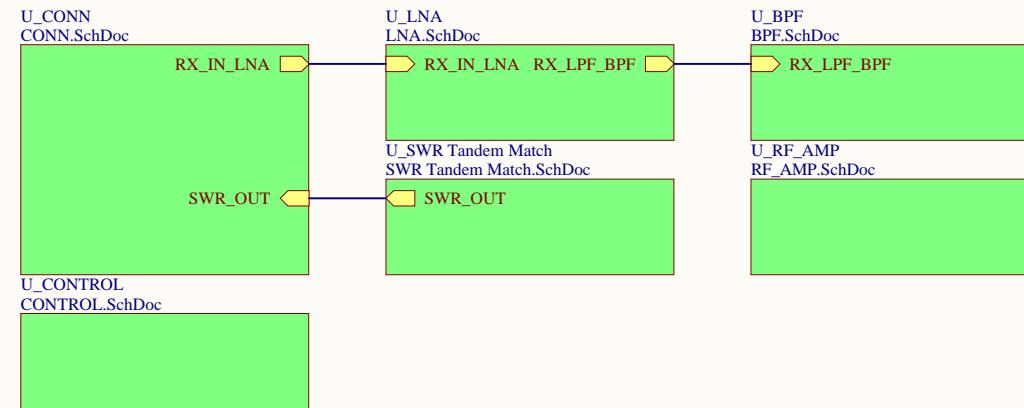
B

C

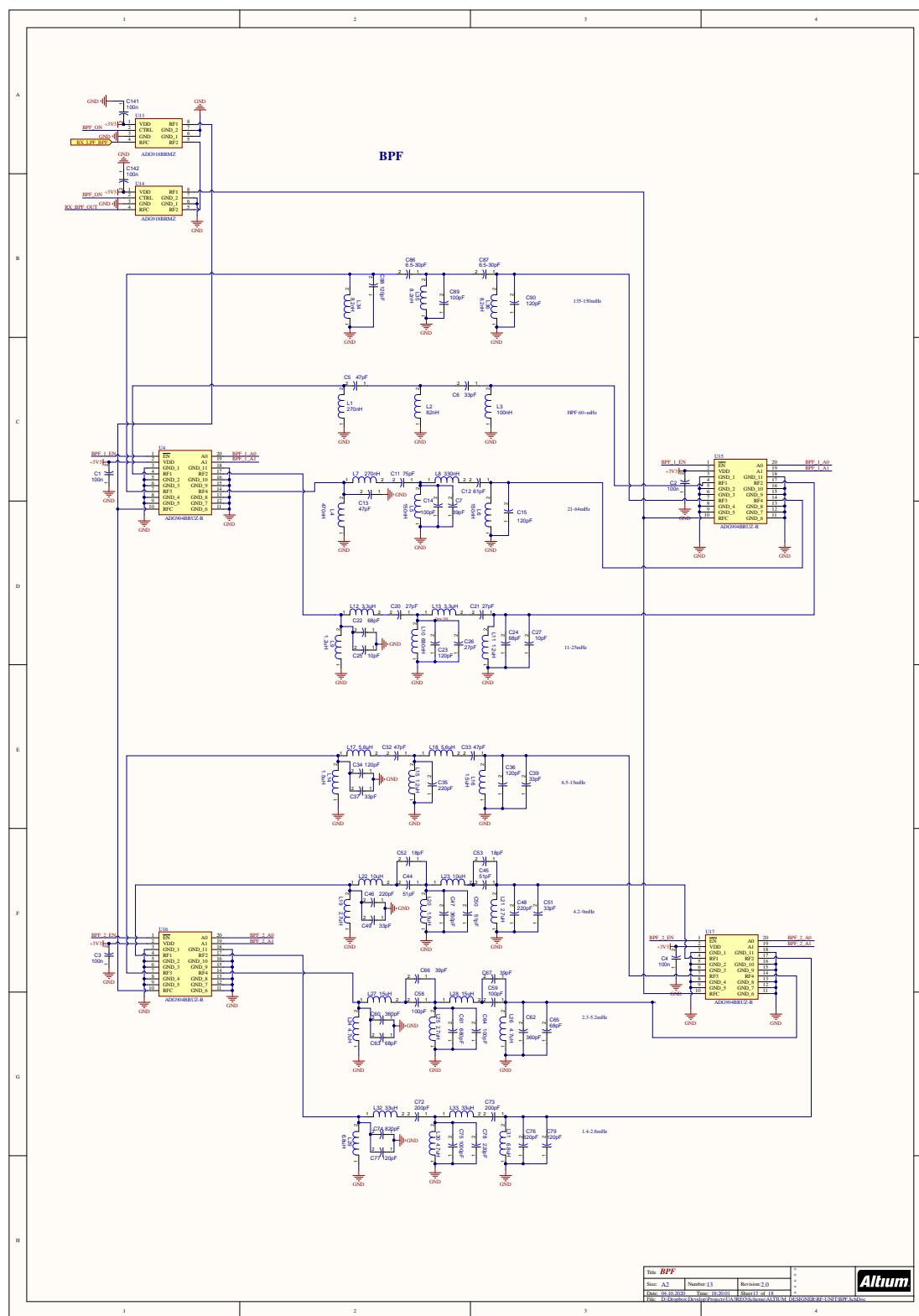
C

D

D

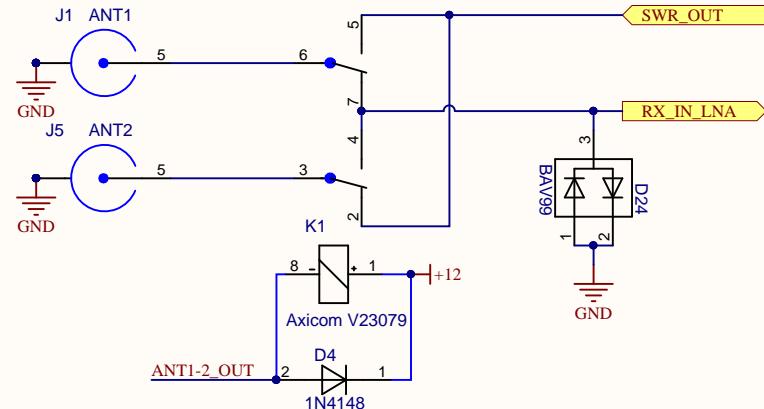


Title <b>RF-UNIT</b>			*
Size: A4	Number:12	Revision:2.0	*
Date: 04.10.2020	Time: 18:20:01	Sheet 12 of 18	*
File: D:\Dropbox\Develop\Projects\UA3REO\Scheme\ALTIUM_DESIGNER\RF-UNIT\RF-UNIT.SCHDOC			Altium®



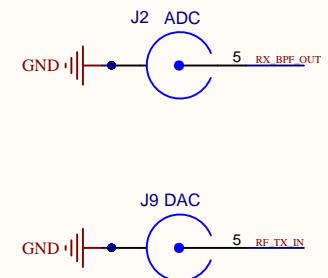
A

## TXRX\_COMUTATOR

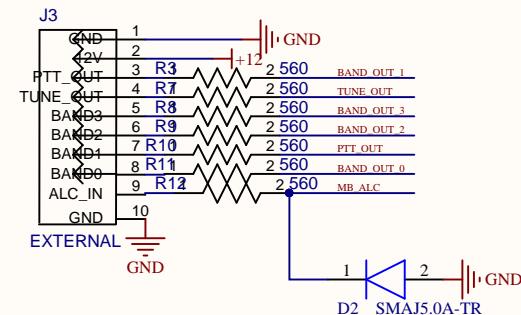
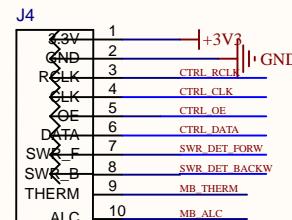


B

## CONN



C

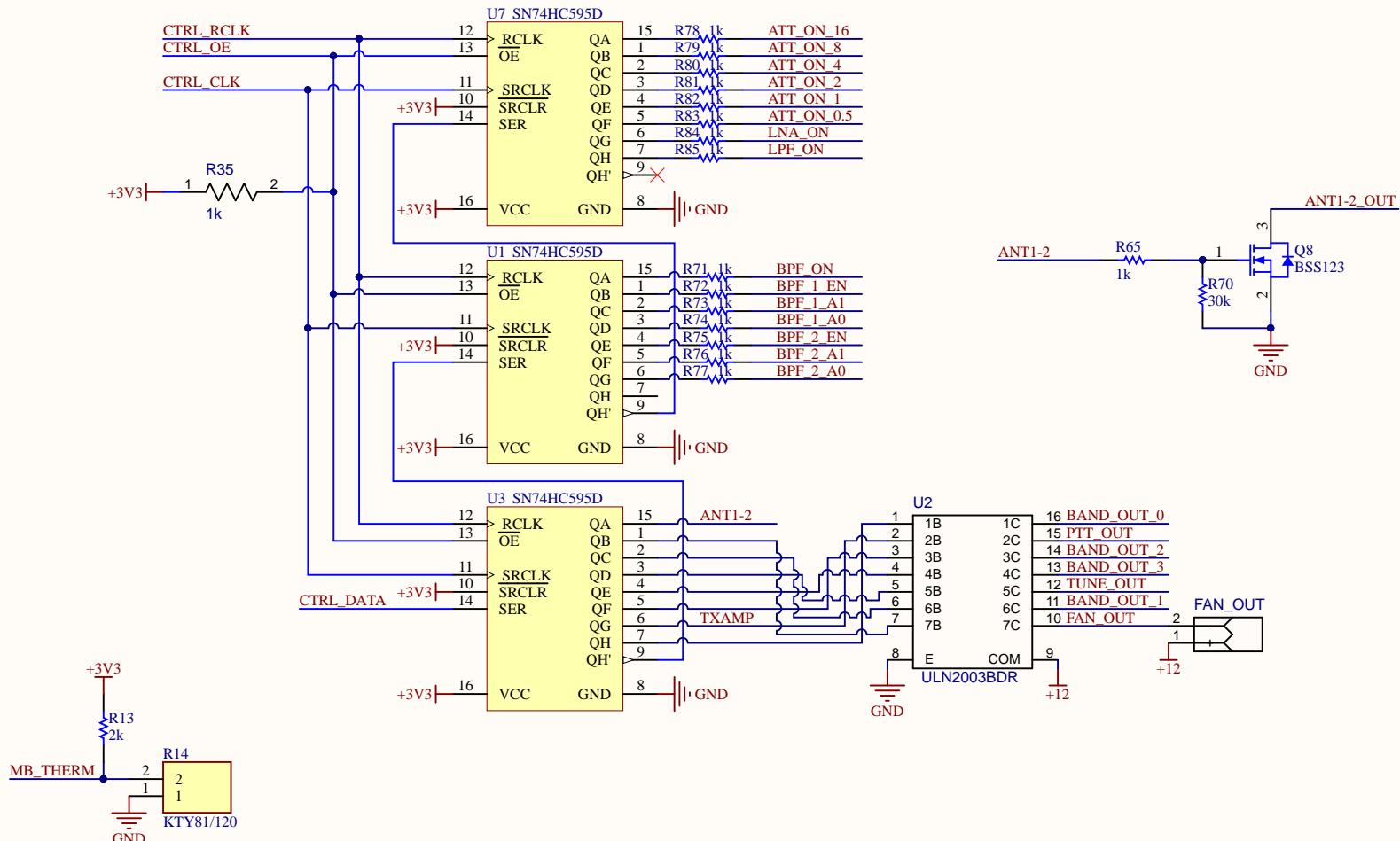


D

Title **CONN**

Size: A4	Number: 14	Revision: 2.0
Date: 04.10.2020	Time: 18:20:01	Sheet 14 of 18
File: D:\Dropbox\Develop\Projects\UA3REO\Scheme\ALTIUM_DESIGNER\RF-UNIT\CONN.SchDoc		*

**Altium**

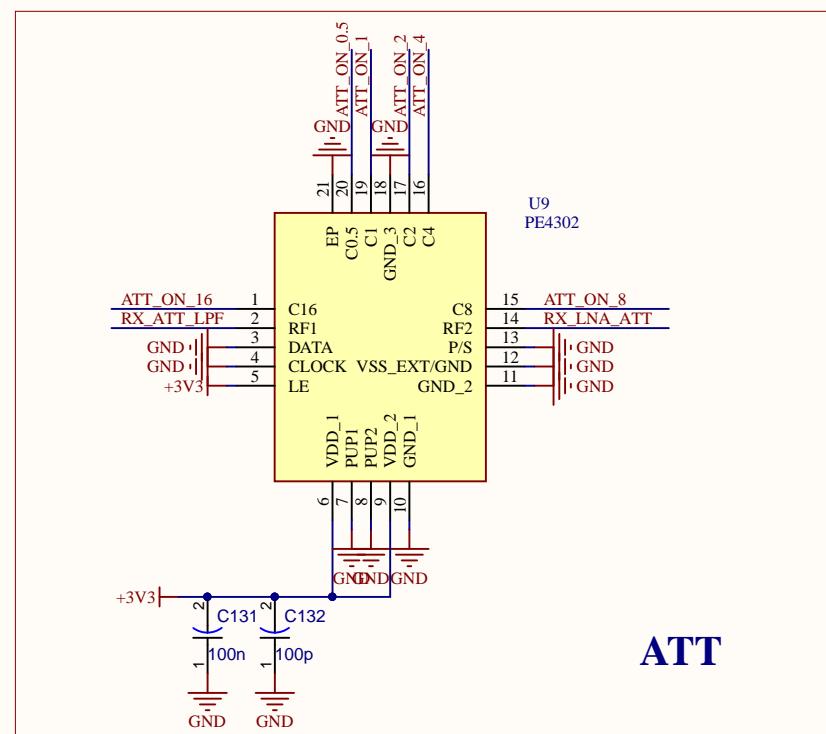
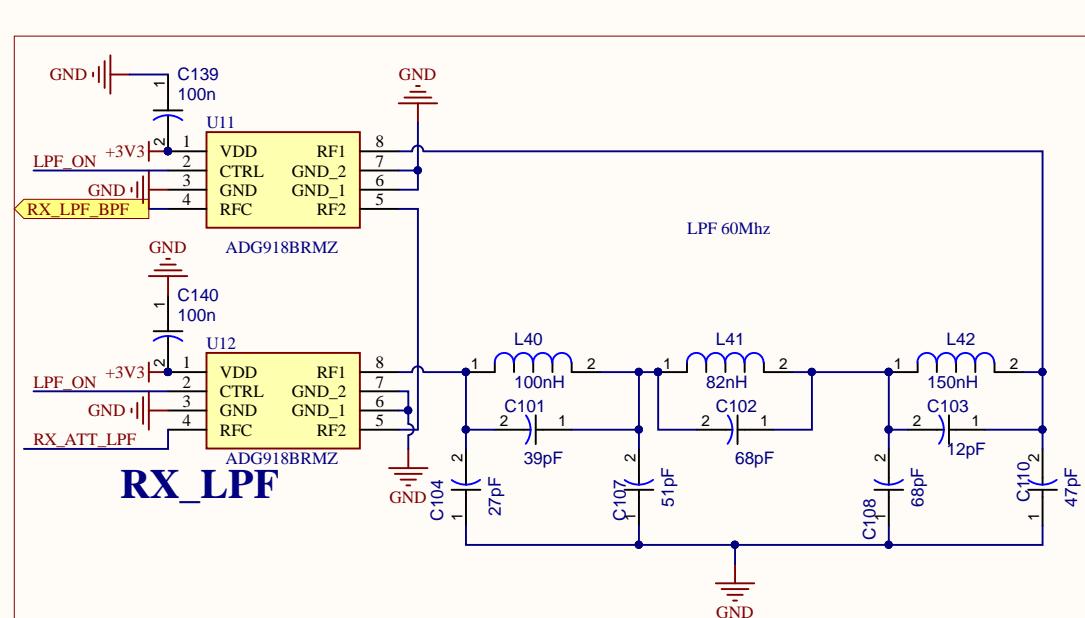
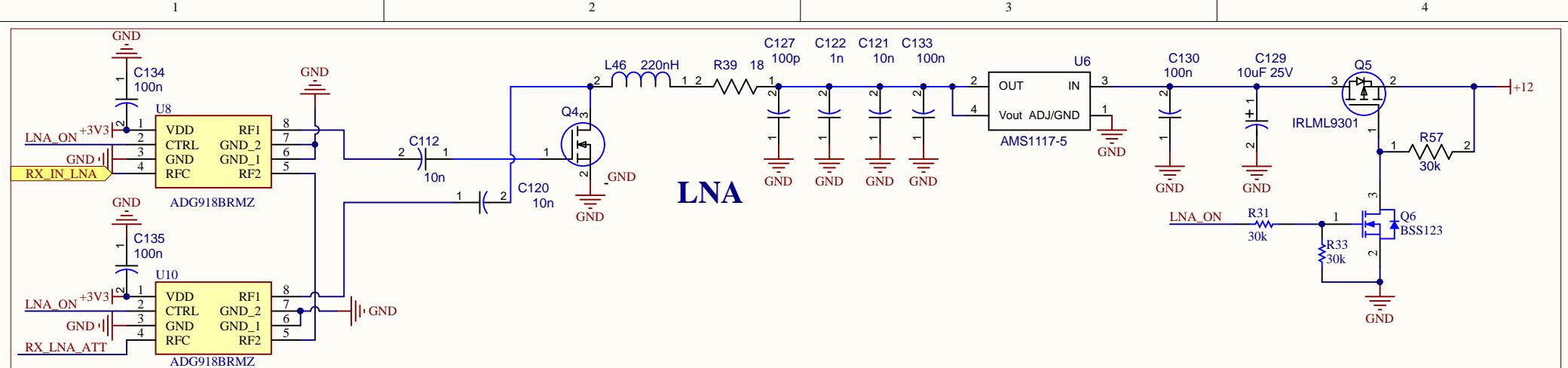
Title **CONTROL**

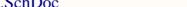
Size: A4 Number:15 Revision:2.0

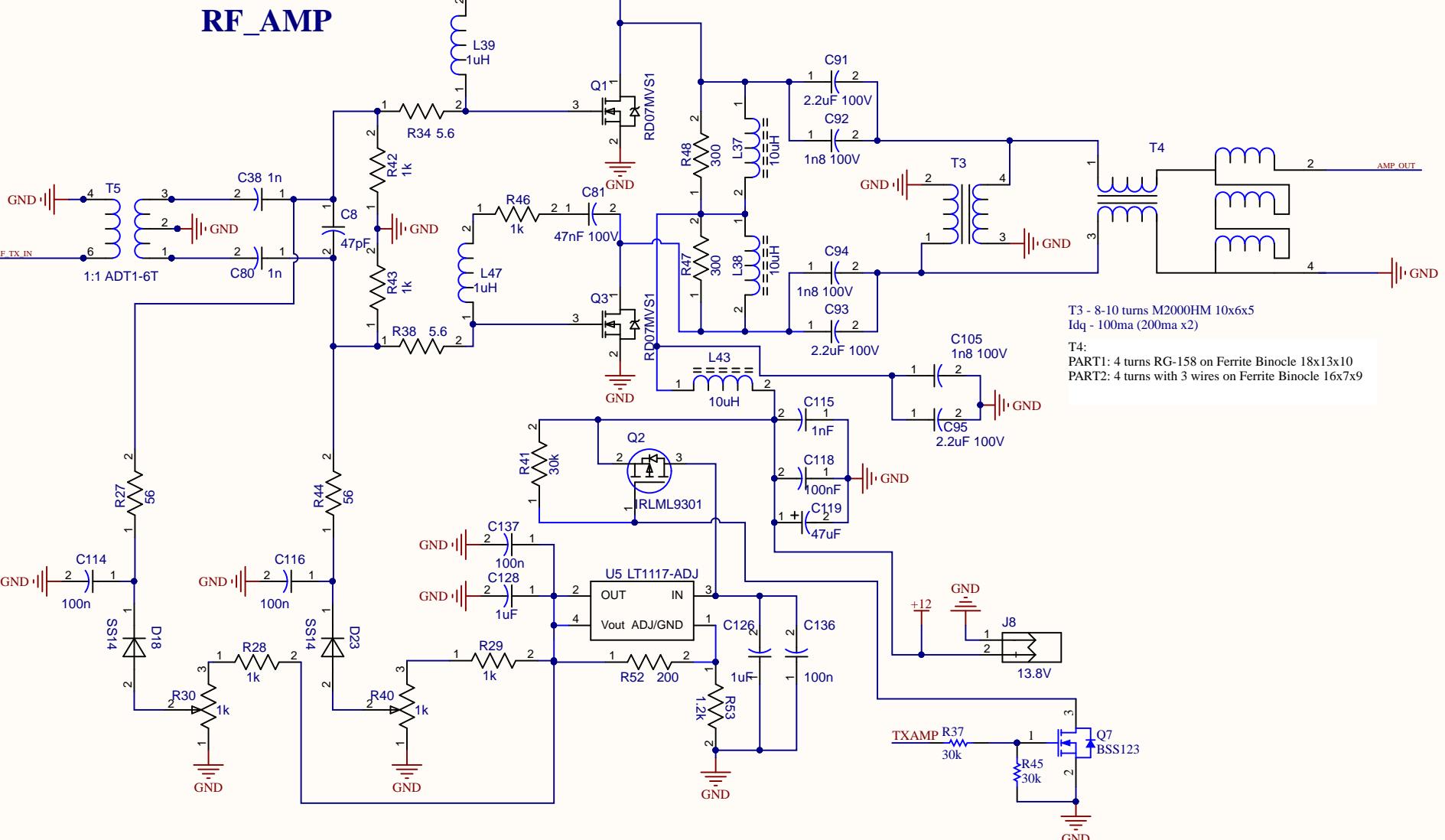
Date: 04.10.2020 Time: 18:20:01 Sheet 15 of 18

File: D:\Dropbox\Develop\Projects\UA3REO\Scheme\ALTIUM\_DESIGNER\RF-UNIT\CONTROL.SchDoc





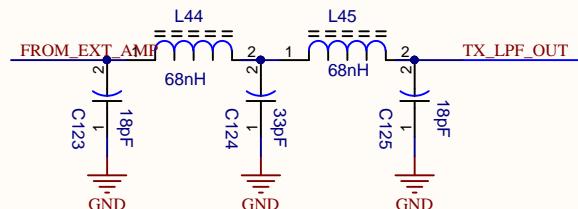
Title <b>LNA</b>			*	
Size: A4	Number: 16	Revision: 2.0	*	
Date: 04.10.2020	Time: 18:20:01	Sheet 16 of 18	*	
File: D:\Dropbox\Develop\Projects\UA3REO\Scheme\ALTIUM DESIGNER\RF-UNIT\LNA.SchDoc			*	
			*	



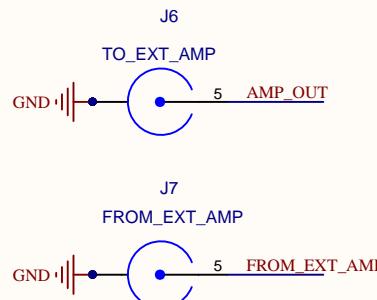
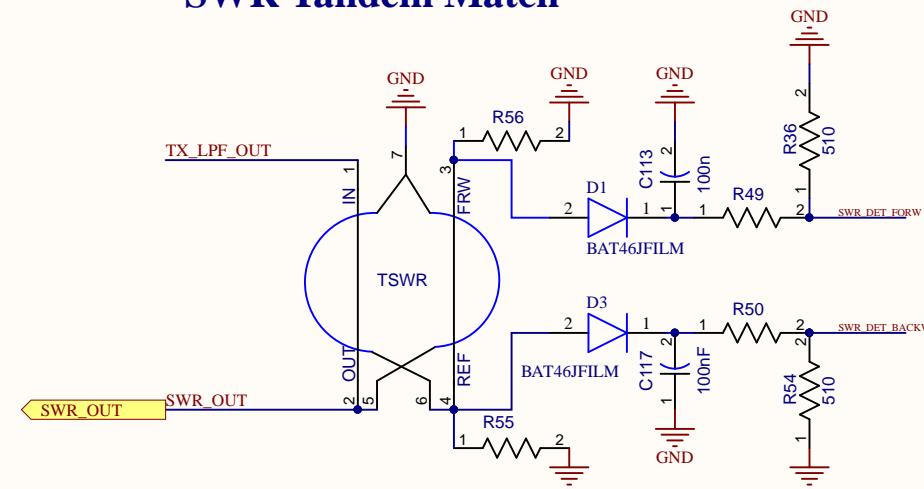
Title <b>RF_AMP</b>		
Size: A4	Number: 17	Revision: 2.0
Date: 04.10.2020	Time: 18:20:01	Sheet 17 of 18
File: D:\Dropbox\Develop\Projects\UA3REO\Scheme\ALTIUM_DESIGNER\RF-UNIT\RF_AMP.SchDoc		

**TX\_LPF**

LPF 170Mhz



Катушки намотаны проводом 0.5мм на оправке диаметром 5мм, 3.5 витка

**SWR Tandem Match**Title ***SWR Tandem Match***

Size: A4 Number:18 Revision:2.0

Date: 04.10.2020 Time: 18:20:02 Sheet 18 of 18

File: D:\Dropbox\Develop\Projects\UA3REO\Scheme\ALTIUM\_DESIGNER\RF-UNIT\SWR Tandem Match.SchDoc

**Altium**