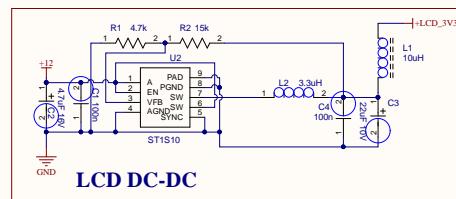




7Inch version



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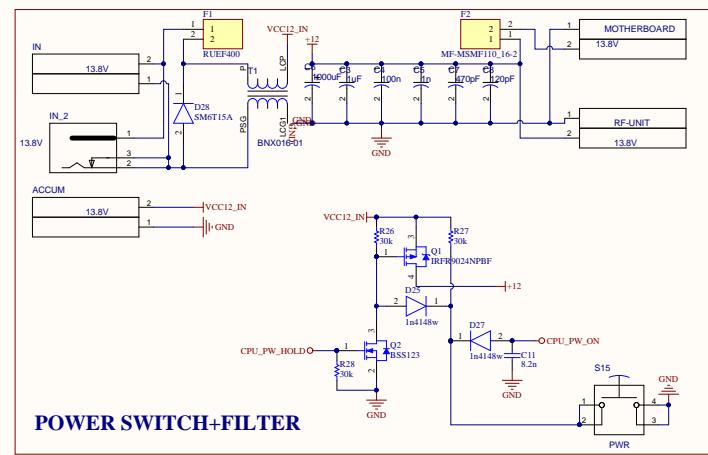
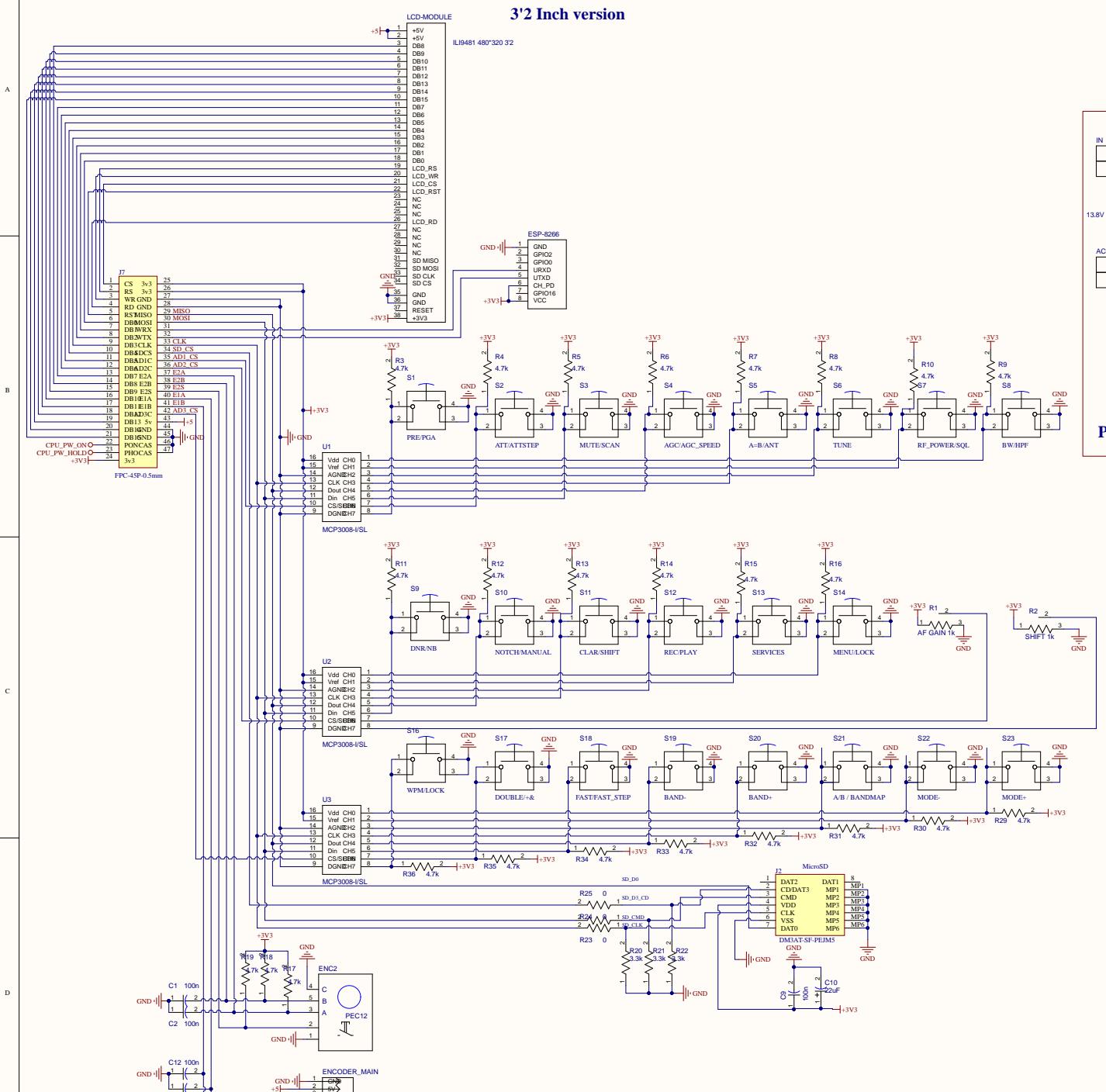
3

4

5

6

3'2 Inch version



POWER SWITCH+FILTER

A

U_POWER
POWER.SchDoc



U_CLOCK_GENERATOR
CLOCK_GENERATOR.SchDoc



A

B

U_CONNECTIONS
CONNECTIONS.SchDoc



U_FPGA
FPGA.SchDoc



U_STM32
STM32.SchDoc



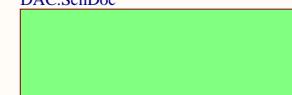
U_AUDIO_CODEC
AUDIO_CODEC.SchDoc



B

C

U_DAC
DAC.SchDoc



U_ADC
ADC.SchDoc



C

D

Title **MOTHERBOARD**

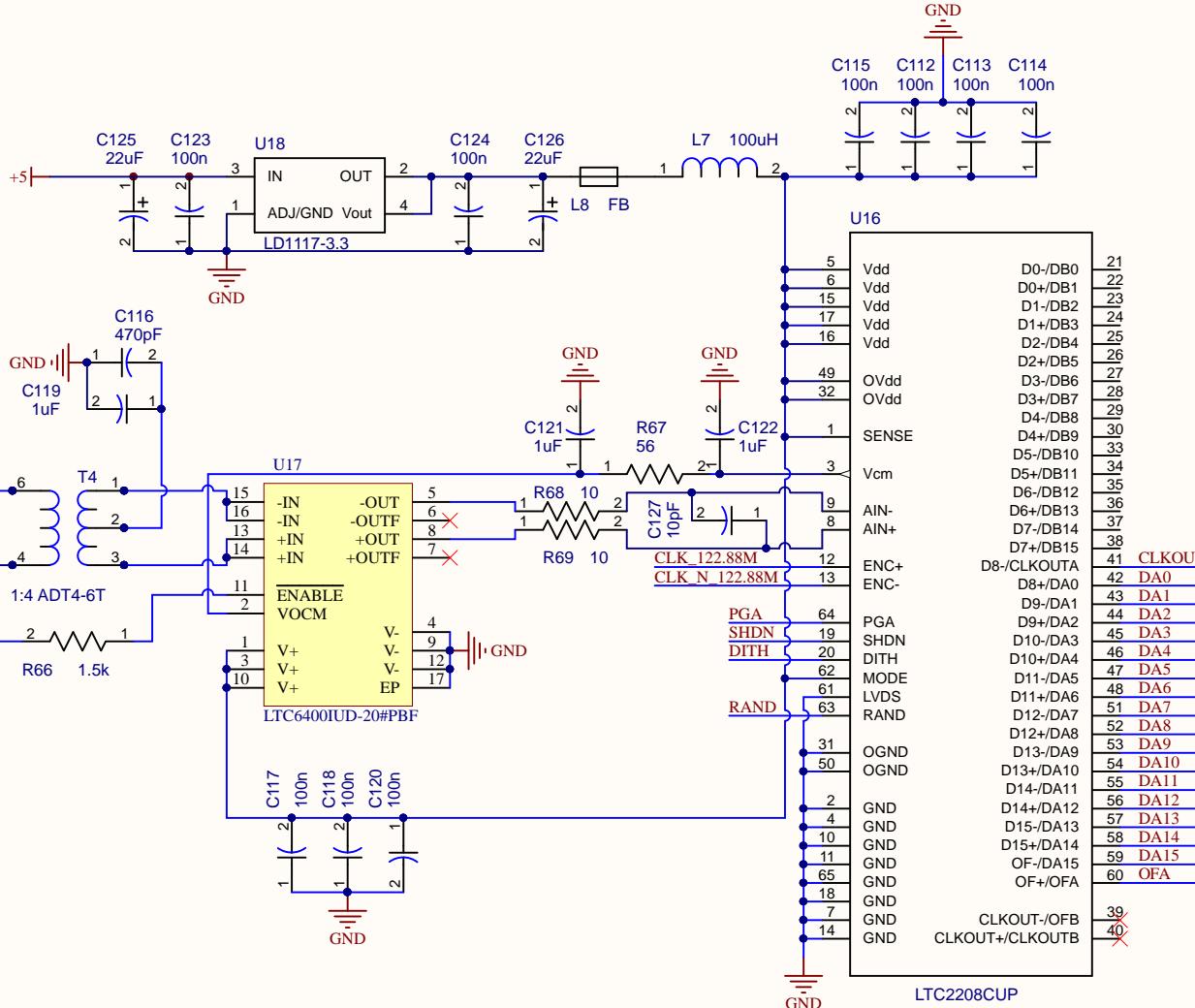
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Date: 09.11.2020	Time: 16:57:46	Sheet 2 of 18
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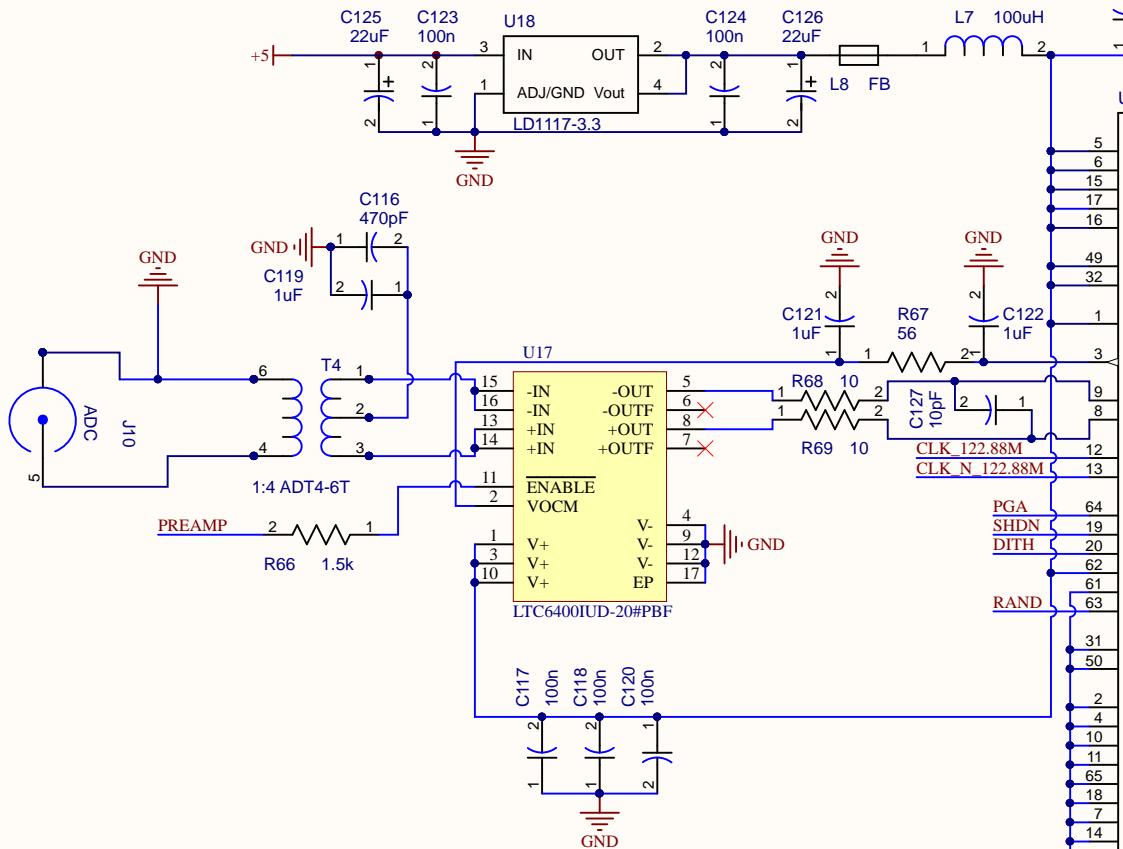
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A



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Title ADC			*
Size: A4	Number:3	Revision:2.0	*
Date: 09.11.2020	Time: 16:57:46	Sheet 3 of 18	*
File: C:\Dropbox\Develop\Projects\WOLF\Schema\ALTIUM_DESIGNER\MOTHERBOARD\ADC.SchDoc			*

A

A

B

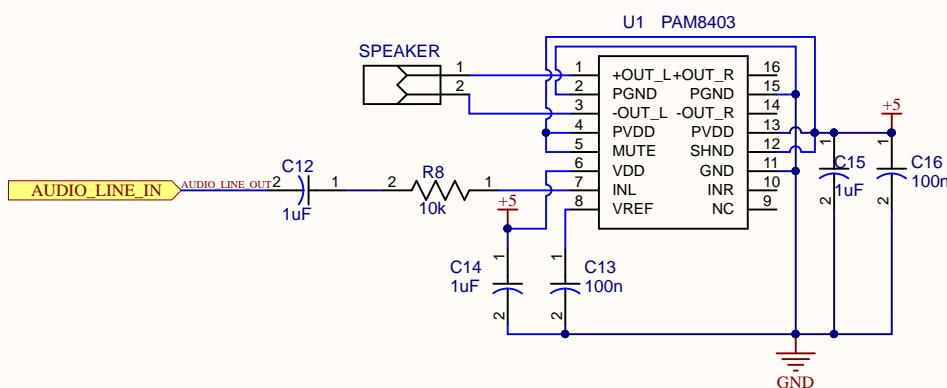
B

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D

Title ***AF AMP***

Size: A4 Number:4 Revision:2.0

Date: 09.11.2020 Time: 16:57:46 Sheet 4 of 18

File: C:\Dropbox\Develop\Projects\WOLF\Schema\ALTIUM_DESIGNER\MOTHERBOARD\AF AMP.SchDoc

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UA3REO
BH8CGJ
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Altium

A

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C

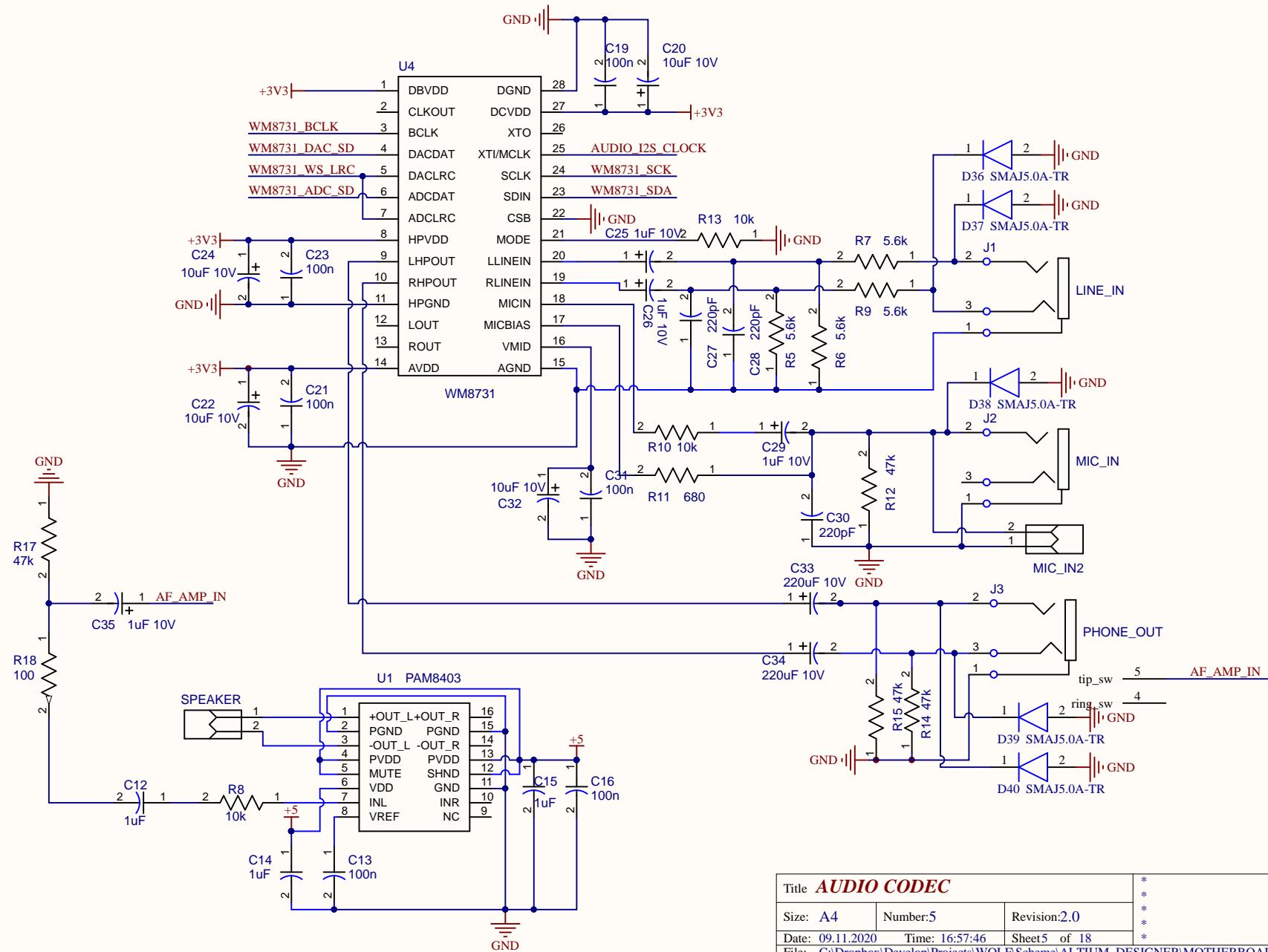
D

A

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D

Title **AUDIO CODEC**

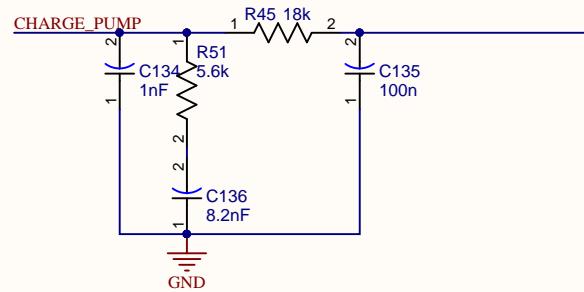
Size: A4 Number:5 Revision:2.0

Date: 09.11.2020 Time: 16:57:46 Sheet 5 of 18

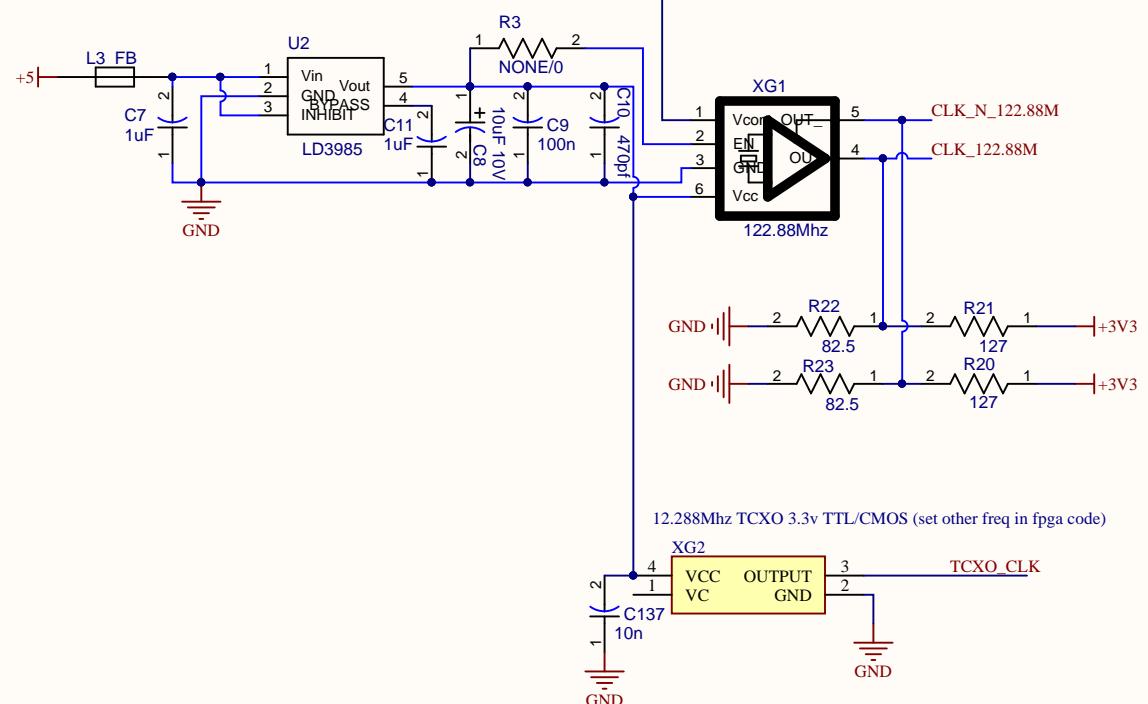
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A



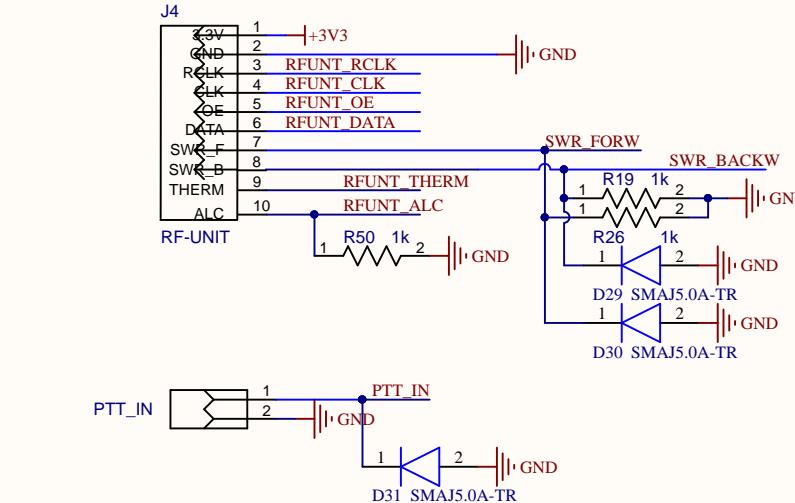
B

Title **CLOCK_GENERATOR**

Size: A4	Number: 6	Revision: 2.0
Date: 09.11.2020	Time: 16:57:47	Sheet 6 of 18
File: C:\Dropbox\Develop\Projects\WOLF\Scheme\ALTIUM_DESIGNER\MOTHERBOARD\CLOCK_GENERATOR.SchDoc		*

Altium

A

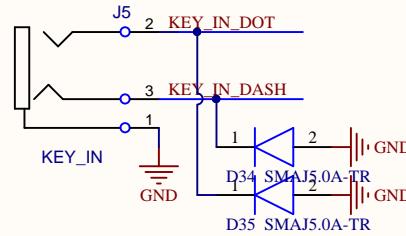


B

FMC_NE1	1	CS 3v3
FMC_A18	2	RS 3v3
FMC_NWE	3	WR GND
FMC_NOE	4	RD GND
STM_NRST	5	RST'MISO
FMC_D0	6	DB'MOSI
FMC_D1	7	DB'WRX
FMC_D2	8	DB2WTX
FMC_D3	9	DB3CLK
FMC_D4	10	DB\$DCS
FMC_D5	11	DB\$AD1C
FMC_D6	12	DB\$AD2C
FMC_D7	13	DB7 E2A
FMC_D8	14	DB8 E2B
FMC_D9	15	DB9 E2S
FMC_D10	16	DB1E1A
FMC_D11	17	DB1E1B
FMC_D12	18	DBAD3C
FMC_D13	19	DB13 5v
FMC_D14	20	DB1GND
FMC_D15	21	DB1GND
PWR_ON	22	PONCAS
PWR_HOLD	23	PHOCAS
	24	3v3

FPC-45P-0.5mm

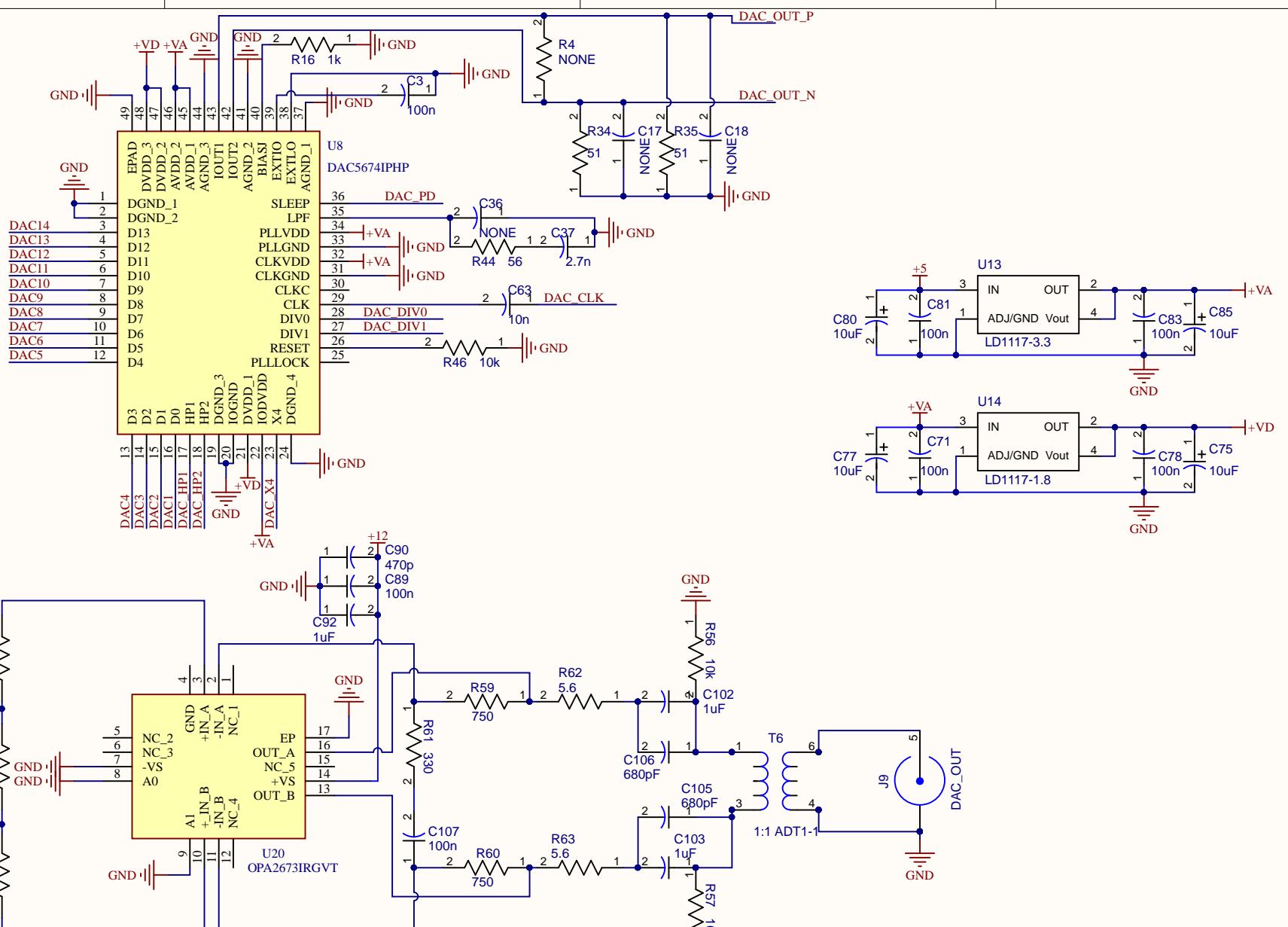
C



D

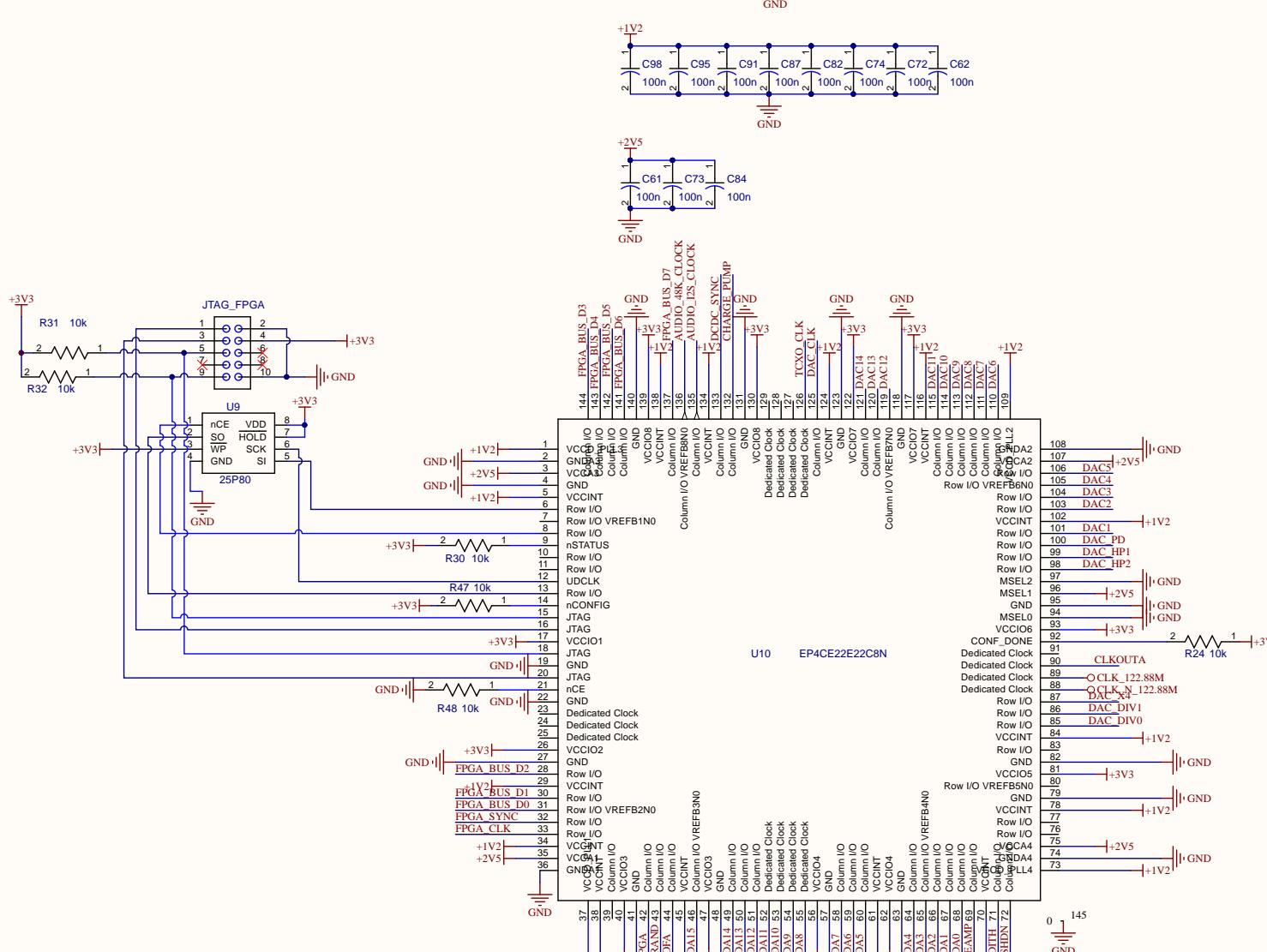
Title CONNECTIONS

Size: A4	Number: 7	Revision: 2.0
Date: 09.11.2020	Time: 16:57:47	Sheet 7 of 18
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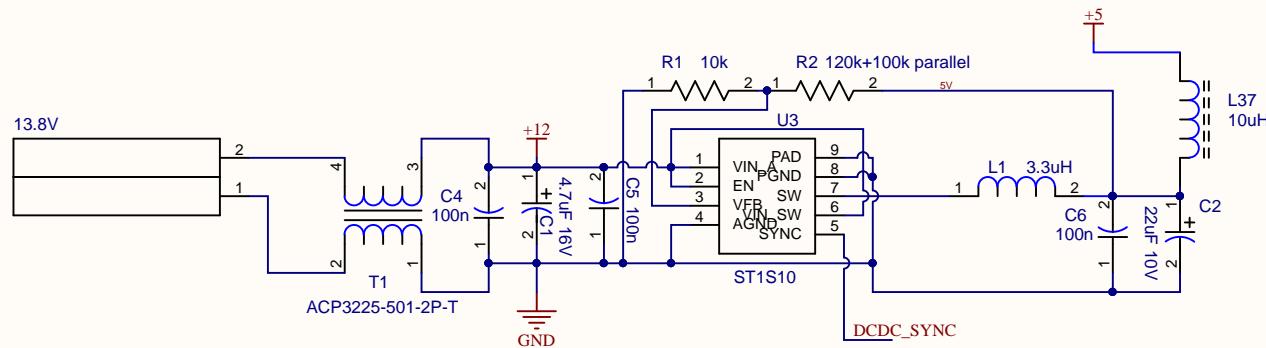


Title DAC		
Size: A4	Number: 8	Revision: 2.0
Date: 09.11.2020	Time: 16:57:47	Sheet 8 of 18
File: C:\Dropbox\Develop\Projects\WOLF\Schema\ALTIUM_DESIGNER\MOTHERBOARD\DAC.SchDoc		*

Altium

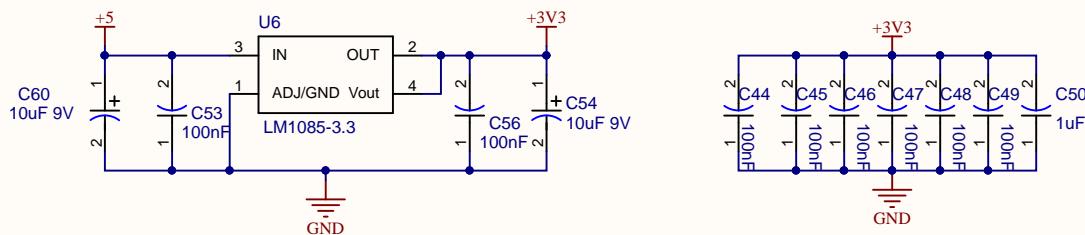


A



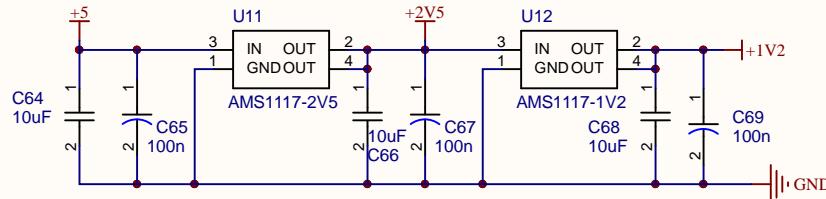
A

B



B

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C

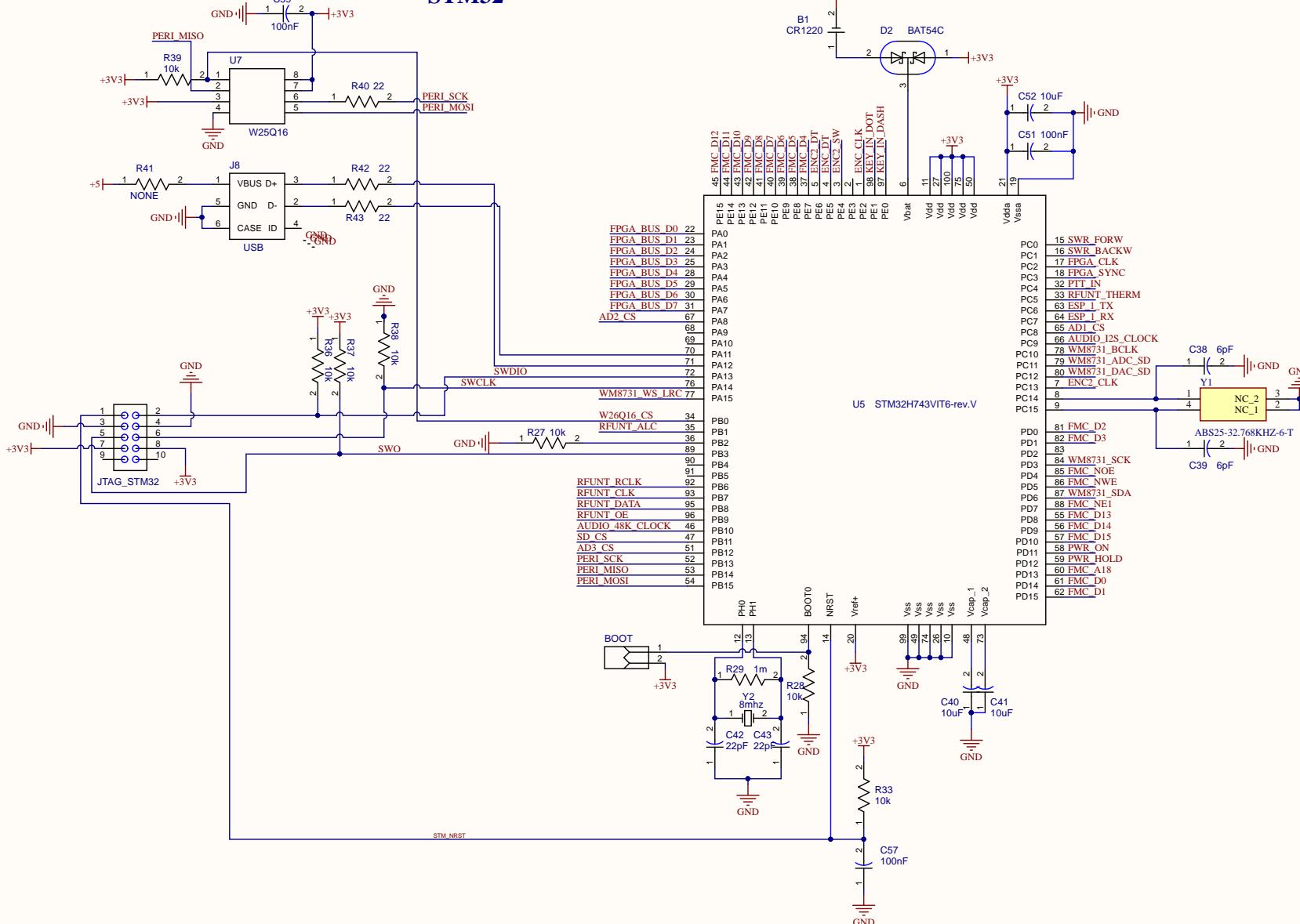
D

Title **POWER**

Size: A4	Number:10	Revision:2.0
Date: 09.11.2020	Time: 16:57:48	Sheet10 of 18
File: C:\Dropbox\Develop\Projects\WOLF\Schema\ALTIUM_DESIGNER\MOTHERBOARD\POWER.SchDoc		*

Altium

STM32

Title **STM32**

Size: A3	Number: 11	Revision: 2.0
Date: 09.11.2020	Time: 16:57:48	Sheet 11 of 18
File: C:\Dropbox\Develop\Projects\WOLF\Scheme\ALTIUM DESIGNER\MOTHERBOARD\STM32.SchDoc		



A

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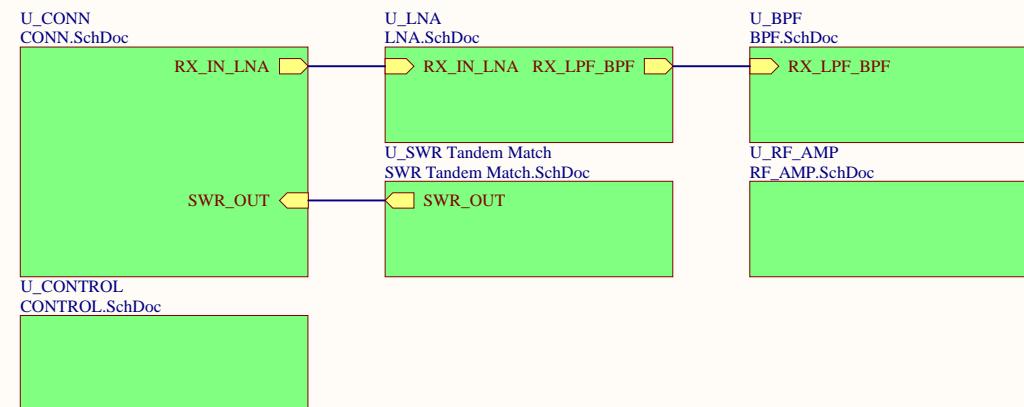
B

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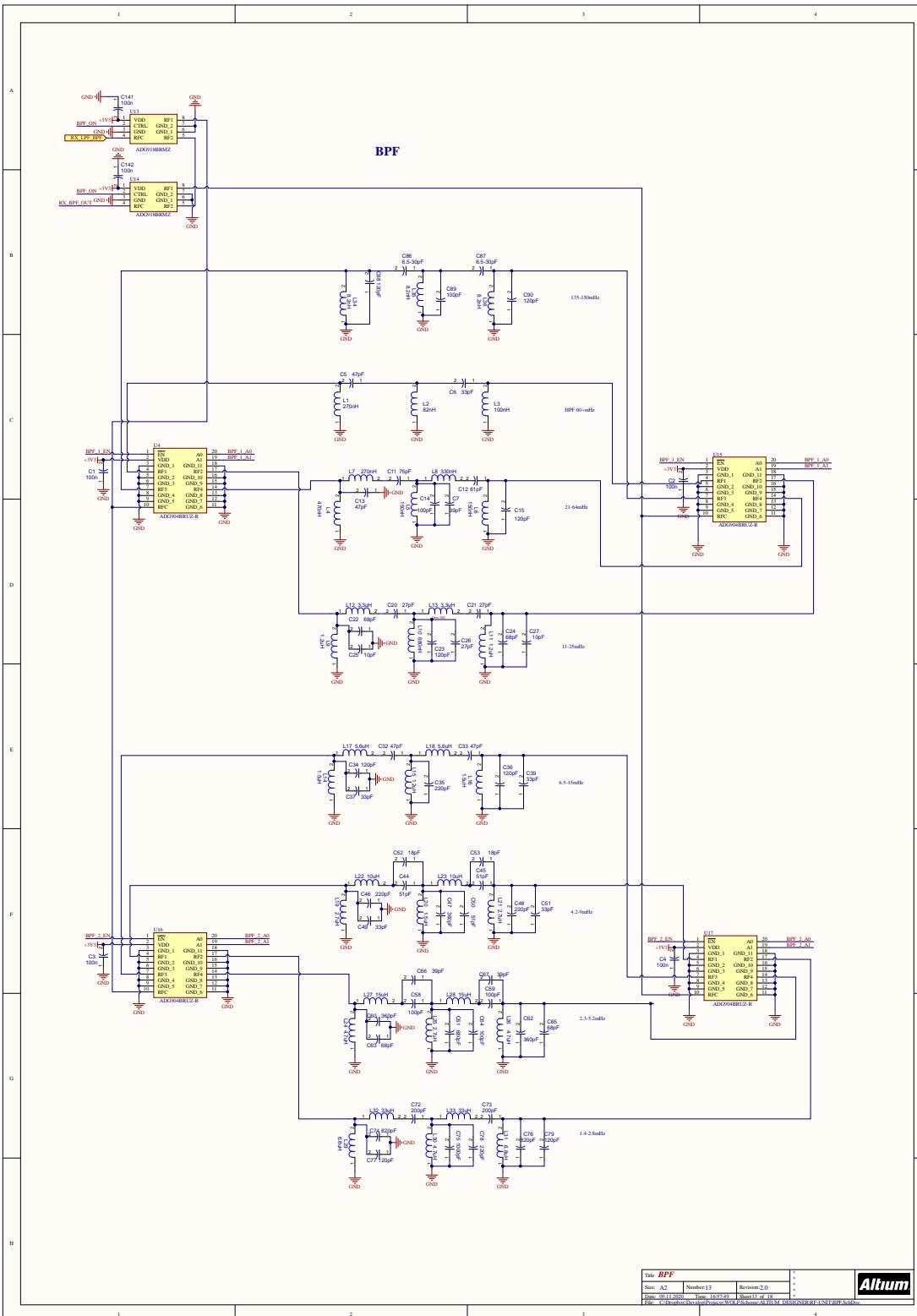
Title ***RF-UNIT***

Size: A4 Number:12 Revision:2.0

Date: 09.11.2020 Time: 16:57:49 Sheet 12 of 18

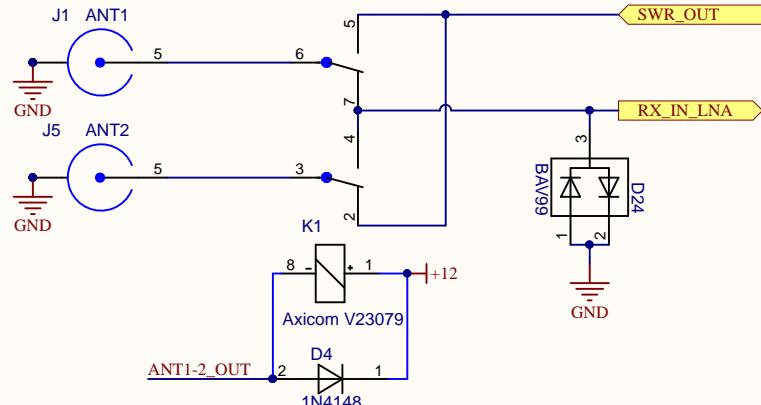
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Altium



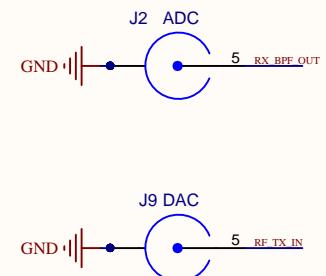
A

TXRX_COMUTATOR

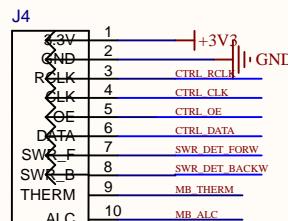


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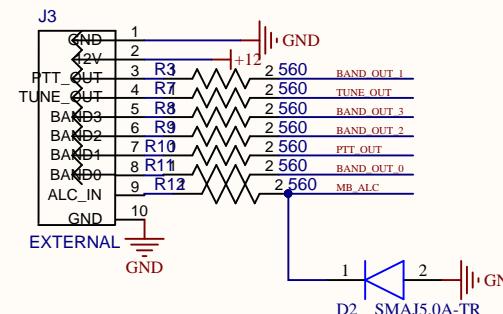
CONN



C



MOTHERBOARD



D

Title **CONN**

Size: A4	Number: 14	Revision: 2.0
Date: 09.11.2020	Time: 16:57:49	Sheet 14 of 18
File: C:\Dropbox\Develop\Projects\WOLF\Schema\ALTIUM_DESIGNER\RF-UNIT\CONN.SchDoc		*

A

A

B

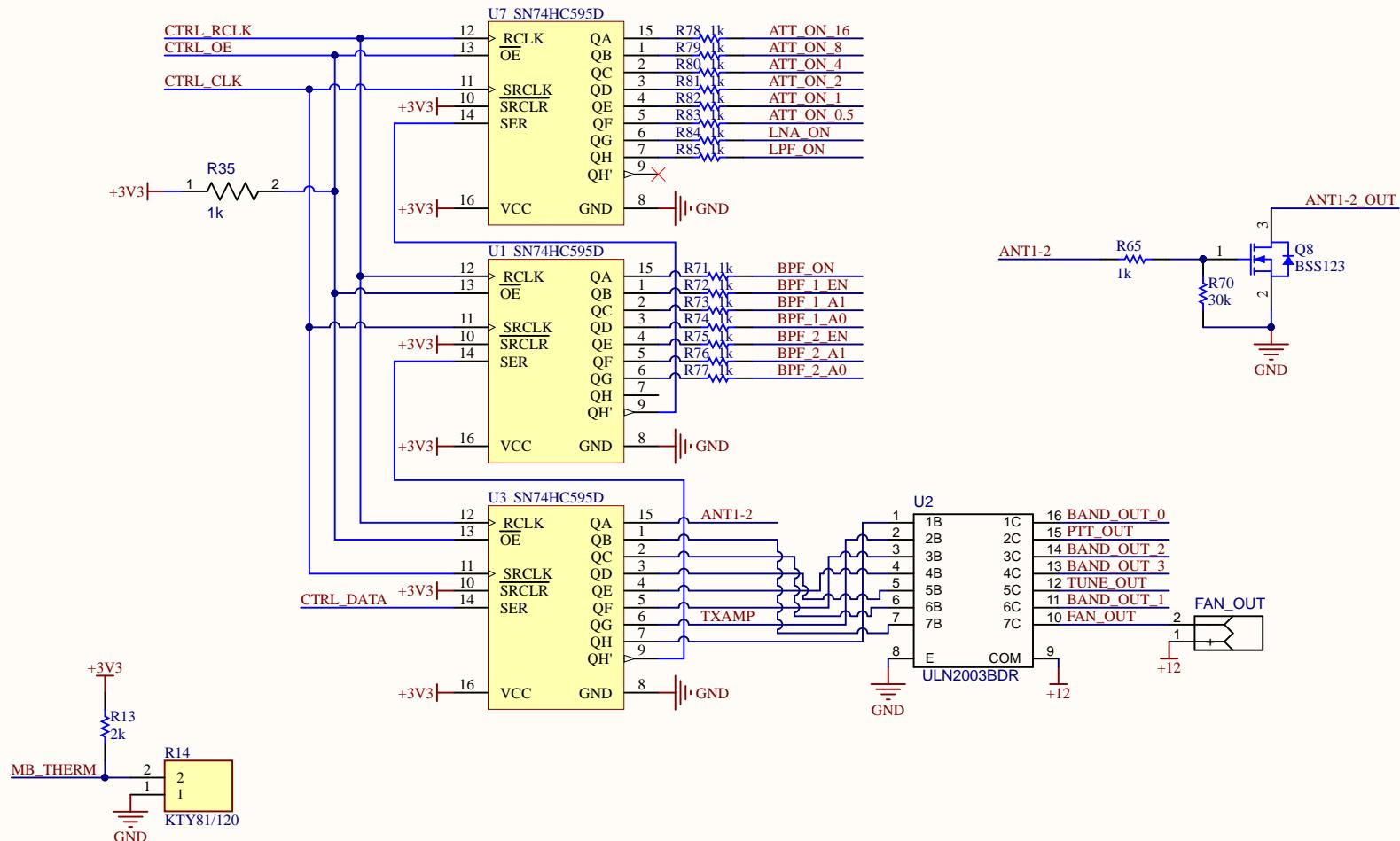
B

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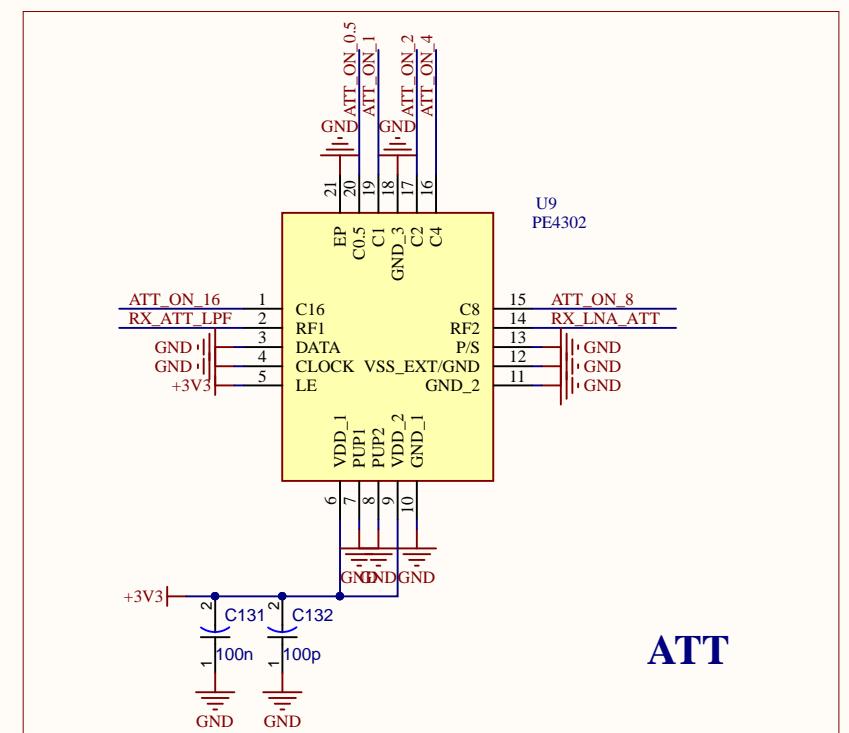
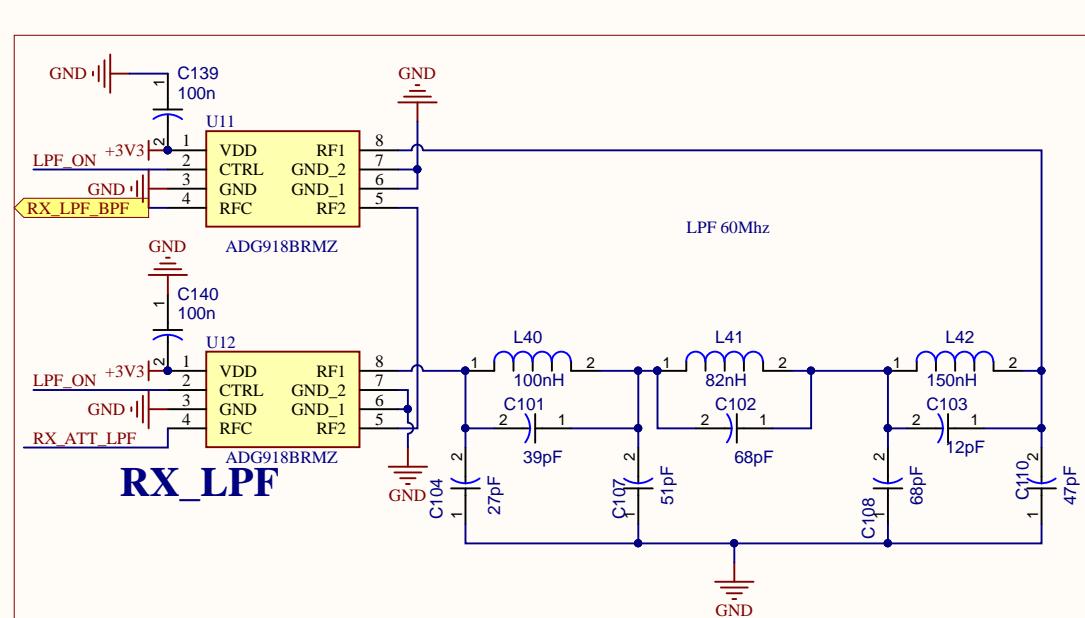
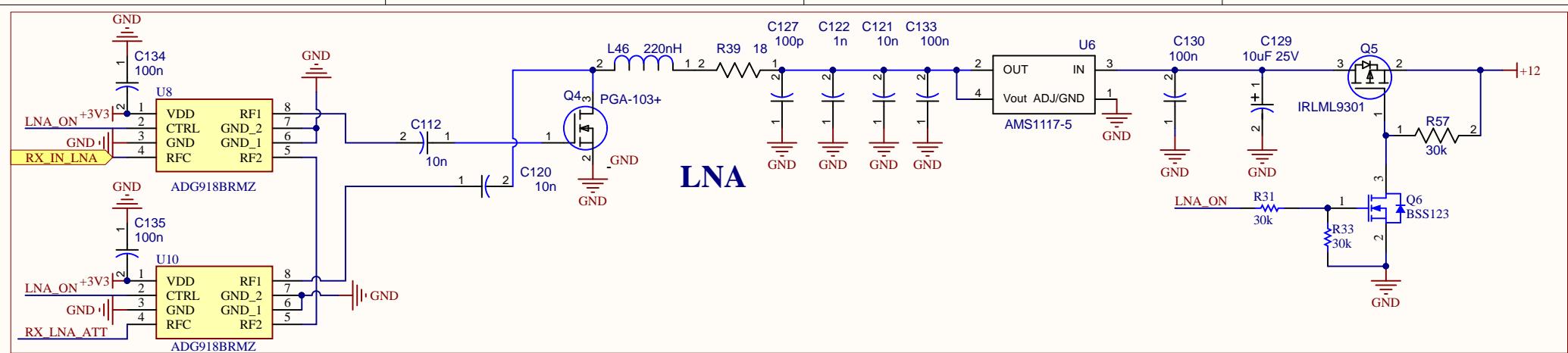
D

D

Title **CONTROL**

Size: A4	Number: 15	Revision: 2.0
Date: 09.11.2020	Time: 16:57:50	Sheet 15 of 18
File: C:\Dropbox\Develop\Projects\WOLF\Scheme\ALTIUM_DESIGNER\RF-UNIT\CONTROL.SchDoc		*

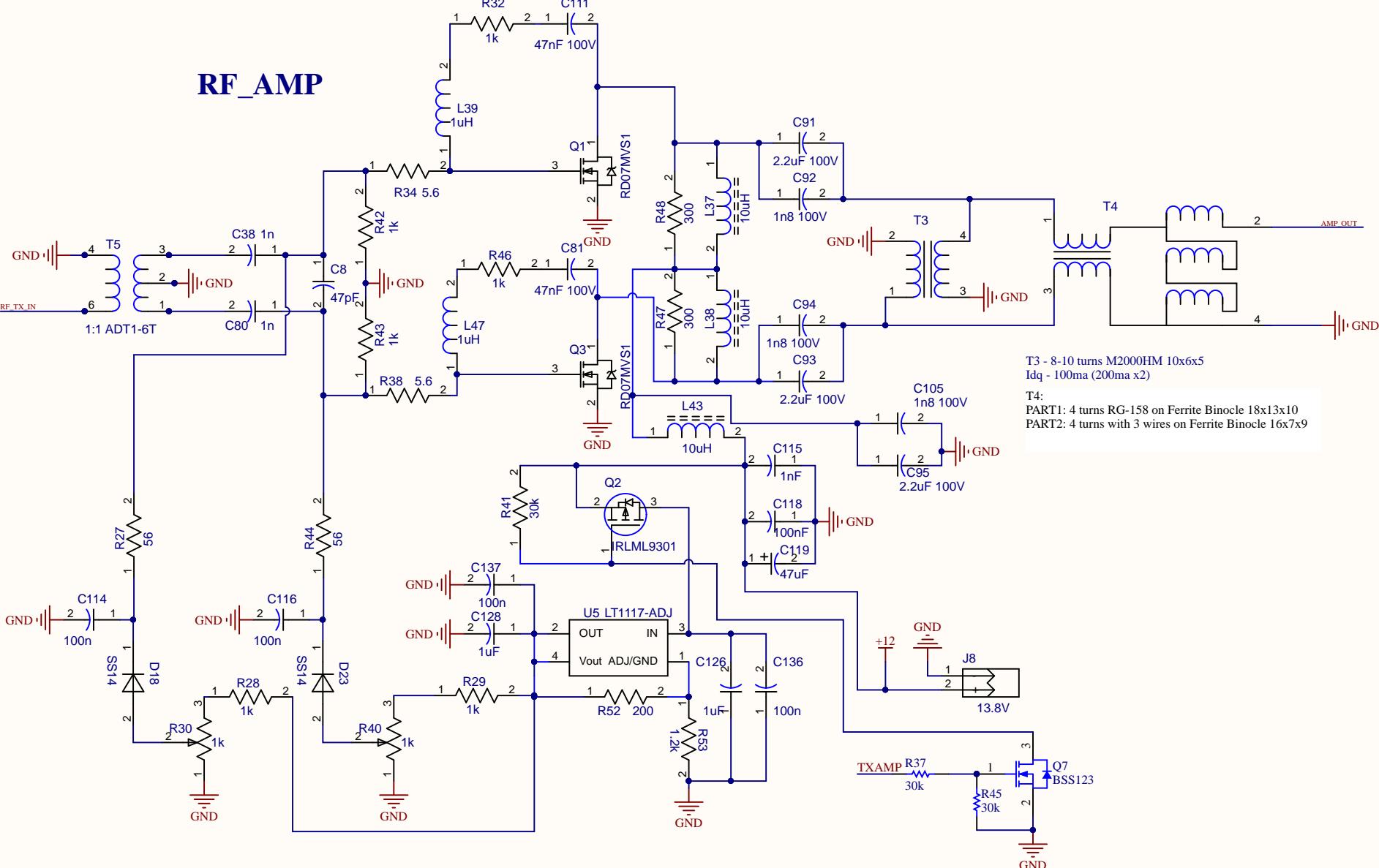
Altium



Title LNA			*
Size: A4	Number: 16	Revision: 2.0	*
Date: 09.11.2020	Time: 16:57:50	Sheet 16 of 18	*
File: C:\Dropbox\Develop\Projects\WOLF\Schema\ALTIUM_DESIGNER\RF-UNIT\LNA.SchDoc			

Altium

RF_AMP



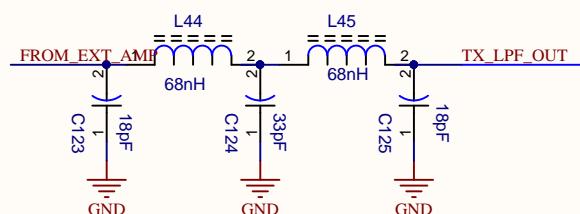
Title **RF_AMP**

Size: A4	Number: 17	Revision: 2.0
Date: 09.11.2020	Time: 16:57:50	Sheet 17 of 18
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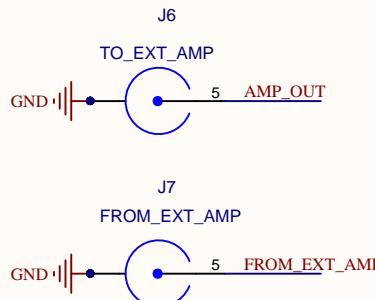
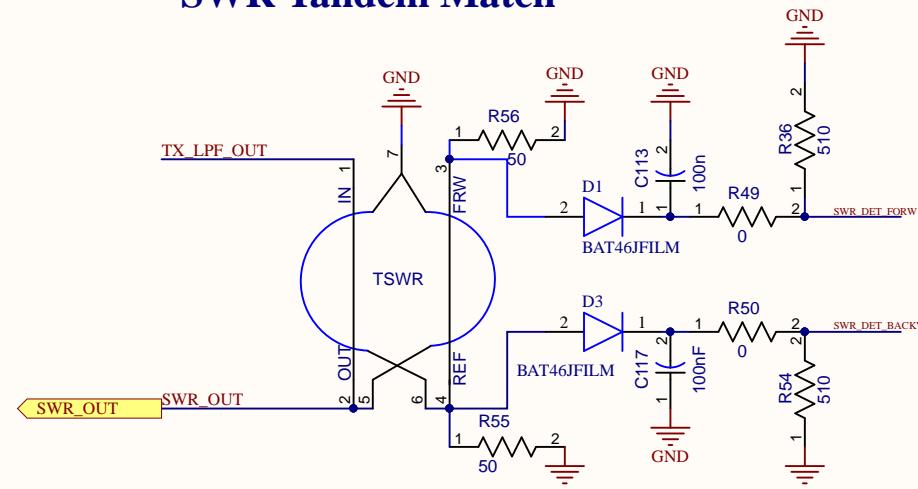
Altium

TX_LPF

LPF 170Mhz



Катушки намотаны проводом 0.5мм на оправке диаметром 5мм, 3.5 витка

**SWR Tandem Match**Title **SWR Tandem Match**

Size: A4 Number:18 Revision:2.0

Date: 09.11.2020 Time: 16:57:50 Sheet 18 of 18

File: C:\Dropbox\Develop\Projects\WOLF\Schema\ALTIUM_DESIGNER\RF-UNIT\SWR Tandem Match.SchDoc

Altium