Compact Metal-Ferroelectric-Insulator-Semiconductor (MFIS) Approaches Versus TCAD For The Modeling Of Ferroelectric Transistors (FeFETs): Percolation, Steep-Subthreshold and Depolarization

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***Abstract*—Ferroelectric-based transistors (FeFETs) are an important emerging technology with applications both as conventional memories and in emerging computational paradigms such as in-memory, neuromorphic and edge computing. A common modeling approach in these structures is to treat the system as a Metal-Ferroelectric-Insulator-Semiconductor (MFIS) effective circuit and use this to both qualitatively and quantitatively model device behavior. However, such approaches completely ignore three-dimensional effects. In this work TCAD is used to conduct three case studies meant to highlight common situations where a non-3D-modeling approach will lead to markedly incorrect predictions of device behavior. These three cases are: 1) channel percolation effects, 2) non-unixial ferroelectricity and 3) geometric depletion effects in SOI, Gate-All-Around (GAA) and nanowire devices. Finally, as a counter-case the observed steep-subthreshold in FeFETs has been argued to be a 3D percolation effect but here it is demonstrated that such behavior is present within an MFIS approach as well.**

***Index Terms*—ferroelectricity, ferroelectric transistors, FeFETs, TCAD, 3D modeling, steep-slope devices, percolation physics**

I. Introduction

Ferroelectric transistors (FeFETs, see Figure 1) are an important emerging technology. Their potential goes beyond being a new type of non-volatile memory into applications for in-memory, neuromorphic and edge computing technologies. Thus, the ability to accurately model and simulate such devices is important and necessary as part of the development of these technologies.

A common approach in the modeling of such devices is a so-called Metal-Ferroelectric-Insulator-Semiconductor (MFIS) compact model where each layer of the gate-stack of an FeFET is treated as an effective circuit (see Figure 2) where the semiconductor channel is modeled with an analytical expression. Such a compact description has great value at providing a qualitative and sometimes quantitative description of the underlying physics but obviously neglects any complexity in the transverse direction of either the channel region of the transistor or the ferroelectric layer itself.

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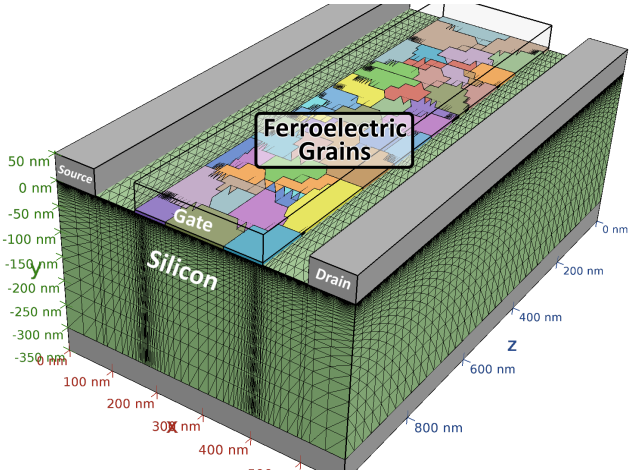

Fig. 1. Planar FeFET device simulated in the GTS Framework with 250 nm x 1 mum gate containing a ferroelectric layer (5 nm, HZO) that has been divided into 50 grains, each with their own ferroelectric model, and a 0.8 nm silicon dioxide layer.

This approach, which treats the ferroelectric layer as a single effective entity is often used despite the fact that real technology-relevant ferroelectrics, such as those based on doped hafnium oxide, are known to be heavily polycrystalline. Thus there are many aspects of the operation of FeFET where a truly 3D TCAD description is absolutely necessary. In this work we will examine three separate cases where an MFIS compact model will lead to markedly different results than a more accurate TCAD description and look at one case that is often claimed to be a 3D effect but is in fact present in an MFIS description as well.

All TCAD simulations were done using the commercial solver GTS Minimos-NT [1] which includes a diverse set

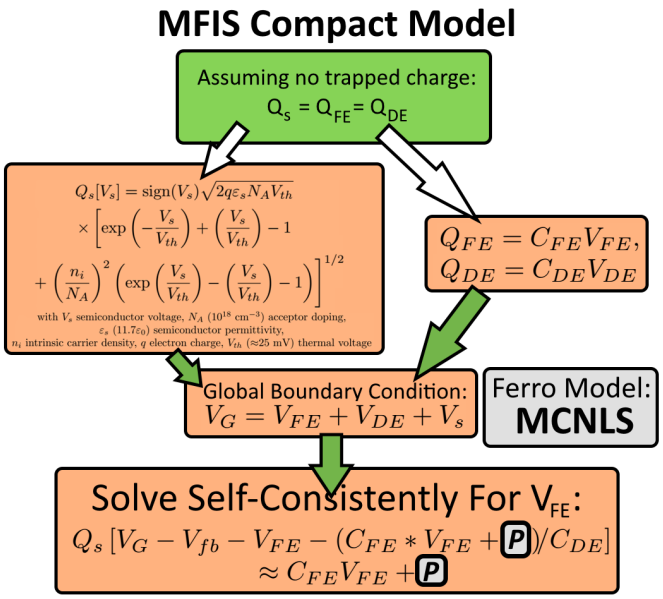

Fig. 2. A Metal - Ferroelectric – Oxide - Semiconductor (MFIS) compact model that models an FeFET as an effective circuit. In both the MFIS and TCAD models the MCNLS ferroelectric model is used.

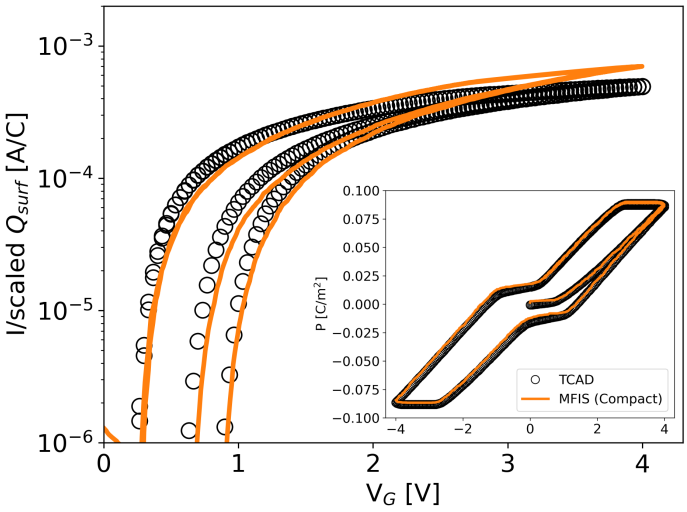

Fig. 3. The $I_D - V_G$ and $P - V_G$ (inset) characteristics produced for both the TCAD (black circles) and the MFIS compact model.

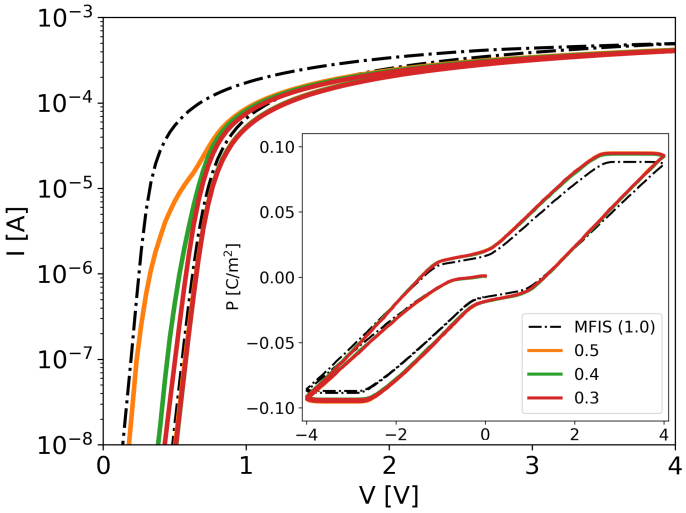

Fig. 4. The $I_D - V_G$ and $P - V_G$ (inset) characteristics of the TCAD device as a fraction of the ferro grains are replaced with non-ferro ones leading to percolation physics in the FeFET channel (e.g. 0.3 = 30% of grains are ferroelectric). In all cases the MFIS model shows full.

of ferroelectric modeling capabilities. The device considered was a planar FeFET (Fig. 1) with a 250 nm x 1 μm gate-stack composed of a 5 nm hafnium zirconium oxide (HZO) and a 0.8 nm silicon dioxide layer. The channel had a bulk doping of 10^{18} cm^{-3} and a source/drain doping of 2×10^{20} cm^{-3}. The ferroelectric layer was divided into 50 grains with each grain's ferroelectric behavior dictated by the Monte Carlo Nucleation-Limited Switching (MCNLS) model as described in [2] and using the experimentally validated parameters also given therein. This MCNLS model was also used to create an MFIS model which self-consistently solves the effective circuit with the well-known analytical result for the surface charge of a semiconductor (Fig. 2).

In order to achieve an estimate of the drain current, I_d, from the MFIS model, the current was assumed proportional to the surface charge density (linear drain current regime). Note that the analytical semiconductor model includes both surface charges and depletion charges, which extend into the bulk of the semiconductor. When estimating I_d only the surface charge should be included as contributing to the drain current through the inversion layer, though the depletion charge is still needed to determine the correct voltages of the stack. Both the TCAD and MFIS layer were then run through a triangular pulse that takes the ferroelectric through its full hysteretic loop and the two models in this case were found to give near identical results (Figure 3).

II. Study #1: Percolation Effects

In real HZO films the "ferroelectric" layer is actually a multi-phasic mixture of ferroelectric and non-ferroelectric (both antiferroelectric and regular dielectric) metallurgical grains. In an MFIS model this reality can be partially handled by considering the "F" layer as a parallel circuit of two capacitors, one ferroelectric one not. Such an approach, however, can never capture effects related to percolative transport in the semiconductor channel. To illustrate this a TCAD simulation was performed for different fractions of ferroelectric grains. The drain current (Figure 4) and average polarization state (inset) of the ferroelectric grains were then plotted as a function of the applied gate voltage. It can be seen that for all ferroelectric fractions that the ferroelectric grains become fully polarized, and an MFIS model would only yield such a result, but for fractions below ∼50% the hysteretic memory window in the drain current effectively disappears. Figure 5 shows the reason for this. The channel region directly below a switched ferroelectric grain will have a higher conductivity

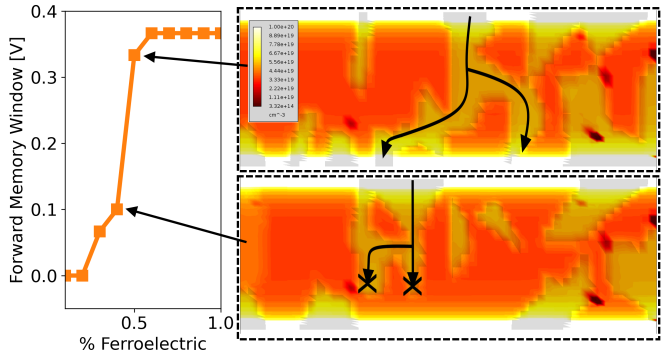

Fig. 5. The threshold voltage shift (i.e. memory window) resulting from a ferroelectric polarizing forward triangular sweep of VG. There is a dramatic closing of the memory window when there are less than 50% ferroelectric grains. The right figures show that this occurs when there is no percolation path through channel regions lying directly underneath a ferroelectric grain.

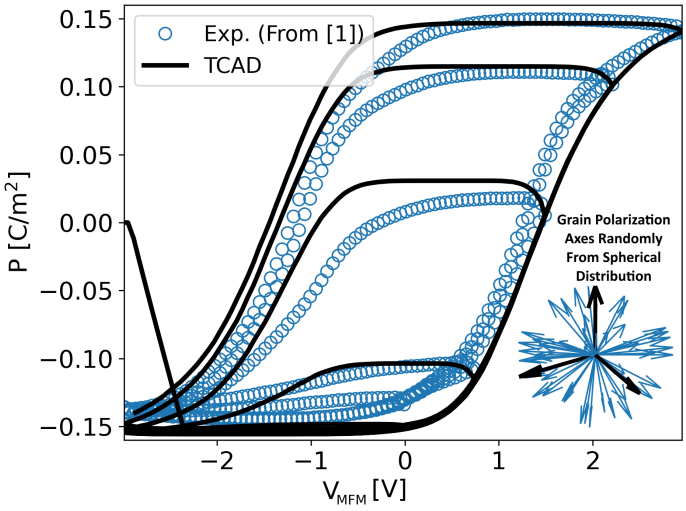

Fig. 6. $P - V_G$ fit of a TCAD model to experiment (From [1]) where non-uniaxial ferroelectricity is assumed with each grain having a polarization axis randomly sampled from a unit sphere.

and thus represents a higher conductive path through the channel if there exists a percolative path for the full channel length. Below ∼50% (the exact value will have some statistical variation) these overlaps disappear and one loses the memory window. This is illustrated in Figure 5.

III. Study #2: Non-Uniaxial Ferroelectricity

An MFIS description inherently assumes that ferroelectricity only occurs along one axis transverse to the gate-stack stacking. However, in polycrystalline ferroelectrics it is possible even for ferroelectric materials that are uniaxial in bulk to exhibit varied polarization axes from grain to grain. Thus an alternative parameterization of a ferroelectric model to experimental data is feasible, where each grain is given a polarization axis uniformly randomly drawn from a unit sphere. Figure 6 shows the result of such an alternative non-uniaxial system as compared to the experimental data in [2].

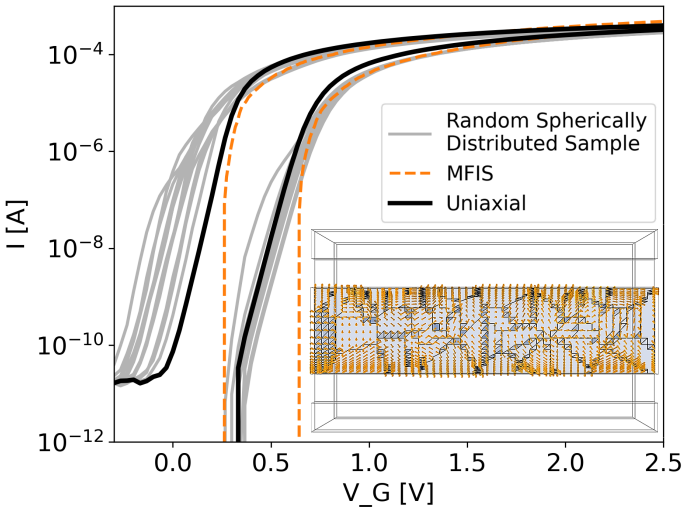

Fig. 7. $I_D - V_G$ for different random samples of spherically distributed polarization axes compared to the MFIS model (inset shows the polarization axes (orange arrows) from a top-view of the device).

Figure 7 shows the drain current characteristics for 6 different random samples of such a system versus the results for the MFIS model (black). It is clear that this 3D effect can have a great impact on the memory window and other device characteristics.

IV. Study #3: Geometric Effects

An MFIS model assumes a semiconductor region that is infinite in extent and ignores any transient effects related to the difficulty of bringing in carriers to the channel for charge compensation. However, the first assumption is not true in many common designs of FeFETs based on Gate-All-Around (GAA), nanowires or SOI where there is no semiconductor bulk from which additional majority carriers can be brought to the channel surface to form an accumulation layer. The second one completely ignores the true 3D aspect of how carriers can or can't be brought in to the channel region and the effect of any penetration of the source and drain regions into the channel. Since majority carriers can not be brought in to form accumulation, when one attempts to switch the ferroelectric layer to the negative polarized state, the majority of the applied negative voltage is instead dropped over the depleted semiconductor and no polarization is produced. The effect of such realities on the hysteresis of a ferroelectric is shown in Figures 8 (source/drain penetration) and 9 (SOI versus planar).

V. Study #4: Steep Slope

As a final study we investigate possible steep-slope characteristics. It has been argued in the literature that the frequently observed sub-60 mV/dec steep slope seen in the reverse current sweep of FeFETs can be attributed to a 3D percolation effect [3] or another 3D effect of negative switching [4]. In Figure 10 we shift the center of the ferroelectric model via varying its intrinsic field (E_i) by 0.5 MV/cm so that its reverse switching

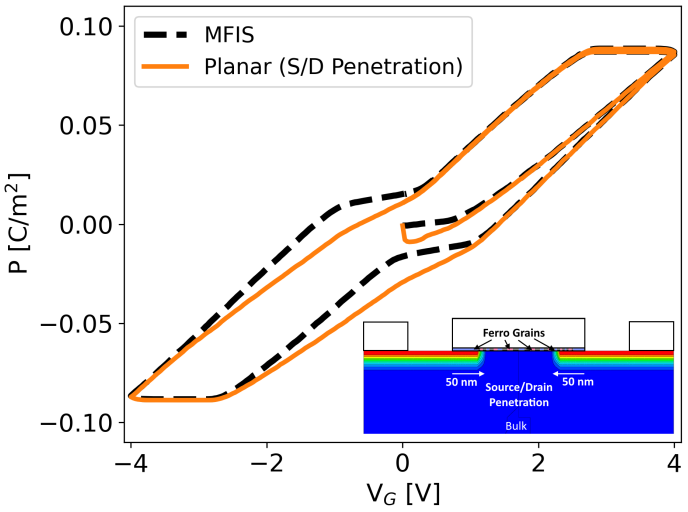

Fig. 8. $P - V_G$ of a regular planar device vs. one where the source/drain regions penetrate into the channel region under the gate. The result is a distortion of the ferroelectric characteristics that would be missed by an MFIS model.

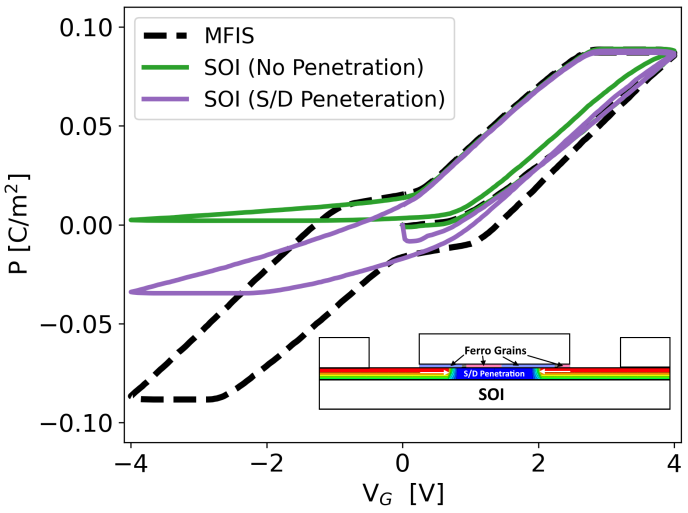

Fig. 9. $P - V_G$ for an SOI device (20 nm channel depth) both with and without S/D penetration. Depolarization from incomplete charge compensation suppresses negative switching.

(i.e. negative slope) portion coincides with the subthreshold voltage range of the FeFET as is argued in [4] to be the origin of this reverse-sweep steep-subthreshold slope. We also remove the 0.8 nm oxide layer to maximize the effect. When taking these measures, both an MFIS and TCAD model exhibit steep-slope reverse sweeps (Figure 11) demonstrating that it is not caused by a 3D effect. In fact, TCAD modeling is needed to demonstrate how steep-slope is actually *suppressed* in the forward sweep as an MFIS model would show that it occurs there too. A further clarification of this effect will be left to a later study.

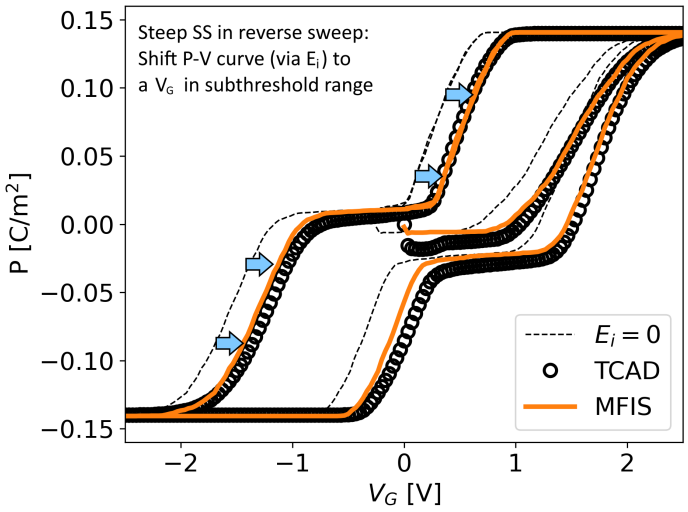

Fig. 10. $P - V_G$ curve that has been shifted (via changing the intrinsic field, E_i, of the ferroelectric model) so that negative polarization coincides with the subthreshold region of the semiconductor.

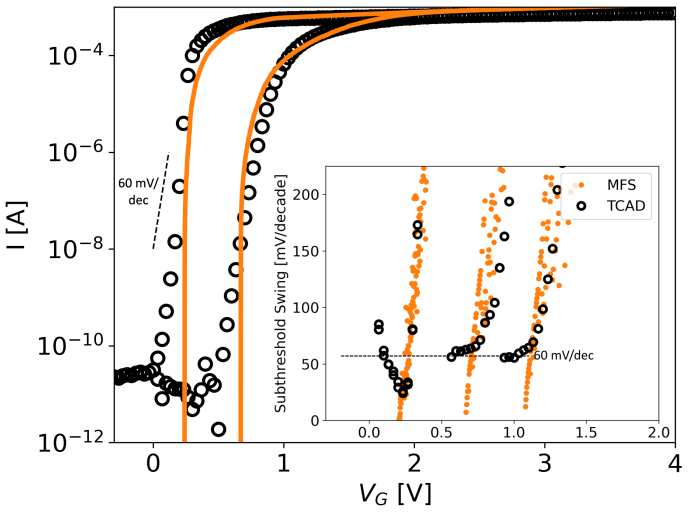

Fig. 11. $I_D - V_G$ showing steep slope switching for the reverse sweep in both the TCAD and MFIS models. Inset shows subthreshold swing at each point.

VI. Conclusion

In this work the short-comings of the oft-used MFIS compact model versus TCAD simulation was demonstrated through the use of three concrete examples. A fourth study provides evidence that reverse current sweep steep-slope behavior is incorrectly attributed to a 3D effect.

References

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