Multi-physics Simulations for Nanoscale CMOS Reliability

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***Abstract*—Multi-scale and multi-physics simulation methods are developed to investigate various reliability problems including trap-induced degradation, self-heating effect and electromigration of interconnects.**

Keywords—CMOS, Reliability, Trap, Electromigration

I. INTRODUCTION

The advanced nano-scale CMOS technologies with new materials, structures and processes introduced, bring the complex multi-physics coupling effects which influence the lifetime of device and circuit [1,2]. The interaction of electric field, thermal effect, stress and trap behavior jointly affects the lifetime of ICs. Hence, the statistics of degradation and time-dependent variability for reliability assessment is a challenge to design and optimize the CMOS ICs.

The electromigration (EM) reliability of interconnects is another reliability issues which becomes more and more challenging in high-density integration [3]. The conventional empirical equation would overestimate the time-to-failure (TTF) of EM due to not taking multi-physics effects into consideration especially in advanced technology nodes. Hence the method to predict EM degradation accuracy and efficient is important to the robust IC design.

Following we will introduce the works in simulation multi-physics effects for nanoscale CMOS reliability [4-11].

II. THERMAL AWARE ENTIRE BIAS SPACE STATISTICAL RELIABILITY SIMULATION FOR NANOSCALE CMOS DEVICES

The device reliability can be attributed to the multi-trap behaviors, including charge trapping from channel/gate, charge detrapping to channel/gate, trap interaction between traps, trap generation and recombination, as shown in the processes (1)-(5) of Fig.1 [8]. 3D-Kinetic Monte Carlo (KMC) based trap dynamics simulator is developed to capture the trap-induced degradation and time-dependent variability for reliability evaluation. Fig.2 shows trap behavior based thermal aware entire bias space statistical reliability simulation method we developed [4-8]. For the given operation conditions (bias sequence and temp(t) by self-heating effect (SHE)), the trap behaviors associated with carrier density, energy distribution, temperature and electric field can be included by the BTE/MC device simulation. The macroscopic degradation and variability can be obtained from charge statistics in the MOSFETs with multilayer gate dielectric under arbitrary Vg/Vd bias combinations. The simulation method shown in Fig.3 is used to calculate self-heated temperature (temp(t)). The simulator is carefully verified and calibrated with the experimental results [12] of different device structure as shown in Fig.4.

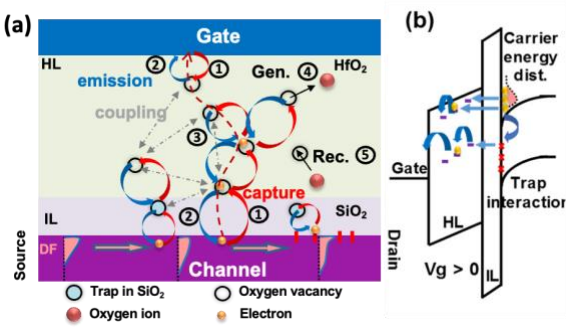

Fig. 1(a) Trap behaviors: (1) charge trapping (2) charge detrapping (3) trap coupling (4) trap generation and (5) recombination induced degradation in the gate dielectrics simulated by 3D-KMC method. (b) the energy band diagram of charge trapping in the nMOSFET with the interfacial layer (IL) and high *k* layer (HL) under stress considering the impact of carrier energy distribution.

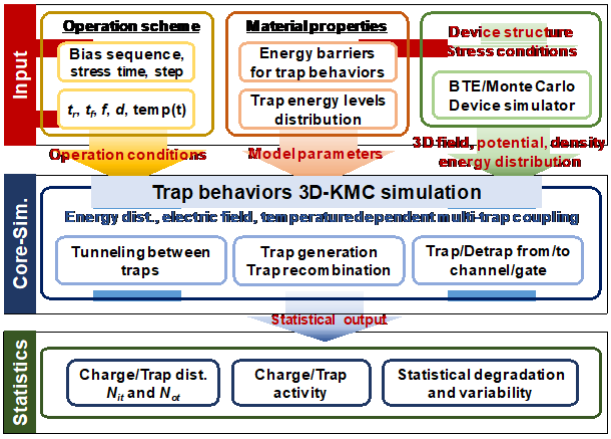

Fig.2 3D-KMC based reliability simulation framework[4,7,8]

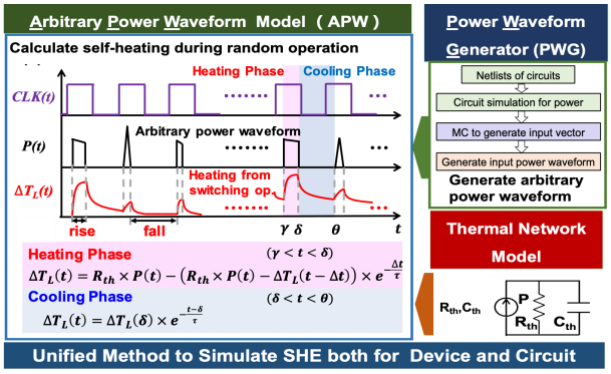

Fig.3 Framework of the unified method to simulate SHE both for device and circuit. Aarbitrary power waveform (APW) self-heating model to calculate self-heating at the arbitrary operation conditions.[4,7,8]

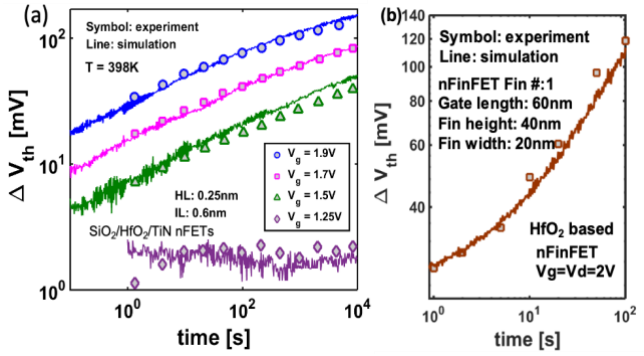

Fig.4 Comparison of simulation results with experiments [12] under various biases conditions both for (a)MOSFET and (b) FinFET.

Since the reliability simulation is based on the statistics of the traps dynamic, the microscopy of trap evolution can be obtained, which can give the physical insight into the macroscopic degradation and variability during stress. The simulated trap and charge distributions evolution in 12nm gate length NS FET after 100s stress under BTI, HCI and OSS (off state stress) stresses is shown in Fig.5 [7].

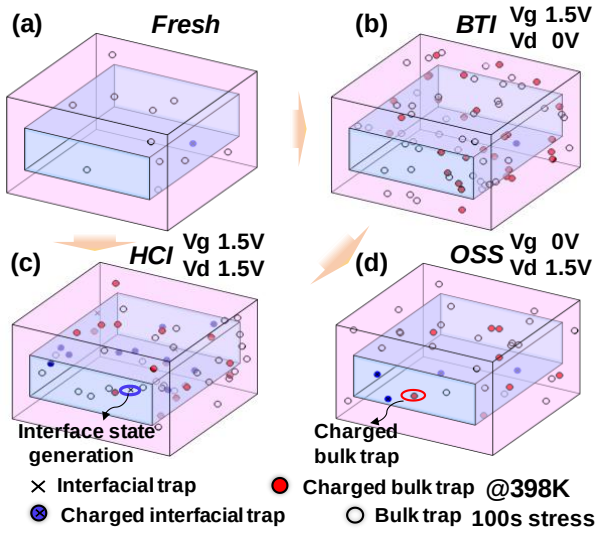

Fig.5 Trap and charge distributions evolution after 100s stress under three bias conditions. Fresh case: traps are randomly distributed and the initial Nit and Not in the NS FETs are $2x10^{10}cm^{-2}$ and $10^{18}cm^{-3}$ [7].

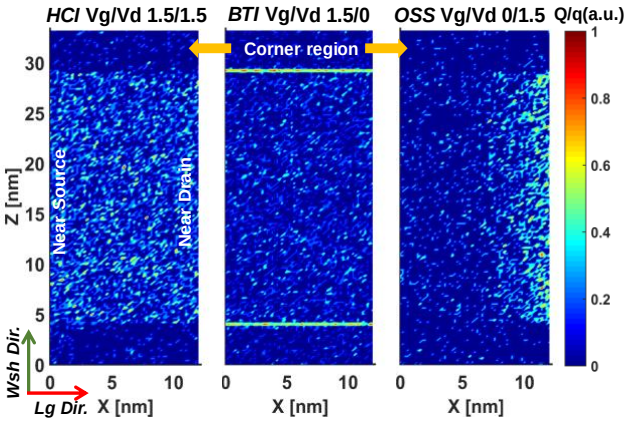

Fig.6 Top view of charge distributions under different biases. Charges are uniform in HCI. For BTI and OSS, charges are mainly located along the dielectric edge and close to the drain, respectively [7].

Top view of statistical charge distributions from 200 samples in the gate dielectrics of NS FETs under HCI, BTI and OSS conditions is shown in Fig.6 [7]. For HCI mode, interfacial charges are mainly close to the drain side and most bulk charges are generated near the source. These two contributions result in the uniform charge distribution in the dielectrics. For BTI mode, partial charges are distributed along the edge of the dielectric corner due to the strong corner effect. For OSS mode, the charges are mainly close to the drain side.

The simulator is capable of statistical reliability simulation for devices stressed by arbitrary mixed bias patterns. Fig.7 plots the simulated threshold degradation (ΔVth) of 12nm gate length NS FETs [8] under arbitrary stress patterns. Fig. 8 shows the mapping of statistical average ΔVth together with the corresponding variance of 200 samples over the entire bias space stressed 100s at 398K [7].

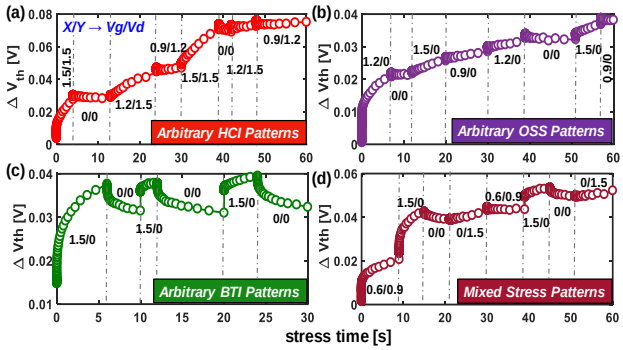

Fig.7 ΔVth degradation under arbitrary stress patterns, including HCI, BTI, OSS and mixed stress[7].

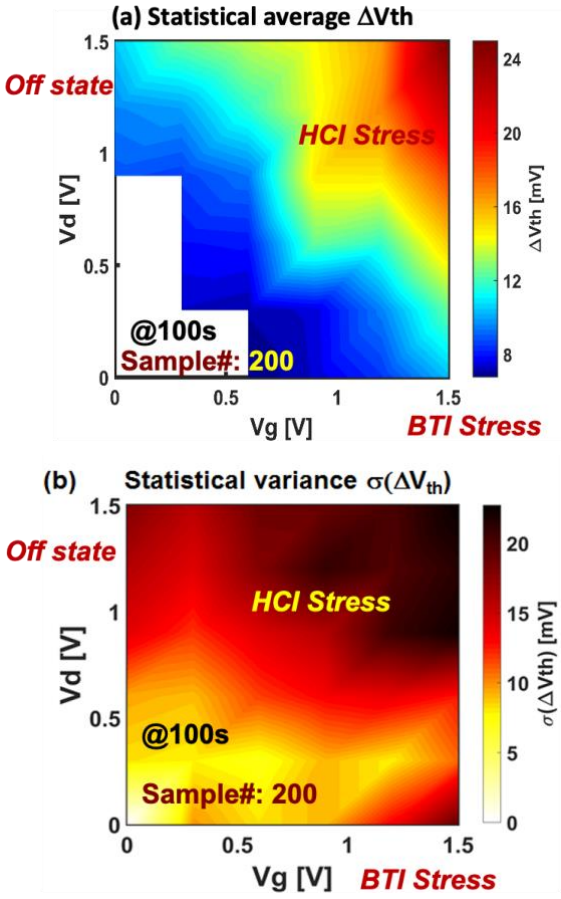

Fig. 8 (a) statistical average ΔVth (b) ΔVth variance mapping after 100s stress over full Vg/Vd bias space at 398K [8].

The CMOS circuits experience various Vg/Vd stress patterns, leading to mixed multi-reliability degradation. Fig. 9 (a)-(b) shows the reliability issues occurring in the CMOS inverter and the t_T definition. The quasi-static simulation with the adaptive time step is employed in the simulator as indicated in Fig.9(c). Fig. 10 shows the frequency-dependent ΔVth in the trainset operations without and with SHE considered. It can be seen that ΔVth is independent of f when f >10Hz, and is weakly increased in the SH case, since SH is accompanied by HCI during the small-duty transition.

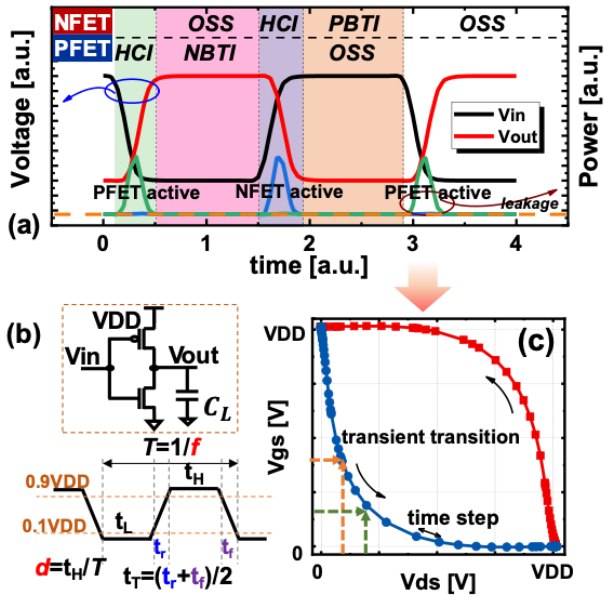

Fig.9 (a) Reliability issues in the inverter when the input voltage is applied. (b) Schematic of effective stress time tT for the transition period. (c) Quasi-static simulation for degradation during the transient transition[8].

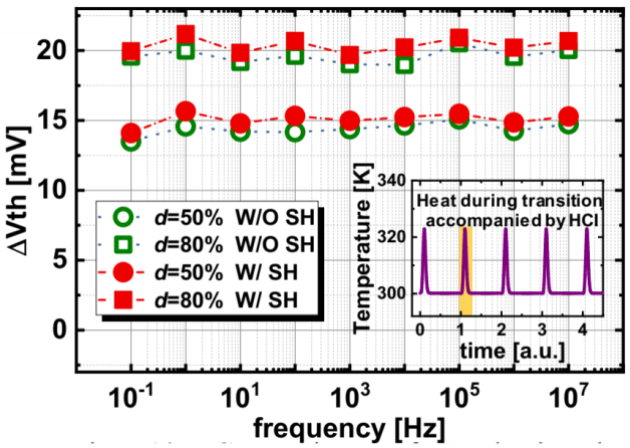

Fig.10 Comparison of ΔVth in the NS nFET based inverter with different AC frequency and duty cycle, respectively, with/without self-heating (SH)[8].

III. Simulation of the Electromigration for Interconnects Design and Reliability Prediction

EM is a typical multi-physics effect of the current driven degradation that forms void due to the mass transport in interconnects. It's strong temperature dependence and sensitive to the process integration including line dimension, interface, grain size, and the complex stress distribution of multilayer interconnect. Usually the time-to-failure (TTF) of EM is projected by the empirical prediction equations [13]. However, the conventional empirical equation would overestimate the time-to-failure (TTF) of EM due to not taking some microscopic physical effects into consideration especially in advanced technology nodes.

We developed a 3D KMC simulator [110,11] as shown in Fig.11 to describe the EM behaviors in multi-layer interconnects based on the microscopic mechanisms during EM including the metal ions activation, hopping and aggregation processes [14-16]. The effects of e-wind, hydrostatic stress and SHE on EM are implemented in the simulator.

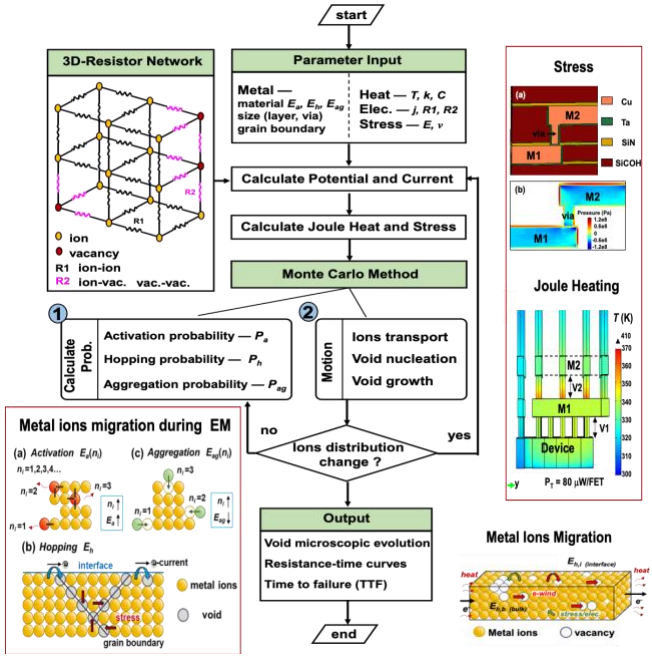

Fig.11 EM simulation flowchart by using 3D KMC method to simulate metal ions migration including the metal ions activation, hopping and aggregation.

In KMC simulator, the grain boundaries of metal interconnect can be generated with dependence on grain sizes. Once the vacancies distribution changed, the heat, electric field, and stress would be updated. To improve the simulation efficiency, the electrical properties of interconnects are calculated by the developed 3D-resistor network. The 3D KMC simulator can visualize the void formation and locates the void positions. Meanwhile, the resistance evolution over time (R-t) and time-to-failure (TTF) can be output during the EM simulation. The simulation results are agreed with the measured [17] cumulative failure distribution and TTF as shown in Fig.12.

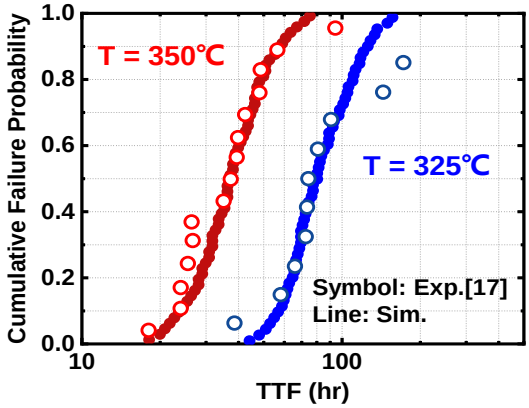

Fig.12 Calibration of cumulative failure distribution between simulation and experimental data [17] at different temperatures.

Fig. 13 shows the simulated void formation in M1-via-M2 Cu interconnects with upstream current flow, which is consistent with the experimental SEM image [17]. The vacancies in the via increase the local current density of the wire, leading to the large Joule heat as shown in Fig. 13 (b-c). The increased temperature accelerates the void growth, further aggravates the EM degradation. Fig. 14 shows the simulated EM degradation with downstream current flow from M2 to M1. The void mainly locates in M1 under the via corresponding to the experimental observation [18]. The resistance shows the less degradation compared to Fig. 13 due to the incomplete void formation.

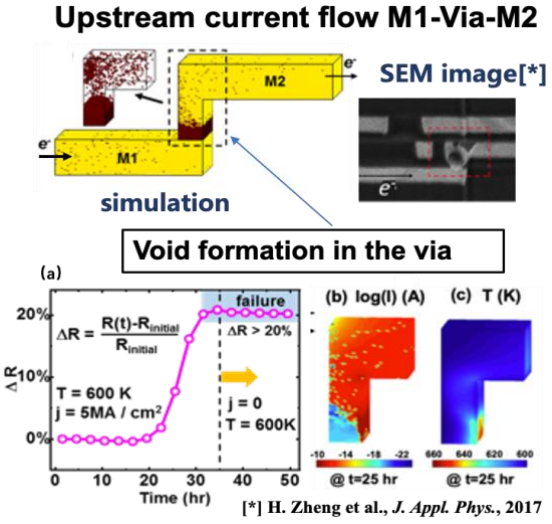

Fig.13 Upstream current flow from M1 to M2 in EM simulation. A void formed in the via (compared with SEM image). (a) R-t curve (b)-(c) local current and temperature distribution of via-M2

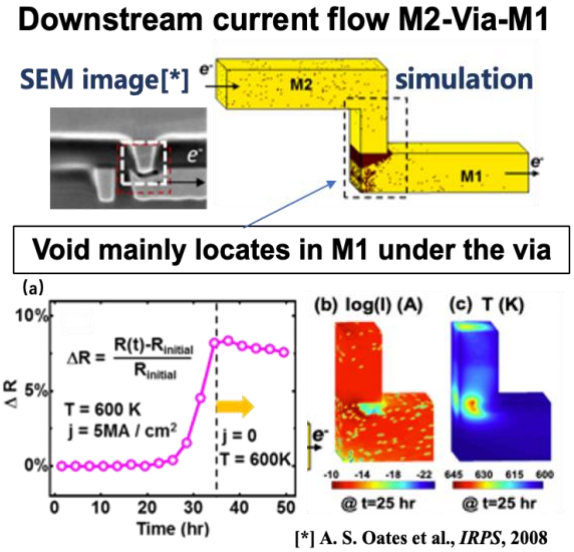

Fig.14 Downstream current flow from M2 to M1 in EM simulation. A void formed in M1 (compared with SEM image). (a) R-t curve (b)-(c) local current and temperature distribution of via-M1.

IV. Summary

Multi-scale simulation methods ranging from 3D KMC trap simulation to stress analysis, are used to simulate the complex multi-physics coupling effects, such as trap-induced degradation and EM. Careful consideration is important to design the interface between different simulation module in order to achieve both high accuracy and efficiency in multi-physics simulations for CMOS reliability.

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