North South University

Department Of Electrical and Computer Engineering

Topic : **ISA Design Project proposal**
Course Name: Computer Organization and Architecture
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Introduction:

Here we are proposing an Instruction Set Architecture (ISA) for a 14 bit CPU. It will be able to perform operations on 14 bit data. For limitation of instructions length we have decided to keep 8 registers in our design 18 instructions and 3 formats.

Operands:

We have decided to keep 3 and 2 operands in our ISA model depending on the format. Mostly they are register based and there are also options for constants or immediate value.

Formats:

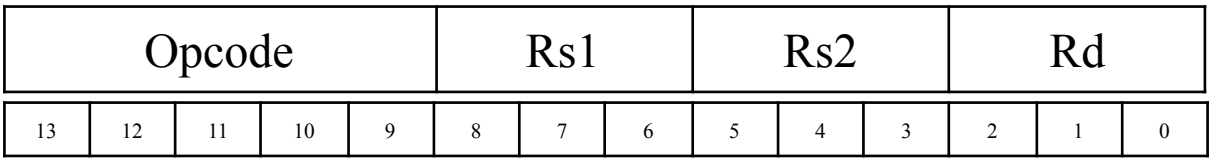
For our ISA design we kept 3 Formats for the instruction.

R - Type,I - Type, J - Type

R - Type Format:

- Bit 0 - 2 destination register.
- Bit 3 - 5 source 2 register.
- Bit 6 - 8 source 1 register.
- Bit 9 - 13 opcode.

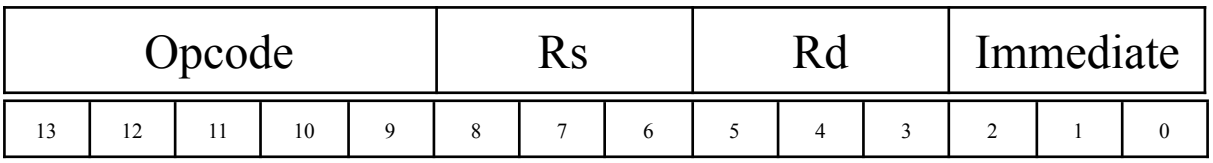
R - Type Format :



I - Type Format:

- Bit 0 - 2 contains an immediate value.
- Bit 3 - 5 destination register.
- Bit 6 - 8 source register.
- Bit 9 - 13 opcode.

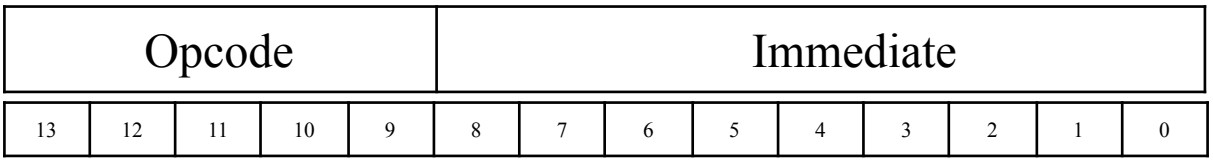
I - Type Format :



J - Type Format:

- Bit 0 - 8 contains an immediate value.
- Bit 9 - 13 opcode.

J - Type Format :



Registers:

There are a total 8 registers numbered from R1 to R7 which are available for load data and make operation. The 1st register named ZERO always keeps value 0 for comparison purposes.

Serial	Name	Access	Comment
1	ZERO	Read only	Always 0
2	R1	R/W	variable
3	R2	R/W	variable
4	R3	R/W	variable
5	R4	R/W	variable
6	R5	R/W	variable
7	R6	R/W	variable
8	R7	R/W	variable

Register R1 to R7 can be used as variables for storing data for ALU operations and can be used for comparison. All these registers have read and write access so any data stored can be overridden. On the other side the 1st or ZERO register is always grounded and always carries value 0 for comparisons. I have only read access and do not have write access.

Instruction Table:

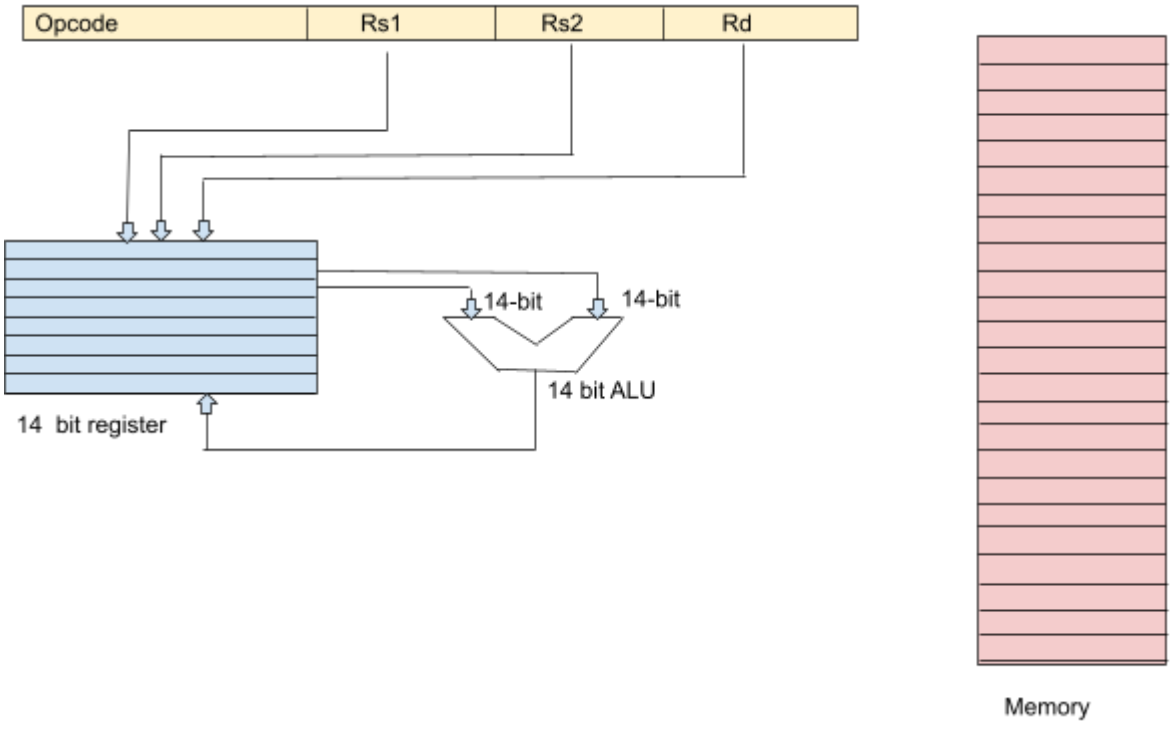
There are a total 18 operations in our ISA design. 4 arithmetic, 5 logical, 4 conditional, 1 unconditional, 2 data transfer and 2 input output operations. Their Name, uses, Type, Example, Meaning and opcodes are given in the table below.

No	***Type***	***NAME***	***Format***	***EXAMPLE***	***Meaning***	***Opcode***
01	Arithmetic	ADD	R	ADD R1, R2, R3	R3 = R1 + R2	00000
02	Arithmetic	ADDi	I	ADDi R1, R2, 5	R2 = R1 + 5	00001
03	Arithmetic	SUB	R	SUB R1, R2, R3	R3 = R1 - R2	00010
04	Arithmetic	SUBi	I	SUBi R1, R2, 5	R2 = R1 - 5	00011
05	Logical	AND	R	AND R1, R2, R3	R3 = R1 & R2	00100
06	Logical	OR	R	OR R1, R2, R3	R3 = R1 | R2	00101
07	Logical	XOR	R	XOR R1, R2, R3	R3 = R1 ^ R2	00110
08	Logical	SLL	I	SLL R1, R2, 4	R2 = R1 << 4;	00111
09	Logical	SRL	I	SRL R1, R2, 4	R2 = R1 >> 4;	01000
10	Conditional	COMP	R	COMP R1, R2, R3	If (R1 < R2) R3 = 1 else R3 = 0	01001
11	Conditional	COMPi	I	COMPi R1, R3, 5	If (R1 < 5) R3 = 1 else R3 = 0	01010
12	Conditional	EQL	I	EQL R1, R2, X	If (R1 == R2) branch to X	01011
13	Conditional	NEQL	I	NEQL R1, R2, X	If (R1 != R2) branch to X	01100
14	Unconditional	JUMP	J	JUMP label	Jumps to where label is	01101
15	Data Transfer	LOAD	I	LOAD R2, R1, 5	Loads value from memory to R1, takes R2 as base address and 5 as offset.	01110
16	Data Transfer	STOR	I	STOR R2 , R1, 5	Stores value saved in R1 into memory, takes R2 as base and 5 as offset.	01111
17	I/O	INPT	I	INPT R1	R1 = User Input	10000
18	I/O	OUT	I	OUT R1,	Print R1 to Display	10001

Addressing Modes:

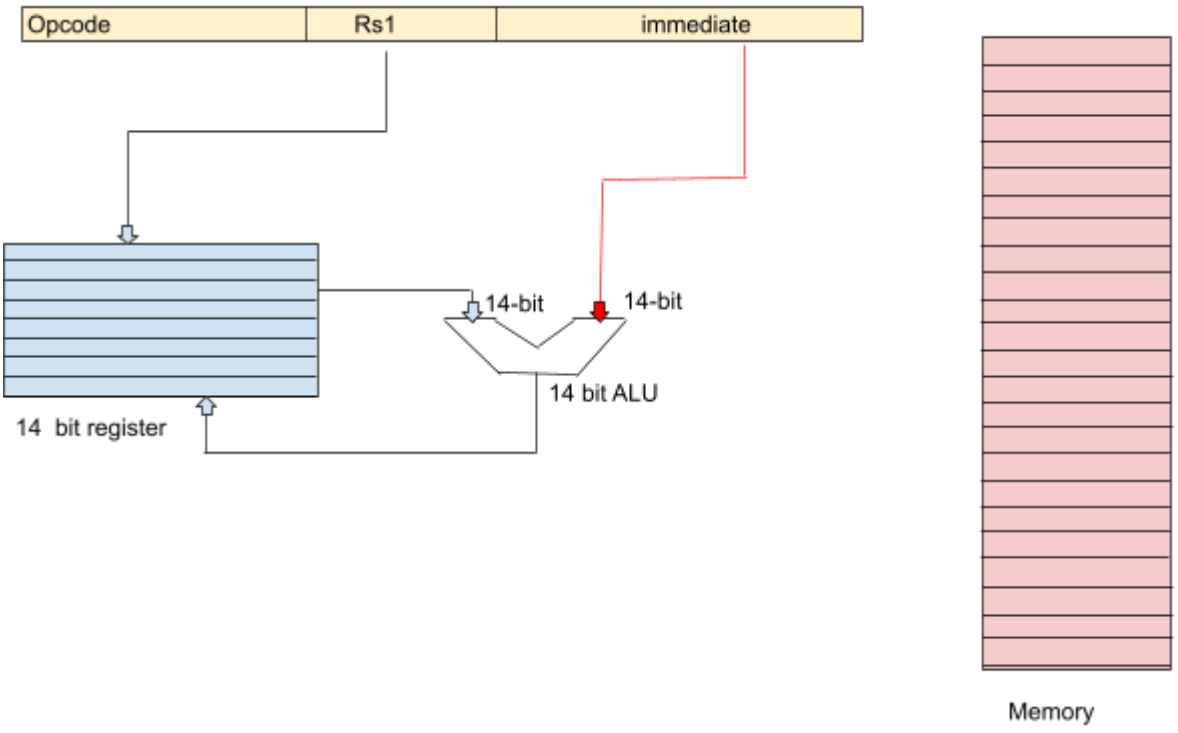
Registrar Addressing:

Here We will provide instruction code or opcode and three register addresses in the instruction. ALU will take two data from one or two registers and store the result after operation into another register according to the providing instruction. In this mode there is no interaction with the *Main Memory.* Here the diagram explains that clearly.

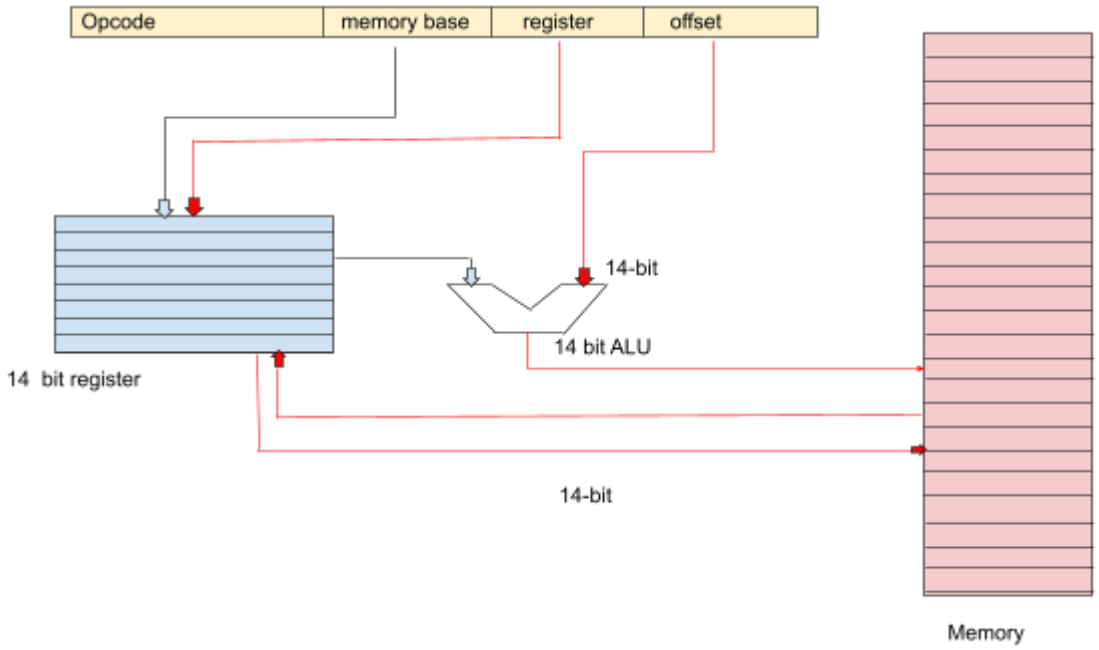


Immediate Addressing:

Here We will provide instruction code or opcode and one register address and an immediate value in the instruction. ALU will take one data from one register, one data from the instruction and store the result after operation into the same register. In this mode there is no interaction with the *Main Memory.* Here the diagram explains that clearly.



Memory (base) Addressing:



Examples For benchmarking

For Loop Execution:

```
for(i = 0; i <7; i++){
        sum += arr[i];
}cout << sum << endl;
[ Registers i = R1,  sum = R2, arr(base) = R3 ]
AND R1, ZERO, R1
#Start
COMPi R1, R4,  7
EQL R4, ZERO, #Break
ADD R3, R1, R4
LOAD R4, R5, 0
ADD R5, R2, R2
ADDi R1, R1, 1
JUMP #Start
#Break
OUT R
```

END OF ASSIGNMENT