

A Smart Hybrid Solid-State-Drive Storage System based on Nonvolatile Storage-Class-Memories - Device, Circuit Design and Architecture -

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Abstract—Recently, there are many kinds of non-volatile memories like NAND flash, MRAM, PCM and ReRAM. Since there is no perfect non-volatile memories, a co-design of device, circuits and systems is essential in order to achieve high performance and reliability with low cost and power consumption. To reach this goal, this paper proposes a hybrid solid-state drive based storage system with optimum circuits to manage each non-volatile memory characteristics.

Keywords—Non-Volatile Memory, Emerging Memory, Solid-State Drive, SSD, Storage-Class-Memory, SCM, NAND flash memory, Magnetic RAM, MRAM, Phase-Change RAM, PCM, PRAM, Resistive RAM, ReRAM, RRAM, Hybrid SSD

I. INTRODUCTION

Computer logic has been improving at an exponential pace, as Moore's law. While a dynamic random access memory (DRAM) is a lot slower than logic, main memory has managed to keep up with the speed of logic by utilizing a hierarchical structure of caches, the upper layers of which use the more expensive and faster static random access memory (SRAM). On the other hand, while storage technology has indeed progressed, it has failed to keep up. There is a massive gap in response times between storage and memory. Thus

recently, faster and more compact solid-state drive (SSD) based on NAND flash memories [1-3] has been replacing more traditional magnetic hard disks drives (HDDs) for many applications. SSDs provide better performance, consume less power and physical durability. However, since NAND flash memory is still much slower than main memory of DRAM. Especially when write operation, it suffers from write-induced wear and has an erase before write limitation.

Then, many alternative non-volatile memories (NVMs) technologies have emerged in recent years. Those technologies provide memory like performance while being persistent like storage and as such, came to be known as a storage class memory (SCM). Table I summarizes a current status of emerging non-volatile memories, for example magnetic RAM (MRAM) [4], phase change RAM (PRAM) [5], resistive RAM (ReRAM) [6]. As Table I shows, there is no perfect non-volatile memory which simultaneously realizes low-cost, high access speed, low energy dissipation and high reliability including infinite write limit. Hence, in order to handle these emerging memories, it is important to develop an optimum circuit design considering device physics and suitable architecture which includes advantages and disadvantages of each non-volatile memories in order to

Table I. SUMMARY OF EMERGING NON-VOLATILE MEMORIES.

	NAND Flash	NOR Flash	MRAM	PRAM	ReRAM
Method	Vth change w/ FN-tunneling	Vth change w/ HCI	Magnetic domain w/ ferro-electric materials	Phase change w/ chalcogenide	Soft-breakdown w/ metal oxide film
Cell size	4F ²	~ 10F ²	6 – 20F ²	4 – 6F ²	5 – 8F ²
Capacity	Excellent	Fair	Poor	Good	Good
Write speed	~ × 1 ms	~ ×10 – 100ns	×1 – ×10 ns	×10 – ×100ns	×10 – ×100ns (w/o verify)
Operating voltage	> 15 V	~12 V	< 2V	< 3 V	~ 3 V
R _{on} /R _{off}	-	-	< ×2	×10 – ×1000	×10 – ×100
Endurance limit	< 10 ⁷ (SLC) < 10 ⁵ (MLC) < 10 ⁴ (TLC)	~ 10 ⁵	Infinite	> 10 ⁸	> 10 ⁸
Pros.	• High cell density	• High speed random access compared to NAND flash	• High speed • Unlimited write cycle • Stable retention	• Well-known materials • Stable write • Unipolar write	• Small write current • Fully compatible with Si-process • High-speed access
Cons.	• High-voltage required • Write cycle limitation • Difficult to scale down due to charge decrease	• Large cell area & cell current (compared to NAND flash)	• Low density (very large cell size) due to small R _{on} /R _{off}	• Large write current • Heat disturbance	• Bipolar write • Unstable read • Initial forming required

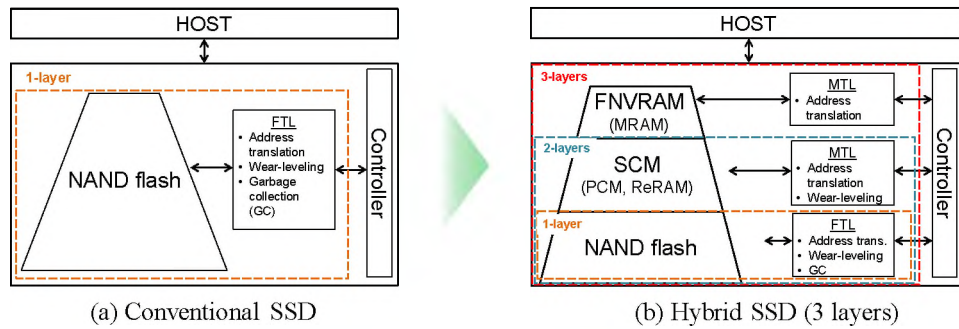


Fig. 1. Proposed hybrid SSD architecture.

enhance access speed and reliability with low power consumption.

Therefore, this presentation will introduce and discuss device characteristic driven circuit design to overcome weak points of each non-volatile memories [7-13]. Also, it will propose a structure and control algorithms with a hierarchical hybrid solid-state drive as shown in Fig. 1 [14-17]. We will first tackle the architecture of hierarchical hybrid SSD: studying the difference between 1-layer, 2-layer and 3-layer designs and the impact of different interconnections on the performance of the system. After that, we will study various control algorithms of such a system and their impact on the performance of the system with a SSD simulator written in C++ language.

REFERENCES

- [1] F. Masuoka, M. Momodomi, Y. Iwata, R. Shiota, "New ultra high density EPROM and flash EEPROM with NAND structure cell," Digest of Technical Papers, 1987 IEEE International Electron Devices Meeting (IEDM1987), pp. 552-555, 1987.
- [2] Y. Iwata, M. Momodomi, T. Tanaka, H. Oodaira, Y. Itoh, R. Nakayama, R. Kirisawa, S. Aritome, T. Endoh, R. Shiota, K. Ohuchi, F. Masuoka, "A high-density NAND EEPROM with block-page programming for microcomputer applications," IEEE Journal of Solid-State Circuits, vol.25, no.2, pp.417-424, 1990.
- [3] T. Tanaka, M. Helm, T. Vali, R. Ghodsi, K. Kawai, J.K. Park, S. Yamada, F. Pan, Y. Einaga, A. Ghalam, T. Tanzawa, J. Guo, T. Ichikawa, E. Yu, S. Tamada, T. Manabe, J. Kishimoto, Y. Oikawa, Y. Takashima, H. Kuge, M. Morooka, A. Mohammadzadeh, J. Kang, J. Tsai, E. Sirizotti, E. Lee, L. Vu, Y. Liu, H. Choi, K. Choen, D. Song, D. Shin, J. H. Yun, M. Piccardi, K.F. Chan, Y. Luthra, D. Srinivasan, S. Deshmukh, K. Kavalipurapu, D. Nguyen, G. Gallo, S. Ramprasad, M. Luo, Q. Tang, M. Incarnati, A. Macerola, L. Pilolli, L. De Santis, M. Rossini, V. Moschiano, G. Santin, B. Tronca, H. Lee, V. Patel, T. Pekny, A. Yip, N. Prabhu, P. Sule, T. Bemalkhedkar, K. Upadhyayula and C. Jaramillo "A 768Gb 3b/cell 3D-floating-gate NAND flash memory," Digest Technical Papers, 2016 IEEE International Solid-State Circuits Conference (ISSCC2016), pp. 142-143, 2016.
- [4] H. Noguchi, K. Ikegami, S. Takaya, E. Arima, K. Kushida, A. Kawasumi, H. Hara, K. Abe, N. Shimomura, J. Ito, S. Fujita, T. Nakada, H. Nakamura, "4Mb STT-MRAM-based cache with memory-accessaware power optimization and write-verify-write / read-modify-write scheme," Digest Technical Papers, 2016 IEEE International Solid-State Circuits Conference (ISSCC2016), pp. 132-133, 2016.
- [5] W. Khwa, M. Chang, J. Wu, M. Lee, T. Su, K. Yang, T. Chen, T. Wang, H. Li, M. Brightsky, S. Kim, H. Lung and C. Lam, "A resistance-drift compensation scheme to reduce MLC PCM raw BER by over 100x for storage-class memory applications," Digest Technical Papers, 2016 IEEE International Solid-State Circuits Conference (ISSCC2016), pp. 134-135, 2016.
- [6] R. Fackenthal, M. Kitagawa, W. Otsuka, K. Prall, D. Mills, K. Tsutsui, J. Javanifard, K. Tedrow, T. Tsushima, Y. Shibahara and G. Hush, "A 16Gb ReRAM with 200MB/s write and 1GB/s read in 27nm technology," Digest Technical Papers, 2014 IEEE International Solid-State Circuits Conference (ISSCC2014), pp. 134-135, 2014.
- [7] K. Johguchi, T. Shintani, T. Morikawa, K. Yoshioka, K. Takeuchi "x10 fast write, 80% energy saving temperature controlling set method for multi-level cell phase change memories to solve the scaling blockade," Elsevier Solid-State Electronics, Vol. 81, pp. 78-85 2013.
- [8] T. Egami, K. Johguchi, S. Yamazaki, K. Takeuchi, "Investigation of multi-level-cell and SET operations on super-lattice phase change memories," Japanese Journal of Applied Physics (JJAP), Vol. 53(4S), 04ED02, 2014.
- [9] K. Johguchih, T. Egami, K. Takeuchi, "Highly reliable, low-power super-lattice phase-change memory without melting and write-pulse down slope," Proceedings of 2013 IEEE International Reliability Physics Symposium (IRPS2013), :MY.5.1, 2013.
- [10] K. Johguchi, T. Egami, K. Miyaji, K. Takeuchi "A temperature tracking read reference current and write voltage generator for multi-level phase change memories," IEICE Transactions on Electronics, Vol. E97-C(4), pp. 342-350, 2014.
- [11] K. Johguchi, K. Yoshioka, K. Takeuchi, "NAND phase change memory with block-erase architecture and pass-transistor design requirements for write and disturbance," IEICE Transactions on Electronics, Vol. E97-C(4), pp. 351-359, 2014.
- [12] K. Higuchi, K. Miyaji, K. Johguchi, K. Takeuchi, "Endurance enhancement and high speed set/reset of 50nm generation HfO₂-based resistive random access memory (ReRAM) cell by intelligent set/reset pulse shape optimization and verify scheme" Japanese Journal of Applied Physics (JJAP), 51(2S), 02BD07, 2012.
- [13] T. Ogura-Iwasaki, S. Ning, K. Takeuchi, "Stability conditioning to enhance read stability 10x in 50nm AlxOy ReRAM," Proceedings of IEEE International Memory Workshop, pp. 44-47, 2013.
- [14] H. Fujii, K. Miyaji, K. Johguchi, K. Higuchi, C. Sun, K. Takeuchi "x11 performance increase, x6.9 endurance enhancement, 93% energy reduction of 3D TSV-integrated hybrid ReRAM/MLC NAND SSDs by data fragmentation suppression," Digest of Technical Papers, IEEE Symposium on VLSI Circuits, :pp. 134-135, 2012.
- [15] S. Hachiya, K. Johguchi, K. Miyaji, K. Takeuchi, "Hybrid triple-level-cell (TLC) /multi-level-cell (MLC) NAND flash storage array," Japanese Journal of Applied Physics (JJAP), Vol. 53(4S), 04EE04, 2014.
- [16] H. Arafat, R. Shimizu, K. Johguchi, "Hierarchical hybrid solid state drive," Proceedings of 2018 IEEE Region 10 Conference, 2018.
- [17] H. Arafat, R. Shimizu, K. Johguchi, "Data management methods for hierarchical hybrid SSD," IEICE General Conference, 2019.