

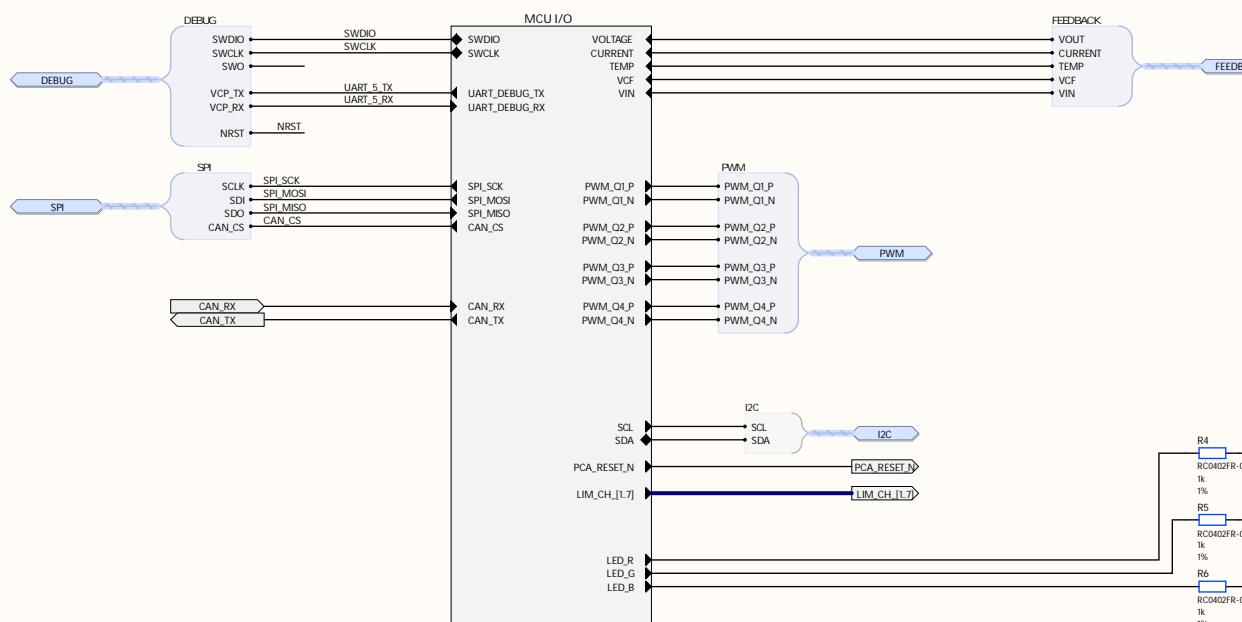
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project: mR Power Module rev: A.1 date: 08/03/2023

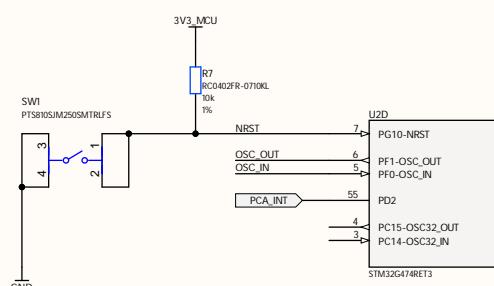
drawn by: Witold Woszczyna size: A3 sheet 1 of 19



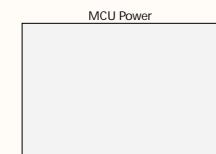
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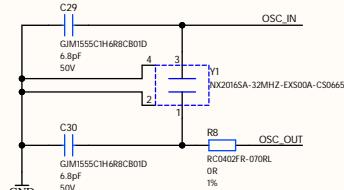
A



B



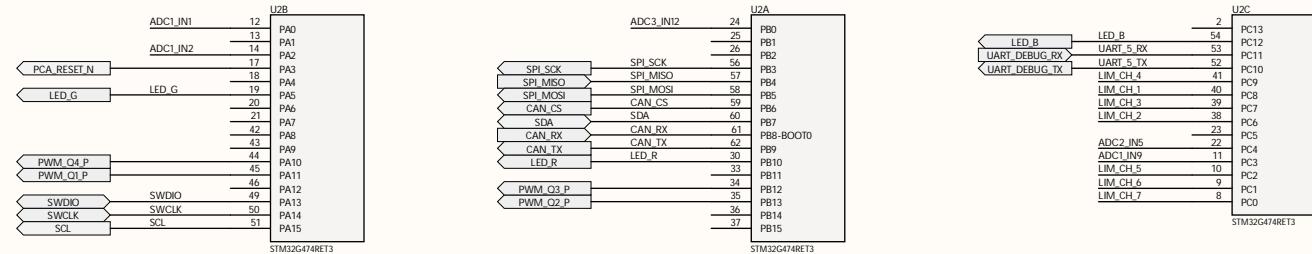
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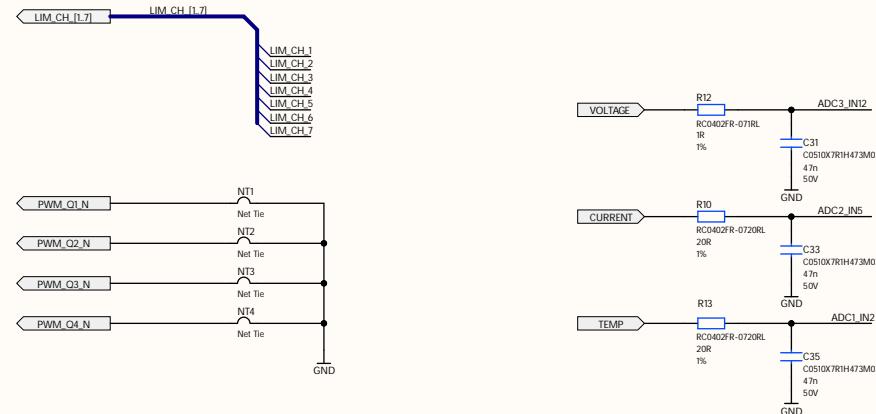
C

C

A



B



C

A

A

B

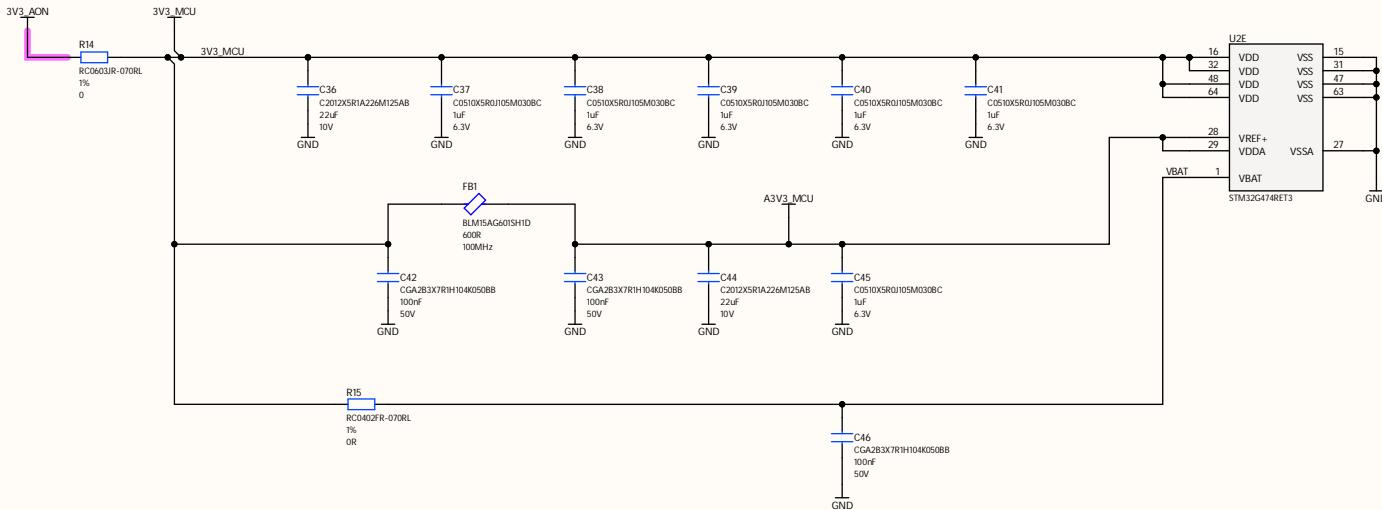
B

C

C

D

D

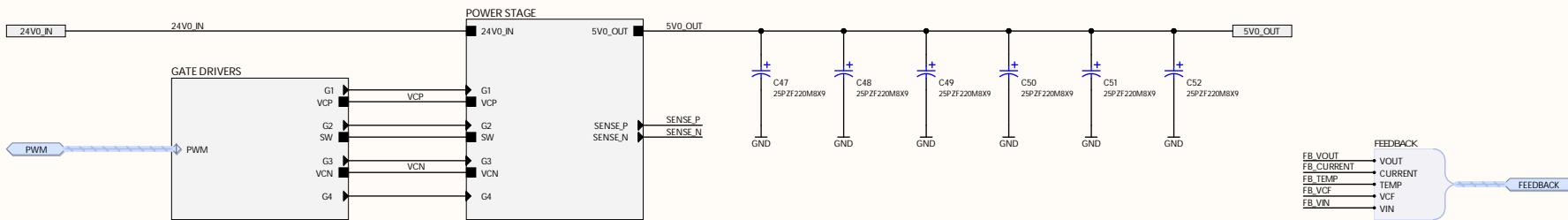


title: Microcontroller Power

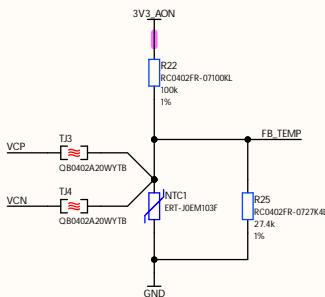
project: mR Power Module rev: A.1 date: 08/03/2023

drawn by: Witold Woszczyński size: A3 sheet 4 of 19

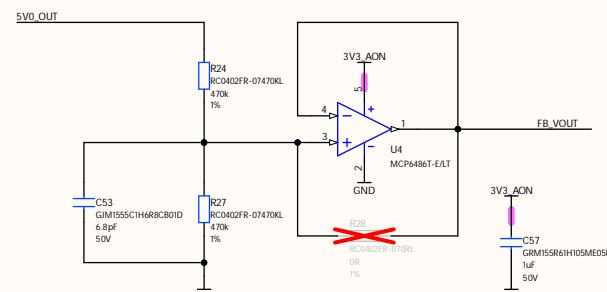




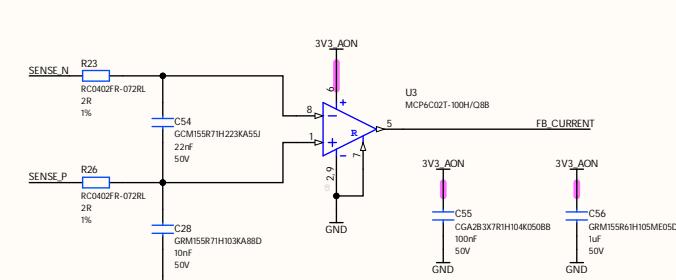
Temperature feedback



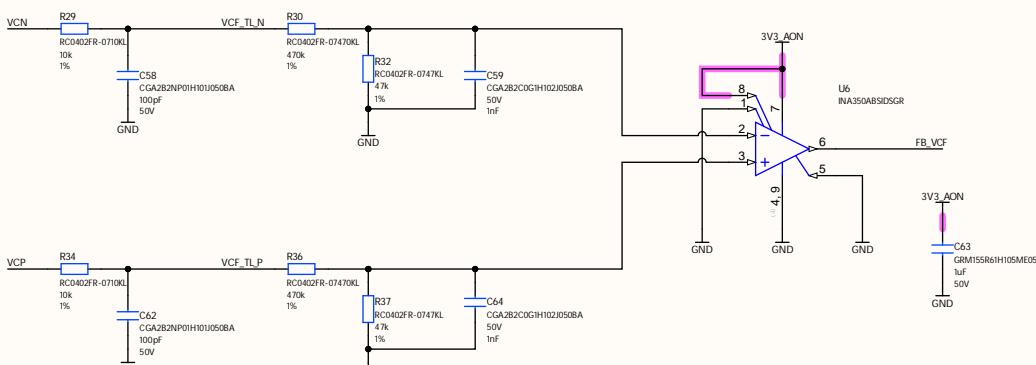
Voltage Feedback



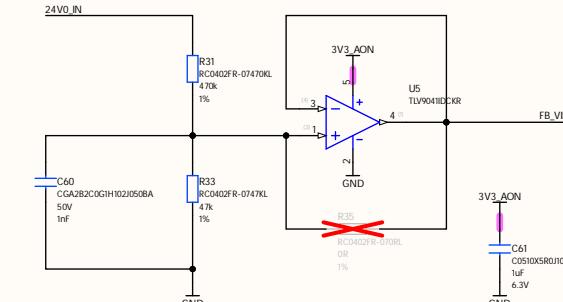
Current Feedback

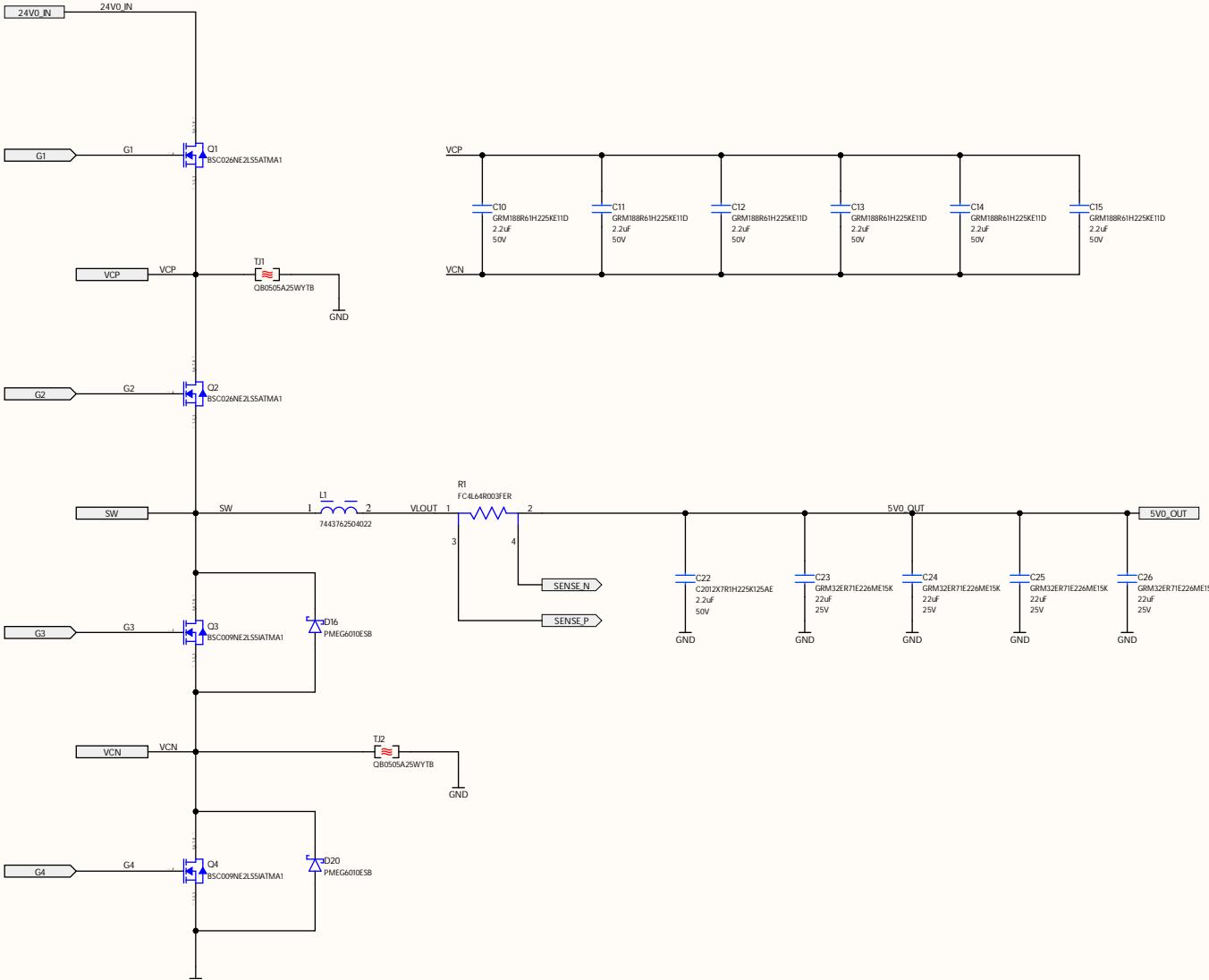
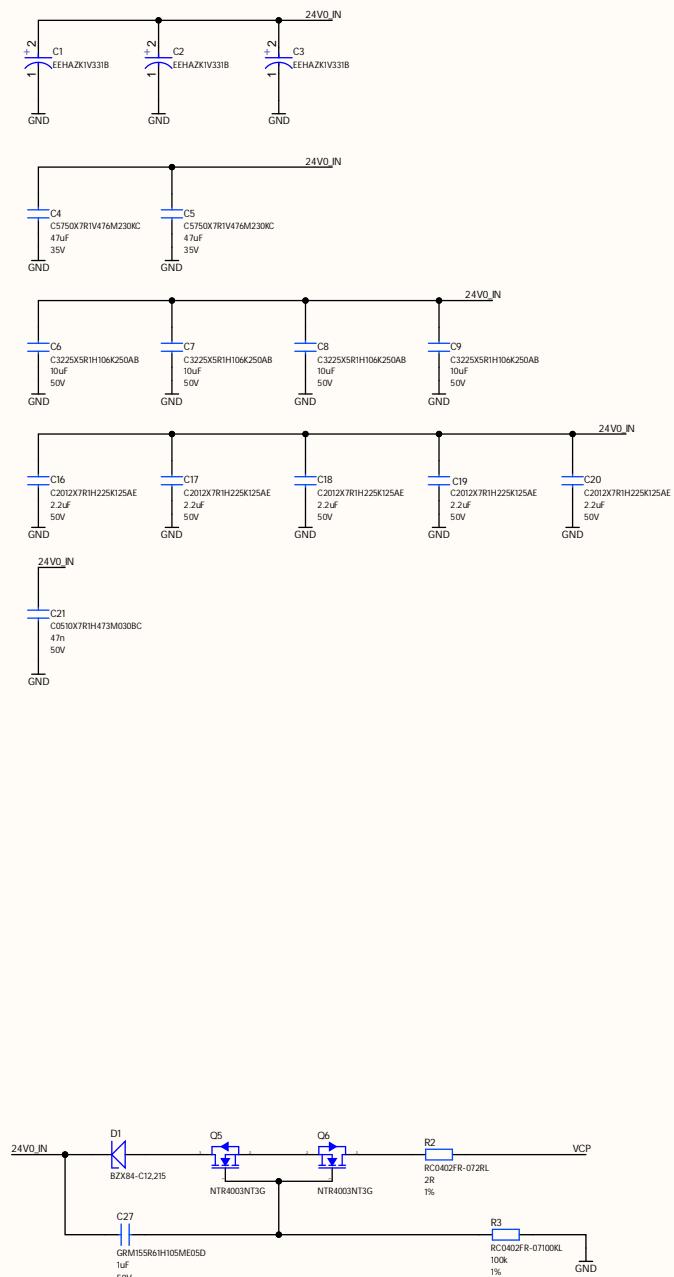


Flying Capacitor Voltage Feedback

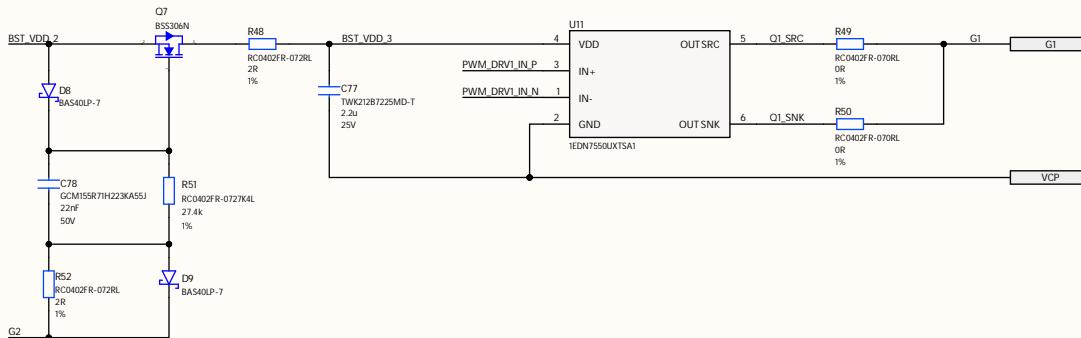


Input Voltage Feedback

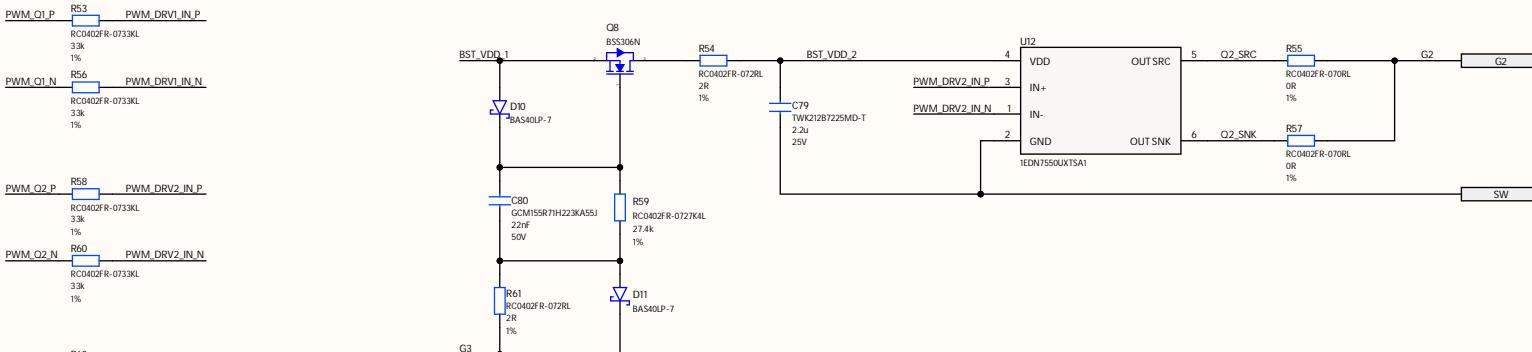




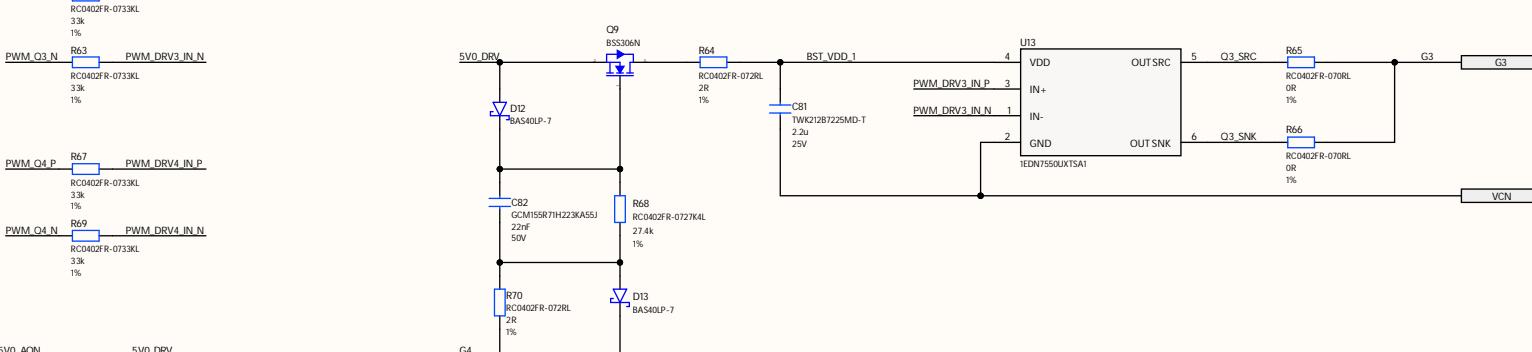
A



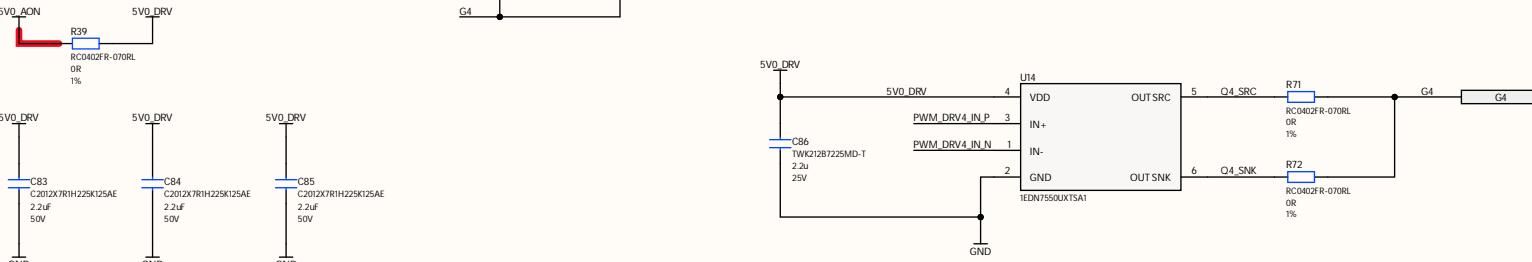
A



B



C



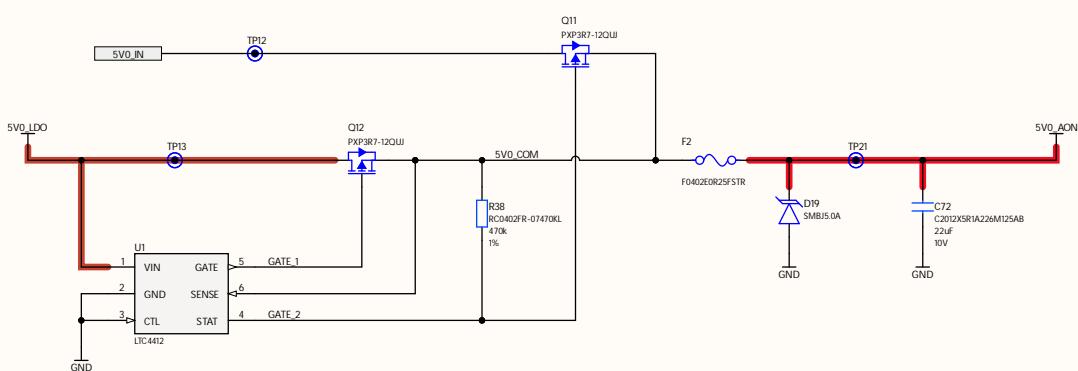
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title:
Gate Drivers

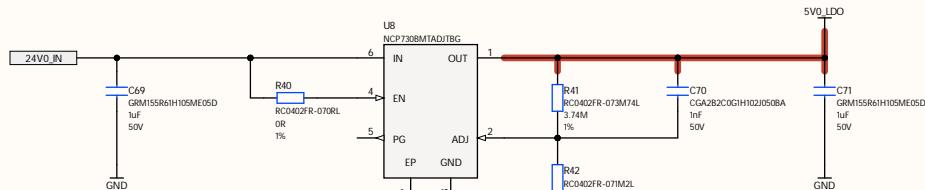
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drawn by: Witold Woszczyna	size: A3	sheet 2 of 19



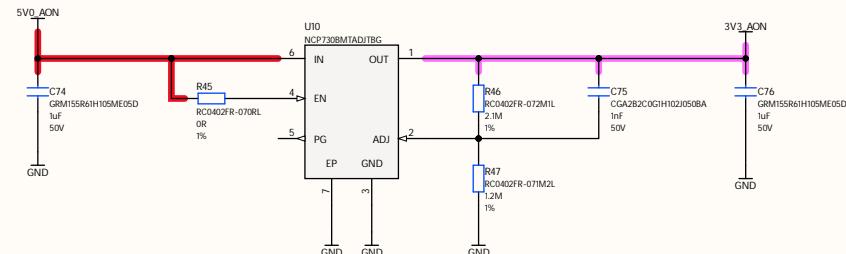
A



A

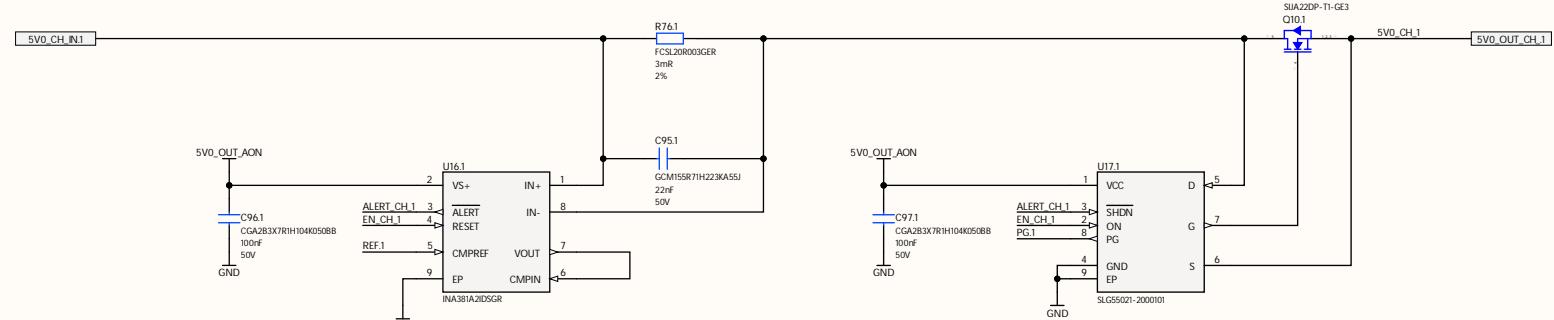


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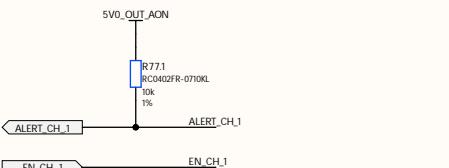


C

A

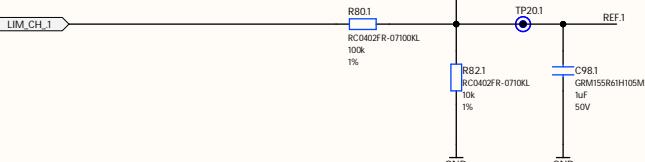


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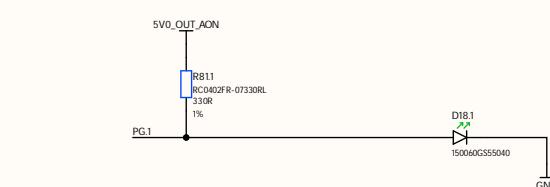
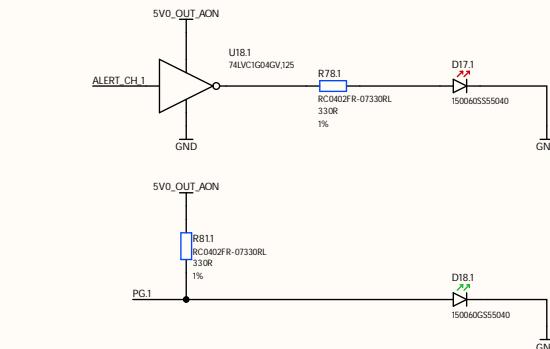


For this application ALERT will be used only in latch mode (INA381 RESET pin high). For reduction of used GPIO pins, RESET on INA381 is connected with ON pin on SLG55021. VLH - Gate driver is on, Comparator in latch mode. VLL - Gate driver is turned off, Comparator - dont care

More info about INA381 mode under "7.4.1.2 Latch Output Mode" section in DS



C



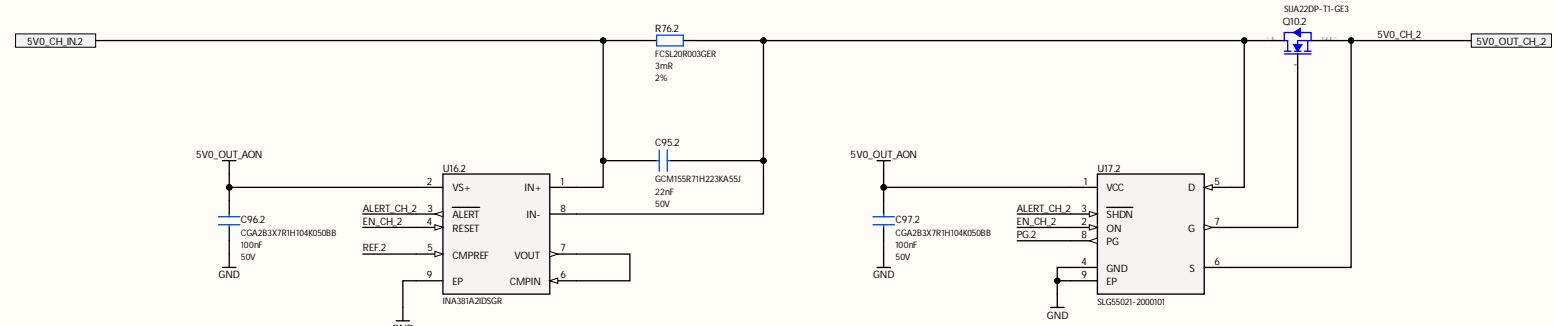
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title: *Output Control*

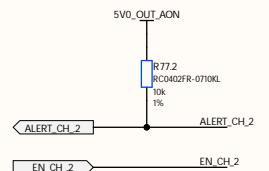
project: mR Power Module	rev: A.1	date: 08/03/2023
drawn by: Witold Woszczyński	size: A4	sheet 9.1 of 19



A

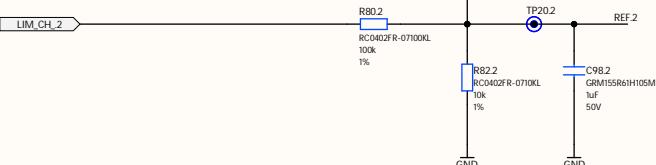


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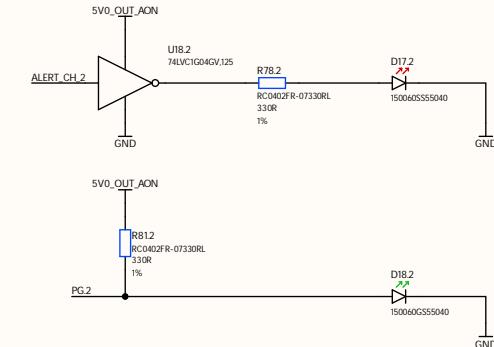


For this application ALERT will be used only in latch mode (INA381 RESET pin high). For reduction of used GPIO pins, RESET on INA381 is connected with ON pin on SLG55021. VLL - Gate driver is on, Comparator in latch mode. VLL - Gate driver is turned off, Comparator - dont care

More info about INA381 mode under "7.4.1.2 Latch Output Mode" section in DS



C



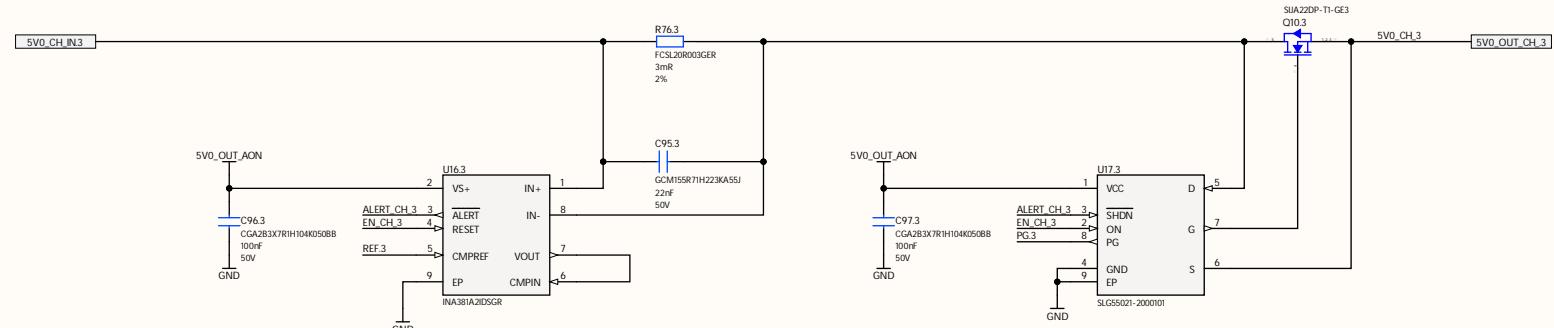
D

title: *Output Control*

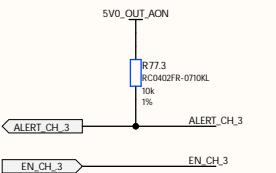
project: mR Power Module	rev: A.1	date: 08/03/2023
drawn by: Witold Woszczyński	size: A4	sheet 9.2 of 19



A

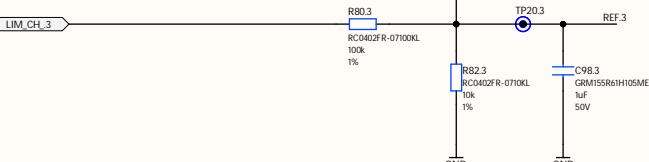


B

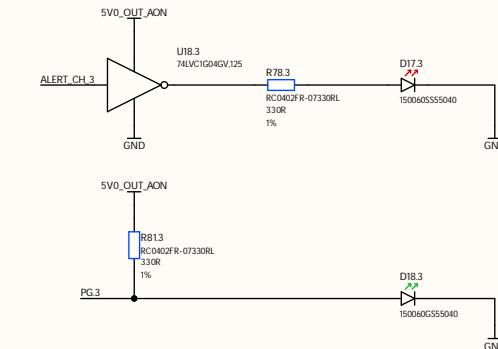


For this application ALERT will be used only in latch mode (INA381 RESET pin high). For reduction of used GPIO pins, RESET on INA381 is connected with ON pin on SLG55021. VLH - Gate driver is on, Comparator in latch mode. VLL - Gate driver is turned off, Comparator - dont care

More info about INA381 mode under "7.4.1.2 Latch Output Mode" section in DS



C



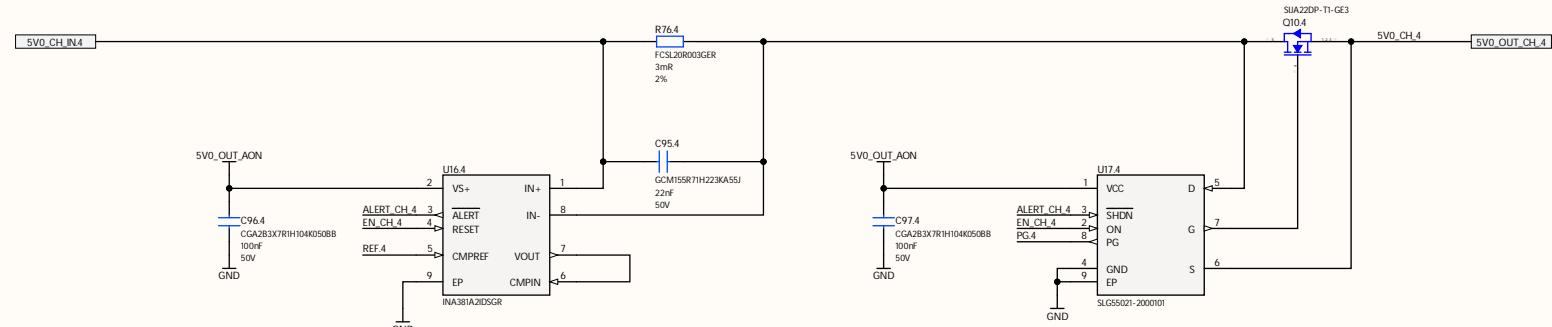
D

title: *Output Control*

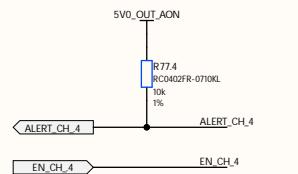
project: mR Power Module	rev: A.1	date: 08/03/2023
drawn by: Witold Woszczyński	size: A4	sheet 9.3 of 19



A

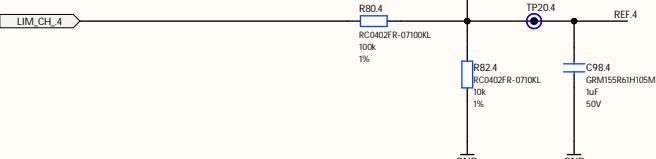


B

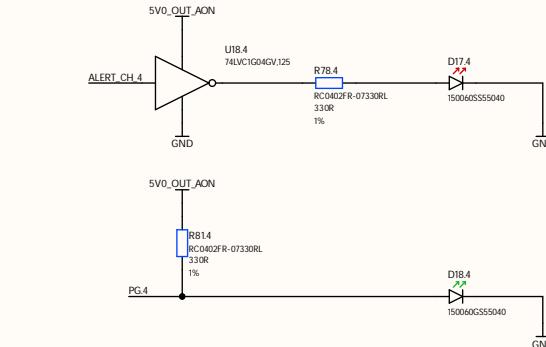


For this application ALERT will be used only in latch mode (INA381 RESET pin high). For reduction of used GPIO pins, RESET on INA381 is connected with ON pin on SLG55021. VLH - Gate driver is on, Comparator in latch mode. VLL - Gate driver is turned off, Comparator - dont care

More info about INA381 mode under "7.4.1.2 Latch Output Mode" section in DS



C



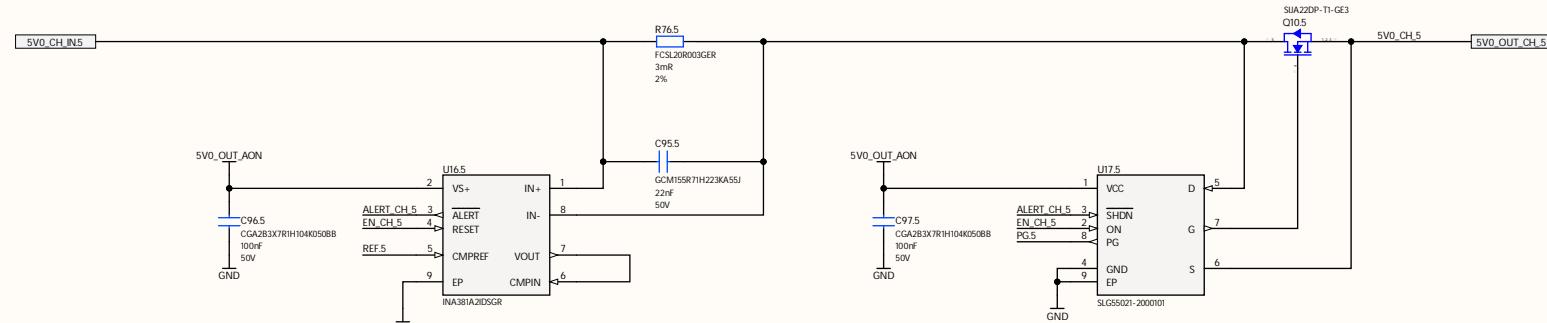
D

title: *Output Control*

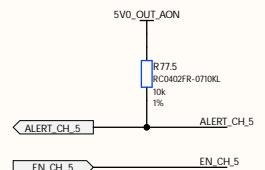
project: mR Power Module	rev: A.1	date: 08/03/2023
drawn by: Witold Woszczyński	size: A4	sheet 9.4 of 19



A

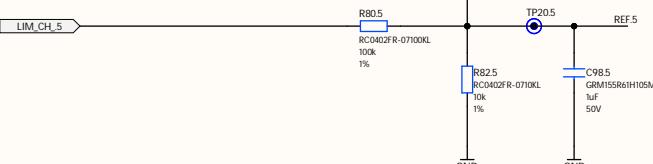


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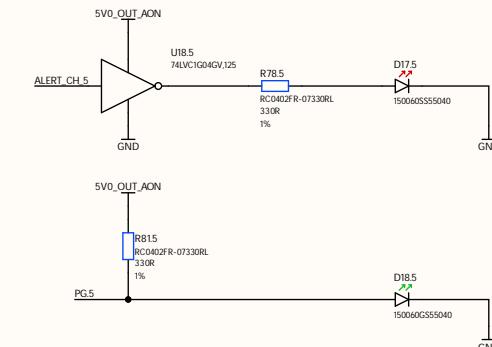


For this application ALERT will be used only in latch mode (INA381 RESET pin high). For reduction of used GPIO pins, RESET on INA381 is connected with ON pin on SLG55021. VLH - Gate driver is on, Comparator in latch mode. VLL - Gate driver is turned off, Comparator - dont care

More info about INA381 mode under "7.4.1.2 Latch Output Mode" section in DS



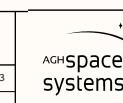
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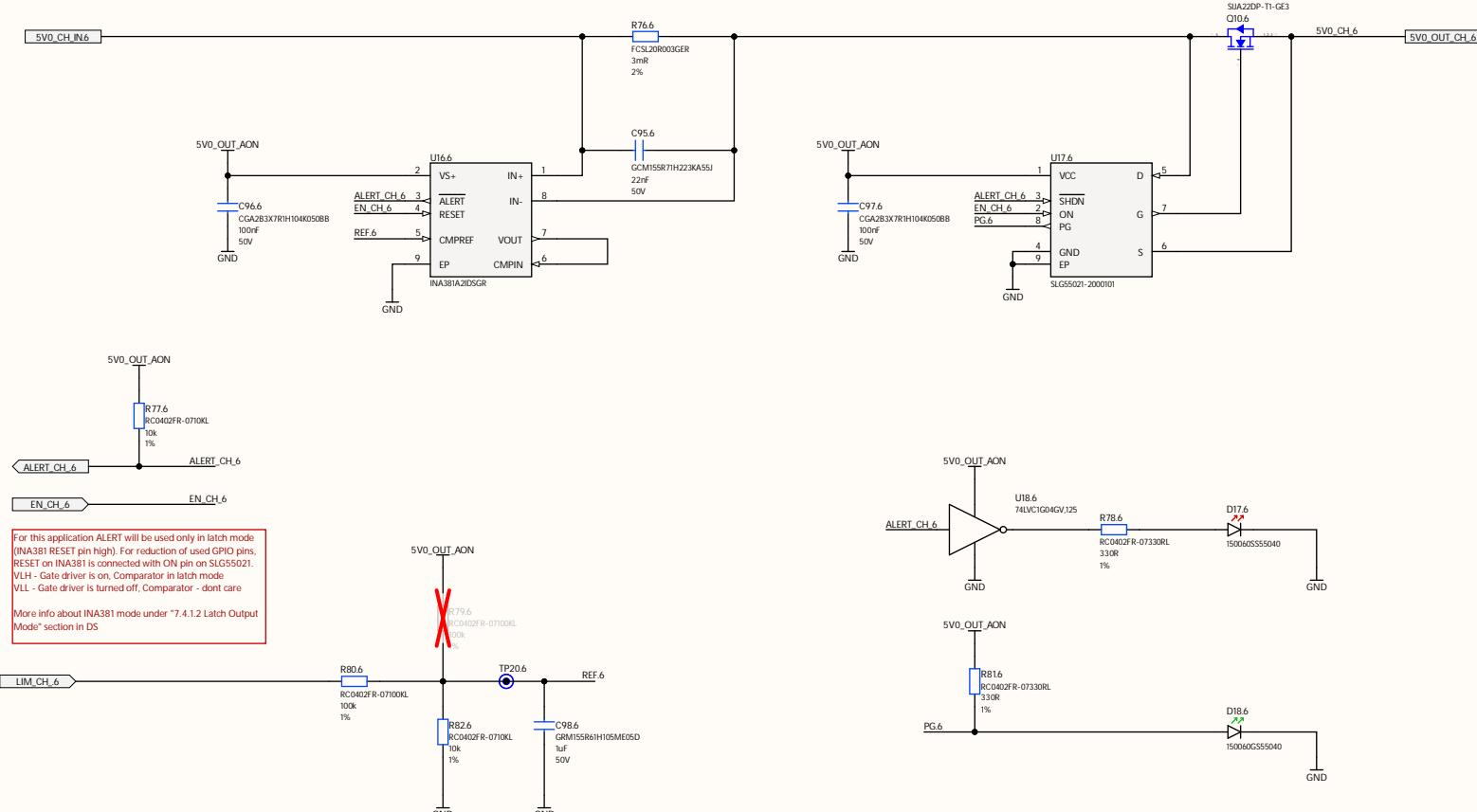
D

title: **Output Control**

project: mR Power Module	rev: A.1	date: 08/03/2023
drawn by: Witold Woszczyński	size: A4	sheet 9.5 of 19



A



B

6

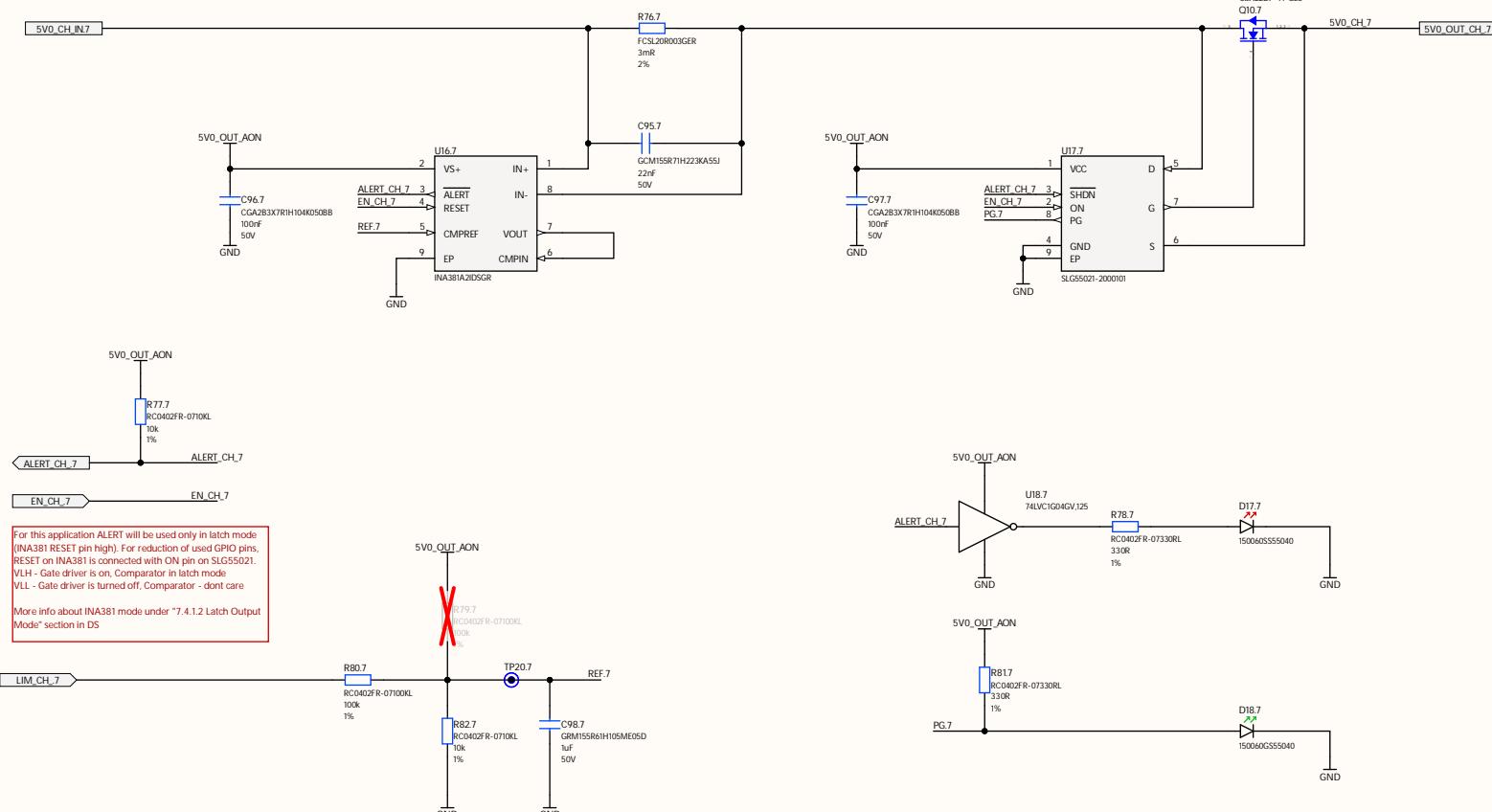
D

A

B

6

D



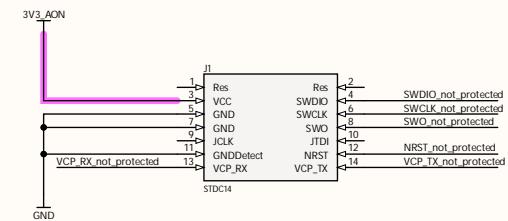
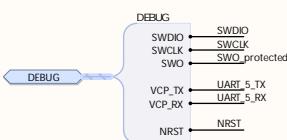
title: *Output Control*

project: mR Power Module rev: A.1 date: 08/03/2023
drawn by: Witold Woszczyna size: 34 sheet 9 of 19

AGH space
systems

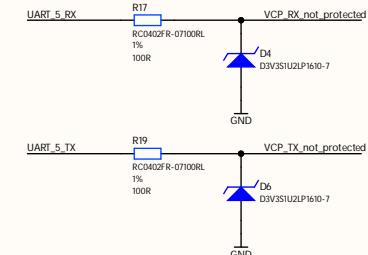
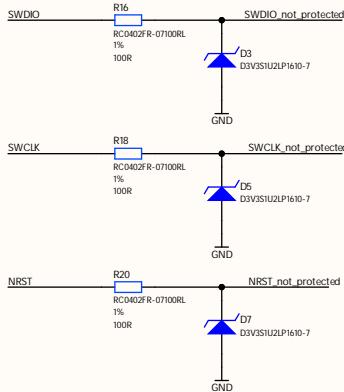
A

A



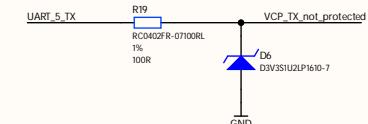
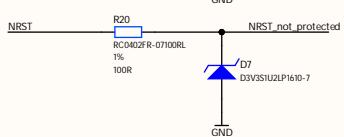
B

B



C

C



D

D

title: **Connector - DEBUG**

project: mR Power Module rev: A.1 date: 08/03/2023

drawn by: Witold Woszczyna size: A4 sheet 10 of 19



A

A

B

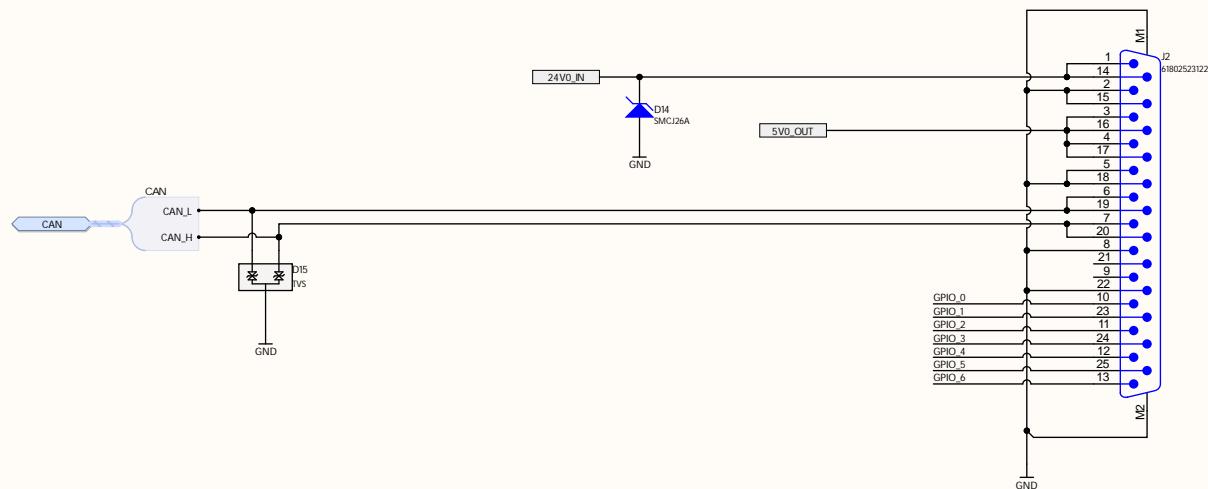
B

C

C

D

D



title: Connector - mini Rack

project: mR Power Module	rev: A.1	date: 08/03/2023
drawn by: Witold Woszczyński	size: A3	sheet 11 of 19

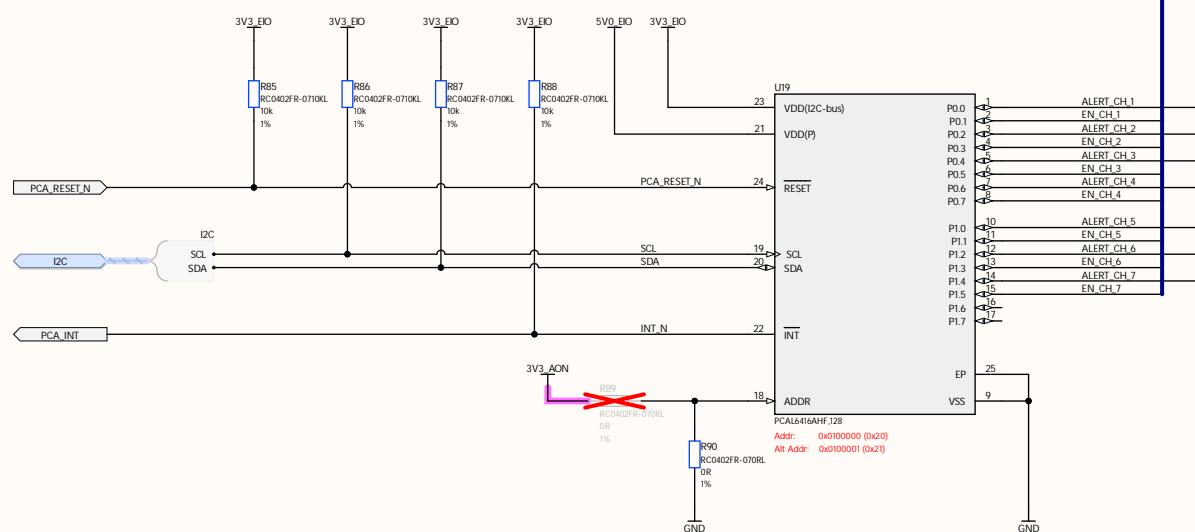


A



ALERT_CH [1..7] EN_CH [1..7]

B



ALERT_CH [1..7] EN_CH [1..7]

C

title: **Interface - I/O**

project: mR Power Module	rev: A.1	date: 08/03/2023
drawn by: Witold Woszczyński	size: A4	sheet 12 of 19



A

A

