# Notes for PSWS ClementineSDR - 06-26-2023

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## My activities this week have included the following:

1. Development tools and documentation:
    - Receive CYUSB3kit for Majid and forward it to him. It should arrive within a couple of days
    - Receive additional Dev. kits for spares and other uses.
    - I currently have three of these kits in hand and one on the way to Majid.
    - I have one CPLD add-on in hand an other on the way for experimentation.
    - I am collecting all of the relevant documentation, app notes, blogs, etc that might relate to this project and will post them in an accessible archive.
2. I have begun work on creating a schematic capture of Oscar Stella's HF-103 design in KiCad.
    - This design supports only HF reception.
    - This schematic is meant to guide discussion of one or more PSWS designs with features to address future requirements.
    - This schematic will be freely available.
    - It will be kept in a format that is usable across operating systems with software that is freely available to all.
    - Creating the initial schematic is fiddly work and takes time. It requires tracking down symbols and footprints for currently available components.
    - It should make future modification and embellishment much easier for all.
3. Until told otherwise, I am starting out with a design that can (as far as is possible) be prototyped from available evaluation and demonstration boards.
    - This seems to be what Oscar Stella has done.
    - My initial idea is to make a board that has two 40 pin sockets for the CYUSB3kit board to plug into.
    - The Rf chain could be implemented and tested on this support board
    - But depending on the A/D chip that we test, there are demo boards that conveniently expose a 40 pin 0.25 mm header along one edge.
    - attachment for the external timing chain components can be provided.
4. I have attempted to keep interested parties informed of activities and interesting found documents. (Let me know if I am not including ***you*** properly).
5. I continue to try to support Scotty's magnetometer boards as best I can for new users.

## My plans for the next week:

1. Continue reading "SuperSpeed Device Design by Example" by John Hyde [Amazon https://www.amazon.com/dp/1500588059?psc=1].

- Work more examples in this book.
- Attempt to build a demo project for the FX3. Maybe more than one.
- Start with CPLD FX3-Slave FIFO CPLD Demo.
- Will CPLD functionality be needed in final design (for timing stuff?)
- Will I2C be needed for control functions?

2. Continue working on "Requirements" spreadsheet derived from:
   "TangerineSDR RF Receiver Module (RXM-5001D)
   Requirements Document"
   Document Number: TSDR-RXM-5001D-REQ,
   version 0.4 Date: Nov. 22, 2019
   provided by Tom McDermott

## What I would like to see happen:

1. Have a technical design meeting , perhaps Wednesday or Thursday evening, to further discuss the progress and direction of this aspect of the ClementineSDR project.
   Participants might include:
   - Majid Mokhtari
   - Franco Venturi
   - Tom McDermott
   - Rob Robinette
   - John Ackermann
   - Students interested in this aspect of the project.
   - ???
2. Read BBRF103 and RX-888 driver code closely to better understand which sort of applications are possible and best suited to SDR designs.
   - from reading, it appears that an asynchronous FX3 Slave FIFO design may be the fastest and most appropriate architecture.
   - Notes from Franco to me:

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 - regarding the maximum throughput achievable with the FX3 the best place to
start IMHO is Cypress AN86947 ([https://www.infineon.com/dgdl/Infineon-
AN86947_Optimizing_USB_3.0_Throughput_with_EZ-USB_FX3-ApplicationNotes-v05_00-
EN.pdf?fileId=8ac78c8c7cdc391c017d073e3a2e6243]
(https://www.infineon.com/dgdl/Infineon-
AN86947_Optimizing_USB_3.0_Throughput_with_EZ-USB_FX3-ApplicationNotes-v05_00-
EN.pdf?fileId=8ac78c8c7cdc391c017d073e3a2e6243)) - as you can see there the
maximum throughput is achieved using an AUTO DMA channel with the GPIF II
interface, 32bit wide, and with a clock rate of 100MHz (and with 4 DMA buffer
of 8kB each - bulk transfer mode)
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 - if I remember correctly, Oscar Steila IK1XPV design is based on the
'cyfxbulklpauto' example (you can find it in
'cyfx3sdk/firmware/dma_examples/cyfxbulklpauto' in the FX3 firmware SDK file
'fx3_firmware_linux.tar.gz'), and on a couple of very useful application notes
from Cypress/Infineon: AN65974 "Designing with the EZ-USB FX3 slave FIFO
interface" ([https://www.infineon.com/dgdl/Infineon-
AN65974_Designing_with_the_EZ-USB_FX3_Slave_FIFO_Interface-ApplicationNotes-
v17_00-EN.pdf?fileId=8ac78c8c7cdc391c017d07396c095deb]
(https://www.infineon.com/dgdl/Infineon-AN65974_Designing_with_the_EZ-
USB_FX3_Slave_FIFO_Interface-ApplicationNotes-v17_00-EN.pdf?
fileId=8ac78c8c7cdc391c017d07396c095deb)), and the 'ping-pong' DMA buffers
approach shown in AN75779 "How to implement an image sensor interface using
EZ-USB FX3 in a USB Video Class (UVC) framework"
([https://www.infineon.com/dgdl/Infineon-
AN75779_How_to_Implement_an_Image_Sensor_Interface_with_EZ-
USB_FX3_in_a_USB_Video_Class_(UVC)_Framework-ApplicationNotes-v13_00-EN.pdf?
fileId=8ac78c8c7cdc391c017d073ad2b85f0d)]
(https://www.infineon.com/dgdl/Infineon-
AN75779_How_to_Implement_an_Image_Sensor_Interface_with_EZ-
USB_FX3_in_a_USB_Video_Class_(UVC)_Framework-ApplicationNotes-v13_00-EN.pdf?
fileId=8ac78c8c7cdc391c017d073ad2b85f0d))
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3. Choose ADC chips for reference schematic(s).
    - Probably choose LTC2208CUP-14 for first efforts because it is small and I have the DEMO854D-D board in hand.
    - The original design for the HF103 used the LTC2217. (I do not have an eval for this one.)
    - Also have the AD9648-125EBZ board in hand, but it is bigger and looks scary.