PSWS FX3 HF103
working prototype

File: PSWS-FX3-HF103-USB.kicad_sch

FX3-USB

File: PSWS-FX3-HF103-ADC-Multi.kicad_sch

LTC-2208 ADC

File: PSWS-FX3-HF103-GPIO.kicad_sch

GPIO

File: PSWS-FX3-HF103-Power.kicad_sch

Power

File: PSWS-FX3-HF103-Notes.kicad_sch

Notes & comments

File: PSWS-FX3-HF103-Filters.kicad_sch

Spare Parts

A development straw-man based on the
Infineon/Cypress FX3 DevKit and LTC2208 Demo modules
[A Minimalist Rework of HF-103 designed by Oskar Stella, ik1xpv]

Dave Witten, KD0EAG

Sheet: /
File: PSWS-FX3-HF103.kicad_sch

Title: PSWS-HF103-proto

Size: A	Date: 2025-06-23	**Rev: 0.1.0**
KiCad E.D.A. 8.0.9		Id: 1/11

CyUSB3Kit-Module

File: CyUSB3KitModule.kicad_sch

CyUSB3 DevKit Module

For possible future direct placement of CYUSB3014-BZXCT on board.

CYUSB-3014

File: PSWS-FX3-HF103-CyUSB-3014.kicad_sch

CyUSB3-3014 Surface Mounted

Deliberately Left Blank

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Sheet: /FX3-USB/
File: PSWS-FX3-HF103-USB.kicad_sch

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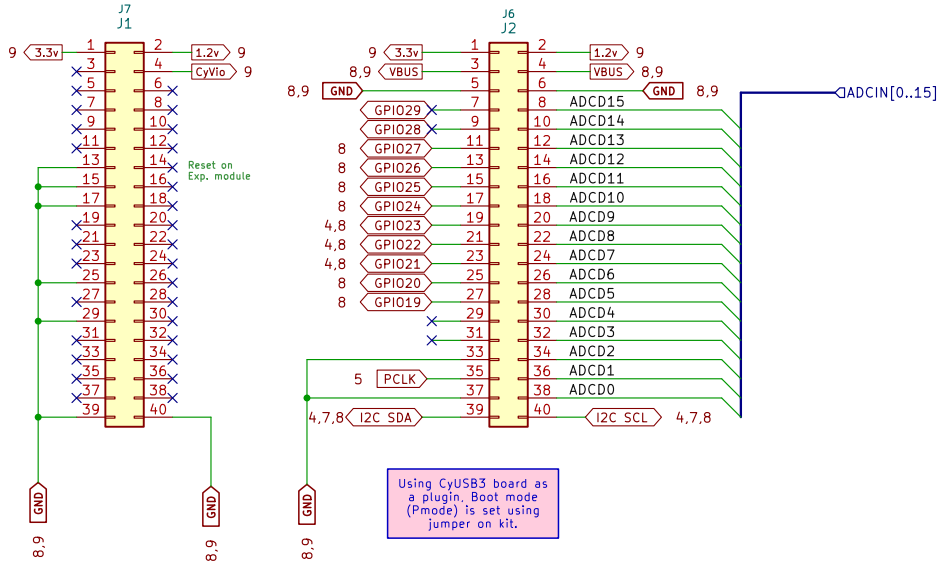
KiCad E.D.A. 8.0.9		Id: 2/11



CyUSB3-KIT003
(FX3 SuperSpeed Explorer)
pin header

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Sheet: /FX3-USB/CyUSB3Kit-Module/
File: CyUSB3KitModule.kicad_sch

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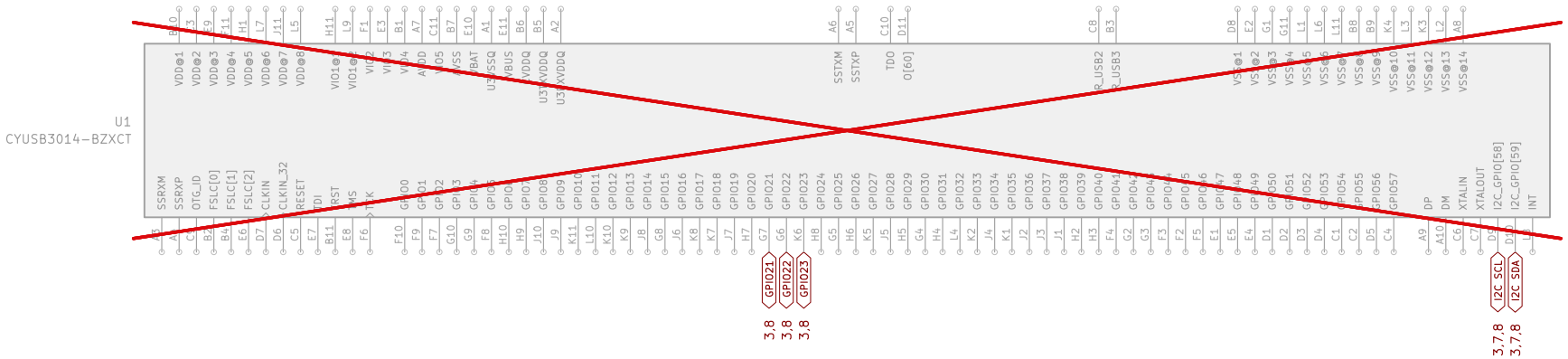

For possible future direct placement of CYUSB3014-BZXCT on board.

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Sheet: /FX3-USB/CYUSB-3014/
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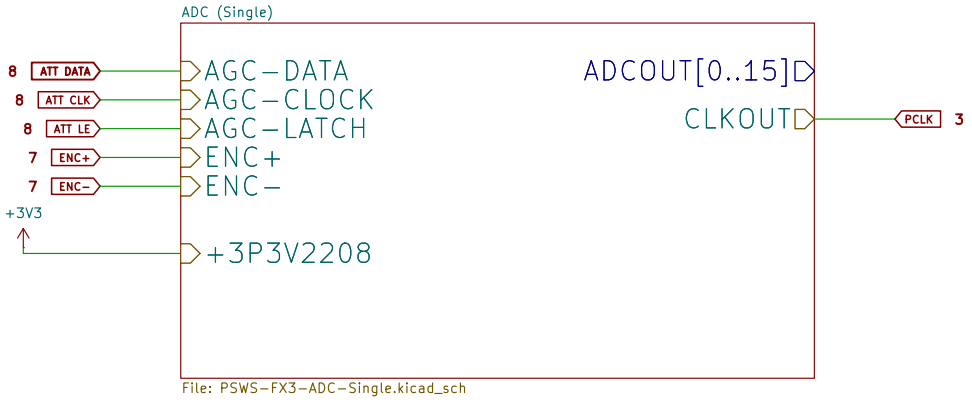

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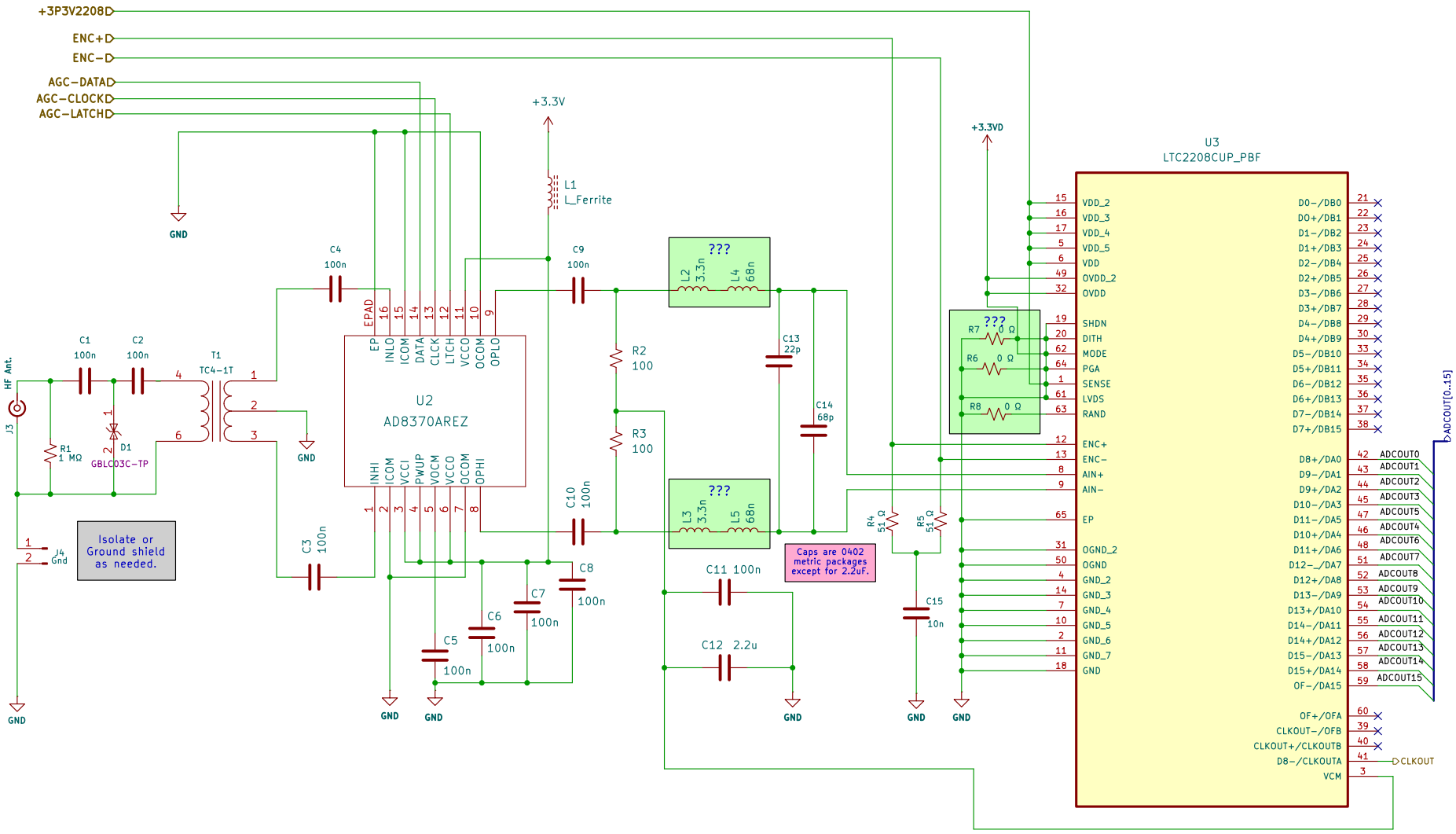
Sheet: /LTC−2208 ADC/
File: PSWS−FX3−HF103−ADC−Multi.kicad_sch

Title: PSWS−HF103−proto

Size: A	Date: 2025−06−23	**Rev: 0.1.0**
KiCad E.D.A. 8.0.9		Id: 5/11



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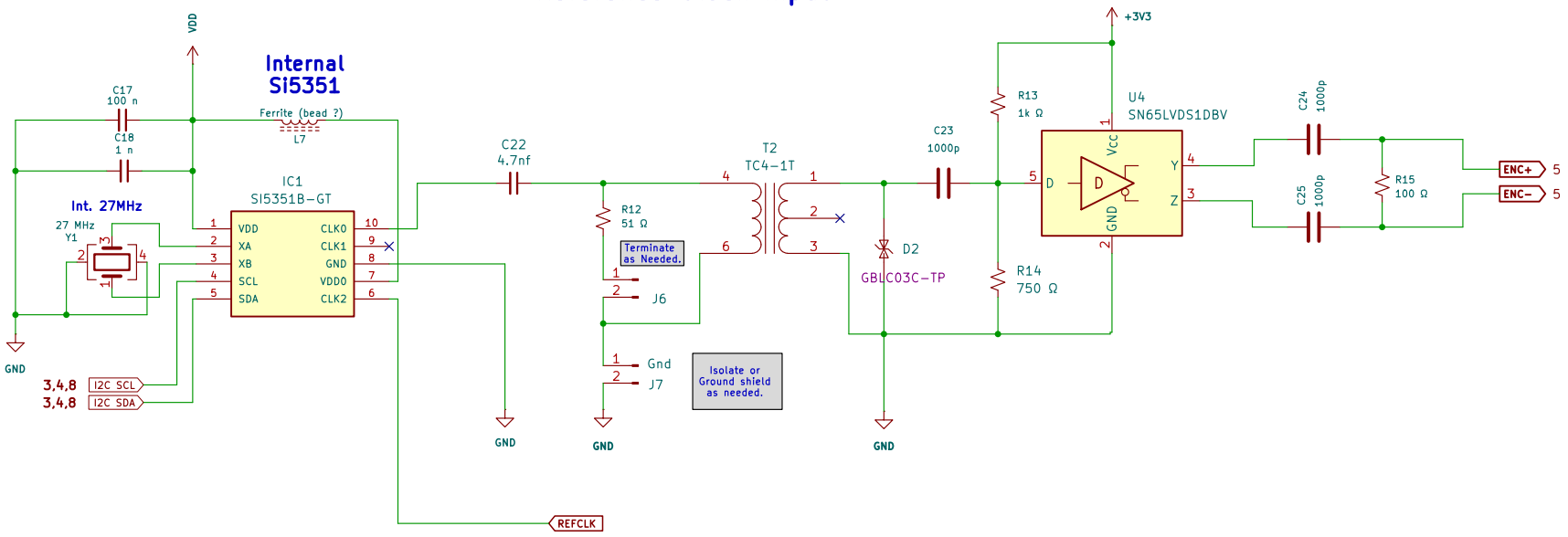
Dave Witten, KD0EAG

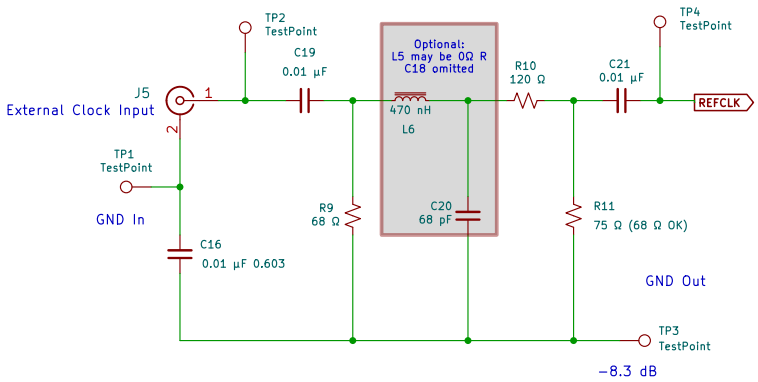
Sheet: /LTC−2208 ADC/ADC (Single)/
File: PSWS−FX3−ADC−Single.kicad_sch

Title: PSWS−HF103−proto

Size: A	Date: 2025−06−23	**Rev: 0.1.0**
KiCad E.D.A. 8.0.9		Id: 6/11

Reference Clock Input





External Clock Conditioning

[Cribbed from Paul Elliot WB6CXC]

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Sheet: /LTC-2208 ADC/ADC (Single)/Timing/
File: PSWS-FX3-HF103-Timing.kicad_sch

Title: PSWS-HF103-proto

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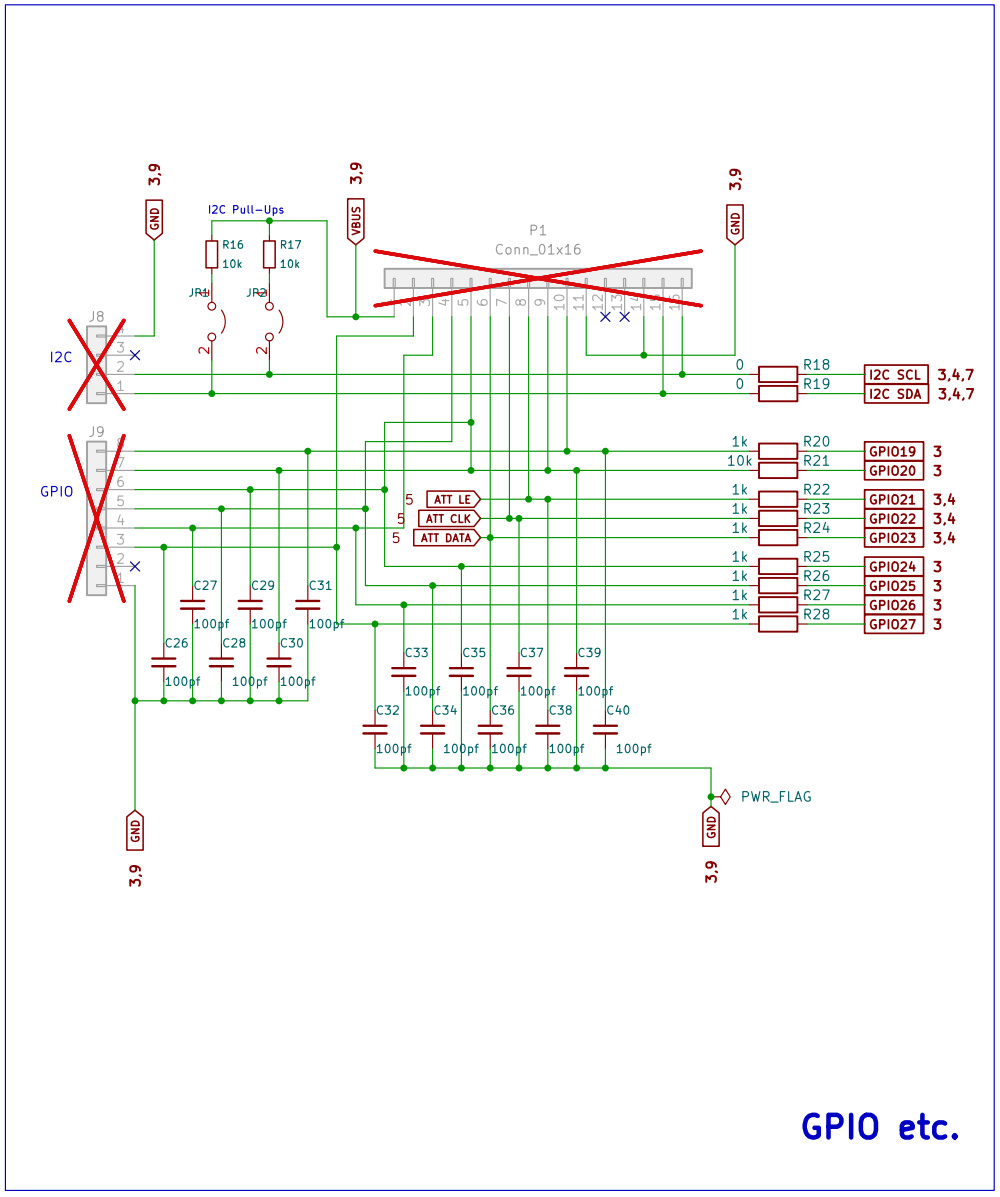
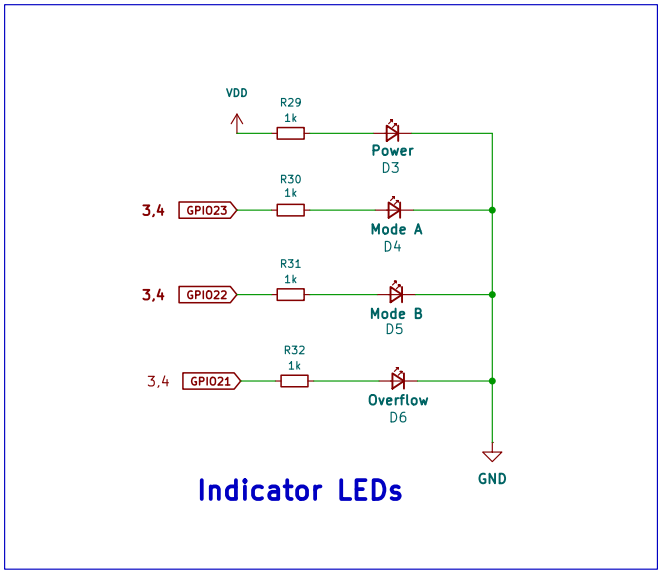
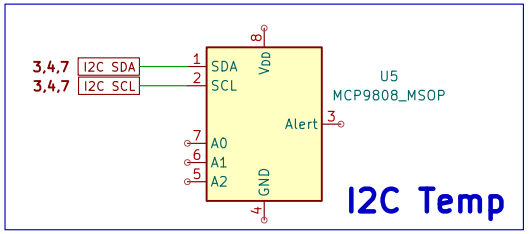
KiCad E.D.A. 8.0.9		Id: 7/11







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Sheet: /GPIO/
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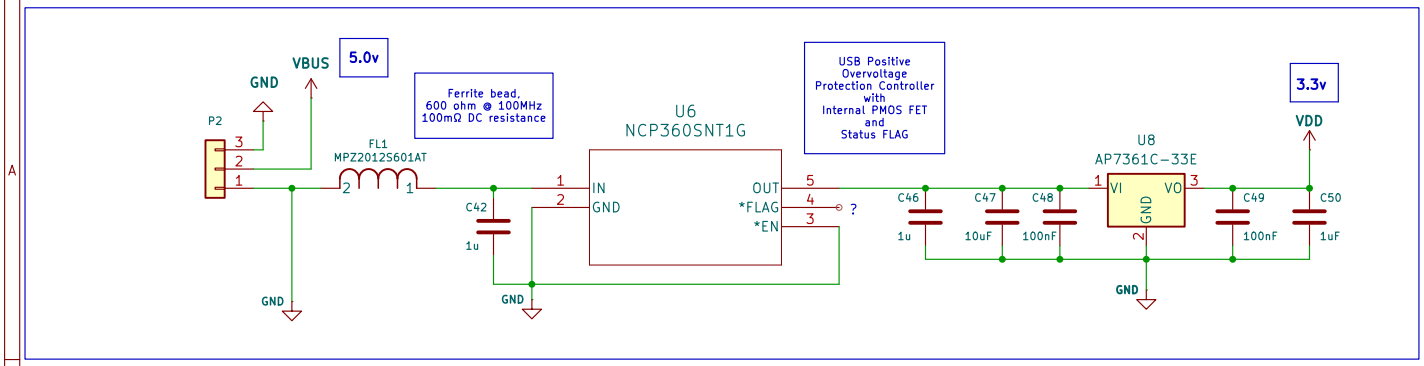
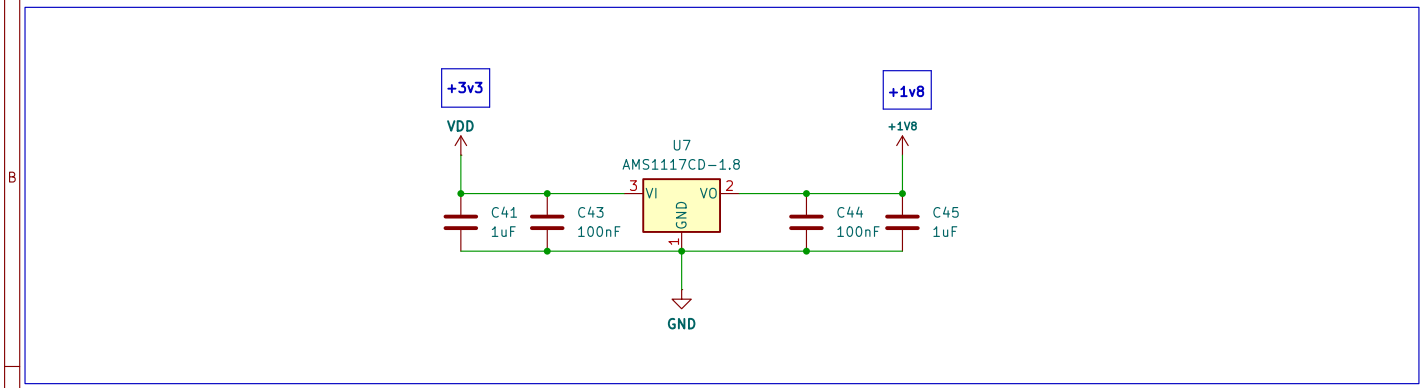
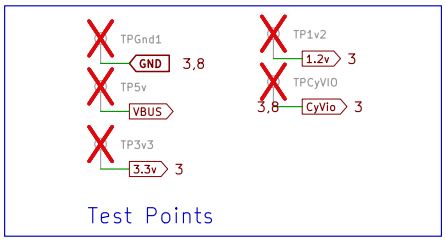


Better regulator options?



More/better Filtration?

Things I want to ask about



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Sheet: /Power/
File: PSWS-FX3-HF103-Power.kicad_sch

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Size: A	Date: 2025-06-23	**Rev: 0.1.0**
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Comments

1. The +3.3V analog power to the LT2208 needs to be heavily LC filtered to keep noise out of the ADC.
The digital (DVDD) can be set to 3.3 or 1.8 volts – it sets the digital logic levels on that part.
I set up the original schematic for 1.8v digital I/O, as that was compatible with the Xilinx FPGA and FX10.
It looks like you are intending digital I/O to be 3.3V. The FX3 may be strappable here.

How 'heavily'?

Track this down.
Downsides?

2. I'm not sure how the external reference clock is wired up to the Si5351 through the needed protective circuitry. The transformer in the timing circuit was intended for the external reference input rather than coupling from the Si5351 to the differential clock driver. There should be a simpler way to couple Si5351 to the driver with just RLC components.

Added components from Paul Elliot's fix for RX-888.
OK?

3. There appears to be an alternate circuit to drive the analog input on the ADC chip. Not sure what was intended.

Oversight.
This has been deleted.

4. The I2C lines on the AD8370 AGC chip need to use the correct logic levels, the datasheet does not say what the voltages are that I can find. It just says "TTL levels" and Not-to-exceed Vcc+0.5.
The diagram on page 14 figure 42 would imply that the logic levels need to be the same as VCC to the chip.
The AGC chip can run on 3.3V or 5V, the RF performance is better at +5V. So the FX3 will need to either supply a full 5V logic level swing, or use a tiny pull-up and an open-collector driver on the pin.

I was expecting to use 3.3v logic wherever possible.
How big is the hit?

On the FX10 the I2C voltage I think is strappable 1.8V or 3.3V, don't know about the FX3. If driving the pins directly from the FX3, need to make sure the FX3-GPIO pins to the AGC amp can handle the voltage range.
Alternatively, can provide +3.3V power to the AGC amp, and set the GPIO pins for 3.3V operation on the FX3.

-- Tom, N5EG

[Notes to self]

Comments – Clint 2025-06-23

1) Remove transformer from RF path to improve low-end performance ???

2) LPF filter – 30 MHz / 60 MHz / Completely external ???

Sampling VERSION TABLE

Assembly Type	U1	T1	C5	C7, C28	R30	R31,R32	L1	INPUT FREQUENCY	Bits	Msps
DC854D-A	LTC2208CUP	MABAES0060	4.7pF	8.2pF	86.6	86.6	56nH	1MHz < Ain < 70MHz	16	130
DC854D-B	LTC2208CUP	WBC1-1L	1.8pF	3.9pF	182	43.2	18nH	70MHz < Ain < 140MHz	16	130
DC854D-C	LTC2208CUP-14	MABAES0060	4.7pF	8.2pF	86.6	86.6	56nH	1MHz < Ain < 70MHz	14	130
DC854D-D	LTC2208CUP-14	WBC1-1L	1.8pF	3.9pF	182	43.2	18nH	70MHz < Ain < 140MHz	14	130
DC854D-E	LTC2217CUP	MABAES0060	4.7pF	8.2pF	86.6	86.6	56nH	1MHz < Ain < 70MHz	16	105
DC854D-F	LTC2217CUP	WBC1-1L	1.8pF	3.9pF	182	43.2	18nH	70MHz < Ain < 140MHz	16	105
DC854D-G	LTC2217CUP	MABAES0060	4.7pF	8.2pF	86.6	86.6	56nH	1MHz < Ain < 70MHz	16	80
DC854D-H	LTC2216CUP	WBC1-1L	1.8pF	3.9pF	182	43.2	18nH	70MHz < Ain < 140MHz	16	80
DC854D-I	LTC2215CUP	MABAES0060	4.7pF	8.2pF	86.6	86.6	56nH	1MHz < Ain < 70MHz	16	65
DC854D-J	LTC2215CUP	WBC1-1L	1.8pF	3.9pF	182	43.2	18nH	70MHz < Ain < 140MHz	16	65
DC854D-P										

MABAES0060 == (ETC1-1-13)

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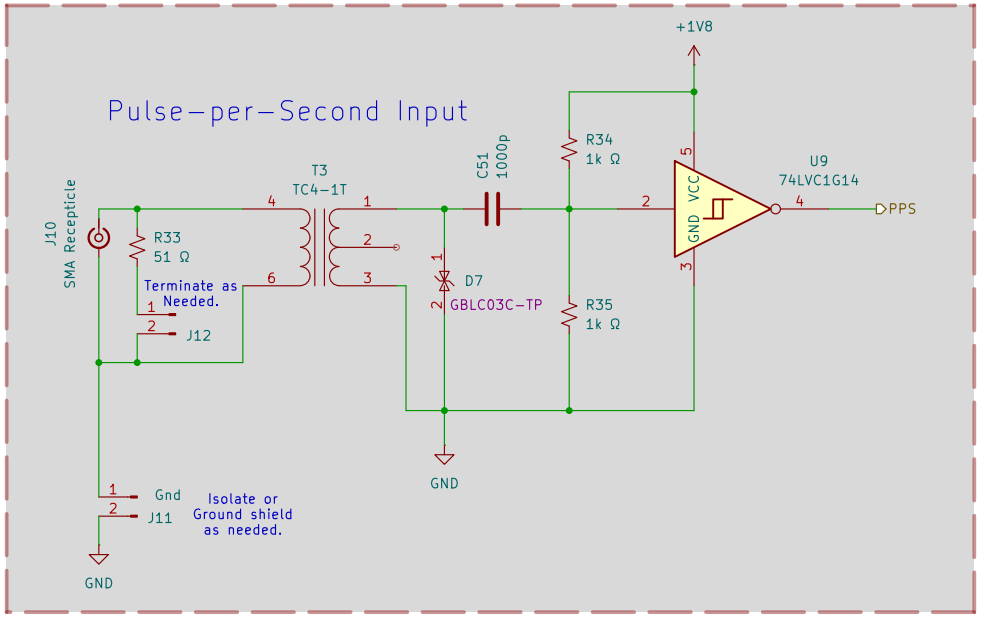

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