07-11-2023
EE-301(Analog Circuits)

EE-301: Course Project

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(2021EEB1030)

Objective: Design of cascode amplifier and cascode current mirror in schematic and layout using LTspice or Cadence and Magic/Cadence tools in 180 nm (supply 1.8 V) technology and only schematic of cascode amplifier, beta multiplier and cascode current mirror in 22 nm (supply 0.8 V) technology node to see the effect of lowering the technology node.

The target specifications for designing the cascode amplifier are as follows:

- VDD = 1.8 V
- AV = 20 V/V
- Power dissipation (PD) < 5 mW
- Load Capacitance (CL) = 1 pF
- Unity Gain Bandwidth (UGB) > 500 KHz.

LTspice Schematic(180nm):

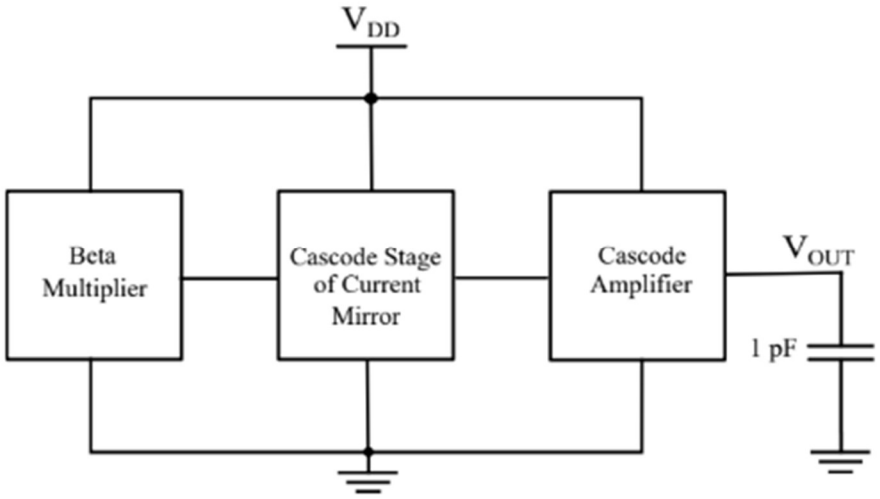


Fig: Block diagram of cascode amplifier with other blocks

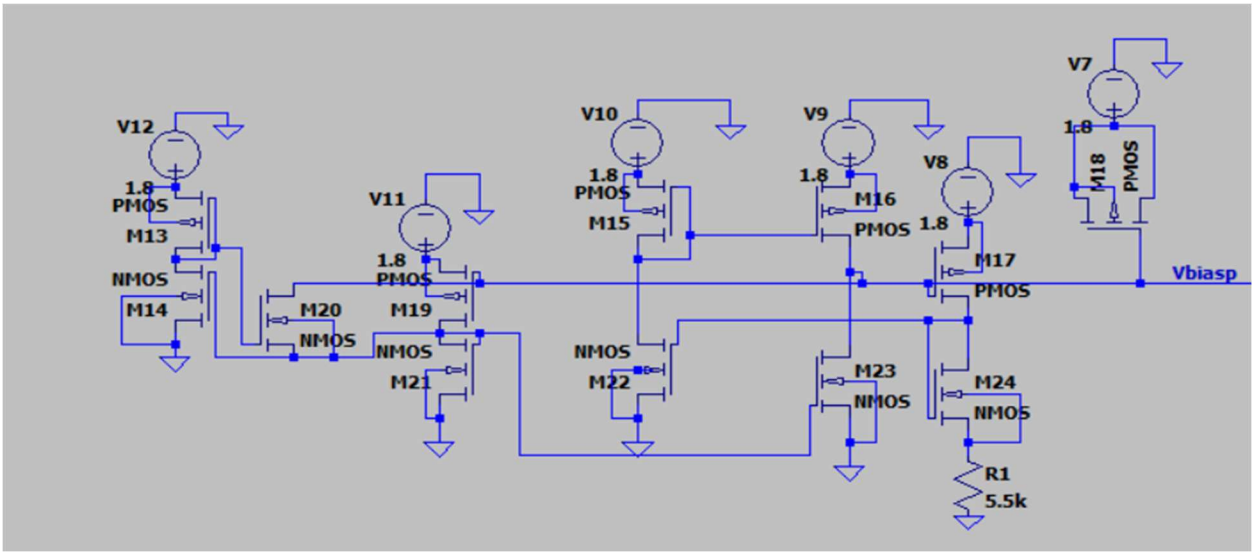


Fig: Circuit for beta multiplier circuit

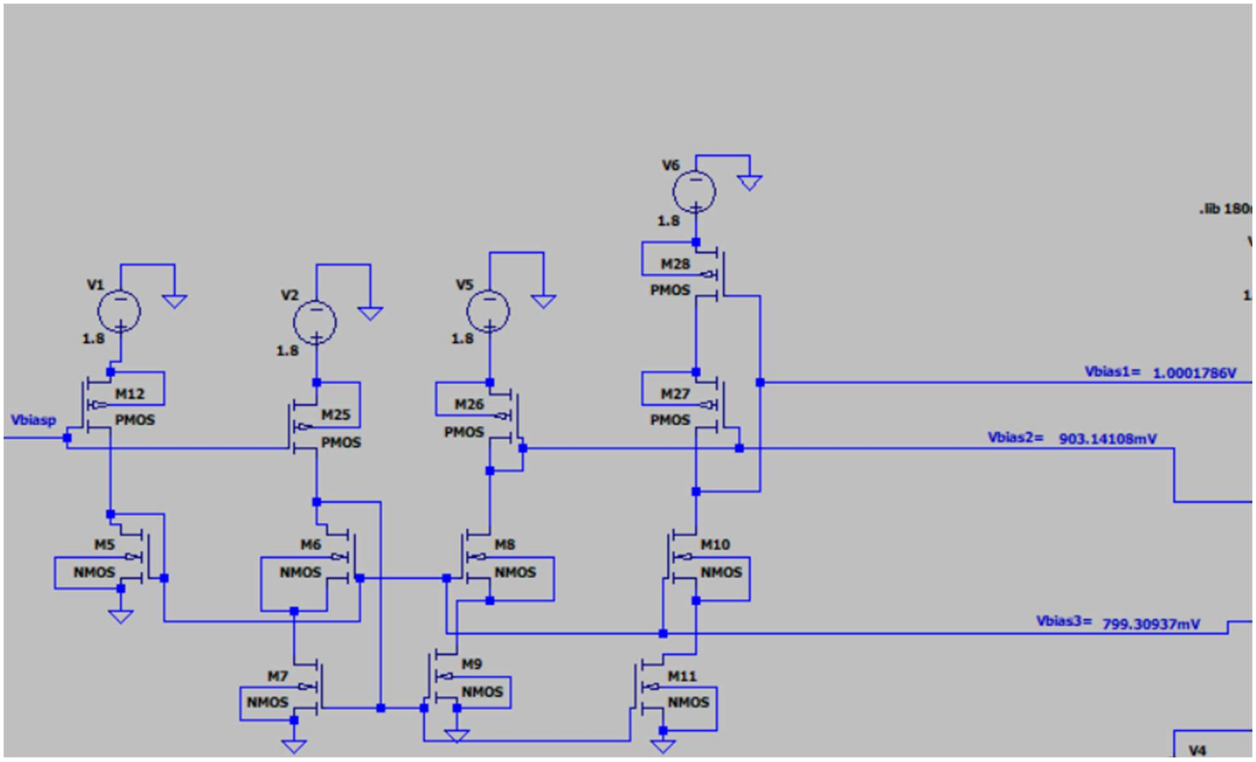


Fig: Circuit for cascode current mirror

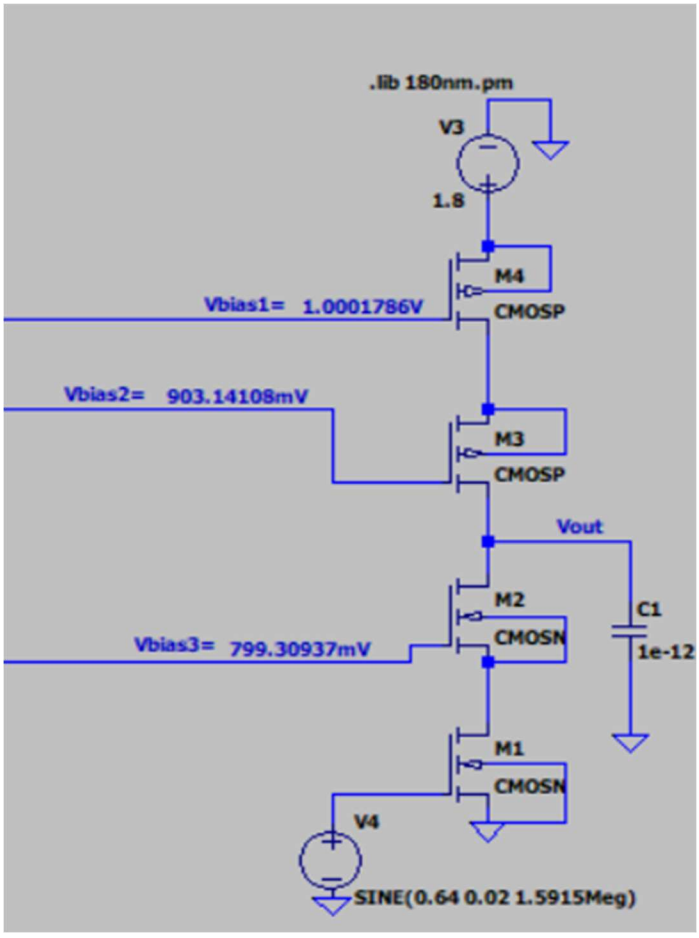


Fig: Circuit for cascode amplifier

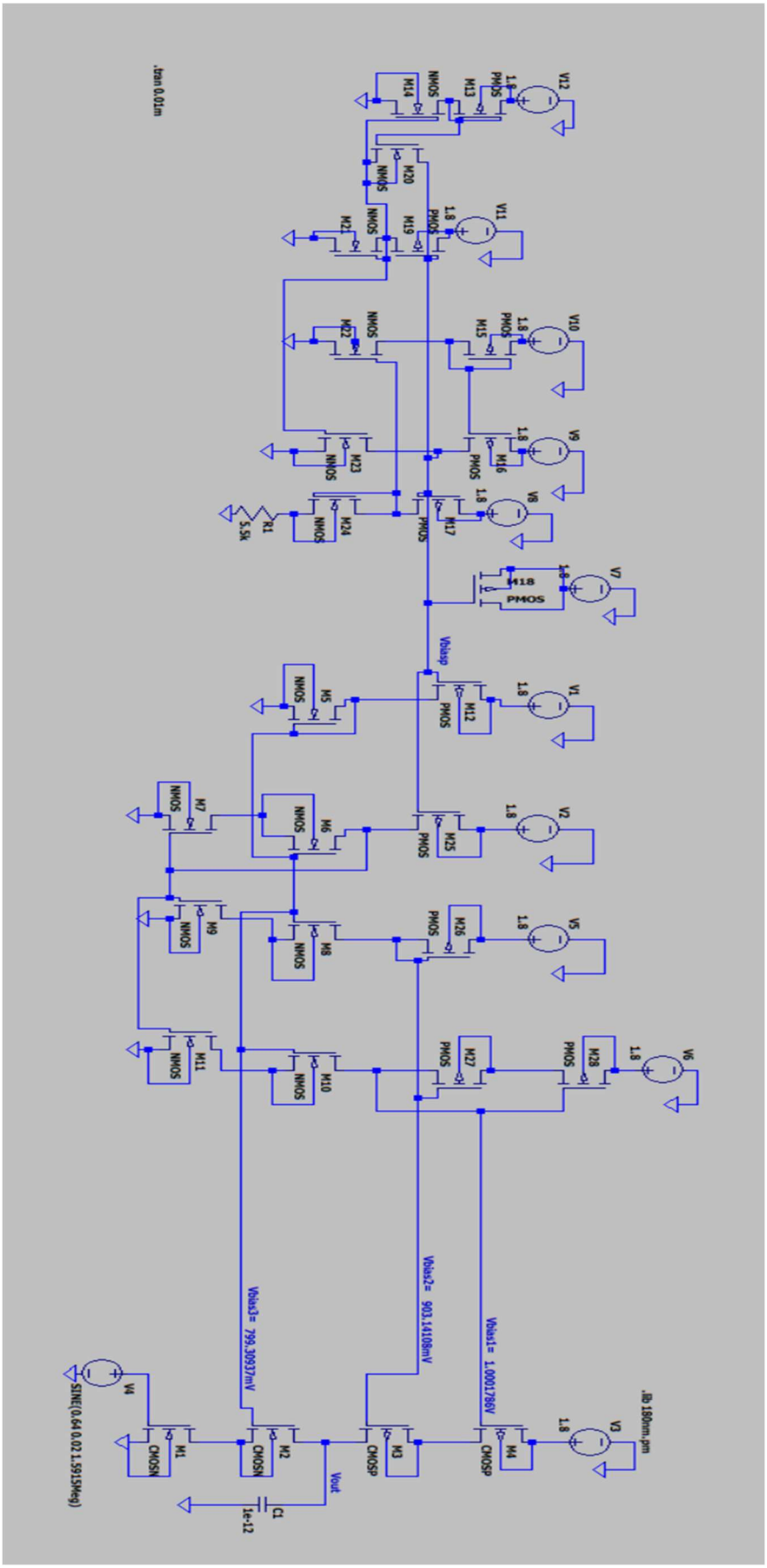


Fig. Complete circuit

Calculations(180nm):

180nm Calculation:

NMOS

$\mu_n C_{ox} = 350.8\ \mu A/V^2$

PMOS $\mu_n C_{ox} = 71.2\ \mu A/V^2$

$V_t = 0.5$

$V_{DD} = 1.8V$

$A_v = 20\ V/V = g_m R_{out}$

Load capacitance = 1 pF

Unity Gain Bandwidth > 500 KH$_2$

For easier calculation

assume $f_{cutoff} = 1.5915\ MH_2$

by using $f = \frac{1}{2\pi R_{out} C}$

$\Rightarrow R_{out} = 100\ KH_2$

$\Rightarrow g_m = 200\ \mu S$

we know that

$$g_m = \mu_n C_{ox} \cdot \frac{W}{L} \cdot (V_{GS} - V_{th}) \quad \text{---(I)}$$

Assume $V_{ds} = 200\ mV$

$V_t = 0.5\ V$

For M_1

For saturation $V_{ds} > V_{GS} - V_t$ ---(II)

$\Downarrow$

$V_G < 0.7\ V$

using ① and ⑪ and provided data

$\boxed{\frac{W}{L} \geq 2.85}$ for saturation

also $V_G < 0.7$

I checked many values of V_G

But got proper output on $V_G = 0.64V$

$$I_d = \mu_n C_{ox} \times \frac{W}{2L} (V_{GS} - V_{TH})^2$$

$$\Rightarrow \boxed{I_d = 24\mu A}$$

For M_2

$$V_{ds} > V_{GS} - V_{th}$$

$$0.2 > V_G - 0.2 - 0.5$$

$$V_G < 0.9$$

using Id equation and Id value obtained above

$\boxed{\frac{W}{L} \geq 3.4}$ for saturation

For BOTH MOSFETs I choosed appropriate value to obtain required gain consider all inequalities..

for M_4

for saturation

$$V_{SD} > V_{SG} - |V_{th}|$$

$V_S = 1.8 \quad V_d = 1.6$

$$\Rightarrow \boxed{V_G > 1.1V}$$

$$I_d = \mu_n C_{ox} \frac{W}{2L} (V_{SG} - |V_{th}|)$$

and for $I_d = 24\,\mu A$ and for saturation

$$\boxed{\frac{W}{L} \leq 17}$$

for M_3

for saturation

$$V_{sd} > V_{SG} - |V_{th}|$$

$$\boxed{V_g > 0.9}$$

From I_d equation and value

for saturation

$$\boxed{\frac{W}{L} \leq 17}$$

Choosed appropriate W/L ratio to obtain required gain considering all in equalities

We need to adjust V_{bias1}, V_{bias2} and V_{bias3} for MOSFETs to work in saturation region and required gain, I adjusted W/L ratios in Cascode current mirror circuit's MOSFETs to get proper biased voltage.

V_{bias1}=1.00V

V_{bias2}=903.14mV

V_{bias3}=799.31mV

Vin=0.640V (DC Bias), Vac=20 mV, f=1.5915 MHz

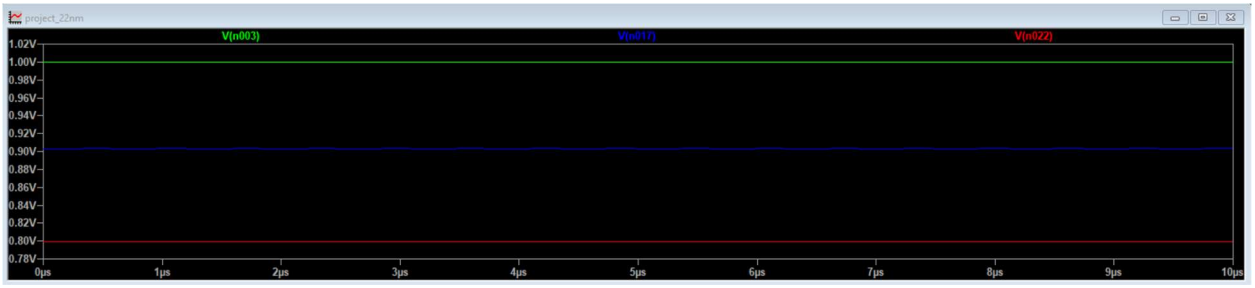


Fig: Above mentioned Biased Voltages

Output(180nm):

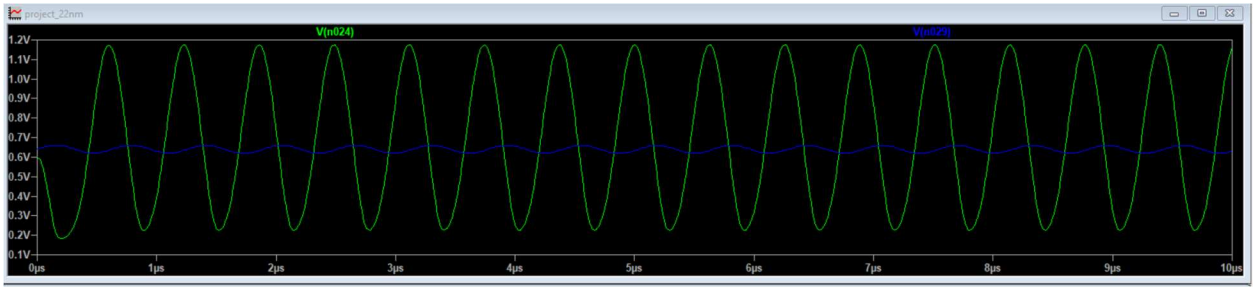


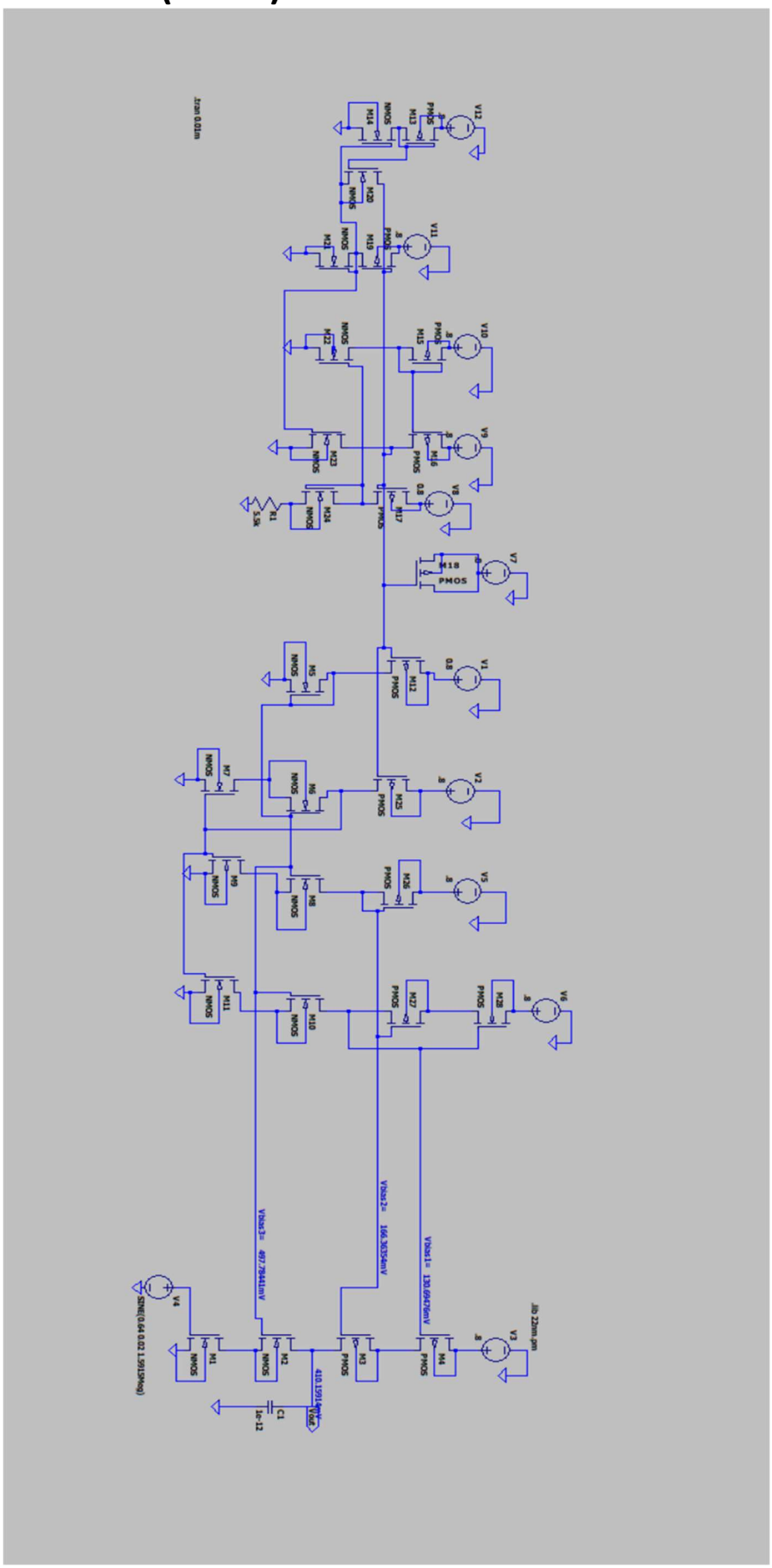
Fig: V_{in} (Blue) and V_{out} (Green)

Output Voltage Swing: (1.17to 0.19) V = 0.98V

Amplitude of Swing= 0.49 V

Gain=27.7dB

LTspice Schematic(22nm):



Calculations:

For 22 nM

NMOS

$\mu_n C_{ox} = 100\ \mu A/V^2$

PMOS

$\mu_p C_{ox} = 50\ \mu A/V^2$

$V_{th} = 0.5\ V$

Unity gain Bandwidth > 500 KHz

Assumed $f_{cutoff} = 1.5915$ MHz

$R_{out} = 100\ K\Omega$ $\left(f = \frac{1}{2\pi R_{out} C}\right)$

$C = 1\ pF$

$\Rightarrow g_m = 200\ \mu S$ for gain = 20 V/V

Also $g_m = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{th})^2$ ——— (1)

Assume $V_{DS} = 0.2V$

$V_{th} = 0.5V$

For M_1 saturation region

$V_{DS} > V_{GS} - V_t$ ——— (11)

$\boxed{V_G < 0.7\ V}$

For M_2

$V_{ds} > V_{GS} - V_{th} \Rightarrow$ Saturation

$0.2 > V_G - 0.2 - 0.5$

$\boxed{V_G < 0.9}$

For M_4

$V_S = 0.8$

$V_d = 0.6$

for saturation

$V_{Sd} > V_{SG} - |V_t|$

$0.2 > 0.8 - V_G - 0.5$

$\boxed{V_G > 0.1}$

For M_3

$V_S = 0.6$, $V_d = 0.4$

For saturation $\Rightarrow \boxed{V_G > -0.1}$

For beta multiplier and cascode current mirror circuits I kept W/L as same as given in problem. Most Of the calculation are same as 180nm for W/L ratios so I

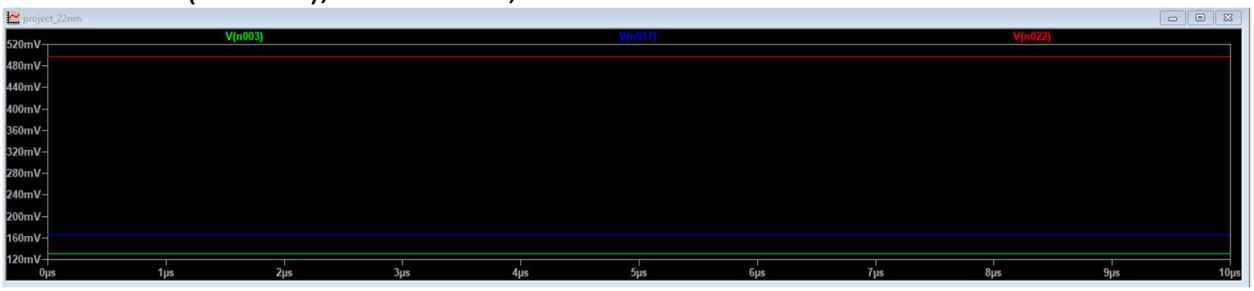
kept it same and modified where its required. I kept same frequency hence got same gm.

V_{bias1}=130.69mV

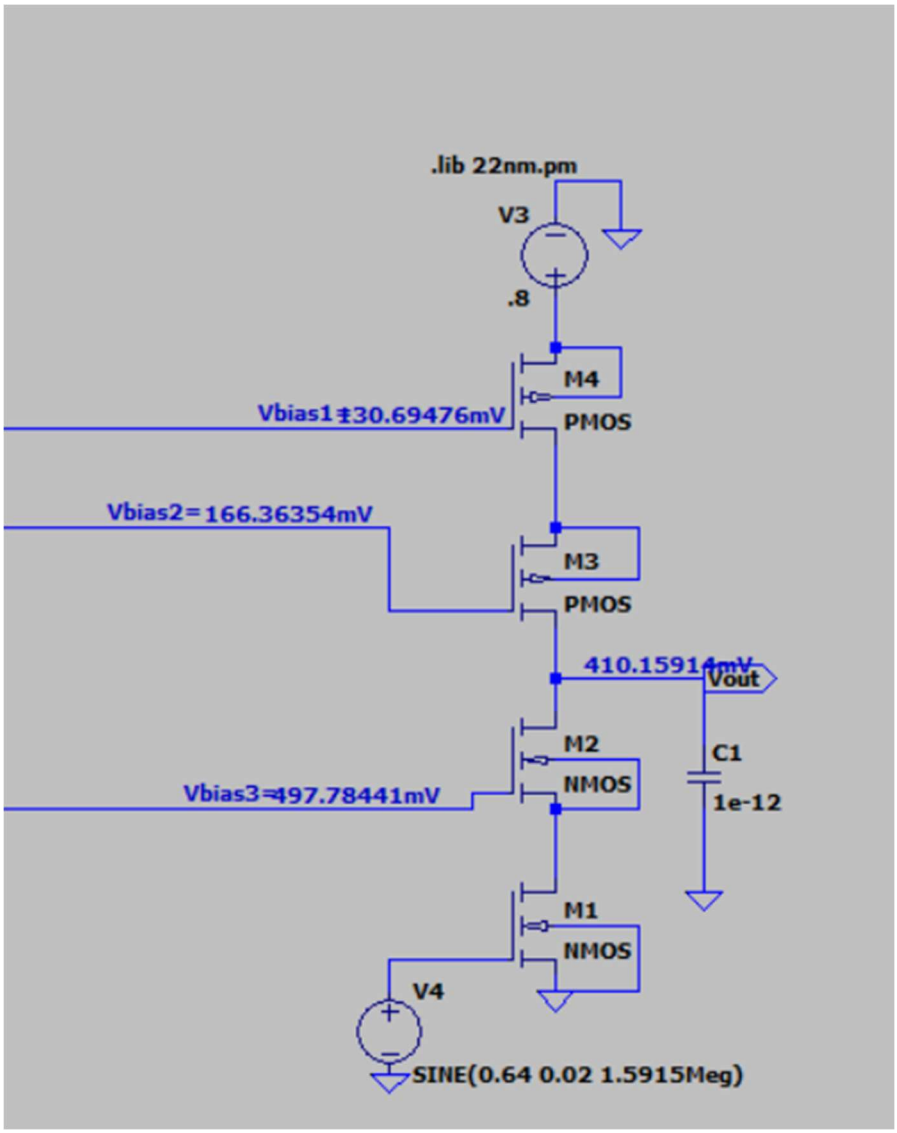
V_{bias2}=166.36mV

V_{bias3}=497.78mV

Vin=0.640V (DC Bias), Vac=20 mV, f=1.5915 MHz



Output:



V_{out} (DC Part) =410.16mV

Gain=410.16/20=20.51 or 26.23dB