5조

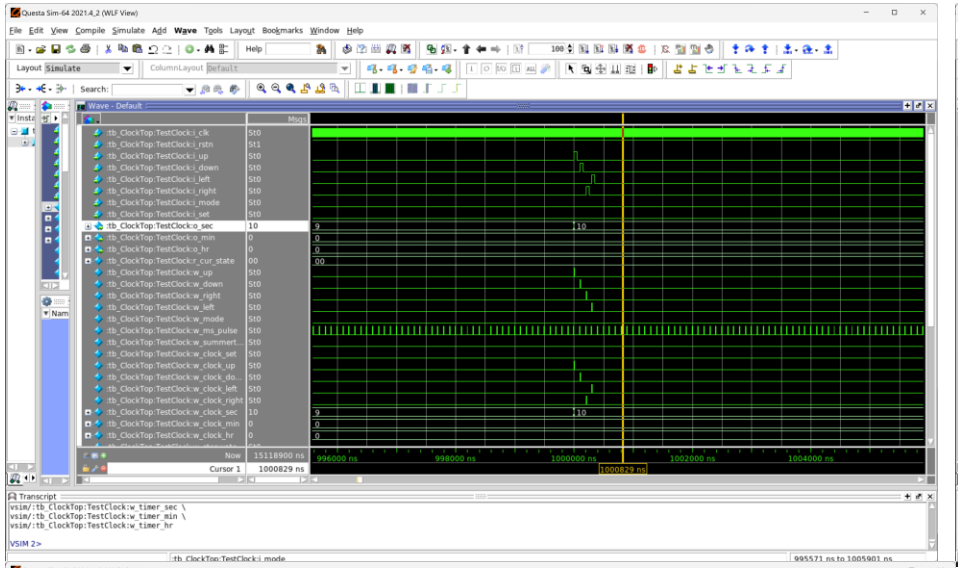
202210 정지헌
2019104054 차동훈

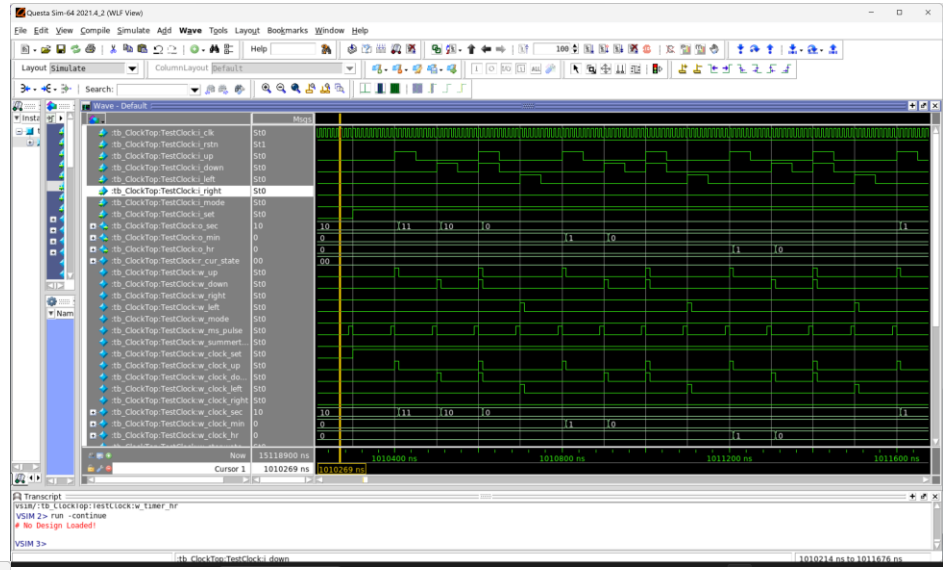
기존 Clock

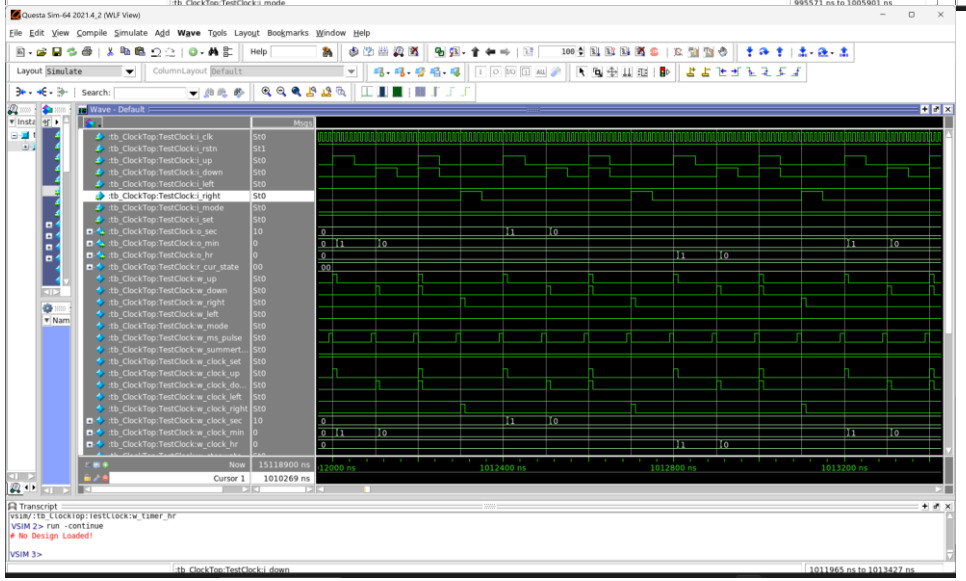
```
Library(s) Used:

    sky130_fd_sc_hd__tt_025C_1v80 (File: /home/dice05_2/dice/lib/db/sky130_fd_sc_hd__tt_025C_1v

Number of ports:                         1965
Number of nets:                          5191
Number of cells:                         3503
Number of combinational cells:           3141
Number of sequential cells:               154
Number of macros/black boxes:               0
Number of buf/inv:                        854
Number of references:                       7

Combinational area:              13352.806051
Buf/Inv area:                     3205.574299
Noncombinational area:            3853.696026
Macro/Black Box area:                0.000000
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:                 17206.502076
Total area:                 undefined
1
```

Project1에서 설계한 Digital Clock의 경우 합성 결과 면적이 너무 커 Clock을 다시 설계하였다.

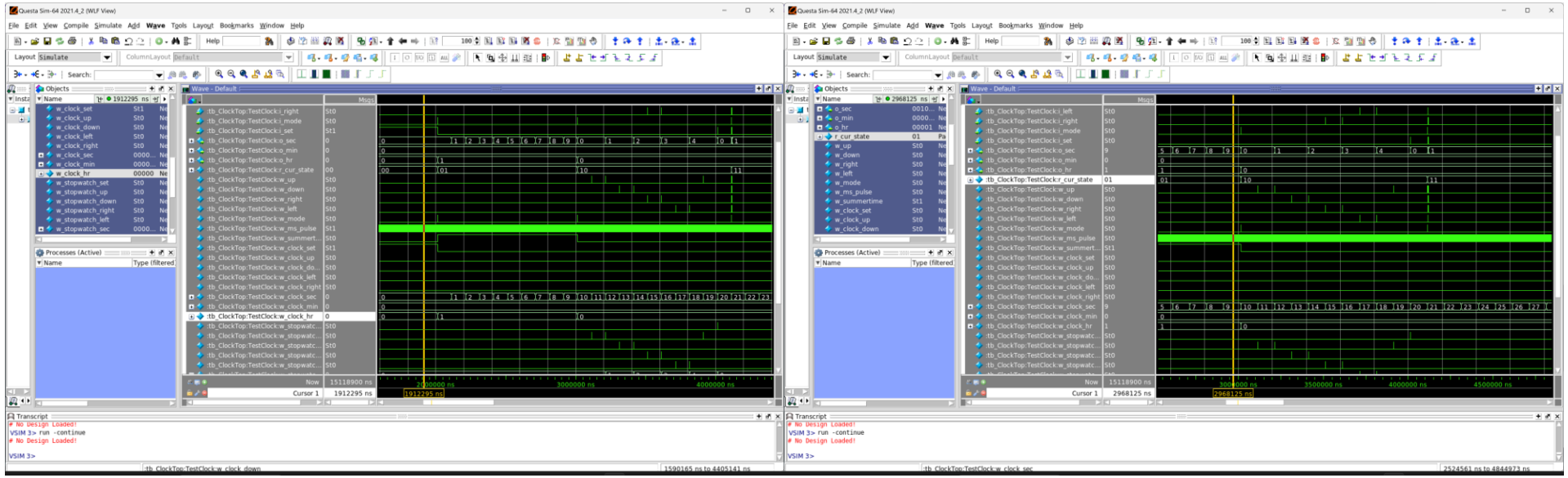
기본 Clock



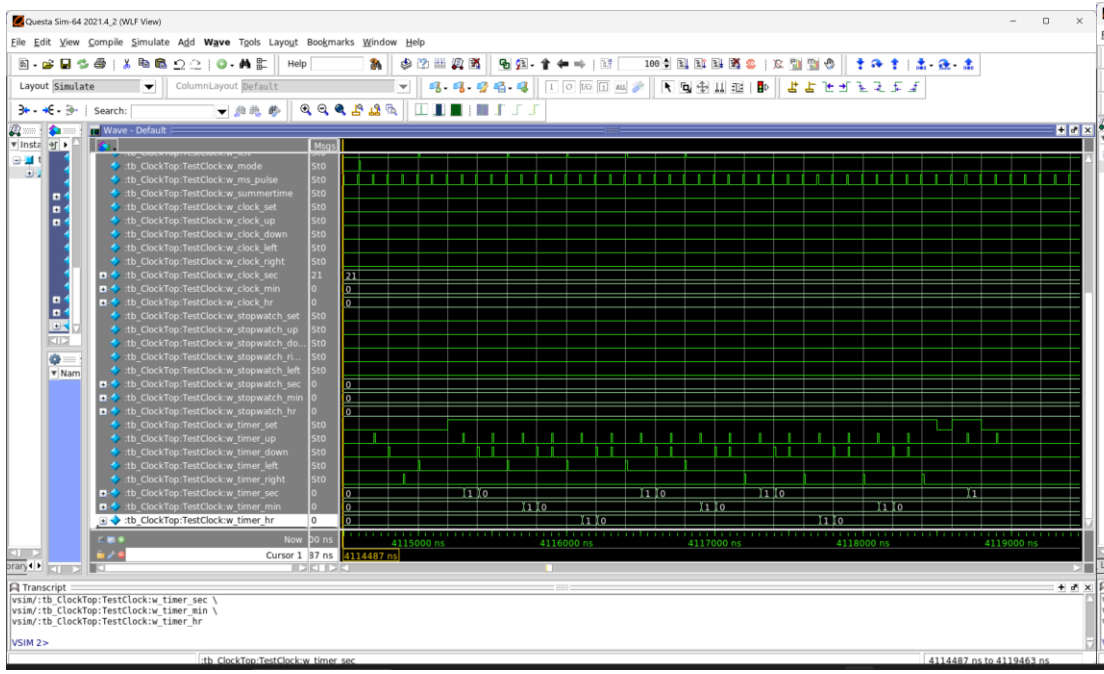


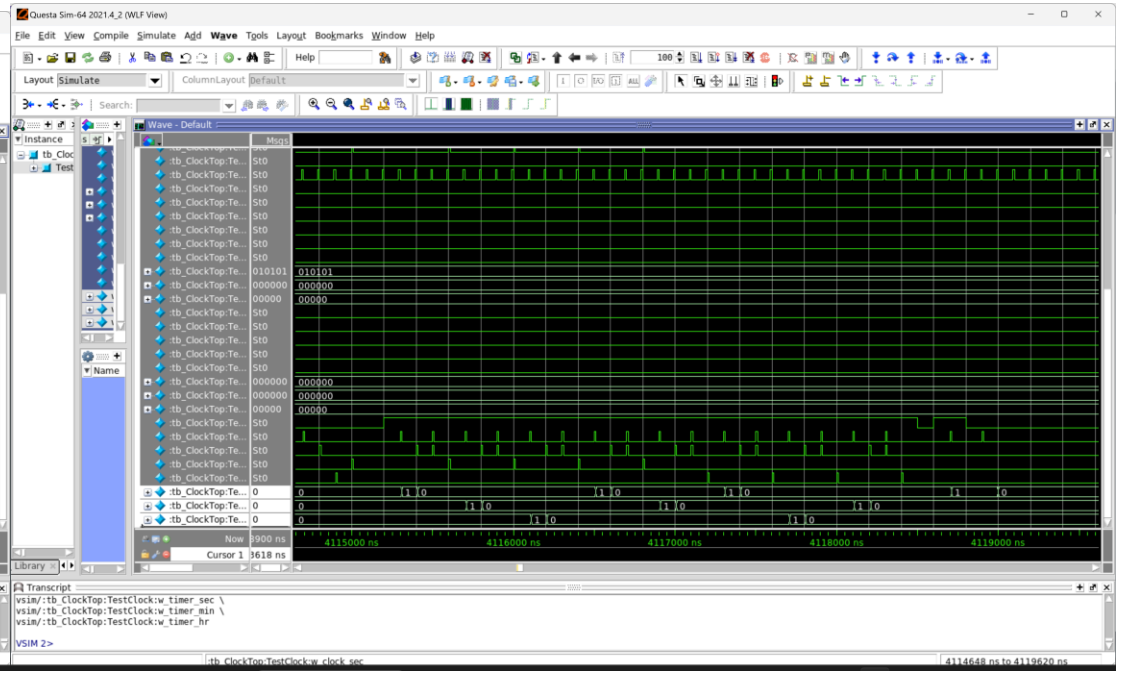


추가 기능1: StopWatch

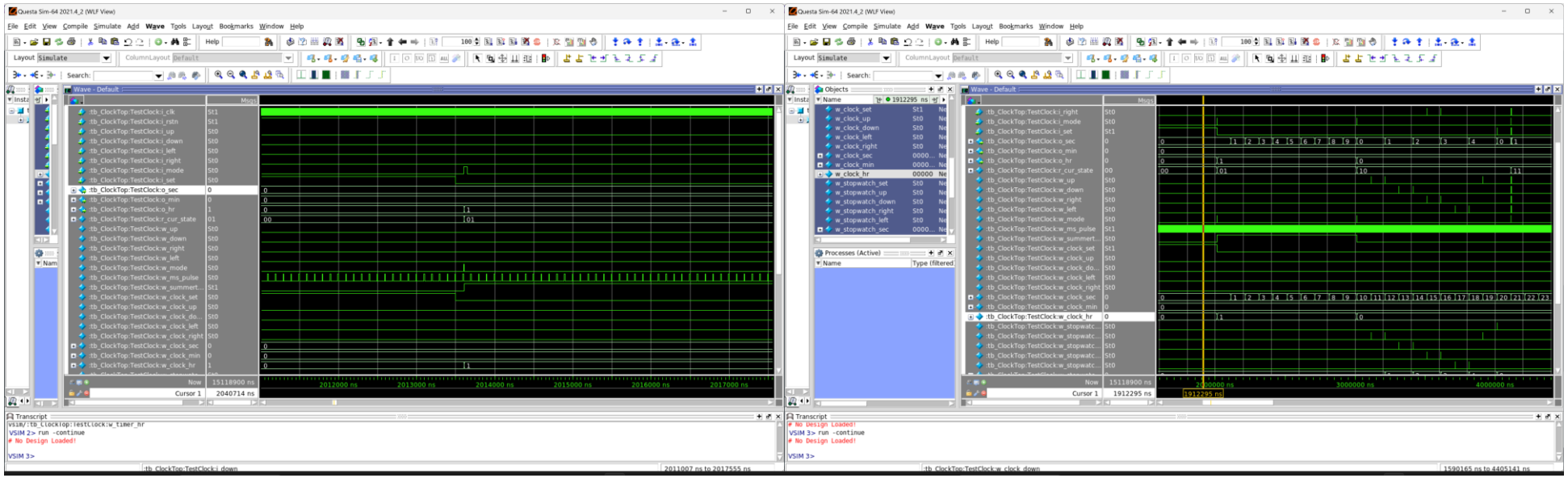


추가 기능2: Timer

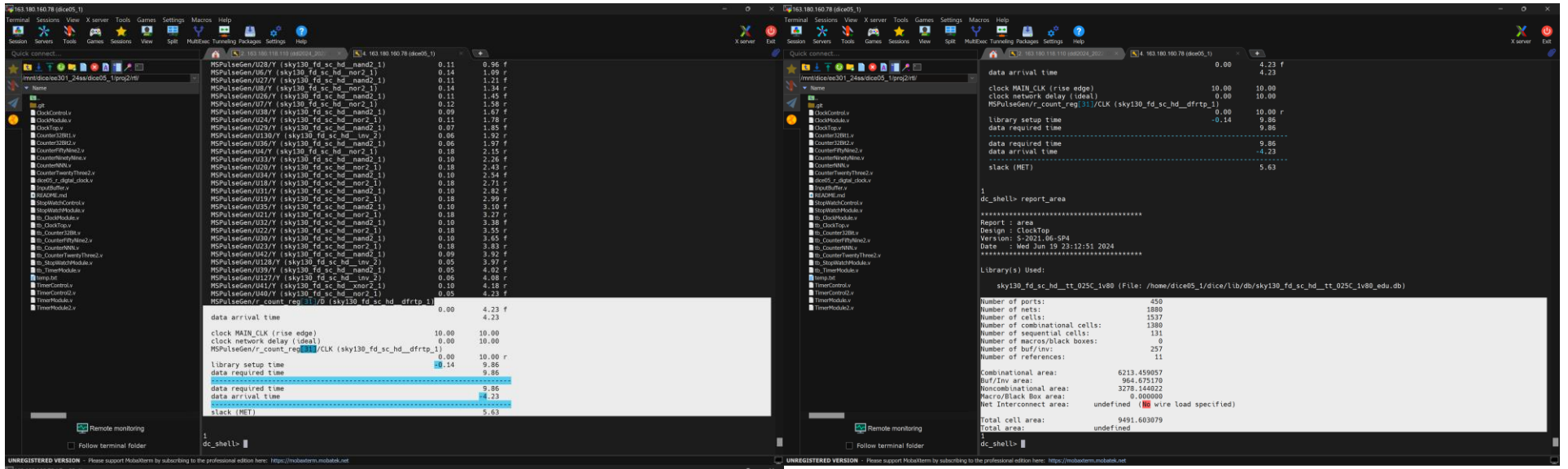

Questa Sim-64 2021.4_2 (WLF View)
Wave - Default
:tb_ClockTop:TestClock:w_mode
:tb_ClockTop:TestClock:w_ms_pulse
:tb_ClockTop:TestClock:w_summertime
:tb_ClockTop:TestClock:w_clock_set
:tb_ClockTop:TestClock:w_clock_up
:tb_ClockTop:TestClock:w_clock_down
:tb_ClockTop:TestClock:w_clock_left
:tb_ClockTop:TestClock:w_clock_right
:tb_ClockTop:TestClock:w_clock_sec
:tb_ClockTop:TestClock:w_clock_min
:tb_ClockTop:TestClock:w_clock_hr
:tb_ClockTop:TestClock:w_stopwatch_set
:tb_ClockTop:TestClock:w_stopwatch_up
:tb_ClockTop:TestClock:w_stopwatch_left
:tb_ClockTop:TestClock:w_stopwatch_sec
:tb_ClockTop:TestClock:w_stopwatch_min
:tb_ClockTop:TestClock:w_stopwatch_hr
:tb_ClockTop:TestClock:w_timer_set
:tb_ClockTop:TestClock:w_timer_up
:tb_ClockTop:TestClock:w_timer_down
:tb_ClockTop:TestClock:w_timer_left
:tb_ClockTop:TestClock:w_timer_right
:tb_ClockTop:TestClock:w_timer_sec
:tb_ClockTop:TestClock:w_timer_min
:tb_ClockTop:TestClock:w_timer_hr
4115000 ns
4116000 ns
4117000 ns
4118000 ns
4119000 ns
Transcript
vsim/:tb_ClockTop:TestClock:w_timer_sec \
vsim/:tb_ClockTop:TestClock:w_timer_min \
vsim/:tb_ClockTop:TestClock:w_timer_hr
VSIM 2>


Questa Sim-64 2021.4_2 (WLF View)
Wave - Default
4115000 ns
4116000 ns
4117000 ns
4118000 ns
4119000 ns
Transcript
vsim/:tb_ClockTop:TestClock:w_timer_sec \
vsim/:tb_ClockTop:TestClock:w_timer_min \
vsim/:tb_ClockTop:TestClock:w_timer_hr
VSIM 2>

추가 기능3: Summer Time



PPA


MSPulseGen/U28/Y (sky130_fd_sc_hd__nand2_1) 0.11 0.96 f
MSPulseGen/U6/Y (sky130_fd_sc_hd__nor2_1) 0.14 1.09 r
MSPulseGen/U27/Y (sky130_fd_sc_hd__nand2_1) 0.11 1.21 f
MSPulseGen/U8/Y (sky130_fd_sc_hd__nor2_1) 0.14 1.34 r
MSPulseGen/U26/Y (sky130_fd_sc_hd__nand2_1) 0.11 1.45 f
MSPulseGen/U7/Y (sky130_fd_sc_hd__nor2_1) 0.12 1.58 r
MSPulseGen/U38/Y (sky130_fd_sc_hd__nand2_1) 0.09 1.67 f
MSPulseGen/U24/Y (sky130_fd_sc_hd__nor2_1) 0.11 1.78 r
MSPulseGen/U29/Y (sky130_fd_sc_hd__nand2_1) 0.07 1.85 f
MSPulseGen/U130/Y (sky130_fd_sc_hd__inv_2) 0.06 1.92 r
MSPulseGen/U36/Y (sky130_fd_sc_hd__nand2_1) 0.05 1.97 f
MSPulseGen/U4/Y (sky130_fd_sc_hd__nor2_1) 0.18 2.15 r
MSPulseGen/U33/Y (sky130_fd_sc_hd__nand2_1) 0.10 2.26 f
MSPulseGen/U20/Y (sky130_fd_sc_hd__nor2_1) 0.18 2.43 r
MSPulseGen/U34/Y (sky130_fd_sc_hd__nand2_1) 0.10 2.54 f
MSPulseGen/U18/Y (sky130_fd_sc_hd__nor2_1) 0.18 2.71 r
MSPulseGen/U31/Y (sky130_fd_sc_hd__nand2_1) 0.10 2.82 f
MSPulseGen/U19/Y (sky130_fd_sc_hd__nor2_1) 0.18 2.99 r
MSPulseGen/U35/Y (sky130_fd_sc_hd__nand2_1) 0.10 3.10 f
MSPulseGen/U21/Y (sky130_fd_sc_hd__nor2_1) 0.18 3.27 r
MSPulseGen/U32/Y (sky130_fd_sc_hd__nand2_1) 0.10 3.38 f
MSPulseGen/U22/Y (sky130_fd_sc_hd__nor2_1) 0.18 3.55 r
MSPulseGen/U30/Y (sky130_fd_sc_hd__nand2_1) 0.10 3.65 f
MSPulseGen/U23/Y (sky130_fd_sc_hd__nor2_1) 0.18 3.83 r
MSPulseGen/U42/Y (sky130_fd_sc_hd__nand2_1) 0.09 3.92 f
MSPulseGen/U128/Y (sky130_fd_sc_hd__inv_2) 0.05 3.97 r
MSPulseGen/U39/Y (sky130_fd_sc_hd__nand2_1) 0.05 4.02 f
MSPulseGen/U127/Y (sky130_fd_sc_hd__inv_2) 0.06 4.08 r
MSPulseGen/U41/Y (sky130_fd_sc_hd__xnor2_1) 0.10 4.18 r
MSPulseGen/U40/Y (sky130_fd_sc_hd__nor2_1) 0.05 4.23 f
MSPulseGen/r_count_reg[31]/D (sky130_fd_sc_hd__dfrtp_1)
data arrival time 0.00 4.23 f
clock MAIN_CLK (rise edge) 10.00 10.00
clock network delay (ideal) 0.00 10.00
MSPulseGen/r_count_reg[31]/CLK (sky130_fd_sc_hd__dfrtp_1)
0.00 10.00 r
library setup time -0.14 9.86
data required time 9.86
data required time 9.86
data arrival time -4.23
slack (MET) 5.63
dc_shell>
Remote monitoring
Follow terminal folder
UNREGISTERED VERSION - Please support MobaXterm by subscribing to the professional edition here: https://mobaxterm.mobatek.net
data arrival time 0.00 4.23 f
clock MAIN_CLK (rise edge) 10.00 10.00
clock network delay (ideal) 0.00 10.00
MSPulseGen/r_count_reg[31]/CLK (sky130_fd_sc_hd__dfrtp_1)
0.00 10.00 r
library setup time -0.14 9.86
data required time 9.86
data required time 9.86
data arrival time -4.23
slack (MET) 5.63
dc_shell> report_area
Report : area
Design : ClockTop
Version: S-2021.06-SP4
Date : Wed Jun 19 23:12:51 2024
Library(s) Used:
sky130_fd_sc_hd__tt_025C_1v80 (File: /home/dice05_1/dice/lib/db/sky130_fd_sc_hd__tt_025C_1v80_edu.db)
Number of ports: 450
Number of nets: 1880
Number of cells: 1537
Number of combinational cells: 1380
Number of sequential cells: 131
Number of macros/black boxes: 0
Number of buf/inv: 257
Number of references: 11
Combinational area: 6213.459057
Buf/Inv area: 964.675170
Noncombinational area: 3278.144022
Macro/Black Box area: 0.000000
Net Interconnect area: undefined (No wire load specified)
Total cell area: 9491.603079
Total area: undefined
dc_shell>
Remote monitoring
Follow terminal folder
UNREGISTERED VERSION - Please support MobaXterm by subscribing to the professional edition here: https://mobaxterm.mobatek.net
Design : ClockTop
Version: S-2021.06-SP4
Date : Wed Jun 19 23:13:06 2024
Library(s) Used:
sky130_fd_sc_hd__tt_025C_1v80 (File: /home/dice05_1/dice/lib/db/sky130_fd_sc_hd__tt_025C_1v80_edu.db)
Operating Conditions: tt_025C_1v80 Library: sky130_fd_sc_hd__tt_025C_1v80
Wire Load Model Mode: top
Global Operating Voltage = 1.8
Power-specific unit information :
Voltage Units = 1V
Capacitance Units = 1.000000pf
Time Units = 1ns
Dynamic Power Units = 1mW (derived from V,C,T units)
Leakage Power Units = 1nW
Cell Internal Power = 555.9114 uW (97%)
Net Switching Power = 19.6274 uW (3%)
Total Dynamic Power = 575.5388 uW (100%)
Cell Leakage Power = 4.6642 nW
Power Group Internal Power Switching Power Leakage Power Total Power (%) Attrs
io_pad 0.0000 0.0000 0.0000 0.0000 (0.00%)
memory 0.0000 0.0000 0.0000 0.0000 (0.00%)
black_box 0.0000 0.0000 0.0000 0.0000 (0.00%)
clock_network 0.0000 0.0000 0.0000 0.0000 (0.00%)
register 0.5465 5.4708e-03 1.8037 0.5519 (95.90%)
(0.00%)
(4.10%)
Total 0.5559 mW 1.9627e-02 mW 4.6642 nW 0.5755 mW
dc_shell>
dc_shell>
dc_shell>
dc_shell>
Remote monitoring
Follow terminal folder
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