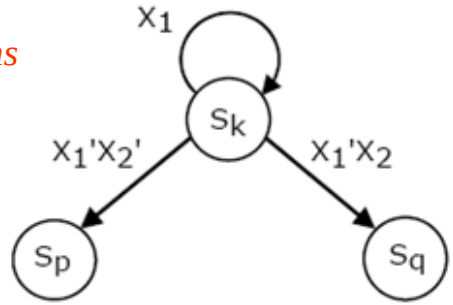
State graphs

Constraints on Input Labels for Every State S_k

1. If I_i and I_j are any pair of input labels on arcs exiting state S_k, then $I_iI_j = 0$ if $i \neq j$.
2. If n arcs exit state S_k and the n arcs have input labels $I_1, I_2, \ldots, I_n$, respectively, then $I_1 + I_2 + \ldots + I_n = 1$.

Notations for state graphs

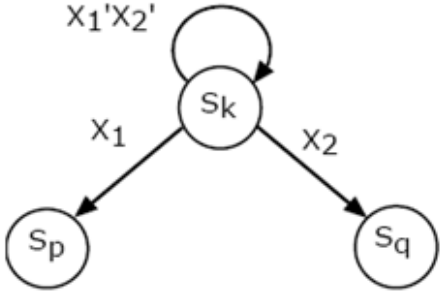
$X_i X_j / Z_p Z_q$



$(X_1)(X_1'X_2') = 0$
$(X_1)(X_1'X_2) = 0$
$(X_1'X_2')(X_1'X_2) = 0$
$X_1 + X_1'X_2' + X_1'X_2 = 1$

In case of
4 inputs (X_1, X_2, X_3, X_4)
and 4 outputs (Z_1, Z_2, Z_3, Z_4)

$X_1 X_4' / Z_2 Z_3$
means 1- - 0 / 0110



Inputs are X_1 X_2 X_3
($X_1 = X_2 = 1$ not allowed)

	000	001	010	011	100	101	110	111
S_k	S_k	S_k	S_q	S_q	S_p	S_p	–	–

1. **state table**

shows what the output is and what the next state is, for each input combination and each state.

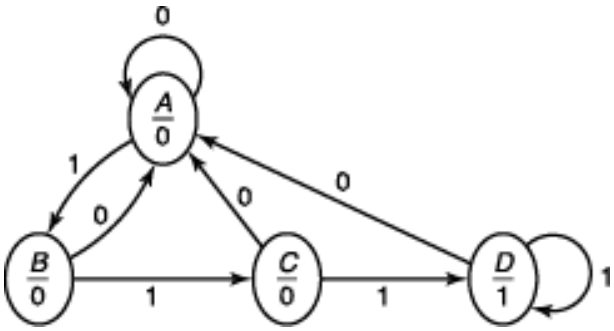
2. **state diagram** (or **state graph**)

a graphical representation of the system behavior, showing for each input combination and each state what the output is and what the next state is

Table 6.1 A state table.

Present state	Next state $x = 0$	Next state $x = 1$	Output
A	A	B	0
B	A	C	0
C	A	D	0
D	A	D	1

Figure 6.3 A state diagram.



Notation

the present state q

the next state q*, q†, q(t+Δ)

Next state?

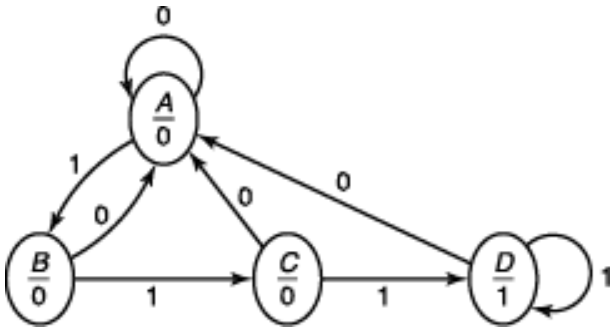
what will be stored in memory after this clock transition

Timing trace for the Table 6.1

Table 6.1 A state table.

Present state	Next state $x = 0$	Next state $x = 1$	Output
A	A	B	0
B	A	C	0
C	A	D	0
D	A	D	1

Figure 6.3 A state diagram.



Trace 6.2 Trace with state

x	0	1	1	0	1	1	1	0	0	1	0	1	1	1	1	1	0	0			
q	?	A	B	C	A	B	C	D	A	A	B	A	B	C	D	D	D	A	A	?	
z	?	0	0	0	0	0	0	1	0	0	0	0	0	0	1	1	1	0	0	0	0

Terminology once more

State: 메모리에 저장되어 있는 2진수 값.

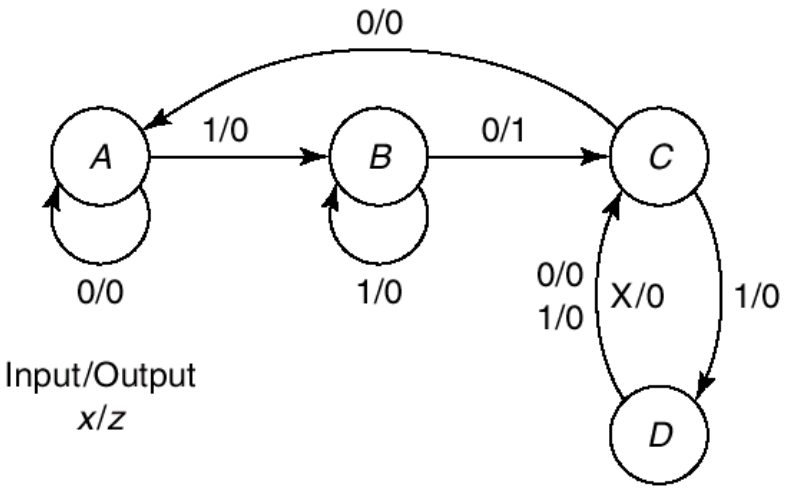
State table: PS와 각 입력조합에 대하여 출력과 NS를 나타낸 도표
(NS: 다음 클럭 후 메모리에 저장될 값)

State diagram or state graph: 상태표를 그림으로 나타낸 것.

Table 5.1 A sample state table.

	q^*		z	
q	$x = 0$	$x = 1$	$x = 0$	$x = 1$
A	A	B	0	0
B	C	B	1	0
C	A	D	0	0
D	C	C	0	0

Figure 5.3 A state diagram.

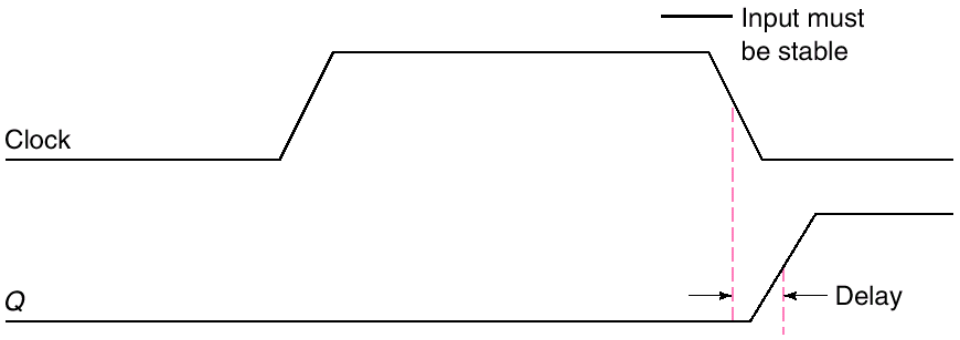


Sequential system is often called as *state machine* or *finite state machine*(FSM)

Flip-flop

- D, JK, SR, T
- clocked binary storage device
- rising (leading)-edge triggered or falling (or trailing)-edge triggered

Figure 5.6 Trailing-edge triggered flip flop timing.



D Flip-flop

Figure 6.7 *D* flip-flop diagrams.

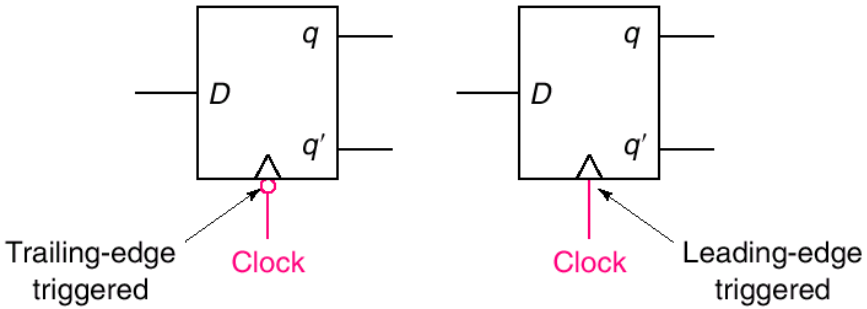
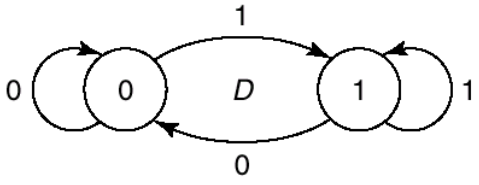
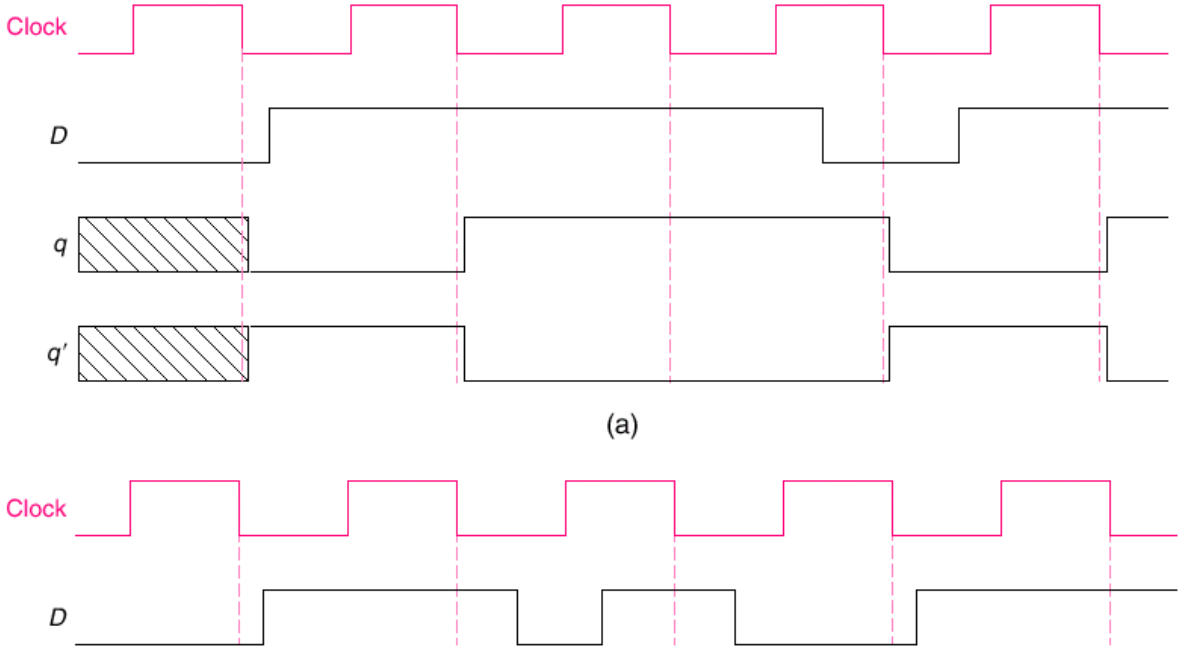


Figure 6.8 *D* flip flop state diagram.



Timing diagram of DFF

Figure 6.9 *D* flip flop timing diagram.



Preset and clear

Figure 6.13 Flip flop with clear and preset inputs.

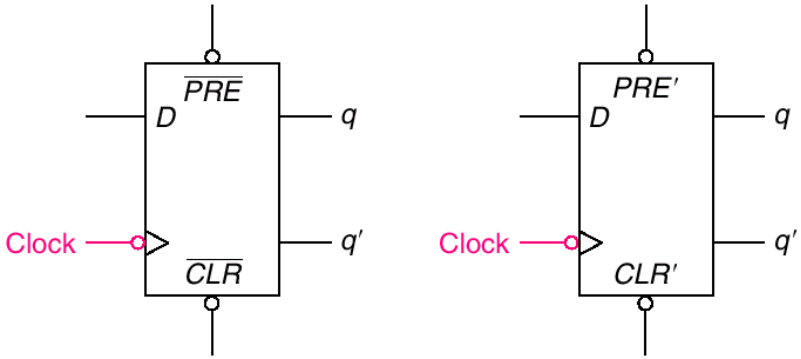
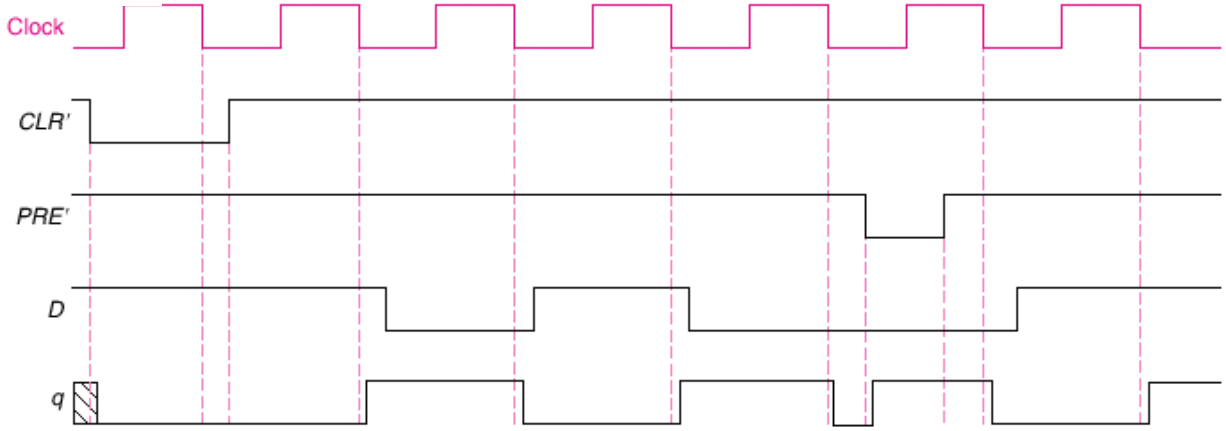


Table 6.3 *D* flip flop with clear and preset inputs behavioral table.

PRE′	CLR′	D	q	q*	
0	1	X	X	1	static
1	0	X	X	0	immediate
0	0	X	X	—	not allowed
1	1	0	0	0	
1	1	0	1	0	clocked
1	1	1	0	1	(as before)
1	1	1	1	1	

Figure 6.14 Time for flip flop with clear and preset.



S/RFF

Figure 6.15 *SR* flip flop state diagram.

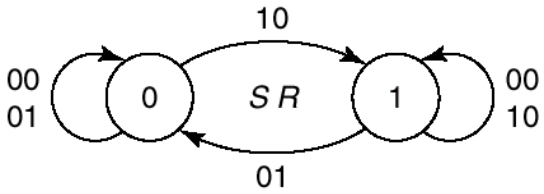
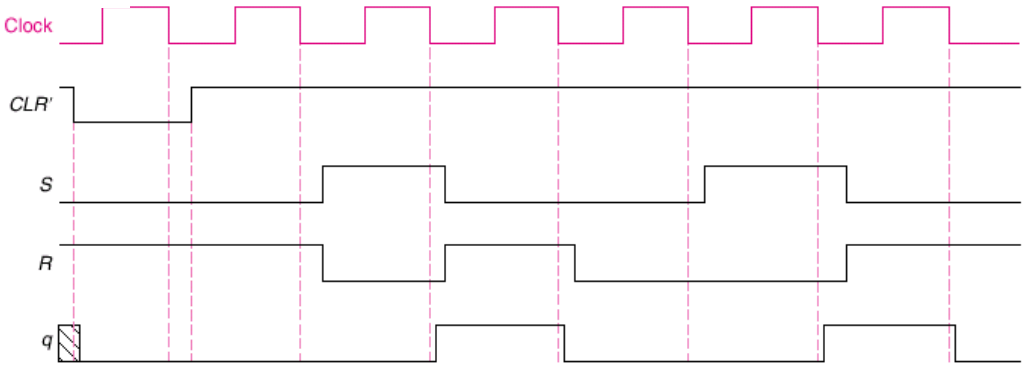


Figure 6.16 *SR* flip flop timing diagram.



TFF

Figure 6.17 *T* flip flop state diagram.

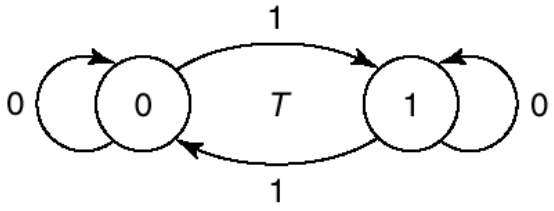
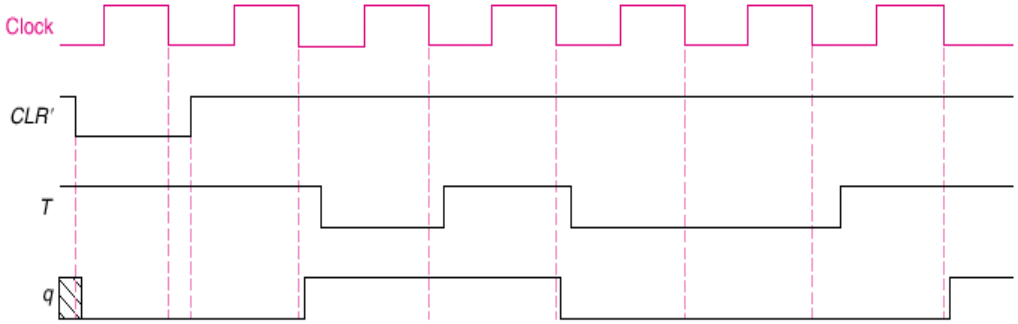


Figure 6.18 *T* flip flop timing diagram.



J/K FF

Figure 6.19 *JK* flip flop state diagram.

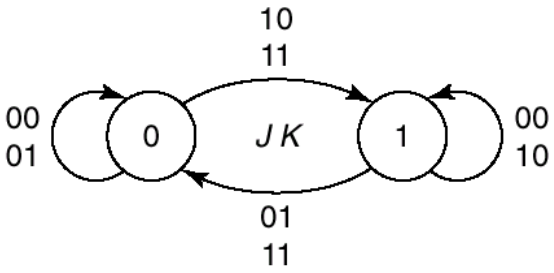
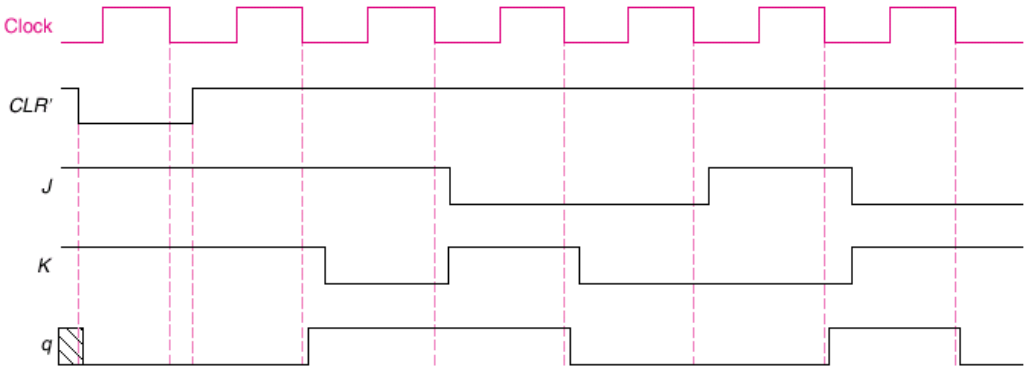


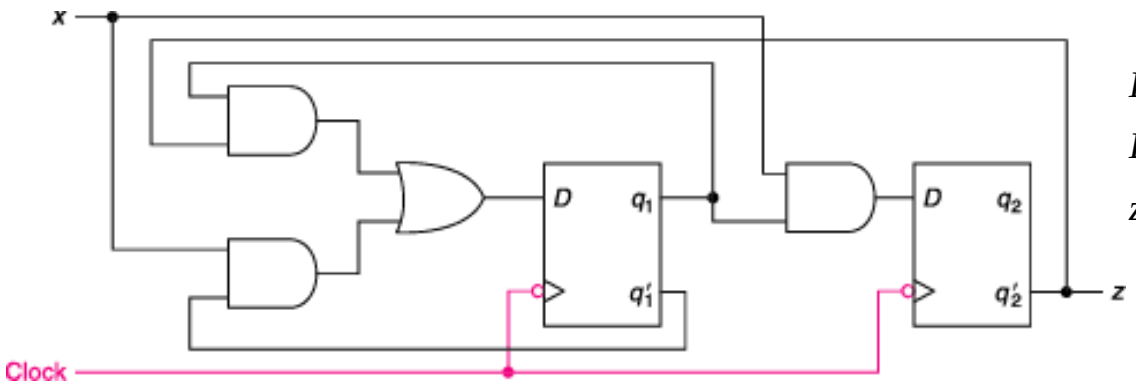
Figure 6.20 Timing diagram for *JK* flip flop.



Analysis of sequential systems

From state machine to state table or state diagram

Figure 6.21 **A D flip flop *Moore* model circuit.**



$$D_1 = q_1 q_2' + x q_1'$$

$$D_2 = x q_1$$

$$z = q_2'$$

Table 6.7a **Partial state table**

$q_1 q_2$	$q_1^* q_2^*$ $x = 0$	$x = 1$	z
0 0	0	1	1
0 1	0	1	0
1 0	1	1	1
1 1	0	0	0

Table 6.7b **Complete state table**

$q_1 q_2$	$q_1^* q_2^*$ $x = 0$	$x = 1$	z
0 0	0 0	1 0	1
0 1	0 0	1 0	0
1 0	1 0	1 1	1
1 1	0 0	0 1	0

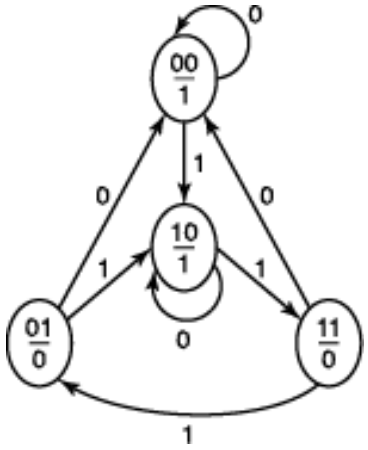
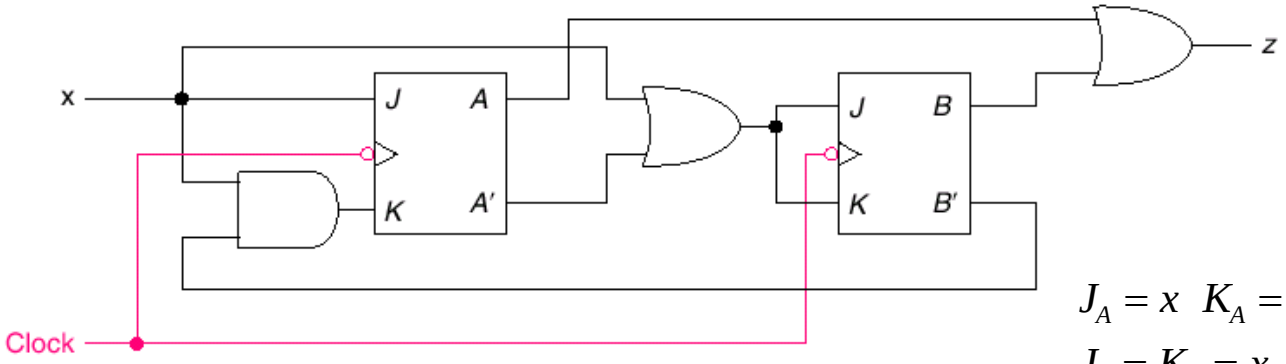


Figure 6.22 **A Moore state diagram.**

Figure 6.23 A Moore model circuit.



$$J_A = x \quad K_A = xB'$$
$$J_B = K_B = x + A'$$
$$z = A + B$$

Outline of state table.

A B	A* B* x = 0	A* B* x = 1	z
0 0			0
0 1			1
1 0			1
1 1			1

Table 6.8a State table with first two entries.

A B	A* B* x = 0	A* B* x = 1	z
0 0	0 1		0
0 1	0 0		1
1 0			1
1 1			1

A B = 0 0, x = 0 $\rightarrow$ $J_A = K_A = 0$ and $J_B = K_B = 1$

A B = 0 1, x = 0 $\rightarrow$ $J_A = K_A = 0$ and $J_B = K_B = 1$

$$J_A = x \quad K_A = xB'$$
$$J_B = K_B = x + A'$$
$$z = A + B$$

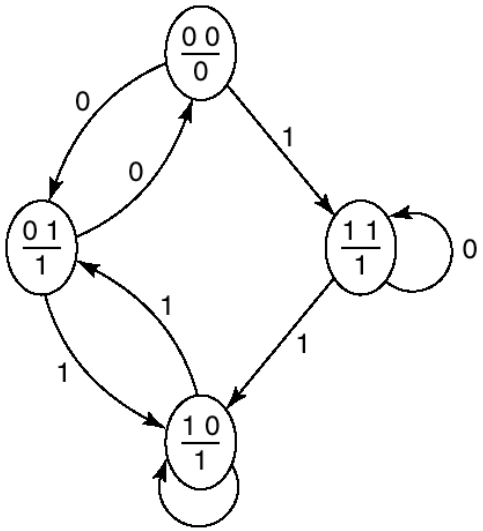
Table 6.8b State table with A^* entered.

A B	A* B* x = 0	x = 1	z
0 0	0	1	0
0 1	0	1	1
1 0	1	0	1
1 1	1	1	1

Table 6.8c Completed state table.

A B	A* B* x = 0	x = 1	z
0 0	0 1	1 1	0
0 1	0 0	1 0	1
1 0	1 0	0 1	1
1 1	1 1	1 0	1

Figure 6.25 State diagram for Table 6.8.



Timing trace 6.3 Trace for Table 6.8.

x	0		0	1	0	1	1	0	
A	0	→	0	0	1	1	1	0	0
B	0		1	0	1	1	0	1	0	1
z	0		1	0	1	1	1	1	0	1

Check the timing diagram in Fig. 6.24

Figure 6.24 Timing diagram for Table 6.8.

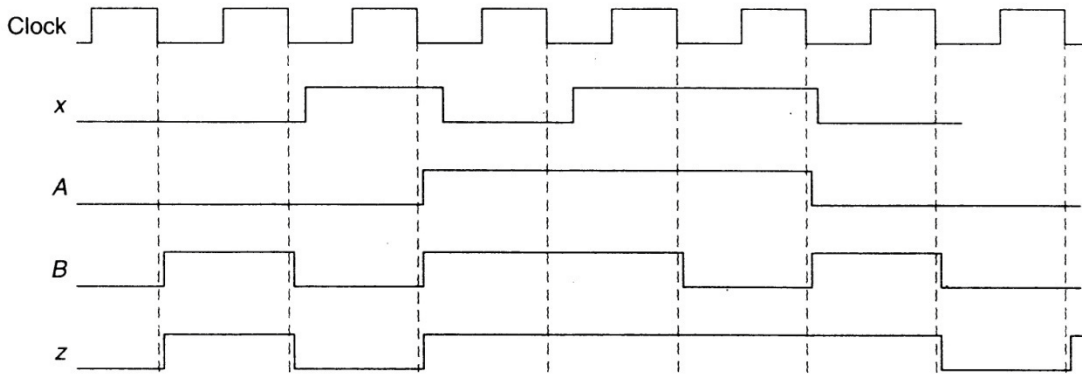
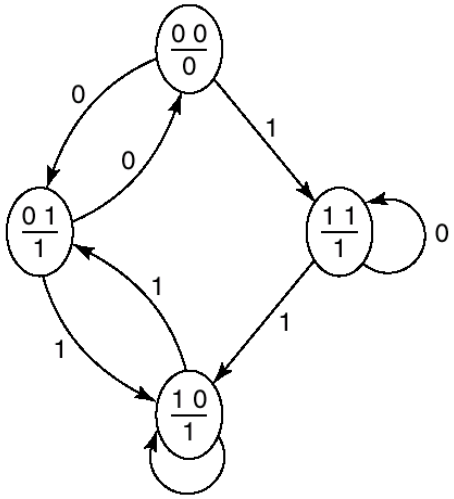


Figure 6.25 State diagram for Table 6.8.



An Example: A Mealy machine

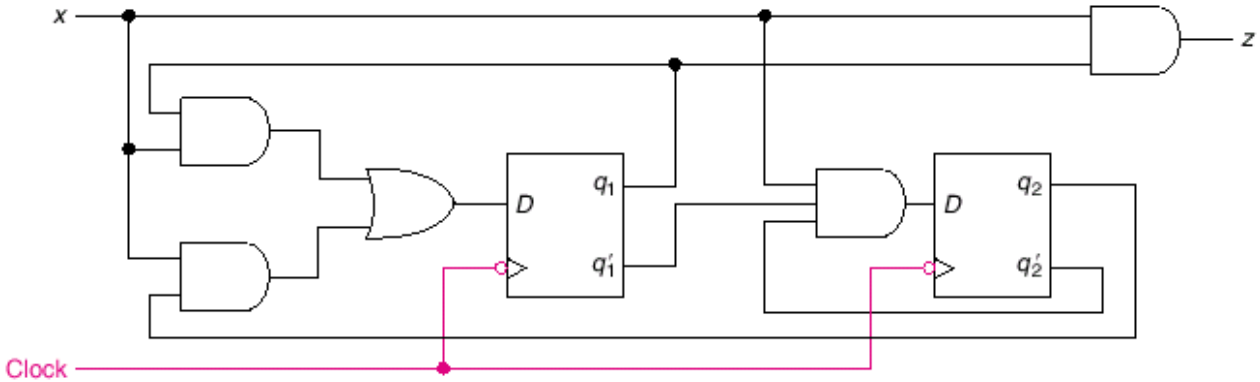


Figure 6.26

1. Logic equation

$$D_1 = xq_1 + xq_2$$
$$D_2 = xq_1'q_2'$$
$$z = xq_1$$

$$q_1^* = xq_1 + xq_2$$
$$q_2^* = xq_1'q_2'$$

2. State table

q	q^* $x=0$	q^* $x=1$	z $x=0$	z $x=1$
0 0	0 0	0 1	0	0
0 1	0 0	1 0	0	0
1 0	0 0	1 0	0	1
1 1	0 0	1 0	0	1

Table 6.9

3. State diagram

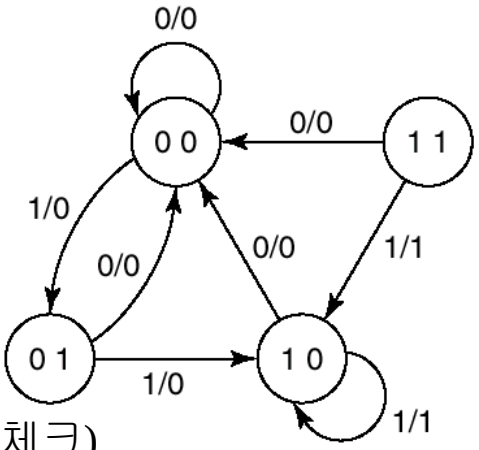


Figure 6.27

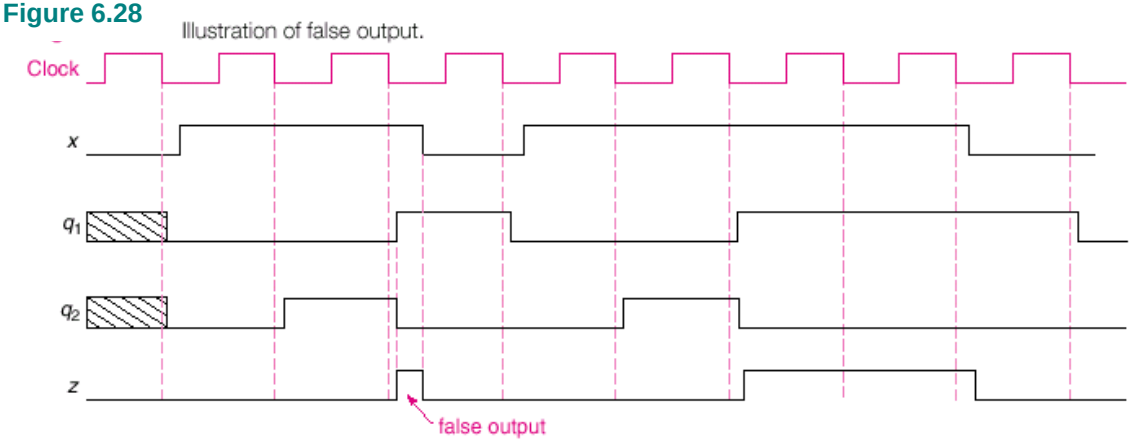
4. Read the state diagram

- CE 6의 해. (3개의 연속된 1을 체크)
- state “11” is unreachable
- 3 states problem
- 초기화를 하지 않아도 처음 0 이 입력된 후 정상 동작

5. Simulation results : timing diagram

Glitch in the output <-- Mealy machine

Figure 6.28



HWork example6.1, 6.2