HW#5 디지털 회로 설계 및 언어 20151040zn 박경진

```
module counter_4bit(
  output reg [3:0] Q,
  output reg C_out,
  input [3:0] I,
  input clk, clrn, load, count
);

  always @(posedge clk, negedge clrn)
    if (~clrn) Q <= 4'b0000; C_out <= 1'b0;
    else
      if (load) Q <= I;
      else
        if (count)
          if(Q == 4'b1111) Q <= 4'b0000; C_out <= 1'b1;
          else Q <= Q+4'b0001;
        else Q <= Q;

endmodule
```

begin ~ end