HW#9 디지털 회로 설계 및 언어 월수 9:00~10:15 2015104027 박정진

Case 1)
pstate = 0 (blocking assignment)
always (S, A, pstate) no else block

```
module RTL_Ex_8_2_v_jin(
   output reg E, F,
   output reg[3:0] A,
   input S, CLK, Clrn
   );
   //specify system registers
   reg [1:0] pstate, nstate; //control register
   //Encode the states
   parameter T0 = 2'b00, T1 = 2'b01, T2 = 2'b10;
   //state transition for control
   always @(posedge CLK, negedge Clrn) begin
      if(~Clrn) pstate = T0; //initial state
      else pstate <= nstate; //colcked operations
   end

   //decision box -> decide next state
   always @(S, A, pstate) begin
      case(pstate)
         T0:
         begin
            if(S) nstate = T1;
         end
         T1:
         begin
            if(A[2]&A[3]) nstate = T2;
         end
         T2:
         begin
            nstate = T0;
         end
      endcase
   end
```

Flow Summary

Flow Status	Successful - Fri Nov 15 03:16:00 2
Quartus Prime Version	15.1.0 Build 185 10/21/2015 SJ Lit
Revision Name	RTL_Ex_8_2_v_jin
Top-level Entity Name	RTL_Ex_8_2_v_jin
Family	Cyclone IV E
Device	EP4CE10E22C6
Timing Models	Final
Total logic elements	18 / 10,320 (< 1 %)
Total combinational functions	14 / 10,320 (< 1 %)
Dedicated logic registers	9 / 10,320 (< 1 %)
Total registers	9
Total pins	9 / 92 (10 %)
Total virtual pins	0
Total memory bits	0 / 423,936 (0 %)
Embedded Multiplier 9-bit elements	0 / 46 (0 %)
Total PLLs	0 / 2 (0 %)

Analysis & Synthesis Resource Usage Summary

	Resource	
1	Estimated Total logic elements	14
2		
3	Total combinational functions	14
4	▼ Logic element usage by number of LUT inputs	
1	-- 4 input functions	4
2	-- 3 input functions	6
3	-- <=2 input functions	4
5		
6	▼ Logic elements by mode	
1	-- normal mode	14
2	-- arithmetic mode	0
7		
8	▼ Total registers	9
1	-- Dedicated logic registers	9
2	-- I/O registers	0
9		
10	I/O pins	9

```
17049 1 registers lost all their fanouts during netlist optimizations.
16010 Generating hard_block partition "hard_block:auto_generated_inst"
21057 Implemented 22 device resources after synthesis - the final resource count might be different
      Quartus Prime Analysis & Synthesis was successful. 0 errors, 15 warnings
```

Estimated Total logic elements : 14
Total Combinational functions : 14
Total Registers : 9

Case 2)
pstate <= 0 (blocking assignment)
always (S, A, pstate) no else block

```
module RTL_Ex_8_2_v_jin(
   output reg E, F,
   output reg[3:0] A,
   input S, CLK, Clrn
   );
   //specify system registers
   reg [1:0] pstate, nstate; //control register
   //Encode the states
   parameter T0 = 2'b00, T1 = 2'b01, T2 = 2'b10;
   //state transition for control
   always @(posedge CLK, negedge Clrn) begin
      if(~Clrn) pstate <= T0; //initial state
      else pstate <= nstate; //colcked operations
   end

   //decision box -> decide next state
   always @(S, A, pstate) begin
      case(pstate)
         T0:
         begin
            if(S) nstate = T1;
         end
         T1:
         begin
            if(A[2]&A[3]) nstate = T2;
         end
         T2:
         begin
            nstate = T0;
         end
      endcase
   end
```

Flow Summary	
Flow Status	Successful - Fri Nov 15 03:16:00 2
Quartus Prime Version	15.1.0 Build 185 10/21/2015 SJ Lit
Revision Name	RTL_Ex_8_2_v_jin
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Timing Models	Final
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Total combinational functions	14 / 10,320 (< 1 %)
Dedicated logic registers	9 / 10,320 (< 1 %)
Total registers	9
Total pins	9 / 92 (10 %)
Total virtual pins	0
Total memory bits	0 / 423,936 (0 %)
Embedded Multiplier 9-bit elements	0 / 46 (0 %)
Total PLLs	0 / 2 (0 %)

Analysis & Synthesis Resource Usage Summary		
	Resource	
1	Estimated Total logic elements	14
2		
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9		
10	I/O pins	9

Estimated Total logic elements : 14
Total Combinational functions : 14
Total Registers : 9
Case 1) 과 차이 없음

Case 3)
always (S, A, pstate) have all else block

```
module RTL_Ex_8_2_v_jin(
   output reg E, F,
   output reg[3:0] A,
   input S, CLK, Clrn
   );
   //specify system registers
   reg [1:0] pstate, nstate; //control register
   //Encode the states
   parameter T0 = 2'b00, T1 = 2'b01, T2 = 2'b10;
   //state transition for control
   always @(posedge CLK, negedge Clrn) begin
      if(~Clrn) pstate <= T0; //initial state
      else pstate <= nstate; //colcked operations
   end

   //decision box -> decide next state
   always @(S, A, pstate) begin
      case(pstate)
         T0:
         begin
            if(S) nstate = T1;
            else nstate = T0;
         end
         T1:
         begin
            if(A[2]&A[3]) nstate = T2;
            else nstate = T1;
         end
         T2:
         begin
            nstate = T0;
         end
      endcase
   end
```

Flow Summary	
Flow Status	Successful - Thu Nov 14 22:38:10
Quartus Prime Version	15.1.0 Build 185 10/21/2015 SJ Lit
Revision Name	RTL_Ex_8_2_v_jin
Top-level Entity Name	RTL_Ex_8_2_v_jin
Family	Cyclone IV E
Device	EP4CE10E22C6
Timing Models	Final
Total logic elements	12 / 10,320 (< 1 %)
Total combinational functions	11 / 10,320 (< 1 %)
Dedicated logic registers	9 / 10,320 (< 1 %)
Total registers	9
Total pins	9 / 92 (10 %)
Total virtual pins	0
Total memory bits	0 / 423,936 (0 %)
Embedded Multiplier 9-bit elements	0 / 46 (0 %)
Total PLLs	0 / 2 (0 %)

Analysis & Synthesis Resource Usage Summary		
	Resource	
1	Estimated Total logic elements	11
2		
3	Total combinational functions	11
4	▼ Logic element usage by number of LUT inputs	
1	-- 4 input functions	4
2	-- 3 input functions	4
3	-- <=2 input functions	3
5		
6	▼ Logic elements by mode	
1	-- normal mode	11
2	-- arithmetic mode	0
7		
8	▼ Total registers	9
1	-- Dedicated logic registers	9
2	-- I/O registers	0
9		
10	I/O pins	9

Estimated Total logic elements : 11 (3 개 감소)
Total Combinational functions : 11
Total Registers : 9

Case 4)
always (S, A, pstate) all non-block assignment

```
module RTL_Ex_8_2_v_jin(
   output reg E, F,
   output reg[3:0] A,
   input S, CLK, Clrn
   );
   //specify system registers
   reg [1:0] pstate, nstate; //control register
   //Encode the states
   parameter T0 = 2'b00, T1 = 2'b01, T2 = 2'b10;
   //state transition for control
   always @(posedge CLK, negedge Clrn) begin
      if(~Clrn) pstate <= T0; //initial state
      else pstate <= nstate; //colcked operations
   end

   //decision box -> decide next state
   always @(S, A, pstate) begin
      case(pstate)
         T0:
         begin
            if(S) nstate <= T1;
            else nstate <= T0;
         end
         T1:
         begin
            if(A[2]&A[3]) nstate <= T2;
            else nstate <= T1;
         end
         T2:
         begin
            nstate <= T0;
         end
      endcase
   end
```

Flow Summary	
Flow Status	Successful - Fri Nov 15 03:09:29 2
Quartus Prime Version	15.1.0 Build 185 10/21/2015 SJ Lit
Revision Name	RTL_Ex_8_2_v_jin
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Total registers	9
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Total virtual pins	0
Total memory bits	0 / 423,936 (0 %)
Embedded Multiplier 9-bit elements	0 / 46 (0 %)
Total PLLs	0 / 2 (0 %)

Analysis & Synthesis Resource Usage Summary		
	Resource	
1	Estimated Total logic elements	11
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4	▼ Logic element usage by number of LUT inputs	
1	-- 4 input functions	4
2	-- 3 input functions	4
3	-- <=2 input functions	3
5		
6	▼ Logic elements by mode	
1	-- normal mode	11
2	-- arithmetic mode	0
7		
8	▼ Total registers	9
1	-- Dedicated logic registers	9
2	-- I/O registers	0
9		
10	I/O pins	9

Estimated Total logic elements : 11
Total Combinational functions : 11
Total Registers : 9
Case 3) 과 차이 없음

Case 5)
always (S, A, pstate) x'b -> decimal integer

```
36    //register tranfer operations
37    always @(posedge CLK) begin
38       case(pstate)
39          T0:
40          begin
41             if(S) begin
42                A <= 0;
43                F <= 0;
44             end
45          end
46          T1:
47          begin
48             A <= A+1;
49             if(A[3]) begin
50                E <= 1;
51             end
52             else begin
53                E <= 0;
54             end
55          end
56          T2:
57             F <= 1;
58       endcase
59    end
60 endmodule
```

Flow Summary	
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Total pins	9 / 92 (10 %)
Total virtual pins	0
Total memory bits	0 / 423,936 (0 %)
Embedded Multiplier 9-bit elements	0 / 46 (0 %)
Total PLLs	0 / 2 (0 %)

Analysis & Synthesis Resource Usage Summary		
	Resource	
1	Estimated Total logic elements	11
2		
3	Total combinational functions	11
4	▼ Logic element usage by number of LUT inputs	
1	-- 4 input functions	4
2	-- 3 input functions	4
3	-- <=2 input functions	3
5		
6	▼ Logic elements by mode	
1	-- normal mode	11
2	-- arithmetic mode	0
7		
8	▼ Total registers	9
1	-- Dedicated logic registers	9
2	-- I/O registers	0
9		
10	I/O pins	9

Estimated Total logic elements : 11
Total Combinational functions : 11
Total Registers : 9
Case 3) 과 차이 없음

최종 코드 :

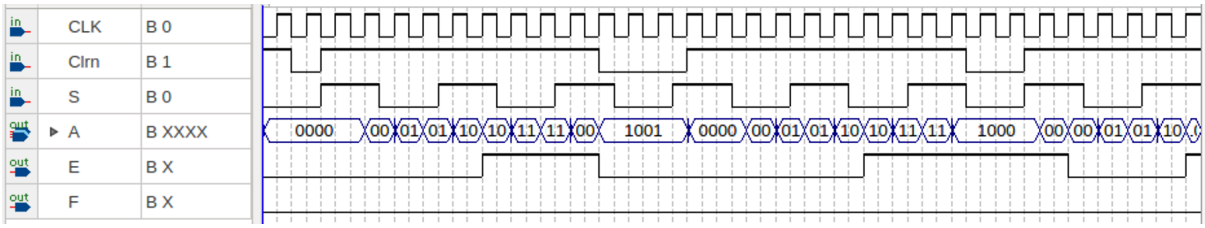
```v
module RTL_Ex_8_2_v_jin(
    output reg E, F,
    output reg[3:0] A,
    input S, CLK, Clrn
    );
    //specify system registers
    reg [1:0] pstate, nstate; //control register
    //Encode the states
    parameter T0 = 2'b00, T1 = 2'b01, T2 = 2'b10;
    //state transition for control
    always @(posedge CLK, negedge Clrn) begin
        if(~Clrn) pstate <= T0; //initial state
        else begin
            pstate <= nstate; //clocked operations
            case(pstate)
                T0:
                begin
                    if(S) begin
                        A <= 4'b0000;
                        F <= 1'b0;
                    end
                end
                T1:
                begin
                    A <= A+4'b0001;
                    if(A[2]) begin
                        E <= 1'b1;
                    end
                    else begin
                        E <= 1'b0;
                    end
                end
                T2:
                    F <= 1'b1;
            endcase
        end
    end

    //decision box -> decide next state
    always @(S, A, pstate) begin
        case(pstate)
            T0:
            begin
                if(S) nstate = T1;
                else nstate = T0;
            end
            T1:
            begin
                if(A[2]&A[3]) nstate = T2;
                else nstate = T1;
            end
            T2:
            begin
                nstate = T0;
            end
        endcase
    end
endmodule
```

```v
module RTL_Ex_8_2_v_jin(
    output reg E, F,
    output reg[3:0] A,
    input S, CLK, Clrn
    );
    //specify system registers
    reg [1:0] pstate, nstate; //control register
    //Encode the states
    parameter T0 = 2'b00, T1 = 2'b01, T2 = 2'b10;
    //state transition for control
    always @(posedge CLK, negedge Clrn) begin
        if(~Clrn) pstate <= T0; //initial state
        else begin
            pstate <= nstate; //clocked operations
        end
    end

    //decision box -> decide next state
    always @(S, A, pstate) begin
        case(pstate)
            T0:
            begin
                if(S) nstate = T1;
                else nstate = T0;
            end
            T1:
            begin
                if(A[2]&A[3]) nstate = T2;
                else nstate = T1;
            end
            T2:
            begin
                nstate = T0;
            end
        endcase
    end

    always @(posedge CLK) begin
        case(pstate)
            T0:
            begin
                if(S) begin
                    A <= 4'b0000;
                    F <= 1'b0;
                end
            end
            T1:
            begin
                A <= A+4'b0001;
                if(A[2]) begin
                    E <= 1'b1;
                end
                else begin
                    E <= 1'b0;
                end
            end
            T2:
                F <= 1'b1;
        endcase
    end
```

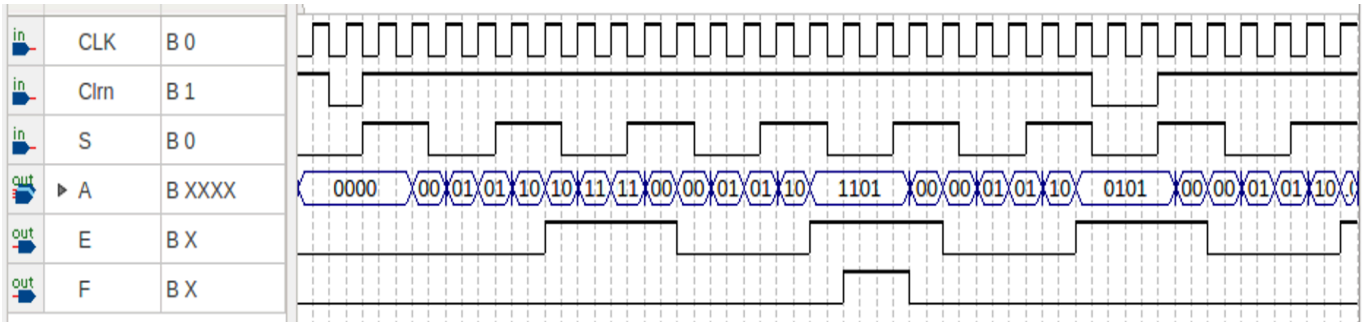


Register operation 의 $A \leftarrow A + 4'b0001$ 동작에서 carry 가 있을 시 A 의 값이 변화하면서 A register 에 저장된 값이 바뀌며 생기는 delay time 이 존재하는 것을 알았고 이와 마찬가지로 Flip-Flop E, F 도 해당 값이 바뀌면 flip flop 에 의한 delay 가 생기는 것을 알 수 있었다.

코드 상에서 $A \leftarrow A + 1'b1$ 로 바꿔도 같았으며 이는 값이 flip-flop 을 통과하며 생기는 어쩔 수 없는 delay time 이라는 것을 알게 되었다. 그래서 이후 combinational logic 으로 control unit 을 짤 때 combinational 은 기억을 하지 못하므로 나온 결과를 Flip-Flop 에 의도적으로 통과 시켜 Register 와 같은 Delay time 을 주어서 연산을 맞추는 것도 필요 할 것 같다는 생각이 든다.

일반적으로 회로가 돌아가고 첫 edge 에서 두 번째 edge 는 클리어 신호를 주어 회로의 초기값을 지정한다. 하지만 책에 있는 대로 state operation 과 Register operation 을 코드 상에서 분리하면 현재 디자인에서는 문제가 없지만 정확하게 이는 시스템 전체를 초기화 시키는 Clrn 의 의미가 아니다.(단순히 state 만을 초기화) 만약 시스템 전체적으로 초기화를 진행하는 Clrn 이라는 의미의 동작을 행하려면 이런 분리된 코드에서는 Register operation 에서도 negedge Clrn 을 추가해 초기화를 해야 한다. 그렇지 않으면 Clrn 0 일 때에도 Clrn 의 신호를 무시한 채 posedge CLK 일 때 Register operation 은 따로 동작하기에 원하는 시스템 전체적으로 초기화가 진행되지 않을 수 있다. 위의 VWF 결과에서도 확인 할 수 있듯이 Clrn 신호가 들어갔음에도 $A \leftarrow A + 1'b1$ 연산이 수행되는 것을 확인 할 수 있다. 이렇게 되면 resigster operation 이 state operation 과 다른 상태(초기값이 맞춰지지 않은 상태)에서 동작을 수행하기에 원하는 결과가 나오지 않을 수 있다. (Ex. Register 의 조건이 next state 를 결정하는 디자인)

VWF (Timing Sequence 확인)



Input		Main input	Counter	FF		Conditions	pstate	nstate	Operations
CLK	Clrn	S	A[3:0]	E	F				
↑	1	0	0000	0	0	$A_3 = 0$ $A_4 = 0$	T_0	T_0	
	↓	0	0000	0	0	$A_3 = 0$ $A_4 = 0$	T_0	T_0	Asynchronous reset
↑	0	0	0000	0	0	$A_3 = 0$ $A_4 = 0$	T_0	T_0	$pstate <= T_0$
	1	1	0000	0	0	$A_3 = 0$ $A_4 = 0$	T_0	T_1	
↑	1	1	0000	0	0	$A_3 = 0$ $A_4 = 0$	T_1	T_1	$T_0 \rightarrow T_1$ $A \leftarrow 4'b0000$ $F \leftarrow 1'b0$
↑	1	1	0001	0	0	$A_3 = 0$ $A_4 = 0$	T_1	T_1	$A \leftarrow A + 4'b0001$ $E \leftarrow 1'b0$
↑	1	0	0010	0	0	$A_3 = 0$ $A_4 = 0$	T_1	T_1	$A \leftarrow A + 4'b0001$ $E \leftarrow 1'b0$
↑	1	0	0011	0	0	$A_3 = 0$ $A_4 = 0$	T_1	T_1	$A \leftarrow A + 4'b0001$ $E \leftarrow 1'b0$
↑	1	1	0100	0	0	$A_3 = 1$ $A_4 = 0$	T_1	T_1	$A \leftarrow A + 4'b0001$ $E \leftarrow 1'b0$
↑	1	1	0101	1	0	$A_3 = 1$ $A_4 = 0$	T_1	T_1	$A \leftarrow A + 4'b0001$ $E \leftarrow 1'b1$
↑	1	0	0110	1	0	$A_3 = 1$ $A_4 = 0$	T_1	T_1	$A \leftarrow A + 4'b0001$ $E \leftarrow 1'b1$
↑	1	0	0111	1	0	$A_3 = 1$ $A_4 = 0$	T_1	T_1	$A \leftarrow A + 4'b0001$ $E \leftarrow 1'b1$
↑	1	1	1000	1	0	$A_3 = 0$ $A_4 = 1$	T_1	T_1	$A \leftarrow A + 4'b0001$ $E \leftarrow 1'b1$
↑	1	1	1001	0	0	$A_3 = 0$ $A_4 = 1$	T_1	T_1	$A \leftarrow A + 4'b0001$ $E \leftarrow 1'b0$
↑	1	0	1010	0	0	$A_3 = 0$ $A_4 = 1$	T_1	T_1	$A \leftarrow A + 4'b0001$ $E \leftarrow 1'b0$
↑	1	0	1011	0	0	$A_3 = 0$ $A_4 = 1$	T_1	T_1	$A \leftarrow A + 4'b0001$ $E \leftarrow 1'b0$
↑	1	1	1100	0	0	$A_3 = 1$ $A_4 = 1$	T_1	T_2	$A \leftarrow A + 4'b0001$ $E \leftarrow 1'b0$

↑	1	1	1101	1	0	$A_3 = 1$ $A_4 = 1$	T_2	T_0	$T_1 \rightarrow T_2$ $A \leftarrow A + 4'b0001$ $E \leftarrow 1'b1$
↑	1	0	1101	1	1	$A_3 = 1$ $A_4 = 1$	T_0	T_0	$T_2 \rightarrow T_0$ $F \leftarrow 1'b1$
↑	1	0	1101	1	1	$A_3 = 1$ $A_4 = 1$	T_0	T_0	
	1	1	1101	1	1	$A_3 = 1$ $A_4 = 1$	T_0	T_1	
↑	1	1	0000	1	0	$A_3 = 0$ $A_4 = 0$	T_1	T_1	$T_0 \rightarrow T_1$ $A \leftarrow 4'b0000$ $F \leftarrow 1'b0$
↑	1	1	0001	0	0	$A_3 = 0$ $A_4 = 0$	T_1	T_1	$A \leftarrow A + 4'b0001$ $E \leftarrow 1'b0$
↑	1	0	0010	0	0	$A_3 = 0$ $A_4 = 0$	T_1	T_1	$A \leftarrow A + 4'b0001$ $E \leftarrow 1'b0$
↑	1	0	0011	0	0	$A_3 = 0$ $A_4 = 0$	T_1	T_1	$A \leftarrow A + 4'b0001$ $E \leftarrow 1'b0$
↑	1	1	0100	0	0	$A_3 = 1$ $A_4 = 0$	T_1	T_1	$A \leftarrow A + 4'b0001$ $E \leftarrow 1'b0$
↑	1	1	0101	1	0	$A_3 = 1$ $A_4 = 0$	T_1	T_1	$A \leftarrow A + 4'b0001$ $E \leftarrow 1'b1$
	↓	0	0101	0	0	$A_3 = 1$ $A_4 = 0$	T_0	T_1	Asynchronous reset
↑	0	0	0101	0	0	$A_3 = 1$ $A_4 = 0$	T_0	T_1	$pstate <= T_0$
↑	0	0	0101	0	0	$A_3 = 1$ $A_4 = 0$	T_0	T_1	$pstate <= T_0$
	1	1	0101	0	0	$A_3 = 0$ $A_4 = 0$	T_0	T_1	
↑	1	1	0000	0	0	$A_3 = 0$ $A_4 = 0$	T_1	T_1	$T_0 \rightarrow T_1$ $A \leftarrow 4'b0000$ $F \leftarrow 1'b0$
↑	1	1	0001	0	0	$A_3 = 0$ $A_4 = 0$	T_1	T_1	$A \leftarrow A + 4'b0001$ $E \leftarrow 1'b0$
↑	1	0	0010	0	0	$A_3 = 0$ $A_4 = 0$	T_1	T_1	$A \leftarrow A + 4'b0001$ $E \leftarrow 1'b0$
(이후 동작 같음)									