EE-584

INTRODUCTION TO VLSI DESIGN AND TESTING

PROJECT REPORT
ON
RING OSCILLATOR -- FANOUT 1

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Objective

The objective of this project is to design a ring oscillator with fanout of one that generates the frequency within the range of the oscilloscope (CRO, 100MHz).

1 Introduction

Ring Oscillator consists of odd number of inverters connected in series to form a closed loop with positive feedback. It is often used to measure the speed of a process. This project deals with designing a 71-stage ring oscillator with fanout of one at each stage. Fanout refers to the number of inputs that the output of a logic gate can drive. The number of stages is chosen in such a way that the frequency generated is within the range of the oscilloscope (CRO).

1.1 Block Diagram

The different blocks used in the project are shown in the figure 1

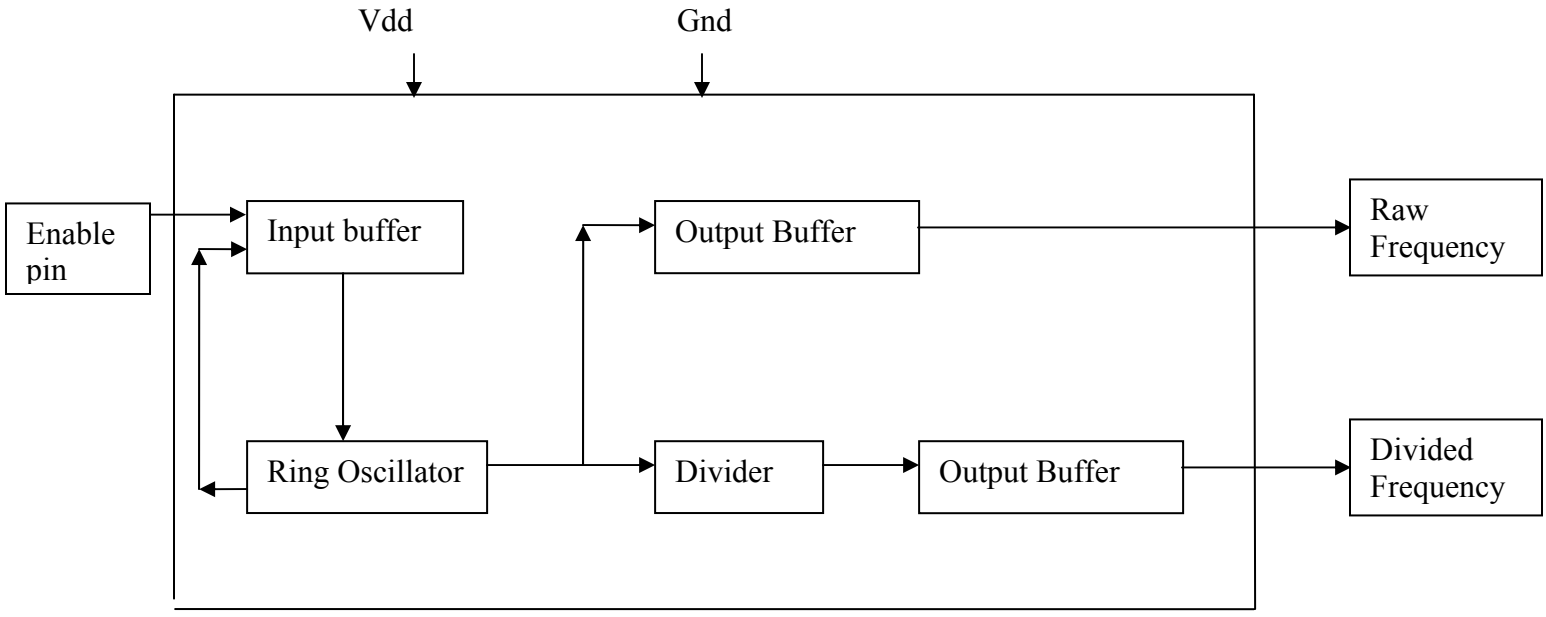

Figure1. Basic block diagram

A tristate buffer is used as the input buffer to reduce the imperfections in the input signal. It has two input pins: enable and the feedback from the ring oscillator. The enable pin is used to enable or disable the ring oscillator. A 71-stage ring oscillator is used to generate

a frequency of 27MHz. The output of the ring oscillator is given to the output buffer to drive the load (10Pf || 1MΩ). The generated frequency is divided using a 10-stage frequency divider circuit(D-Flipflop)

2 The Ring Oscillator

Initially a three stage ring oscillator circuit is used to estimate the frequency of oscillations. Figure 2 shows the basic 3-stage ring oscillator. The output at the third stage gets inverted as odd numbers of stages are used and this output is fedback to the first stage. Therefore the output of the third stage keeps on changing after each cycle and this results in oscillations. Each inverter has intrinsic propagation delay and the output appears after finite time period.

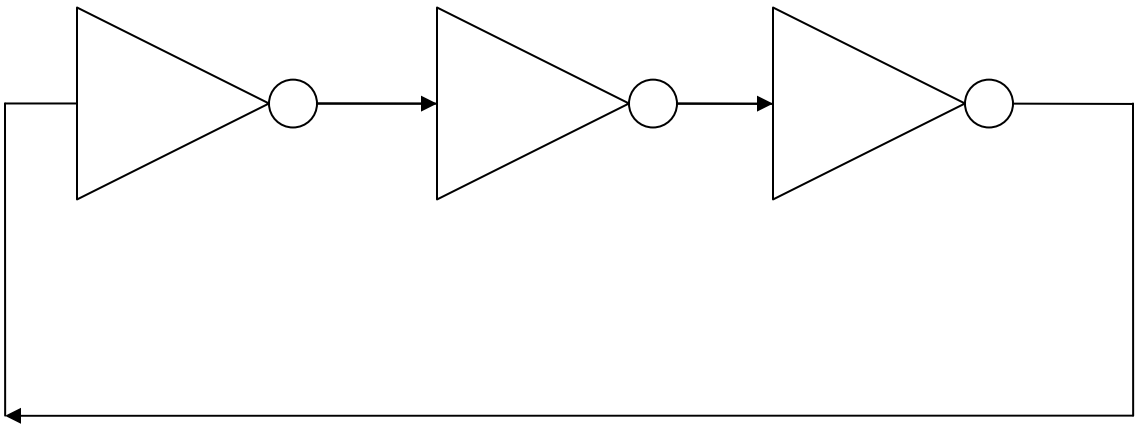

Figure2: 3 stage ring oscillator

Based on the frequency of the 3-stage ring oscillator, the frequency for a single stage is calculated. 71-stages are considered so that the frequency is within the range of the CRO even in the worst case of the process variations.

2.1 3-stage inverter schematic

The schematic for a 3 stage ring oscillator is shown in figure 3. Minimum size Pmos and Nmos are used for the inverter and the width of the Pmos is twice the width of Nmos(Wp/Wn=2.1/1.05).

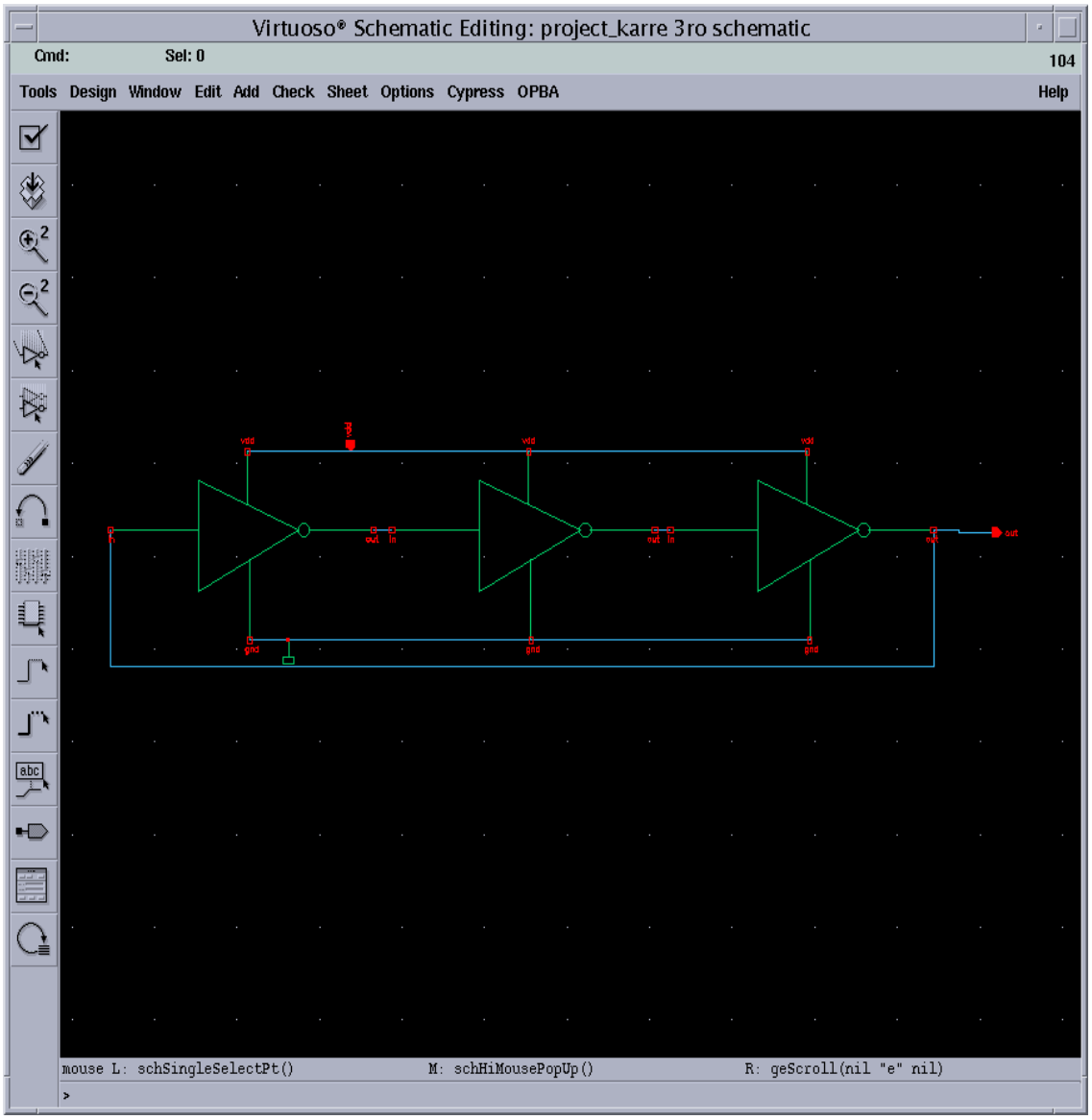

Figure3. Schematic of 3 stage ring oscillator

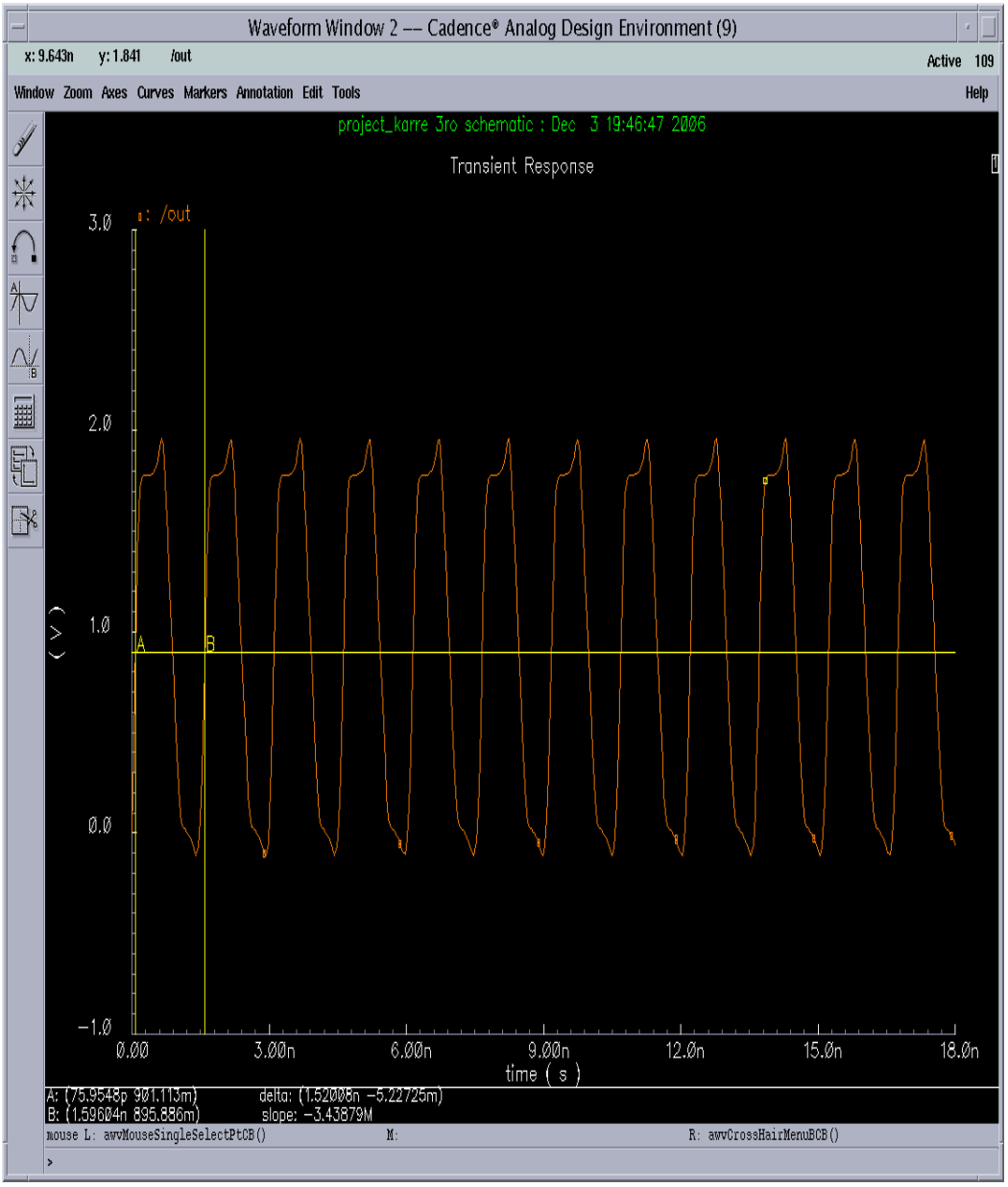

Figure4. Output of 3 stage ring oscillator

The schematic of the 3-stage ring oscillator is simulated and the figure 4 shows the simulation result. The time period is found to be 1.52ns. Therefore the time period of a single stage ring oscillator is 1.52n/3=0.506ns.The minimum number of stages was found to be 20 to generate a frequency less than 100MHz. But considering various factors such as the minimum size inverter and the load of an oscilloscope , the number of stages were chosen as 71.

2.2 Ring Oscillator Schematic

The schematic for 71-stage ring oscillator is as shown in the figure 5. Inverters are connected in series and the output of the last stage is fed back as input to the first stage. The size of each inverter is 2.1/1.05.

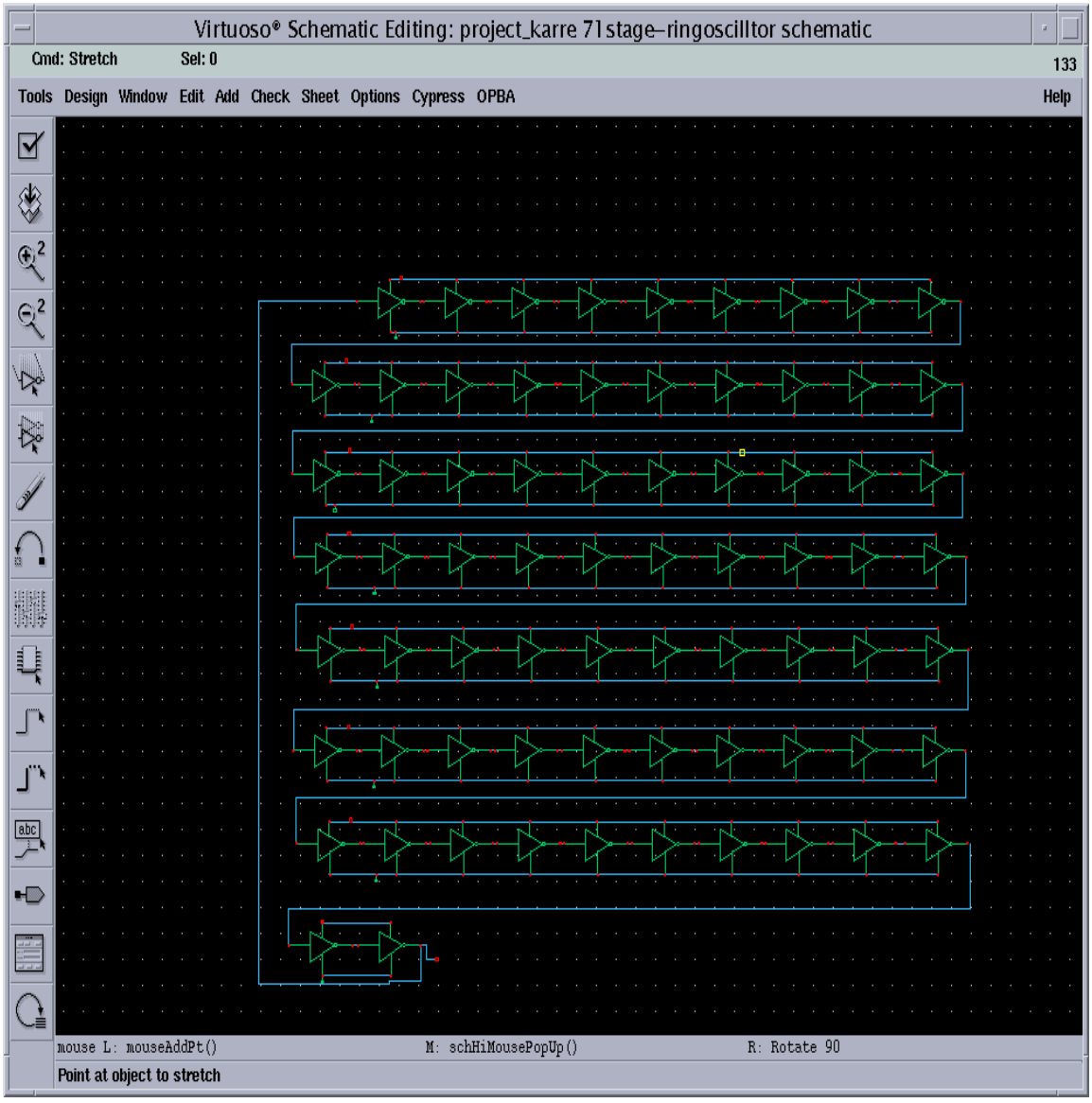

Figure5. Schematic of 71-stgae ring oscillator

2.3 Ring oscillator Layout

The inverters in the 71-stage ring oscillator are connected in a serpentine manner such that the routing is easier and the area of the layout is minimized. The interconnection routing between the input and output of the successive stages of the RO inverters have been done using PYL1 and L1M1 contact. Common VDD pin is used to connect the sources of the all the pmos and common GND pin is used to connect the source of all the nmos. Figure 6 shows the layout for 71-stage ring oscillator.

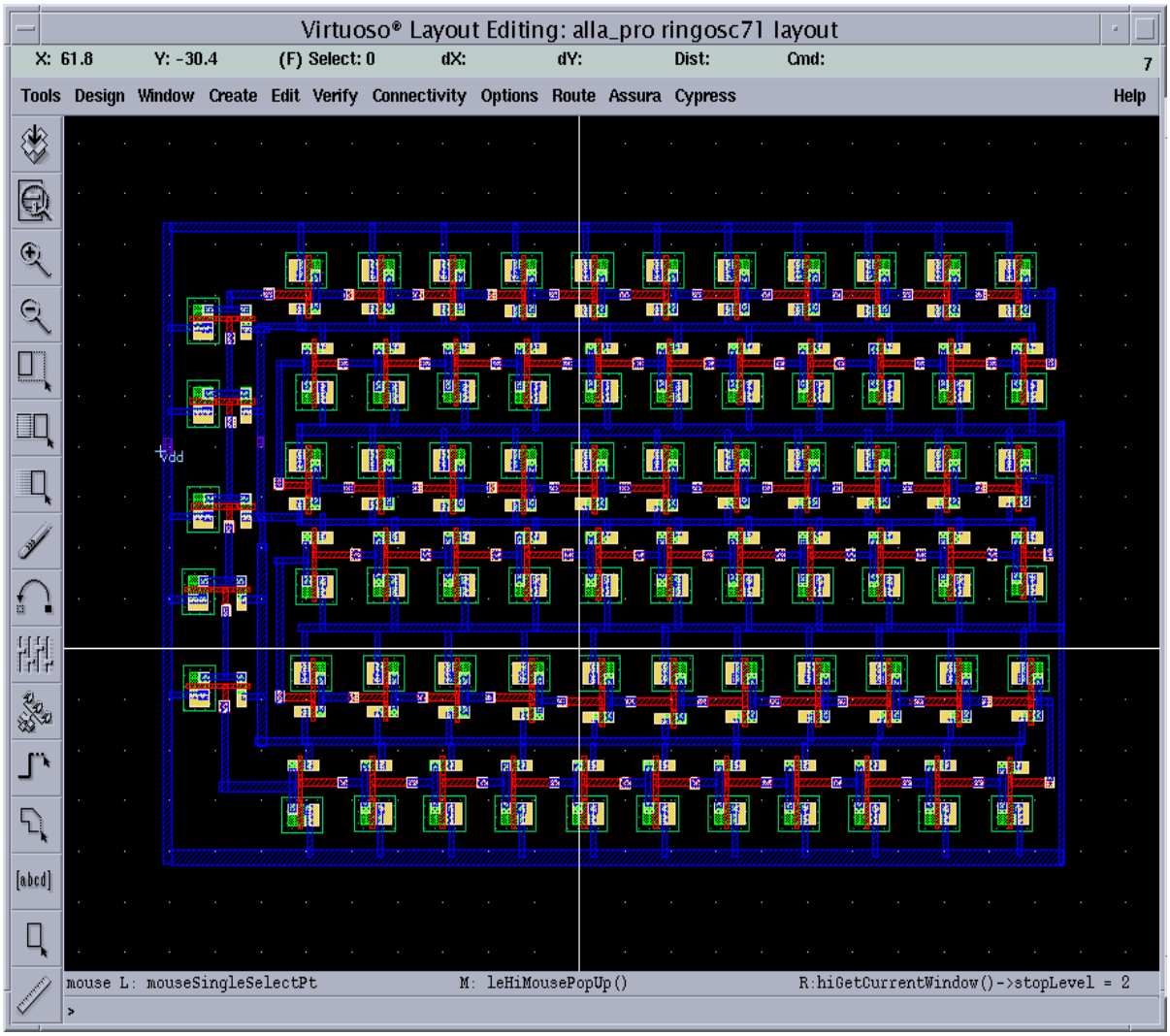

Figure6. Layout of 71- stage ring oscillator

2.4 Simulation results for 71-stage ring oscillator

The waveform generated for 71-stage ring oscillator is as shown in the figure 7. The period of the waveform generated is ~37ns. Therefore the frequency generated is approximately 27MHz. During the simulation, the initial condition for the ring oscillator is set to zero in order to generate oscillations. Spikes can be seen in the waveform at the instances where output changes its state. This is because when the input voltage changes sharply, the capacitance at input of the inverter opposes sudden change in the output. By introducing a load capacitor at the output of the oscillator these glitches can be reduced.

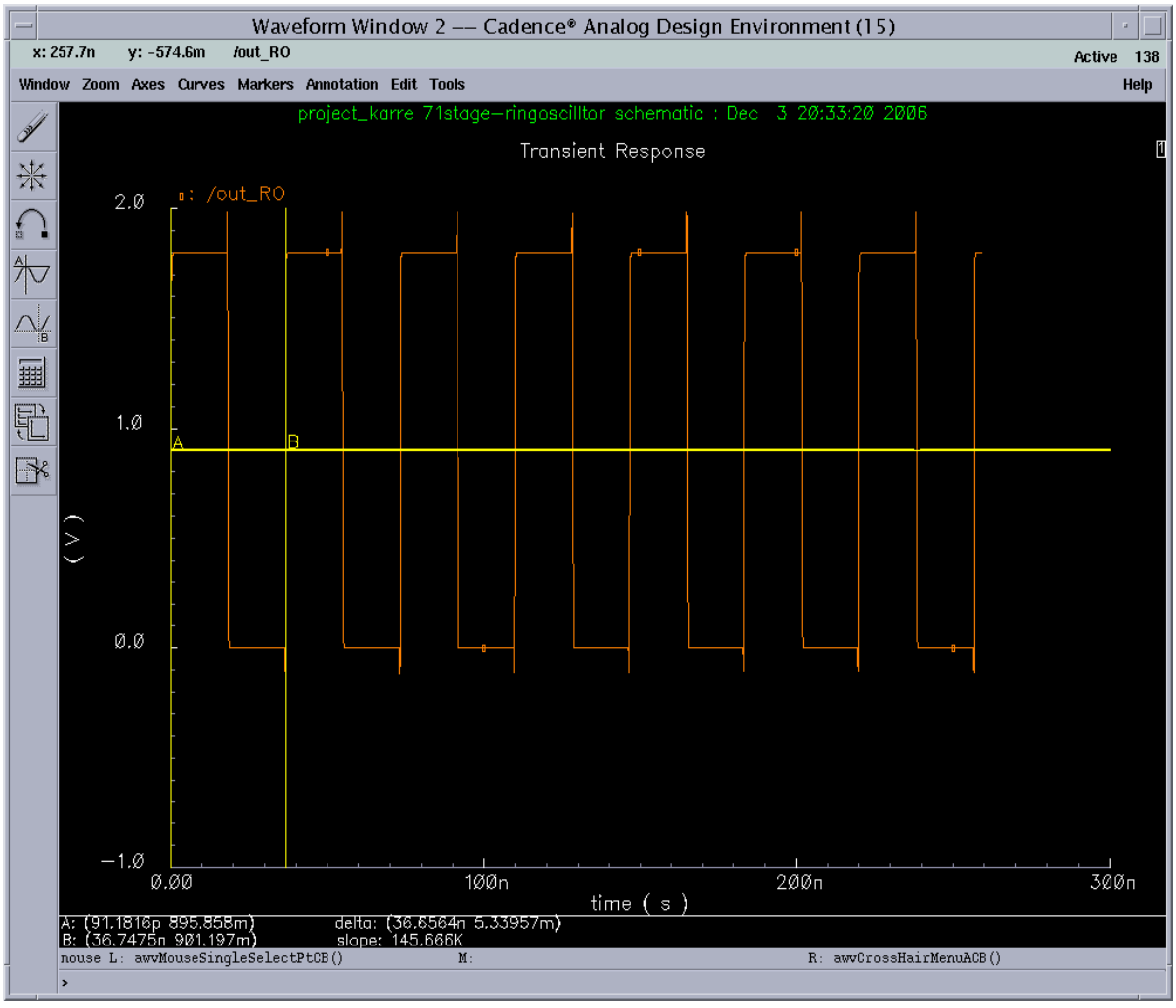

Figure7. Output of 71- stage ring oscillator

3 Input Buffer[1]

The input buffer is used to improve the signal strength. This buffer is placed in between the enable input and the ring oscillator. A tri-state buffer is preferred over other buffers as only one switch is in series with vdd or ground.It consists of a nand gate and nor gate followed by an inverter (when enable is high). When the enable is low, the output goes into the high impedance state and when the enable is high; the input signal strength is improved and is passed to the output. Figure 8 shows the schematic of the tri-state buffer.

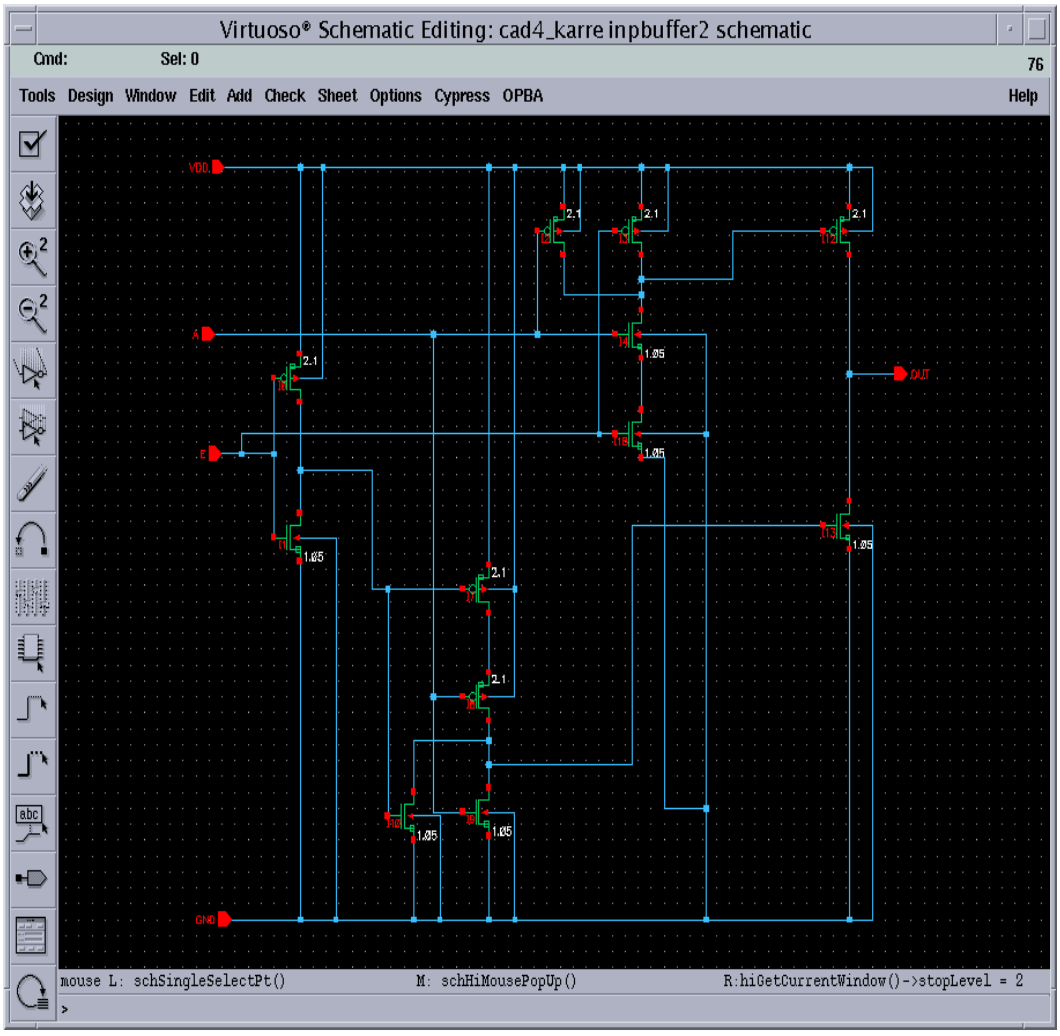

Figure8: Schematic of input buffer

The layout of the input buffer is as shown in the figure 9

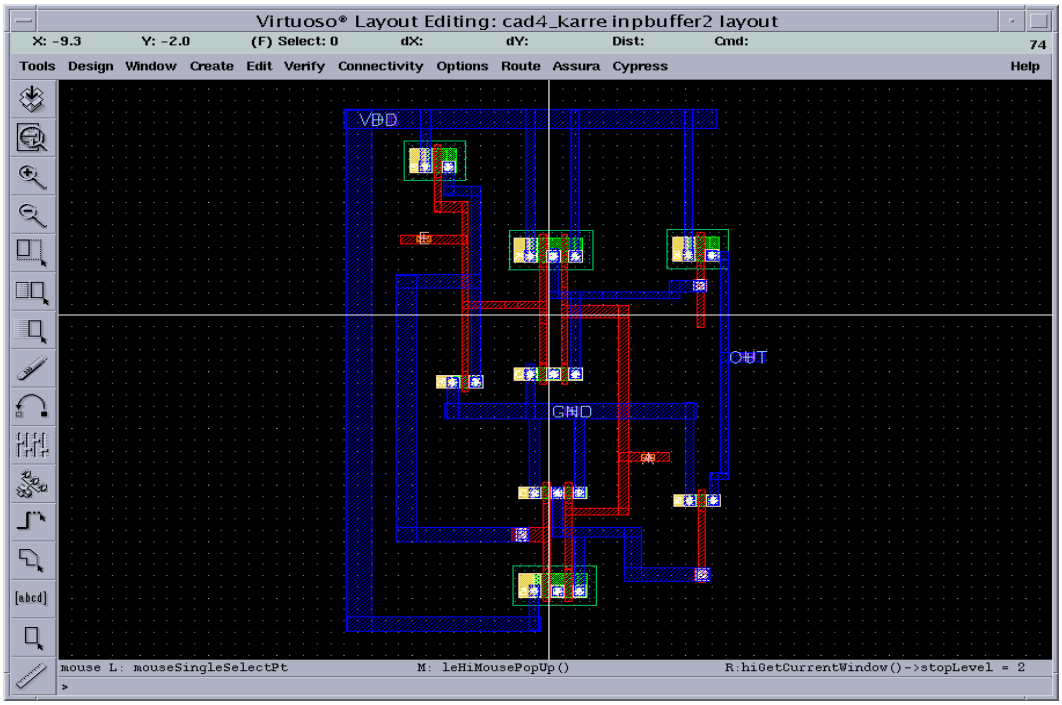

Figure9: Layout of input buffer

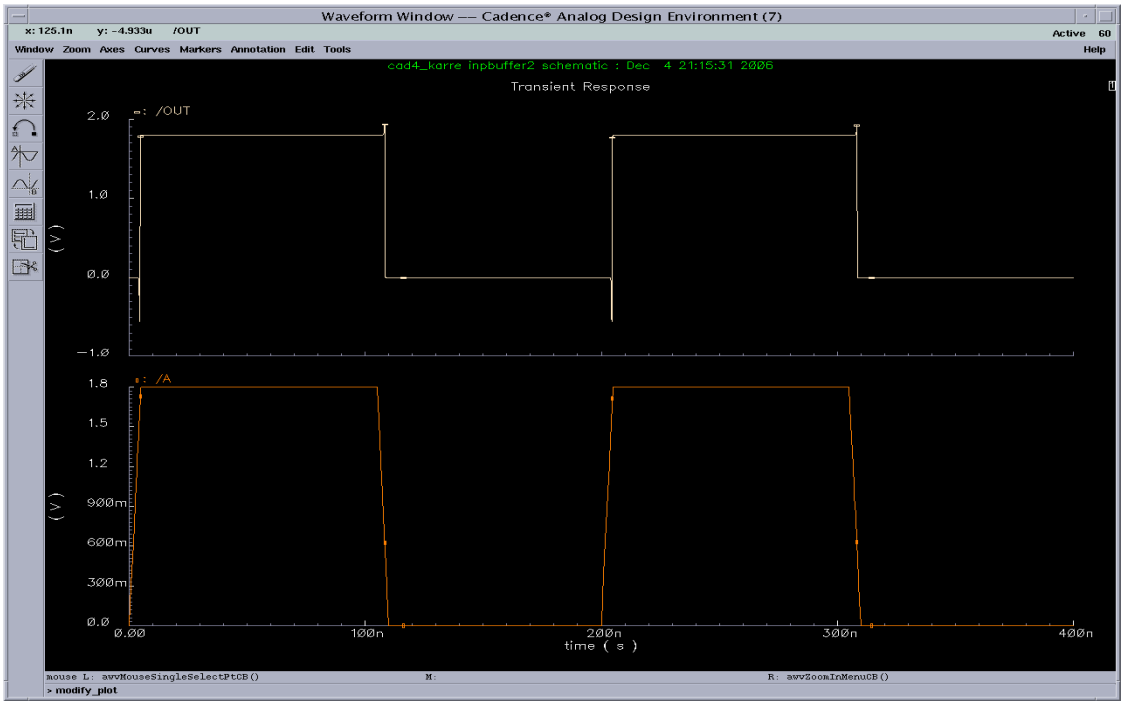

Figure10: Output of input buffer

As shown in the simulated wavform of input buffer(figure 13) the rise and fall times of the input signal are reduced thereby improving the signal.

4 Output buffer

The output buffer consists of a number of inverters connected in series to drive large load. This is connected in between the on-chip logic and the I/O pads.

The size of each inverter is larger than the previous inverter by a factor A (width of each inverter is multiplied by A).

4.1 Calculation of A and N [1]

To determine the values of *A* and N, the input capacitance is determined first. The inverter is connected to a large capacitive load (10pf) which makes the internal capacitances negligible. From the simulated result the values of t_{plh} and t_{phl} are computed.

t_{plh}=759.56ns and t_{phl}=373.5ns

Using these delay times and the load capacitance, the resistances R_p and R_n are calculated using the relations, $t_{phl}=0.7*R_p*C_{load}$ and $t_{plh}=0.7R_n*C_{load}$

Rp=54k, Rn=108k

The capacitive load is then removed and the propagation delays (t_{plh1} and t_{phl1}) are calculated again from the simulated result.

$t_{plh'}$=271.93p and $t_{phl'}$=501.14p

Using the values,(R_p,R_n,$t_{phl'}$,$t_{plh'}$),the value of the C_{out} is computed.

$C_{out}=0.7(Rp+Rn)*C_{load}$

$C_{in}=(3/2)*C_{out}$

C_{in}=10.22Ff

Using C_{in} N IS calculated as $N=\ln(C_{load}/C_{in})$

N=6.7

A is determined as $A=(C_{load}/C_{in})^{\wedge}{}_{(1/N)}$

A=2.73~3

4.2 Trade off considered

Making N smaller makes the stages to have large W/L values, this also increases the input capacitance and thus increases the delay. The value of N was obtained as 6.7 and the circuit has been implemented using 6 stages

4.3 6-stage output buffer

Considering the minimum size of the inverter, the size of the first stage of the buffer is taken as 2.1/1.05.The successive stages are multiplied by the factor (A~3). Therefore the size of the inverters' used are (2.1/1.05),(6.3/3.15),(18.9/9.45),(56.7/28.35),(170.1/85.5),(510.3,256.5). The schematic, layout and simulation are shown n the figure 11, 12 and 13 respectively.

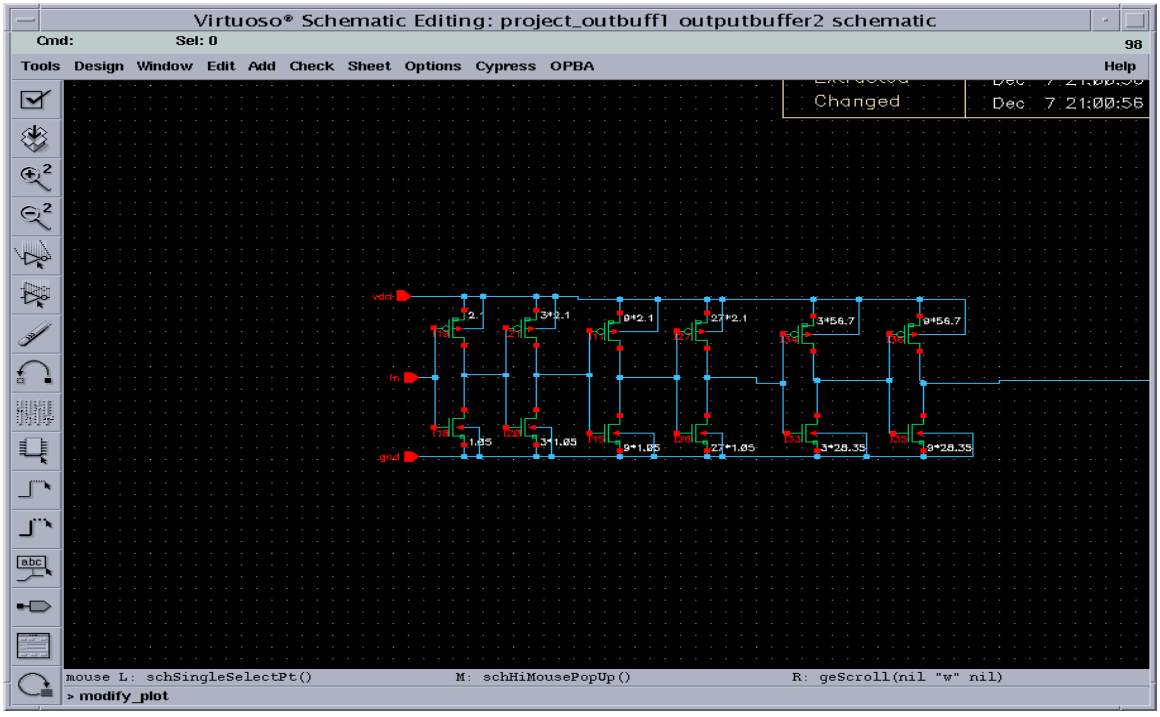

Figure11: Schematic of 6-stage output buffer

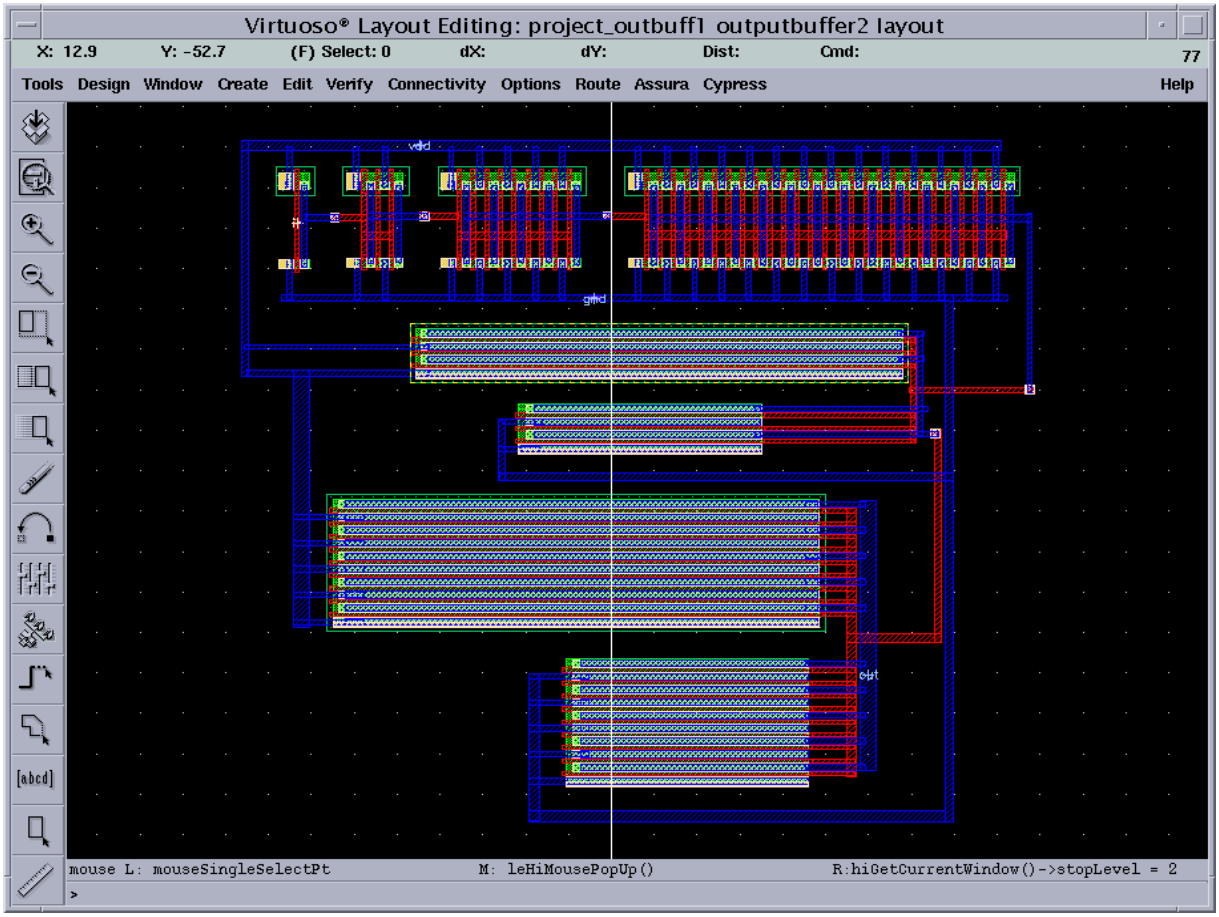

Figure12:layout of 6-stage output buffer

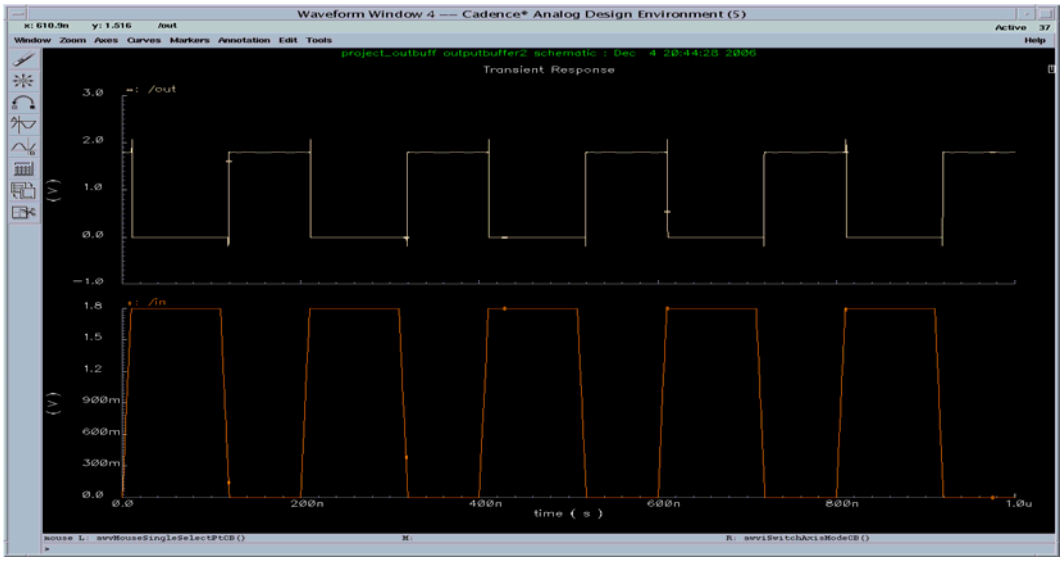

Figure13:output of 6-stage output buffer

5 Divider circuit

An edge-triggered D flip-flop is used to divide the frequency of the ring oscillator. It consists of two level sensitive latches in cascade. The first stage represents the master latch and the second stage represents the slave latch. When the clock is low, first stage tracks the D input and the second stage holds the previous output. When the clock goes high, the first stage captures the input and transfers it to the second stage. The schematic for a 10-stage divider circuit is shown in figure 14. As shown in the figure, all the dividers are connected in series and the output of the final stage divider gives the divided frequency.

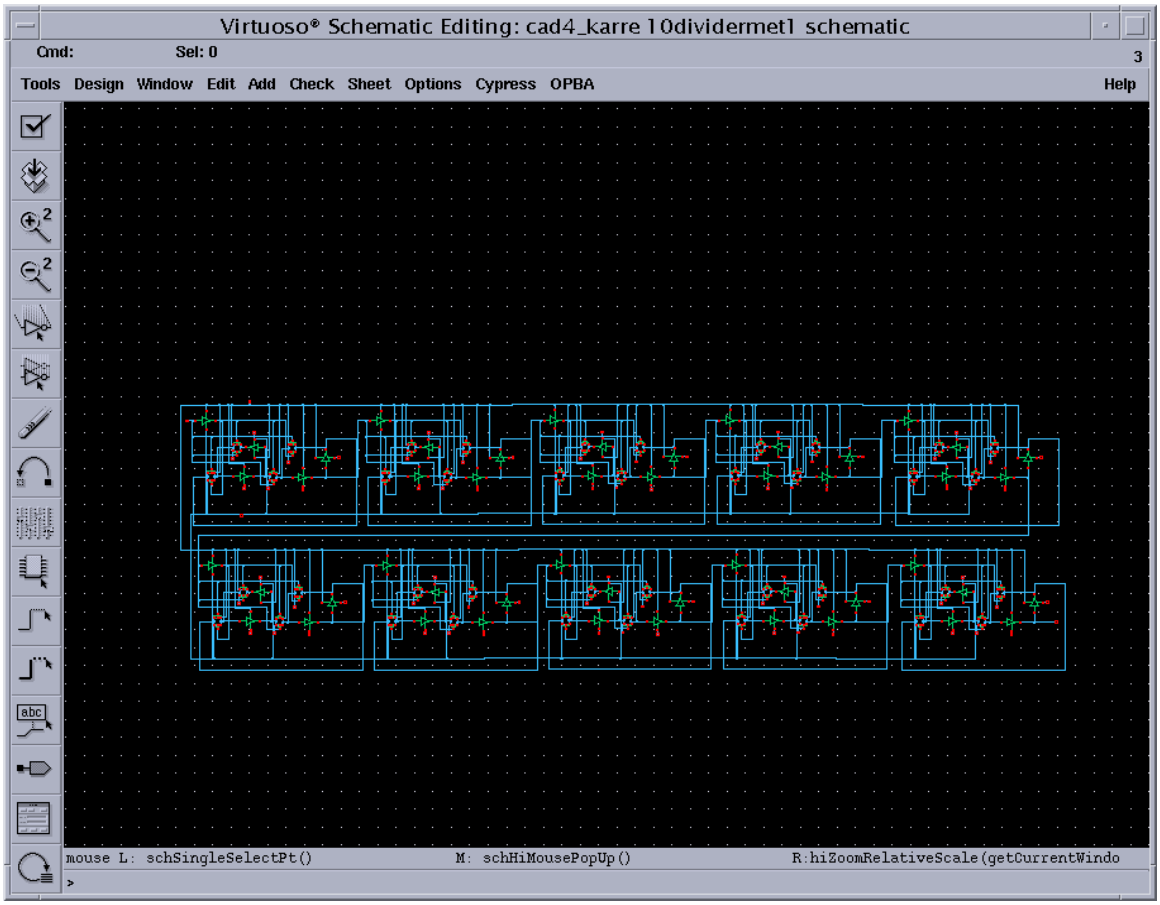

Figure14. Schematic of 10 stage frequency divider

5.1 Layout of 10 stage frequency divider

The figure 15 shows the layout of the 10-stage frequency divider. Metal1 is used to make all the connections. Separate ground pins are used to connect the tap of the nmos of the transmission gate.

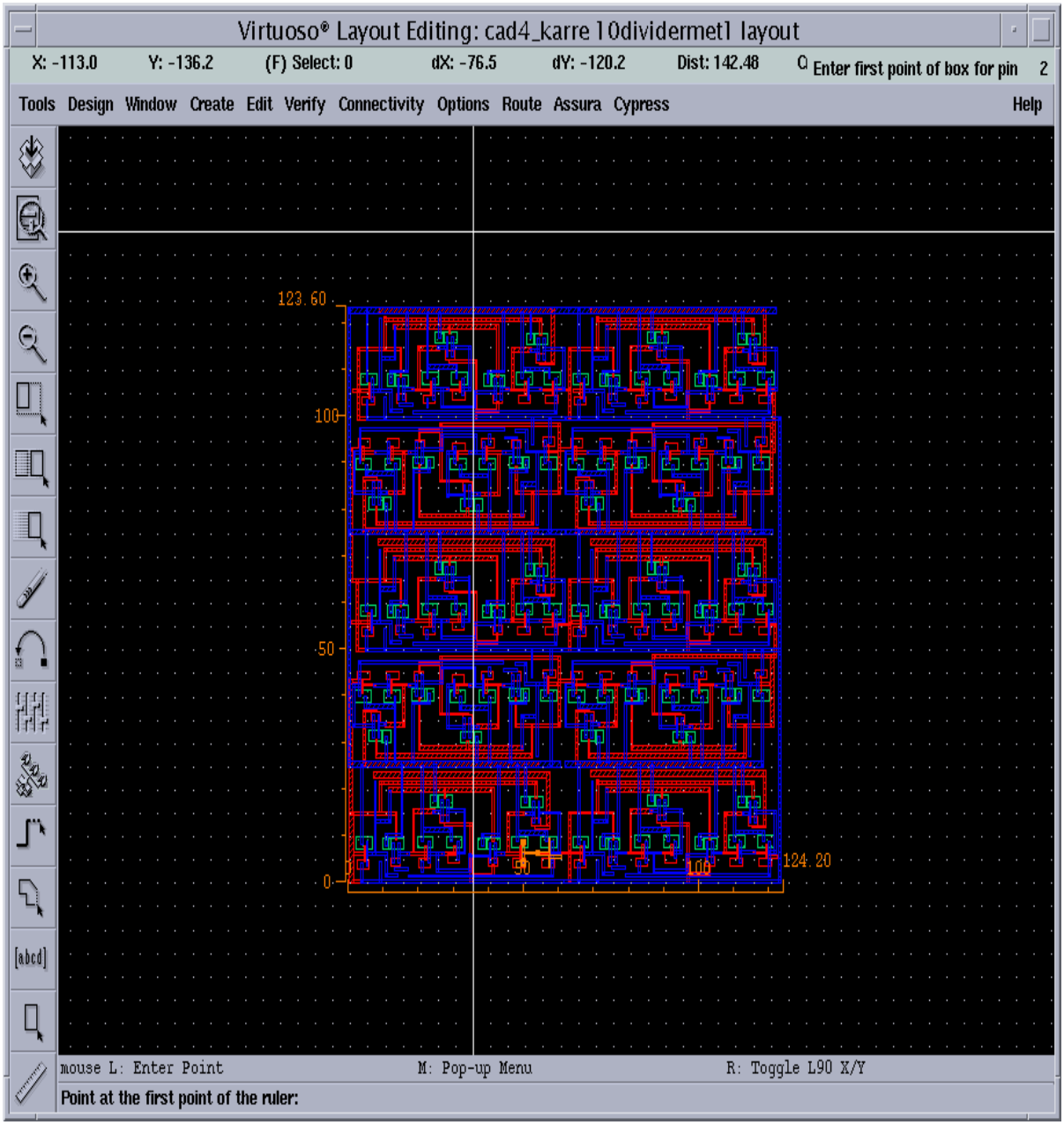

Figure15. Layout of 10 stage frequency divider

5.2 Simulation of 4-stage divider

In the output of 4 stage divider, the time period was increased by 16 and therefore the frequency was divided by 16 as shown in the figure.

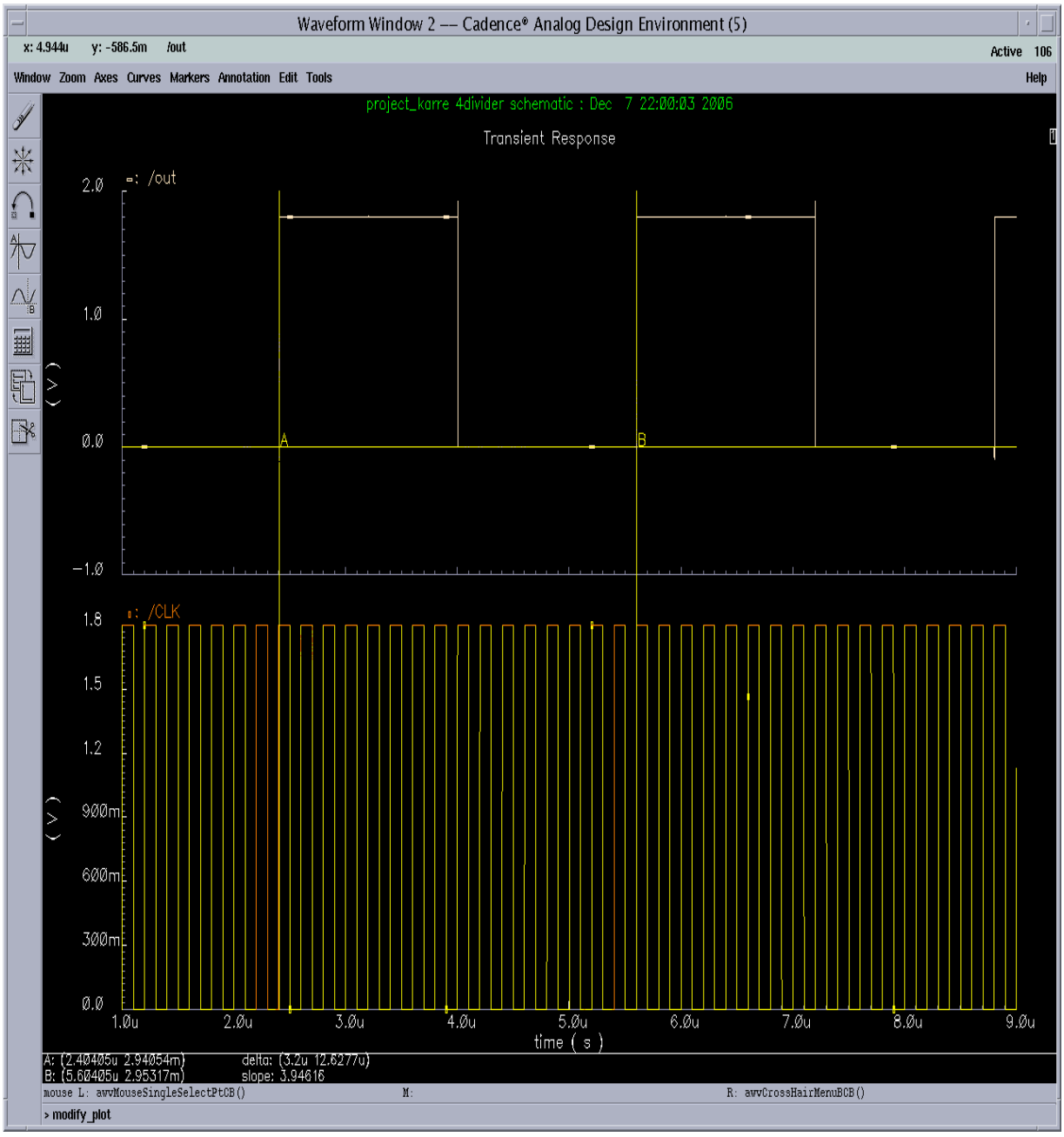

Figure16. Output of 1 stage frequency divider

6 Final circuit

Figure 17, 18 and 19 show the schematic, layout and output waveform of the entire circuit.

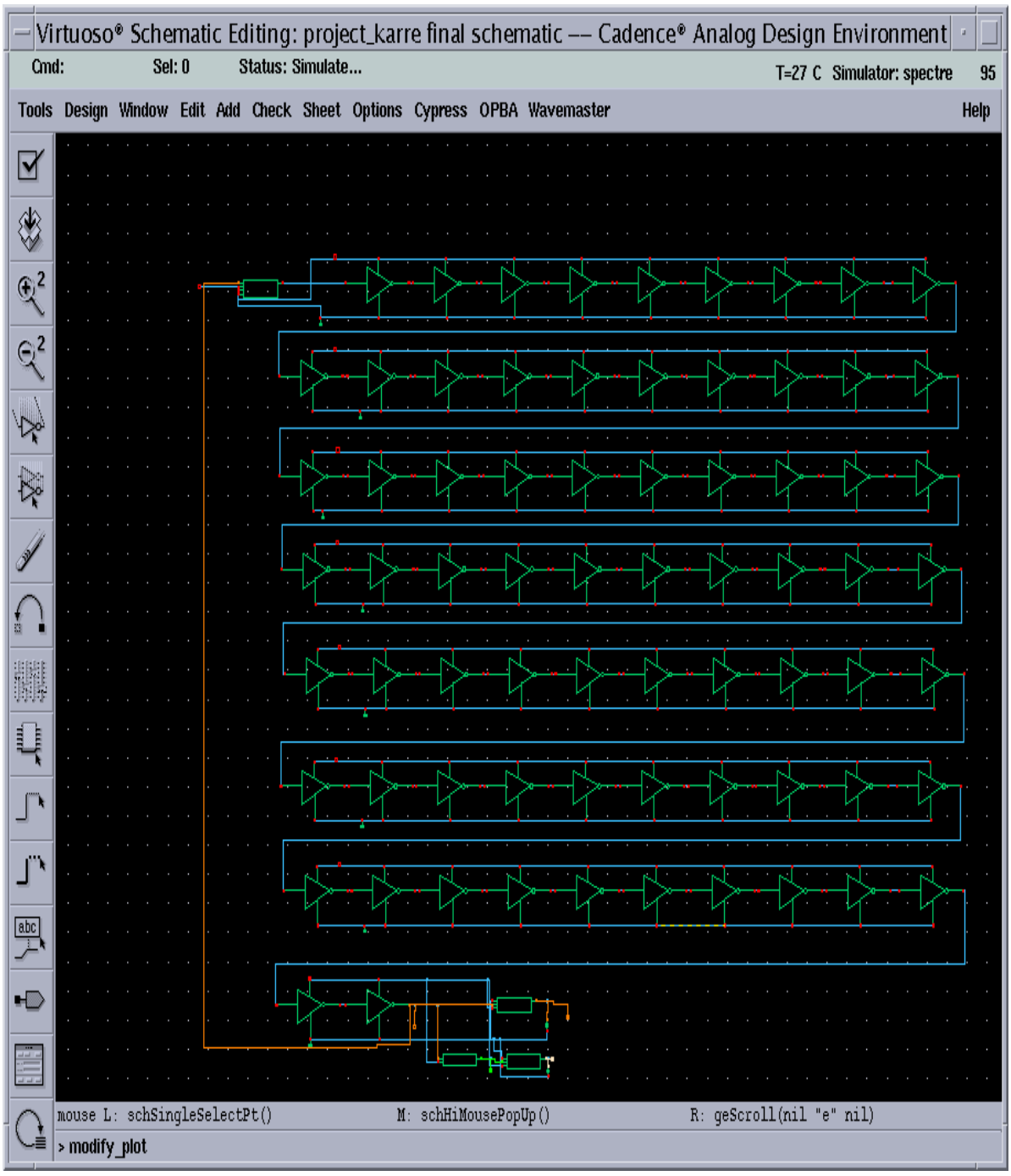

Figure 17: schematic of the total circuit

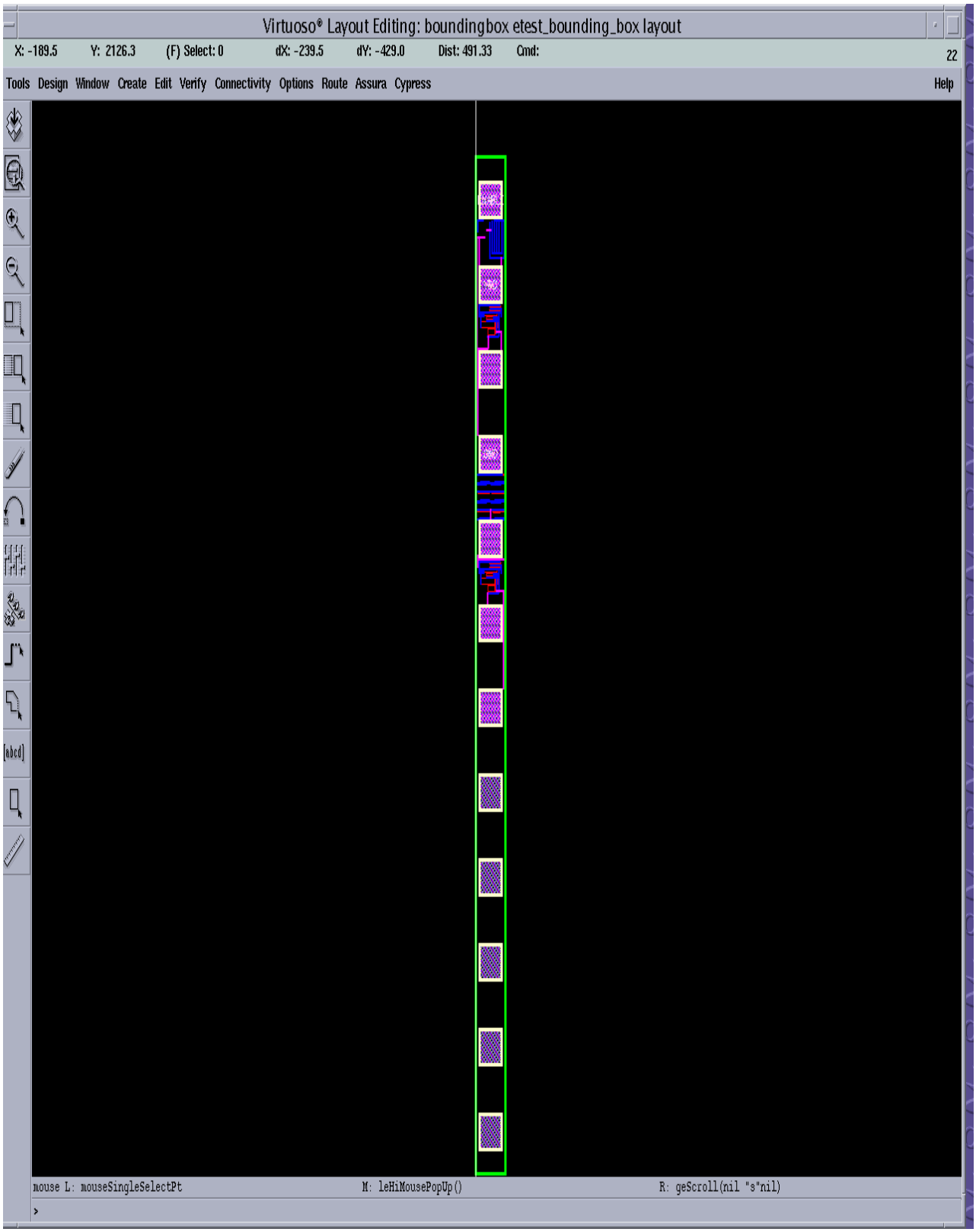

Figure 18: layout of the entire circuit inside the bounding box

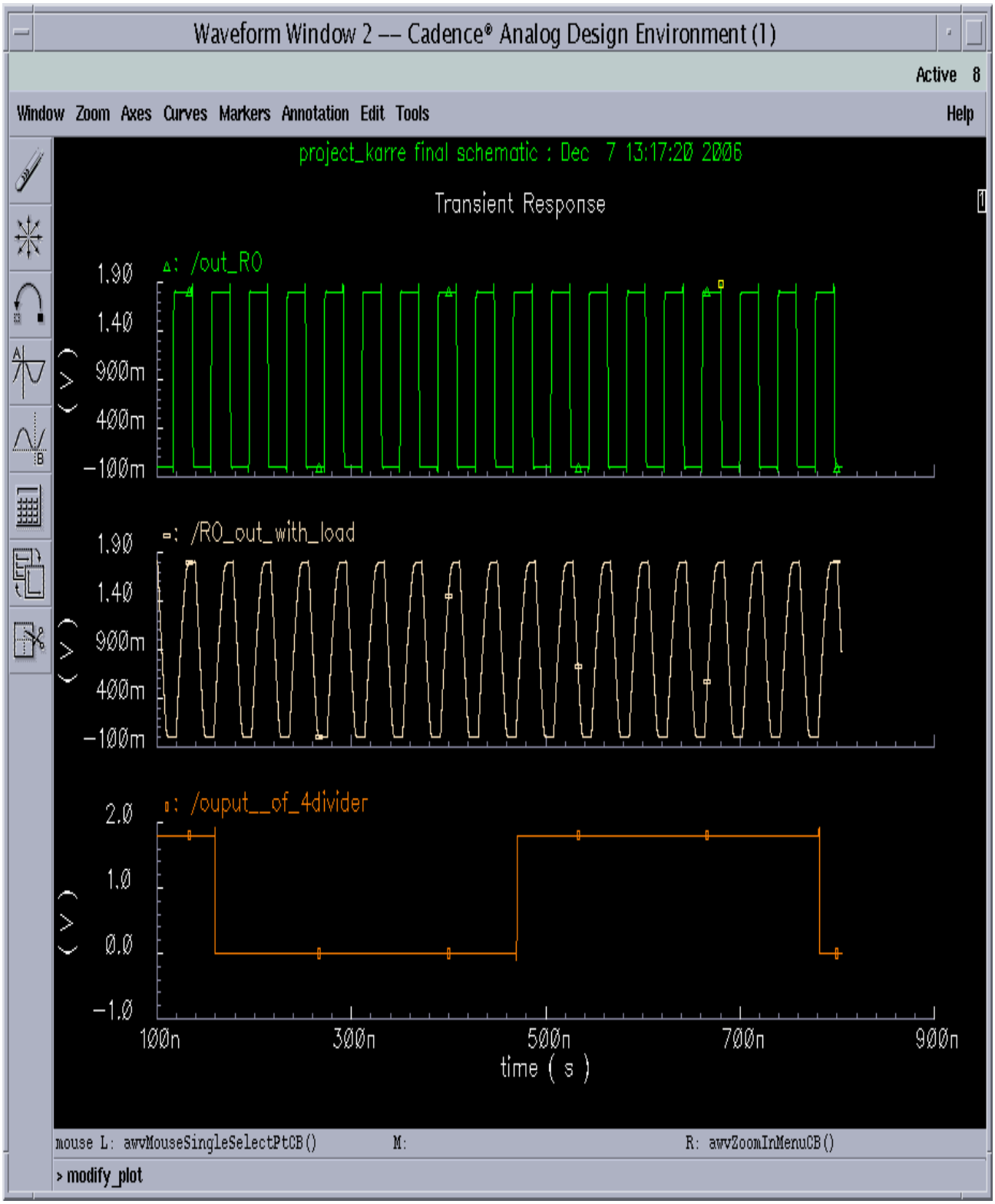

Figure19. Output of ring oscillator without load, with load and the divided output

7 Simulation at corner conditions

Corner simulations are done in five different conditions to observe the working and driving capabilities of ring oscillator. The five conditions are slow-slow, typi-typi, fast-fast, slow-fast and fast-slow. The variation in the frequency of the ring oscillator is observed by varying the VDD and the temperature.

7.1 Typical Condition

The schematic is first simulated for the typical condition. Figure 20 shows the simulation result of the ring oscillator with and without load at Vdd=1.8v and 27degree centigrade. Vout_ro is the output of ring oscillator and Vout_out_with_load is the output of the output buffer along with load. The markers are placed at the 50% of the input and output so that the difference gives the delay.

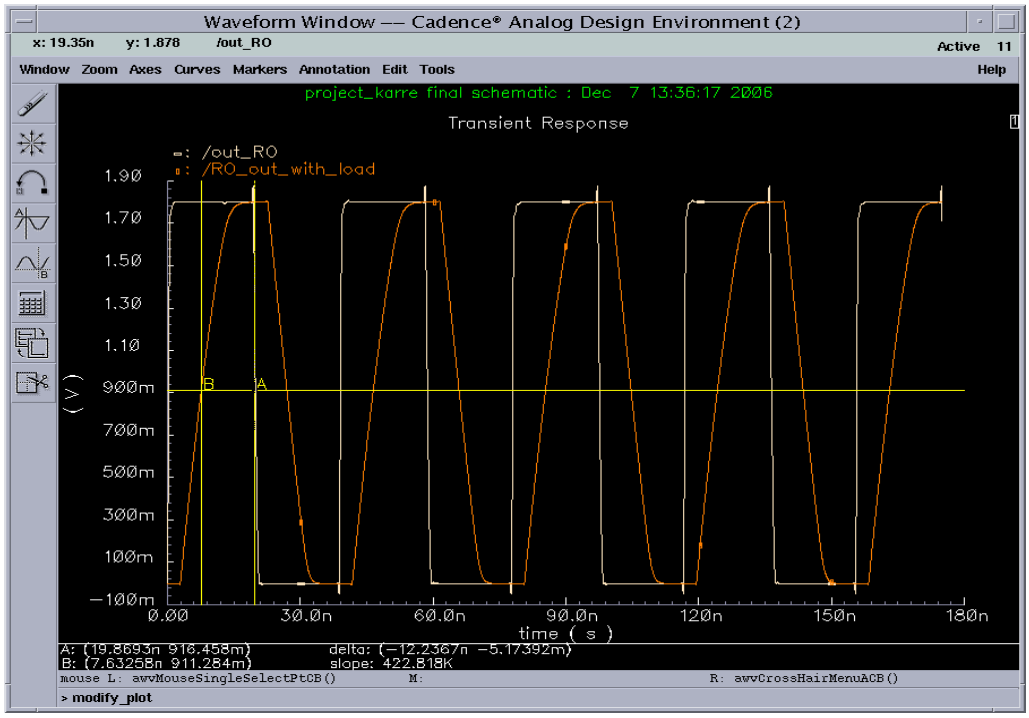

Figure20: Output of output buffer for typical corner

From the above simulated waveform,

t_{PLH} = 7.34ns,

t_{PHL}= 7.16ns

and the time period was found to be 38.81ns and the frequency was approximately 26MHz.

7.2 Fast Condition

The schematic is simulated for the fast condition and the simulation results are shown in the figure 21.

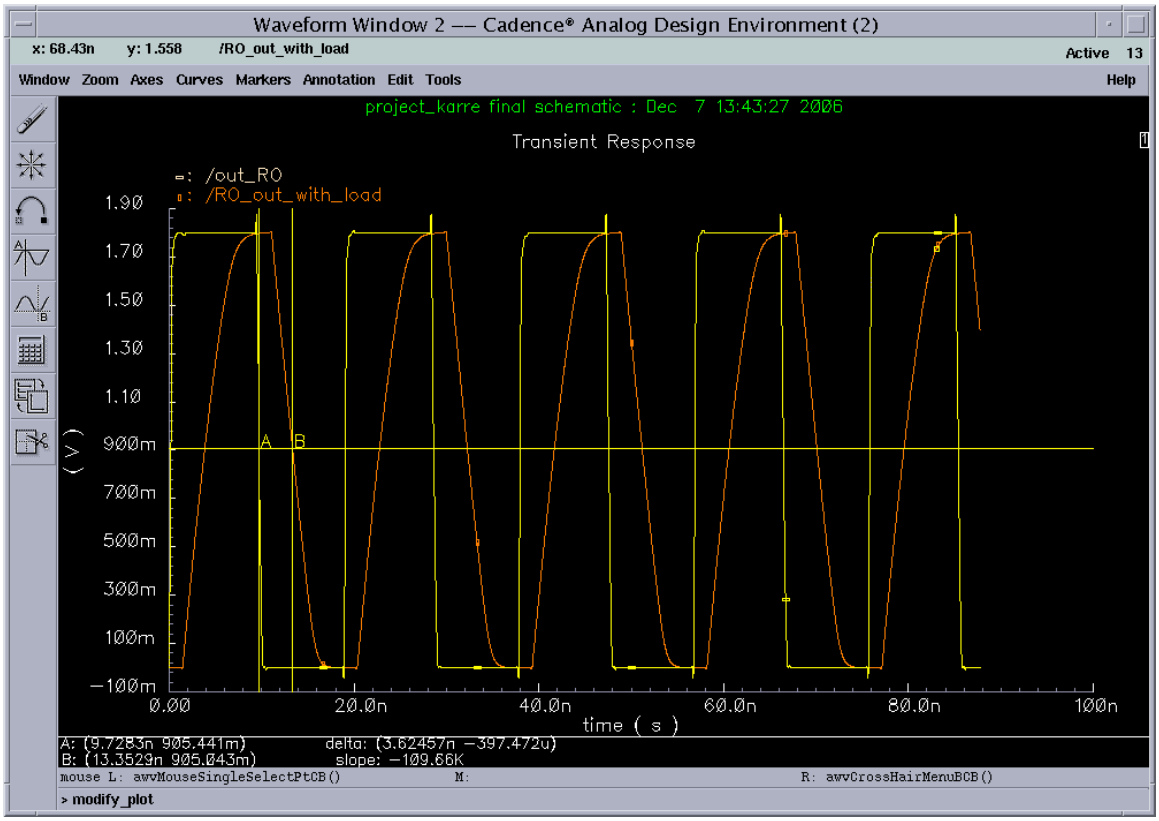

Figure21. Output of output buffer for fast corner

From the above waveform,

t_{PLH}=3.65ns,

t_{PHL}= 3.6ns

The t_{PHL} and t_{PLH} values were decreased to half compared to the typical condition values and so time period was also decreased to half and was found to be 18.64ns(frequency was approximately 54MHz). Therefore the fast corner simulation was approximately twice as fast as typical corner simulation.

7.3 Slow Condition

The schematic simulation results for the slow corner condition are as shown in the figure 22.

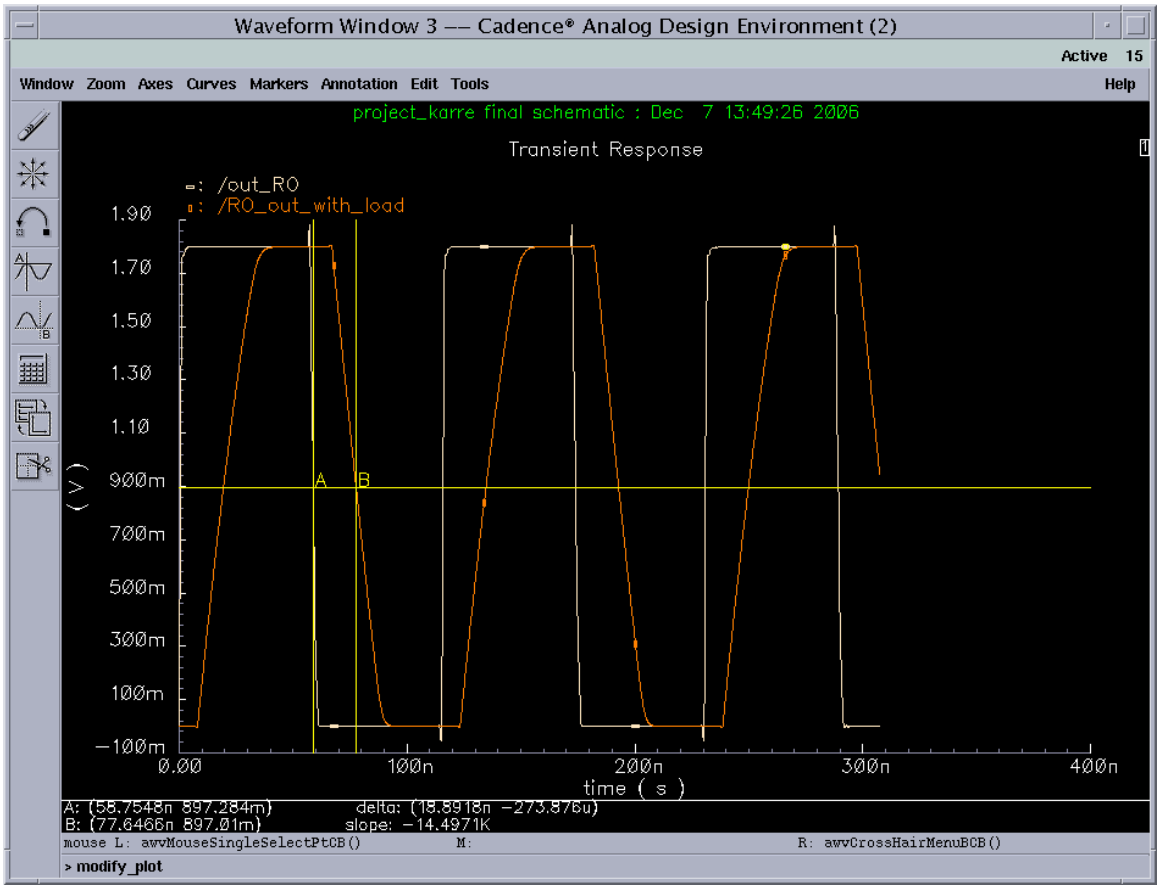

Figure22. Output of output buffer for slow corner

The t_{PLH} and t_{PHL} values were found to be 18.8ns and 18.89ns respectively and the time period was found to be 115.23ns (frequency= 8.6MHz). It was observed that the dealy and the time period were more than thrice the values in the typical case.

It was also noticed that in all the three corner conditions the output voltage was 1.8v and this shows the buffer was able to drive the load providing the drive current and the entire range of input voltage.

7.4 Fast-slow Condition

In the fast-slow condition, the Pmos is made faster and the Nmos is made slower. Due to this the switching time from the lower voltage level to the higher voltage levels is less and similarly the switching time from the higher to the lower voltage level is more. The schematic simulation results for fast-slow condition are shown in figure 23.

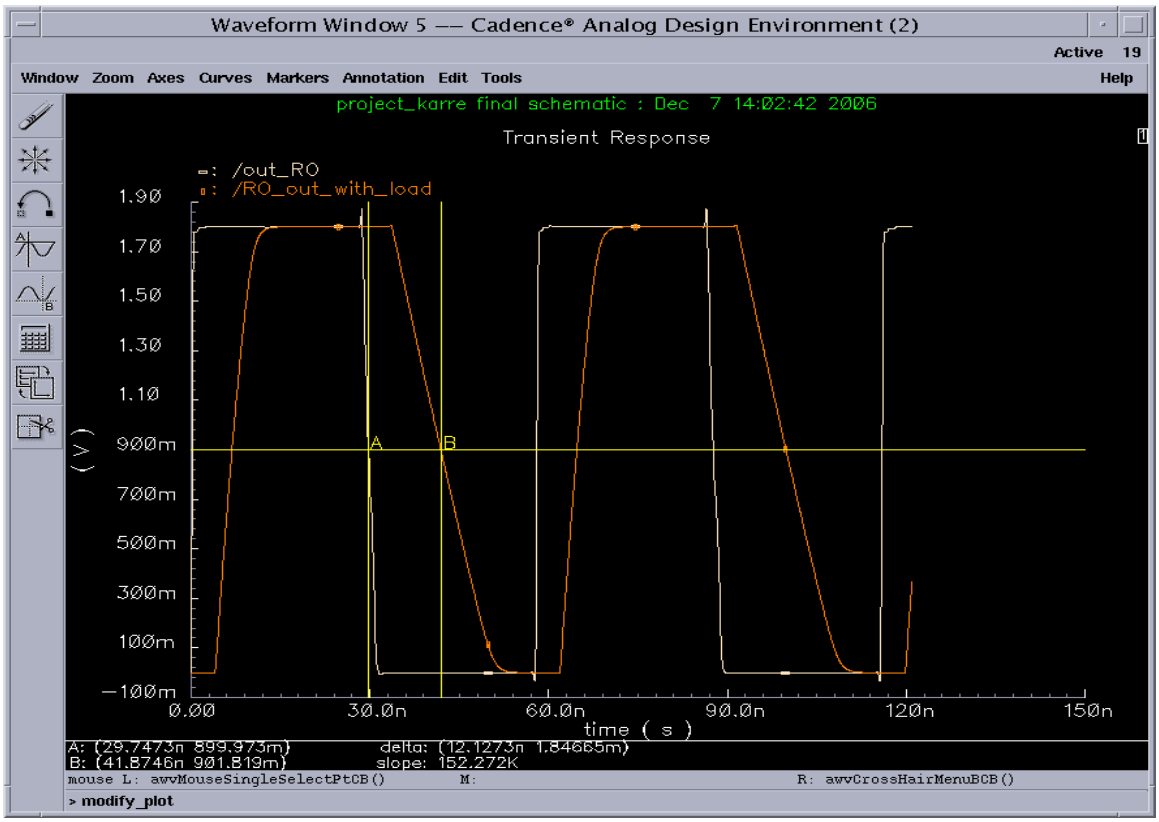

Figure23. Output of output buffer for fast-slow corner

From the above waveform the t_{PLH} and t_{PHL} values are found to be 7.62ns and 12.15ns and the period is 57.9ns(frequency=17.27MHz).

7.5 Slow-fast Condition

In this case, the Pmos is made slower when compared to the Nmos and due to this the switching time from the lower voltage level to the higher voltage level will be more when compared to the switching time from the higher voltage level to the lower voltage level. The schematic simulation results are shown in the figure 24.

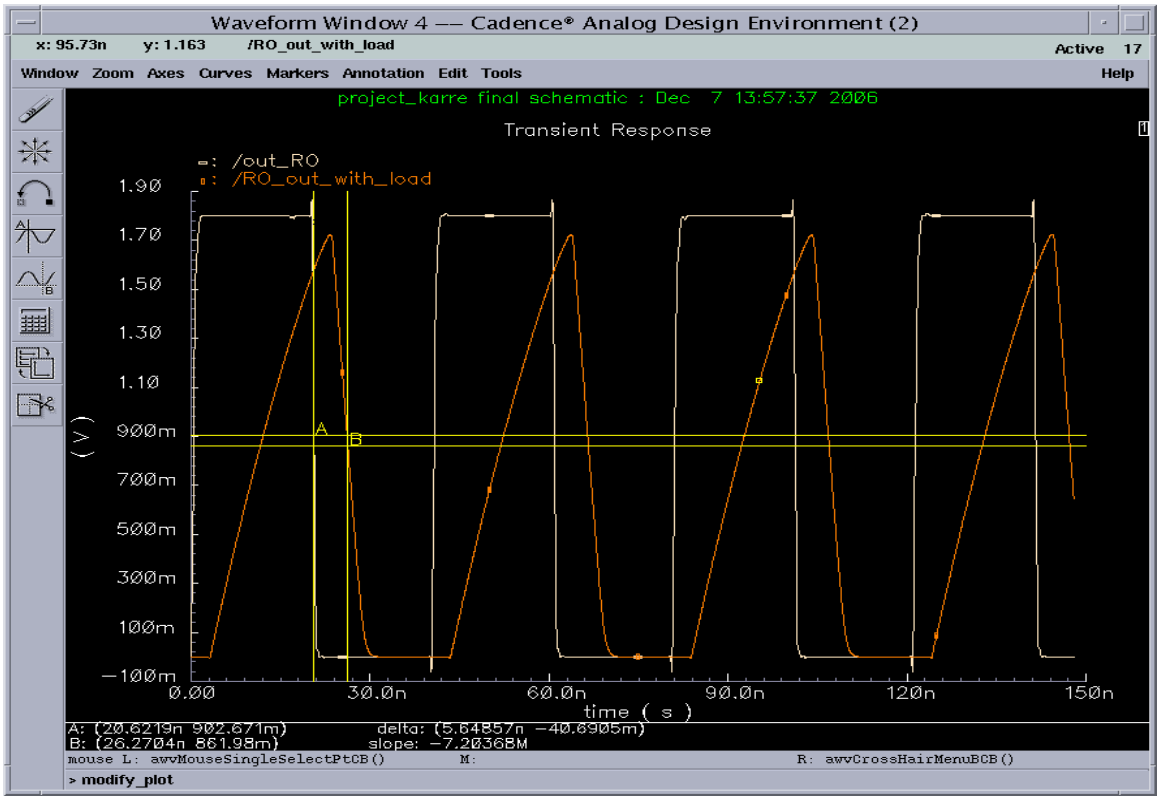

Figure24. Output of output buffer for slow-fast corner

The t_{PLH} and t_{PHL} and the time period values are found to be 11.23ns, 5.65ns and 40.31ns respectively.

8 Effect of temperature and voltage on frequency

The variations of time period with voltage and temperature for all the five corner conditions (typi-typi, fast-fast, slow-slow, fast-slow, slow-fast) are observed. The variations are graphically represented in the form a 3-D plot. The voltage was varied from ± 10% of Vdd i.e., from 1.62v to 1.98v and the temperature was varied from -40 to 150 degrees Celsius.

8.1 Typical Condition

The circuit is simulated under typical condition for different values of temperature and Vdd and the time period is noted. These results are tabulated in table 1 and the figure 23 shows the 3D-plot.

Table1. Typical corner

Vdd	Temperature (degree Celsius)					
	-40	0	27	65	100	150
	Time period (ns)					
1.62	178.04	107.03	83.21	62.58	50.82	40
1.7	98.59	68.47	56.55	45.46	38.65	31.95
1.8	55.64	43.85	38.81	32.73	29	25.08
1.9	37.09	31.09	28.12	25.03	22.86	20.45
1.98	28.34	24.72	22.91	20.9	19.43	17.74

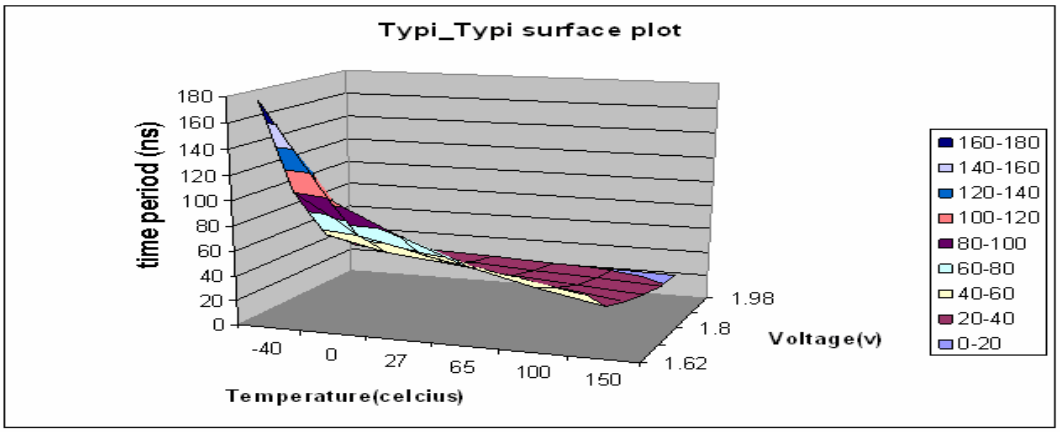

Figure23: Typical surface plot

From the plot and table it is observed that the time period decreases with increase in temperature as well as voltage. This is because; with the increase in temperature the mobility and threshold voltage (Vth) decreases. Therefore the switching from one level to the other level is faster and so the time period is decreased.

Increase in Vdd decreases the delay because it makes more carriers to be attracted into the channel and increases the channel current. In other words, a strong inversion is created which decreases the delay.

8.2 Fast Condition

The circuit was simulated for the fast corner by varying the temperature and Vdd and time period values are noted and tabulated in table 2. Figure 24 shows the 3D-plot of the variations.

Table2. Fast corner

Vdd	Temperature (degree Celsius)					
	-40	0	27	65	100	150
	Time period (ns)					
1.62	52	38.35	32.74	27.31	23.75	20.16
1.7	34.98	27.81	24.77	21.56	19.34	16.96
1.8	23.41	20.22	18.64	16.85	15.55	14.07
1.9	17.4	15.73	14.82	13.78	12.96	12.01
1.98	14.34	13.3	12.69	11.99	11.42	10.23

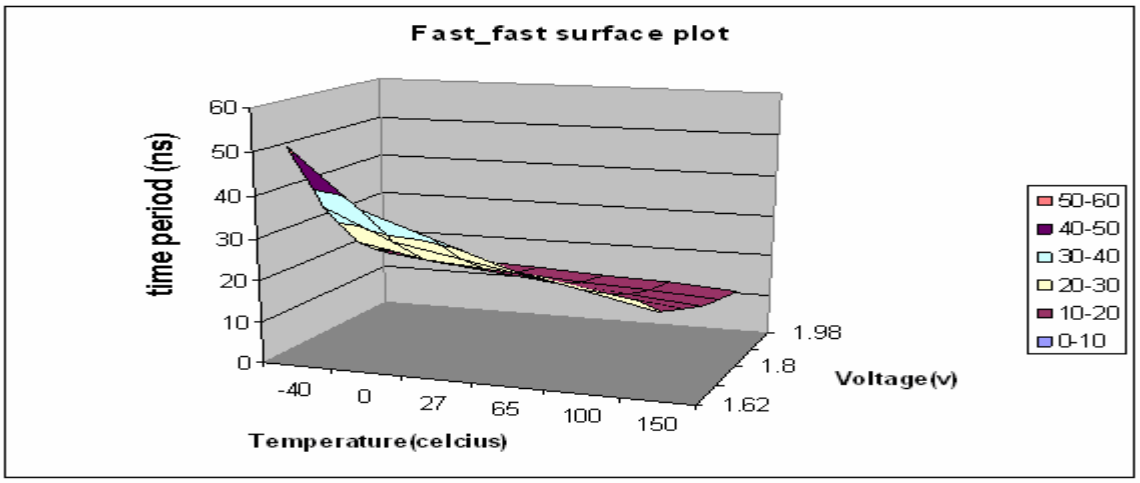

Figure24: Fast_fast surface plot

By comparing the plots of fast corner and typical corner, it can be said that the time period of fast corner is less than the typical corner.

8.3 Slow Condition

The circuit was simulated for the slow corner by varying the temperature and Vdd and time period values noted. These results are tabulated in table 3 and are plotted as shown in figure 25.

Table3. Slow corner

Vdd	Temperature (degree Celsius)					
	-40	0	27	65	100	150
	Time period (ns)					
1.62	1440	594.7	377.3	228.35	159.27	107
1.7	628.98	304.84	212.5	143.31	108.12	78.59
1.8	251.37	149.2	115.2	86.76	70.61	55.59
1.9	122.149	84.67	70.44	57.36	49.22	41.18
1.98	79.18	59.98	51.99	44.22	39.14	33.88

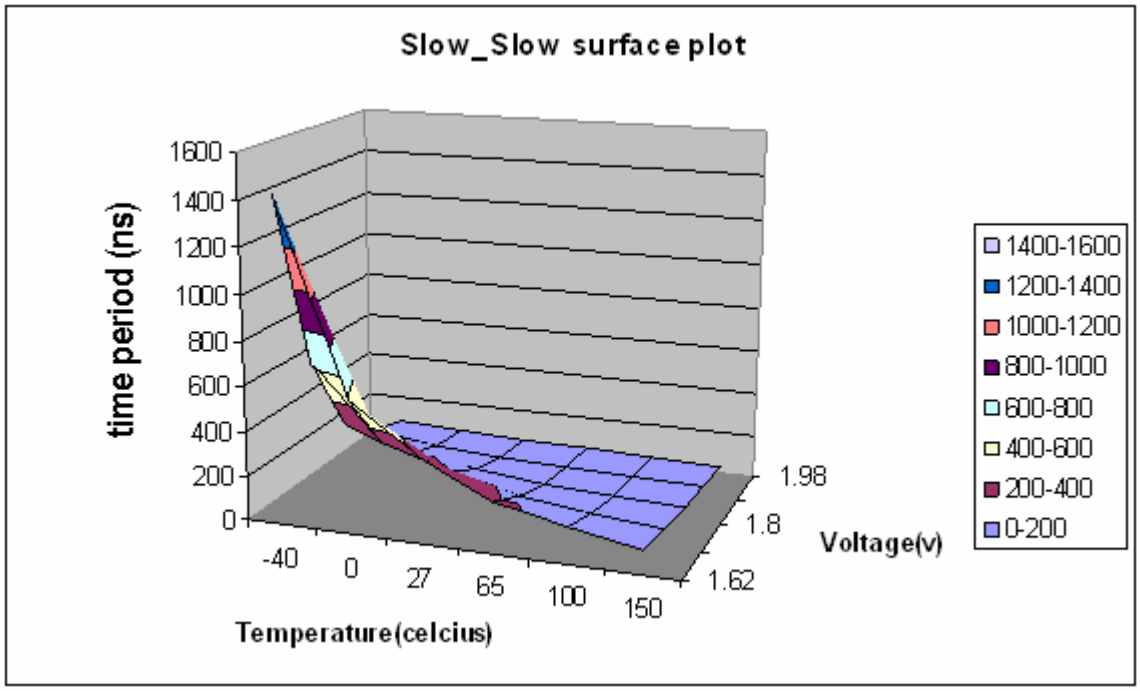

Figure25. Slow_slow surface plot

8.4 Slow-fast condition

The variation of time period with respect to vdd and temperature are shown in the table 4 and the figure 26 shows the linear plot of the results.

Table 4: slow-fast corner

Vdd	Temperature (degree Celsius)					
	-40	0	27	65	100	150
	Time period (ns)					
1.62	179.66	94.96	71.48	53.25	43.45	34.53
1.7	114.8	68.56	54.22	42.33	35.53	29.2
1.8	71.68	48.48	40.31	33.02	28.62	24.3
1.9	48.51	36.14	31.26	26.63	23.67	20.65
1.98	37.13	29.38	26.9	22.84	20.66	18.37

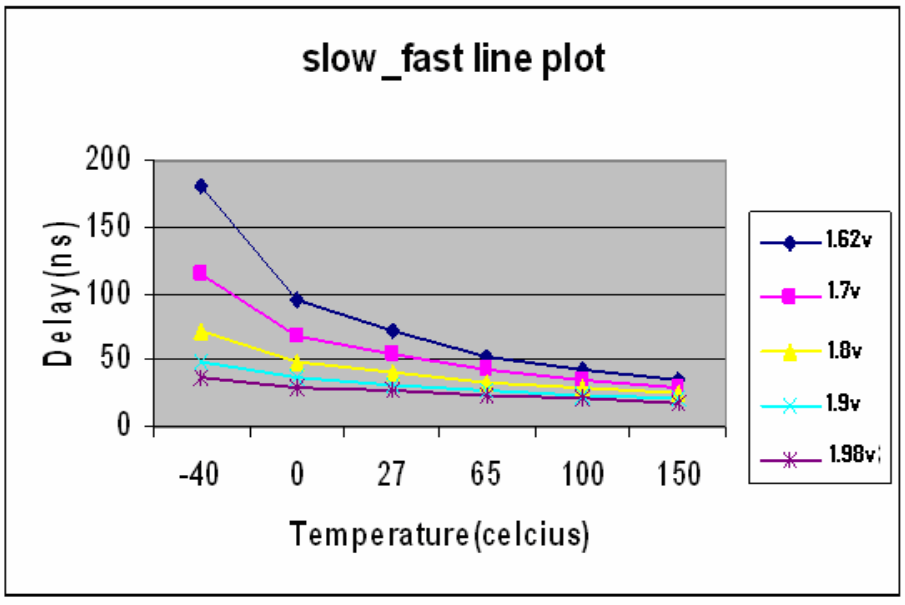

Figure 26: slow-fast linear plot

8.5 Fast-slow condition

The results for the fast-slow condition are tabulated in the table 5 and the linear plot is shown in the figure 27.

Table 5: Fast-slow condition

Vdd	Temperature (degree Celsius)					
	-40	0	27	65	100	150
	Time period (ns)					
1.62	589	268.95	180.63	116.54	85.14	59.96
1.7	258.48	140.7	103.95	74.54	58.8	44.59
1.8	104.84	70.72	57.9	46.29	39.14	32.24
1.9	52.04	41.18	36.38	31.45	28.13	24.52
1.98	34.39	29.45	27.09	24.47	22.55	20.33

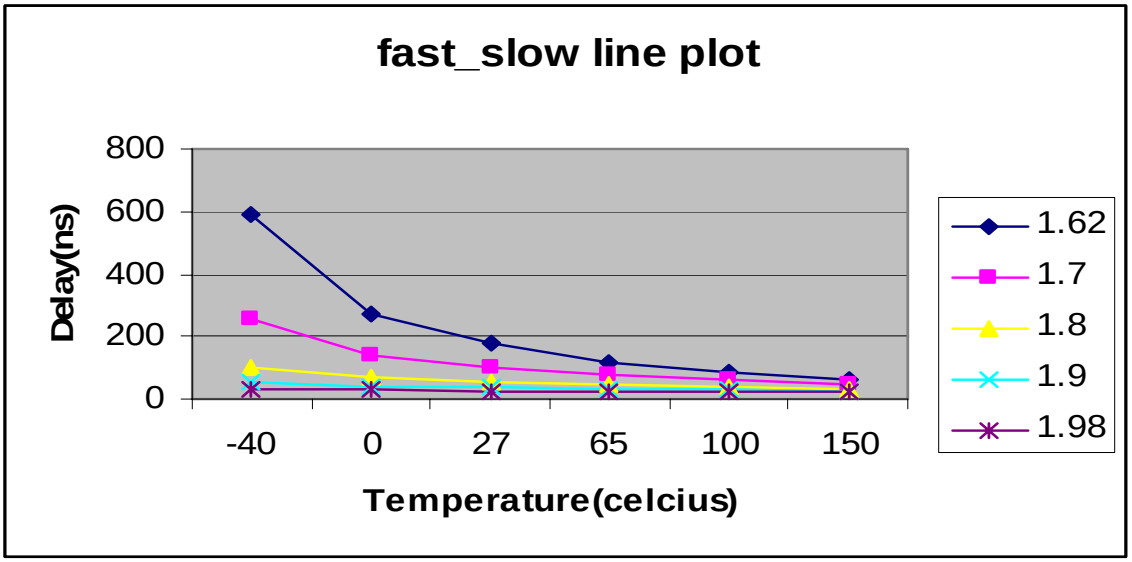

Figure 27: Fast-slow condition

9 Comparison of all the corner conditions

The table 6 shows the variation of time period with different corner conditions at a constant voltage. Here the voltage was taken as 1.8v. Figure 26 shows the line plot of these variations.

Table6: Comparison of various corners

Vdd	Temperature (degree Celsius)					
	-40	0	27	65	100	150
	Time period (ns)					
1.8	23.41	20.22	18.64	16.85	15.55	14.07
1.8	55.64	43.85	38.81	32.73	29	25.08
1.8	104.84	70.72	57.9	46.29	39.14	32.24
1.8	71.68	48.48	40.31	33.02	28.62	24.3
1.8	251.37	149.2	115.2	86.76	70.61	55.59

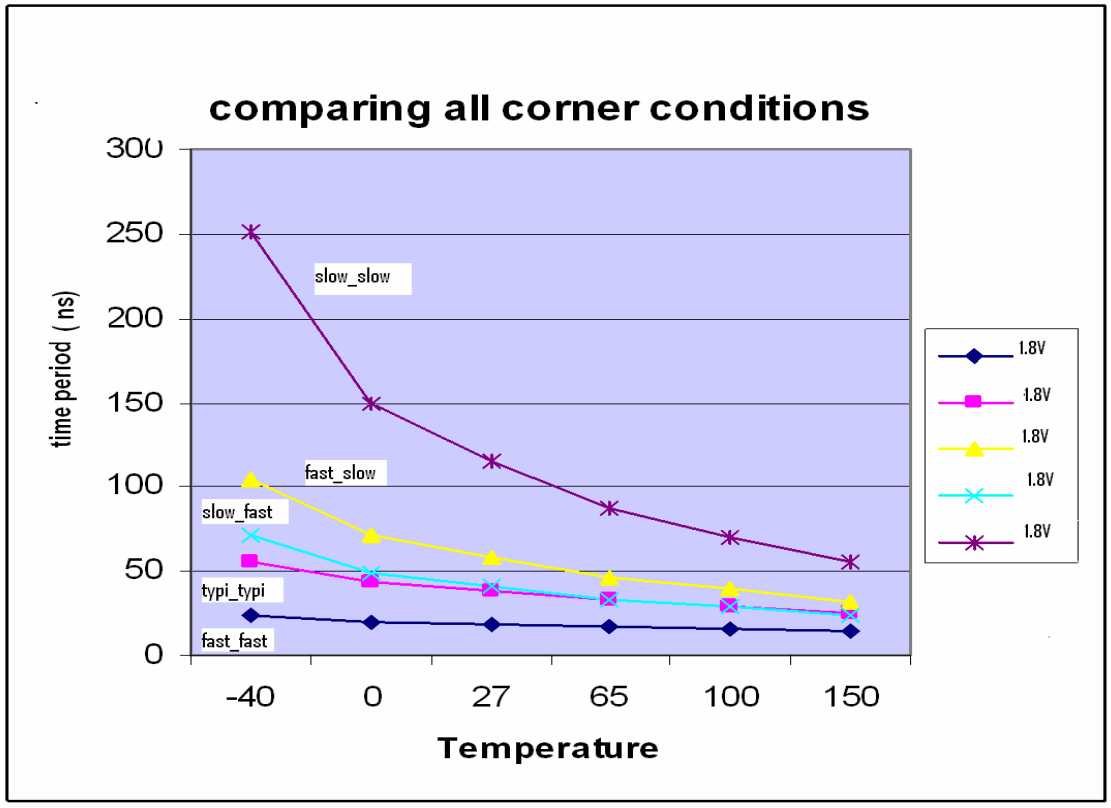

Figure26. Deviation plot for various corners

CONCLUSION

A 71-stage ring oscillator has been designed to generate the desired frequency even in the worst conditions of process variations. The raw output (frequency) is divided using a 10-stage divider circuit (D-flip flop). A six stage output buffer has been designed so that it can drive a load of 10pf. The raw and the divided output can be probed using an oscilloscope. The entire circuit is simulated under different corner conditions and the results are tabulated and plotted.

REFERENCE

1. CMOS Circuit, Layout, Design and Testing- R.J.Baker