VLSI Systems Designs: Midterm Exam (2017 Fall)

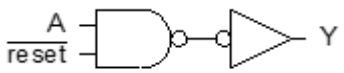
15:00-16:30, 11/13/2017, Prof. Jinsang Kim

Assume that a matched unit inverter has widths of 45nm for nMOS and 90nm for pMOS, respectively. The 45nm process technology uses the followings unless stated otherwise:
$V_{DD} = 1\,V,\ Vto = 0.3\,V, \beta_n = 1mA/\,V^2, \Phi_s = 0.6\,V, \gamma = 0.3\,V^{0.5}, \lambda = 0.02, \tau = 3RC = 3ps,$
$electron velocity = 10^5 cm/s$

1. (15pts) Find the best number of stage, N, in a logic block which provides the minimum delay when there are no extra inverters (buffers) at the output. Using this number, design the inverter chain and find the delay when input and output loads are 1 unit and 148.42 unit, respectively. What are the sizes of the inverters.

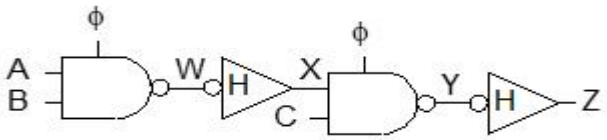
2. (15pts) There are two metal wires and adjacent capacitance between two wires is 20fF. 5x inverters drive the two metal wires and there are 3x inverters at the end of the wires. The wires are 1 um long and 2λ wide with $R = 0.08\ \Omega/\square$, $C_{permicron}$ =0.2 fF/μm . Assume that the gate capacitance of a unit inverter is C=2fF/um and resistances of both nMOS and pMOS are $R = 2.5\,K\Omega \cdot \mu m$. Estimate the delay from the driver to load when an input changes from '0' to '1' while an input changes from '1' to '0' on the other wire.

3. (15pts) The asymmetric two input NAND gate favors signal 'A' and the inverter has the fastest average delay. In this problem, assume the mobility ration of the matched inverter is 3. Determine the sizes and logic efforts of all gates including the inverter.



4. (15pts) Design an efficient 2 input NAND gate and find logical efforts of all signals in case of static CMOS logic, pseudo-nMOS logic, and dynamic logic.

5. (25pts) The 2 input NAND gates in the following logic favor signal 'A' and 'X' over 'B' and 'C' by 10%. Determine the sizes of the following transistors and find the delay from 'A' to 'Z' when input and output capacitances are 1fF and 200fF, respectively.



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