HSPICE & Layout LAB (VLSI Systems Design: 2020 Fall) (100pts)

Due: 6:00 PM, 10/23/2020 (upload to e-campus or email(jskim27@khu.ac.kr)) Prof. Jinsang Kim

1. (15pts) Design and simulate a matched inverter. Please add corner simulations.

   I-V and DC simulation using HSPICE, Noise margins (9), corner (4), Analysis&Comments (2)

2. (15pts) Measure the FO4 delay and the FO4 power. For this experiment, please refer to the HSPICE lecture note or the textbook.

   HSPICE program(5), Analysis&Comments (10)

3. (20pts) Simulate CMOS D Flip-Flop. Also, try to analyze the setup time and the hold time.

   HSPICE Program(5), simulation (5), setup & hold time (5), Analysis&Comments (5)

4. (50 pts) Given Y= (AB+CDE)F (complementary inputs are not available). Simulate and layout a two-stage CMOS circuit by adding an output inverter. Also, measure propagation delays and contamination delays.

   simulation using HSPICE (10), layout and simulation (30) Analysis&Comments (10)