AUTOMOTIVE SEMICONDUCTOR
SAFETY INNOVATION CONFERENCE
ASSIC KOREA 2019 Oct 24th, 2019

Radiation Tests of Modern Devices

Sung Chung
CTO, QRT Inc.

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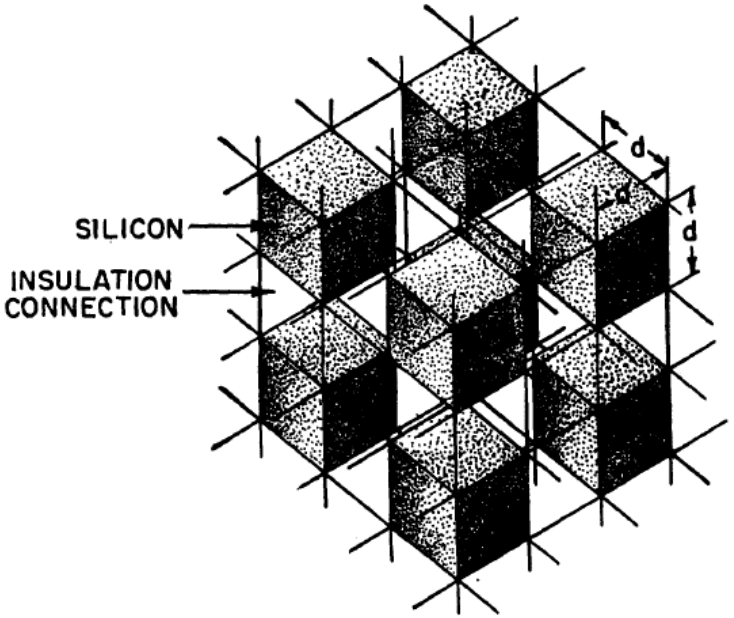
ASSIC KOREA 2019

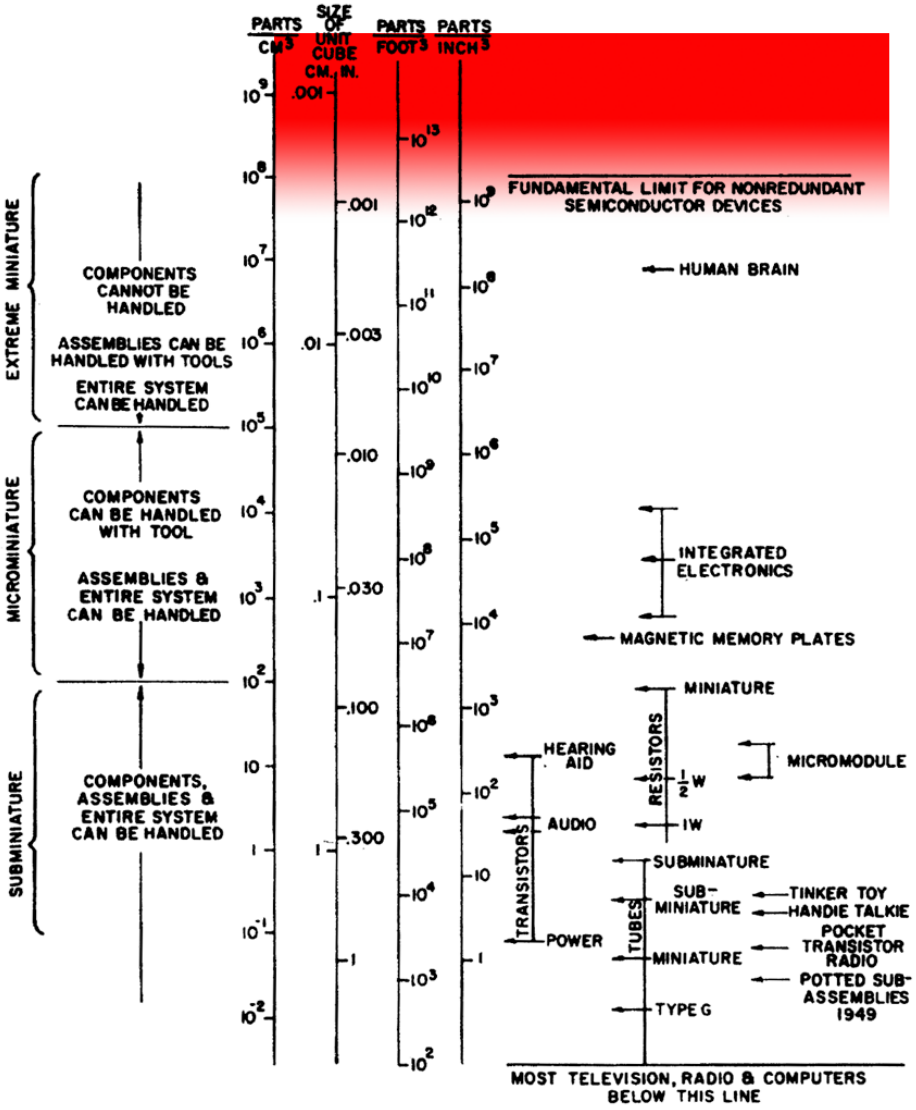
00

Opening Remark

1962: 10µm Limit!

J. T. Wallmark and S. M. Marcus, "Minimum Size and Maximum Packing Density of Nonredundant Semiconductor Devices", Proc. IRE, Vol. 50(3), pp. 286 – 298, March 1962 (RCA)





"minimum device size… approximately ($10\mu m^3$) , 10^8 components/cm^3"
"limited by cosmic ray events and thermal considerations"

After Robert C. Baumann, "LANDMARKS IN TERRESTRIAL SINGLE-EVENT EFFECTS" IEEE 50th *2013 NSREC Short-Course*

Intel: EUV-Enabled 7nm Process

EUV estimated demand per fab by market

Range of layers and corresponding systems per fab[1]

Market	Fab Capacity (kwspm[2])	EUV layers	EUV systems/fab
Logic (7nm – 5nm)	45	10 – 20	10 – 20
DRAM (16nm -1Anm)	100	1 - 6	2 - 10

Logic EUV capacity:
1 EUV layer requires 1 EUV system for every 45k wafer starts per month

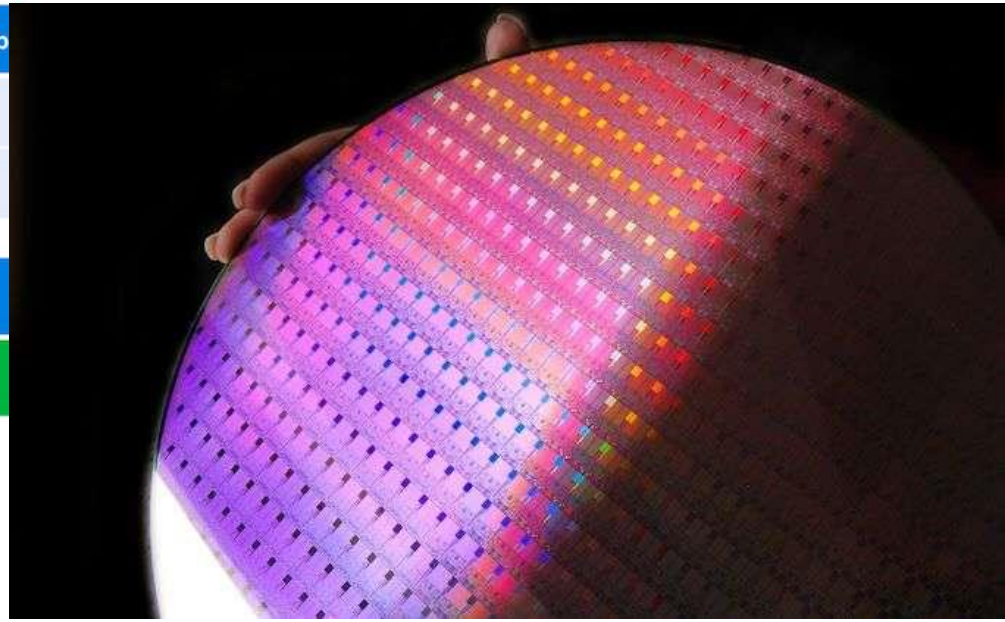
DRAM EUV capacity:
1 EUV layer requires 1.5 to 2 EUV systems for every 100k wafer starts per month

[1] "Typical" process and system conditions in the 2018-2022 timeframe, not specific customer condition
[2] kwspm: x1000 wafer starts per month

Extreme Ultraviolet Lithography (EUVL) Demand

ASML
Public
Slide 9
8 November 2018

Dec. 6, 2018



We are quite pleased with our progress on 7 nm.
In fact, very pleased with our progress on 7 nm.

Murthy Renduchintala, chief engineering officer & president of technology

https://www.anandtech.com/show/13683/intel-euvenabled-7nm-process-tech-is-on-track

Google has reached Quantum Supremacy

01

최근에 일어난 변화들

전자신문

초미세 D램 개발, 세 가지 걸림돌

강해령 입력 2019.05.10. 14:37 수정 2019.05.12. 20:16 댓글 21개

지난 10일 열린 한국반도체디스플레이학회 2019년 춘계학술대회에서 황상준 삼성전자 메모리사업부 상무가 발표하고 있다.

D램 크기가 갈수록 작아지면서, 기술적으로 극복해야 할 3가지 문제가 제기됐다. 비행기로 반도체를 운송할 때 방사선의 영향을 받아 생기는 불량, D램 크기가 작아지면서 생기는 로 해머링(Row Hammering) 현상, D램 셀 전기용량(캐패시턴스) 저하가 그것이다. 글로벌 D램 반도체 업체들은 이를 극복하기 위해 다양한 방안을 고민하고 있다.

초미세 D램 뿐만 아니라 초미세 SoC도 동일한 방사선 영향을 받는 불량이 나타날 수 있다

2018년 12월: ISO26262:2018 자동차 기능안전 표준

ISO 26262

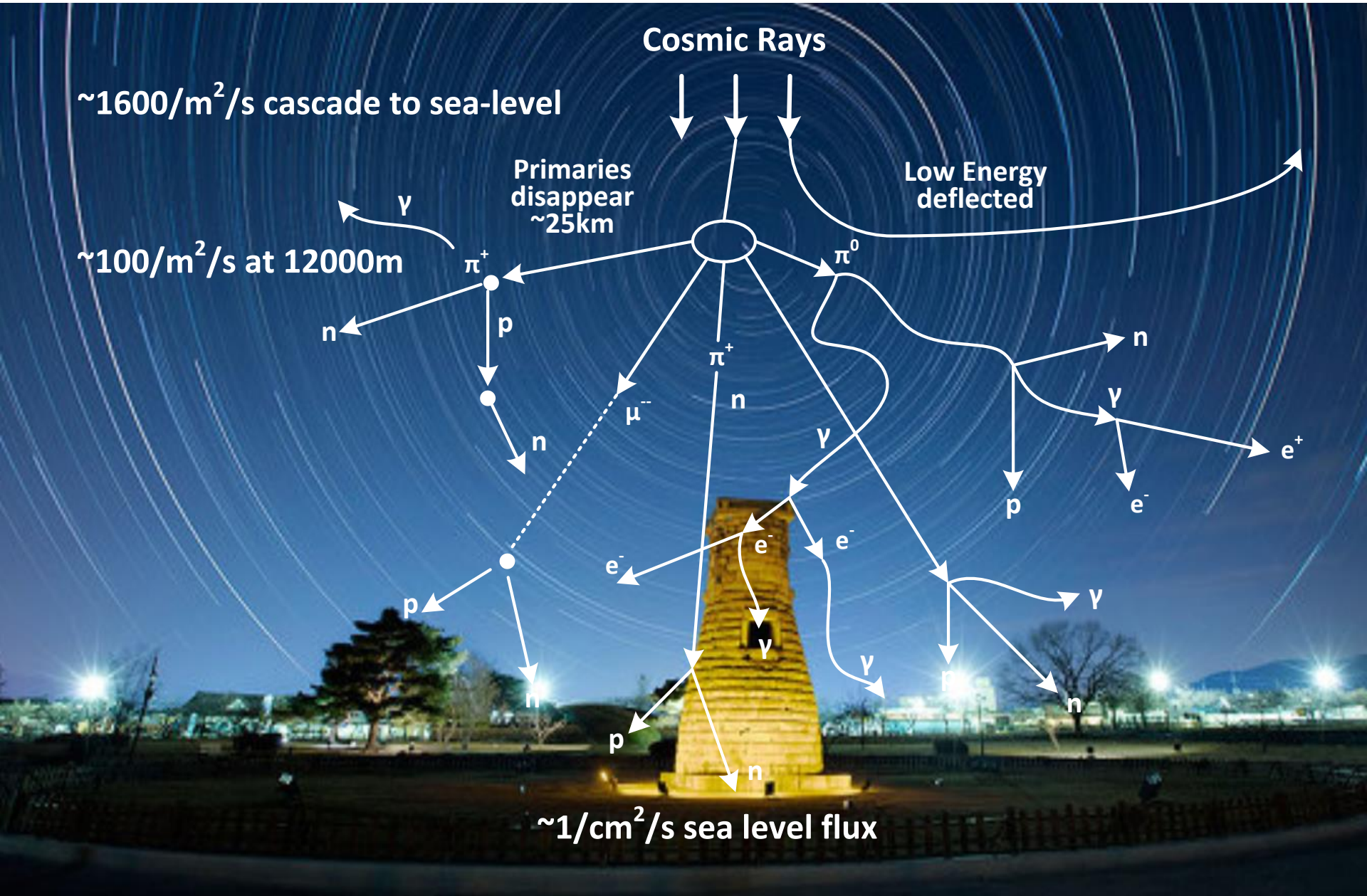
Functional Safety for Road Vehicles

반도체 소프트 오류 검사의 의무화

狱

놀라 달아날

중성자 준비 없이는 살수 없는 세상



"Soft errors induce the highest failure rate of all other reliability mechanisms combined." Baumann, Robert.

- "The SER of advanced CMOS devices is **higher than all other reliability mechanisms combined**."

  Baumann, Robert. "The impact of technology scaling on soft error rate performance and limits to the efficacy of error correction." IEDM'02.

- "Left unchallenged, **soft errors** have the potential for inducing **the highest failure rate of all other reliability mechanisms combined**.

  Baumann, Robert. "Radiation-induced soft errors in advanced semiconductor technologies." IEEE Trans on Device & materials reliability 5, no. 3 (2005)

- "Soft errors have become a huge concern in advanced computer chips because, uncorrected, they produce a **failure rate exceeding that of all other reliability mechanisms combined**."

  Baumann, Robert. "Soft errors in advanced computer systems." IEEE Design & Test of Computers 22, no. 3 (2005): 258-266.

- "Thus, one could postulate that there will be a cross-over point where **SET induced error rates will exceed the traditional SEU error-rates**"

  La Bel, Kenneth A., and Lew M. Cohn. "Radiation testing and evaluation issues for modern integrated circuits." (2005).

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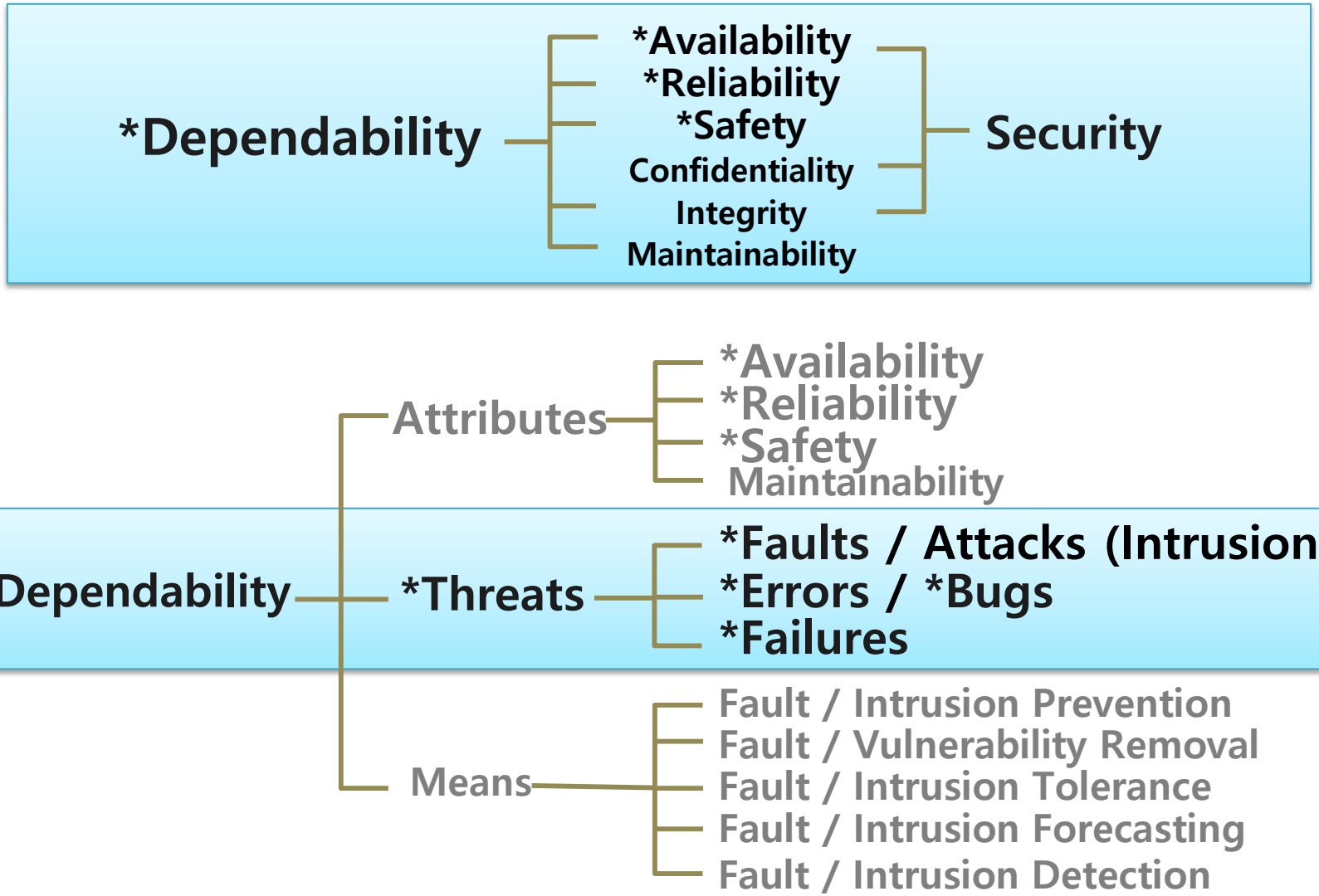
02

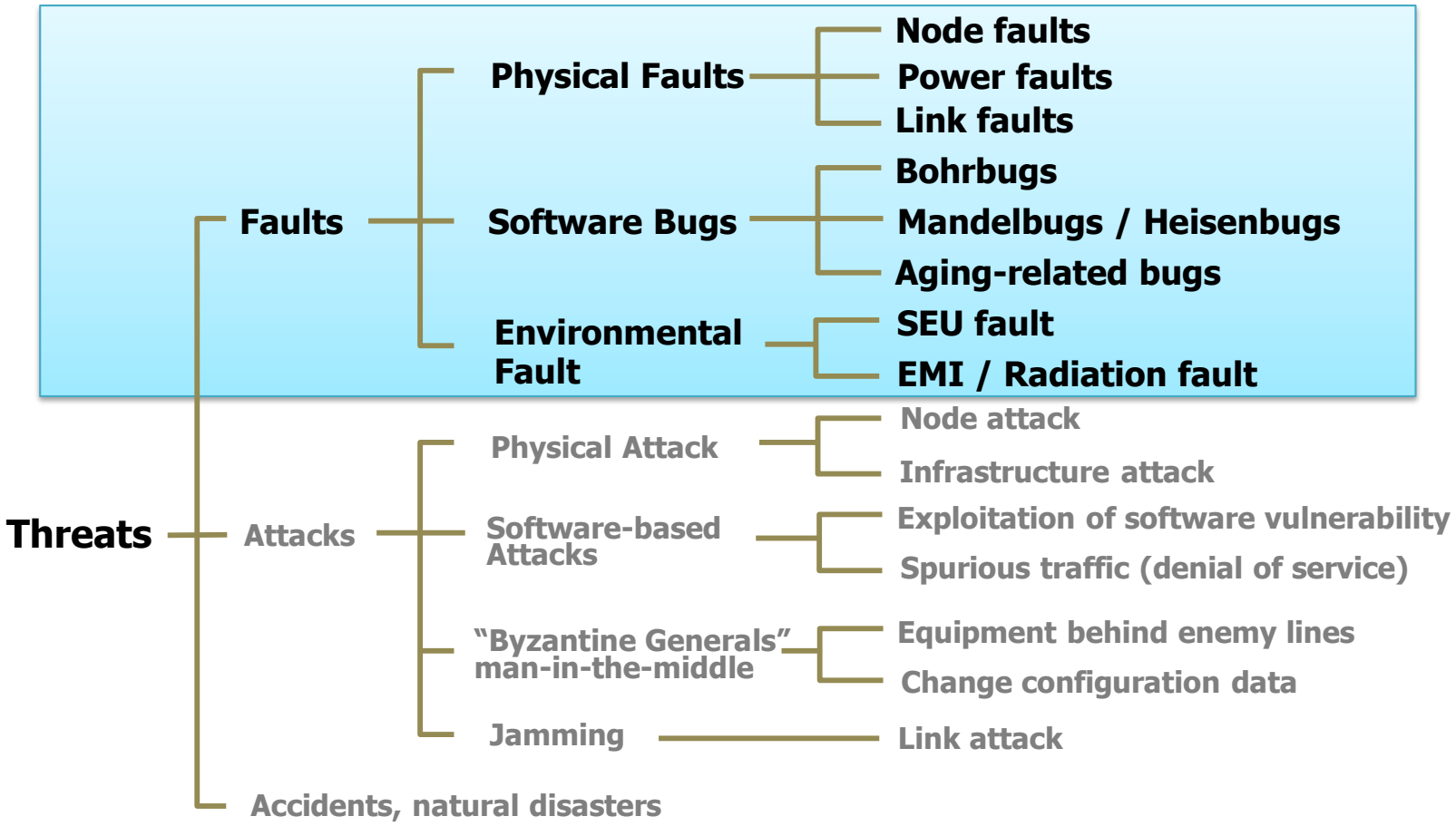
용어 정리

신뢰성 시스템 개요



Adopted from Kishor S. Trivedi, "Dependability, Security and Survivability Models," NGNS 2010 Keynote, July 2010

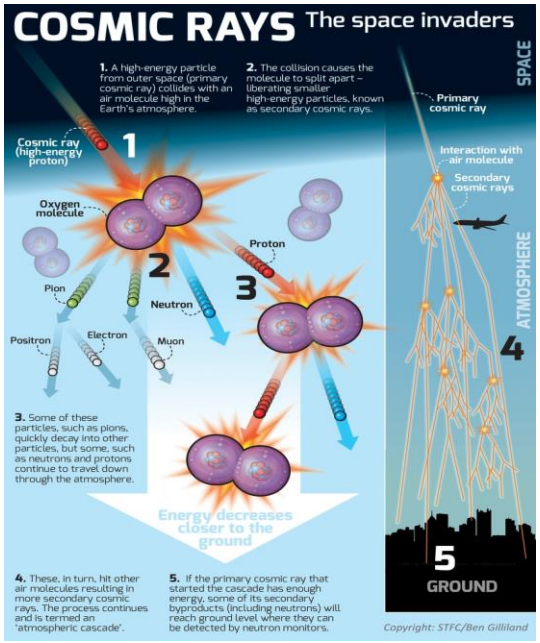
시스템에서 보는 결함의 종류

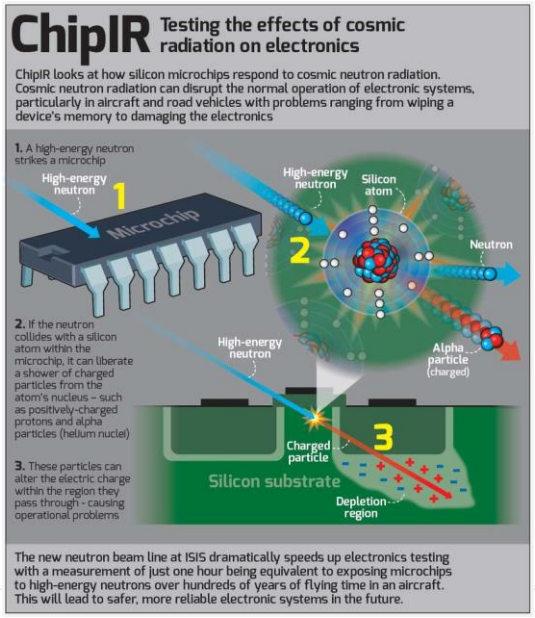


Adopted from Kishor S. Trivedi, "Dependability, Security and Survivability Models," NGNS 2010 Keynote, July 2010

소프트 에러 용어

- SE **Single Event**
  - **단일 사건(單一 事件)**
  - 단일(單一) 이벤트
- SEE **Single Event Effect**
  - **단일 사건 효과 (單一 事件 效果)**
  - 단일(單一) 이벤트 효과((效果)
- SEU **Single Event Upset**
  - **단일사건 여기 (單一 事件 勵起)**
  - 단일(單一) 이벤트 여기(勵起)
- **Soft Error**
  - **소프트 오류 (誤謬)**
  - 소프트 에러
- Neutron **Radiation Test**
  - 중성자 **방사선 시험 (**中性子 **放射線 試驗)**





https://stfc.ukri.org/news/aeroplane-and-internet-systems-better-protected-thanks-to-unique-uk-technology/

03

ISO26262 표준의 기능안전 용어

ISO26262 표준의 결함 정의

ISO 26262:2018 Road Vehicles Functional Safety-Part 1: **Vocabulary**

- 3.51 "**fault**"

  "**abnormal condition that can cause an element** (3.38)**or an item** (3.82) **to fail**"

  - Permanent, intermittent, and transient faults (3.172) (especially soft -errors) are considered.

- 3.172 "**transient fault**"

  "**fault** (3.51) **that occurs once and subsequently disappears**"

  - Transient faults can appear due to electromagnetic interference, which can lead to bit-flips.

    Soft-errors such as "Single Event Upset" (**SEU**) and "Single Event Transient" (**SET**) are **transient faults**.

일시적 결함의 종류

- **Single Event Transient (SET):** A momentary voltage excursion (e.g. a voltage spike) at a node in an integrated circuit caused by the passage of a single energetic particle
- **Single Event Upset (SEU):** A soft error caused by the signal induced by the passage of a single energetic particle
- **Single Bit Upset (SBU):** A single storage location upset from a single event
- **Multiple Cell Upset (MCU):** A single event that induces several bits in an IC to fail at the same time. The error bits are usually, but not always, physically adjacent
- **Multiple Bit Upset (MBU):** Two or more single-event-induced bit errors occurring in the same nibble, byte, or word. An MBU could be not corrected by a simple ECC (e.g. a single-bit error correction)

1. **SET, SEU, SBU, MCU** and **MBU** are typically indicated as "soft errors".
2. **Transition faults** and similar timing related phenomena are considered when relevant for the specific.
3. **Some fault models** can have the same effect as other fault models and therefore can be detected by the same safety mechanism. (**masking, derating**) An appropriate justification is provided to show that correspondence.

ISO 26262 Reference ISO 26262-11:2018 [5.1.2] Fault models of non-memory digital components

오류율 감소: Derating

- In case of **soft errors**, **reducing the base failure r**ate by only considering the operating time of the vehicle leads to an excessive and therefore artificial reduction of the average probability per hour.
  - Moreover, the base failure rate for soft errors is provided without de-rating it with respect to “architectural vulnerability factors” or the effect of safety mechanisms such as ECC.

ISO 26262 Reference	ISO 26262-11:2018 4.6.1.8 Transient fault quantification

    - **Architectural vulnerability factor (AVF)** is the probability that a fault in a design structure will result in a visible error in the fi nal output of the function
    - **Vulnerability factors** are taken into account when considering of the number of safe faults, as described in 5.1.7.2.

ISO 26262 표준 참고	ISO 26262-11:2018 [5.1.11] Safety Manual for digital components ISO 26262-11:2018 [5.2.6] Safety Manual for analogue or mixed signal components ISO 26262-11:2018 [5.3.6] Safety Manual for PLD ISO 26262-11:2018 [5.5.6] Safety Manual for Sensors and Transducers

구조적 취약 인수 Architectural Vulnerability Factors

- **Architectural vulnerability factor (AVF)** is the probability that a fault in a design structure will result in a visible error in the final output of the function as, for example, described for processor designs in reference [25].
- **Vulnerability factors** are taken into account when considering of the number of ***safe faults***, as described in 5.1.7.2.
  - 5.1.7.2. How to consider transient faults of digital components

ISO 26262 Reference	ISO 26262-11:2018 Subclause [4.6.1.8] Considering the number of safe faults

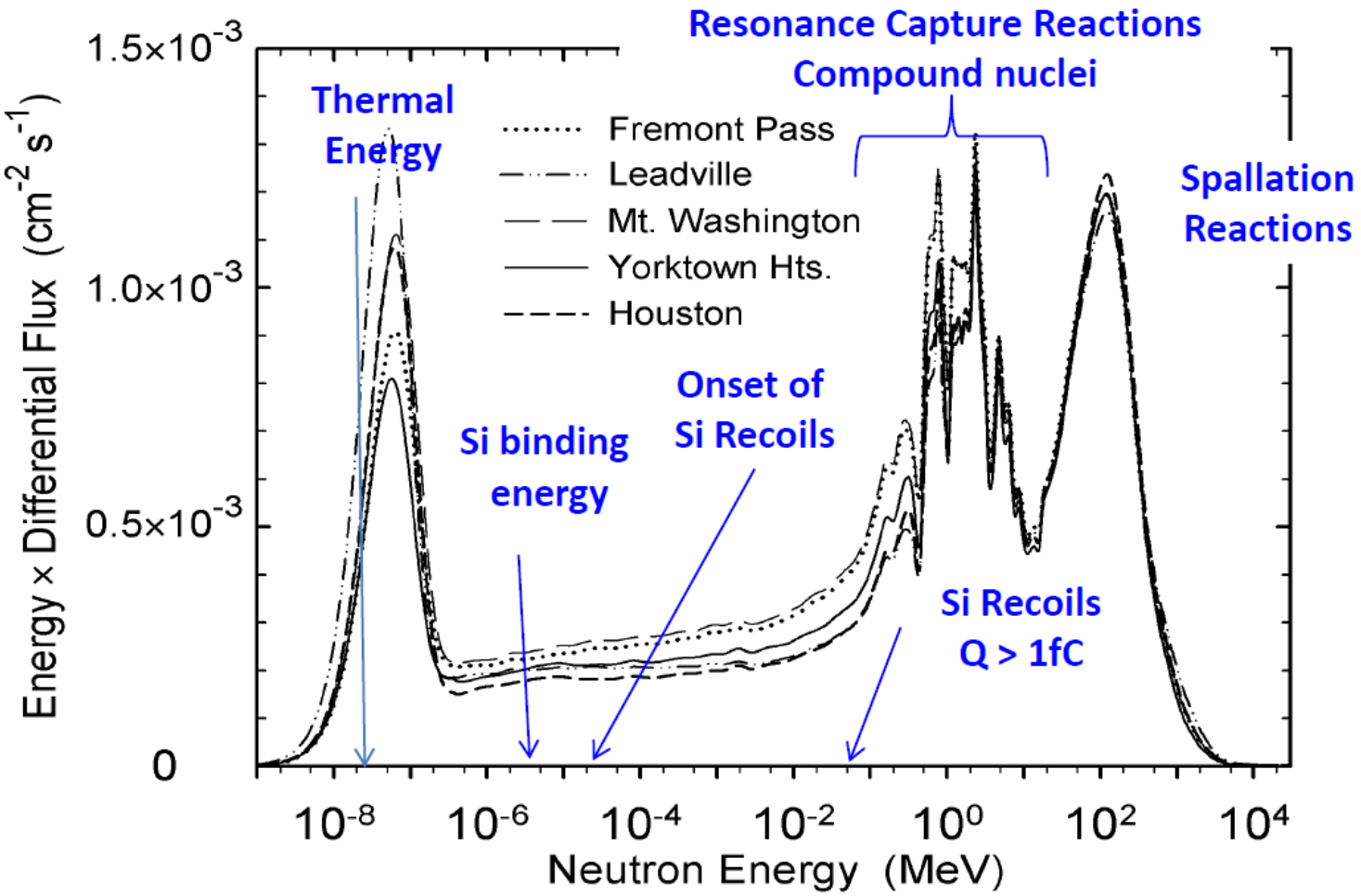
S. Mukherjee, C. Weaver, J. Emer, S. Reinhardt, T. Austin, "A systematic methodology to compute the architectural vulnerability factors for a high-performance microprocessor," In Proc of Inter Symp on Microachitecture (MICRO), pp; 29–42, 2003.

04

소자의 중성자 민감도

지상 우주선

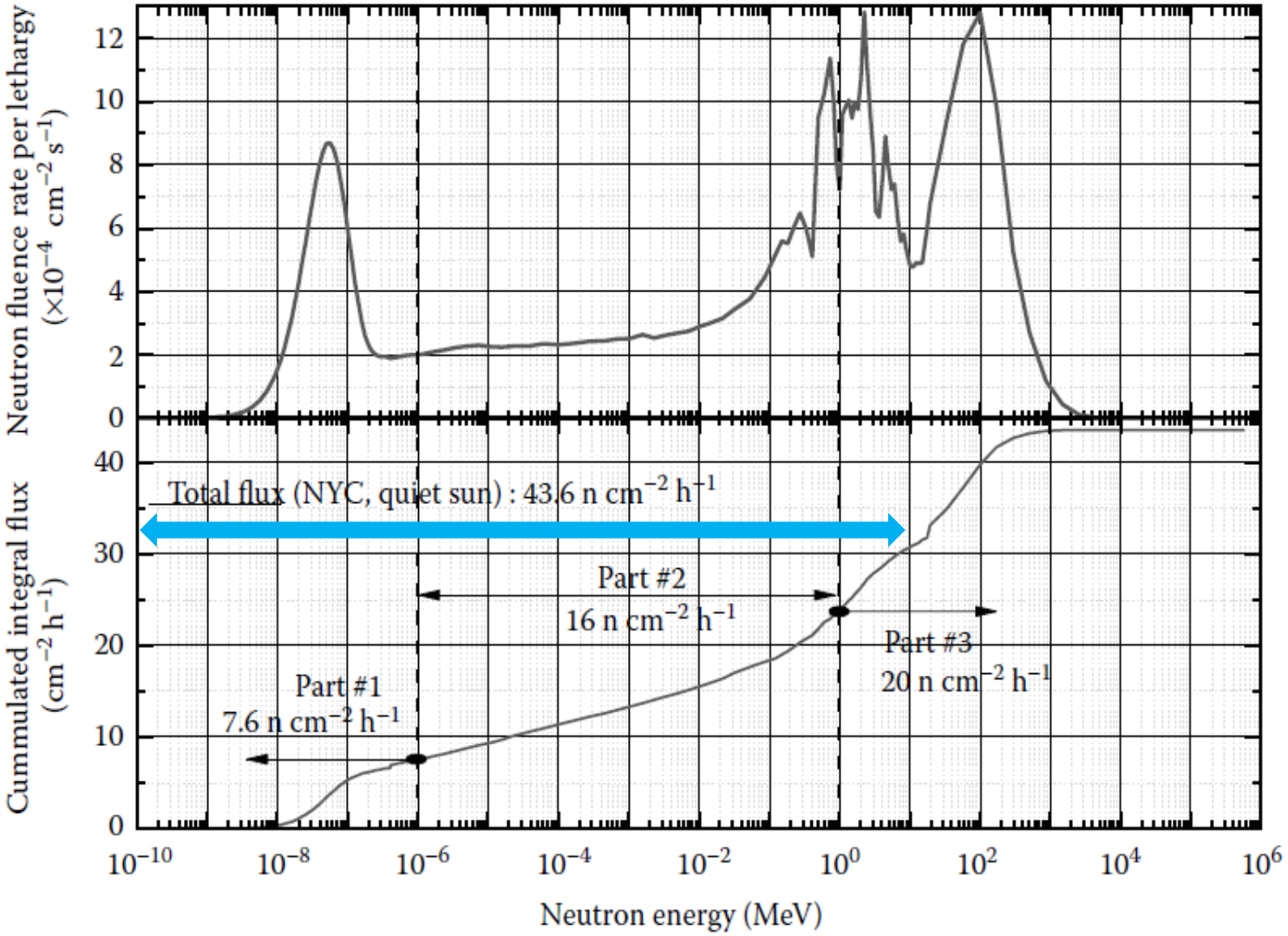
JEDEC JESD89A Standard flux is~13 n/cm²-hr @ Sea-Level, NYC En ≥10 MeV



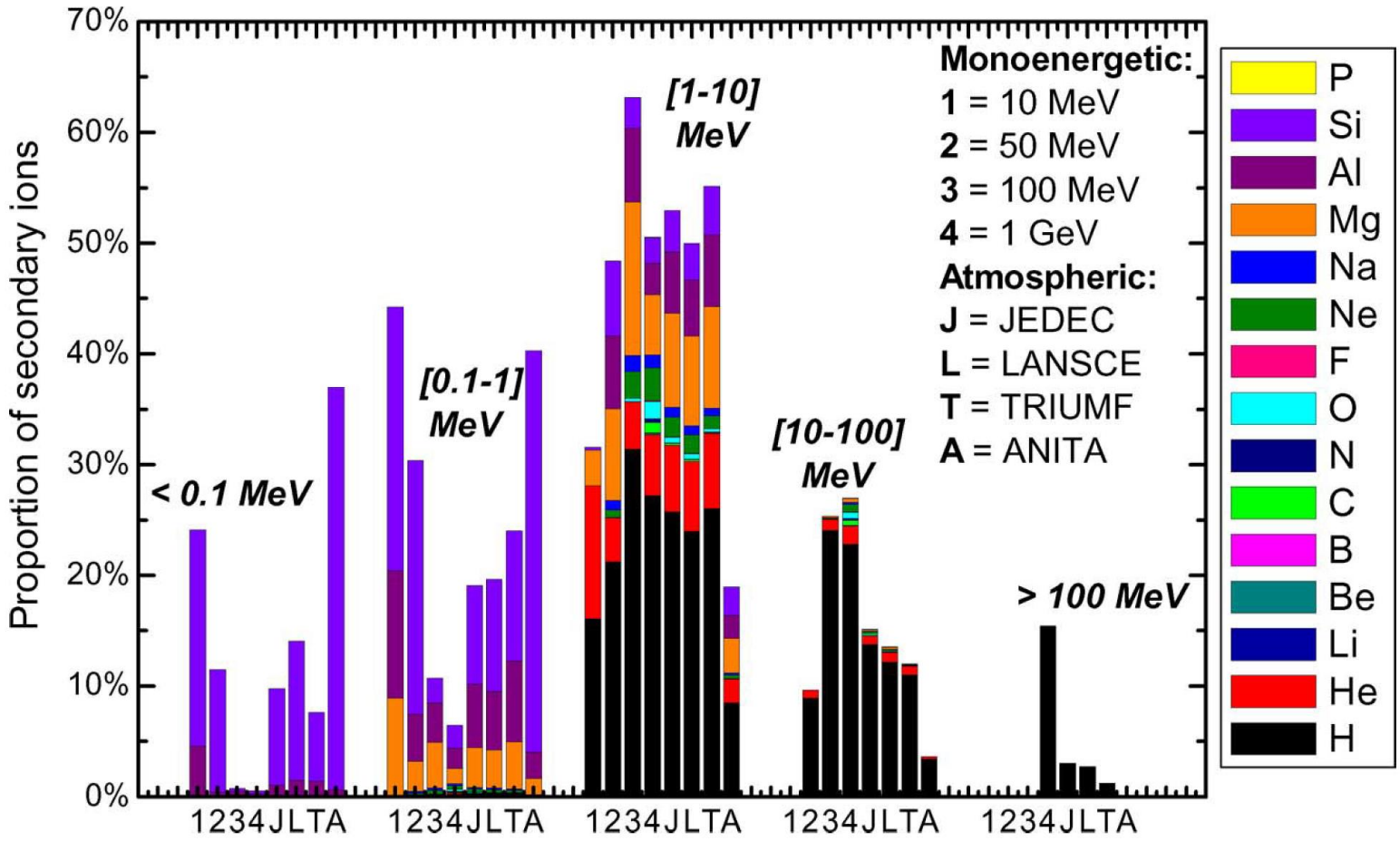
After Robert C. Baumann, "**LANDMARKS IN TERRESTRIAL SINGLE-EVENT EFFECTS**" IEEE 50th *2013 NSREC Short-Course*

M. Gordon, P. Goldhagen, et al., "Measurement of the Flux and Energy Spectrum of Cosmic-Ray Induced Neutrons on the Ground," IEEE Trans. Nucl. Sci., 51(6), pp. 3427-3434, Dec. 2004.

10 MeV까지 중성자 33개 (/cm²/Hr)



중성자 에너지와 반도체 소자의 반응 비교



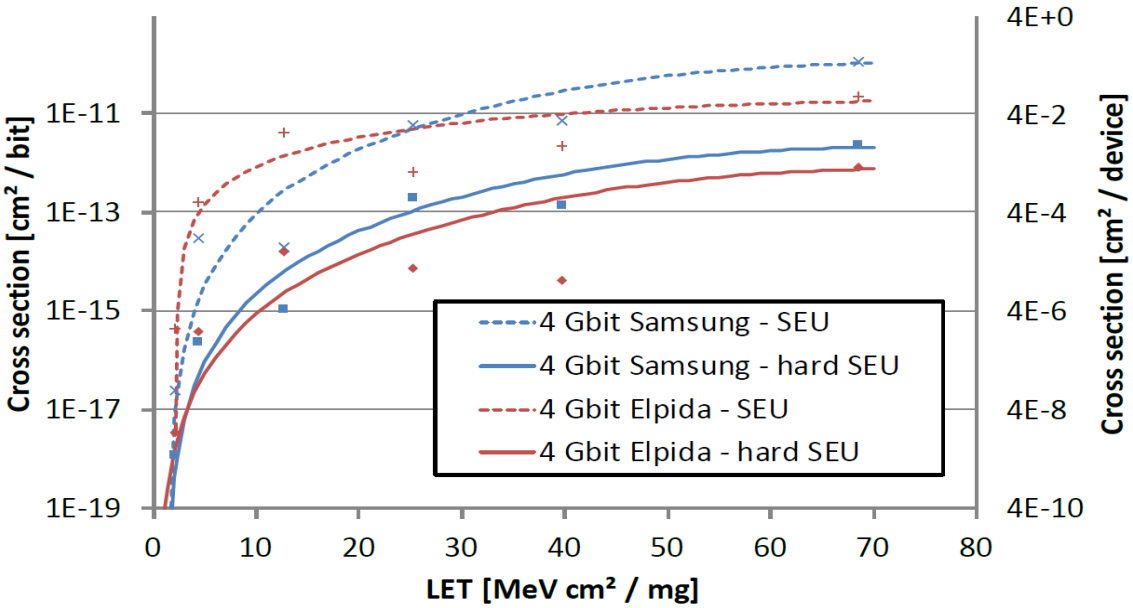
Energy histogram for the secondary ion cocktails produced by n-Si interactions for the different neutron sources considered

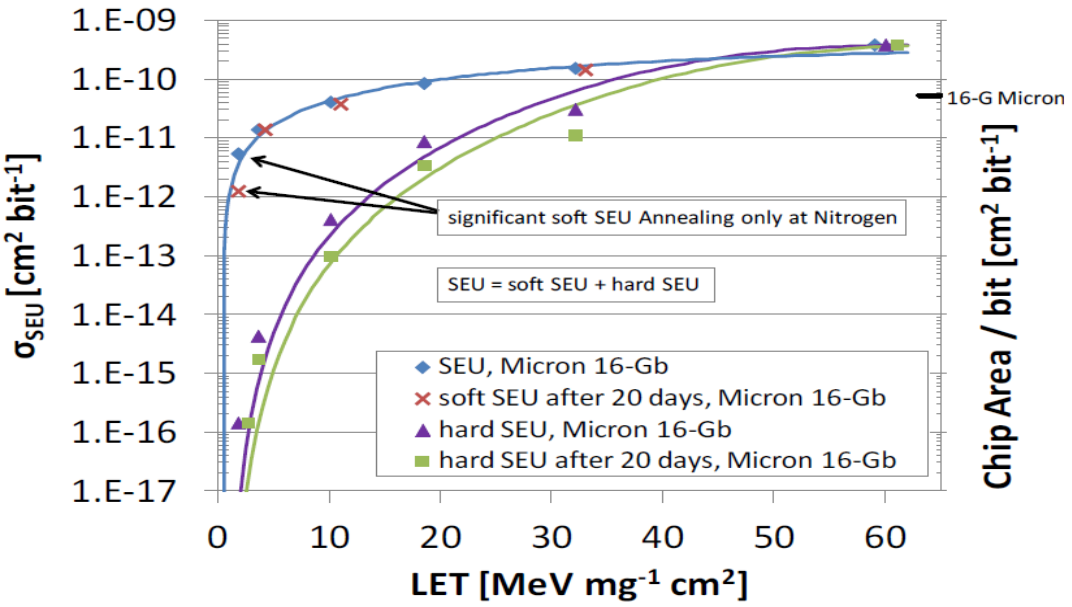
Serre, S., S. Semikh, S. Uznanski, Jean-Luc Autran, Daniela Munteanu, G. Gasiot, and P. Roche. "Geant4 analysis of n-Si nuclear reactions from different sources of neutrons and its implication on soft-error rate." IEEE Transactions on Nuclear Science 59, no. 4 (2012): 714-722

05

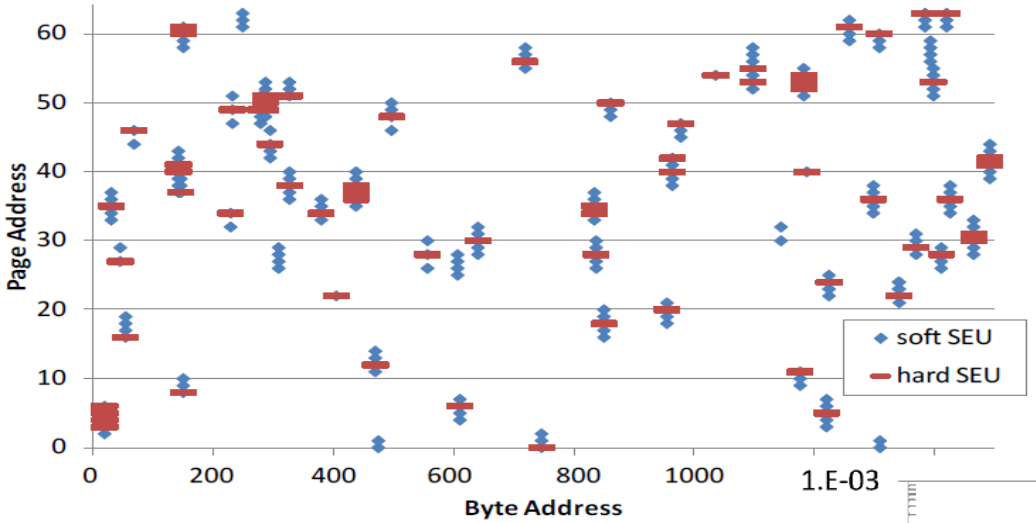
한국 주력 반도체: D램과 Flash

DDR3 와 NAND – 고정 비트



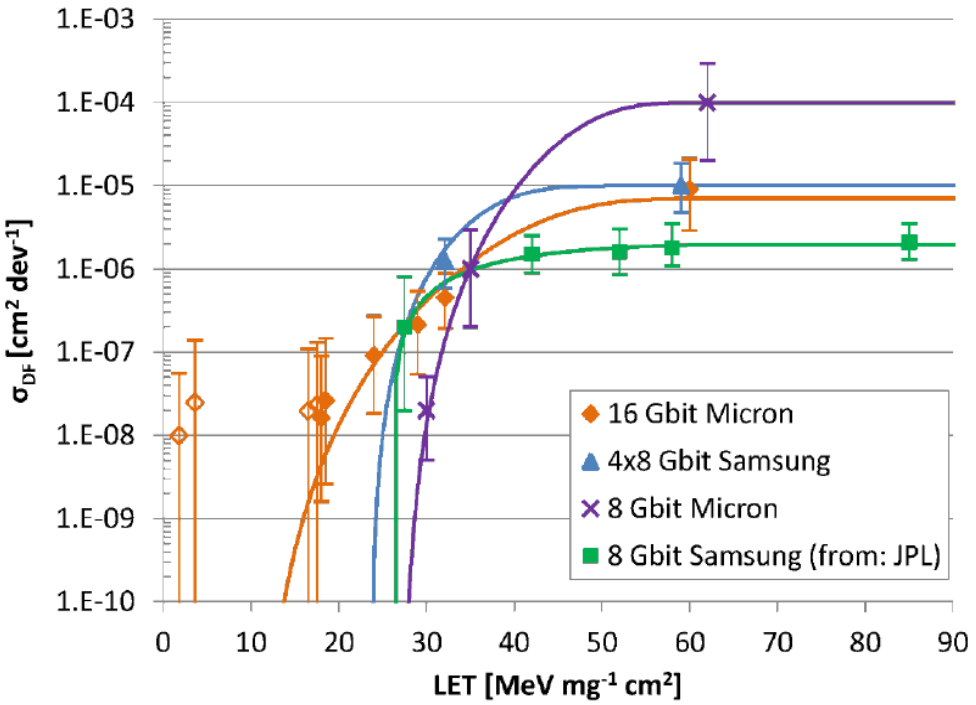


NAND와 Flash의 Soft, Hard, Destructive 오류



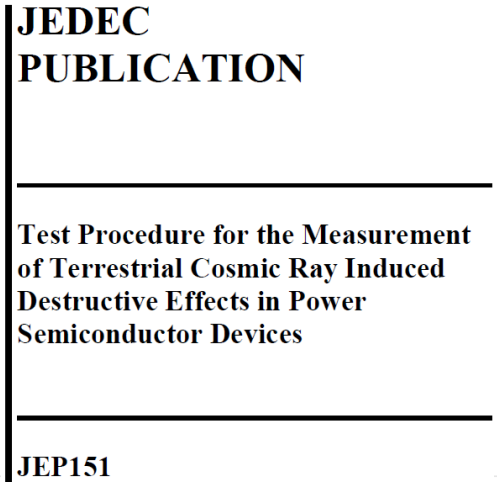
Stuck bits in NAND-flash

Destructive events in NAND-Flash



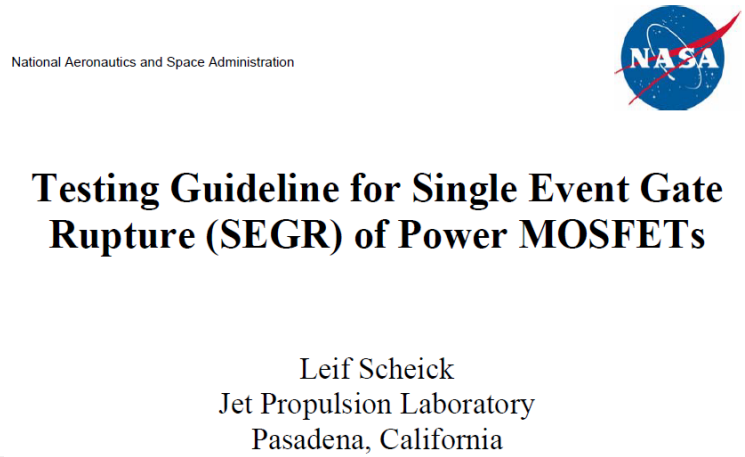
전력반도체 SEE 메커니즘과 평가 표준

- 전력반도체의 대기 중성자 SEE 메커니즘
  - SET (Single Event Transient)
  - SEL (Single Event Latch-up)
  - SEBO (Single Event Burn Out)
  - SEGR (Single Event Gate Rupture)
  - TID (Total Ionizing Dose) Effect
  - NIEL (Non-Ionizing Energy Loss)
  - SEDD (Single Event Displacement Damage)
- NASA와 JEDEC SEE 평가 표준


JEDEC
PUBLICATION

Test Procedure for the Measurement of Terrestrial Cosmic Ray Induced Destructive Effects in Power Semiconductor Devices

JEP151


National Aeronautics and Space Administration

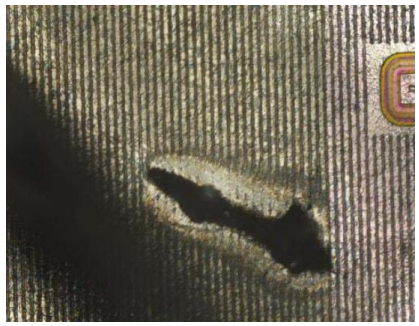
NASA

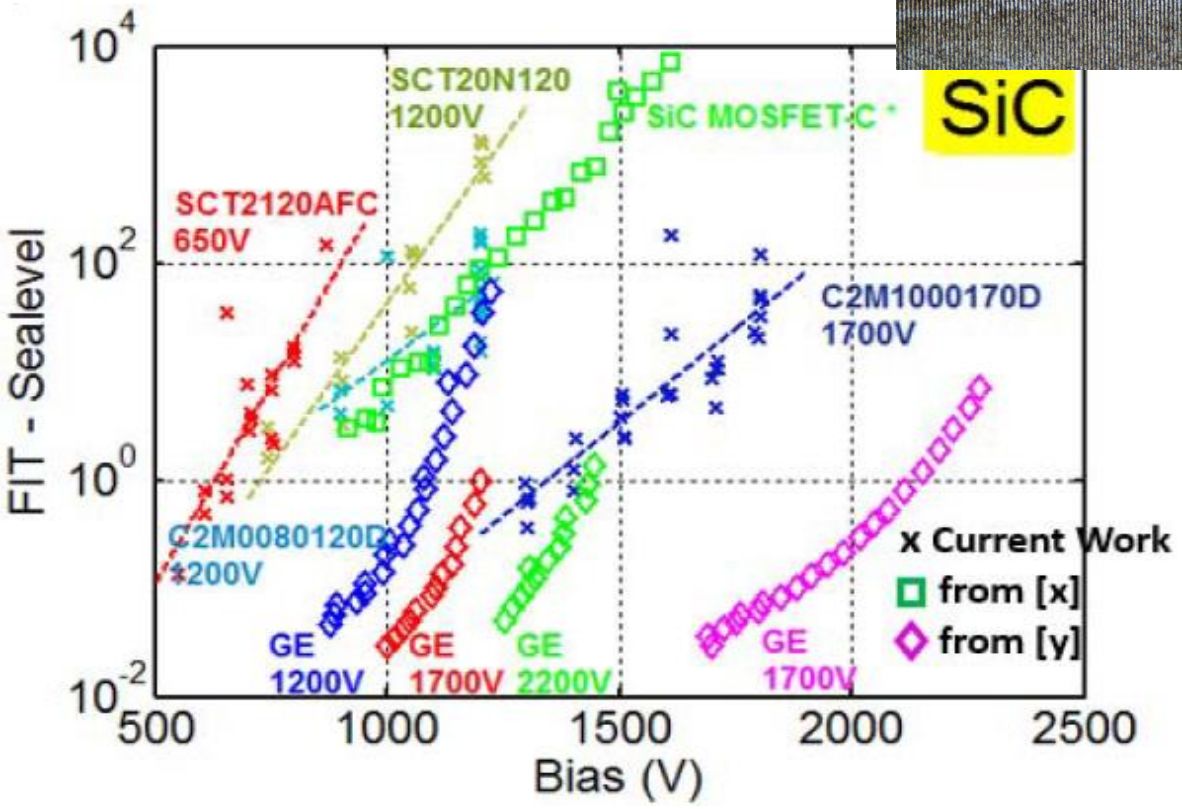
Testing Guideline for Single Event Gate Rupture (SEGR) of Power MOSFETs

Leif Scheick
Jet Propulsion Laboratory
Pasadena, California

전력반도체 중성자 SEE 평가 자료 1

Damage occurred during destructive mode testing in SiC power MOSFETs.

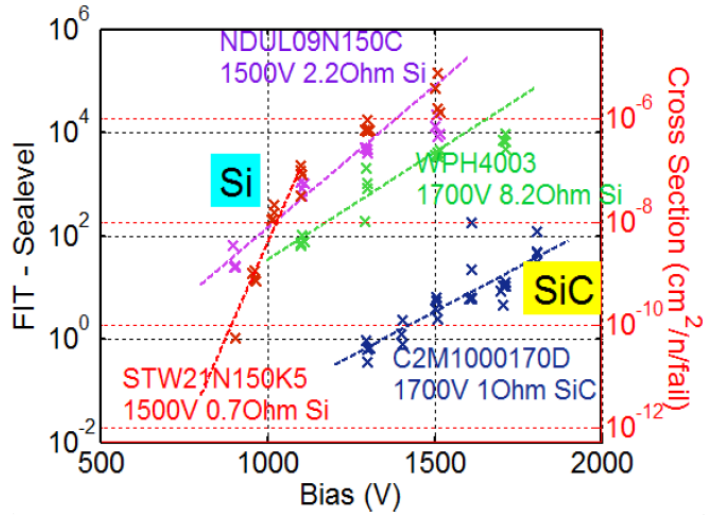


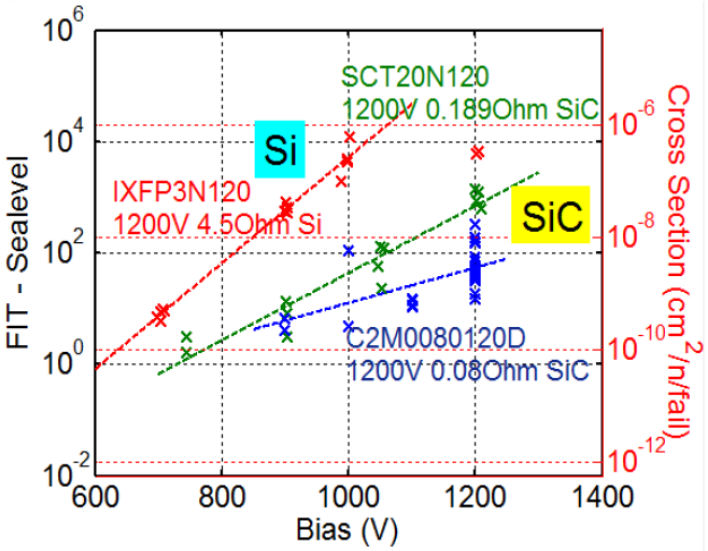


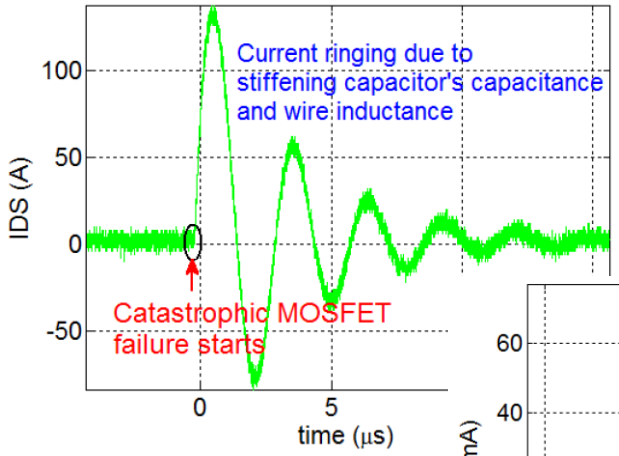
The SiC power MOSFETs test result at Los Alamos Neutron Science Center

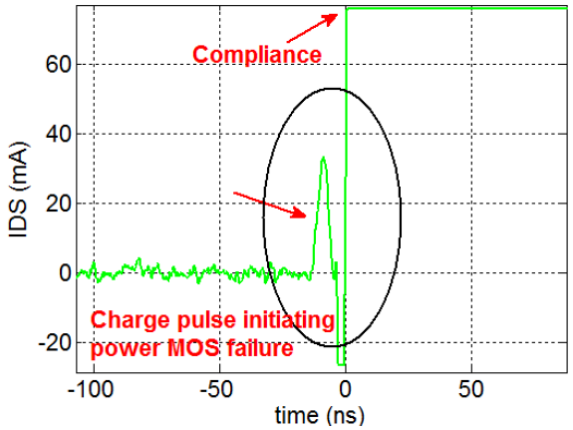
Akturk, A., R. Wilkins, J. McGarrity, and B. Gersey. "Single event effects in Si and SiC power MOSFETs due to terrestrial neutrons." IEEE Transactions on Nuclear Science 64, no. 1 (2016): 529-535.

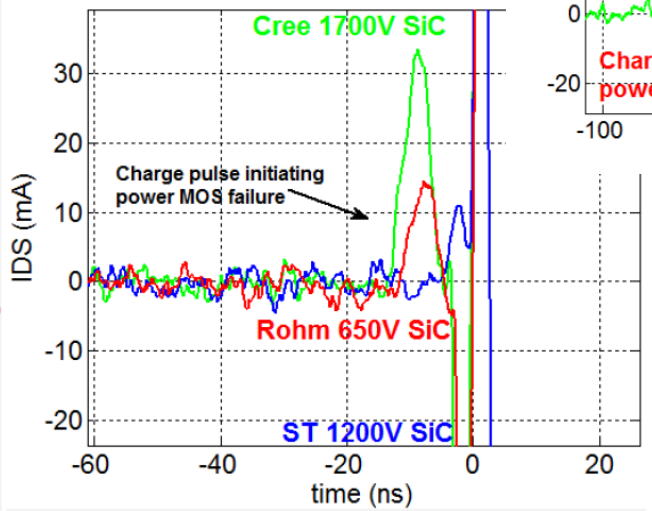
전력반도체 중성자 SEE 평가 자료 2











Neutron induced single event transients and the determination of critical charge to failure.

Akturk, A., R. Wilkins, J. McGarrity, and B. Gersey. "Single event effects in Si and SiC power MOSFETs due to terrestrial neutrons." IEEE Transactions on Nuclear Science 64, no. 1 (2016): 529-535.

06

단일이벤트여기 평가 특이점

ISO26262가 정한 메모리 결함평가 사항

Element	Fault models
FLASH (NAND, embedded)	stuck-at, additional fault models[a], **soft error model**
ROM, OTP, eFUSE	stuck-at, additional fault models[a]
EEPROM	stuck-at, additional fault models[a]
Embedded RAM	stuck-at, additional fault models[a], **soft error model**
DRAM	stuck-at, additional fault models[a], **soft error model**

a For example, Stuck-open Faults (SOFs), some kind of coupling faults. Based on memory structure, for example, addressing faults (AF), addressing delay faults (ADF), Transition Faults (TFs), Neighbourhood Pattern Sensitive Faults (NPSFs), Sense Transistor Defects (STDs), Word-line Erase Disturb (WED), Bit-line Erase Disturb (BED), Word-line Program Disturb (WPD), Bit-line Program Disturb (BPD). These fault models are for RAM but it can be shown that the same fault models are also valid for embedded FLASH or NAND FLASH, even if caused by different phenomena (see References [48], [49] and [50]).

ISO 26262 표준 참고 ISO 26262-11:2018 [5.1.3] Detailed fault models of memories

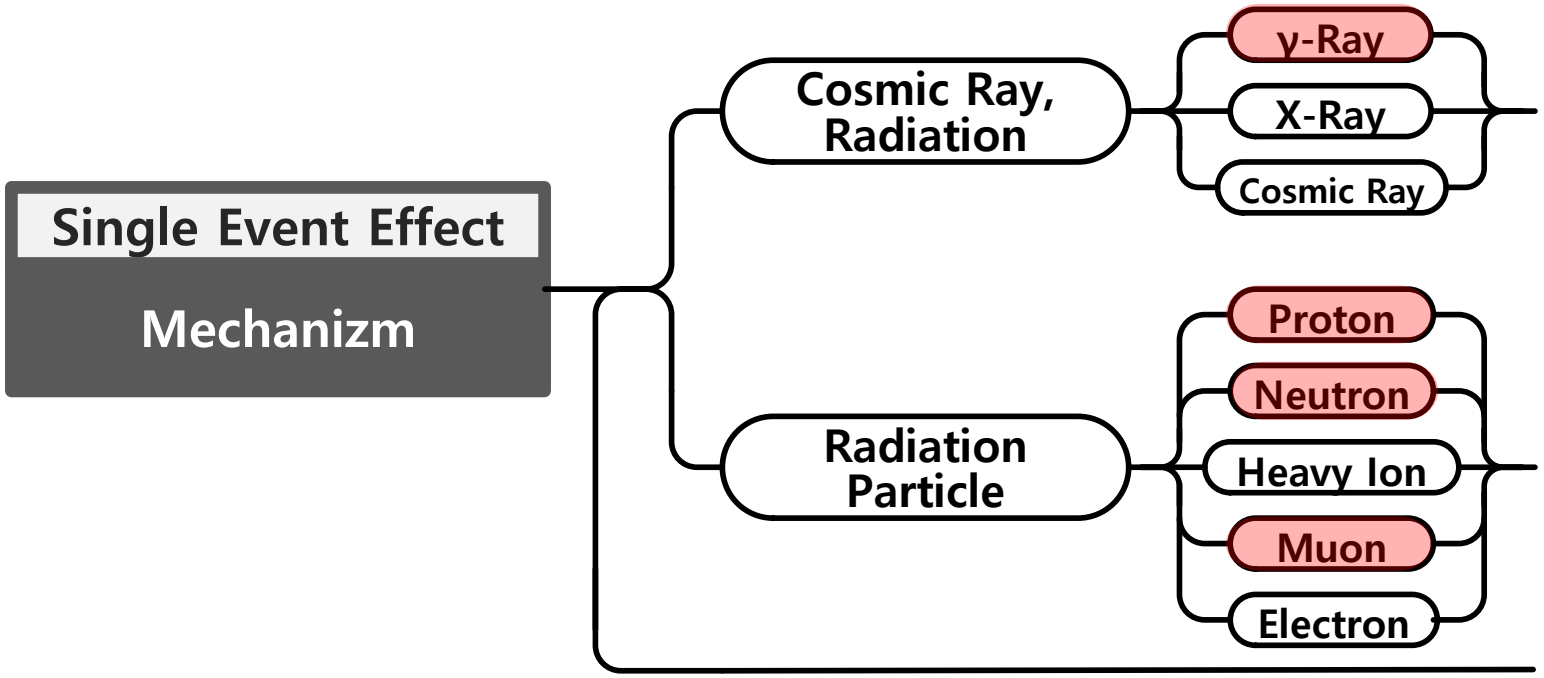
일반적인 SEE 종류와 효과

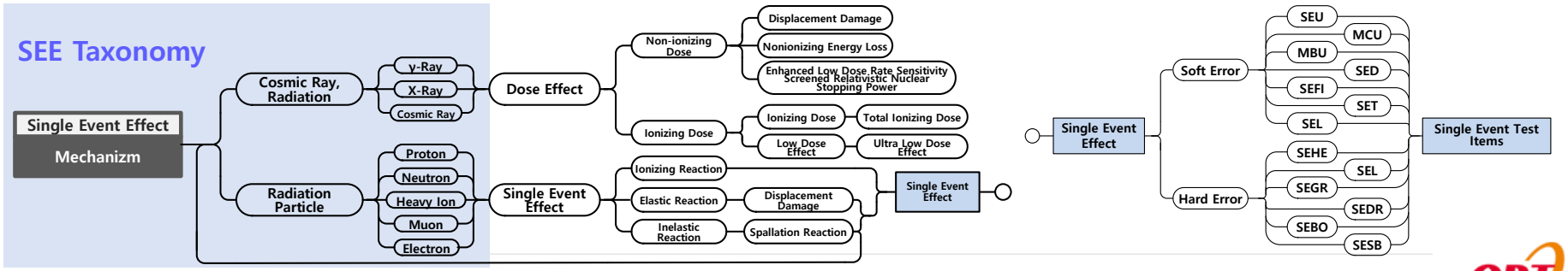
SEE Type	Effect	Affected Electronics
SEU	A single event upset, corruption of the information stored in a memory element	Memories, latches in logic devices
MBU	Multiple bit upset, corruption of several memory elements in a single hit	Memories, latches in logic devices
SEFI	A single functional interrupt, loss of normal operation	Complex devices with built-in state/control sections
SET	A single transient, impulse response of certain amplitude and duration	Digital, analog and mixed-signal circuits, photonics
SED	A single event disturb, momentary corruption of the information stored in a bit	Combinatorial logic, latches in logic devices
SHE	A single event hard error, unalterable change of state in a memory element	Memories, latches in logic devices
SEL(*)	A single event latch-up, high-current conditions	CMOS , BiCMOS devices
SESB(*)	A single event snap back, high-current conditions	N-channel MOSFET
SEB(*)	A single event burnout, Destructive burnout	Bipolar junction transistors, N-channel power MOSFET
SEGR(*)	A single event gate rupture, rupture of gate dielectric	Power MOSFET
SEDR(*)	A single event dielectric rupture, rupture of dielectric	Non-volatile NMOS structures, FPGA, linear devices

Note: (*) = potentially destructive SEE-types, NMOS = n-metal oxide semiconductor

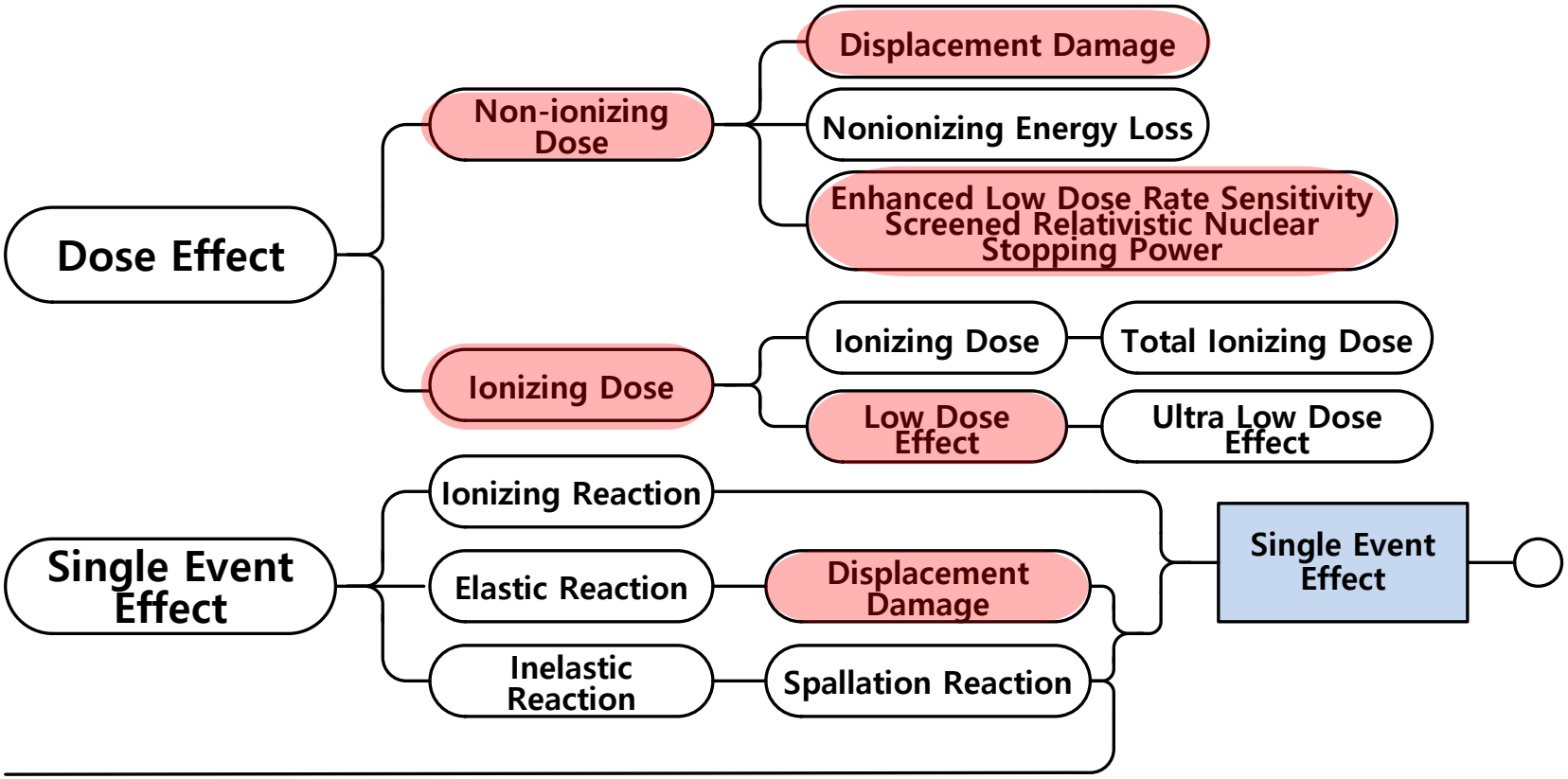
Single Event Effects Mitigation Techniques Report, DOT/FAA/TC-15/62. Federal Aviation Administration

SEE 분류 : DRAM과 SRAM의 예

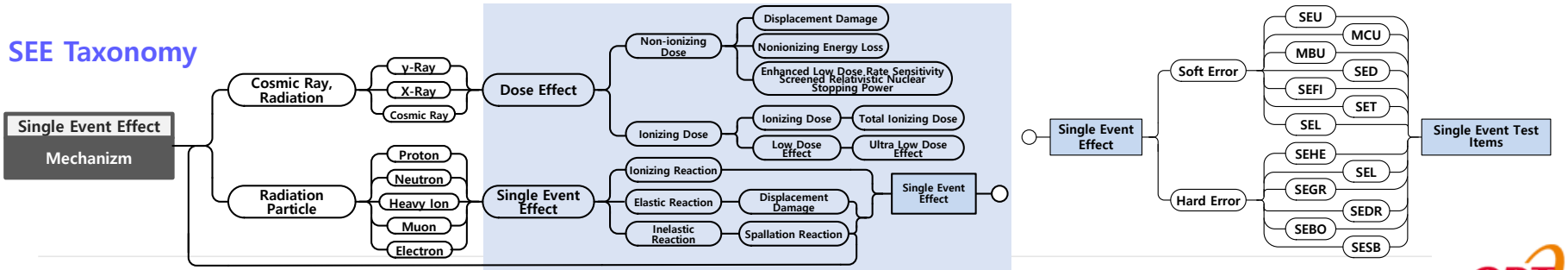




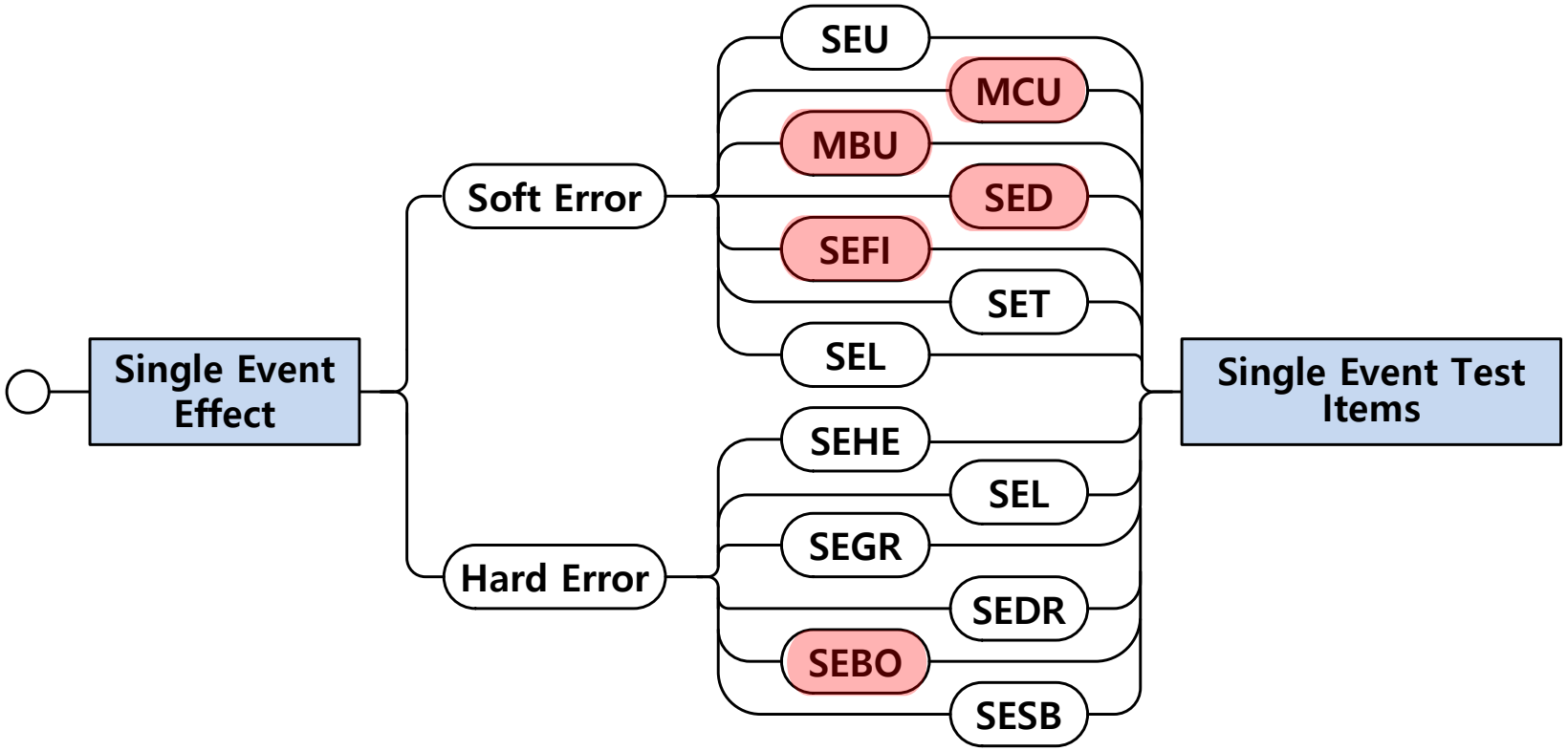
SEE 분류 – 선량 효과와 SEE



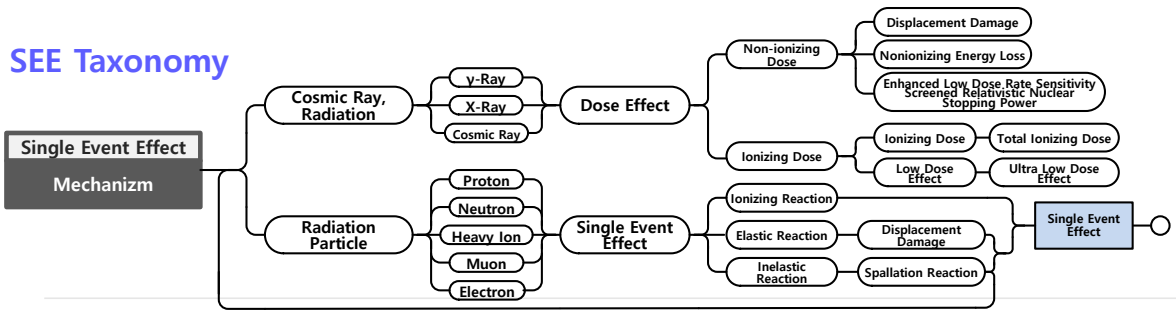
SEE Taxonomy

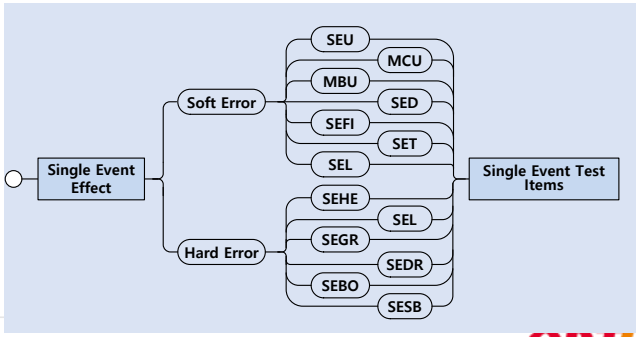


SER 평가 주목 항목



SEE Taxonomy





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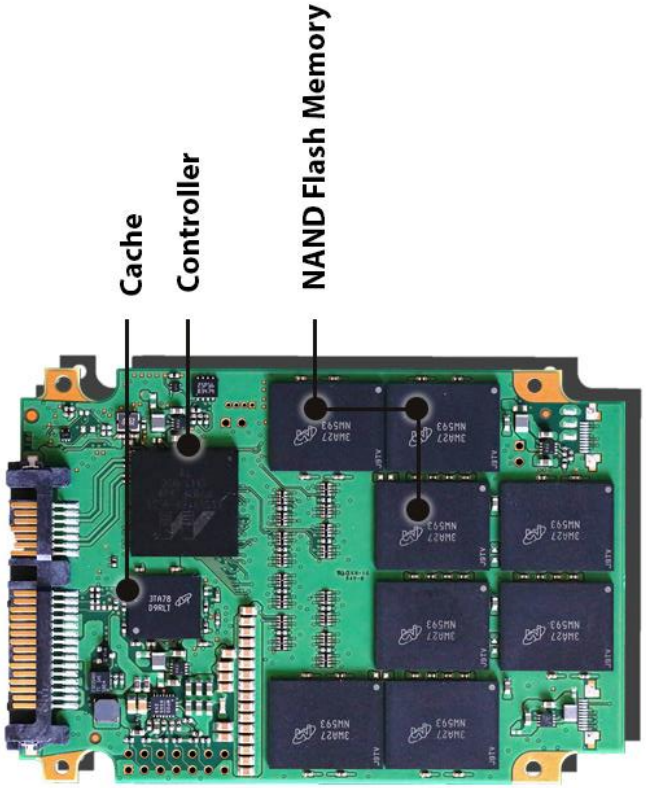
최근 반도체의 단일 이벤트 현상 평가

Flash/SSD 소프트 에러 평가

- **평가 대상 소자**
  - SSD: PCIe, SATA, NVMe, eMMC,
  - Flash: SLC, MLC, TLC, QLC
  - Controller: SoC, µC, DRAM, embedded SRAM
  - SW, Firmware Performance:
    - Performance measurement, error handling



- **평가 항목**
  - Soft Error: SBU, MCU, MBU, SEL, SESB
  - Undetected Error: SDC (Silent Error), UBER (CBER)
  - Hard Error: SBHE, MBHE, Broken program/erase circuits
  - Parametric Error: HCE
  - Block Error: SEFI, ADF
  - Functional Error: Read/Write Error
  - System Error: Hang, Brick
  - ECC Effectiveness, Row Hammering Dependency, TID Dependency

Flash/SSD 소프트에러 평가 및 분석 예

- Init, Control, R/W, P/E을 기본으로 한 평가 알고리즘은 아래의 일반적인 검출 확인 방법을 적용하여 구성
  - 실시간 Expected와 Actual 값 비교
  - 오류 감지후 최근 R/W, P/E 중 R 혹은 R/W 반복, Expected와 Actual 값 비교
  - 전원 전압 비교, 전원 사이클 제외한 복원기능 시행 후 오류 재확인
  - 오류가 지속될 경우, 전원 사이클후 평가 알고리즘 재시작

- 에러 징후에 따른 개별 알고리즘별 에러분석

●: 항상 가능, ○: 가끔 가능

SEU Type	Fault Location			Recovery				
	Cell	Control Logic	Function	Retry	Reset	Initialize	Power Cycle	Never
SBU, MCU	√			●	●	●	●	
MBU	√	√	√	●	●	●	●	
SEL, SESB	√	√			○	○	●	
SDC	√			○	○	○	●	
SEFI, ADF		√	√		○	○	●	
HCE		√				○	●	
SBHE, MBHE	√	√						●
R/W Error		√	√	○	○	○	●	
Hang,		√	√			○	●	
Brick		√	√					●

최신 소자의 소프트오류 평가 챌린지

Device Type	Test Method	Error Detection	Error Masking Things to watch
SRAM	a. R/W Test Algorithm b. Reset, Init c. Power Cycle	a. Compare Actual to Expected b. Error Recovery c. Function Recovery	• None to few • SED is new • Need smart algorithm
DRAM	a. R/W Test Algorithm b. Reset, Init c. Power Cycle d. Check T_{ref}	a. Compare Actual to Expected b. Error Recovery c. Function Recovery d. Shmoo T_{ref}	• Few to many • Need smart algorithm • Need parametric test • Dose Effect indirectly from Neutron
Flash	a. R/W Test Algorithm b. Reset, Init c. Power Cycle d. Check Current e. Check Time Delay f. Check hang clash	a. Compare Actual to Expected Undetected error a. Error Recovery b. Function Recovery c. Excess Current d. Performance	• Many including undetected parametric change • FG damage is complex to quantify • Need complex algorithm • Need parametric test • Long term Dose Effect from Neutron • Measure time delay is crucial
SSD	a. R/W Test Algorithm b. Reset, Init c. Power Cycle d. Check Current e. Check Delay f. Check Integrity	a. Compare Actual to Expected Undetected error a. Error Recovery b. Function Recovery c. Excess Current d. Performance e. Check Recovery from Hang and Crash	• Many including undetected parametric change • Need complex algorithm • Need parametric test • Long term and gradual Dose Effect • Must measure delay • Check Brick and Recovery
SoC, SiP, AI Device	a. Divide and Concur b. R/W Test Algorithm c. Benchmark Suite d. Diagnostic e. Functional Test f. Reset, Init g. Power Cycle	a. All SSD issues b. Wrong execution c. SDC d. Crash e. Hang	• Many maskings are possible • Derating is very difficult • ACE, FVF, SVF analysis • Device Specific

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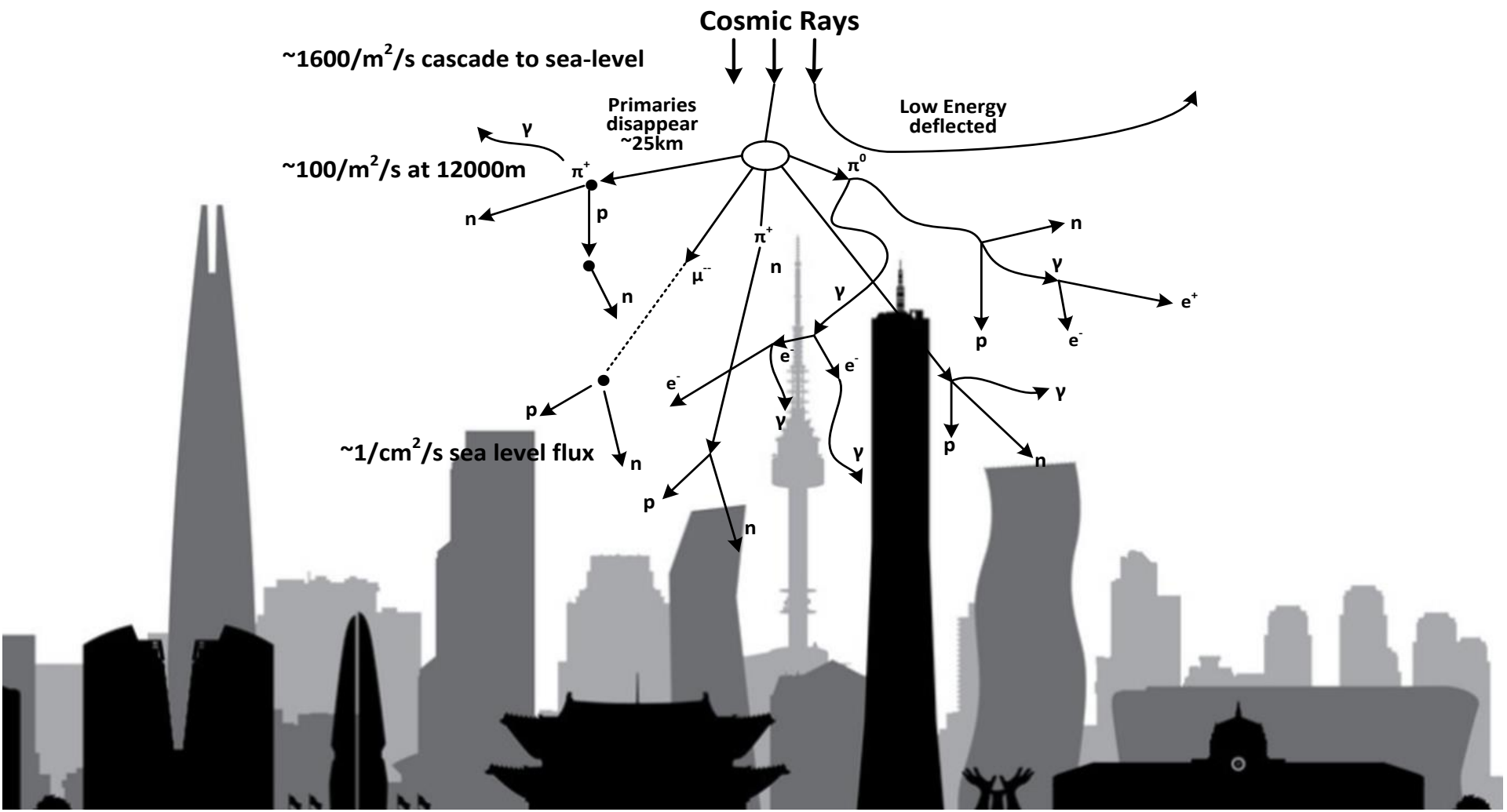
마 치 면 서

마치면서

- **SRAM, DRAM**
  - 가속 중성자 평가는 쉬운 편
  - DRAM은 TID에 대한 새로운 평가방법과 경감 기술이 요구
- **Flash, SSD**
  - 새로운 평가 방법과 자료 분석에 대한 요구가 증가
  - 계속적으로 신뢰성 (Extrinsic) 향상이 필요하며 이를 위한 새로운 평가와 분석기술이 요구
  - 새로운 기능 및 지구력 평가기술이 요구
- **전력 반도체**
  - SEBO, SEGR, SEL, SED과 같은 파괴성 에러 분석 기술이 요구
  - GaN, SiC, IGBT 모두 ISO 26262의 전기 자동차 산업 필수 신뢰성 (Extrinsic) 향상이 요구
- **ISO26262 자동차 기능안전 표준 지원**
  - 다변화된 반도체로 인해 지원을 충족할 저변 기술 미비
  - Fabless 중소기업을 위한 SoC, SiP, μP, μC 평가 지원이 절실

Q & A


Cosmic Rays
~1600/m²/s cascade to sea-level
Primaries disappear ~25km
Low Energy deflected
~100/m²/s at 12000m
~1/cm²/s sea level flux
γ
π+
π0
n
p
μ--
e-
e+