EE714 Final Exam (2018 Spring)

1. (10pts) In the design requirement, the maximum capacitance of a bitline of an array subsytem is 2 fP. If the subsystem has both 16 bit addresses and 16 bit I/O, decide how many address bits are used for a column decoder. Assume that the capacitance of a bitline is 10 fP without a column decoder.
   Grading: 10/2=5, 3bit (10)

2. (10pts) Draw both a transistor-level SRAM cell and the wave forms of write of '0' when the cell stores '1'. Also, discuss the sizes of all transistors.
   Grading: ckt(2), waveform(5), size(3)

3. (10pts) Design both a SRAM column conditioning and a large signal read SRAM circuit including operational wave forms.
   Grading: precharging ckt(3), read buffer(2), waveform(5)

4. (10pts) Design a low-power small-signal sense amplifier and then discuss its operations.
   Grading: circuit (6), operation (4)

5. (10pts) Explain the detailed steps for DRAM refreshing including whys and hows.
   Grading: why (2), how(8, refresh cycle, refreshing steps)

6. (10pts) Design a pseudo-nMOS 3x8 decoder from logic level to transistor level including size information.
   Grading: logic level(3), circuit level(4), size (3)

7. (10pts) Design a 2x2 CAM subsystem and its conditioning circuits at the transistor level. Also explain its operations.
   Grading: a CAM cell(2), architecture(3), conditioning circuits(3), operations (2)

8. (10pts) Design a ROM subsystem at the transistor level which implements 3^n table (0 <= n <= 4).
   Grading: function (3), cells (4), other circuits(3)

9. (10pts) Draw the equation of the threshold difference at the flash memory cell.
   Grading: max. (10)

10. (10pts) Design the one bit circuit of a four-word NAND flash memory cell and explain how to program and read the third word line.
    Grading: circuit (4), program (3), read (3)

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