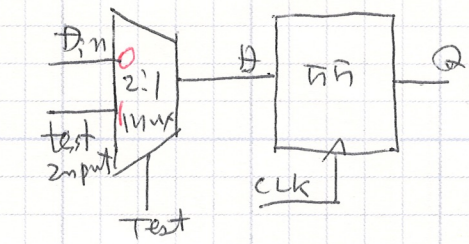
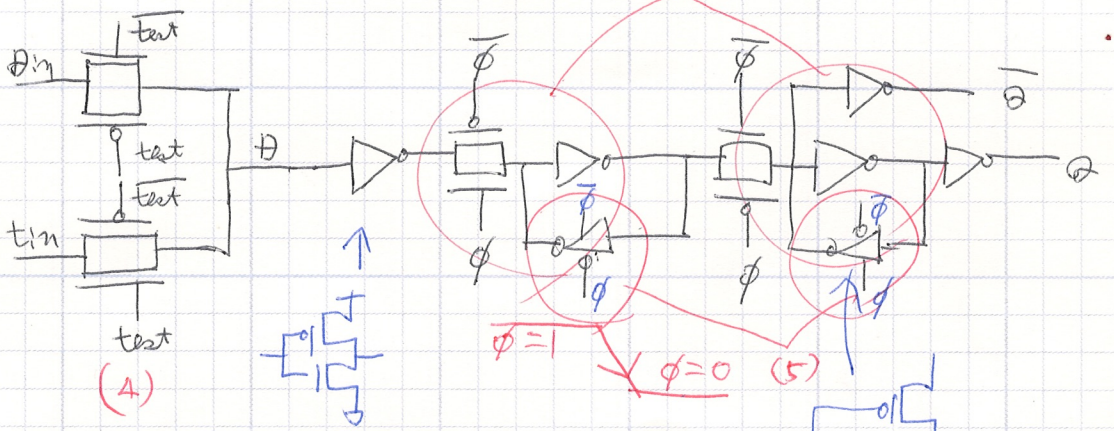
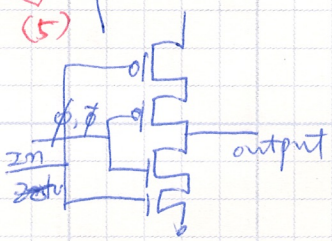
EE716 Midterm Exam

1. (10) "Synthesis of RTL", (5) since the netlist consists of the cells in the library (5)

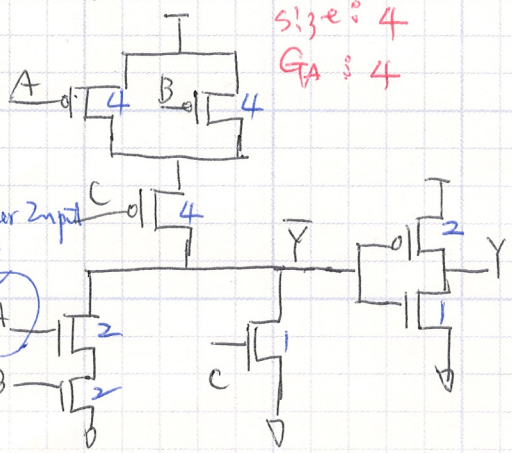
2. (14)





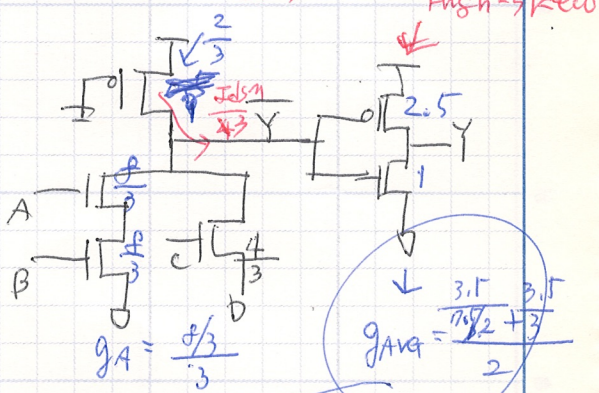


3. (36) CMOS (12) ckt: 4, size: 4, G_A: 4



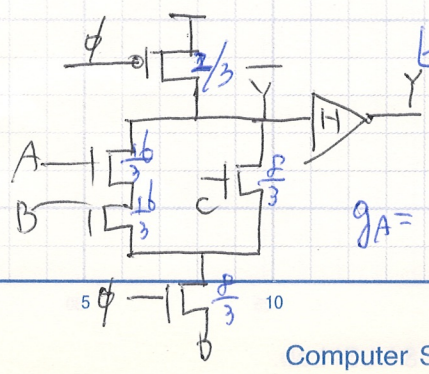
$G_A = \frac{6}{3} \cdot \frac{3}{3} = 2$

pseudo-nMOS (12)



$G_A = g_A \cdot g_{AVG}$

Domino Logic (12)



$g_A = \frac{16/3}{3} \Rightarrow G_A = g_A \cdot g_{AVG}$

4. a) ~~Inv~~ : $t_{hold} - t_{ccq} + t_{skew} = 25 - 30 + 50\,ps = 45\,ps$ (10)

b) ~~Two~~-phase Latch : $t_{hold} - t_{ccq} - t_{nonoverlap} + t_{skew}$ (10)

$= 25 - 30 - 40 + 50 = 5\,ps$

c) pulsed Latch : (10)

$t_{hold} + t_{pw} - t_{ccq} + t_{skew} = 25 + 60 - 30 + 50$

$= 105\,ps$

5. (10) $\frac{T_c}{2} - (t_{setup} + t_{nonoverlap} + t_{skew}) = \frac{500}{2} - (20 + 40 + 50) = 140\,ps$