EE 716 Digital IC Design Term Project

2019, Fall

Prof. Jinsang Kim

In this project, we design a digital IC chip using standard cell-based front-end and back-end Synopsys CAD tools. The CAD manuals can be downloaded from the KLAS website. The starting point is to write or use a Verilog HDL model. You may use the existing Verilog codes at your lab or download or write them by yourself. **But you should understand all the codes and cannot use Verilog codes used for previous MPW projects or projects done in this class.**

1. For this project, each student does his/her own project. The minimum design complexity is 40K gates/student.
2. The following should be included, but not limited
   A. Should explain the algorithm of your design and draw the functional block diagram.
   B. Do RTL synthesis and analyze performances such as the number of gates, timing and power consumption.
   C. Do floorplaning the chip and P&R and add IO pads.
   D. Write the report, present, and demonstrate your design including
      i. Algorithm & architecture
      ii. Verilog HDL codes
      iii. Your design methodology from the front-end to back-end
      iv. The experimental result and analysis at each step of your design methodology
      v. Datasheet of your design
   E. Each student should show me that he/she knows all the steps for this design.
   F. A sample FFT Verilog code will be given so that you can finish all the details steps. Also, you should report the exercise report including results and analysis of all the intermediate (interchange formats) files of each step as possible.
3. Important dates: upload at KLAS website
   A. 11/04/2019: design proposal (team leader only), each team: max. 4 members.
   B. 11/11/2019: exercise report using the sample FFT codes (all the students, individual report).
   C. 11/25/2019: intermediate report (team leader only) of the front-end design.
   D. 12/09/2019: Submit the final report and all sources (zipped) at the KLAS website.
   E. 12/10/2019: demo and final presentation.