ASTRO P&R
USER GUIDE

2017. Fall

Kyung Hee University
CSA&VLSI Lab

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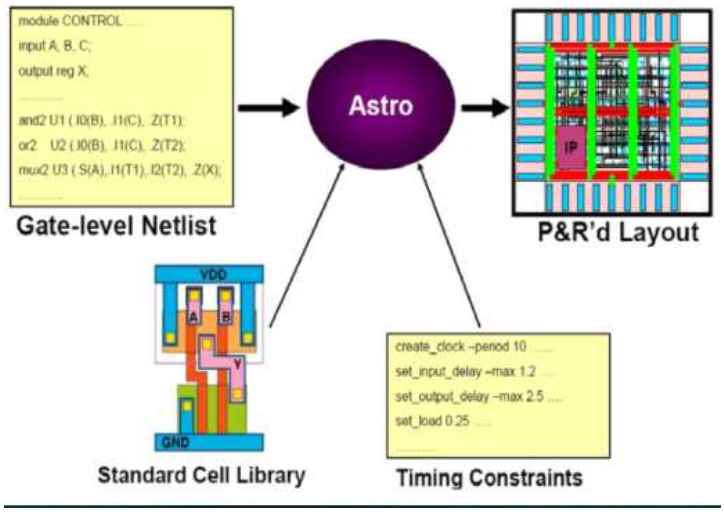
Introduction to the Astro P&R Tool

※ ASTRO functions and roles



※ Standard Cell Library?

- A Standard Cell is a pre-designed layout of one specific basic logic gate.
- Each cell has the same height.
- A Standard Cell Library has a variety of standard cells
- Libraries are provided in the ASIC vendor library group.

※ Place and Routes?

- Layout has three types of reference cells: Macro cells (ROMs, RAMs, IP vlocks), Standard cells (nand2, inv, dff, ...) Pad cells (input, output, Vdd, Vss pads)
- There is a floorplanning stage to locate Macro and Pad cells prior to placement and routing
- Location of all Standard Cells is automatically determined according to routability and timing during placement.
- Pins are physically connected during routing.

※ Astro Input / Output Files

- Input Files

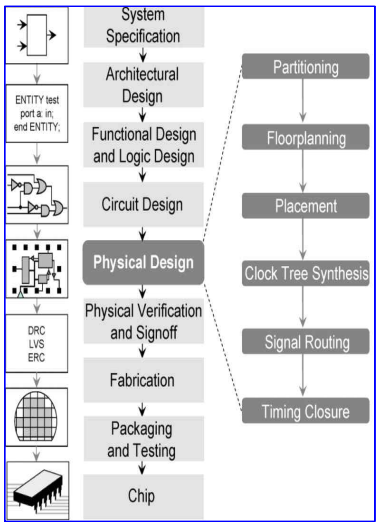
File type or format	File content
Technology .tf	Design rules, net resistance and capacitance, units of measurement.
GDSII	Physical layout information.
Synthesis library .lib or .db	Cell timing and functionality. For information about using .db, see the application note.
Verilog netlist .v, VHDL netlist .vhd, or EDIF netlist .edf	Connectivity information.
Timing constraints .sdc	Timing constraints, clock definitions.
Design .def or .pdef	Floorplan information, including core size, placement sites, port locations, RAM locations, and routing and placement obstructions.

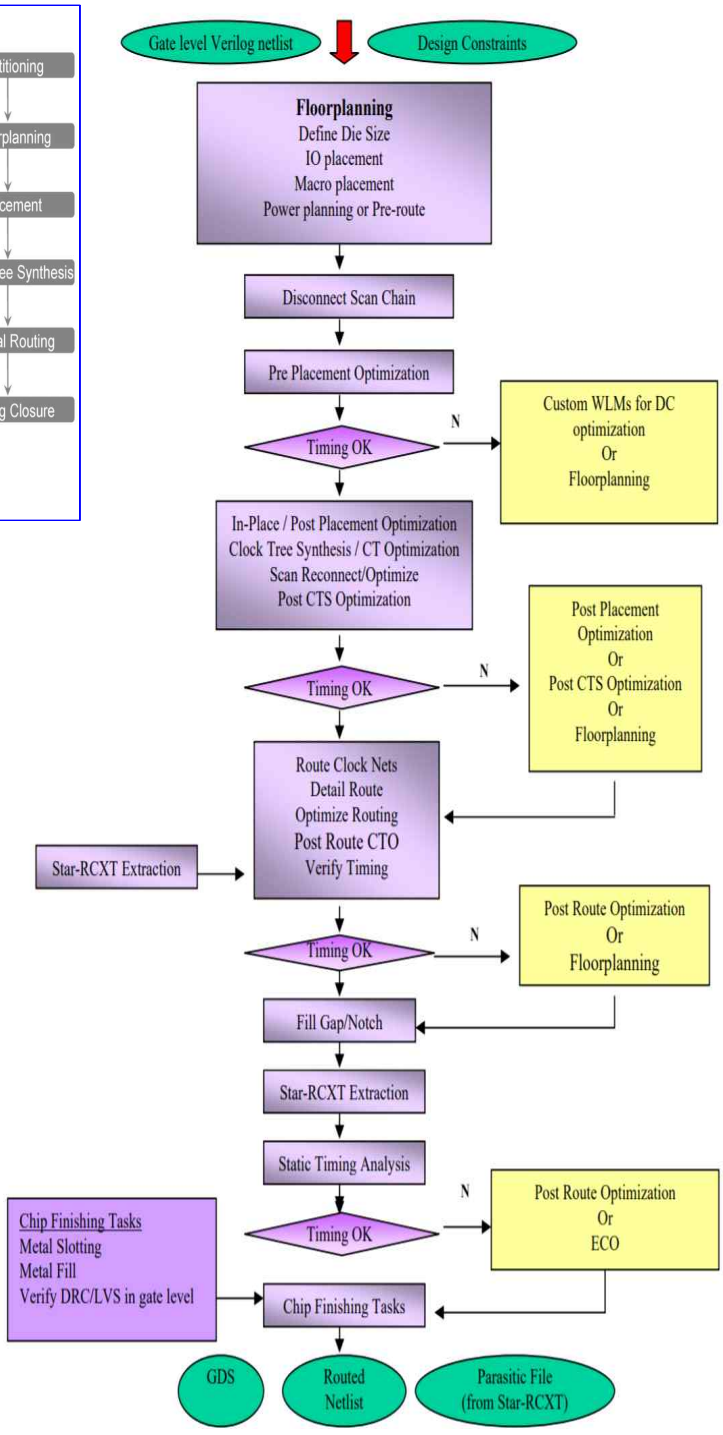
- Output Files

2

File type or format	File content
Design .sdf	Post-floorplanning timing
Parasitic .spef or .spf	Parasitic information
Verilog .v (flattened) or .hv (hierarchical)	Optimized netlist
GDSII	Updated physical layout information
(Optional) Updated design .pdef	Cell placement locations
(Optional) Updated design .def	Netlist and floorplan (cell placement) information

※ Astro Design Flow





Required files for P&R: .v (netlist file), .sdc (constraint file), .tdf (pad location information file), The process providing library (L18CB.zip)

1. Run Xshell 3.0 and connect to the server IP with your account
2. Assume that Astro's license and path settings are completed.
3. Create a directory to perform Astro tasks: mkdir directory name + ↲ (Enter)
   ex) mkdir [folder name] + ↲ (Enter)
4. Copy and unpack the library provided by the process **(you may skip this!!)**: When installing the process library, be sure to understand the installation method provided by the library. And the library can not be partially copied.
5. The tdf file (provided in the process) to determine the location of the input and output pads and prepare TECH file (included in the library by default) using techgen. Copy the converted file to the following path: samsung/Prim_phantom/TEC

※ The reason for converting the TECH file is to match it when the number of metals in the TECH file is different.

6. Create a folder called design_data in the working directory to run Astro. In this folder, copy the synthesized netlist and sdc files through the design compiler.
7. Go back to your working directory to run Astro again and run the Astro command
   ※ Astro &
9. If ASTRO is running normally, you will see the screen shown in Figure 1. If you see a warning about the license, you can close the Astro window and fix the license problem.

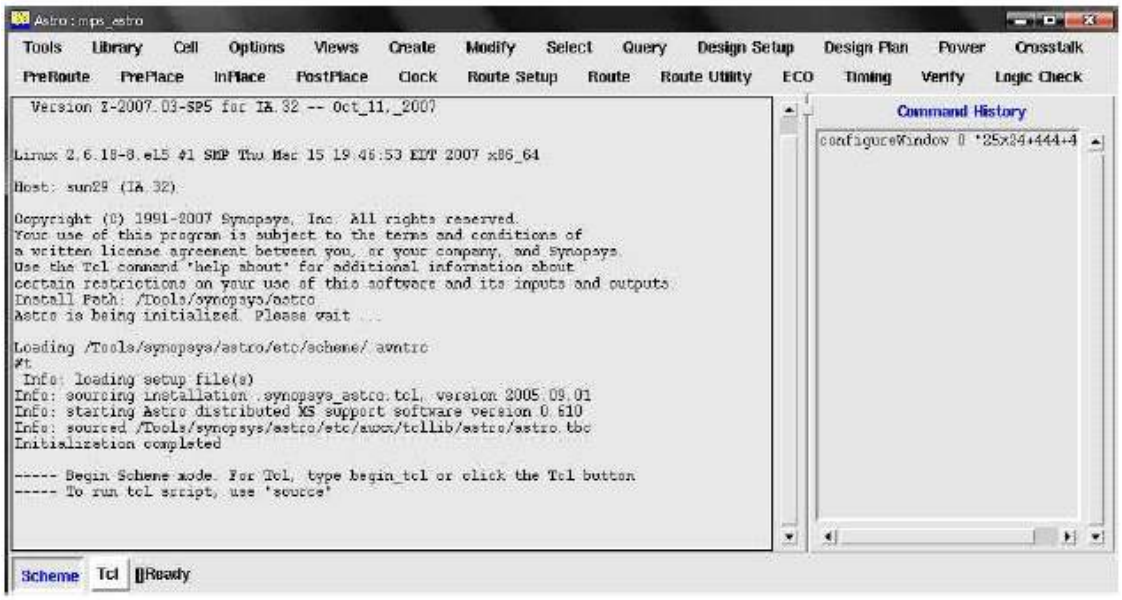


Figure 1. Normal Astro run screen

Lab1. Design and Timing Setup

1. Select **Tool -> Data Prep** to make the "Data Prep" pull-down menus visible
2. Select **Netlist In -> Verilog To CEL** ...

: This is the first step in creating a CELL for P &R using the netlist file generated by the design compiler and the process library and TECH file.

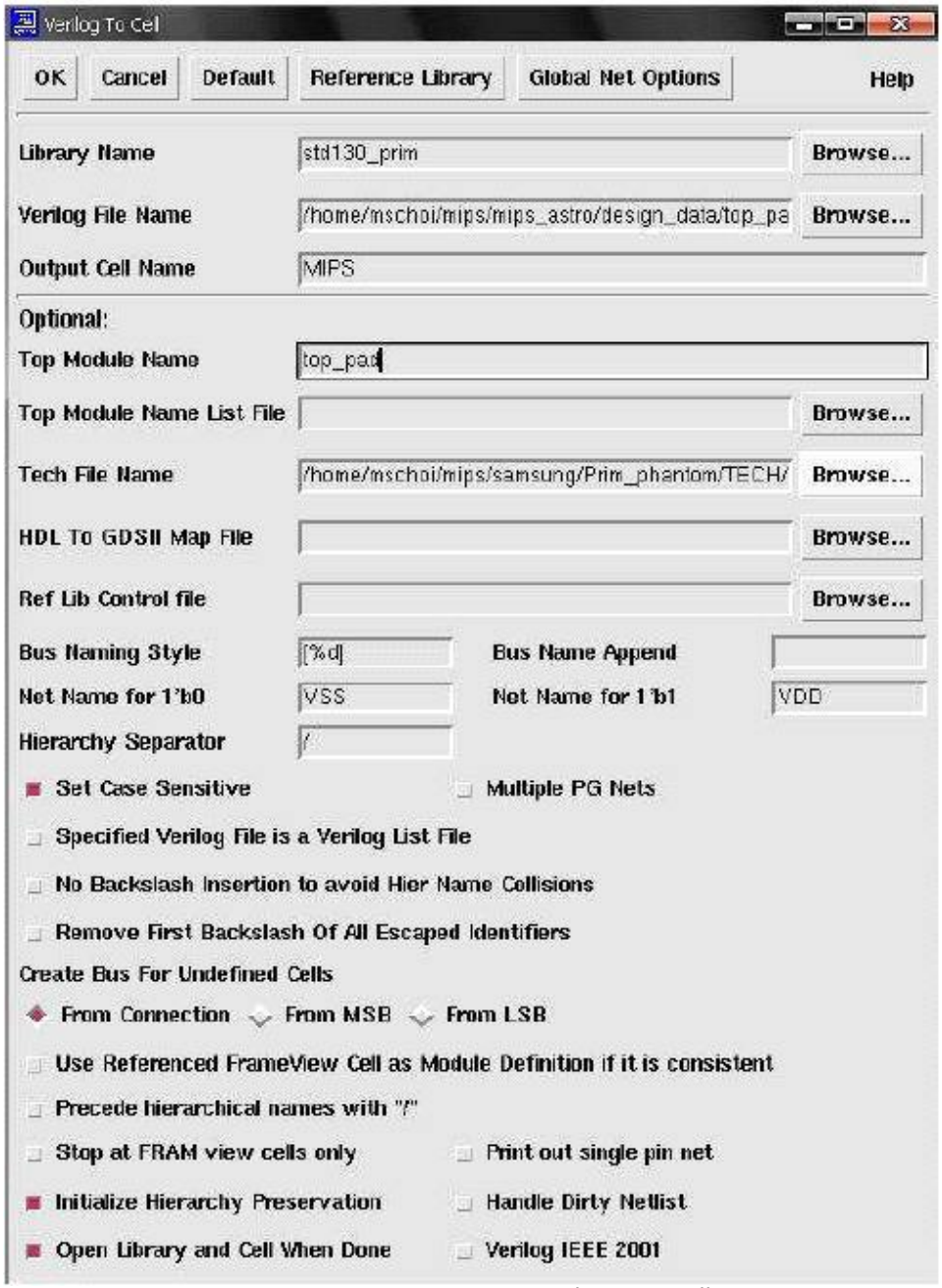


Figure 2. Verilog To Cell

2.1 Library Name

Create Directory to do P &R tasks. Save all the output files of the P &R work here.

2.2 Verilog File Name

Set file location (use Browse ...) to load the design's gate-level netlist
/home/Enter your account /mips/mips_astro/design_data/top_pad.v

2.3 Top Module Name

Top module name in Design
For example, the top module name for mips is top_pad.

2.4 Tech File Name

Provide the technology file (.tf file) provided by the process.
/home/your account /mips/samsung/Prim_phantom/TECH/std130_prim_4m_v2.techgen.tf

2.5 Reference Library

Set the location to load the Reference Library for the created Memory Cell compiled in memory compiler and Cells (standard cells, I/O cells) provided in the process.

Select Reference Library button. -> Browse ... (select corresponding Cell and Memory Lib)

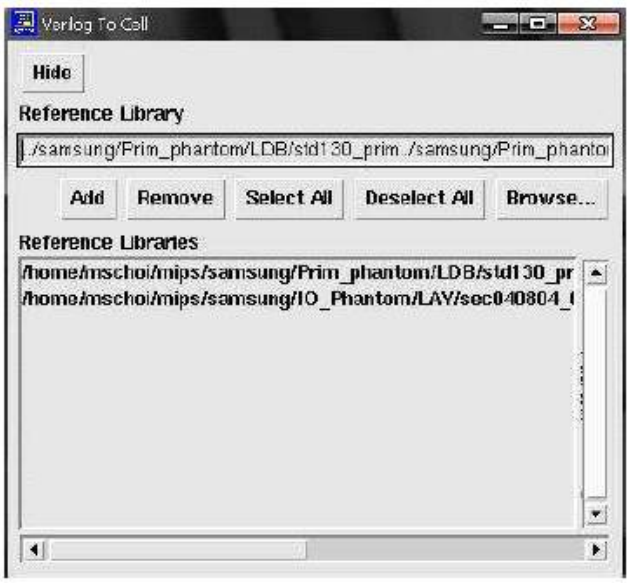


Figure 3. Reference Library

If you have added all the libraries, press the Hide button and exit.

2.6 Global Net Options

This is the step to set the global power/ground of the chip. VDD and GND are combined into one Global Net. For example, to set VDD, enter VDD in the Net Name and Port Pattern in Figure 4 and click Apply. t this time, Number Defined increases from 0 to 1. o the same for VSS (Ground).

Select Global Net Options button.

Net Name	VDD	VSS
Port Pattern	VDD.*	VSS. *

After inputting VDD and VSS as above, click Apply button. Mode must be set to Add.

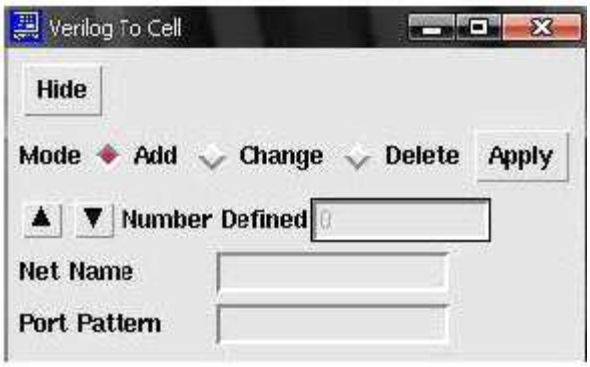


Figure 4. Global Net Options

※ Types of VDD / VSS

VDD/VSS: power supplied to core
VDDO/VSSO: Power supplied to pad
VDDQ/VSSQ: power supplied to the pad

In case of Samsung Lib, since VDDO and VDDQ are connected automatically when Pad filler is inserted, in this manual, we consider only VDD and VSS.

Ensure that the following options are ON.
- Set Case Sensitive
: When the option is not selected (default is selected), Astro will convert all names to uppercase which can lead to problems with other tolls downstream.
- Initialize Hierarchy Preservation
: This option is selected to preserve the logical hierarchy.
- Open Library and Cell When Done
※ Leave all other potions at their default setting.

When you are finished with **Verilog To Cell,** press OK to create the cell. Figure 5 shows a generated cell.

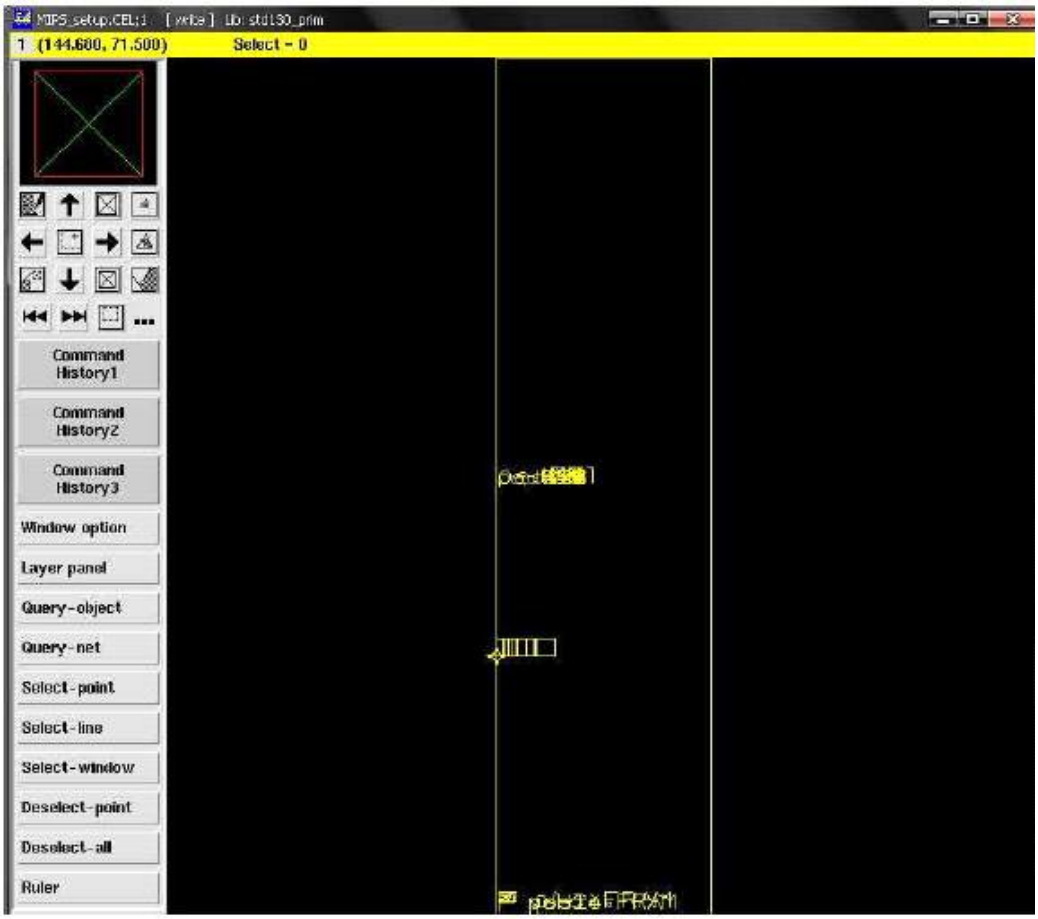


Figure 5. Cell output through Verilog To Cell

3. Select Cell -> Mark Module Instances Preserved ...

: Click the Default button.

Enter "Cell Name (MIPS)" for Flattened Cell Name

Click OK

This work is used to maintain the hierarchical characteristic of the logical level.

4. Perform a Timing Data Check

: Go back to the Astro menu set with: Tools -> Astro

4.1 Load the SDC file: Select Timing -> Constraints: Load SDC ...

* Must be removed from Astro SDC file

: set_area, wire_load, operation condition

set_ideal_network -> set_propagated_clock [get_clocks clk]

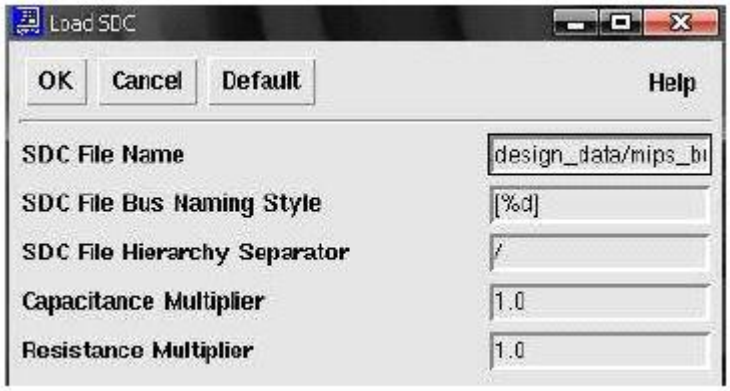


Figure 6. Load SDC

SDC File Name: Enter the path and file name of the SDC file and click OK button

4.2 Timing Data Check: Select Timing -> Astro Time: Timing Data Check ...
: This is the process of confirming that the netlist and SDC files are properly created.

5. Perform a Timing Sanity Check
5.1 Timing Setup
: Select Timing -> Astro Time: Timing Setup
5.1.1 Select "Model" tab: Change Net Delay Model Medium Effort to Low Effort
This will have no effect on the timing sanity check; it is, however, a recommended setting for pre-CTS optimization
5.1.2 Select the Environment tab: Turn the Ignore Interconnect option ON
Net delay is ignored because it is still before placement. This option must be converted to OFF after timing sanity check.
Turn the Ignore Propagated Clock option ON
Turn the Include Non Propagated Nets ON
: ignore Propagated clock and net since it is the process before CTS
<Refer to the reference figure>
5.1.3 Select the Optimization tab: Change Optimization Max Capacitance value 0
Change Optimization Max Capacitance value 0.
Change Optimization Max Transition value 0.
Ignore Max Capacitance and Transition values
and Apply.

Reference figure. Option in environment Pre-CTS

5.2 Generate a Timing Report

: Select Timing -> Timing Report ... -> Report Constraints: Max Trans and Max Cap ON -> Click "OK"

After execution, you can get the result shown in Figure 7.

Make sure that Setup / Hold / MaxTrans / MaxCap has (non-zero ?) slack.

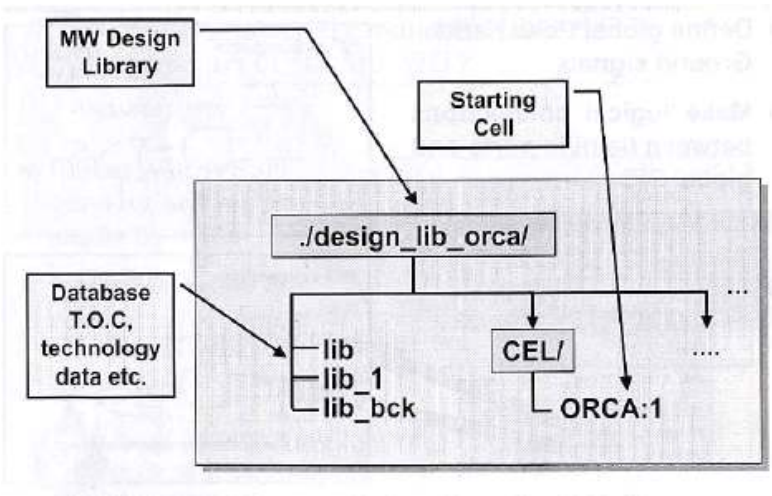
```
ASTSUM  Summary of timing analysis (w/o xtalk)
ASTSUM         Setup (Target=0.0000)          Hold          Num      Num
ASTSUM       Slack    Num      Total      Slack    Num  MaxTrans MaxCap
ASTSUM      16.264      0        0.0      0.115      0        0      0
@@@ Total CPU      Time =    0:00:04
@@@ Total Elapsed Time =    0:00:06
@@@ Peak  Memory  Used =  153.27 MB

Timing Report OK
```

Figure 7. Timing Report Results

6. Save the cell as Setup

Select Cell -> Save As ...

※ Astro Database structure



The structure of the Astro database is shown in the figure above. CELL converted
The MW Design Library is created in the working folder according to the Library name specified during the conversion process through Netlist to CEL.
There are lib_* folders in the generated MW Design Library, It is the generated directory for converted CELL from technology data After each Lab, when we save Cell using "save as", the corresponding file is stored in CEL folder.
When a P&R task is stopped due to computer malfunction, the corresponding Cell is changed to "Lock mode" from which we can not continue to work. In this case, go into the CEL folder inside the MW design library folder and delete the most recent file specified as .lock.

Lab2. Floorplanning

: Floorplanning requires a .tdf file provided by the process. TDF file is a file which contains the location information of the I/O pads.

1. Load the tdf file

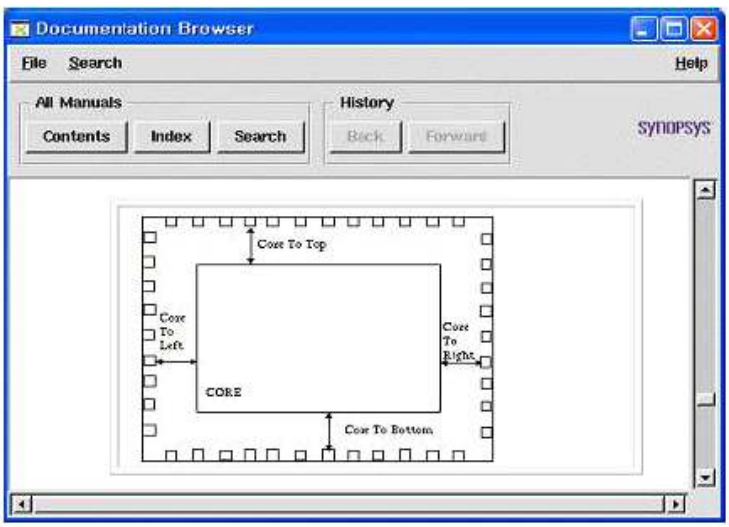
: Select Design Setup -> TDF: Load TDF ...
Leave the Cell Name field blank
Write the path and file name of the corresponding TDF file in the TDF File Name and click the OK button

2. Set up Floorplanning

: Select Design Setup -> Floorplan: Set Up Floorplan ...

Figure 8. Floor planning

To specify the core region directly (except for the pad cell), select the width and height of the Control Param. Then the disabled Core Width and Core Height are activated.
Then select Double Back, Start First Row, and Flip First Row. More about this, see Help in the upper right corner. (Row / Core Ratio must be set to 1)
Core To Left represents the distance between the core region and the left Pad. (See figure below)



You can specify this yourself. Consider size and fill in the appropriate size for each field. After pressing Apply, you can see the result of floorplan as shown in Fig. 9
(Core Utilization must be 0.6 ~ 0.65)

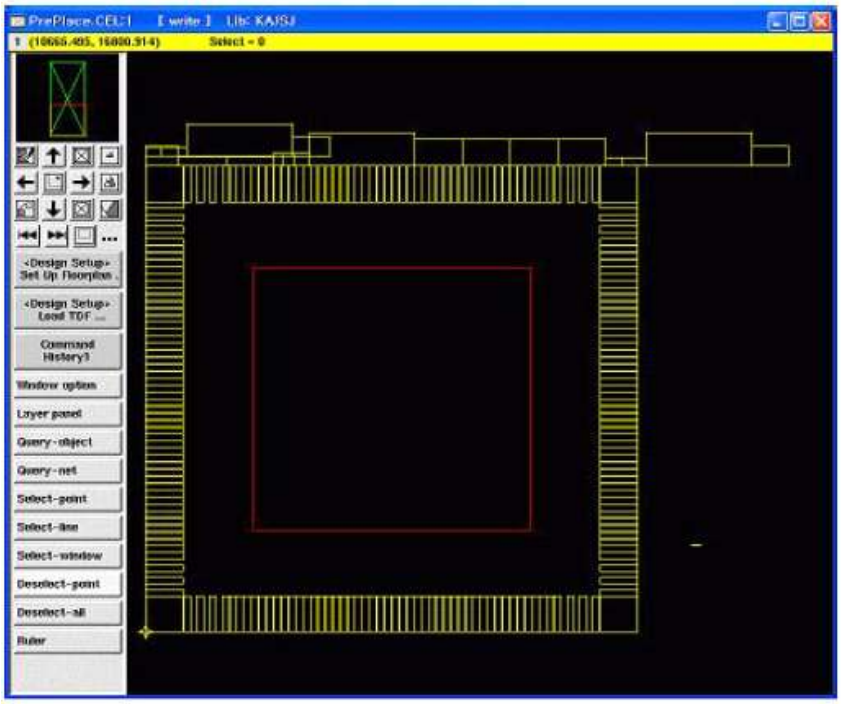


Figure 9. Floorplan Results

Adjust **Core To Left, Right, Bottom, and Top** properly to match the entire chip size and check the end point coordinates. Make sure that the end point coordinates match the size suggested in the PDK. Continue to adjust if it does not fit.

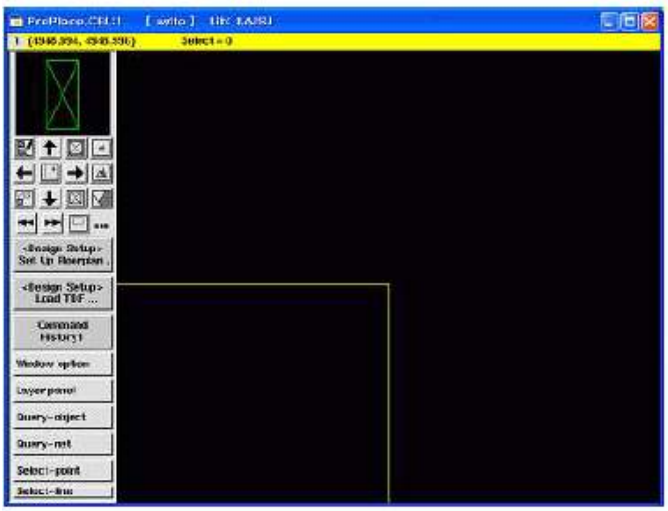


Figure 10. Floorplan endpoint coordinates adjustment

3. Insert pad filler

: Fill the blank space between the Pads with Filler insertion. In the Samsung Lib.,
Pad power line is connected in the PAD filler.
Select PostPlace -> Filler Cell: Add Pad Fillers ...
Write the filler name in order of largest to smallest. Then Astro will begin filling from llarge filler and fill small fillers in the remaining space to reduce the number of fillers.

4. Connection of Port Logical Power / Ground

: Performs a P/G connection on each logical port (not just a PAD).
Select PreRoute -> Connect Ports to P / G ...
Click "Default"
Select Pad to add to Cell Types
Select Update Tie Up/Down option: Convert logical connections to physical connections
4.1. Net Name = VDD
Port Pattern = VDD. *
Net Type = Power
Click Apply
4.2 Net Name = VSS
Port Pattern = VSS. *
Net Type = Ground
Click OK
// Make sure the pad is checked in the option

5. Place Macros

: Astro does not support automatic placement of Macro blocks (IPs), so manual placement is needed.
Queay -> Flyline: Show Net Connections ... Show connection info
"Ignore Connection to Standard Cells"
Modify -> Move ..
Directly using Modify -> Transform ..

6. Blockage

: The area is set so that other parts (blocks) are not placed on the specific area when the parts are placed.
Hard/Soft blockage: Hard blockage does not allow to place other parts in any case, Buffers may occasionally be included in Soft blockage.
PrePlace -> Placement Blockage Create Hard / Soft ...

7. Create Rectangular Rings

: All cells in the core can not be routed directly from the core power pad to get power. That's why the power ring should be made to provide power source to all cells in the core.

Select PreRoute -> Rectangular Rings ...

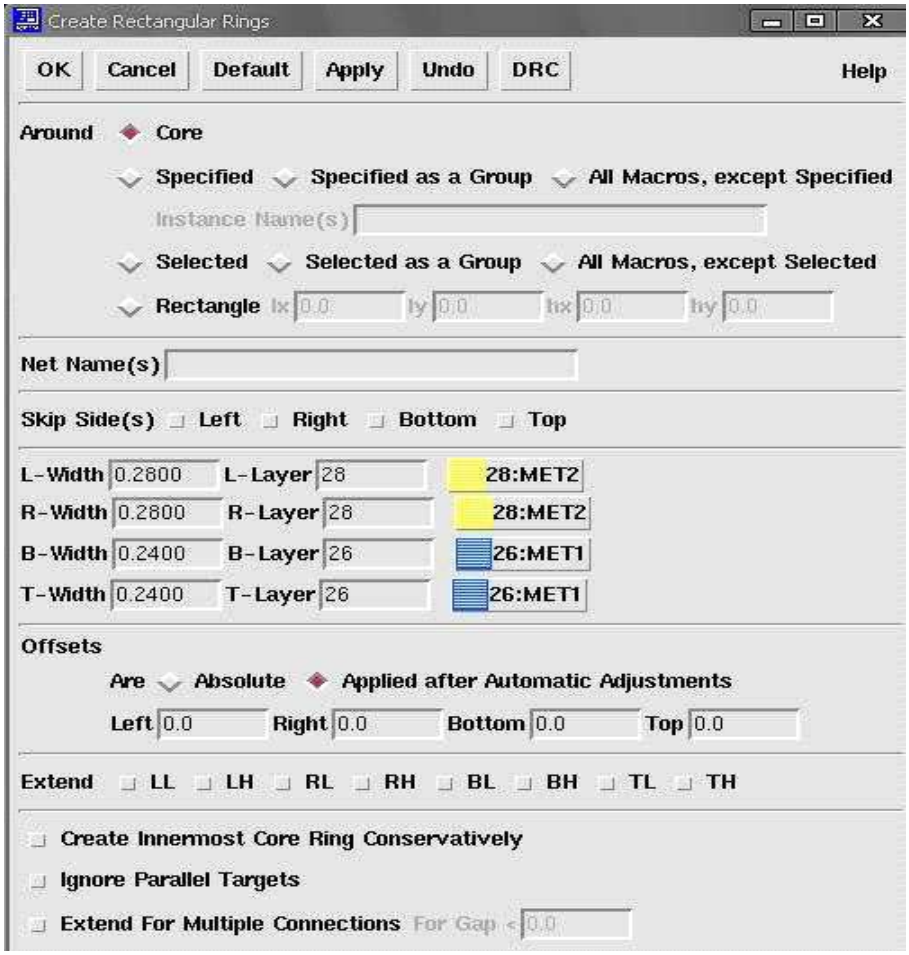


Figure 11. Rectangular Rings

Around: If you select Core (meaning you will create a ring around the Core)
Net Name (s): Enter the name of the P/G net you want to create (ex, VDD, VSS)
L/R/T/B: Power ring thickness setting
Offsets: Indicates the distance from the core.
※ For macroblock powering, select All macros, except Specified in the Around.

8. P/G Line Drawing

: Select PreRoute -> Custom Wires

In Figure 12, you need to adjust **Specify Nets** to **by Net Name** and enter the name of the **Power net** you would like to place on the **Net Name**. And write the desired thickness in the Horizontal Width, and Vertical Width menu. Then, in the Lay out window, click the button to draw a line. At the point you want to turn, click once on the left button. Then right-click where you want to finish drawing the line.

Please note, however, that horizontal and vertical metal should be used separately. If wrong, select line using Select Point and modify -> Delete in setting window in order to delete it.

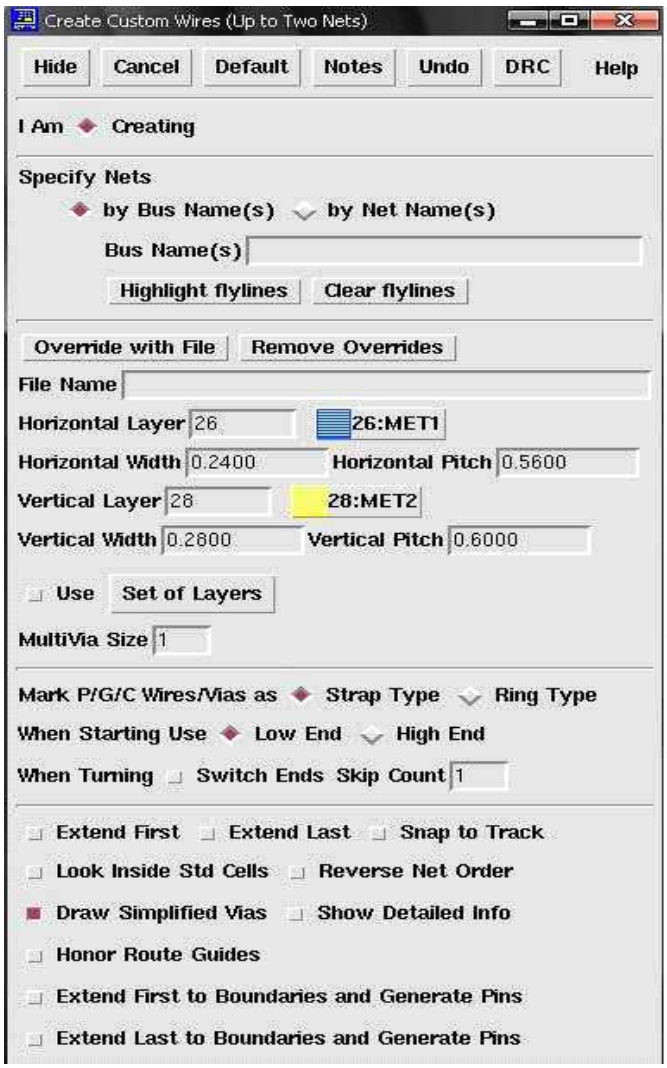


Figure 12 Custom Wires

9. Connection between power pad and core ring

: Select PreRoute -> Macros / PAds

Instance type (s): Select pad

Primary Routing Layer: Select Pin -> Apply

10. Pre Route the Standard cells

: Select PreRoute -> Standard Cells ...

Click Default

Select **Fill All Empty Rows option** (an option allows you to select a specified region only.)

Click OK

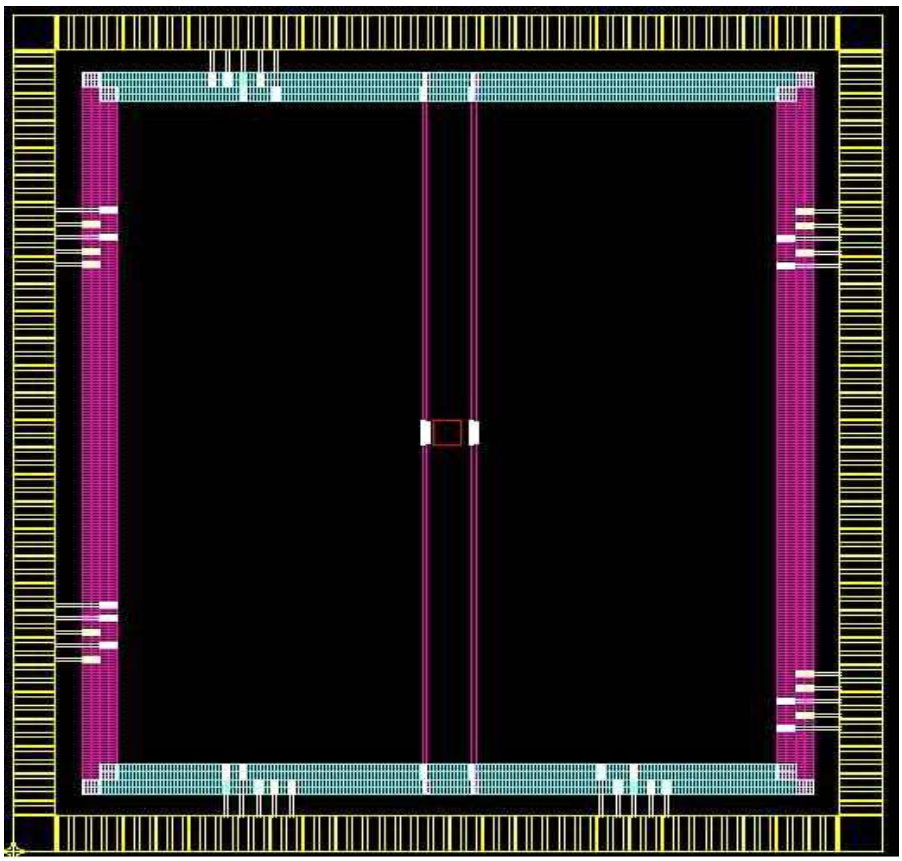


Figure 13. Completed Floorplan

11. Save the cell as Setup

Select Cell -> Save As ...

Lab3. Placement

1. Scan Chain remove

: Since the placement with scan chains can result in complicated connections, remove scan chain and perform optimization after CTS.

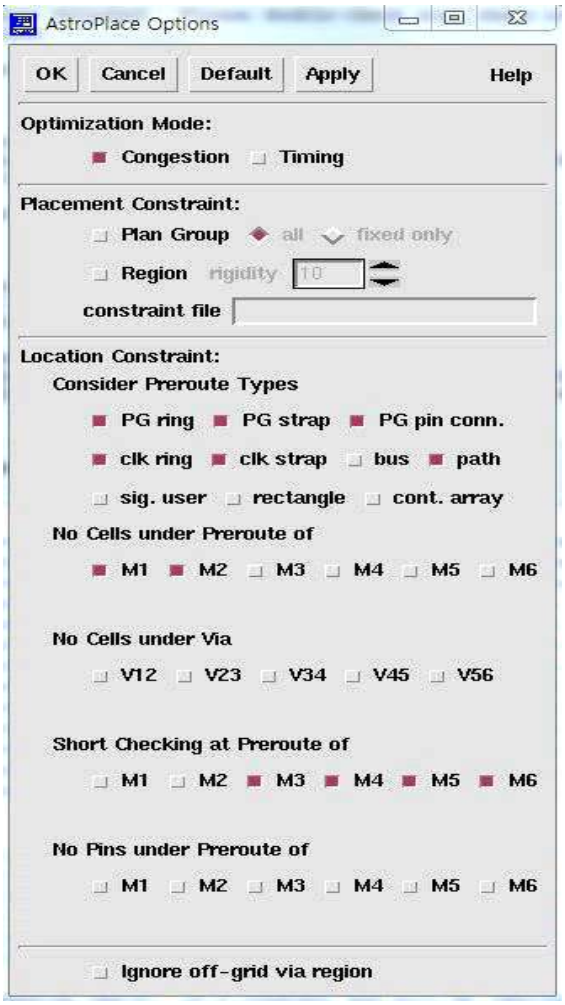
PrePlace -> ScanChain: Optimize / Delete Scan Chain ... mode: Delete only

2. set placement option

: Option settings for the Placement: InPlace -> Placement Common Options

No Cells under Preroute of: Do not add cells to metal for power

Short Checking at Preroute of: check shortage in other metals except power metals



3. Prototype Placement

3.1 Select Timing -> Astro Time: Timing Setup ..

Set Environment tab / Optimization tab / Model tab as shown in Fig. 14, 15, 16

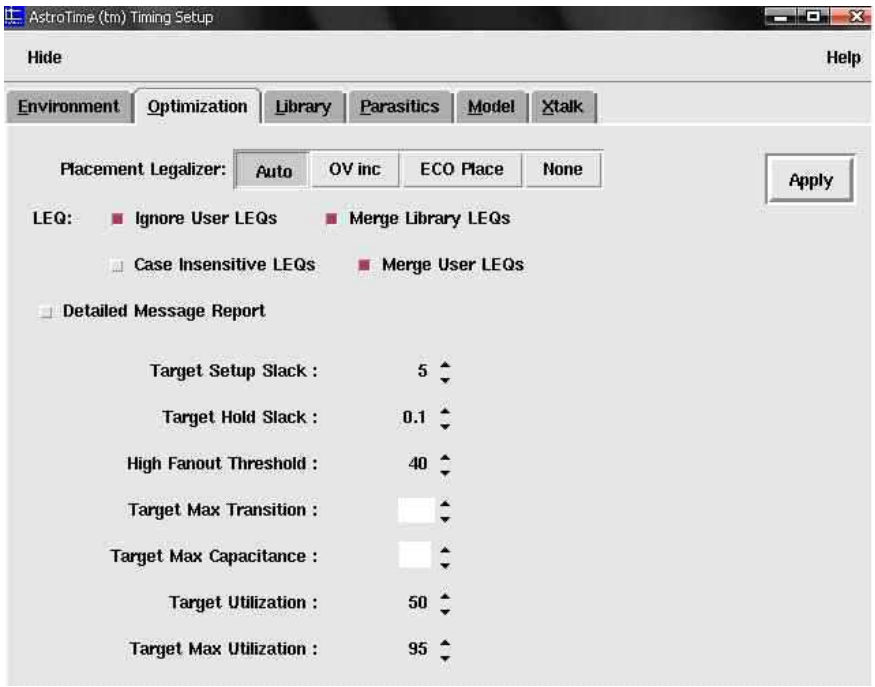


Figure 14. Envionment tab

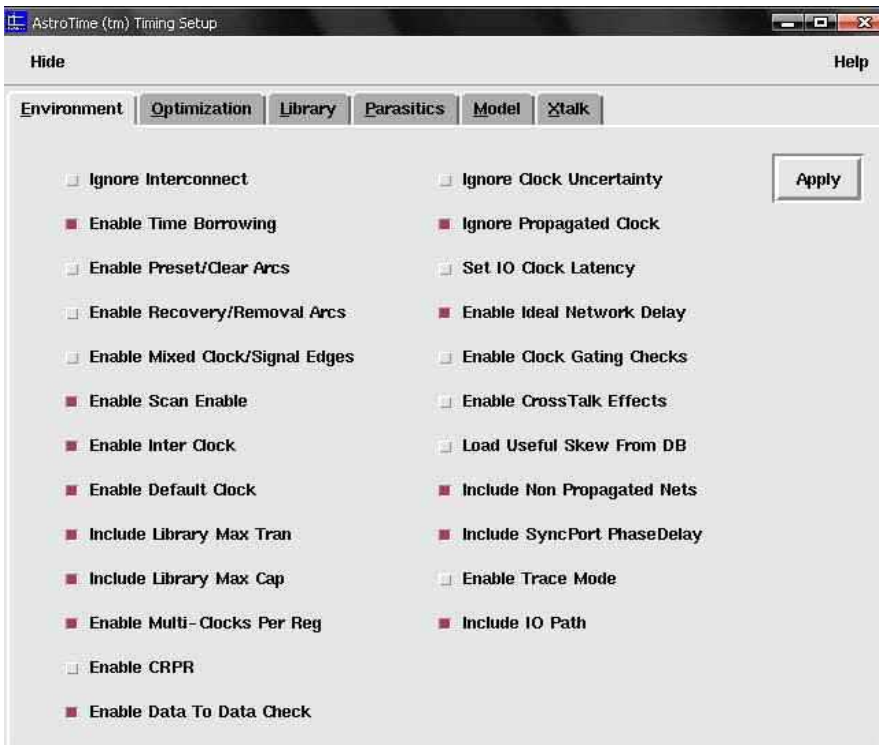


Figure 15. Optimization tab

Figure 16. Model tab

The Max Transition and Max Capacitance values in Figure 15 correspond to the Constrain value of the design compiler,
Put the value according to the design. A value of 0 tells Astro to ignore this setting.

3.2 Select InPlace -> Auto Place ...

Change the Effort form "Medium" to "Prototype"
Un-select the Pre-Place and Post-Place Stage, Leaving only In-Place selected.
Click OK

4. Analyze Congestion

Select InPlace -> Placement Mpas: Display Congestion Map ...
Select Route -> Global Route: Estimate Global Route Congestion!
Select InPlace -> Placement Mpas: Display Congestion Map ...
Click Clear -> Click Cancel

5. Auto Place

Select InPlace -> Auto Place ...
The Effort should be set to "Medium". The Pre-place, In-place and Post-place Stage buttons should be selected.

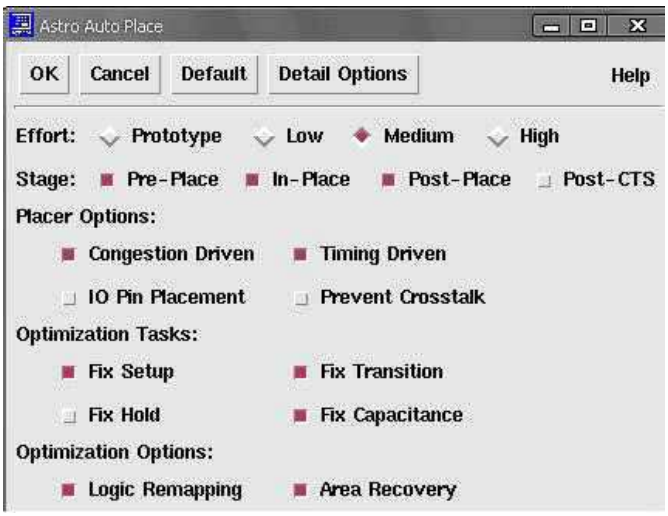


Figure 17. Auto Place

6. Handling Violations after Auto-Place

: Optimization when Violation occurs after Auto-Place

6-1 Enter pdsCROptimization in the tcl window and press Enter

6-2 Select InPlace -> Auto Place ..

Click on "Default"

Select the "High" Effort option

DeSelect Pre-Place and In-Place (only the Post-Place stage is selected)

Figure 18 shows the placement completed.

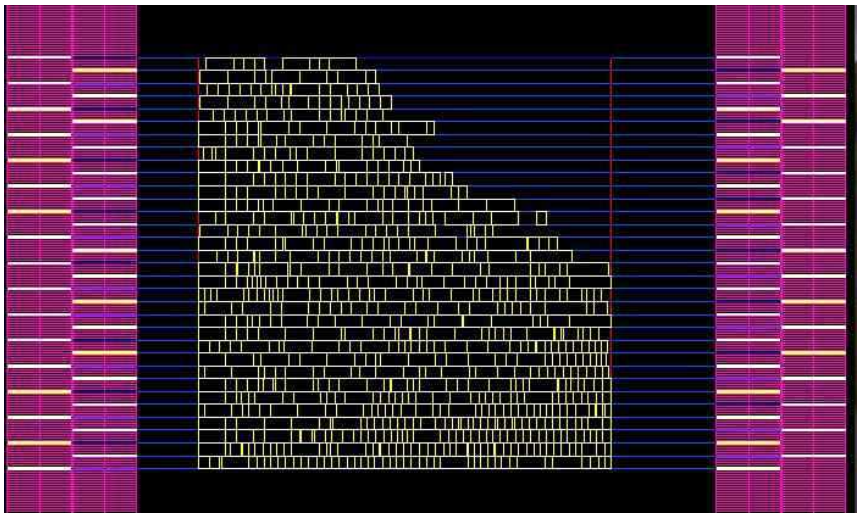
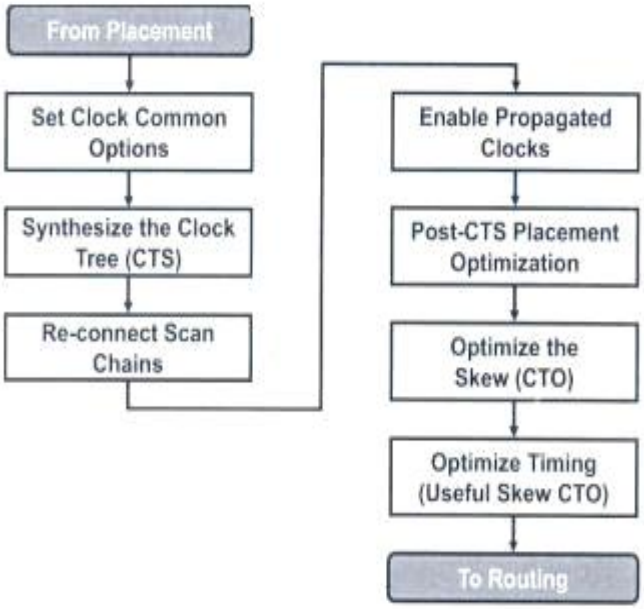


Figure 18. Placement

5. Save the cell as Setup

Select Cell -> Save As ...

Lab4. Clock Tree Synthesis (CTS)



Total Flow of Clock Tree Synthesis

1. Things to check before CTS

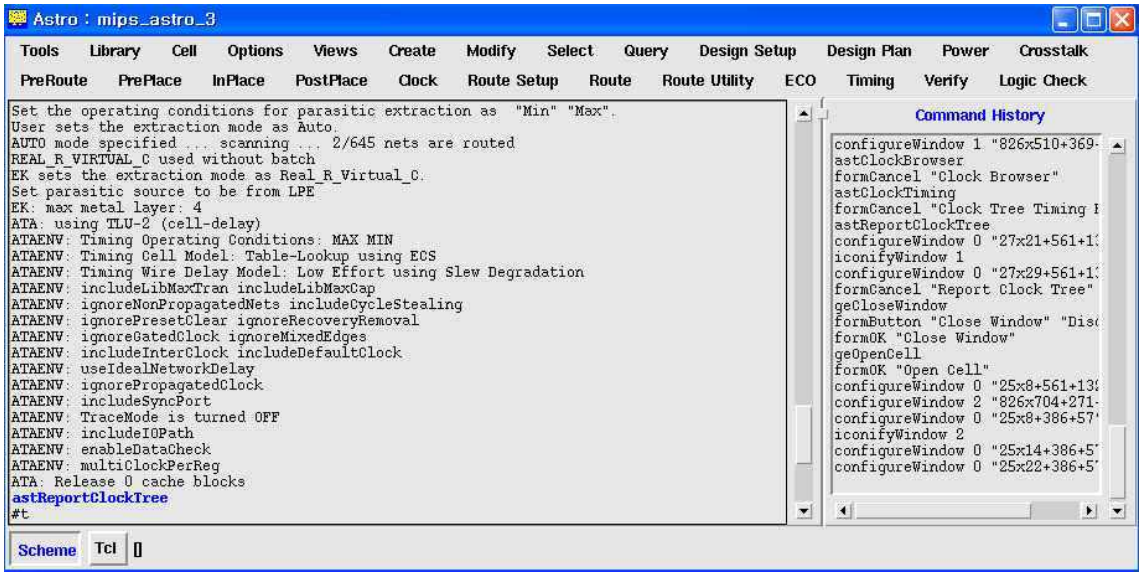
1) Placement must be completed completely.
2) Power and ground nets must be prerouted.
   -> If you have run it, you should check if the P / G connection is good.
   (PreRoute -> Verify P / G Connectivity ...)
3) Congestion map should be checked.
   -> 4 If metal is used, the Congestion value should not be 4 or more.
4) Timing violation should be avoided immediately after the placement.
   (Enter "ataReportSummary" in execution window)

```
Summary of timing analysis (w/o xtalk)
      Setup (Target=0.0000)          Hold          Num      Num
     Slack    Num      Total      Slack    Num  MaxTrans MaxCap
    15.278      0        0.0      0.213      0       0       0
```

5) Are there any high fanout nets?

2. Report Clock Tree

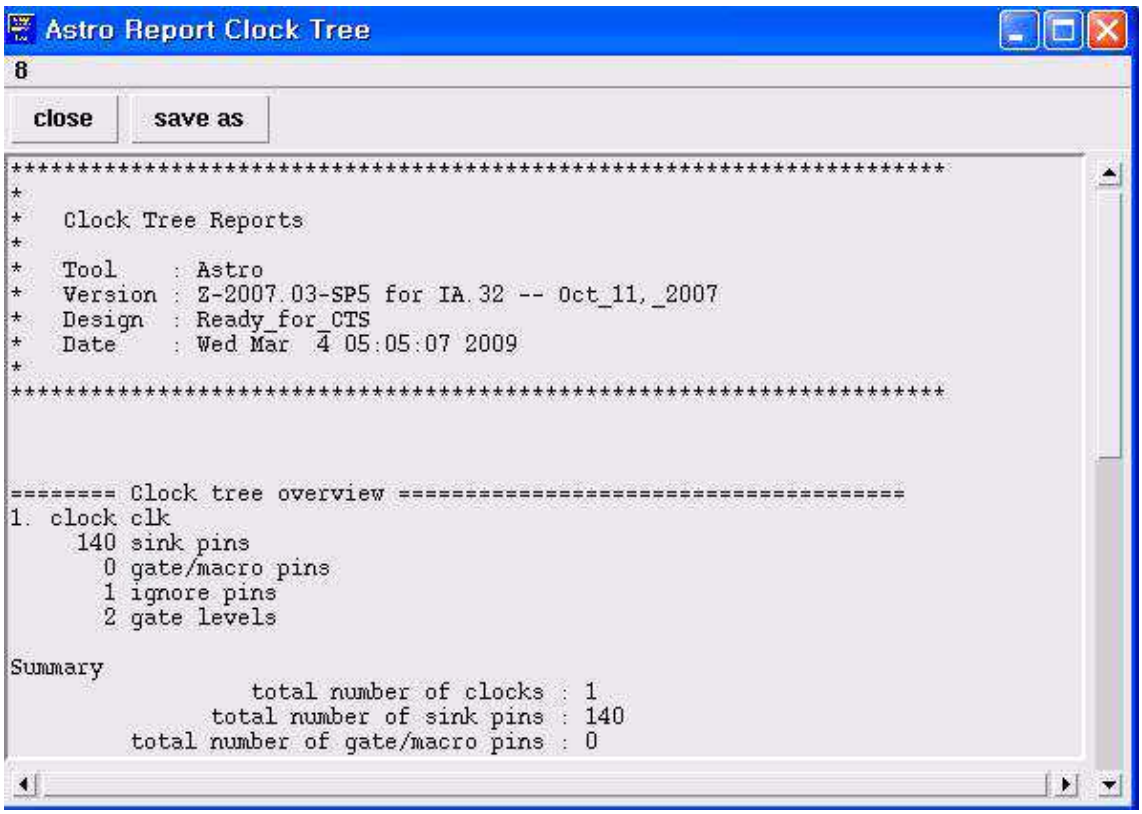
-> Before you do CTS, you should check how the actual clock tree is formed.



-> press astReportClockTree in the execution window and Enter

-> At the Report Clock Tree window, click Default and then select all options. Leave File Name blank and press OK

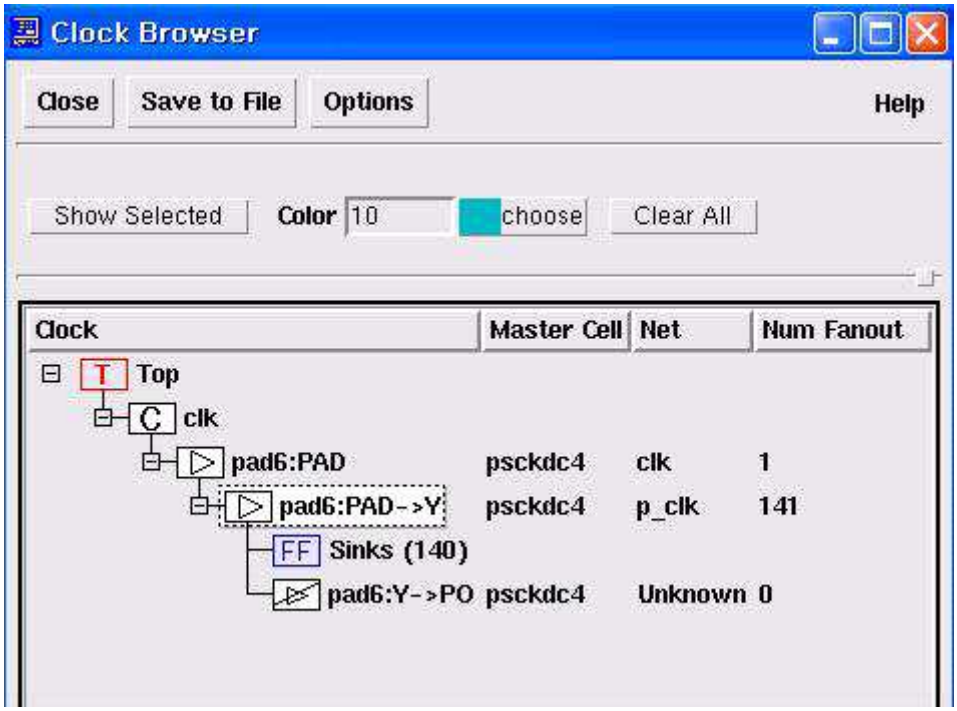
In the Astro Report Clock Tree window, information about the current clock tree is displayed.



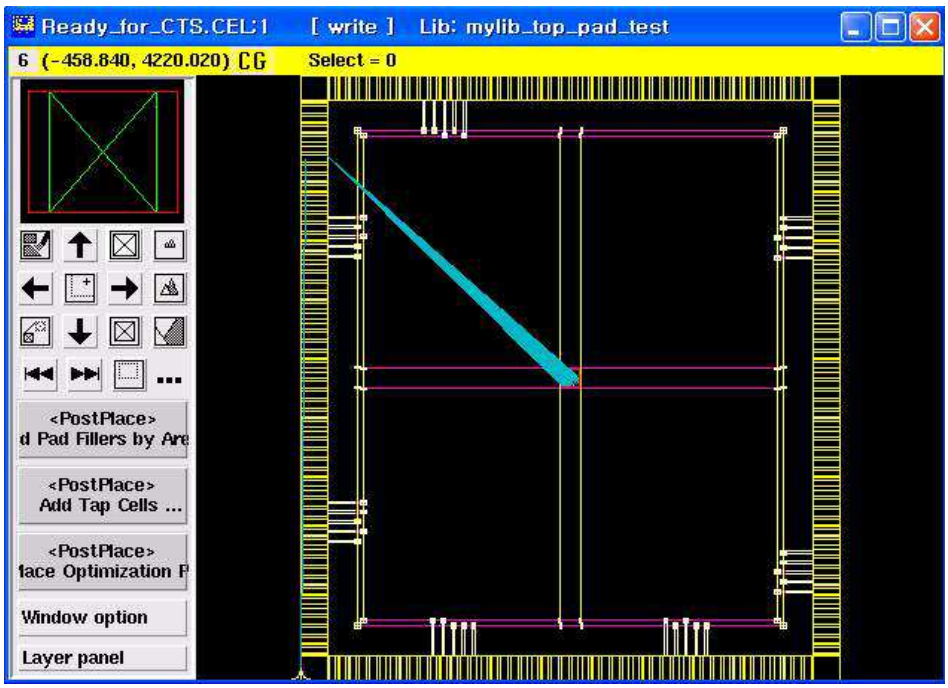
In the above report, Clock is "clk" and 140 cells require clk.

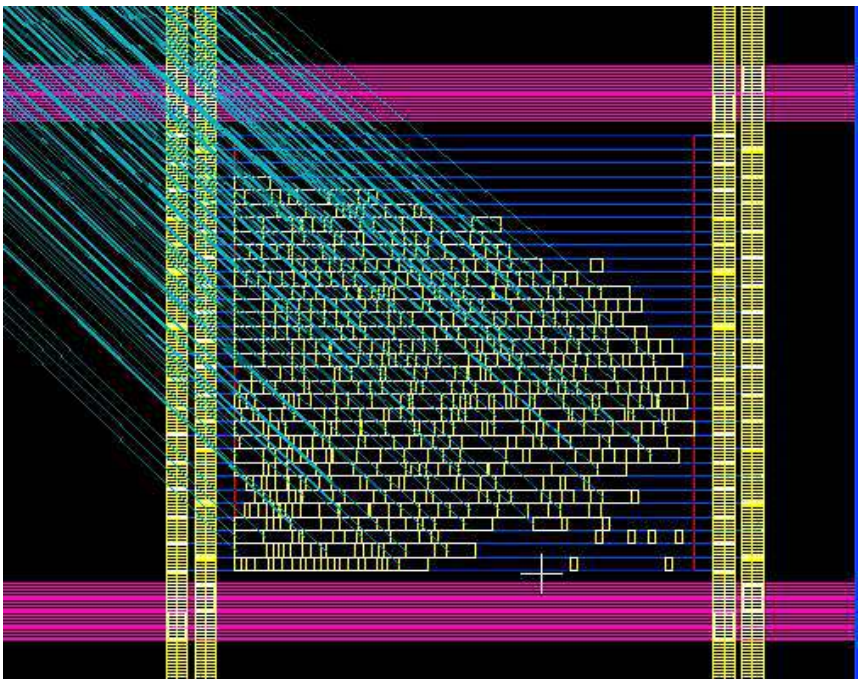
3. Clock Browser

- Select Clock-> Utilities: Clock Browser ...

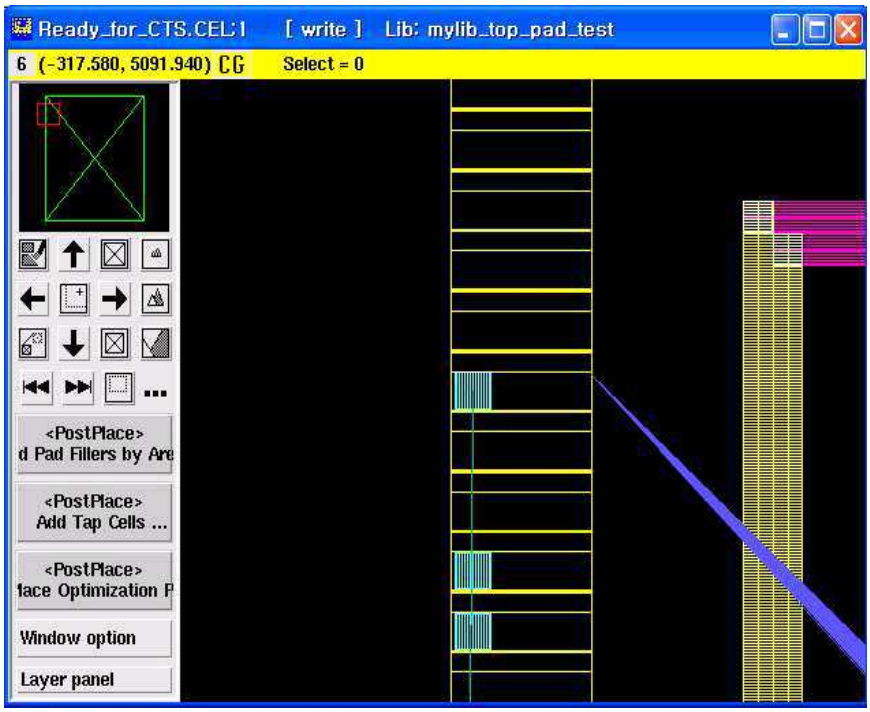


After running Clock Browser, select clk in clk tree and clk tree will be displayed as below.





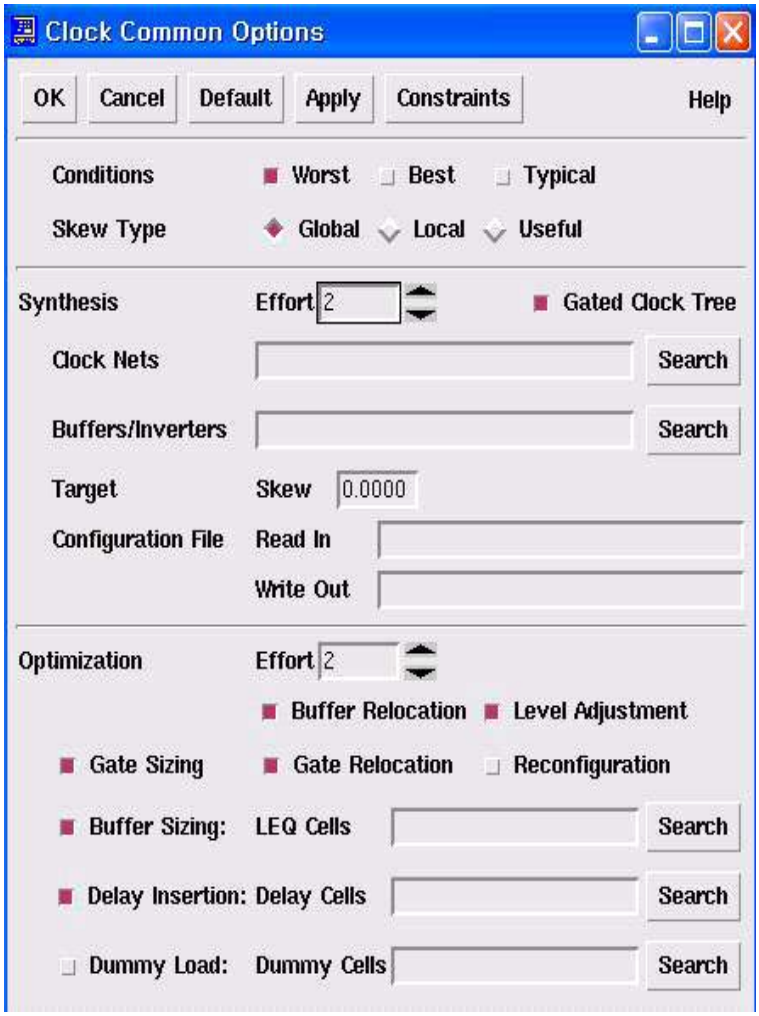
<clock tree inside core>

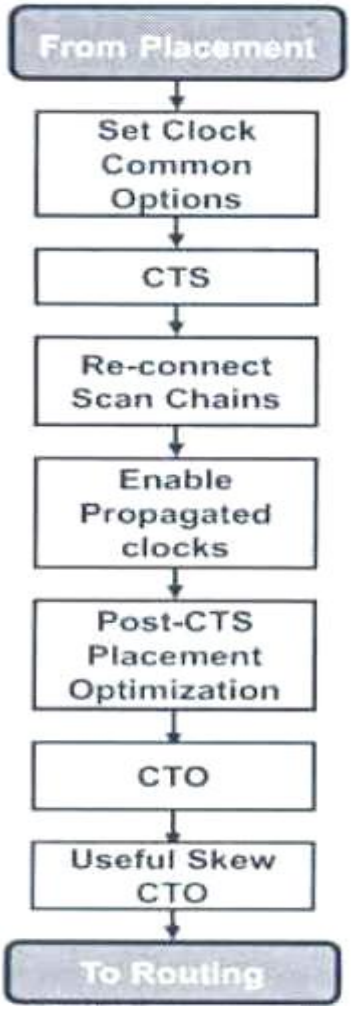


<Clock pad>

4. Set Clock Common Options

- Select Clock-> Clock Common Options ...
  -> Click on "Default" and "Apply"

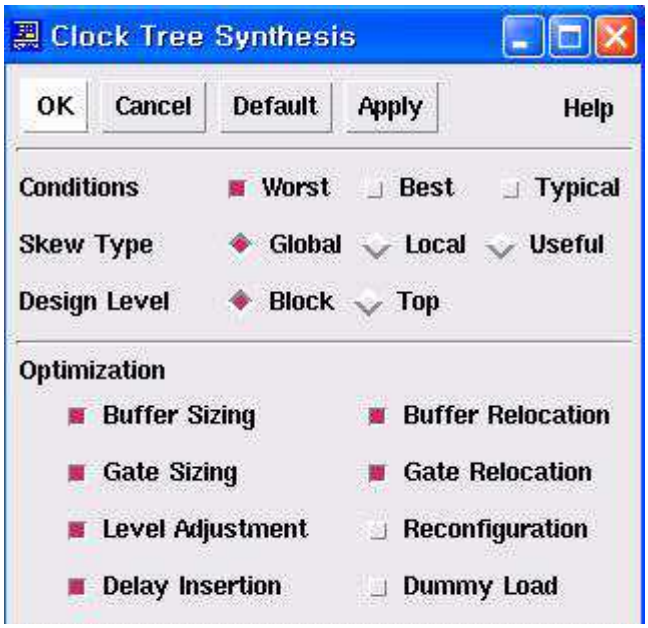


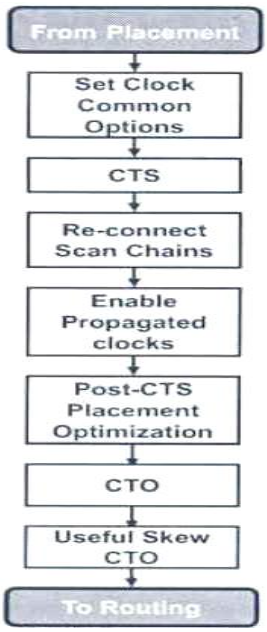


5. Clock Tree Synthesis

Select Clock -> Clock Tree Synthesis: Clock Tree Synthesis ...

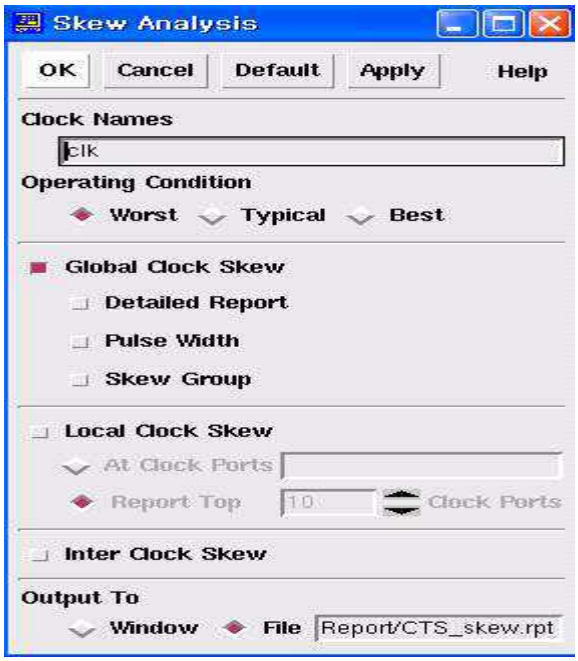
Click on "Default" and "OK"

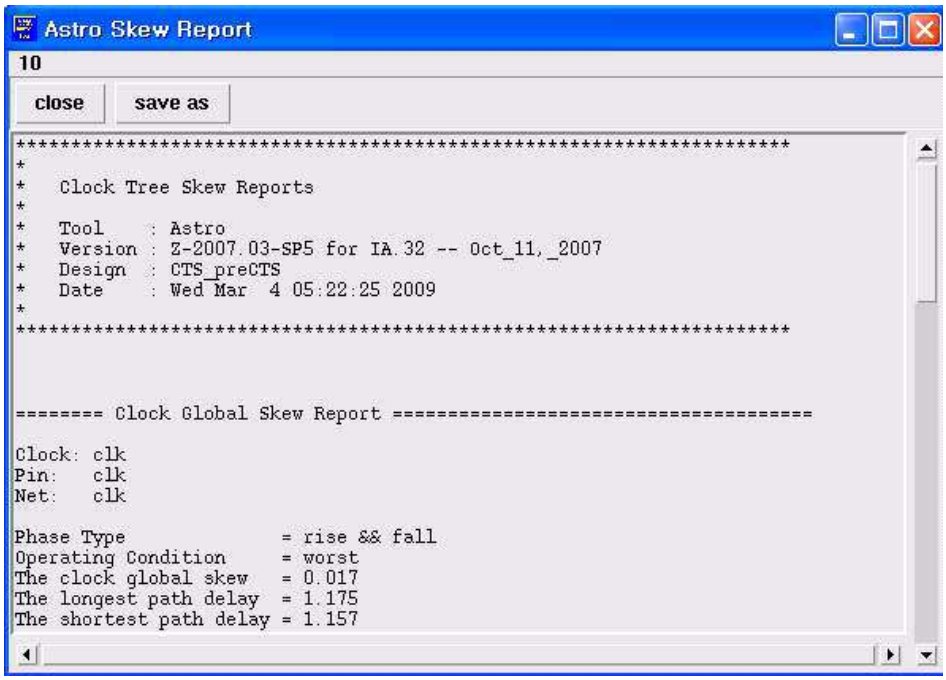




6. Skew Analysis

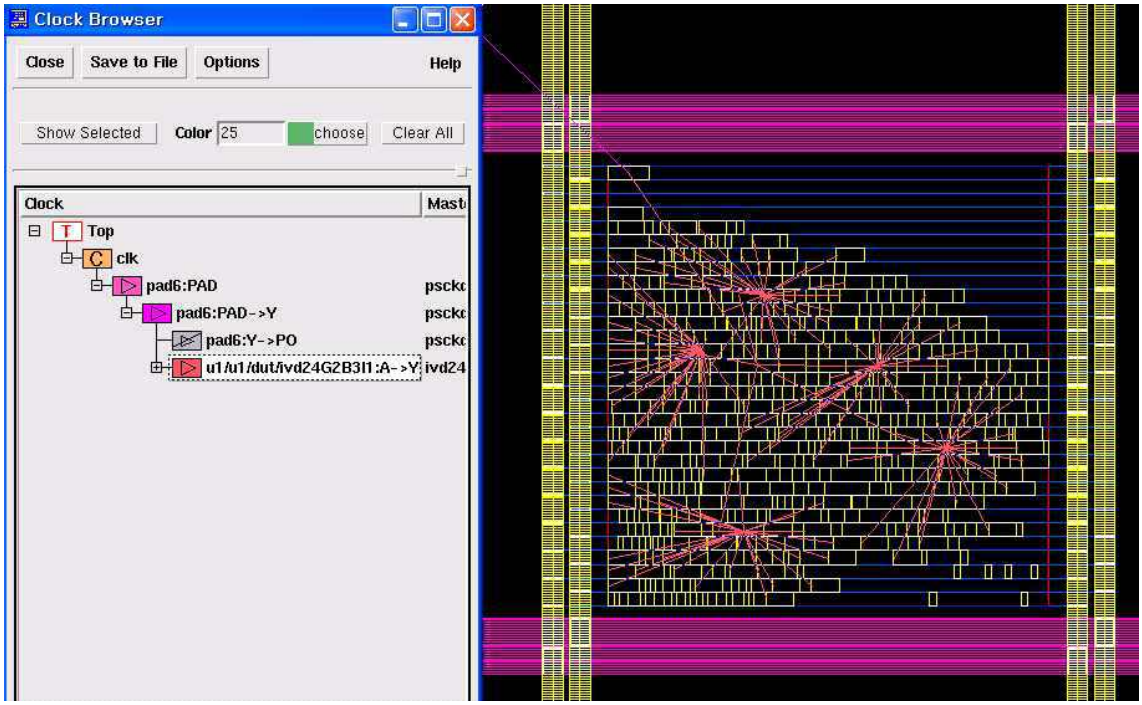
- Select Clock-> Reports: Skew Analysis ...
- Click on "Default"
- Enter real clock name as Clock Names ("clk" for mips)
- Click "OK"





7. Clock Browser

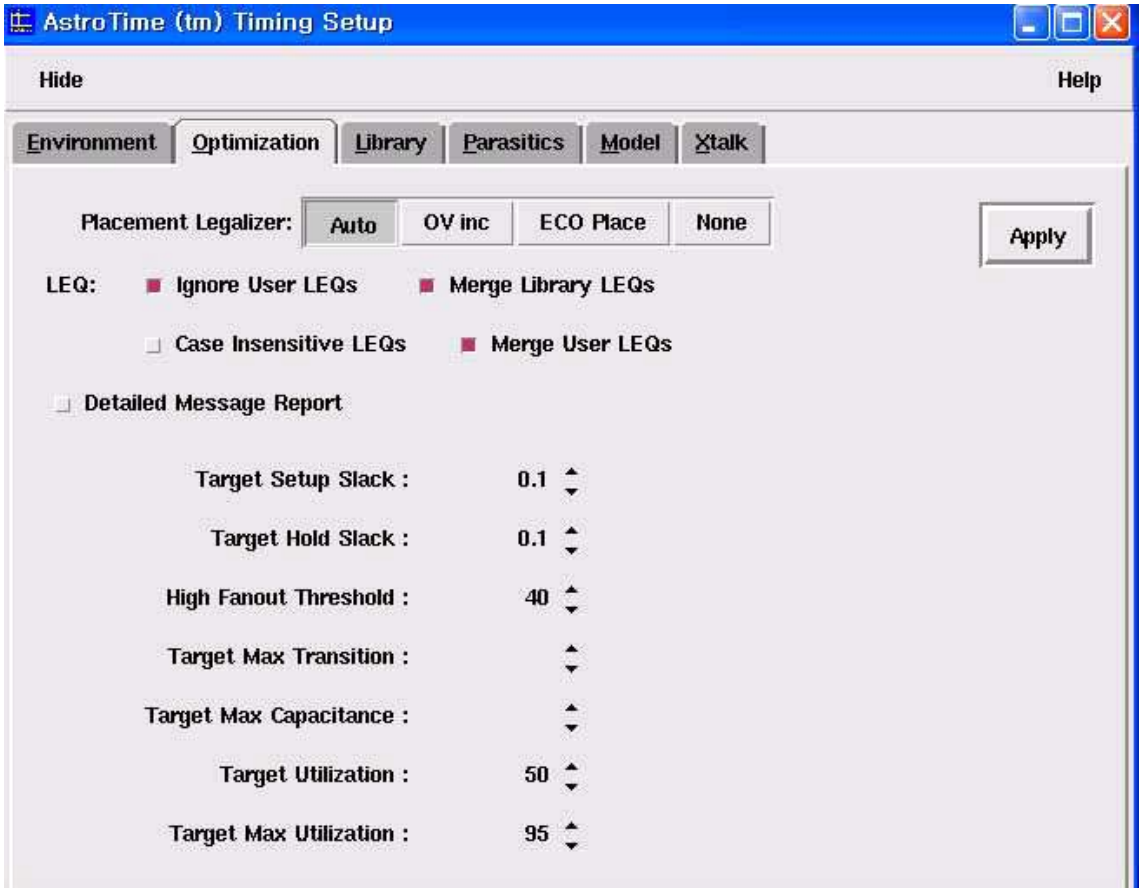
- Select Clock -> Utilities: Clock Browser ...



8. Post CTS Timing Setup

- Select Timing -> AstroTime: Timing Setup ...
- Click on "Environment"
- Select options as like the picture below
- Click "Apply"

- Click on "Optimization"
- Select options as like the picture below
- Click "Apply"



- Click "Hide"

9. Re-connect San Chains

- Optimize the broken scan chain

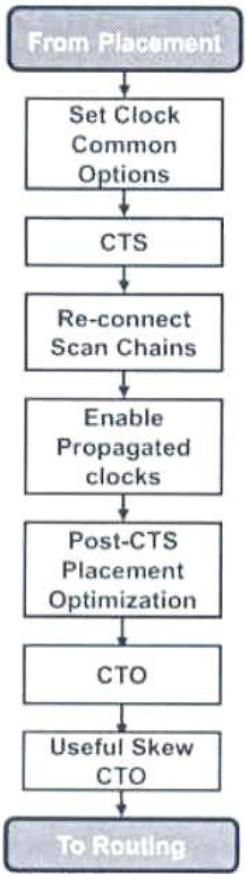
PrePlace -> Scan Chain: Optimize.Delete Scain Chain ..

mode: optimize, use the option "Clock Net Based Reordering"

10. Propagated_clock

- Apply the Propagated, Unsertainty values in the SDC file for all clocks.

Enter sdc "set_propagated_clock [all_clocks]" on execution window

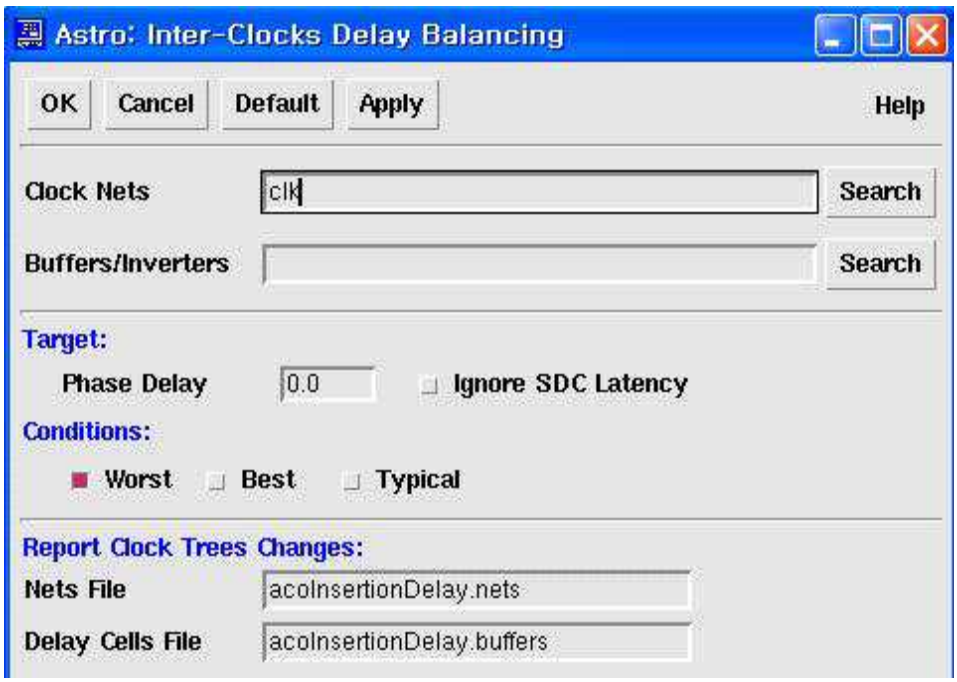


10. Timing Check

Enter ataReportSummary on execution window
Select Timing -> Astro Time: Timing Report ...
Click on Default and OK

11. Perform Inter-Clocks Delay Balancing (astCTOInterClocksBalance)

Select Clock -> Clock Tree Optimization: Inter-Clocks Delay Balancing ...
Enter inter_clock name in Clock Nets field ("clk" for mips)
Click OK

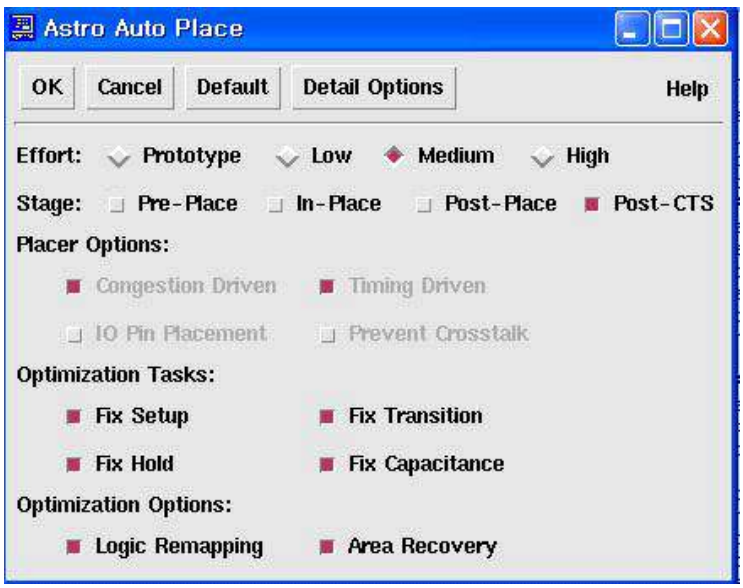


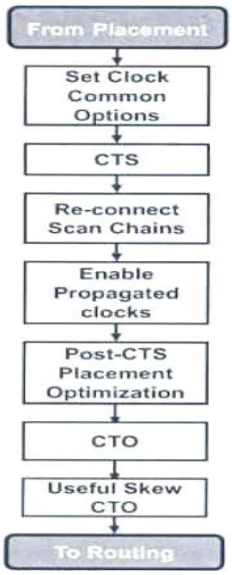
12. Timing Check

Enter ataReportSummary on excution window
Select Timing -> Astro Time: Timing Report ...
Click on Default and OK

13. POST_CTS Placement Optimization

Select InPlace -> Auto Place ...
Click on "Default"
Deselect "Pre-Place", "In_Place" and "Post_Place"
Select "Post-CTS"
Select "Fix Hold"
Click "OK"





-> Timing Checking after Post-CTS if setup/hold, max tran/cap viloations are still existed, then perform Post-CTS Optimization with other options again.
ex) High effort, change Optimization Tasks by user's idea.

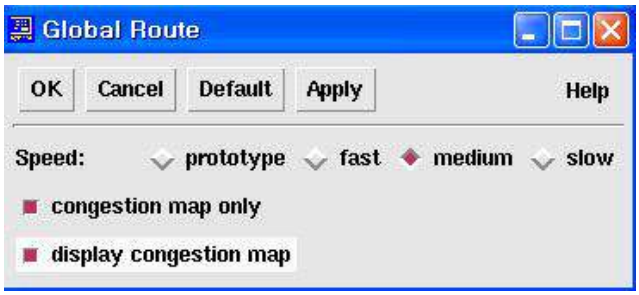
14. Timing Check&Congestion map check

Timing Check

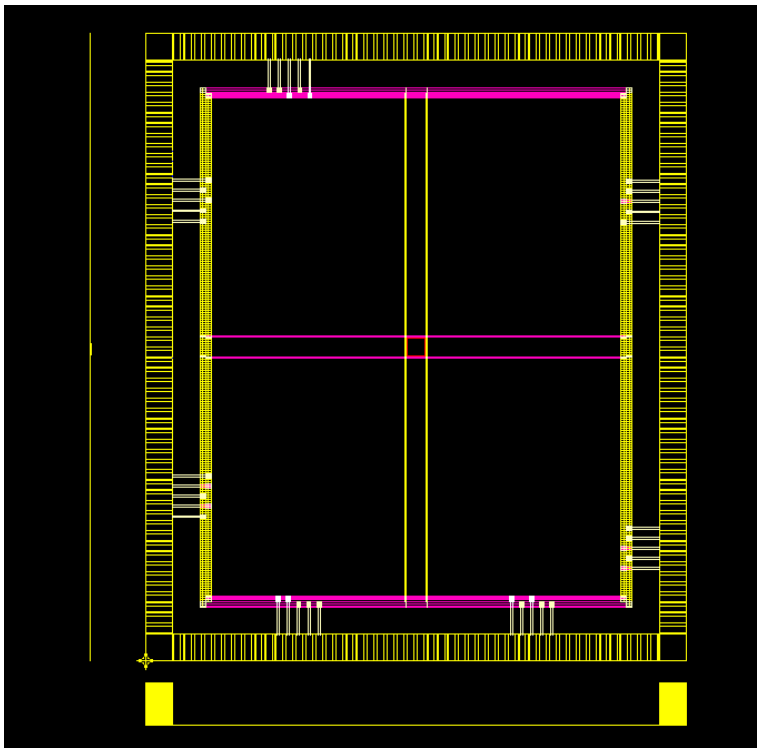
- Enter "ataReportSummary" on excution window

Check Congestion map

- Select Route-> Global Route: Global Route ...
- Select the "congestion map only", and the "display congestion map" options
- Click "OK"



Check Congestion map as like in placement flow.

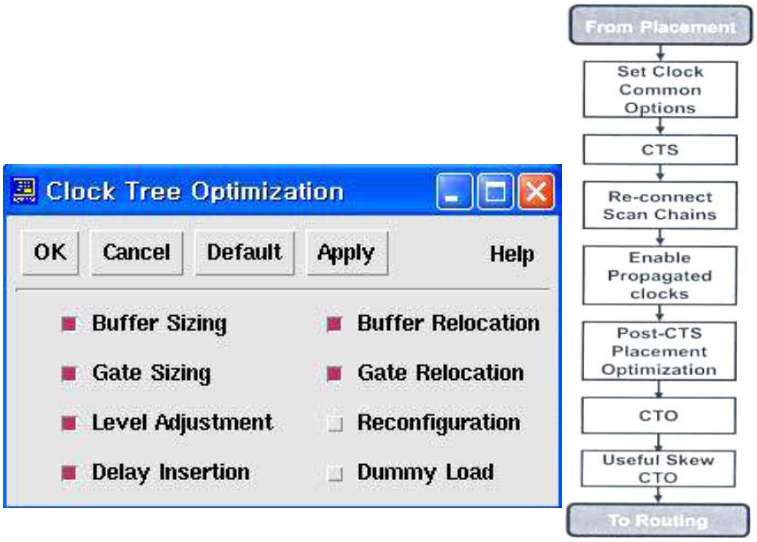


15. Skew Analysis

- After analyzing Skew after Post Clock Tree Optimization, decide whether or not to run CTO and Useful Skew CTO.
- Select Clock-> Reports: Skew Analysis ...
- Click on "Default"
- Enter real clock name as Clock Names ("clk" for mips)
- Click "OK"

16. Optional: Clock Tree Optimization

- Clock -> Clock Tree Optimization: Clock Tree Optimization ...



-> When we analyze the skew result of CTO, clock skew
Can be confirmed.

17. Optional: Useful Skew Optimization

Enter the command in execution window as like below.

For example,
tcl "useful_skew_opt -buffer_sizing -hold_target -2.0"
tcl "useful_skew_opt -level_adjustment -hold_target -2.0"
tcl "useful_skew_opt -buffer_insertion –hold_target -2.0"

The above is one of the examples and you need to find the correct value.
-> In this example, we did not do Useful Skew Optimization.

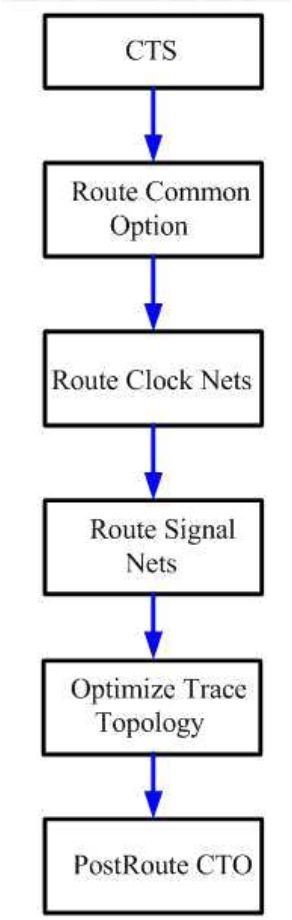
18. Check after CTS

-> Always check the following four items at all stages of CTS. Also,
Save as Cell-> Save as (do not save).
- Timing Check
- Check Congestion map
- Clock browser
- analysis Skew

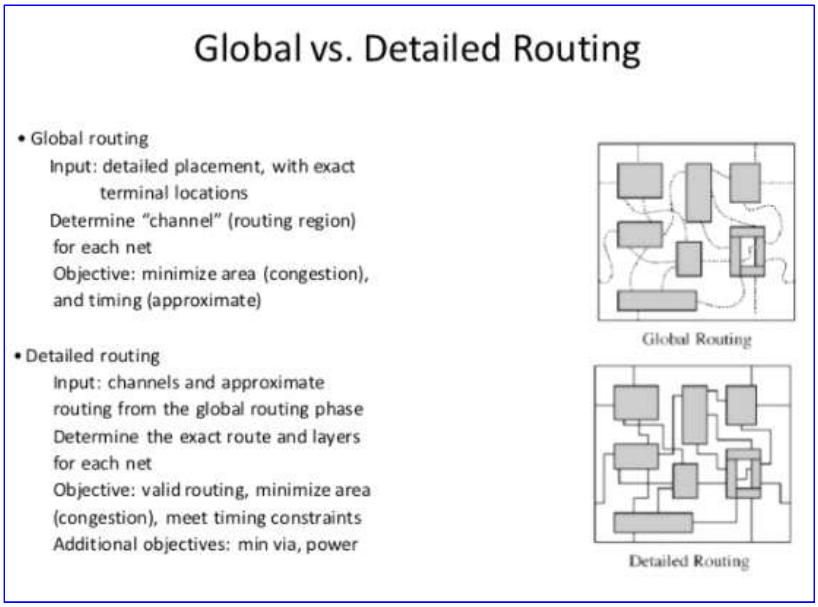
19. Tips for CTS

- Make sure the name of the exact clock name is used in the design.
- CTS result can be different depending on whether one clock or muti-clock is used.
- You should know what value of the clock skew is appropriate for your design.
- Make sure that the values of the propagated, unsertainty, and delay of the clock in the SDC file are appropriate or not.

Lab5. Routing

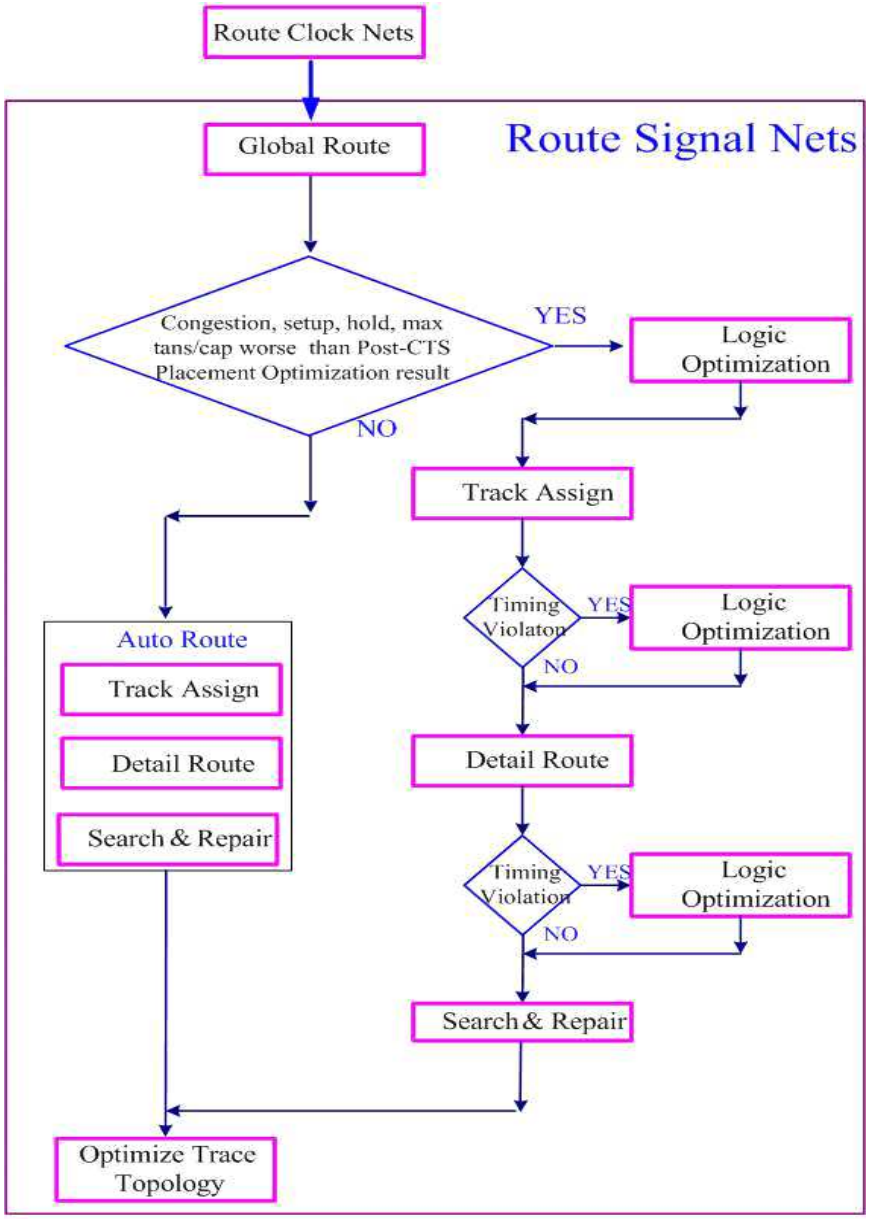


Total Flow of Routing



Detail Flow of Route Signal Nets

After the Clock Net routing has been done, and after the Golbal Route, perform Congestion and Timing check. After post-CTS Placement Optimization Timing, if the results are better compared to the Congestion results before the CTS, run Auto Assign Track Assign, Detail Route, Search&Repair at the same time. If not, go to the logic optimization step.



Check list before Routing

1) Check if placement is completed
2) Check if CTS is completed
3) Make sure Power &Ground nets are routed
4) Check that the congestion map is acceptable
5) no timing violation (setup, hold, max trans, max cap)
   -> Very low values of the violations may be disappeared during routing.
6) Check if clock skew is acceptable

1. Timing Setup before Routing

Select Timing-> AstroTime: Timing Setup ...

in Environment

: make sure to keep to option "Ignore Clock Uncertainty" unset

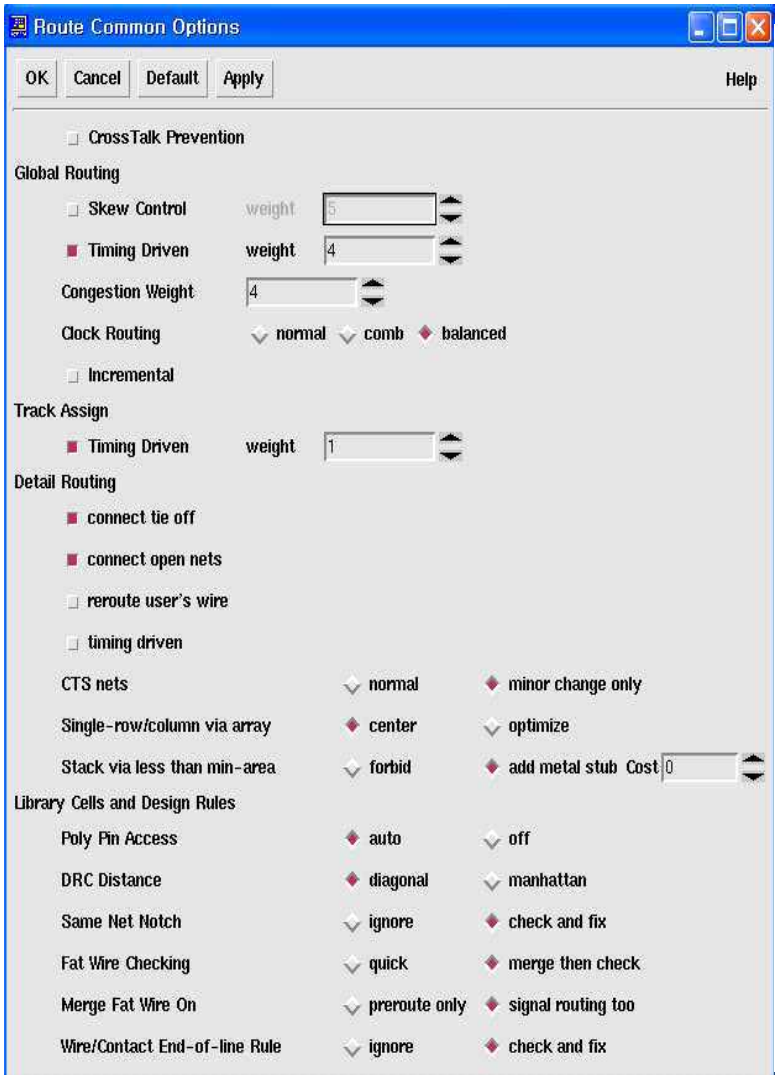
in Optimization

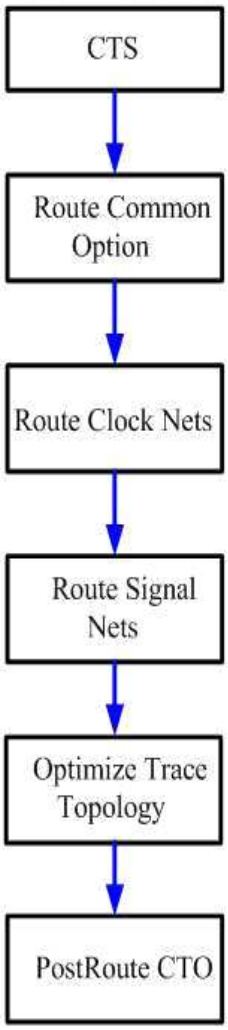
: Target Hold Slack -> 0.1

-> for in Optimization, you have to set the appropriate value according to your design.

2. Set Routing Options

Select Route Setup -> Route Common Options ...
Click "Default"
Select "Timing Driven" under both Global Routing and Track Assign
Select "check and fix" for "Same Net Notch"
Select "check and fix" for "Wire / Contact End-of-line Rule"
Click "OK"

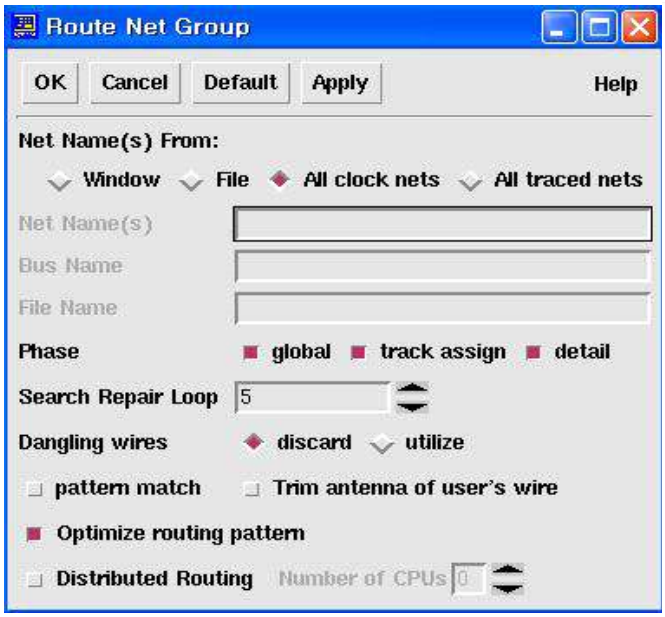


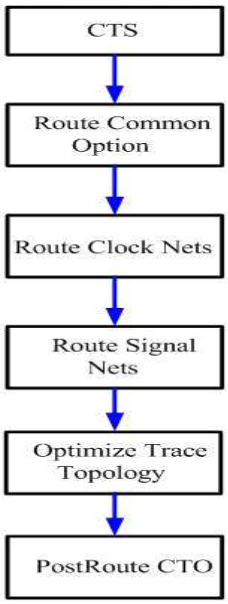


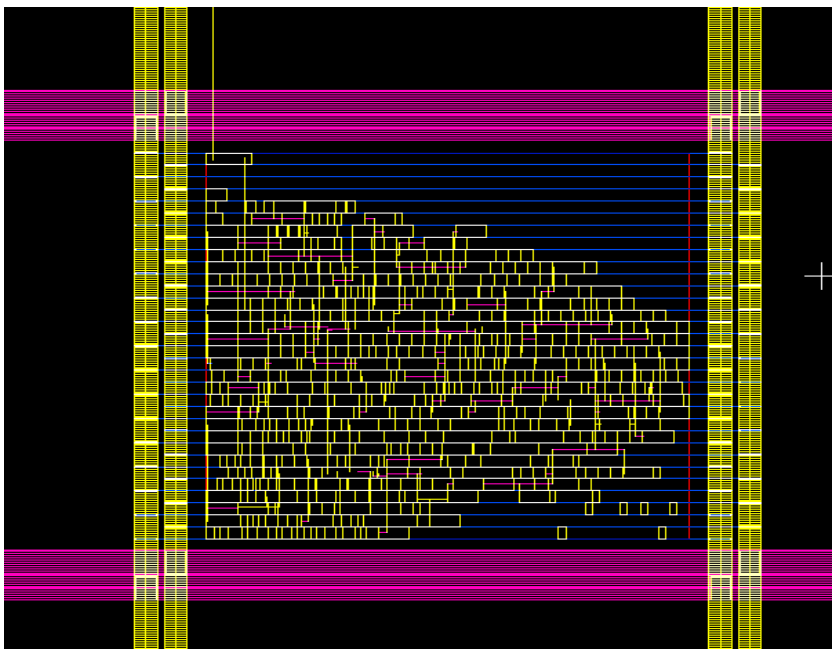
3. Route the Clock Nets

CTS has been conducted so far. But actually, the clock is not physically connected to cells. Therefore, the first thing to do in Routing is to do physically routing to each cell based on the previous CTS results.

Select Route-> Route Net Group ...
Click "Default"
Select "All clock nets" under Net Name (s) From to route all clock nets
Click "OK"



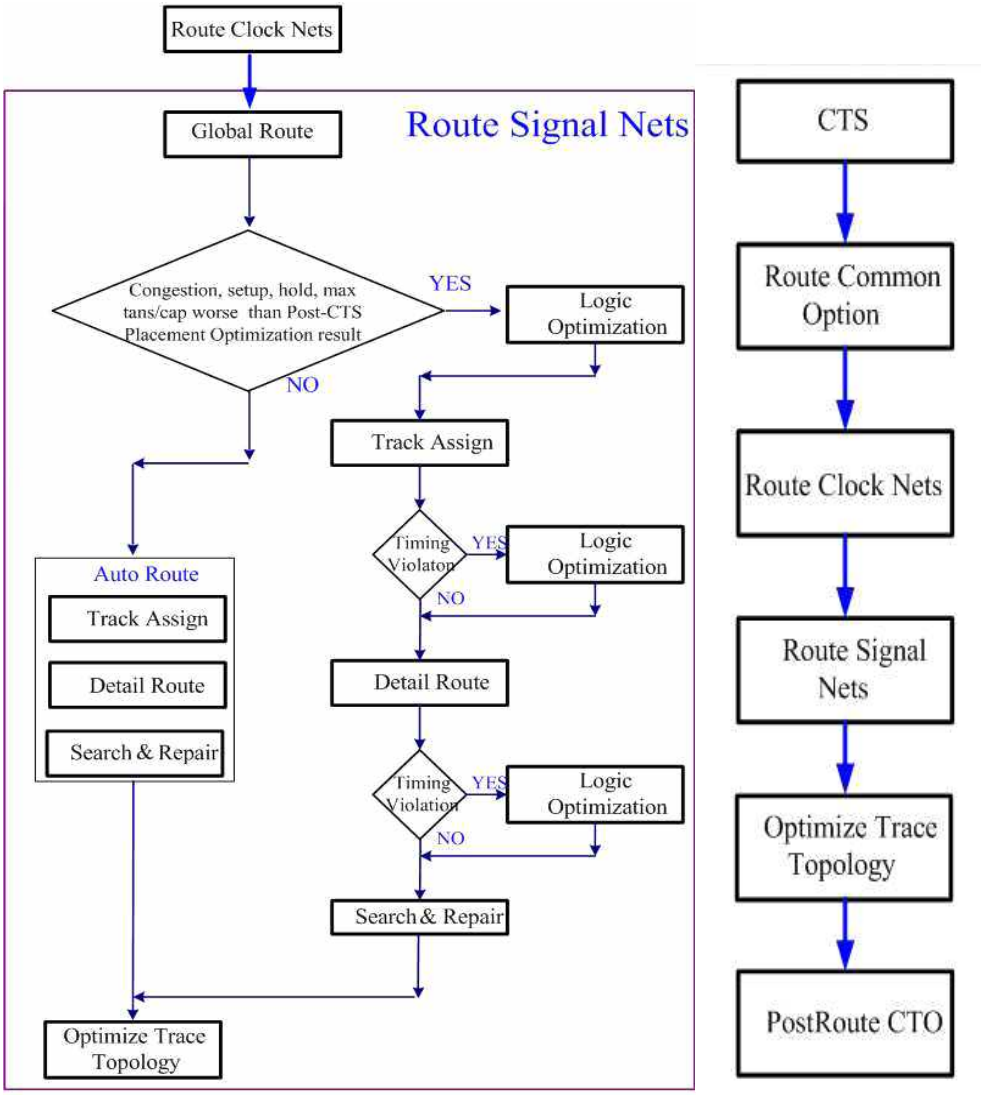




<clock inside the core after running Routing>

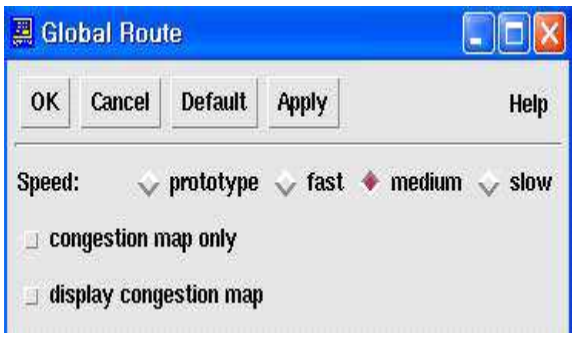
4. Detail Flow of Route Signal Nets

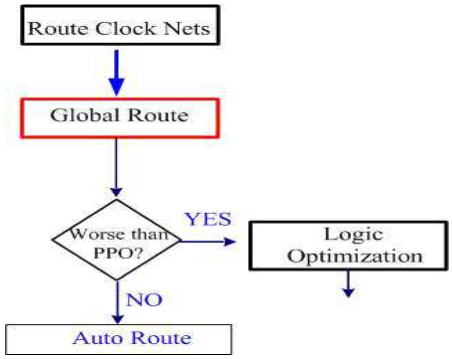
After Route Clock Nets has been done and then executing the Global Route, check Congestion and Timing. If the results are better compared to the Timing and Congestion results after post-CTS Placement Optimization, execute Assign Track, Detail Route, Search &Repair at the same time using "AutoRoute". If not, perform logic optimization by checking violations.



5. Global Route

Select Route -> Global Route: Global Route ...
Click "Default" &"OK"

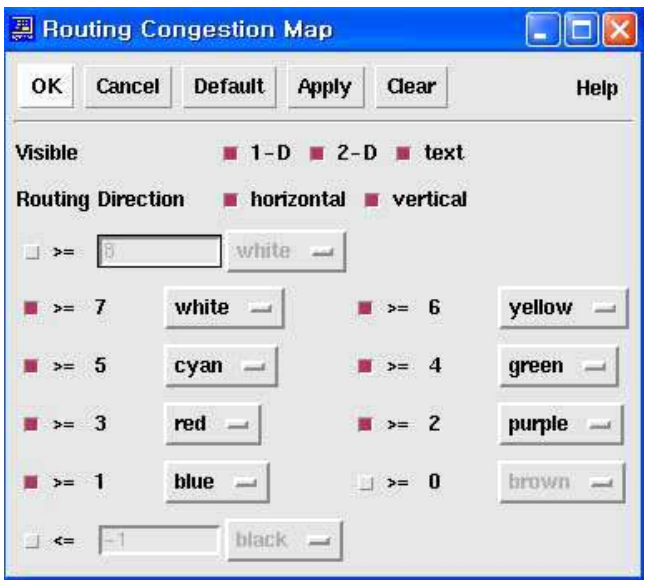




6. Display the Congestion map &Timing Check

Compare with Post-CTS Placement Optimization results. For the comparison, You should save the Congestion and Timing results during CTS.

Select Route -> Global Route: Display Congestion Map ...
Click "Apply" on Routing Congestion Map Window

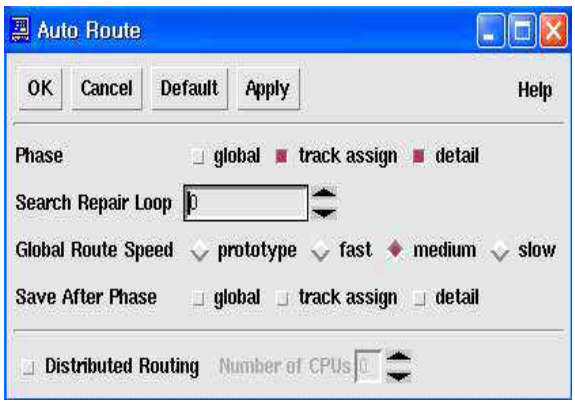


Select Timing-> Astro Time: Timing Report

Now, according to the result of the comparison, you can execute Auto Route or logic optimization again. We introduce two methods here.

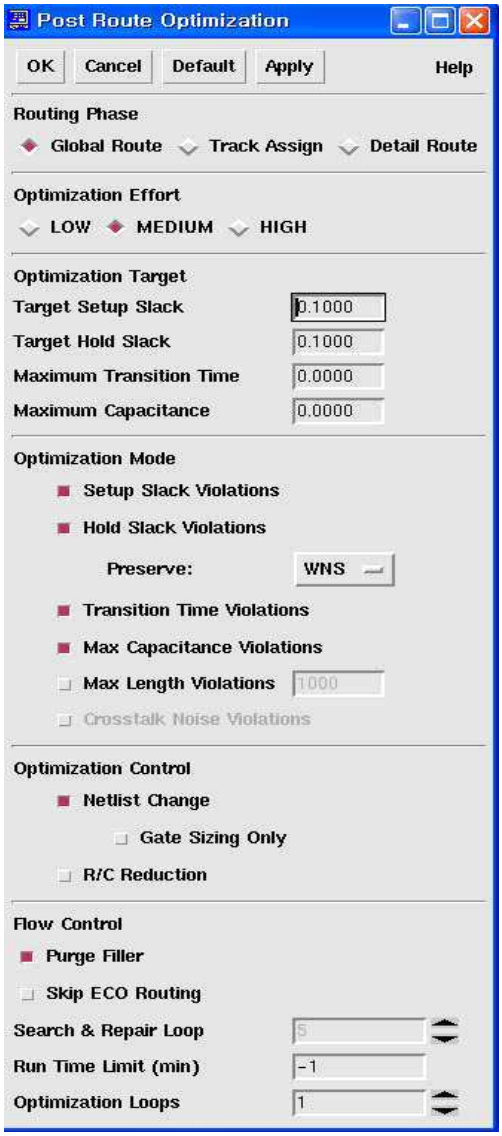
6-1. Auto Route

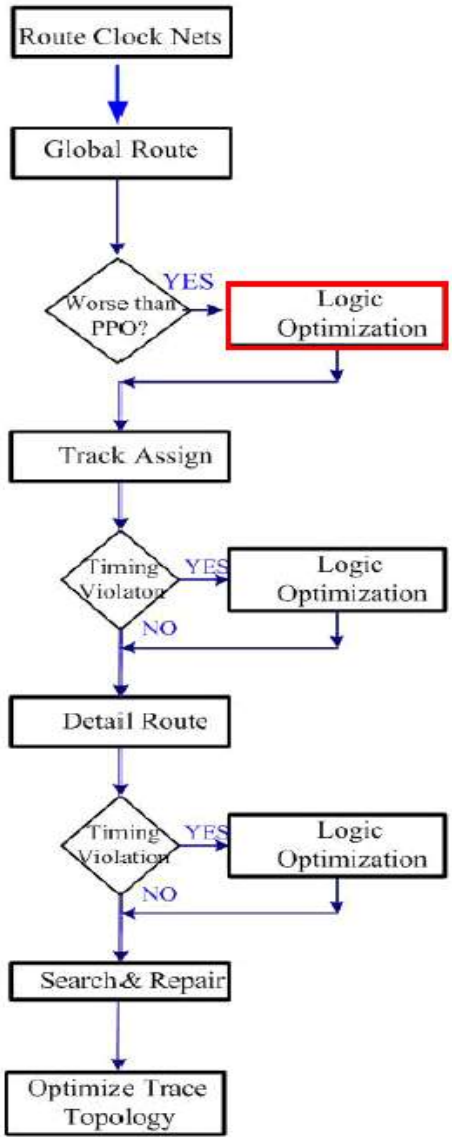
Select Route -> Auto Route ...
De-select the global route phase
Set the Search &Repair loop to 5 loops
Click OK



6-2-1. Global Route Optimization

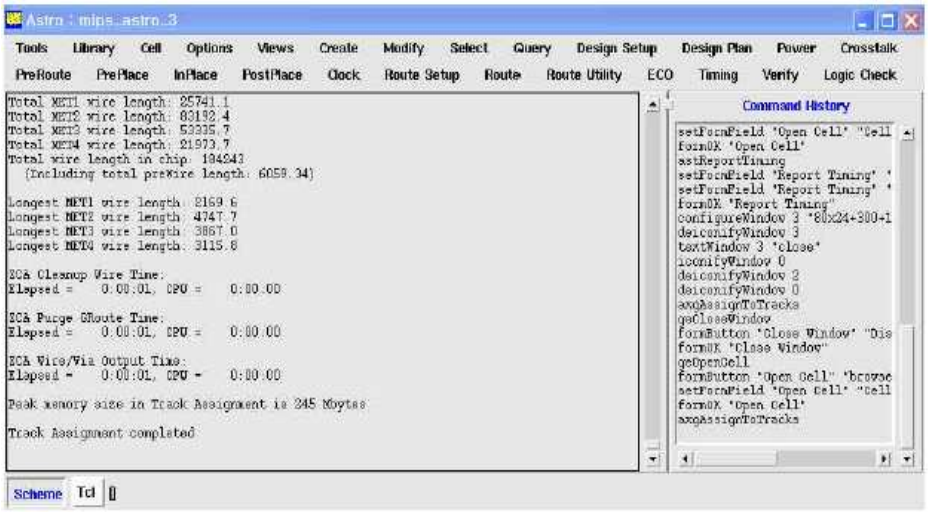
Select Route -> Global Route: Global Route Optimization ...
click "OK"





6-2-2. Track Assign

Select Route -> Track Assign!

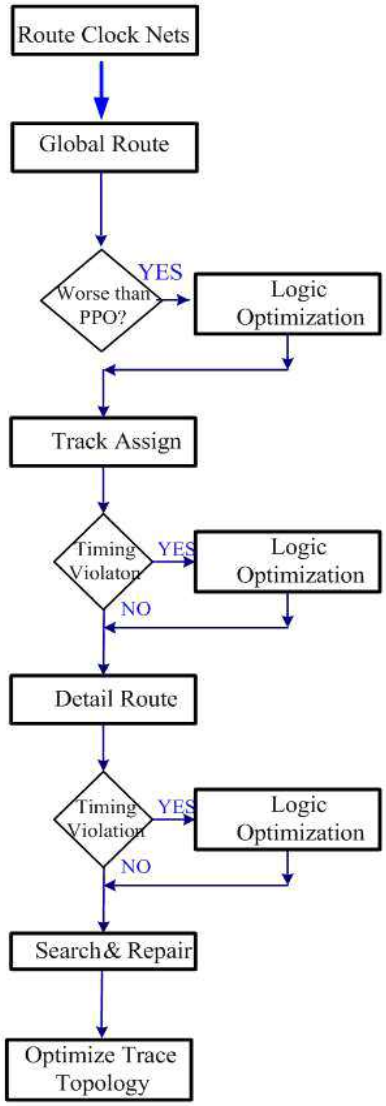


6-2-3. Timing Check

Enter "ataReportSummary" on execute window

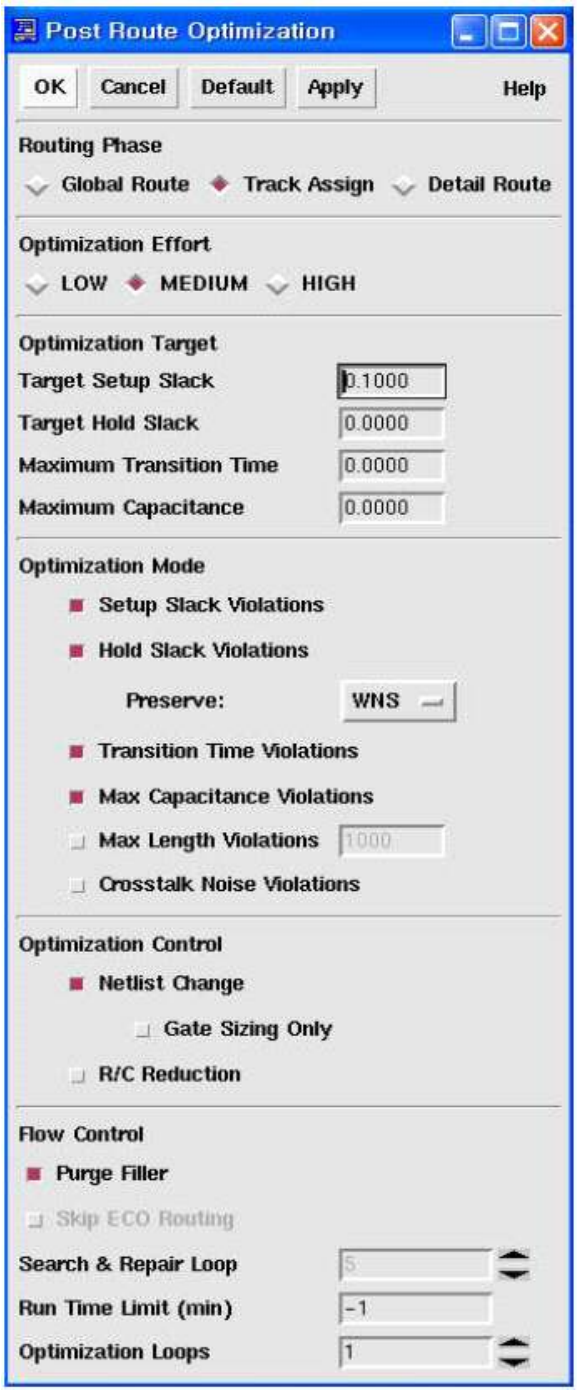
or

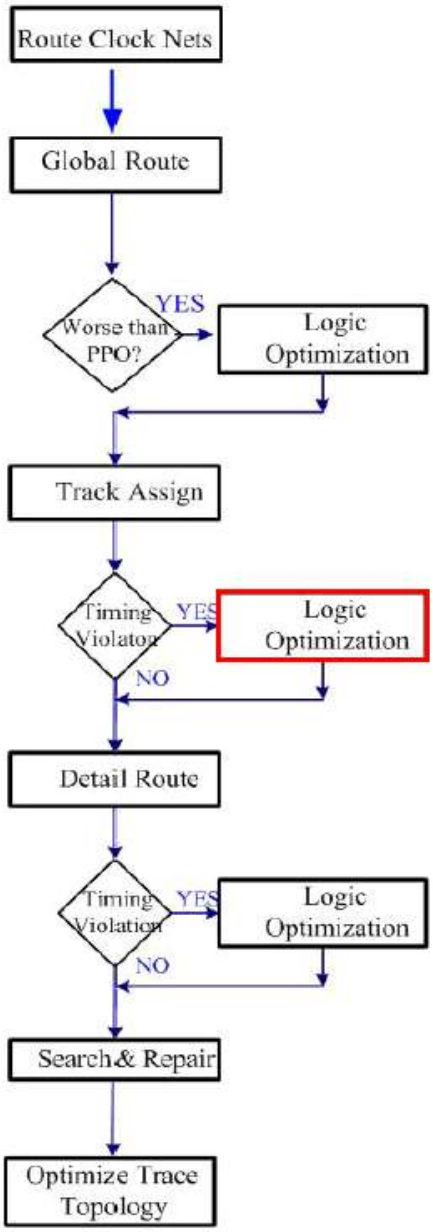
Select Timing-> Astro time: Timing Report



6-2-4. Track Assign Optimization

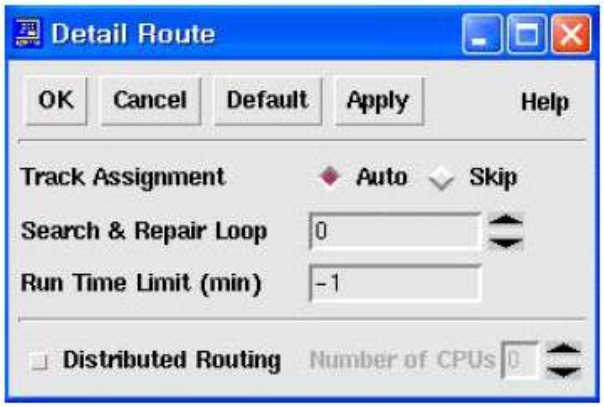
Select Route -> Track Assign: Track Assign Optimization ...

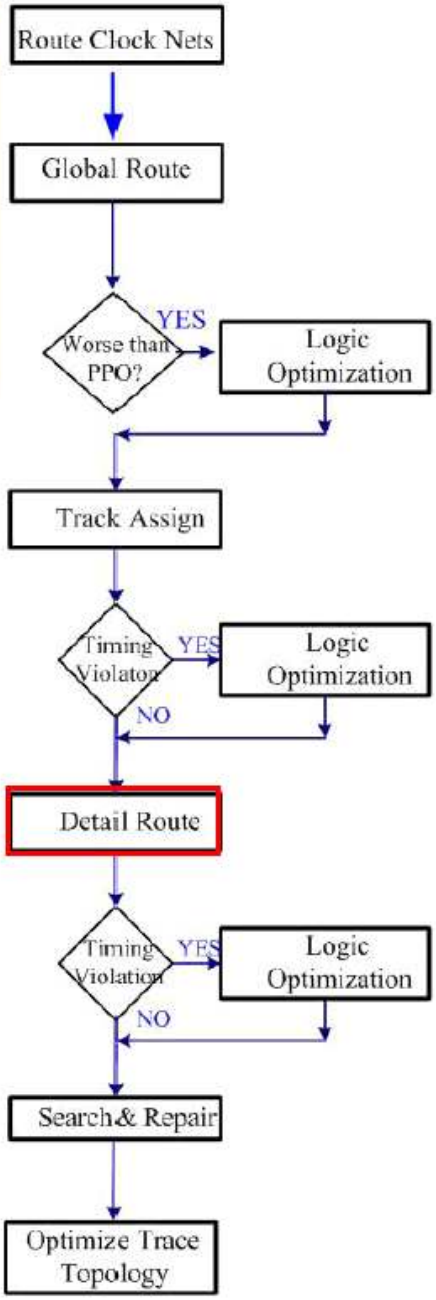




6-2-5. Detail Route

Select Route -> Detail Route: Detail Route ...



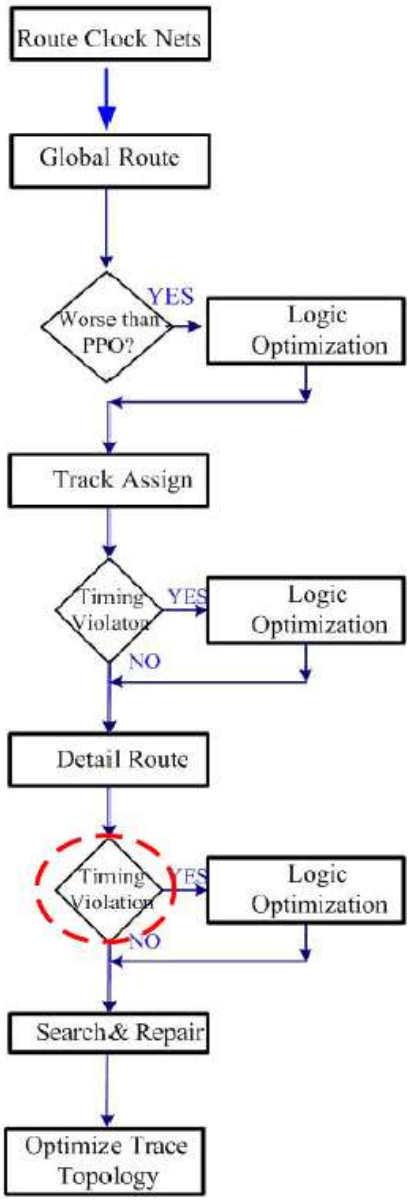


6-2-6. Timing Check

Enter "ataReportSummary" on execute window

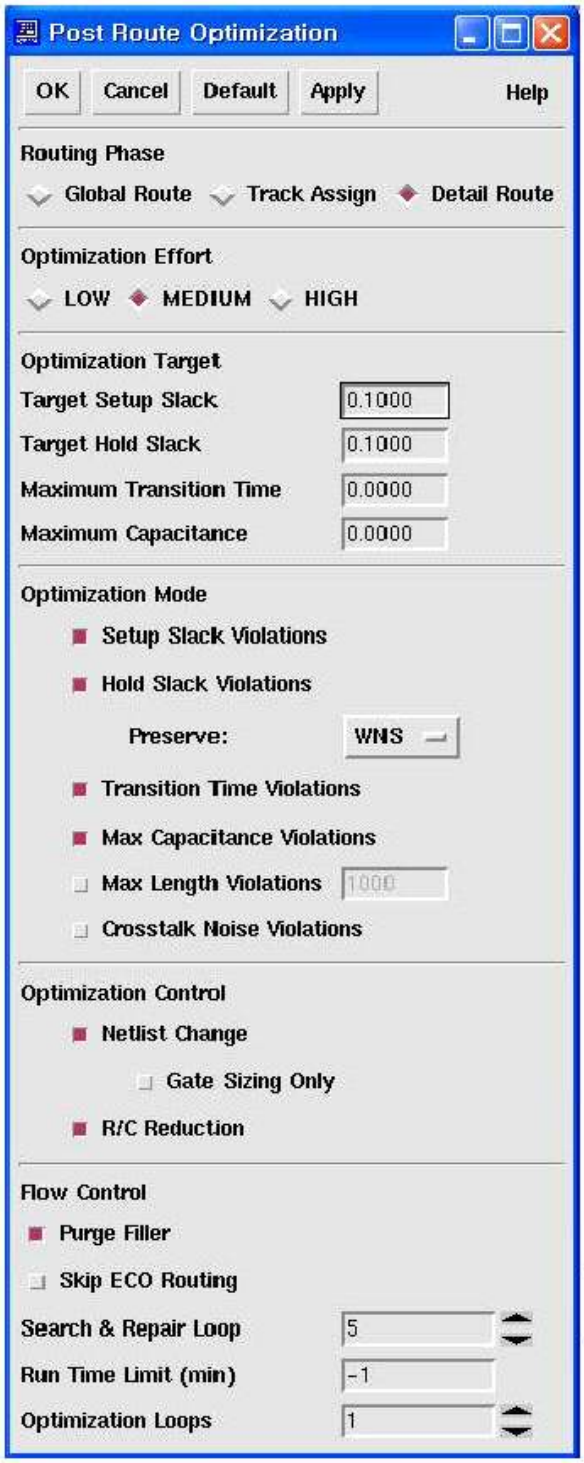
or

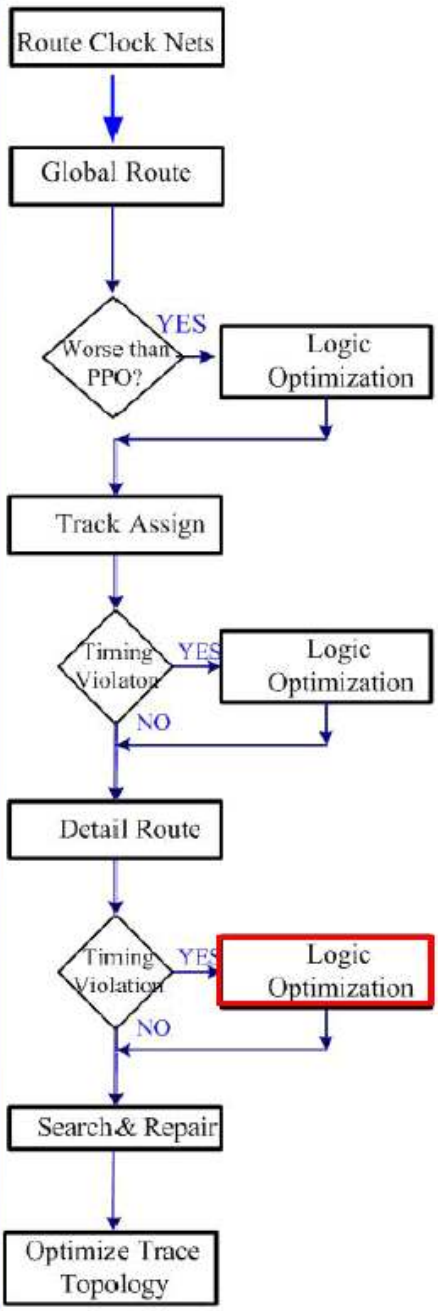
Select Timing-> Astro time: Timing Report



6-2-7. Detail Route Optimization

Select Route-> Detail Route: Detail Route Placement / Route Optimization ...

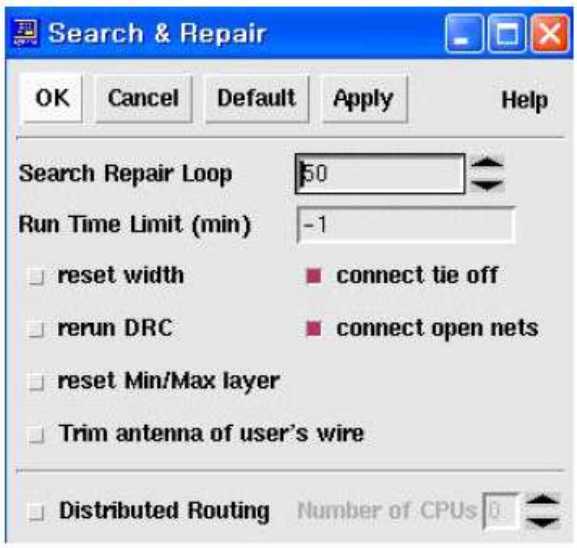


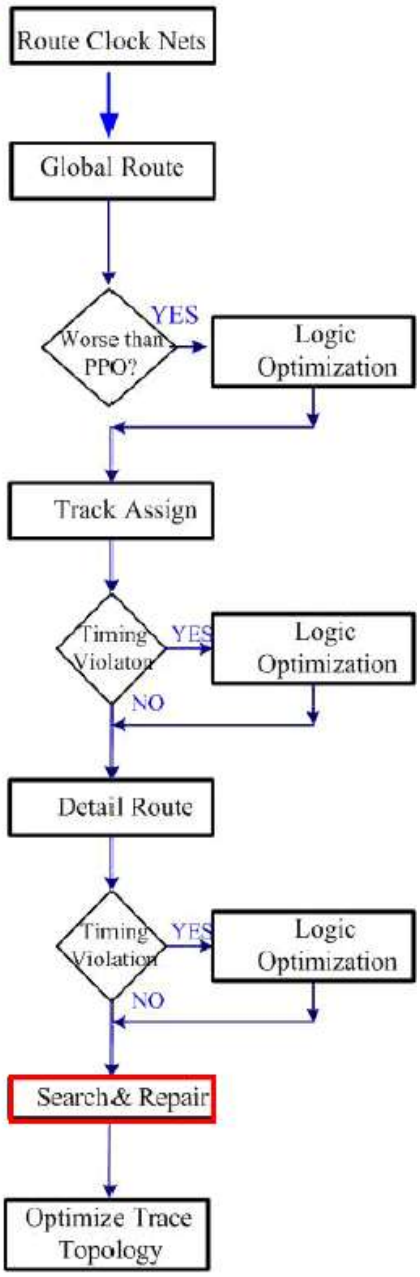


6-2-8. Search and Repair

Search & Repair fixes remaining DRC violations through multiple loops.

Select Route-> Detail Route: Search and Repair ...
Enter "50" on Search &Repair Loop





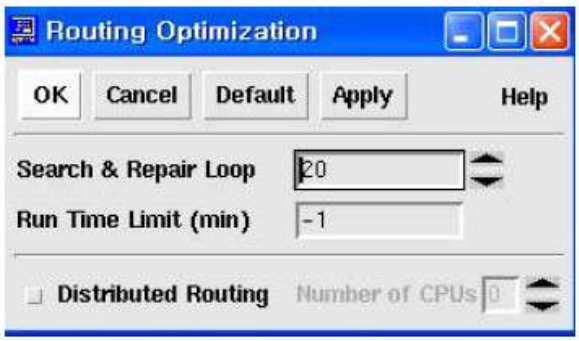
7. Change Delay Model

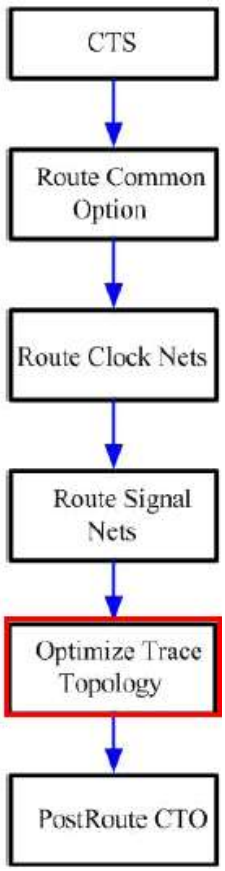
So far, the Delay Model was low or middle. But for actual chip operation, You should apply Delay Model to High Effort.

Select Timing-> AstroTime: Timing Setup ...
in Model
- change the Delay Model to High Effort in Net Delay Model

8. Trace Topology Optimization

Select Route -> Detail Route: Detail Route Wirelength Optimization ...

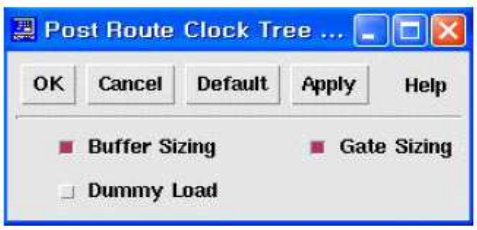


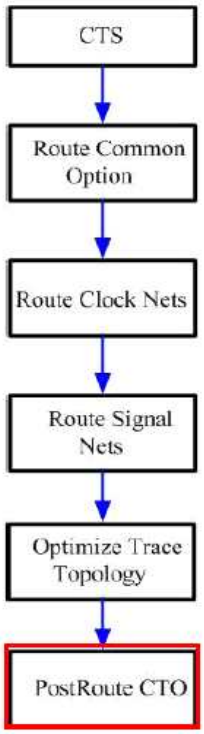


9. Post Route Optimization of Clock Skew

Select Clocks -> Clock tree optimization: Post Route CTO ...

Select buffer sizing and / or gate sizing





10. Items to check after routing has been finished

1. Timing Report: must be no violation (no minus slack, no max Cap / Trans)
2. DRC, LVS, advaced_DRC check: should have no violation.

10-1. DRC &LVS check

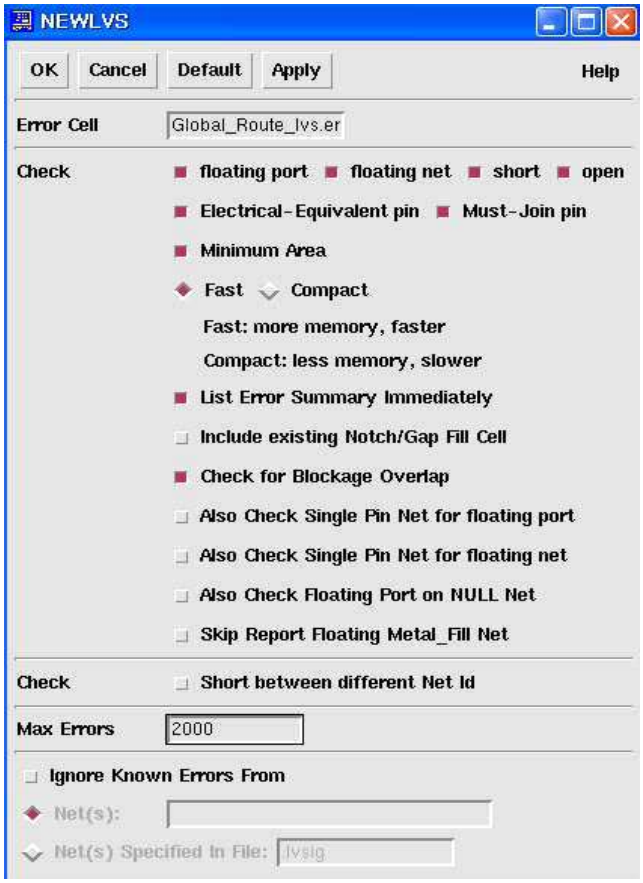
Before you check DRC/LVS, save and close the existing cell and then reopen the saved cell. Otherwise, it is applied to the existing cell. Satisfactory results may not be obtained. In addition, Max errors should be entered from 1000 to 2000 or more for more accurate inspection.

The option for error checking actually was "the Defaults value". Of course, you can define the other values for more accurate design. In particular, lots of "open errors' can occur during DFM (Design for Manufacturing) checking process, if the whole chip is covered by top metal. Therefore, you should avoid those errors by using other values instead of "the Defaults value".

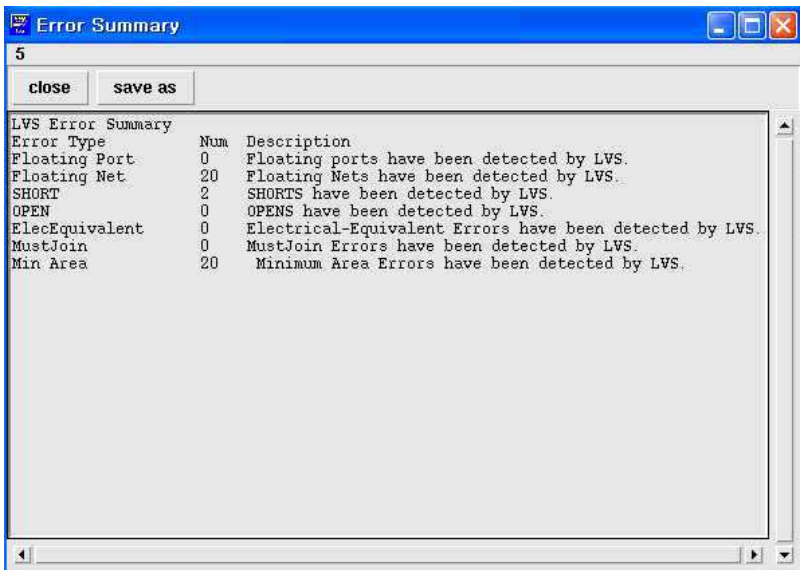
10-1-1. LVS

Verify-> LVS ...

select "List Error Summary Immediately"



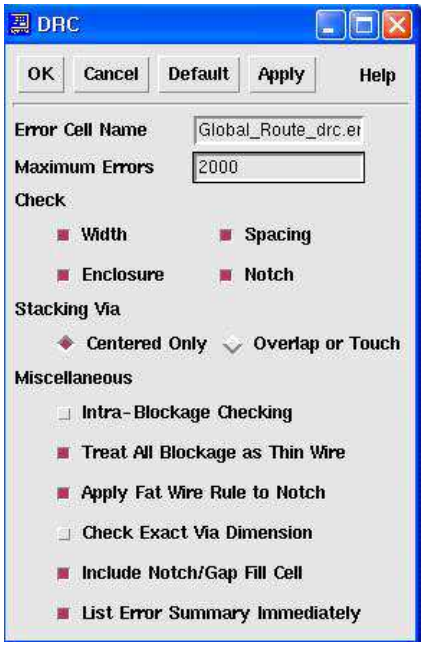
We recommend to save "LVE Error Summary" at a new file for later comparison.



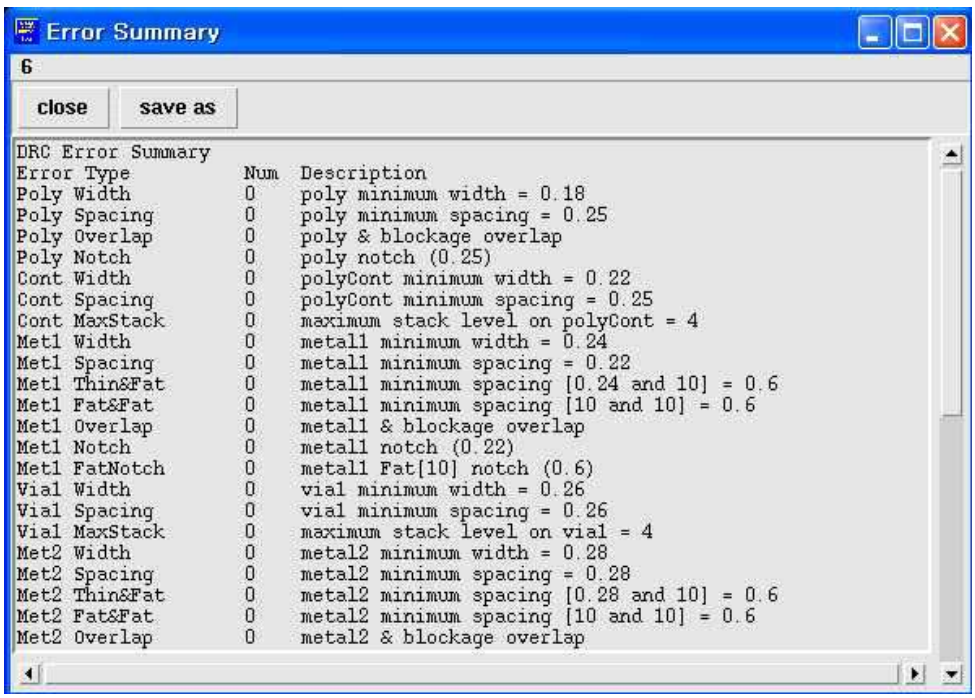
10-1-2. DRC

Verify-> DRC ...

select "List Error Summary Immediately"



We recommend to save "DRC Error Summary" at a new file for later comparison.



10-1-3. Advanced DRC

Verify-> Advanced DRC ...

We think "Advanced DRC" is more accurate than regular DRC. It is the same as the DRC using Hercules tool.

11. Tip for DRC &LVS

- Always store and exit the Cell before DRC &LVS check and then re-open the Cell.
- The results of LVS &DRC is best with "0" errors. If not, please go to the previous P&R design steps. We think errors occur if you do not follow the P&R design flow correctly. If you do not solve the problems due to the errors, the chip will not work after manufacture.

  Verify-> LVS ...
  Verify-> DRC ...
  Verify-> Advanced DRC ...

- in case of DRC / LVS errorr, run Search &Repair again. Most of the errors will be gone.
- If the error does not disappear after performing Search &Repair, run advanced process (to be added later), and if it still does not disappear, e-open the stored cells during routing processes, and check if there are any mistakes, especially the timing setup information.
- Another way is to add options during routing in case the errors are due to the routing steps.
- Also, I recommend check how you have chosen placement or CTS or Route common options. In some cases, if you run the P&R steps without an option, you may have thousands of errors

12 Tip for Timing Check

- Even if there is no LVS&DRC, slack can be negative small value in the timing report after routing. In the case of a small value, the routing is carried out from the beginning again. Increase the frequency of search&repair and try the effort as **High**. There is also a way to try **High Effort**. If it still does not disappear or minus slack and the value is large, find the path where this problem occurs in the Timing Report. You will have to find a cell and find an alternative.
- If Max Cap/Trans does not disappear, Once check whether the violation type is S, C, or G and see if there is a value that is fixed by the problem in the design. If so, you can fix it by modifying the DC or ASTRO custom values, or It may be necessary to modify the design itself. If not, try Search&Repair once. And if the results are not satisfied, run Routing or CTS or placement again. At this time, the target value of Astro is less than DCconstraint, and then perform the DRC / LVS test with the value of 0 and check if the violation comes out.
- In the case of Timing Check, even though you do not any violation until CTS, make sure you have not set the delay model to low or middle. If you change effort to **High**, violation may occur.

Lab6. Design For Manufacturing (DFM)

I recommend you do refer to the "ICC User Guide.pdf" file for Design for Manufacturing (section 9).

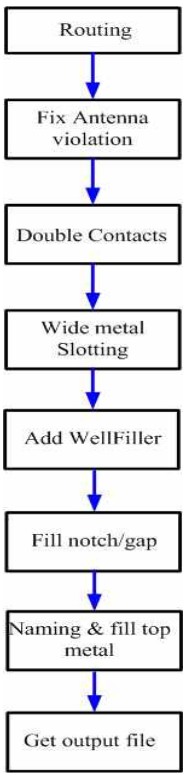
What you should know before doing DFM

DFM may differ from PDKs or foundries. This course is based on the Samsung 180nm process.

**** Basic DFM flow *****

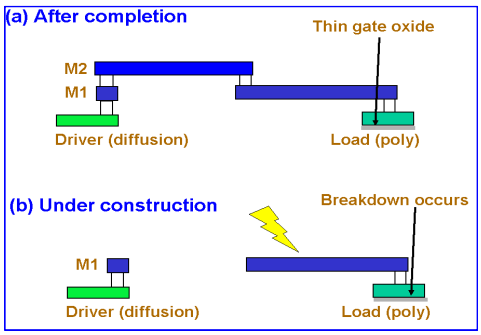
1. Fix Antenna violation (introduce two methods)
2. double Contacts
3. Wide metal slotting
4. Add WellFiller
5. Fill notch / gap
6. Naming a chip (Samsung does not really want!!)
6. Covering a chip with two top metals (Samsung does not really want!!)
7. Get output files

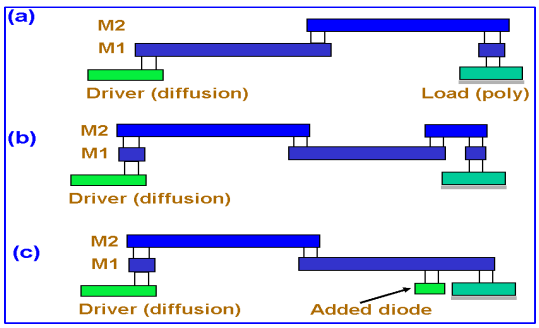
- PR Summary
- Save LVS &DRC error reports
- Delay information extraction (SDF file)
- Parasitic Output Extraction (.SPEF, .DSPF)
- Netlist file extraction (.v) -> 2 ways
- GDS file extraction



1. Fix Antenna violation

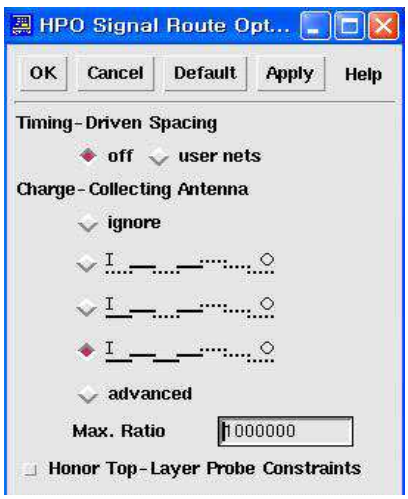
In chip manufacturing, gate oxide can be easily damaged by electrostatic discharge. The static charge that is collected on wires during the multilevel metallization process can damage the device or lead to a total chip failure. The phenomena of an electrostatic charge being discharged into the device is referred to as either antenna or charge-collecting antenna problems. To prevent antenna problems, IC Compiler verifies that for each input pin the metal antenna area divided by the gate area is less than the maximum antenna ratio given by the foundry:





In order to prevent such an antenna violation, two methods are proposed in Astro (IC Complier). One is to apply the antenna rule proposed in Astro. The other is to apply an antenna rule file from a foundry vendor. Here, we will introduce the first method.

1. Select Route Setup -> HPO Signal Route Options ...



2. From top to bottom in Charge-Collecting Antenna
Select fourth ("include all lower-layer segments") and Press "OK".
3. On the Astro execution window
Enter the command "axReportAntennaRatio (geGetEditCell)" and Press Enter.

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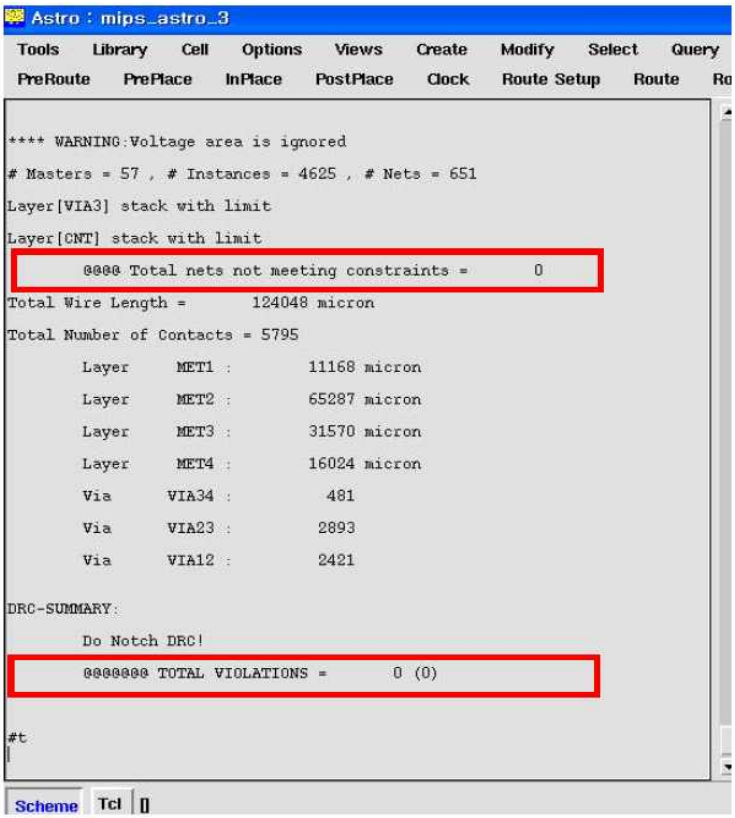
The first and second steps of what we just did is to decide which antenna rule to apply to this cell. The third is to test the cell based on the applied antenna rule. The test below shows that special antenna violation is not noticeable.



If the red part of the execution result is not 0, it should be corrected. You can basically fix it with Search&repair that you did in Routing.

4. Select Route -> Detail Route: Detail Route Search &Repair
5. Click "OK"

Once Search &Repair is done, check the antenna violation again.

6. Enter the command "axReportAntennaRatio (geGetEditCell)" in the Astro execution window. Press the Enter key. If the violation is 0, it does not matter. But if it is not 0, you should insert the antenna diode.
7. Select Route Utility-> Charge-Collecting Antenna: Insert Diode with Checking...
8. Select "Always" under the Routing section and Click "OK"
9. Inspect the antenna violation again.

If there is no antenna violation,

10. Select Route Setup -> HPO Signal Route Options ...
11. Select "ignore" in Charge-Collecting Antenna and press "OK" button. Antenna rule check is over.

The second method to fix Antenna violation is applied when the antenna rule file is given.

1. Write load "path/antenna rule filename" on execution window and Enter
ex) Here, load "scripts/s35_4m_antenna.cmd"
2. Select Route Setup -> HPO Signal Route Options ...
3. Select advanced and press OK.
4. The procedure below is the same as the first one. Samsung AntennaRule.cmd file used in 0.35um process (I have slightly Modified it for 0.18um process. Be careful it may be wrong.)

```
define _libId (dbGetCurrentLibId)
dbClearLibAntennaRules _libId
dbDefineAntennaRule _libId 1 2 100 20
dbAddAntennaLayerRule _libId 1 "MET1" 100 '(0.203 0 400 3700)
dbAddAntennaLayerRule _libId 1 "MET2" 100 '(0.203 0 400 3700)
dbAddAntennaLayerRule _libId 1 "MET3" 100 '(0.203 0 400 3700)
dbAddAntennaLayerRule _libId 1 "MET4" 100 '(0.203 0 8000 50000)
dbAddAntennaLayerRule _libId 1 "VIA1" 5 '(0.203 0 83.33 75)
dbAddAntennaLayerRule _libId 1 "VIA2" 5 '(0.203 0 83.33 75)
dbAddAntennaLayerRule _libId 1 "VIA3" 5 '(0.203 0 83.33 75)
```

2. Double Contacts

The contact (via) that literally connects metal and metal, metal and cell. When the via is doubled, the contact surface between the two becomes larger and delay will be reduced. Also, a mistake in the process can be avoided if double contacts are used.

How to run

1. Write load "path/cmd file name" on execute window. For Samsung PDK, load "scripts/optContacts.cmd".

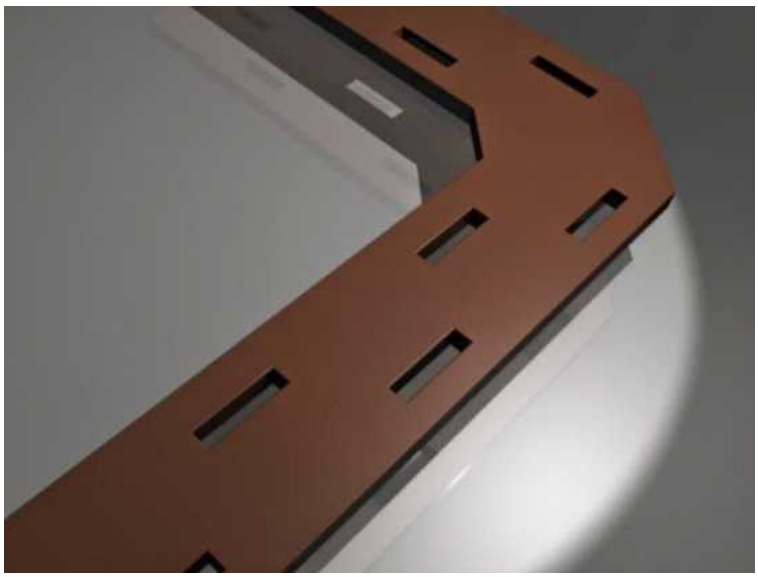
cmd file contents for double contact used in Samsung 0.18um process:

```
;; Optimize Contact
axDrouteOptimizeContact (geGetEditCell) '(
(& Quot; VIA 12 &quot; &quot; VIA 12 &quot; 2)
(& Quot; VIA23 &quot; &quot; VIA23 &quot; 2)
(& Quot; VIA34 &quot; &quot; VIA34 &quot; 2)
)
```

When execution is completed, Check DRC and You can find the error.

3. Slotting Wire

Metal (wire) slotting is used for reducing stresses on the wire. For example, if a wide metal wire is slotted, also called "cheesing", the thermal stress can be reduced.



1. write load "path / corresponding .cmd file" on execution window
Here, load "scripts / sloting_Metal.cmd"

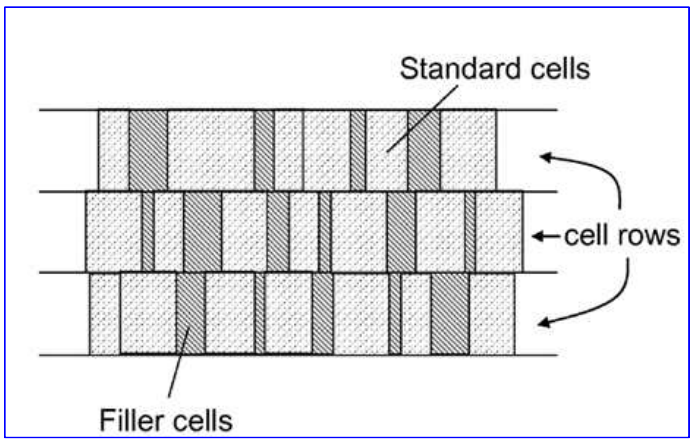
Contents of cmd file for Sloting Wire in Samsung 0.18um:

```
axgSlotWire
configureWindow 4 "650x678 + 507 + 293"
setFormField "Wire Slot" "Net Name" "VDD, VSS"
setFormField "Wire Slot" "CutWidth 0" "2"
setFormField "Wire Slot" "CutWidth 0" "20"
setFormField "Wire Slot" "CutLength0" "1"
setFormField "Wire Slot" "CutLength0" "10"
setFormField "Wire Slot" "CutLength0" "100"
setFormField "Wire Slot" "Width 0" "5"
setFormField "Wire Slot" "Length 0" "50"
setFormField "Wire Slot" "SideSpace 0" "5"
setFormField "Wire Slot" "EndSpace 0" "5"
setFormField "Wire Slot" "SideClearance0" "5"
setFormField "Wire Slot" "EndClearance0" "5"
formApply "Wire Slot"
formCancel "Wire Slot"
```

If you want to run it manually, select PreRoute -> Slot Wires ...

4. Fill WellFiller

After routing is complete, you can fill small gaps that violate the spacing rule for the well layer with well filler cells. You can fill gaps between cells in the same row or between rows.



axgAddWellFiller
setFormField "Add Well Filler (IntraCell)" "Layer" "6"
formOK "Add Well Filler (IntraCell)"

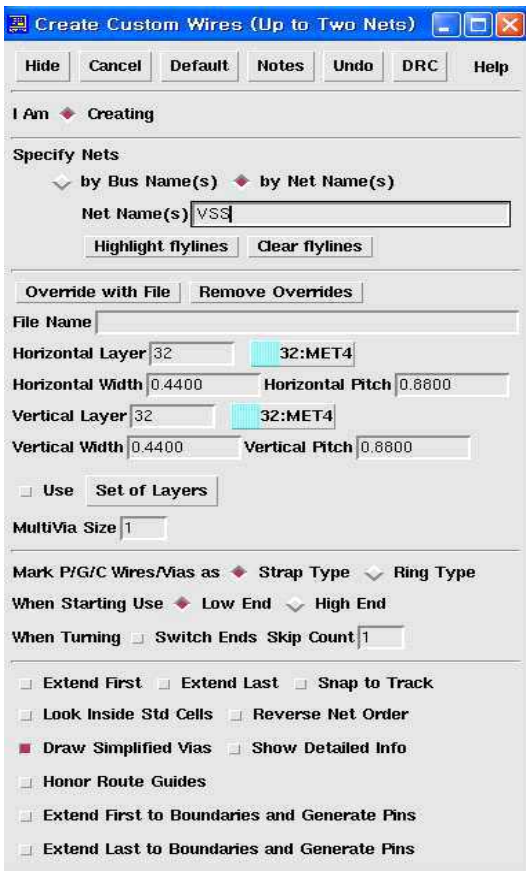
5. Fill Notch/Gap

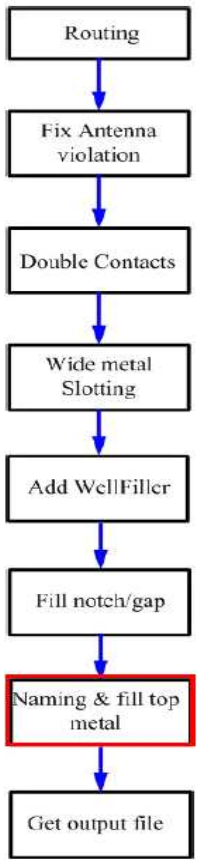
geNewFillNG
formOK " New Fill Notch and Gap "

6-1. Naming

at the corner cell in the bottom left of the chip, Top Metal (here Metal4) is used to draw the "name of your chip" using a mouse manually.

- Select PreRoute-> Custom Wires

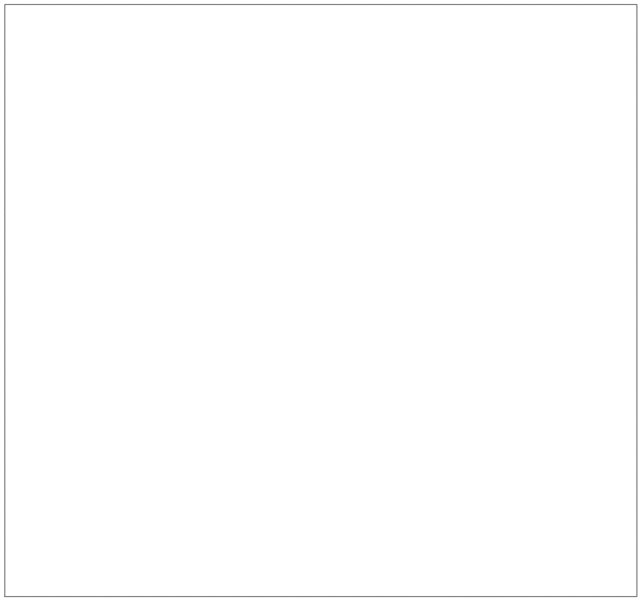




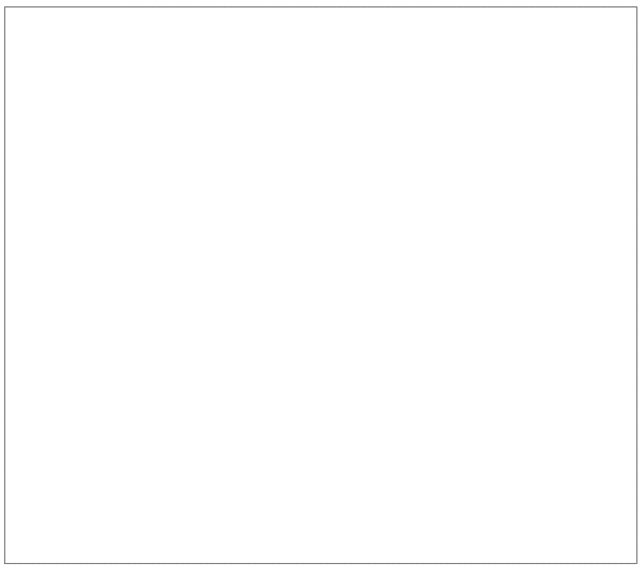
In the following figure, the initials "KHCJM", You can see that it is written.

6-2 Fill Top Metal

- Select Route Utility -> Fill Wire Track ...
- Click "Default"
- Select self in the Output to field
- Set the From Metal option to 2
- Set To Metal option to 4
- Click "OK"



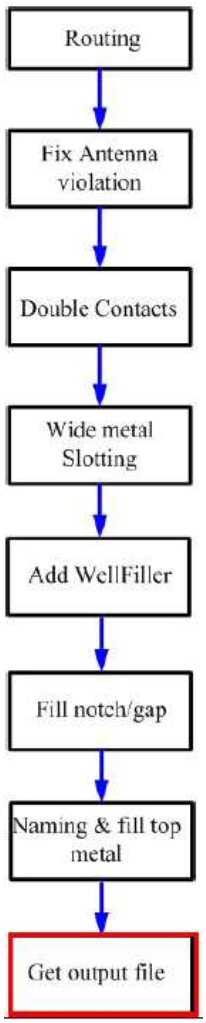
The figure below shows the Cell after execution.



7. hot to get output files

Now all of ASTRO's process is finished. For the tools to be used after finishing Astro P&R, you should get the following results.

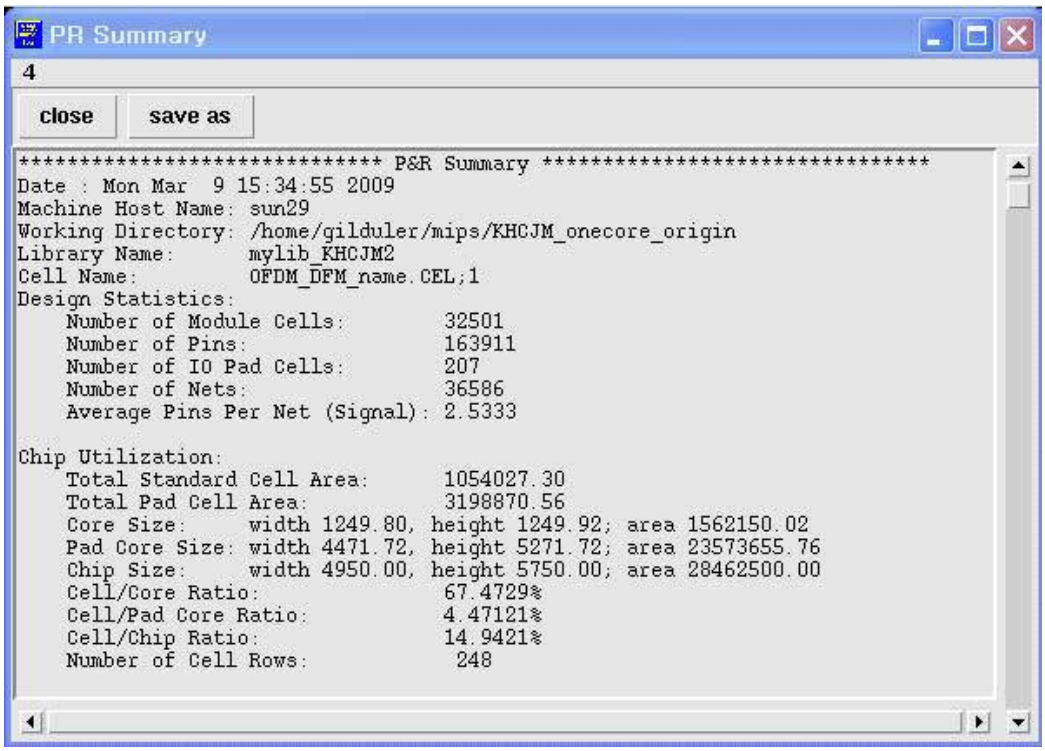
1. PR Summary
2. Save the LVS &DRC error report
3. Delay information extraction (SDF file)
4. Parasitic Output Extraction (.DSPF)
5. Netlist file extraction (.v) -> 2 things
6. GDS file extraction



7-1 PR Summary

Select Query -> List PR Summary!

- PR Summary reports place and route detailed results.
- Press "save as" to save it.

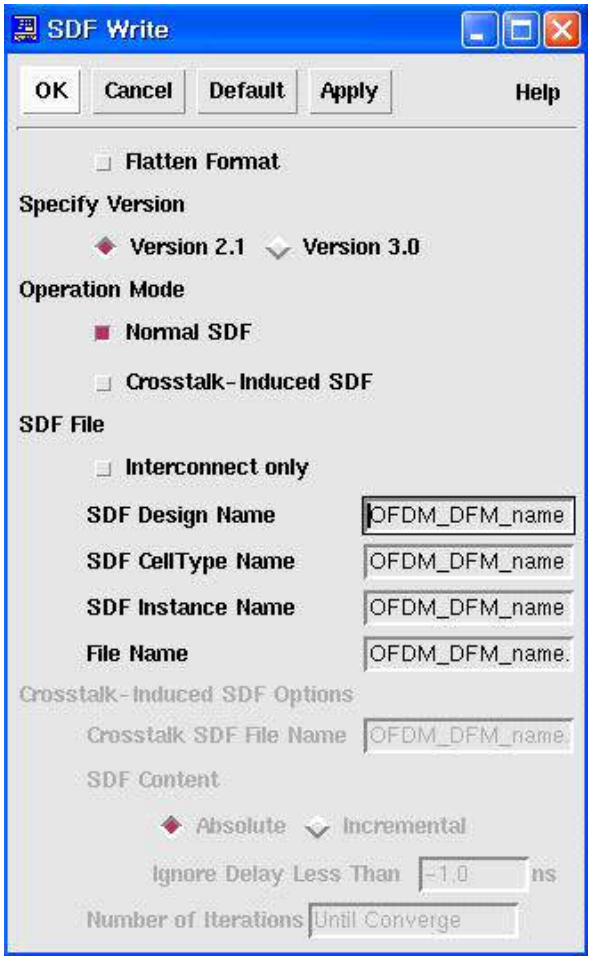


7-2 Save LVS &DRC error report

The method of extracting and storing the LVS and DRC errors is the same as the way done after the DRC.

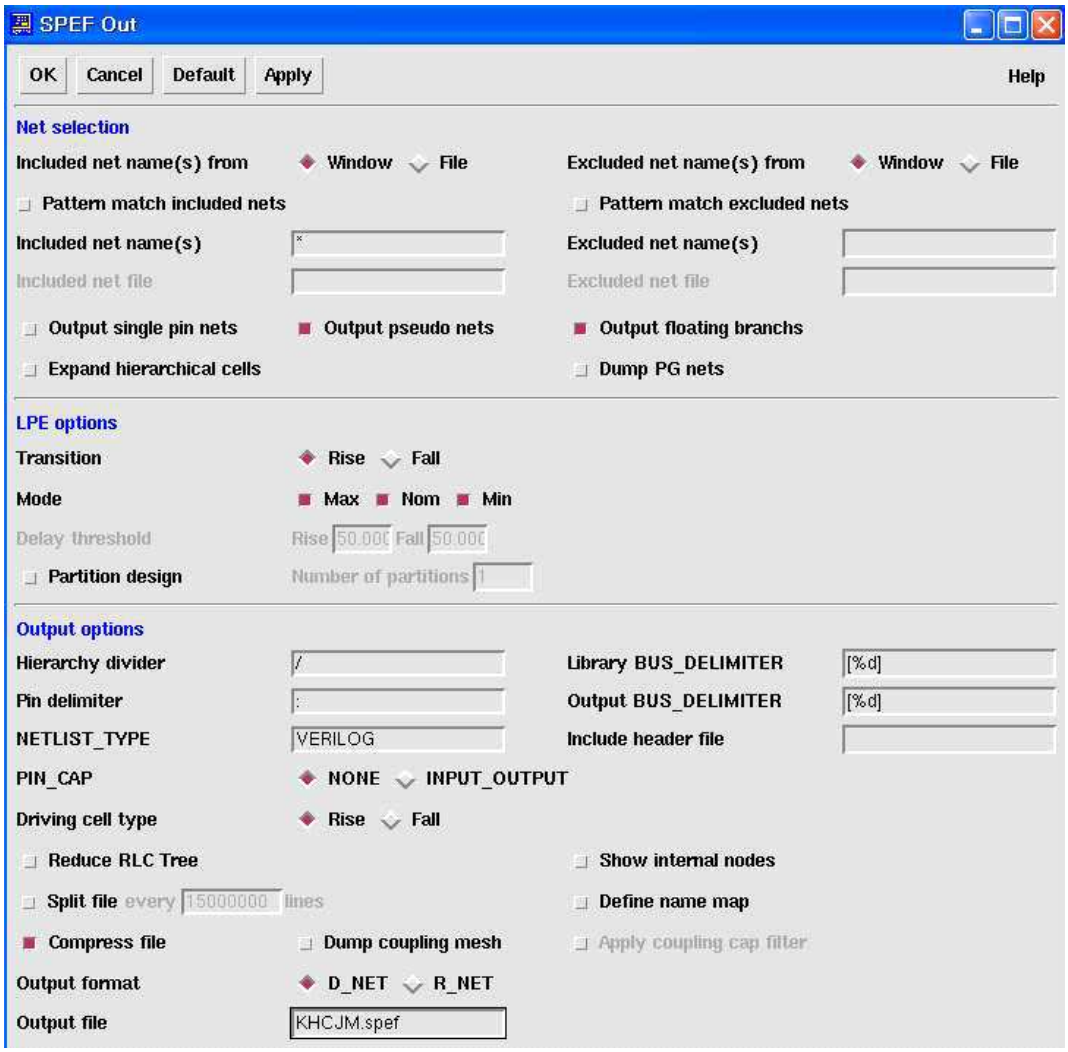
7-3 Delay information extraction (SDF file)

Select Timing-> Delay Output: SDF Out ...



7-4-1. Parasitic Output 1 Extraction (.SPEF)

Select Timing -> Parasitic Output: SPEF Out ...
Click "Default"
Unselect the "Output single pin nets" option near the top
Unselect the "Reduce RLC Tree" near the bottom of the dialog box
Select Compress file to creat .gz file
Enter Cell name .spef as the Output file
Click "OK"



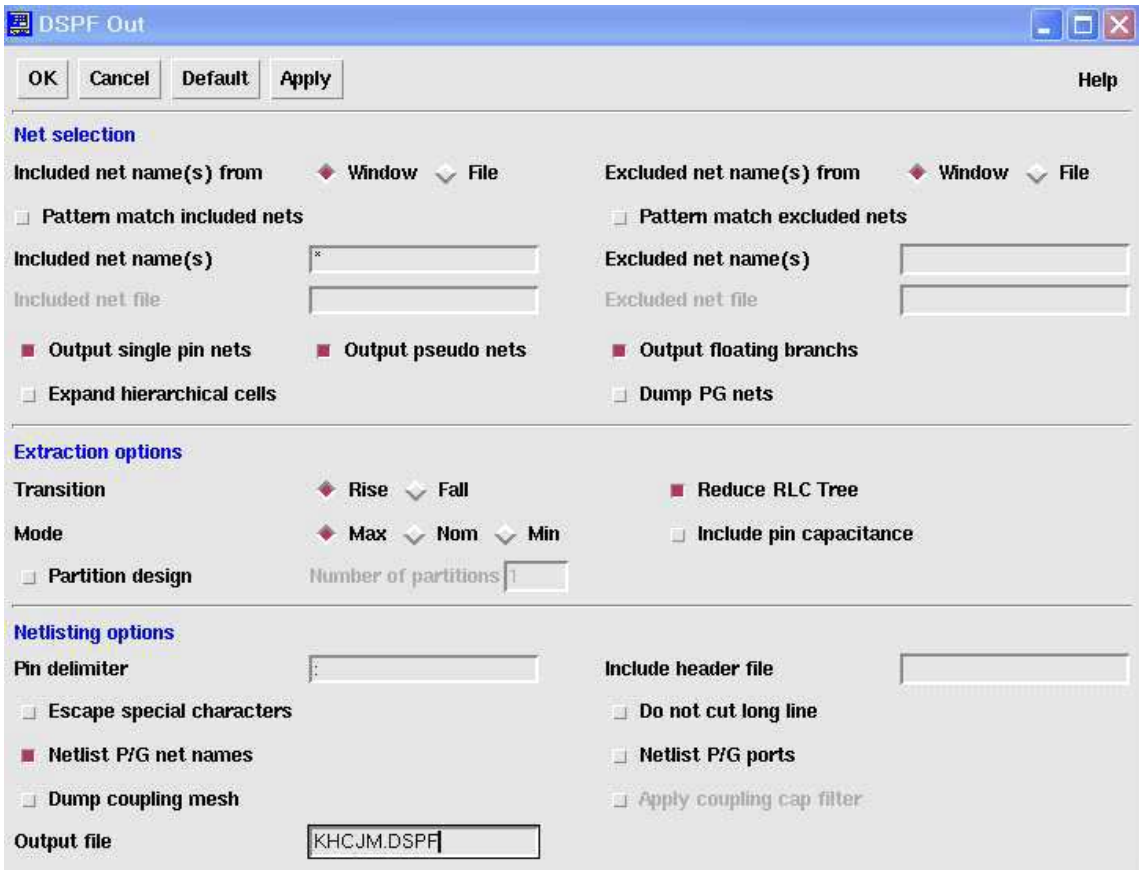
7-4-2 Parasitic Output 2 Extraction (.DSPF)

Select Timing -> Parasitic Output: DSPF out ...

Click "Default"

Enter Cell name .DSPF as the Output file

Click "OK"



7-5. Netlist file extraction (.v) -> 2 ways

1. Select Cell -> Save!
2. Select Cell -> Close ...

Select Discard All

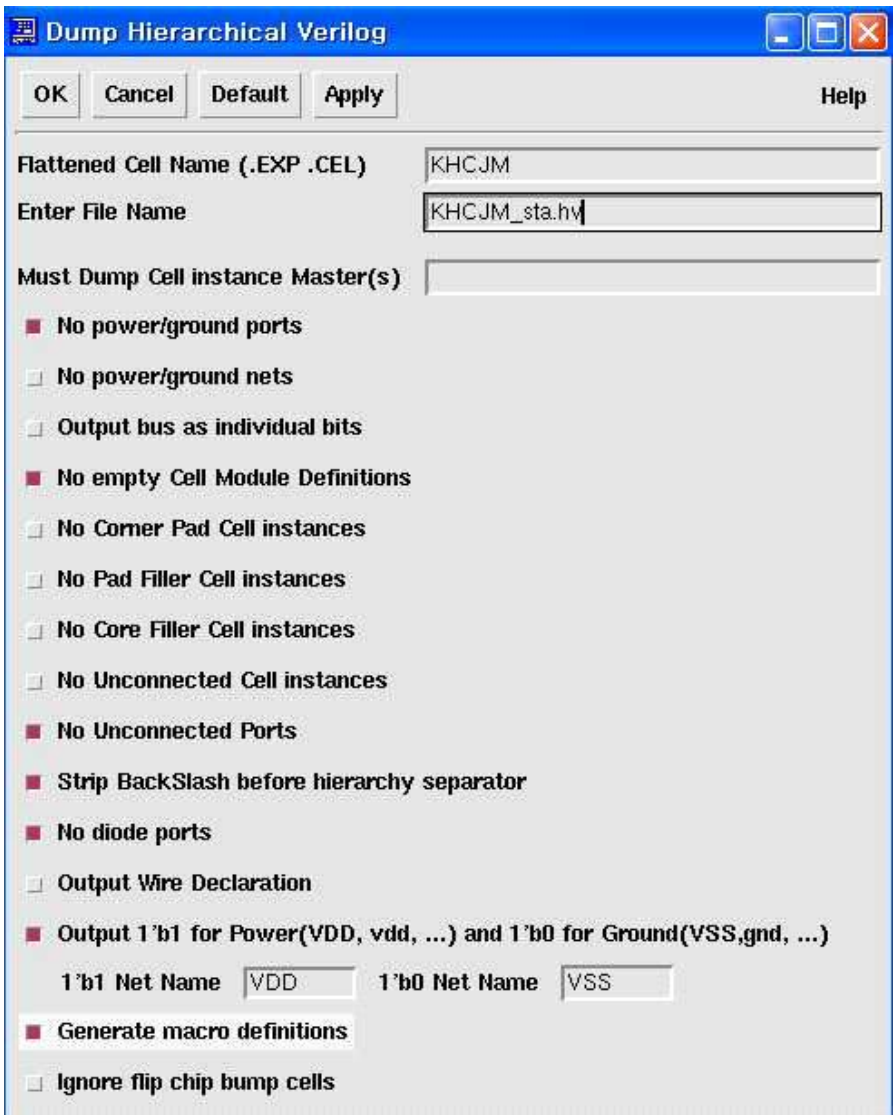
Select "OK"

3. Netlist extraction for Prime time

Select Cell -> Hierarchy Preservation: Hierarchical Verilog Out ...

Select the option as shown below and enter the Cell Name and File Name.

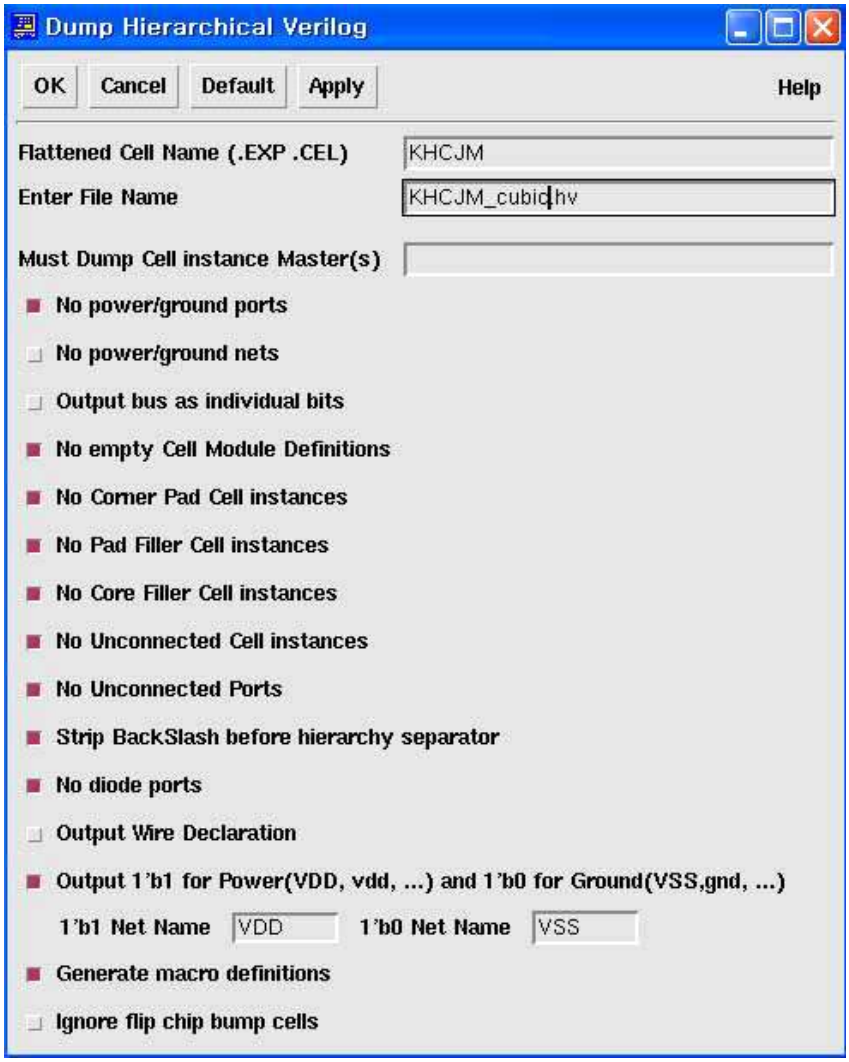
Then click OK



4. Extract netlist for use in Cubic

Select Cell -> Hierarchy Preservation: Hierarchical Verilog Out ...

Select the option as shown below and enter the Cell Name and File Name. Then click OK.

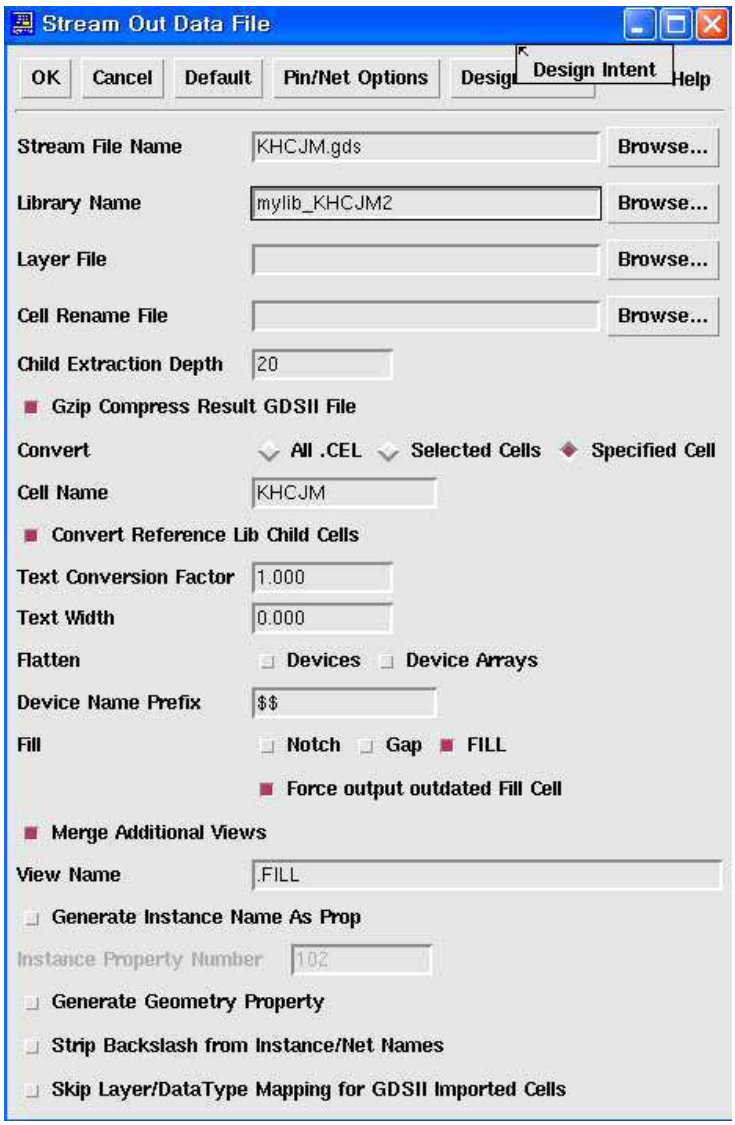


7-6. GDS file extraction

Select Tool -> Data Prep

Select Output -> Stream Out ...

Select the following options and enter the Stream File Name (cell name.gds), Library Name (Name of library you worked on), Child Extraction Depth (about 20), Cell Name, View Name(.FILL) and press OK.



--- END ---