VLSI Systems Designs: Quiz1 (2018 Spring)

04/10/2018, 09:00-10:20 Prof. Jinsang Kim

Part I: ***If not specified,*** *use 45nm process technology of the following parameters:* $V_{DD} = 1.0\,V$, $V_{t0} = \pm 0.3\,V$ for $NMOS$ and $PMOS$, $\beta_n = 200 \cdot \frac{W_n}{L_n} A/V^2$, $\beta_p = 100 \cdot \frac{W_p}{L_p} A/V^2$, $\Phi_s = 0.3\,V$, $\gamma = 0.2\,V^{0.5}$, $\lambda = 0.02$.

1. **(15pts)** A pMOSFET of W_p/L_p=4 has the following initial terminal voltages: gate=0.0V, source=0.8V, drain=0.1V
   a) (10pts) calculate the current difference between an ideal and a nonideal transistor when the body is Vdd.
   b) (5pts) estimate the switching delay of the nonideal transistor in case the equivalent transistor capacitance is 0.005pF.

2. **(30pts)** Given $\overline{Y} = AB + CDE$
   a) (10pts) design the circuit of a CMOS compound gate with size information.
   b) (10pts) do layout
   c) (10pts) when the input and output load capacitance is 1fp and 3fP, respectively estimate the delay from signal 'A' to 'Y' using logical effort

3. **(10pts)** Briefly discuss the mechanism of drain-induced barrier lowing and gate-induced drain leakage.

4. **(15pts)** Four 2-input NAND gates are connected in series, estimate the delay of the circuit and decide the sizes of the gates when input and output capacitances are 4fF and 16fF, respectively.

5. **(10pts)** An 8x inverter drives the two metal wires and there is a 4x inverter at the end of the wires. The wires are 1 um long and 2λ wide with the sheet resistance of 0.08 and $C_{permicron}$ of 0.2fF/um. Assume that the gate capacitance of a unit inverter is C=1fF/um and resistances of both nMOS and pMOS are $R = 2.5\,K\Omega \cdot \mu m$. Estimate the delay from the driver to load when an input changes from '1' to '0'.

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