Positive, negative and zero setup time

As we know from the definition of setup time, setup time is a point on time axis which restrains data from changing after it. Data can change only before occurrence of setup timing point. **Theoretically, there is no constraint on occurrence of setup time point with respect to clock active edge**. It can either be before, after or at the same time as that of clock edge. Depending upon the relative occurrence of setup time point and clock active edge, setup time is said to be positive, zero or negative.

Positive setup time: When setup time point is before the arrival of clock edge, setup time is said to be positive. Figure 1 below shows positive setup time.

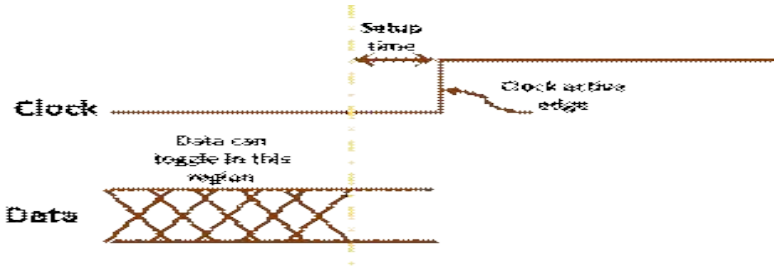


Figure 1: Positive setup time

Zero setup time: When setup time point is at the same instant as clock's active edge, setup time is said to be zero.

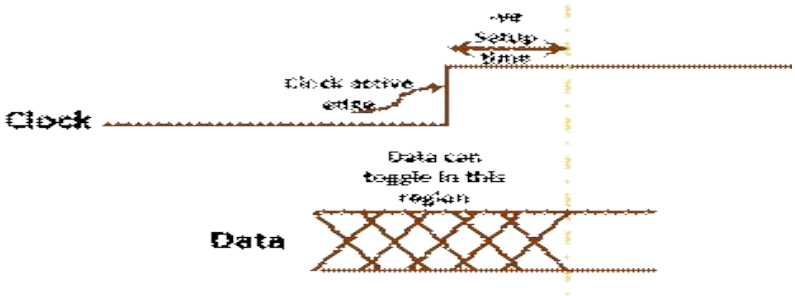


Figure 3: Negative setup time

negative setup time: When setup time point occurs after clock edge, setup time is said to be negative. Figure 3 shows timing waveform for negative setup time.

What causes different values of setup time: We have discussed above theoretical aspects of positive, zero and negative setup time. Let us go a bit deeper into the details. Figure 4 shows a positive level-sensitive D-latch. As we know from the definition of setup time, setup time depends upon **the relative arrival times of data and clock at input transmission gate** (We have to ensure data has reached up to NodeD when clock reaches input transmission gate). Depending upon the relative arrival times of data and clock, setup time can be positive, zero or negative.

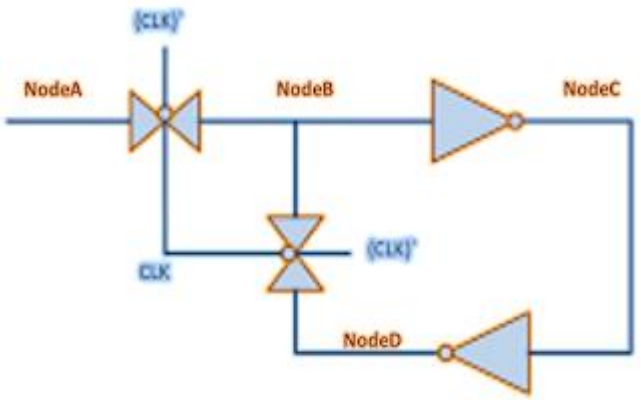


Figure 4: Positive level-sensitive latch

Let us assume the delay of **an inverter is 1 ns.** Then, to ensure that the data has reached NodeD when clock edge arrives at input transmission gate, data has to be available at the input transmission gate at least 2 ns before. **So, if both data and clock reach the reference point at the same time, the latch has a setup time of 2 ns.**

Now, if data takes 1 ns more than clock to reach input transmission gate from the reference point, then, data has to reach reference point at least 3 ns before clock reference point. In this case, setup time will be 3 ns.

Similarly, if data takes 1 ns less than clock to reach input transmission gate, setup time will be 1 ns. **And if data takes 2 ns less than clock to reach input transmission gate, setup time will be zero.**

Now, if there is further difference between delays of data and clock from respective reference points to input transmission gate, the hold time will become negative. For example, i**f data takes 3 ns less than clock to reach input transmission gate, setup time will be –1 ns.**

This is how setup time depends upon relative delays of data and clock within the sequential element. And it completely makes sense to have negative setup time.

Positive, negative and zero hold time

As we know from the definition of hold time, hold time is a point on time axis which restrains data from changing before it. Data can change only after hold time has elapsed. Now, there is no constraint on the occurrence of hold time point with respect to clock edge. It can either be after, before or at the same instant of time as that of clock active edge.

Posotive hold time: When hold time point is after the arrival of clock active edge, hold time is said to be positive hold time. Figure 1 below shows positive hold time.

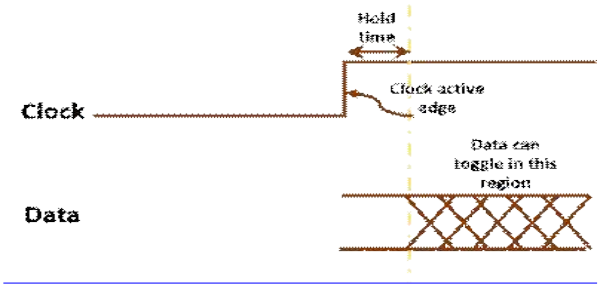


Figure 1: Positive hold time

Zero hold time: When hold time point is at the same time instant as that of clock active edge, we say that hold time of the sequential element is zero.

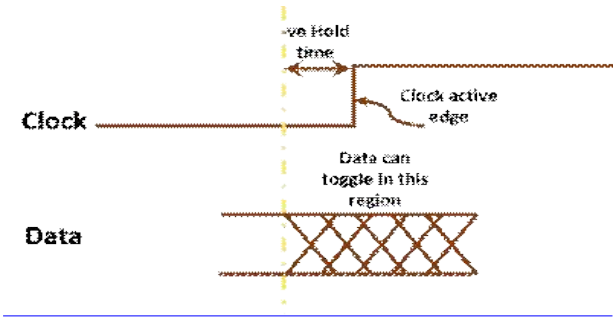


Figure 3: Negative hold time

Negative hold time: Similarly, when hold time point comes earlier on time scale as compared to data, we say that hold time of the sequential element is negative.

We have discussed above theoretical aspects of positive, zero and negative hold time. Let us go a bit deeper into the details. Figure 4 shows a positive level-sensitive D-latch. **As we know (from definition of hold time), hold time depends upon the relative arrival times of clock and data at the input transmission gate** (We have to ensure data does not reach NodeC). Depending upon the times of arrival of clock and data, hold time can be positive or negative.

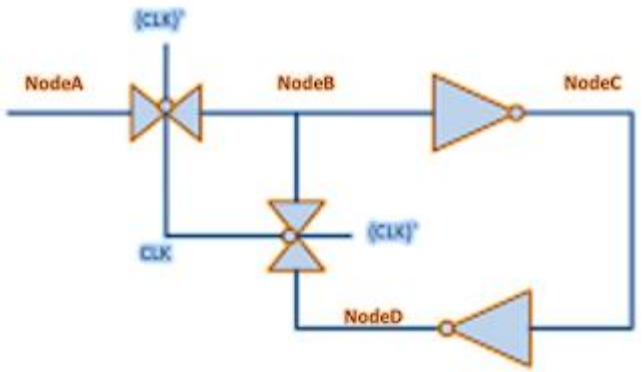


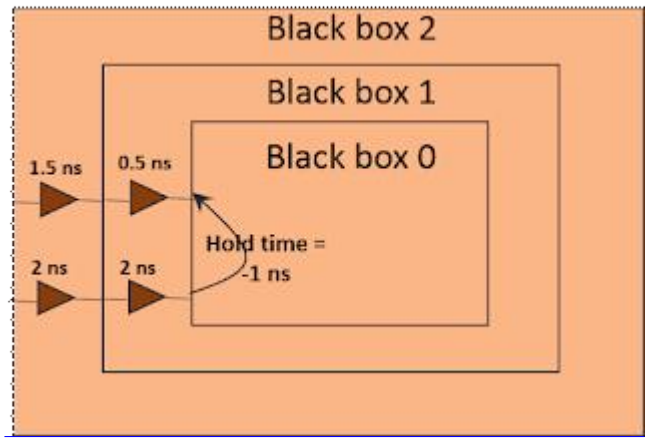
Figure 4: Positive level-sensitive D-latch

Let us say, the delay of an inverter is 1ns. Then, we can afford the data to reach transmission gate input even **0.9ns** before arrival of clock at transmission gate. This will ensure data reaches NodeC (-0.9+1=) **0.1ns** after arrival of clock edge, if allowed. But, since, clock closes transmission gate, data will not reach NodeC. **So, in this case, hold time is -1ns**. If the delay from NodeB to NodeC was something else, hold time would also have been different.

Now, **if we say that clock arrives at transmission gate 1ns earlier than data, then, by above logic, hold time of this latch will be** –2ns. Similarly, if clock arrives at transmission gate 0.5ns after data, hold time will be –0.5ns.

And if clock arrive at transmission gate 1ns after data, hold time will be zero. If the arrival time of clock is made more late, hold time will be greater than zero. For example, if arrival time of clock is 2ns after data, hold time will be +1ns.

Hold time of the circuit is also dependent upon the reference point. For example, consider a multi-level black box as shown in figure 5. **If we look at black box 0**, its hold time is -1 ns. At level of black box 1, wherein clock travels 2ns and data travels 0.5ns to reach black box 0, hold time is (-1+2-0.5=) 0.5ns. Similarly, at the level of black box 2, hold time is 1ns. **This is how, hold time depends upon the relative arrival times of clock and data.** And it completely makes sense to have a negative hold time.



source: https://vlsiuniverse.blogspot.com/2017/01/negative-hold-time.html