EE 716 Digital IC Design Term Project

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Design Proposal: RISC-V CPU

I. Introduction:

RISC, or *Reduced Instruction Set Computer*. is a type of microprocessor architecture that utilizes a small, highly-optimized set of instructions, rather than a more specialized set of instructions often found in other type of architectures.

RISC (Reduced Instruction Set Computer) is used in portable devices due to its power efficiency. For Example, Apple iPod and Nintendo DS. RISC is a type of microprocessor architecture that uses highly-optimized set of instructions. RISC does the opposite, reducing the cycles per instruction at the cost of the number of instructions per program Pipelining is one of the unique features of RISC. It is performed by overlapping the execution of several instructions in a pipeline fashion. It has a high performance advantage over CISC.

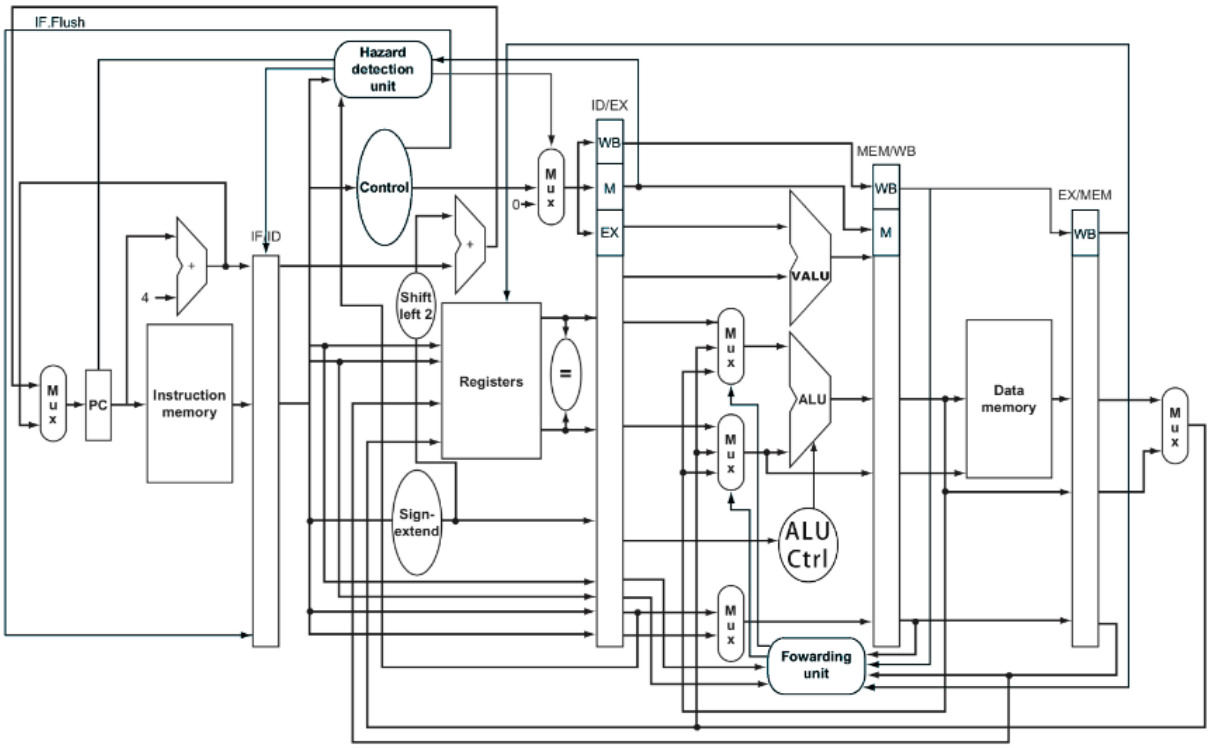
Main characteristics of RISC architectures:

- The instruction set is limited and includes only simple instructions.
    - Simple and small decode and execution hardware are required.
    - The CPU takes less silicon area to implement and runs also faster.
- Execution of one machine instruction per clock cycle.
- Register-to-register operations.
- Only LOAD and STORE instructions reference data in memory.
- Instructions use only few addressing modes.
    - Almost all RISC instructions use simple register addressing
    - Complex modes can be synthesized in software from the simple ones
- Instructions are of fixed length and uniform format.

    - Loading and decoding of instructions are simple and fast. It is not needed to wait until the length of an instruction is known in order to start decoding it.
    - Decoding is simplified because the opcode and address fields are located in the same position for all instructions.
- A large number of registers is available.
    - Variables and intermediate results can be stored in registers and do not require repeated loads and stores from/to memory.
    - All local variables of procedures and the passed parameters can be stored in registers.
- Less design complexity, reducing design cost, and reducing the time between designing and marketing.

In this project, we implement a 32-bit 5-stage pipelined RISC-V that supports basic instructions and some arithmetic.

II. Block Diagram:



III. Pin description:

No.	Pin	I/O	Description
1	clk	Input	Input clock signal
2	instr_i[7:0]	Input	Reads in instructions 8-bit at a time
3	dataorreg	Input	Output value saved in Data Memory, else output value saved in register
4	addr	Input	Address that you want to access, this input is 5-bit since size of both data memory and register are 32
5	value_o_addr	Input	The value saved in memories are 32-bit, but our CPU can only output 8-bit at a time. Thus, we need to decide which 8-bit are to be read.
6	rst	Input	Reset input signal
7	value_o	Output	Output value
8	is_positive	Output	This is for handling overflow cases when doing vector sum.