EE714 VLSI Systems Designs: Quiz#1 (2020 Fall)

Due: 09/29/2020 PM6:00, submit by email to me(jskim27@khu.ac.kr) the Prof. Jinsang Kim

Assume that a matched unit inverter has widths of 45nm for nMOS and 90nm for pMOS, respectively. The 45nm process technology uses the followings unless stated otherwise:
$V_{DD} = 1\,V,\ Vto = 0.3\,V, \beta_n = 1mA/\,V^2, \Phi_s = 0.6\,V, \gamma = 0.3\,V^{0.5}, \lambda = 0.02, \tau = 3RC = 3ps,$
$electron velocity = 10^5 cm/s$

1. (15pts) Calculate the current of the bottom pMOS transister of 2-input NOR gate when the output voltage is 0.7V.
2. (15pts) Explain the 2nd order effects of MOSFETs.
3. (15pts) Explain the aging effects and their solutions of MOSFETs.
4. (40pts) Given Y= (AB+CDE)F (complementary inputs are available)
   a) draw a **one-stage** transistor-level CMOS circuit diagram
   b) determine the size of all transistors
   c) show the layout of this circuit
   d) estimate the rising propagation delay when the load is a 2-input NOR gate. Explain the details of the delay components.
   e) estimate the falling contamination delay when the load is a 2-input NOR gate. Explain the details of the delay components.
5. (15pts) A back-to-back flip-flop circuit suffers from the race condition if there is clock skew between flip-flops. One of the solutions to this problem is that the use of a buffer chain. Decide how many inverters are needed by assuming that the clock skew is 5ps.
6. (15pts) Try to graphically estimate the two noise margins of a skewed inverter of Bn=1.5Bp.