

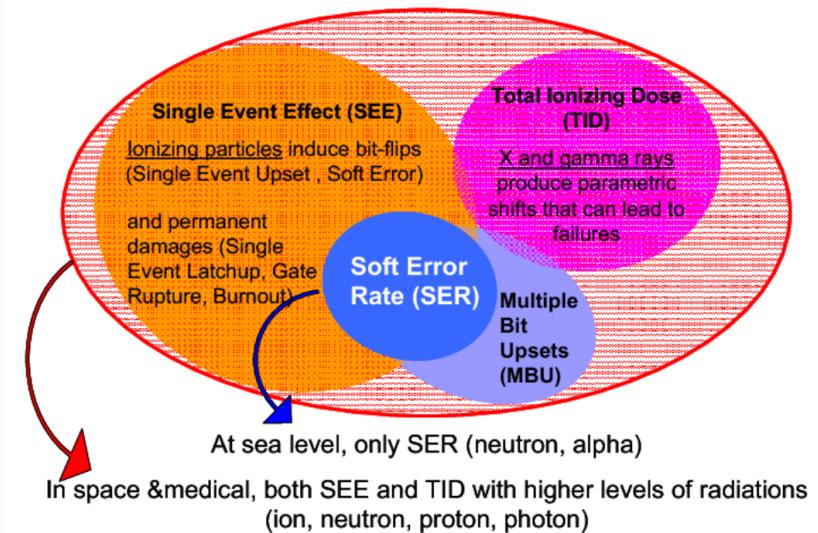
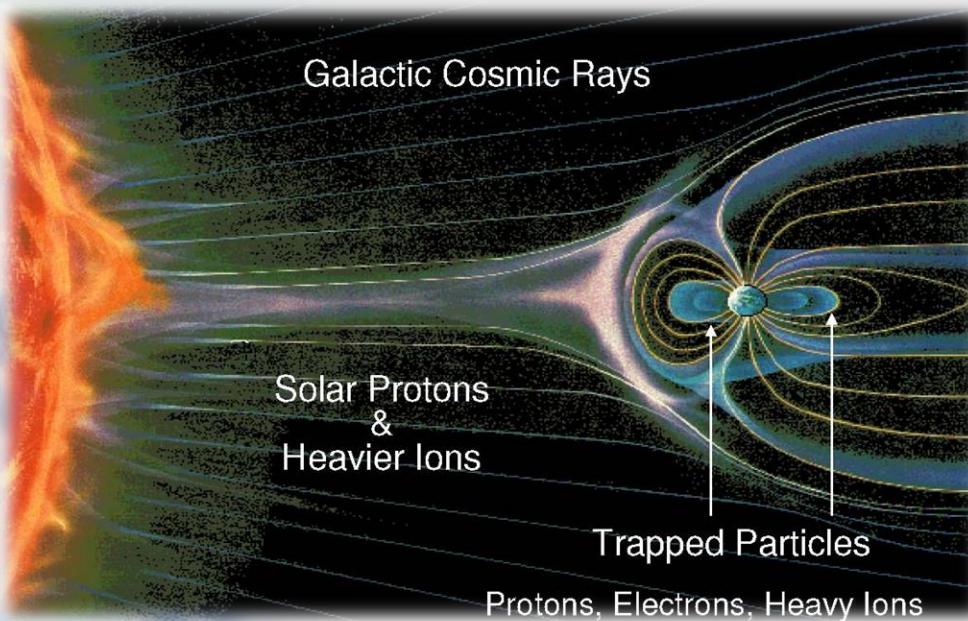
# Radiation-Hardening by Design (RHBD)

경희대학교 장 익준 교수

- **Research Background**
- **SEU-Hardening Design Techniques**
- **TID-Hardening Design Techniques**
- **Radiation Damage in DRAM**
- **Conclusion**

- **Research Background**
- **SEU-Hardening Design Techniques**
- **TID-Hardening Design Techniques**
- **Radiation Damage in DRAM**
- **Conclusion**

# Radiation in Space



## Summary of Space Radiation Environments and their Effects on CMOS Devices (from The NASA ASIC Guide)

Source	Particle Types	Primary Effects in Devices
Trapped radiation belts	Electrons	Total Ionizing Dose
	Protons	Total Ionizing Dose, SEE
Galactic cosmic rays	High-energy charged particles	Single-event effects
Solar flares	Electrons	Total Ionizing Dose
	Protons	Total Ionizing Dose, SEE
	Lower energy/heavy-charged particles	SEE

# Radiation in Atmosphere

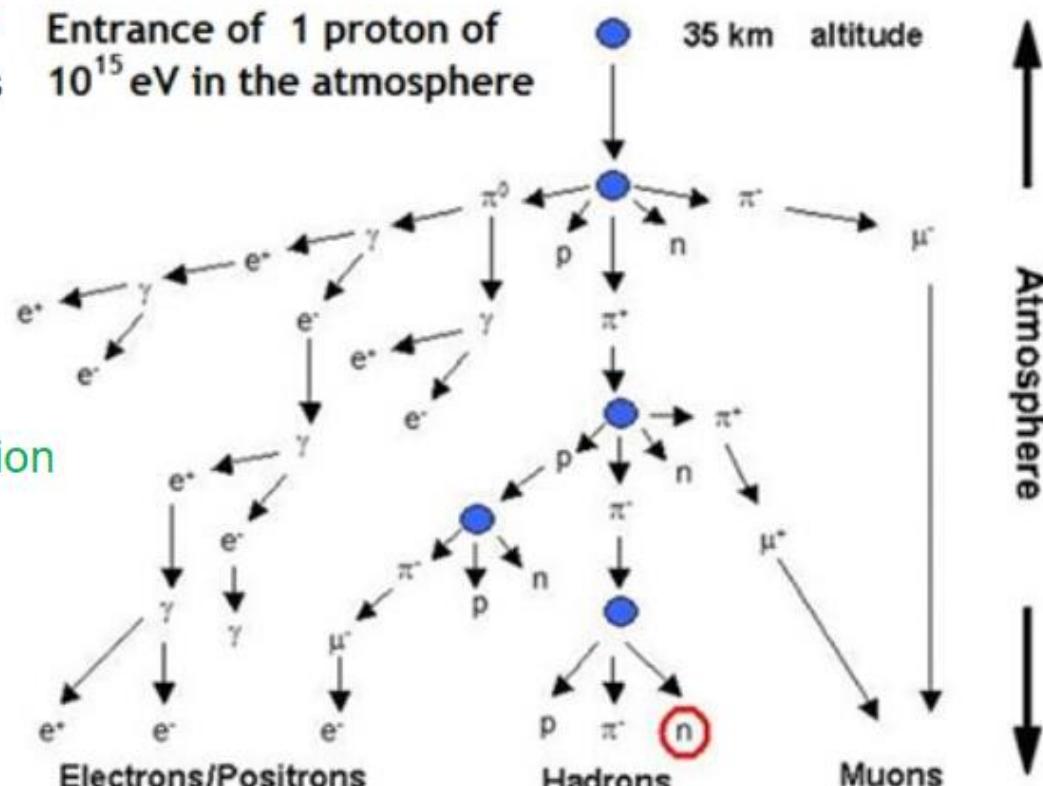
- Primary Cosmic Radiation

- Galactic Cosmic Rays
- Sun's particles
- Protons (85%)
- He nuclei (13%)

Entrance of 1 proton of  $10^{15}$  eV in the atmosphere

- Secondary Cosmic Radiation

- Neutrons
- Protons
- Muons
- Pions
- Photons
- Electrons/Positrons



$10^6$  particles to the ground:  
80%  $\gamma$ ; 18%  $e^-/e^+$ ; 1,7% muons; 0,3% hadrons

<Source: "Neutron production in atmosphere", Nuclear Physics in Galactic Cosmic Rays in the AMS-02 era, 2012>

# *Summary of Radiation Damages in Transistors*

## Cumulative Effect

Ionizing

Total-ionizing  
dose (TID)

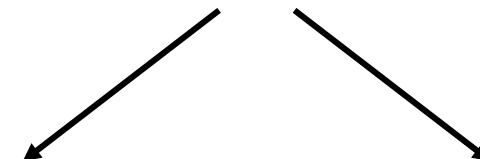
MOSFET,  
BJT

Non-Ionizing

Displacement  
Damage

BJT, CCD,  
Solar Cells

## Single-event Effect



Destructive  
(Hard-error)

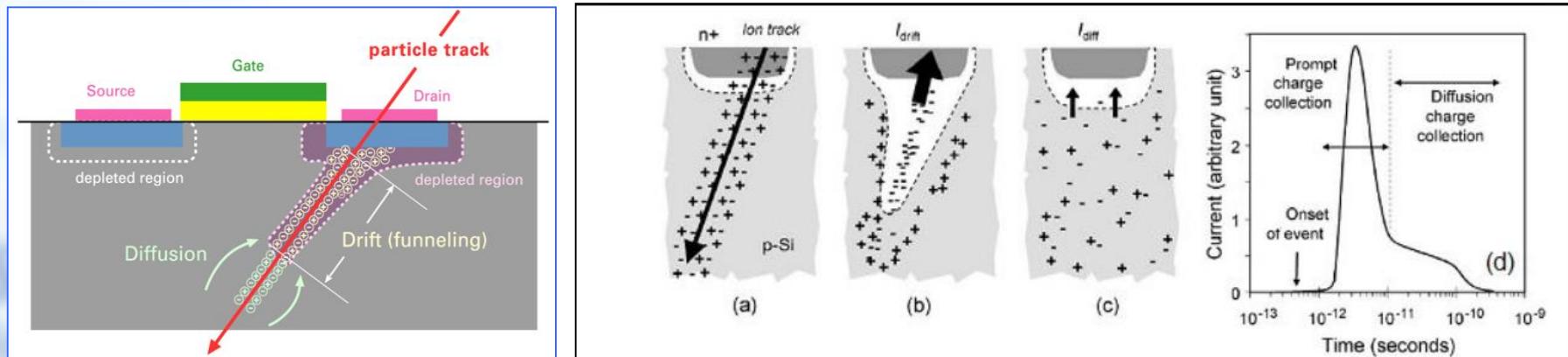
- Single-event Burn-out
- Single-event Dielectric Failure
- Single-event Gate Rupture
- Single-event Latch-up

Recoverable  
(Soft-error)

- Single-event Upset
- Single-event Transient

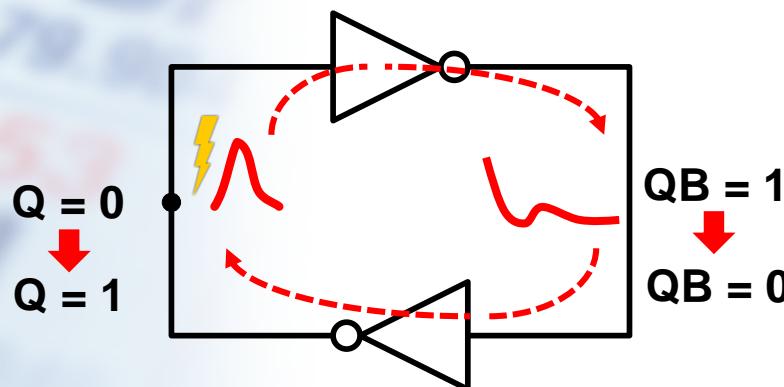
Memory

# Single-event Effects (SEE)



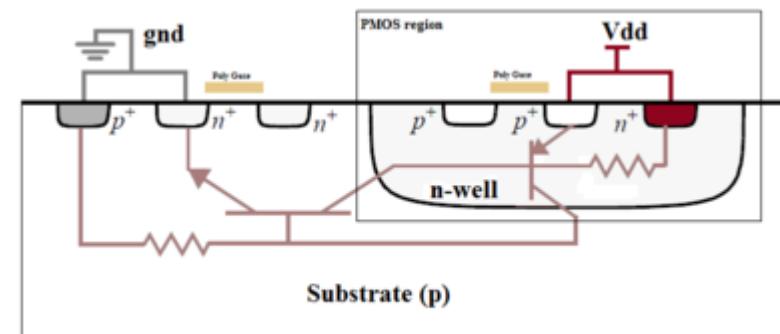
<Source:Jean-Luc Autran, Sergey Semikh, Daniela Munteanu, Sébastien Serre, Gilles Gasiot and Philippe Roche, "Soft-Error Rate of Advanced SRAM Memories: Modeling and Monte Carlo Simulation">

## Soft-error (Recoverable)



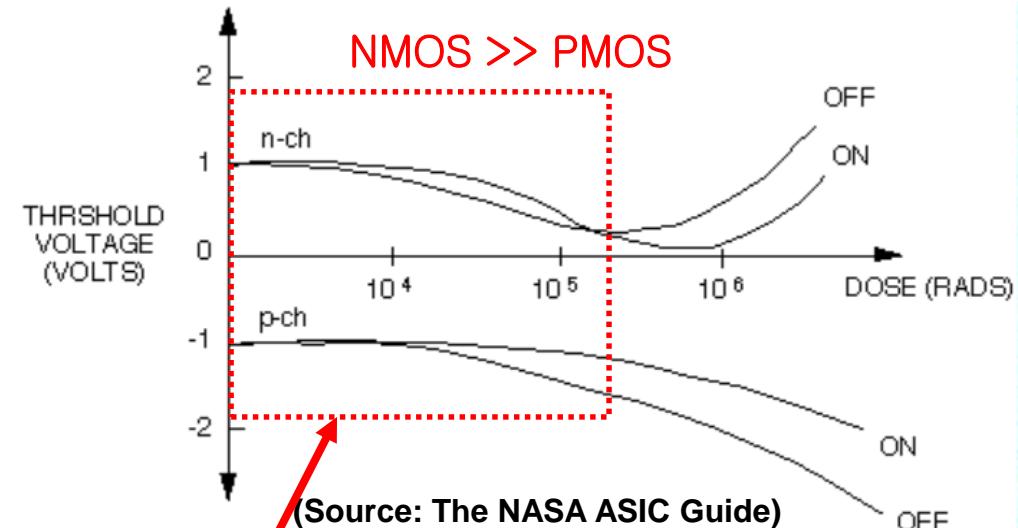
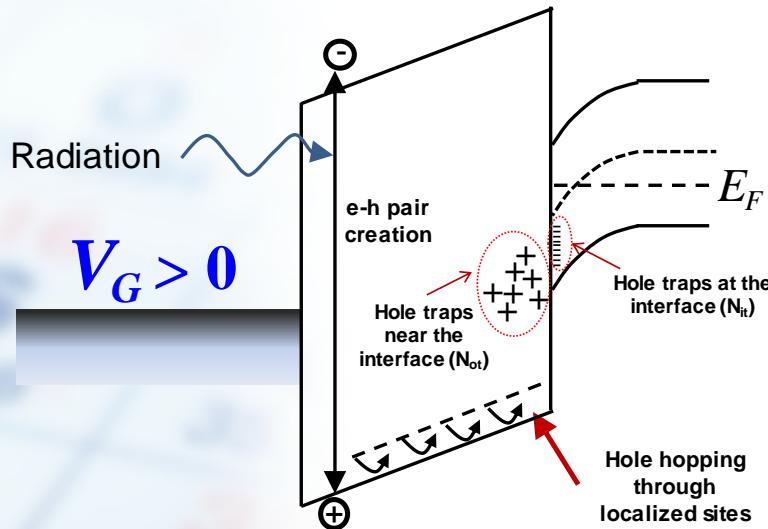
*Single-event transition → Single-event upset (single-bit or multiple-bit flipping)*

## Hard-error (Non-recoverable)



*Single-event latch-up (SEL)*

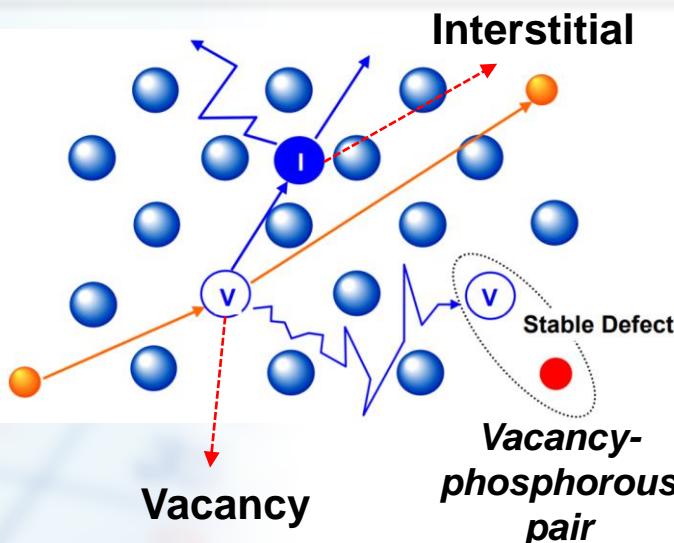
# Total Ionizing Dose (TID)



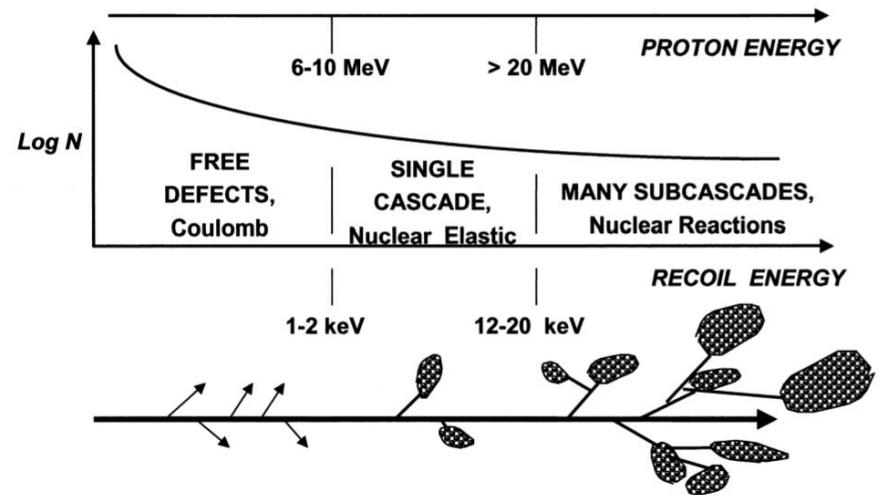
Radiation Condition	Specification	Unit of Measurement
TID Tolerance	300	Krad (Si)
Soft-error Rate without EDAC and scrubbing engine	1e-7	error/bit/day
Soft-error Rate with EDAC and scrubbing engine	1e-15	error/bit/day

<Source: Radiation testing of CMOS devices required for space use, Military Embedded System>

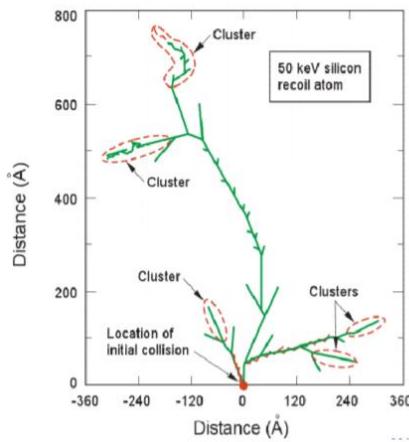
# Displacement Damage (DD)



## Displacement Damage Processes in Si

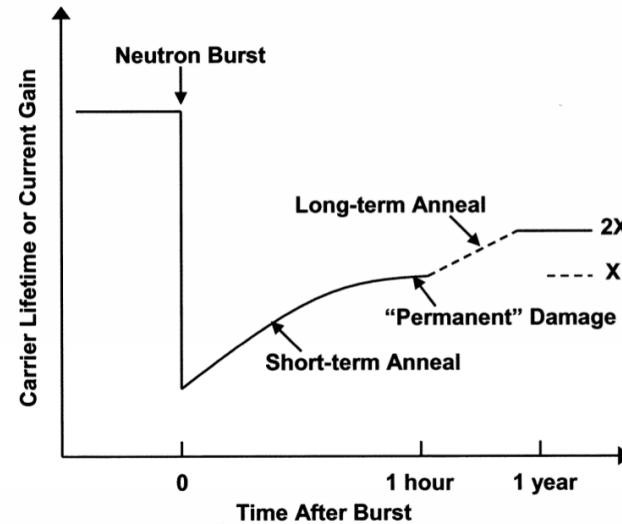


## Cascades - Examples



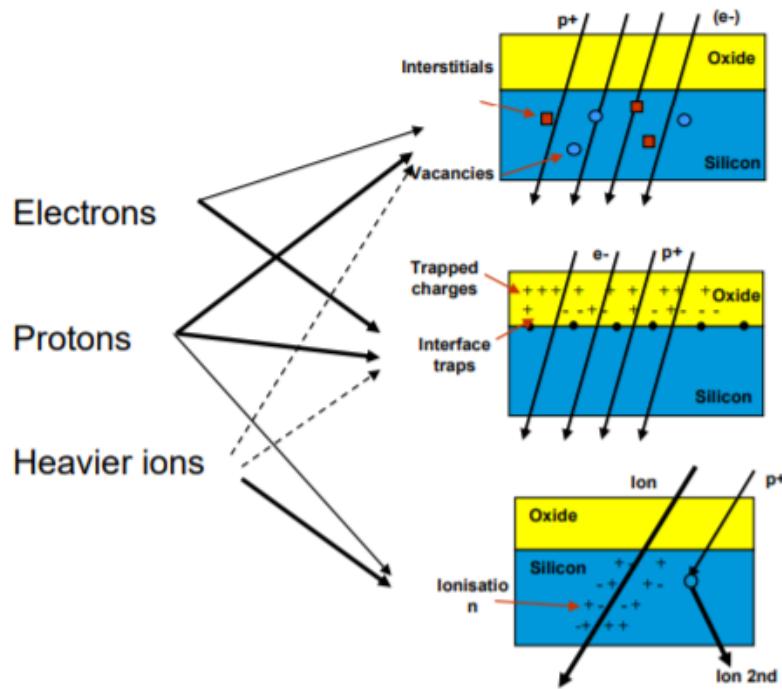
- 50 keV PKA is typical of what can be produced by a 1MeV neutron or high energy proton
- Threshold displacement energy in Si: 21 eV

(After Johnston,  
NSREC short course 2000)



<Source: "Review of Displacement Damage Effects in Silicon Devices", IEEE Transaction on Nuclear Science 2003>

# SEE vs. TID vs. DD



Displacement Damage

Total Ionising Dose

DD is a result of particle Energy deposition in the bulk of semiconductors (Si, GaAs,...)

Only a very small fraction of Energy deposition goes into Displacement Damage

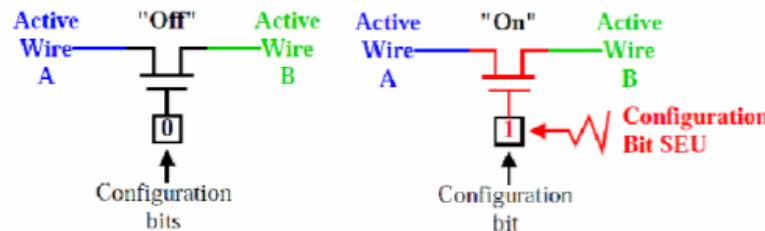
Single Event Effects

- **DD:** Silicon 내부의 일부 부분에 응집하여 보임
- **TID :** Insulator 전체에 걸쳐 유사하게 나타남, Insulator 전압에 영향을 받음
- **SEE:** Silicon에서 나타남

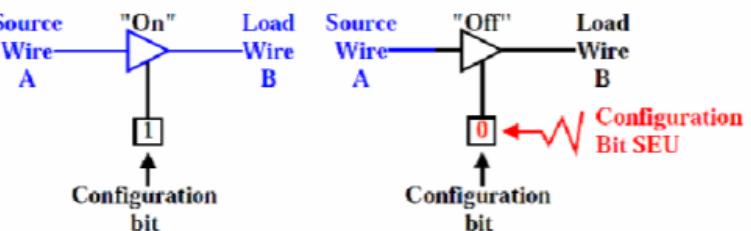
- Research Background
- **SEE-Hardening Design Techniques**
- TID-Hardening Design Techniques
- Radiation Damage in DRAM
- Conclusion

# Why SEE is Critical? (FPGA)

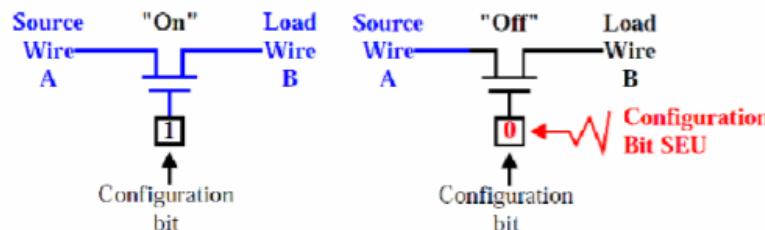
PIP short



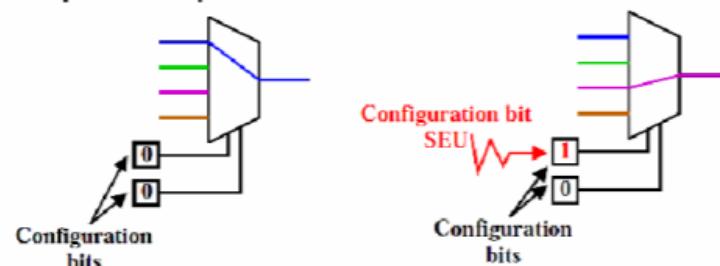
buffer open



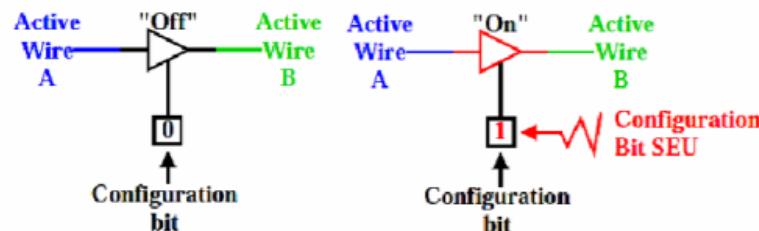
PIP open



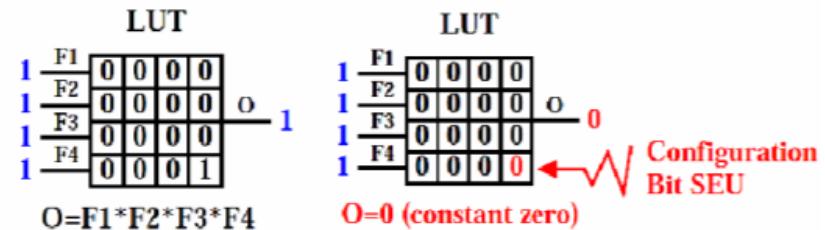
Multiplexer upset



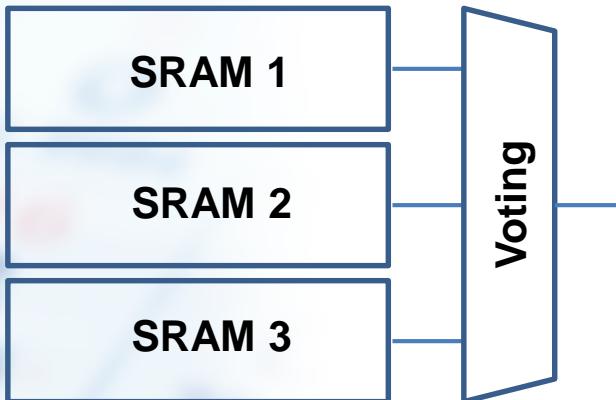
buffer short



LUT upset

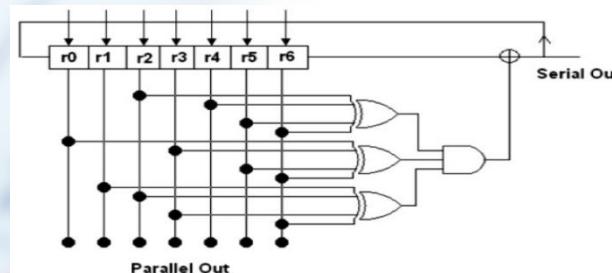


# System-level Technique



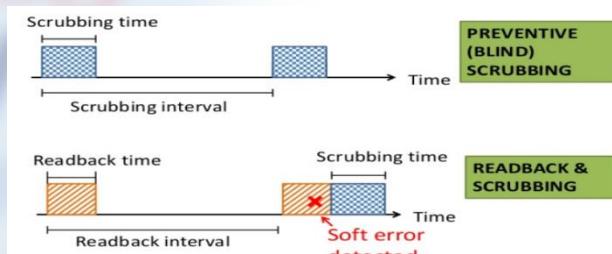
## Triple-Modular Redundancy

- Single-error Correction, Double-error Detection
- $3x + \alpha$  (for voting) Energy , 3x Area, More latency
- Finer granularity (from chip-level to cell-level)  
→ More Powerful, but more overhead
- Dual Redundancy (Lock-step) → Only detection



## Error-Correction Code

- Hamming or SECDED due to latency constraint
- Bit-interleaving to address MBU
- How to handle accumulation problems ?

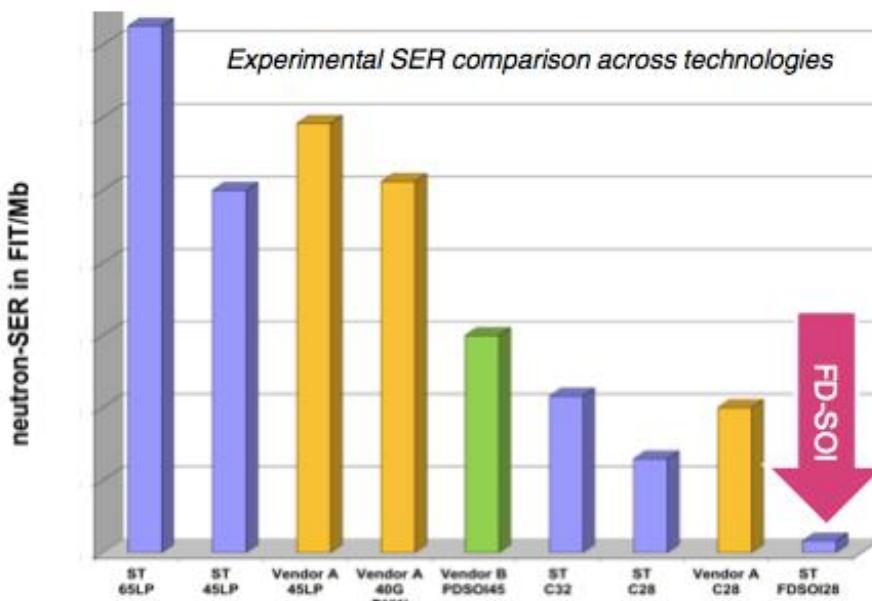
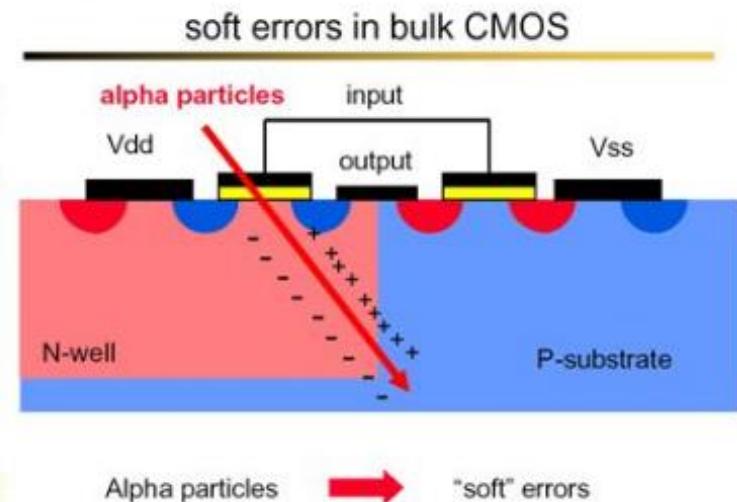
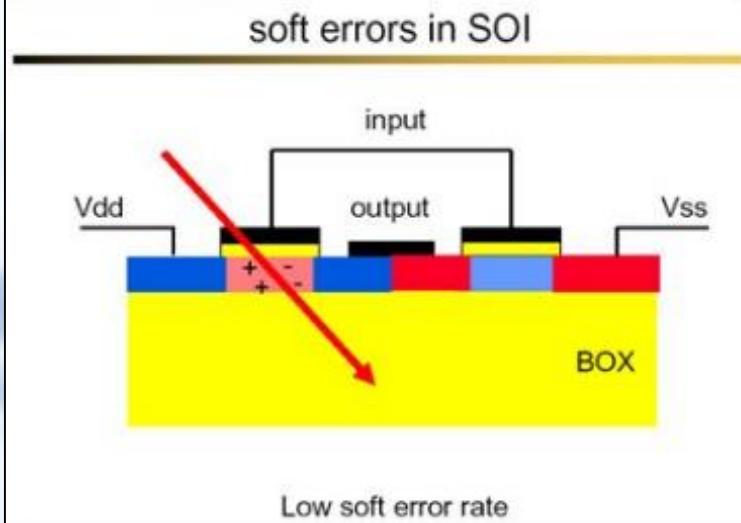


<Frame-level redundancy SRAM-based FPGA  
by Jorge Tonfat>

## Scrubbing

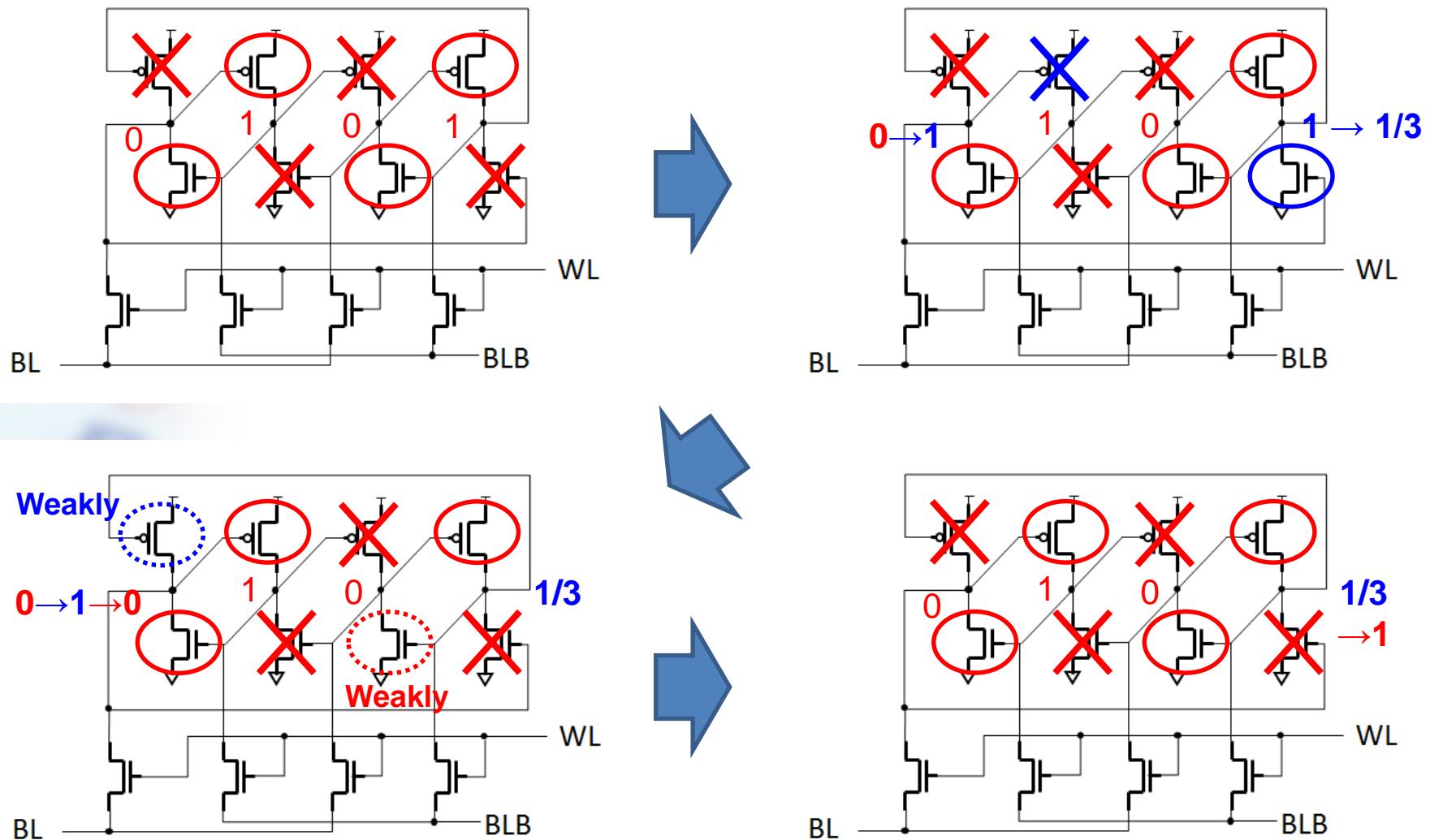
- Accumulation of soft-errors are addressed
- Software or Hardware Approaches (Should be combined with TMR or ECC)
- Energy / Performance Penalty

# Device-level Techniques: SOI

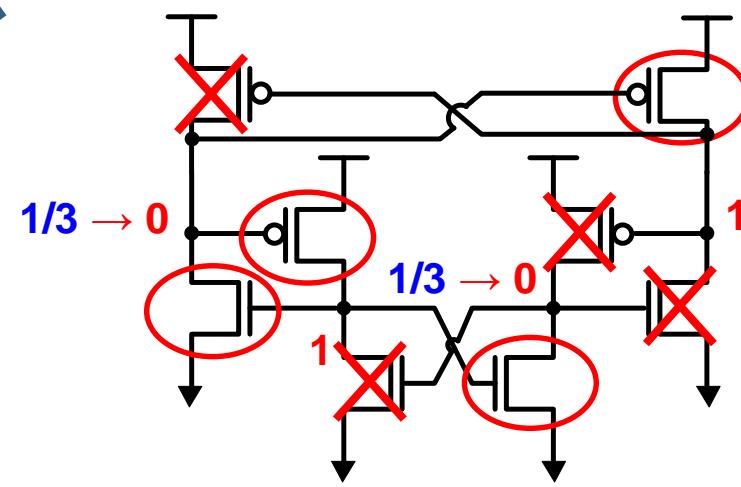
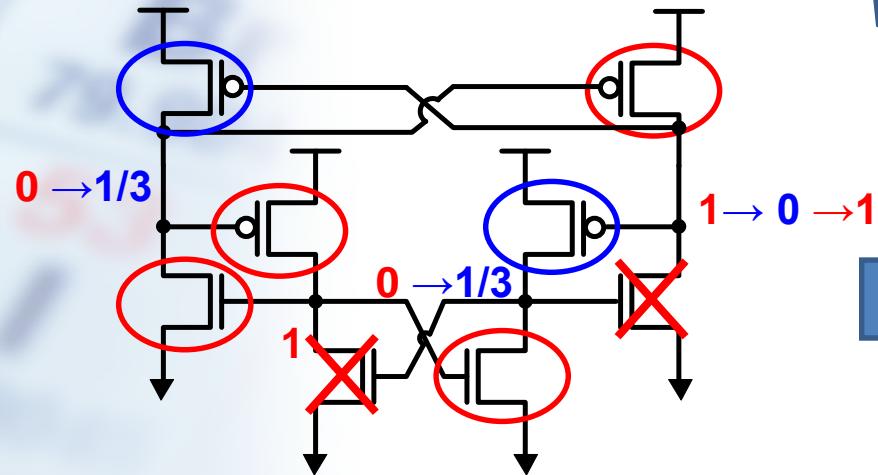
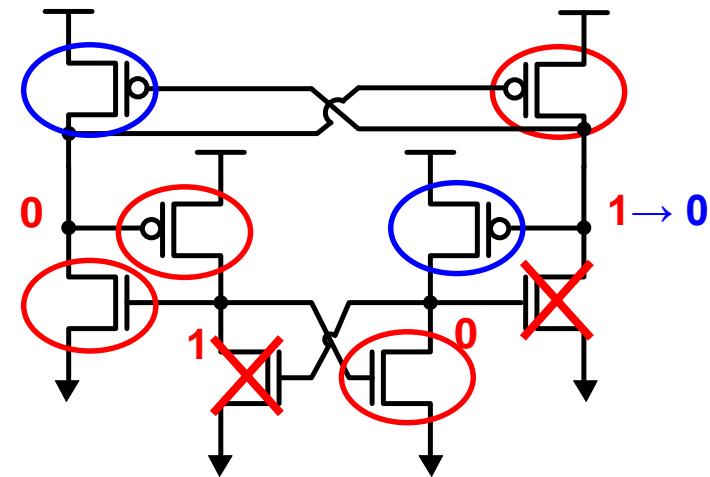
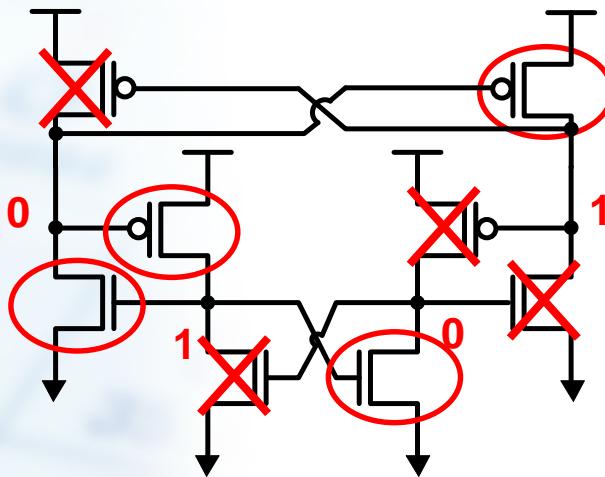


- SOI is more robust to SEU than Bulk-CMOS (due to insulated body)
- SOI is more robust to SEL than Bulk-CMOS (no parasitic BJT)
- PMOS, NMOS in triple-well is better than NMOS

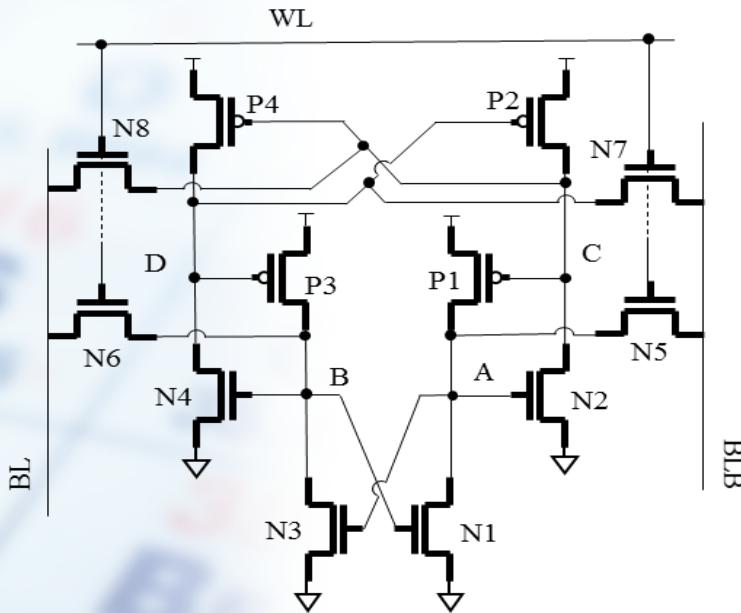
# *Circuit-level Techniques: DICE SRAM CELL*



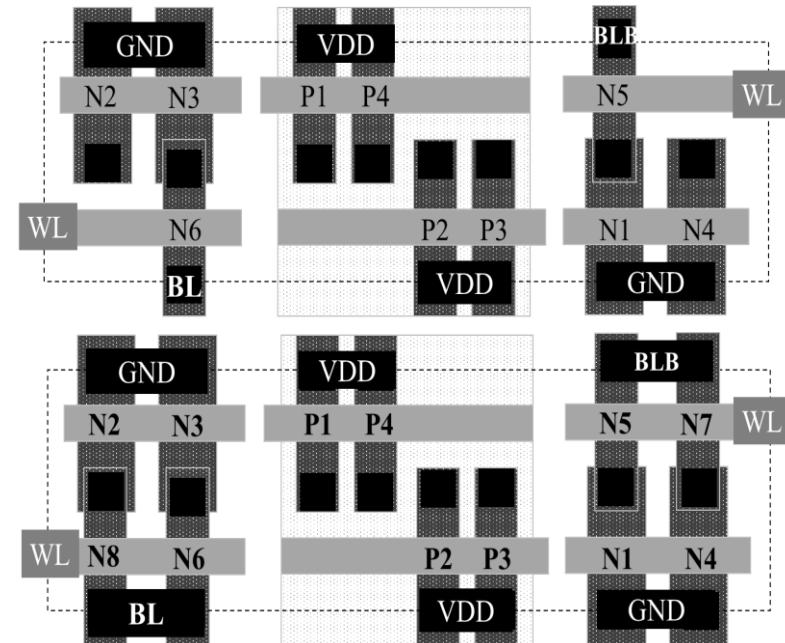
# Circuit-level Techniques: Quatro SRAM CELL



# Our Approach: New SRAM Cell named as 'We-Quatro'

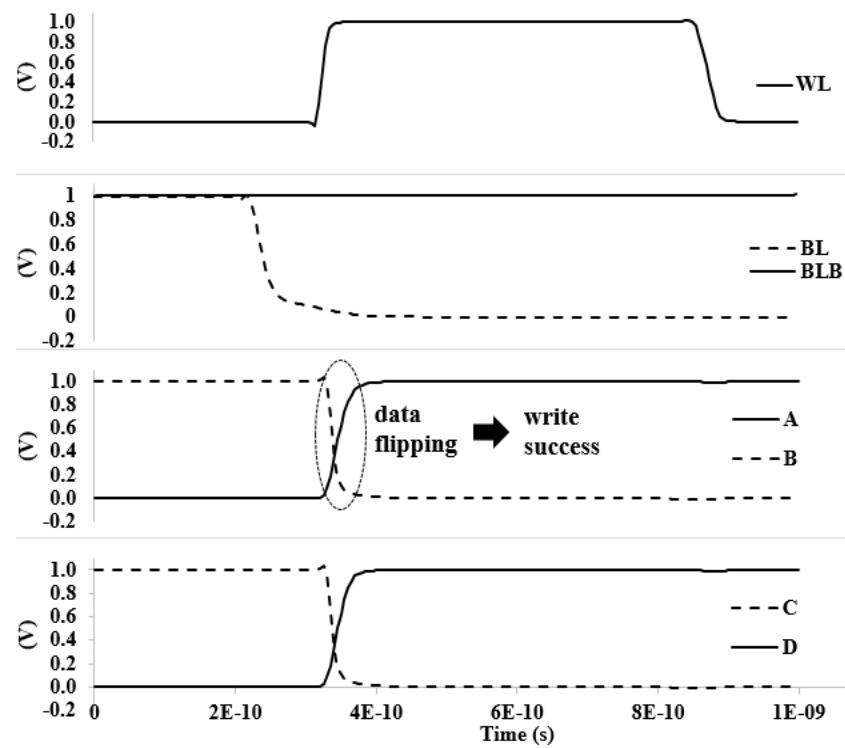
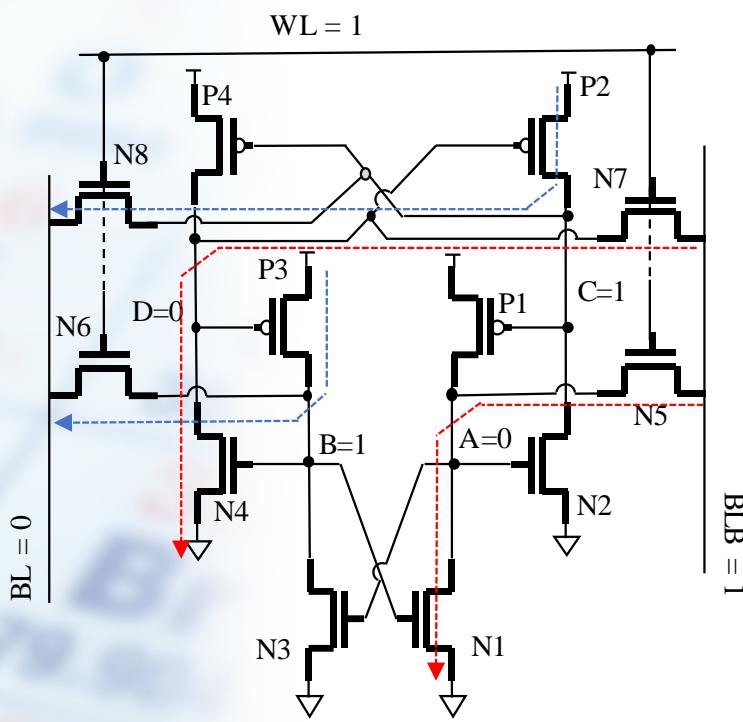


We-Quatro



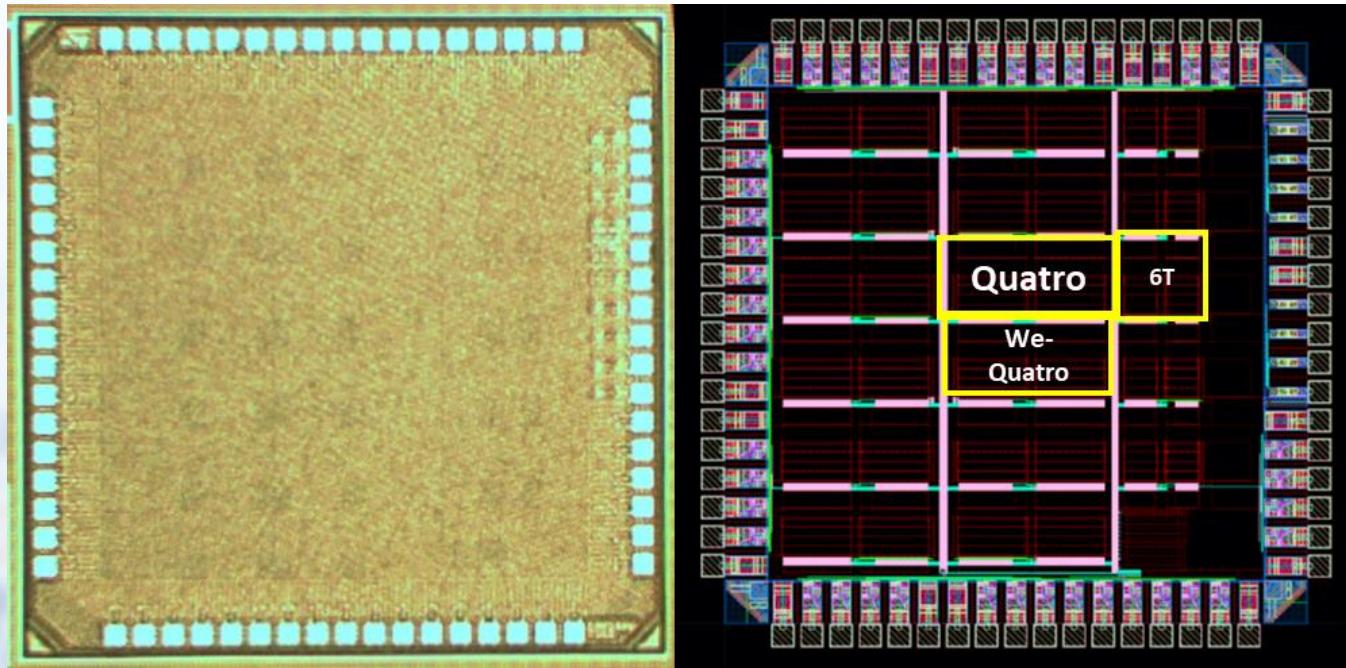
- Published at IEEE Transaction on Nuclear Science, Sep./2017
- We-Quatro : Writability-enhanced Quatro
- In Thin-cell type layout, Area(Quatro) = Area(We-Quatro)
- BL = metal-3 layer unlike 6T SRAM (metal-2 layer)
- Under logic rules of 28nm FD-SOI, Area(We-Quatro) =  $2.1 \times$ Area(6T SRAM)  
**(But we cannot compare under SRAM rules)**

# *Write Operation of 'We-Quatro'*

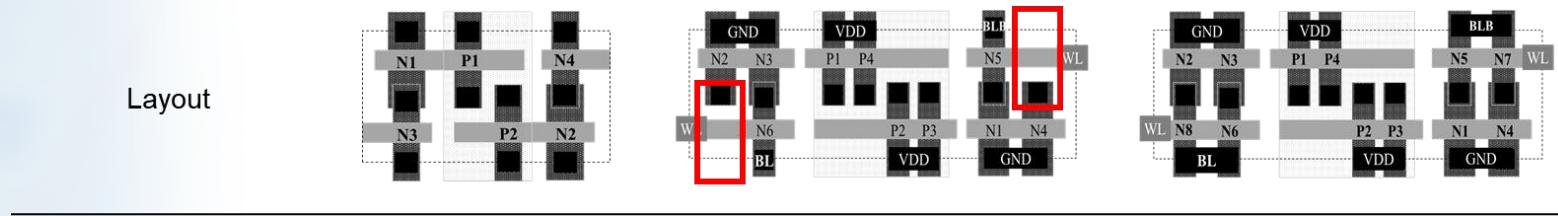


- Pull-down of N6 and N8 triggers writing (similar to 6T)
- Parallel accessing of all memory nodes : write performance will be enhanced

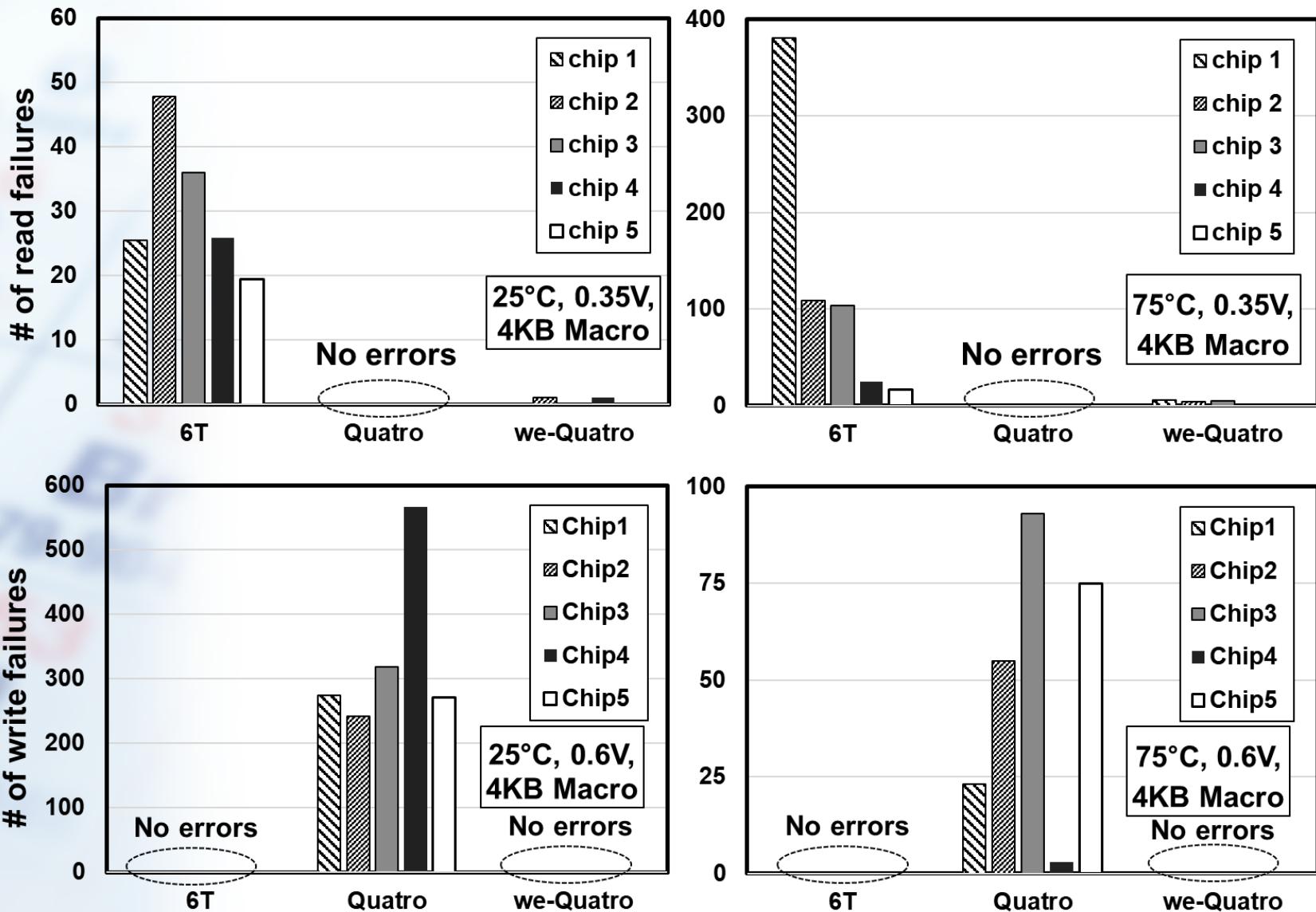
# *Test-chip Fabrication (6T, Quatro, we-Quatro)*



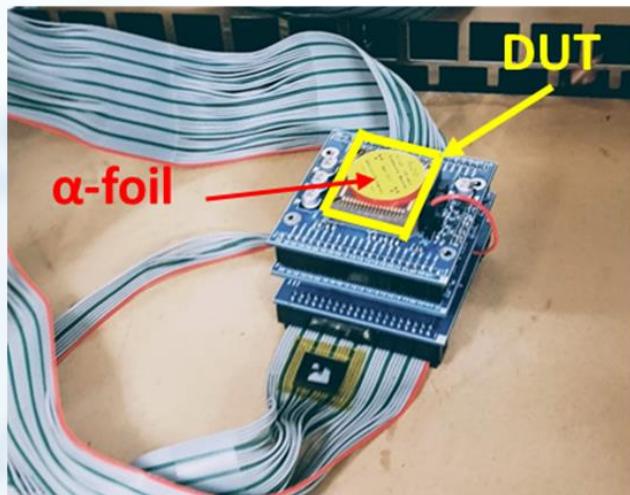
Technology: 28nm FD-SOI	6T	Quatro	we-Quatro
Cell Size under Logic Design Rule	$0.30\mu\text{m}^2$ (1x)	$0.63\mu\text{m}^2$ (2.1x)	$0.63\mu\text{m}^2$ (2.1x)



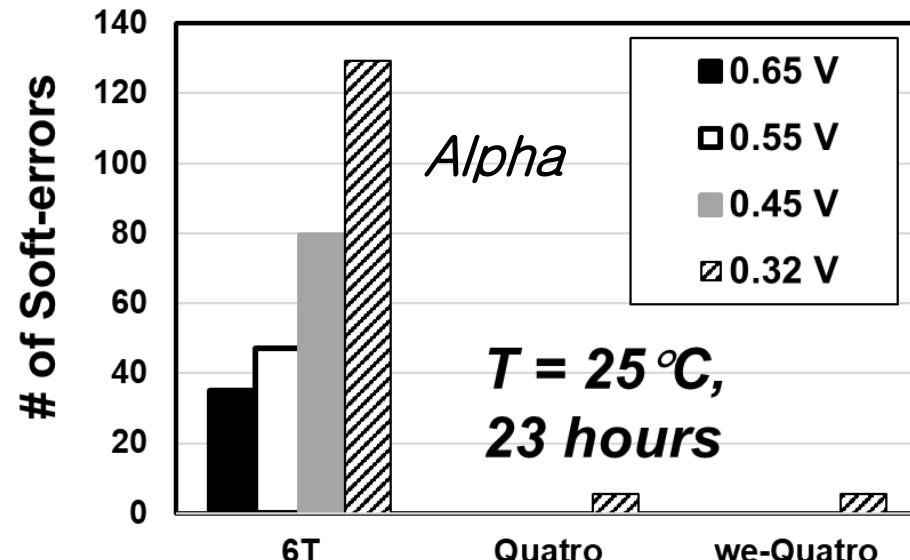
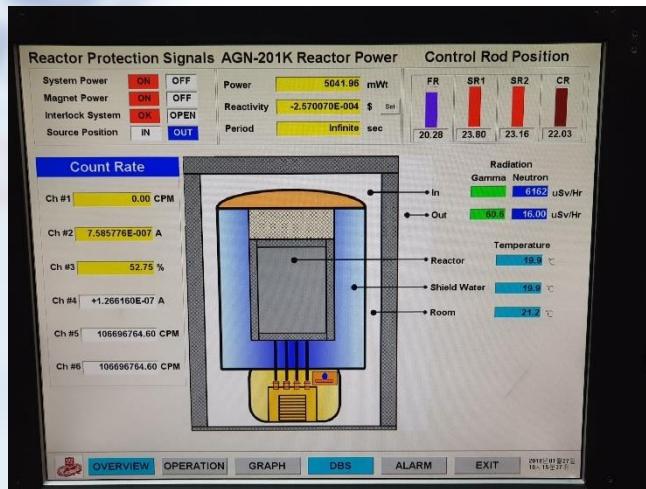
# Read and Write Stability Measurement Results



# SEU Tests under Radiation (Alpha, Neutron)

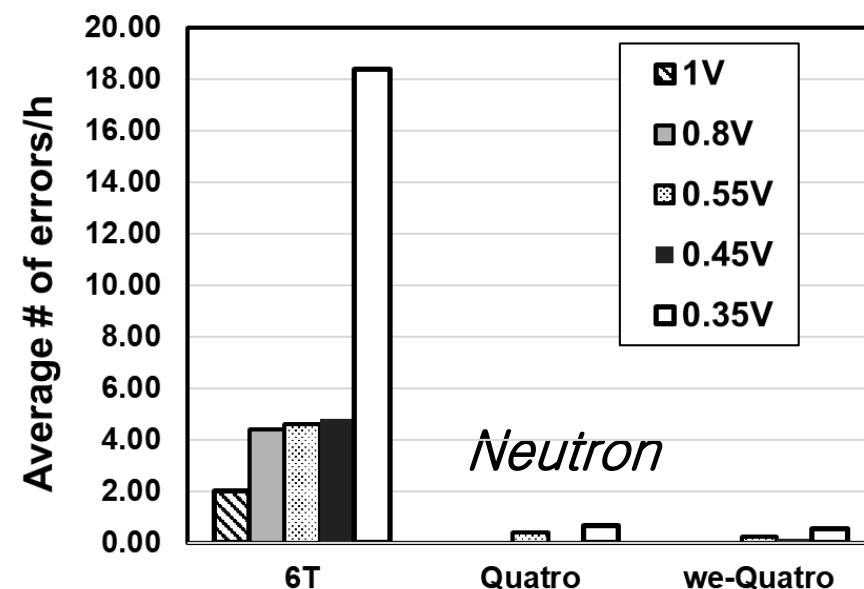


DUT under Alpha source  
(Polonium-210, 0.1uCi, 5407.5 keV)



Alpha

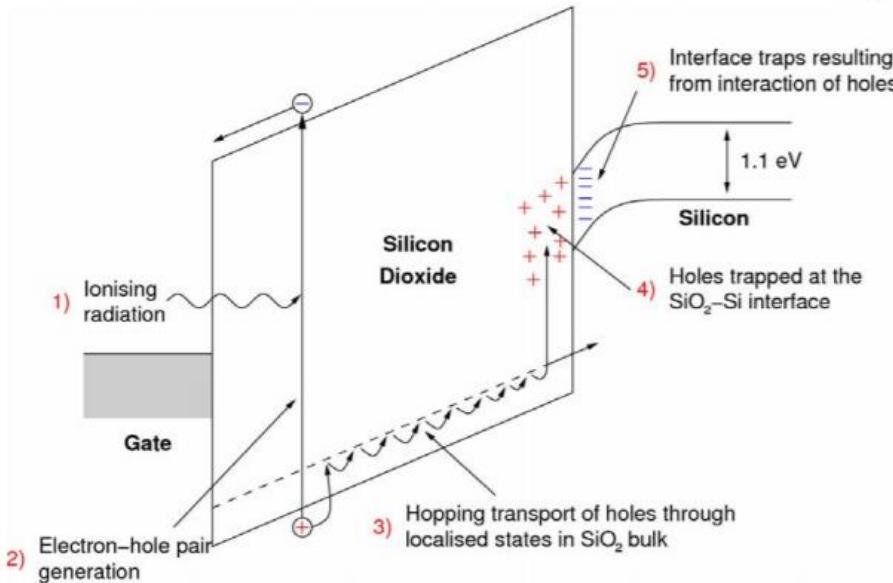
$T = 25^{\circ}\text{C}$ ,  
23 hours



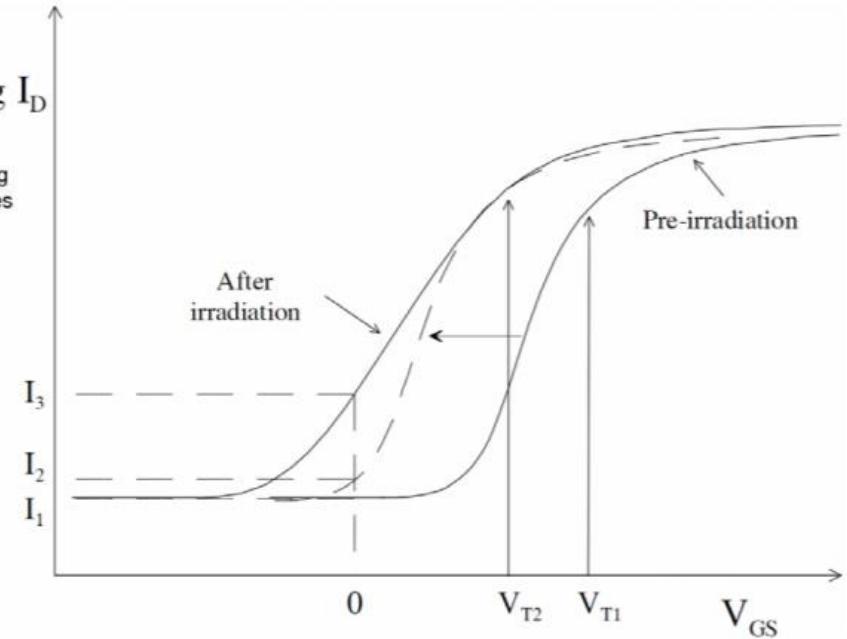
Neutron

- Research Background
- SEE-Hardening Design Techniques
- **TID-Hardening Design Techniques**
- Radiation Damage in DRAM
- Conclusion

## Threshold voltage shift



Energy band diagram of a Metal-Oxide-Semiconductor structure with a positive gate voltage applied



Increase of the sub-threshold current in a NMOS transistor given by a decrease in the threshold voltage and change of the sub-threshold slope

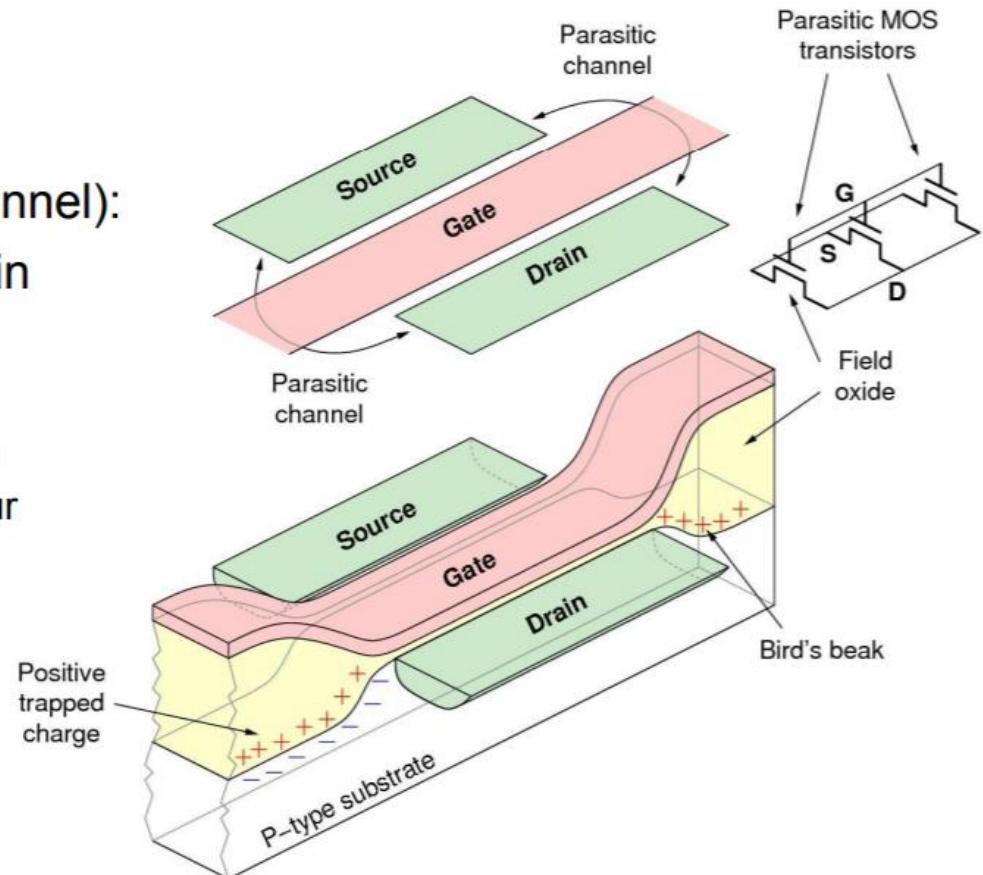
<Source: “Radiation Damages to Electronic Components”, GSI Experiment Electronics

# TID Damage – Parasitic MOS Transistors

Leakage current (parasitic channel):  
path between Source and Drain

→ prevent e.g.

- switch-off of the transistor
- change of circuit behaviour  
(operation point, ...)

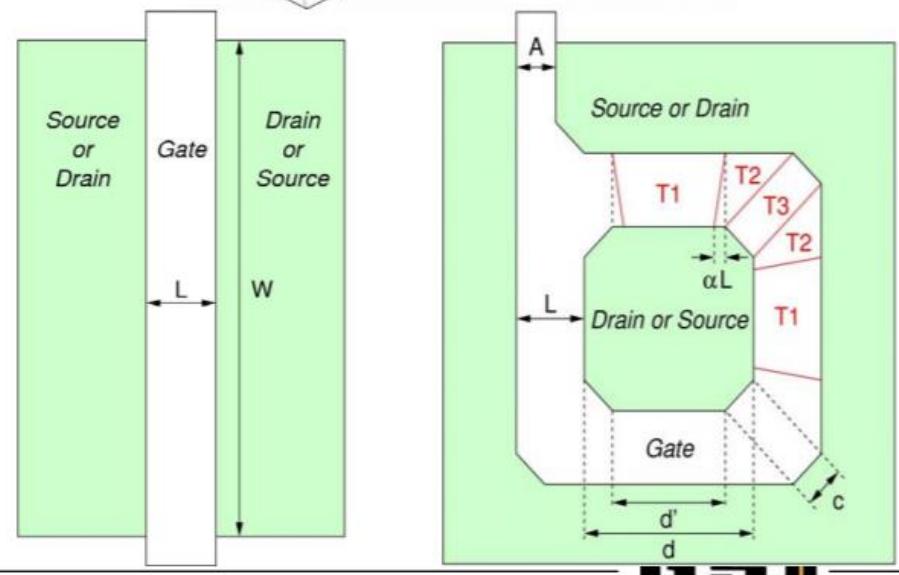
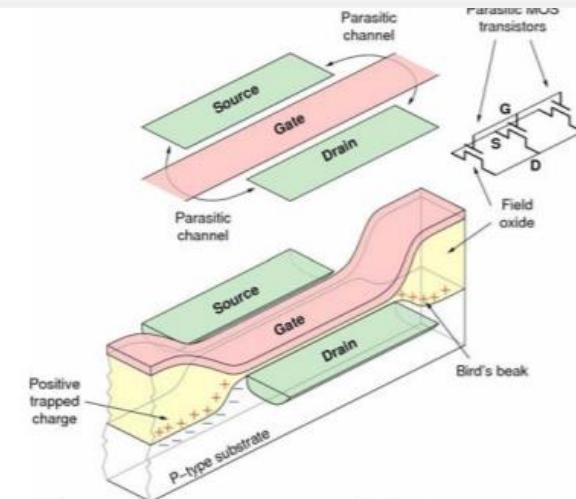


<Source: “Radiation Damages to Electronic Components”, GSI Experiment Electronics

# TID Hardening By Layout

Steps towards a radiation hard layout in CMOS:

- Prevent of nMOS leakage currents due to chip irradiation:
  - Using enclosed transistors (right) instead of linear transistors (left)
- Disadvantage:
  - Complex model of transistor behavior
  - Larger area consumption
  - Bigger parasitic capacitances
  - Small W/L ratios not possible



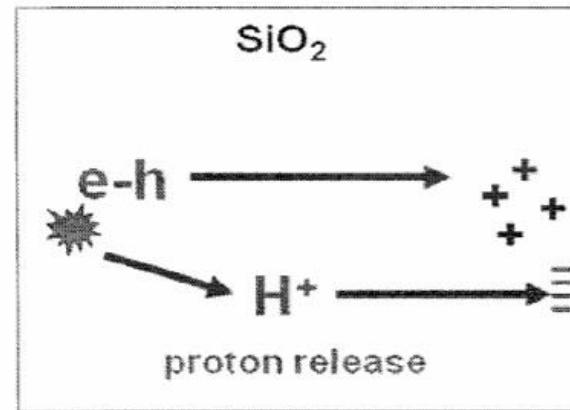
<Source: “Radiation Damages to Electronic Components”, GSI Experiment Electronics

# Enhanced Low Dose Rate Sensitivity (ELDRS)

Explanation of ELDRS via space charge models:

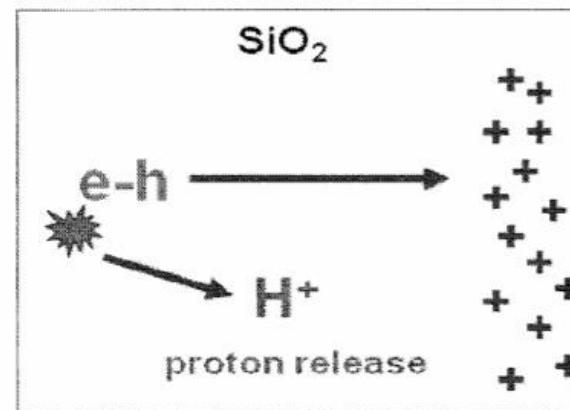
At high dose rate

- large amount of positive charge generated
- acts as barrier for holes and hydrogen transport to the interface
- reducing the degradation rate



Low dose rate

hole trapping ( $E'$ )  
interface defect formation ( $P_b$ )



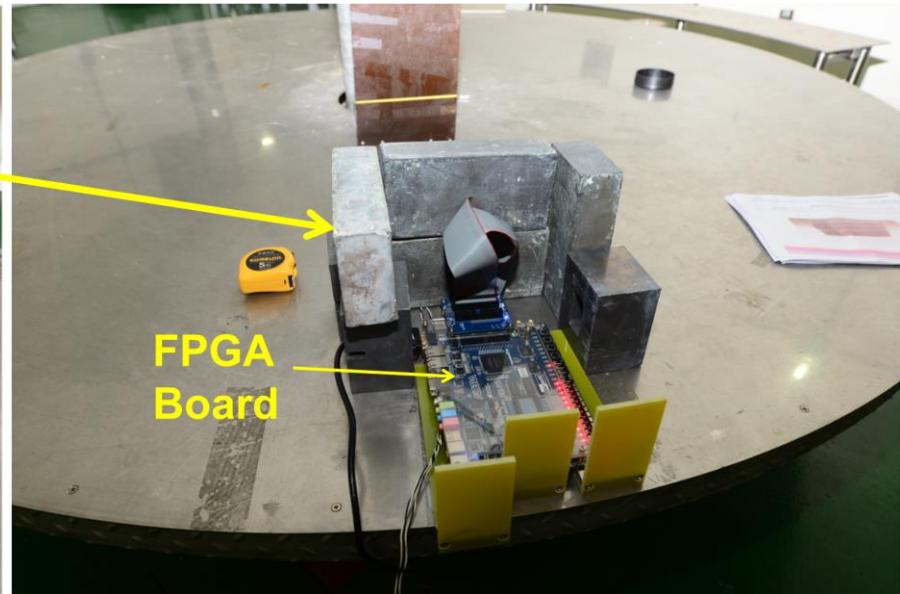
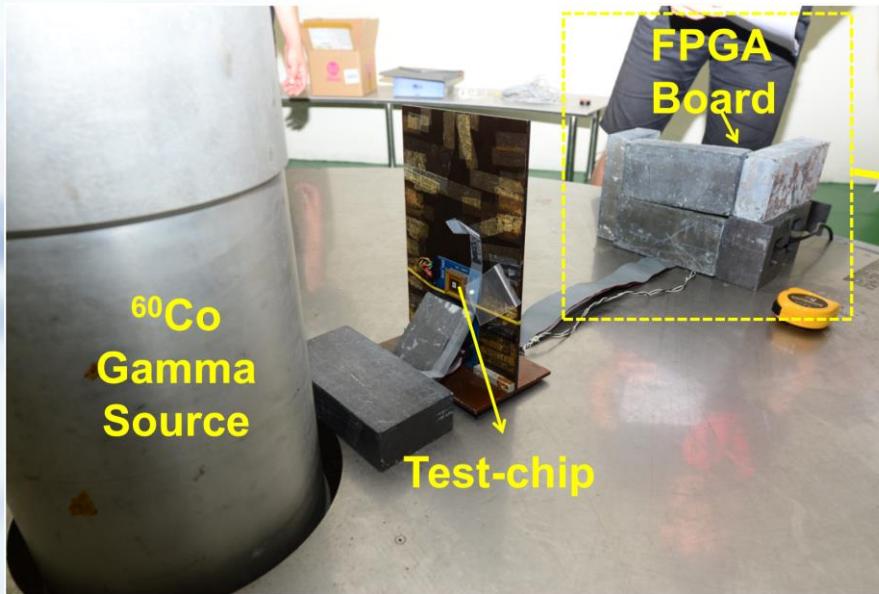
High dose rate

hole trapping ( $E'$ )  
+ electrostatic barrier

**Dose Rate is very critical in TID Measurement!**

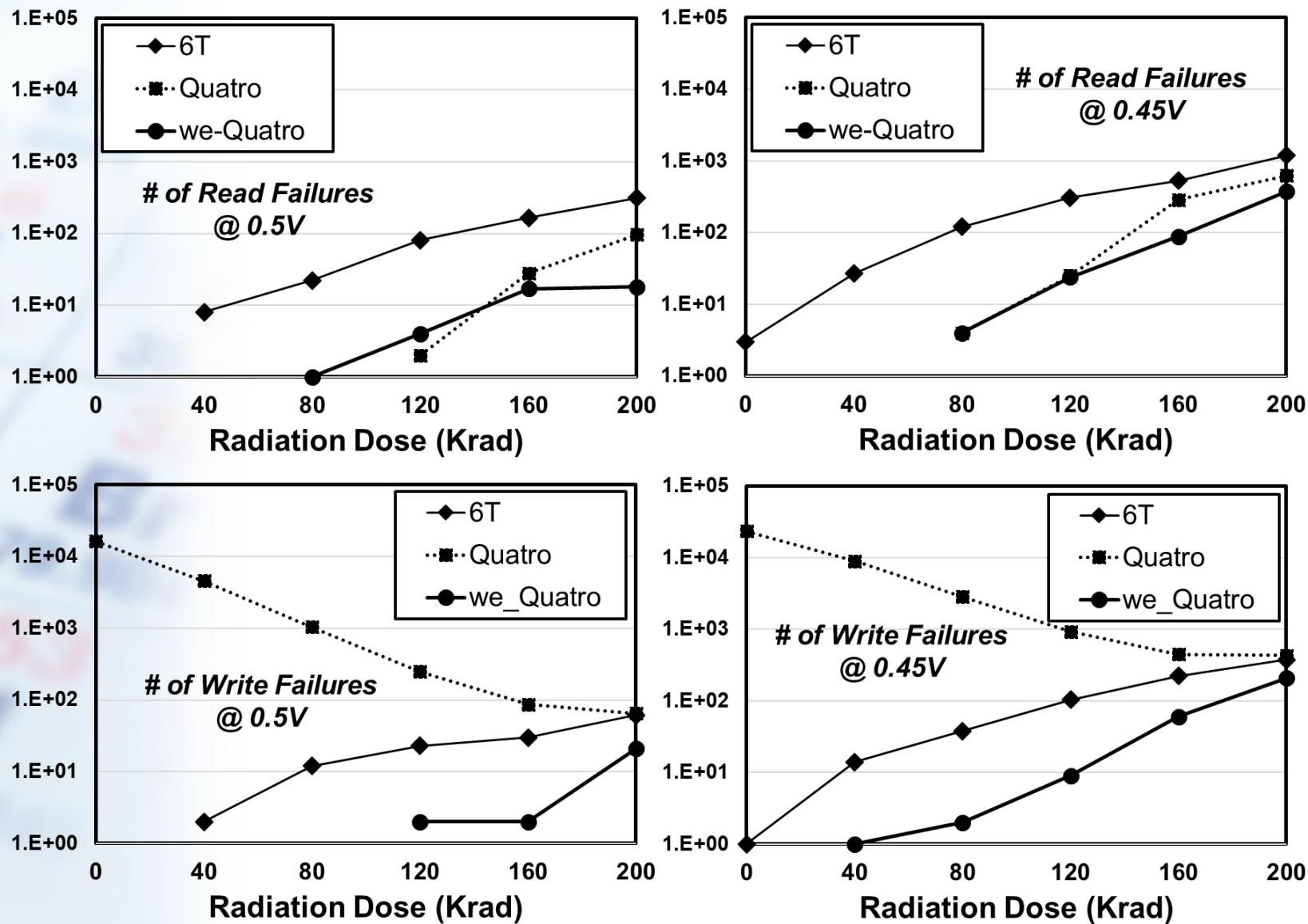
<Source: "Radiation Damages to Electronic Components", GSI Experiment Electronics

# Our TID Measurements

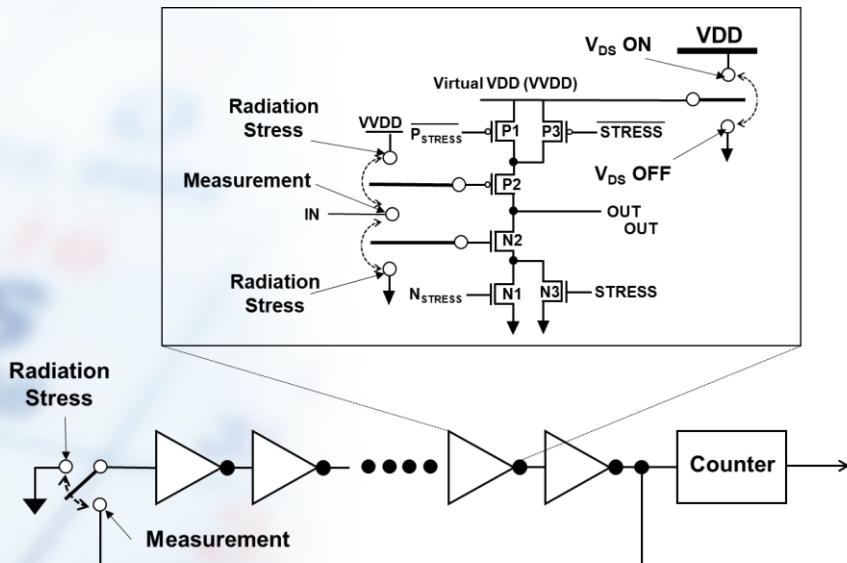


- **Source:** $^{60}\text{Co}$  Gamma Ray
- **Dose Rate :** 10Krad/hour ( $\text{SiO}_2$ )
- **Radiation Stress:** 20hours

# SRAM Measurement Results

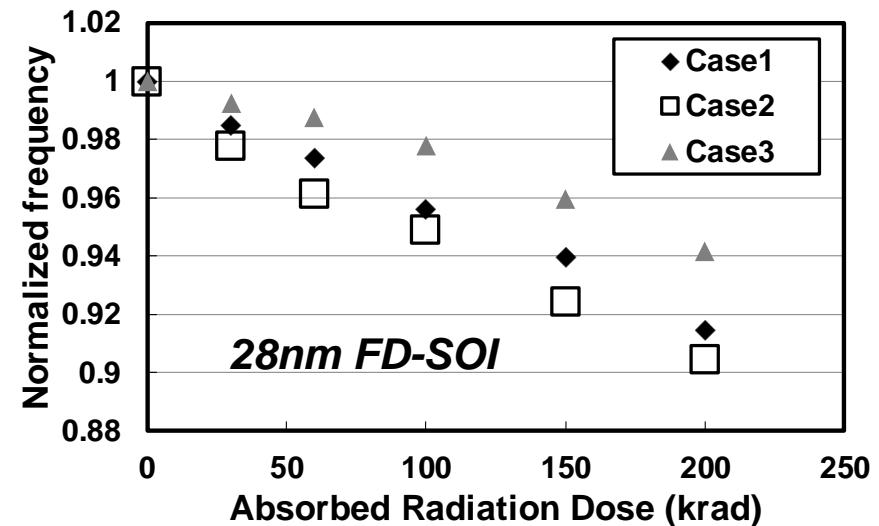
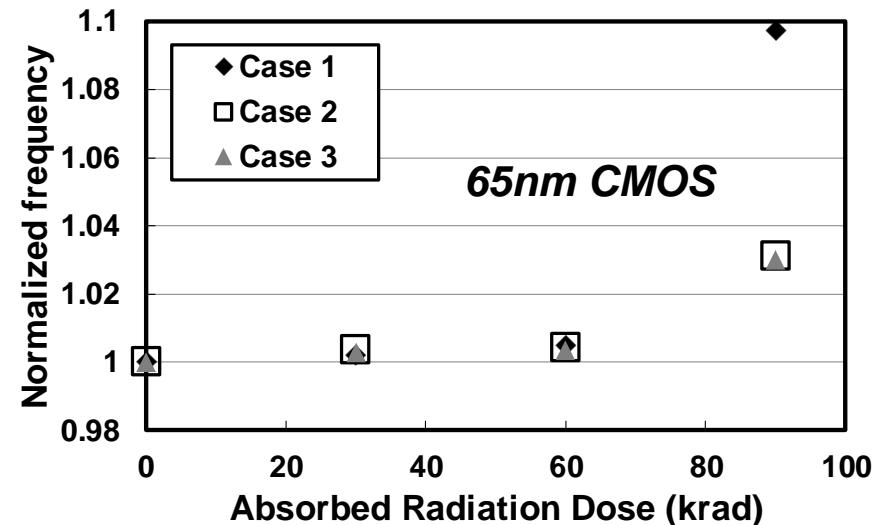


# TID Characterization in Ring Oscillator



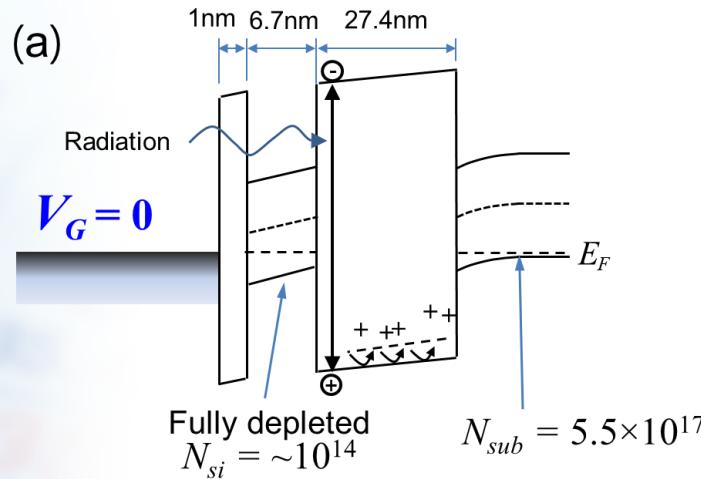
Mode	Signal	Case 1: N1 Stress	Case 2: P1 Stress	Case 3: No Biasing
Radiation Stress	P <sub>STRESS</sub>	Low	High	Low
	N <sub>STRESS</sub>	High	Low	Low
	STRESS	High	High	High
Measurement (V <sub>DS</sub> ON)	P <sub>STRESS</sub>	High (P1 ON)		
	N <sub>STRESS</sub>	High (N1 ON)		
	STRESS	Low (P3, N3 OFF)		

**CMOS : Intuitive**  
**FD-SOI: Not intuitive**

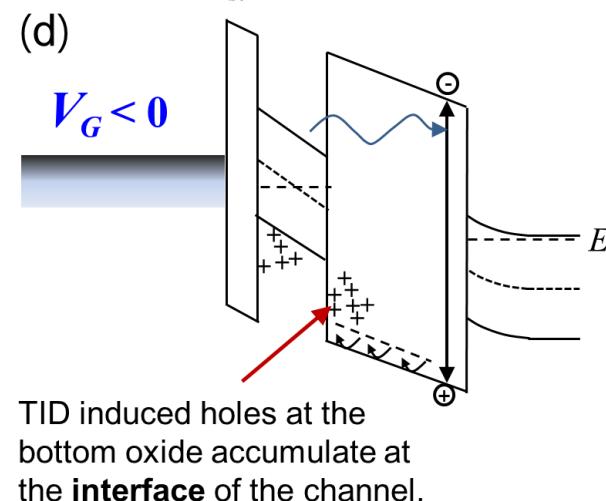
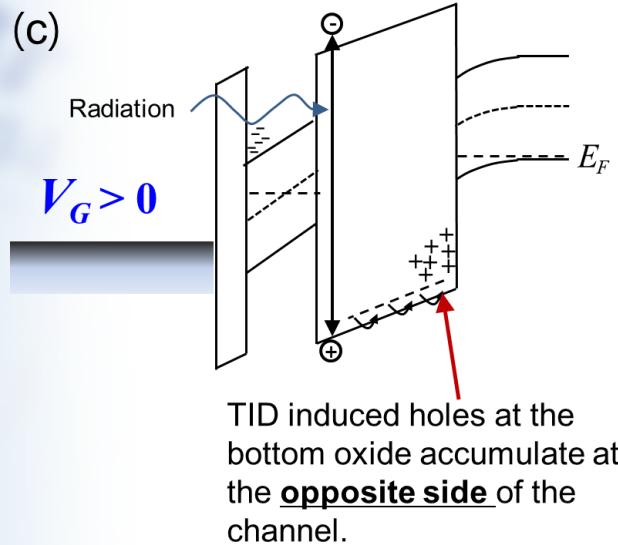
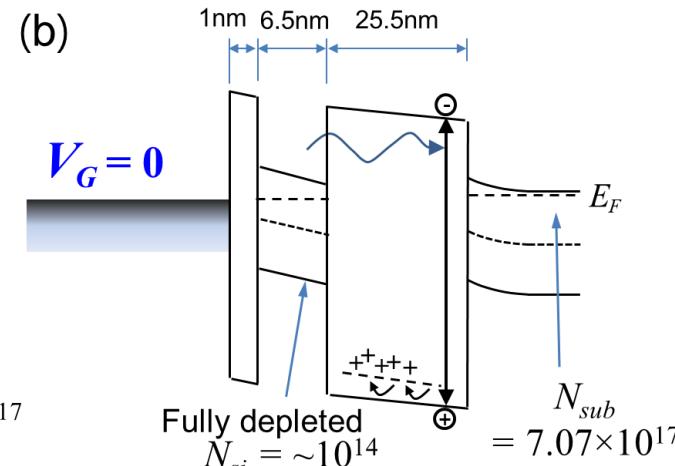


# TID Model in 28nm FD-SOI

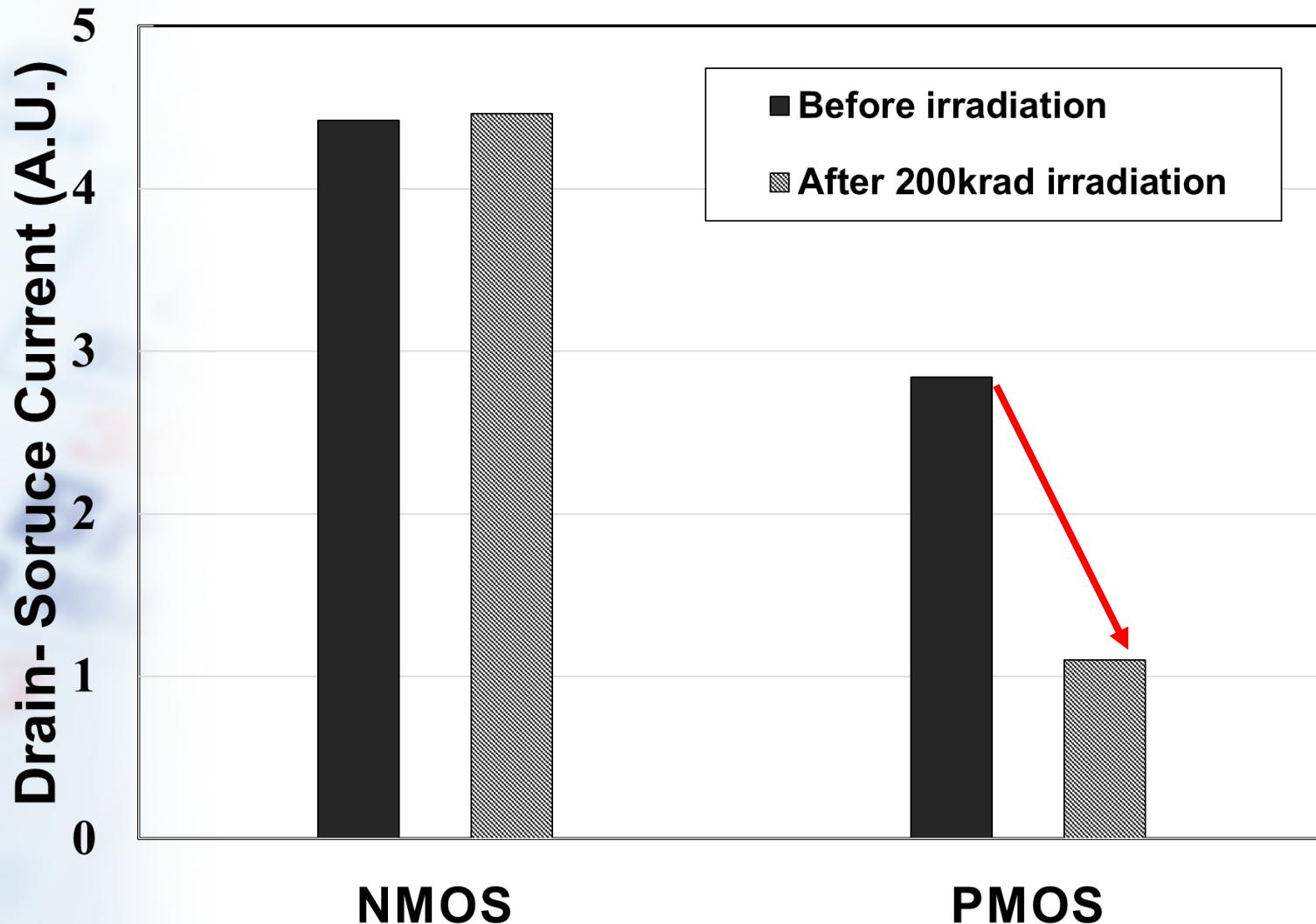
## FDSOI NMOS



## FDSOI PMOS



# *On Current Measurement under TID*



- Research Background
- SEE-Hardening Design Techniques
- TID-Hardening Design Techniques
- **Radiation Damage in DRAM**
- Conclusion

# *Conclusion*

- TID, DD, SEE are studied
- Some radiation-hardening techniques are introduced.
- Our propose SRAM, namely we-Quatro, provides good resilience to SEE and TID.

**Acknowledgement:** Dr. Han, Jin-woo in NASA

|

Thank you!