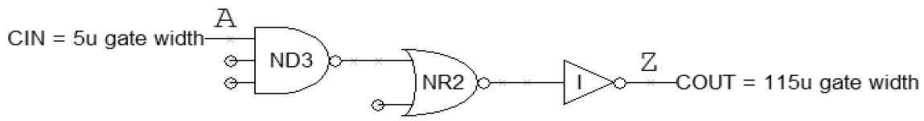
VLSI Systems Designs(SoC DM): Final Exam (2016 Fall)

10:30 ~ 11:50, 12/14/2014, Prof. Jinsang Kim

Assume that a matched unit inverter has widths of 45nm for nMOS and 90nm for pMOS, respectively. The 45nm process technology uses the following parameters unless stated otherwise: $V_{DD} = 1\,V,\ Vto = 0.3\,V, \beta_n = 1mA/V^2, \Phi_s = 0.6\,V, \gamma = 0.3\,V^{0.5}, \lambda = 0.02, \tau = 3RC = 3ps$

1. (35pts) You need to decide the minimum delay and widths of logic gates in the following circuit. Input and output capacitances are denoted based on a unit matched inverter (5u gate width means width is 5 times larger than that of the unit matched inverter). ND3 = 3 input NAND, NR2 = 2 input NOR, I = Inverter, respectively.



   a) calculate the logical efforts of all logic gates (ND3, NR2, and I) on the path "A" ~ "Z". (6pts)
   b) calculate path logical effort, path electrical effort and total path effort of the path "A" ~ "Z"(6pts)
   c) what are the stage efforts of ND3, NR2 and I for the minimum delay of the path "A" ~ "Z" (3pts)
   d) determine the widths of ND3, NR2 and I (6pts)
   e) assume that you need to change the above 3-stage logic into one-stage compound logic. Design the compound logic and compare the delay of the compound logic with the above 3-stage logic (14pts)

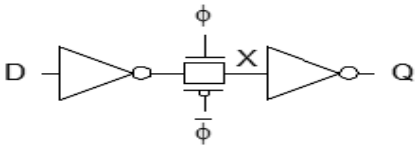
Use the following parameters for the following questions.

	setup time	clk-to-Q delay	D-to-Q delay	contamination delay	hold time	clock skew
FF	65 ps	50 ps	n/a	35 ps	30 ps	50 ps
latches	25 ps	50 ps	40 ps	35 ps	30 ps	50 ps

2. (15pts) For each of the following sequencing styles, determine the maximum logic propagation delay in each cycle (or half-cycle, for two-phase latches).
   a) FFs
   b) two-phase transparent latches with 60ps of nonoverlap between phases

3. (17 pts) You need to add testability for a two-bit adder sequencing block using FFs. Draw the RTL level architecture including testability of all the sequential and combinational blocks.

4. (5pts) Try to generate a test vector based on the SA1 fault model at ϕ.



5. (28pts) Draw the architecture of a PLL which multiplies frequency by N times at S domain. Also, derive the transfer equations of each sub-block and the corresponding circuit.

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