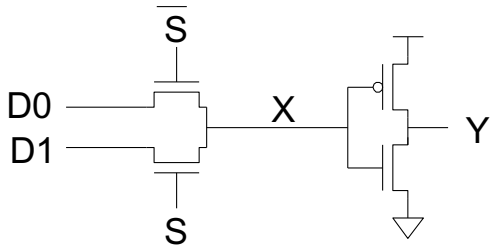
Circuit Pitfalls

Circuit Pitfalls

- Detective puzzle
  - Given circuit and symptom, diagnose cause and recommend solution
  - All these pitfalls have caused failures in real chips

Bad Circuit 1

- Circuit
  - 2:1 multiplexer



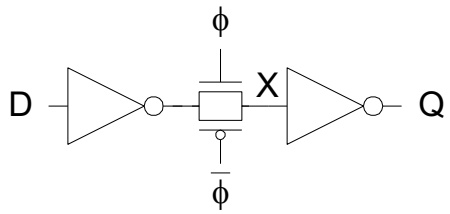
- Principle:
  -
  -
  -

- Solution:

- Symptom
  - Mux works when selected D is 0 but not 1.
  - Or fails at low V_{DD}.
  - Or fails in SFSF corner.

Bad Circuit 2

- Circuit
  - Latch

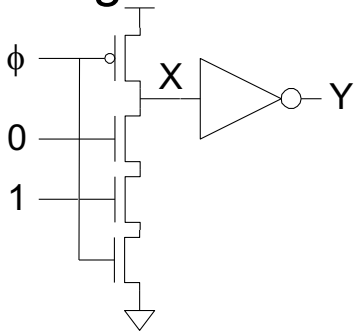


- Principle:
  -
  -
- Solution:

- Symptom
  - Load a 0 into Q
  - Set ϕ = 0
  - Eventually Q spontaneously flips to 1

Bad Circuit 3

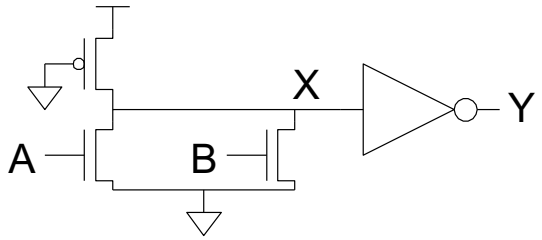
- Circuit
  - Domino AND gate



- Symptom
  - Precharge gate (Y=0)
  - Then evaluate
  - Eventually Y spontaneously flips to 1
- Principle:
  -
  -
- Solution:

Bad Circuit 4

- Circuit
  - Pseudo-nMOS OR

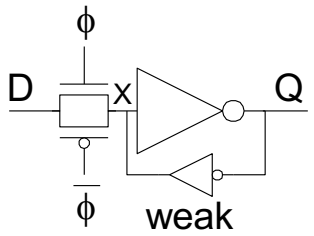


- Principle:
  -
  -
- Solution:

- Symptom
  - When only one input is true, Y = 0.
  - Perhaps only happens in SF corner.

Bad Circuit 5

- Circuit
  - Latch



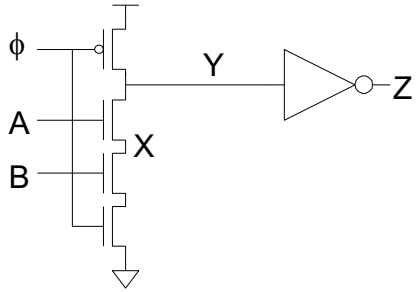
- Principle:
  -

- Solutions:

- Symptom
  - Q stuck at 1.
  - May only happen for certain latches where input is driven by a small gate located far away.

Bad Circuit 6

- Circuit
  - Domino AND gate

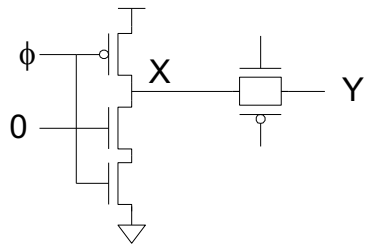


- Principle:
  -
- Solutions:

- Symptom
  - Precharge gate while A = B = 0, so Z = 0
  - Set ϕ = 1
  - A rises
  - Z is observed to sometimes rise

Bad Circuit 7

- Circuit
  - Dynamic gate + latch

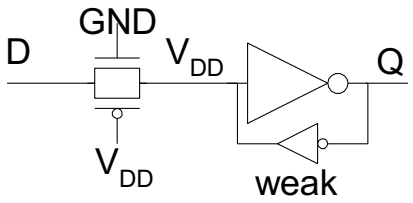


- Principle:
  -
- Solution:

- Symptom
  - Precharge gate while transmission gate latch is opaque
  - Evaluate
  - When latch becomes transparent, X falls

Bad Circuit 8

- Circuit
  - Latch



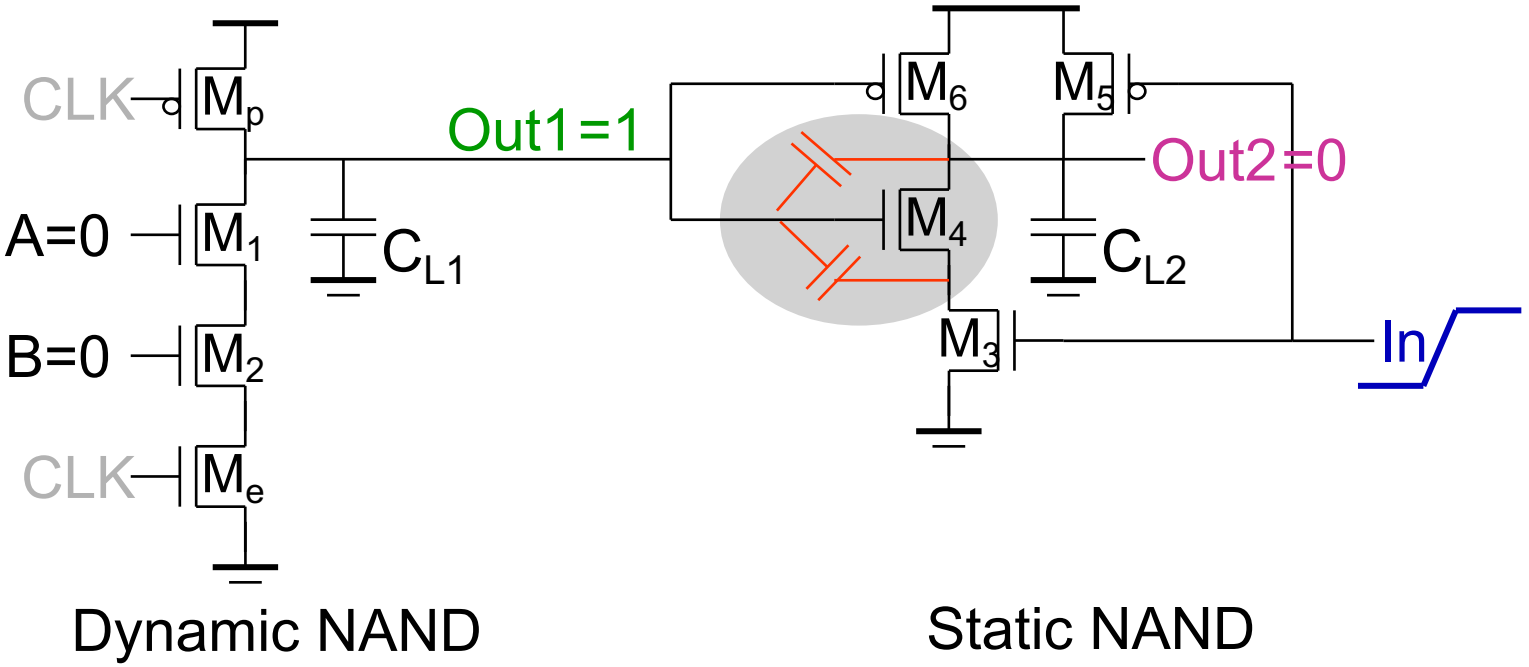
- Symptom
  - Q changes while latch is opaque
  - Especially if D comes from a far-away driver
- Principle:
  -
  -
- Solution:

Summary

- Causes of circuit pitfalls
  - Threshold drops, ratio failures, leakage, charge sharing, power supply noise, coupling, diffusion input noise sensitivity, race conditions, hot spots, soft errors, process (corner) sensitivity,
  - Metastability
  - Minority carrier injection
  - Back-gate coupling
  - Delay matching

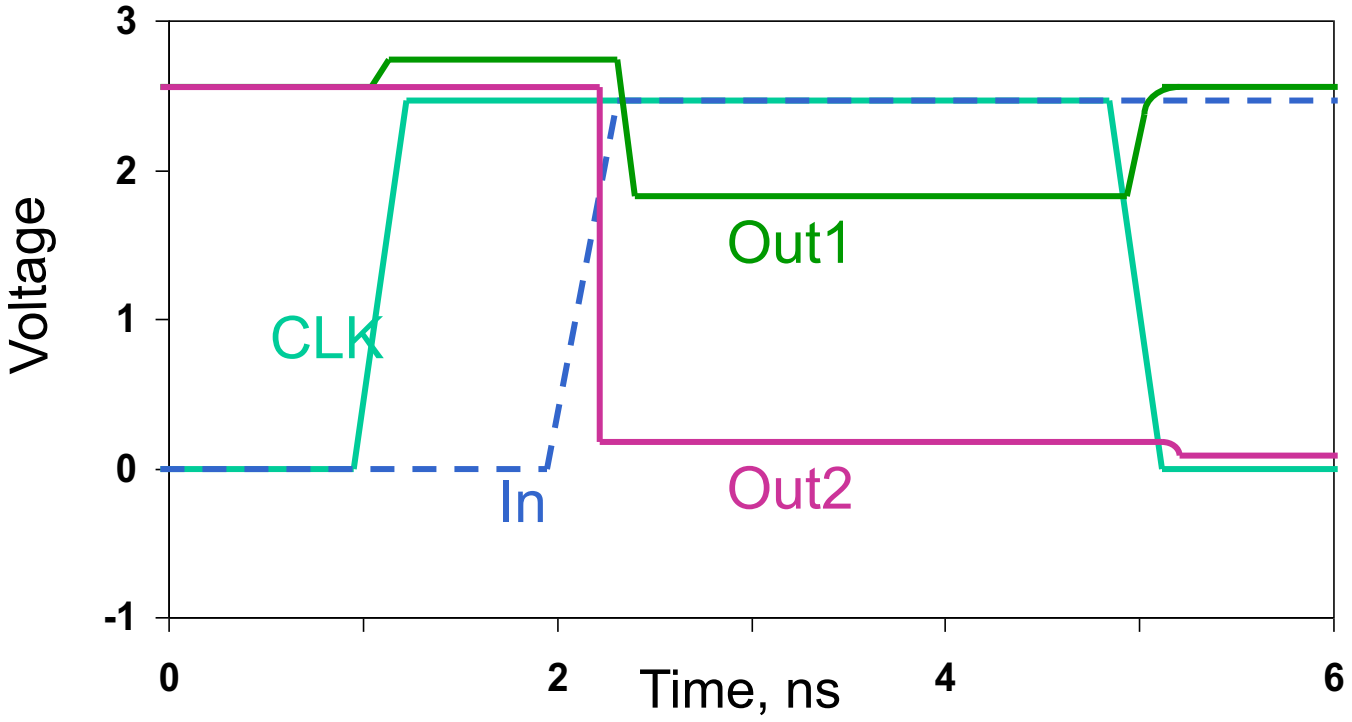
Back-gate Coupling

- Susceptible to crosstalk due to 1) high impedance of the output node and 2) backgate capacitive coupling
  - Out2 capacitively couples with Out1 through the gate-source and gate-drain capacitances of M4



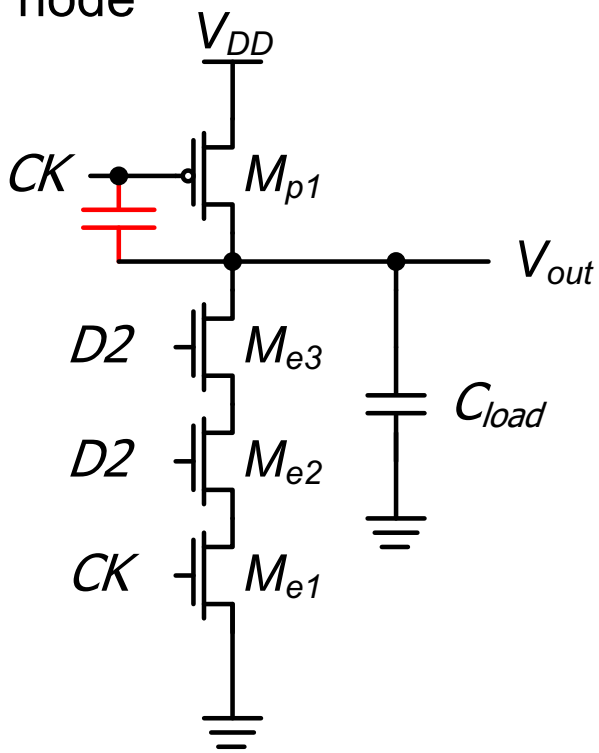
Back-gate Coupling

- Capacitive coupling means Out1 drops significantly so Out2 doesn't go all the way to ground



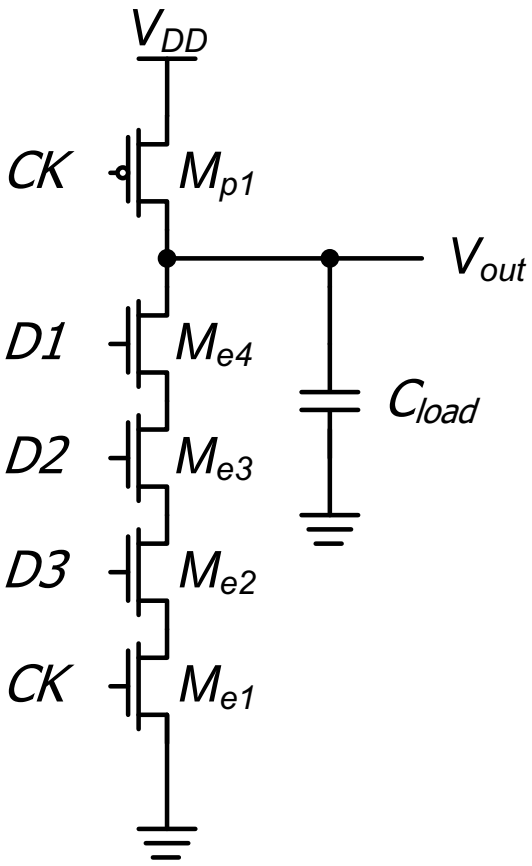
Clock Feedthrough

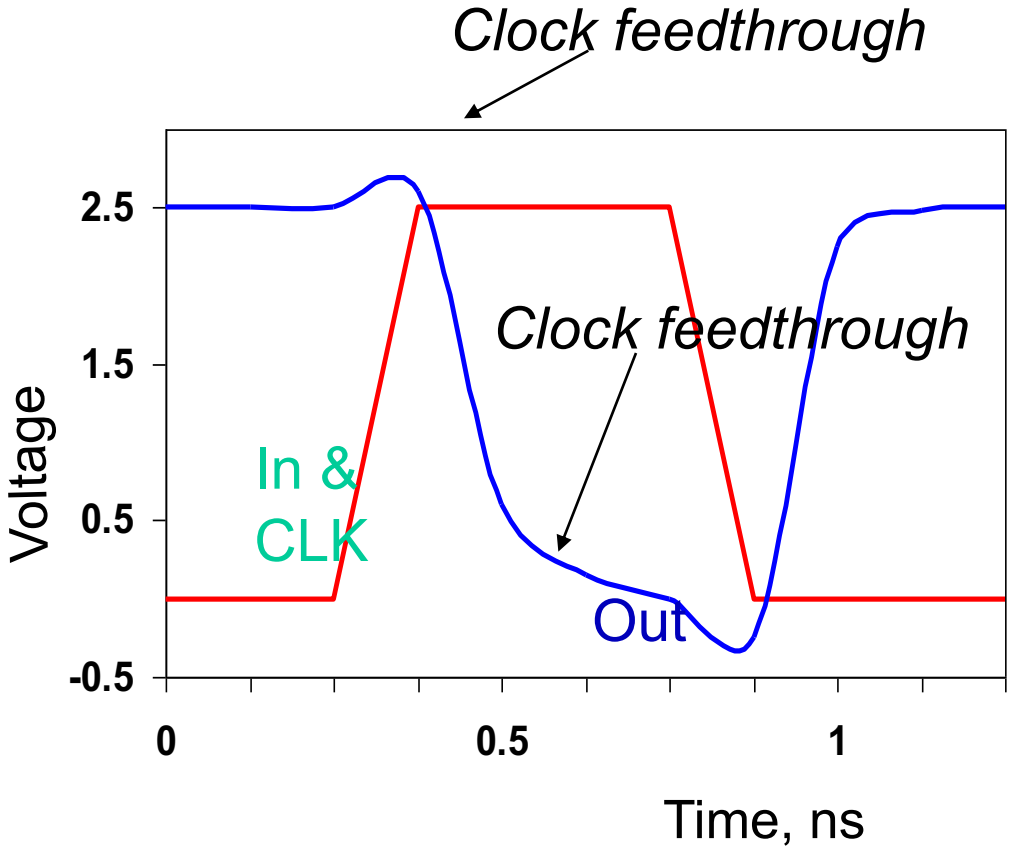
- A special case of backgate capacitive coupling between the clock input of the precharge transistor and the dynamic output node



- Coupling between output node and *CK* input of the precharge device due to the gate-drain capacitance. So V_{out} can rise above V_{DD}. The fast rising (and falling edges) of the clock couple to output.

Clock Feedthrough





Summary

- Static CMOS gates are very robust
  - Will settle to correct value if you wait long enough
- Other circuits suffer from a variety of pitfalls
  - Tradeoff between performance & robustness
- Essential to check circuits for pitfalls
  - For large chips, you need an automatic checker.
  - Design rules aren't worth the paper they are printed on unless you back them up with a tool.