HSPICE LAB (VLSI Systems Design: 2016 Fall) (100pts)

Due: 6PM, 10/29/2016 (upload to KLAS website) Prof. Jinsang Kim

1. (10pts) Design and simulate a matched inverter. Please add corner simulations.
   10 pts: simulation (4), corner (4), Analysis&Comments (2)
2. (42pts) Design, simulate, and layout CMOS Set/Reset Flip-Flop. Also, try to analyze the setup time and the hold time.
   20 pts: simulation & layout (30), setup & hold time (8), Analysis&Comments (4)

3. (48pts) Design and measure the performance of 2 input NAND logic using following logic families. For the performance measurements, please include tpd, tcd, power consumption, etc.

   each 6 pts: measurements (5), Analysis&Comments (1)

   A. Static CMOS
   B. Asymmetric
   C. High-Skew CMOS
   D. Low-Skew CMOS
   E. Pseudo NMOS
   F. Dynamic Logic
   G. Domino Logic (just 2-input AND)
   H. Dural-rail Domino Logic (also NAND)