EE 716 Midterm Exam (2018 Spring)

09:00-10:20, 05/15/2018, Prof. Jinsang Kim

Assume that a matched unit inverter has widths of 50nm for nMOS and 100nm for pMOS, respectively. The 50nm process technology uses the followings unless stated otherwise: $V_{DD} = 1\,V,\ Vto = 0.3\,V, \beta_n = 1mA/\,V^2, \Phi_s = 0.6\,V, \gamma = 0.3\,V^{0.5}, \lambda = 0.02, \tau = 3RC = 3ps,$ $electron velocity = 10^5 cm/s$

1. (10pts) The following netlist is an output of a cell-based design methodology. Decide the design step which produces the following netlist. What is your criteria for your decision?

```
module nco_struct(input          fclock, reset,
                  input  [15:0]  initial_phase, phase_increment,
                  output [7:0] q);

   wire [6:0] ROM_data;
   wire [15:0] phase_0;
   wire [5:0] nbus_5;
   wire [7:0] wave_out;
   wire [5:0] nbus_2;
   wire [15:0] nbus_1;
   wire [15:0] phase;

   xor i_7(wave_out[7], phase[15], 1'b0);
   xor i_6(wave_out[6], phase[15], ROM_data[6]);
   .
   .
   .
   xor i_2(wave_out[2], phase[15], ROM_data[2]);
   .
   .
   not i_10(nbus_5[2], phase[10]);
   not i_9(nbus_5[1], phase[9]);
   not i_8(nbus_5[0], phase[8]);
   generic_flip_flop phase_reg_15(.q(phase[15]), .d(phase_0[15]),
      .clk(fclock));
   .
   .
   .
   .
   quarter_wave sine_table(.addr(the_address), .q(ROM_Table));
   .
endmodule
```

2. (14pts) Design a scannable negative edge sensitive D-type FF at the transistor level.

3. (36pts) Given $Y = AB + C$, We should design the circuits using CMOS logic, pseudo-nMOS logic and domino logic, respectively. Please try to design a perfect circuit as possible. The signal 'A' arrives later than the signal 'B'.
   a) design the transistor-level circuits of each logic
   b) decide the transistor sizes of each logic
   c) estimate the logical effort of the signal 'A' for each logic

	setup time	clk-to-Q delay	D-to-Q delay	Contamination delay	hold time	clock skew
FFs	60 ps	45 ps	-	30 ps	25 ps	50 ps
latches	20 ps	45 ps	35	30 ps	25 ps	50 ps

4. (30pts) For each of the following sequencing styles, determine the minimum logic contamination delay in each clock cycle (or half-cycle for two-phase latches) of 500 ps.
   a) FFs
   b) two-phase latches with 40 ps of nonoverlap between phases
   c) pulsed latches with 80 ps pulse width

5. (10pts) In the case of 4.b), what is the maximum time borrowing of the first combinational logic.

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