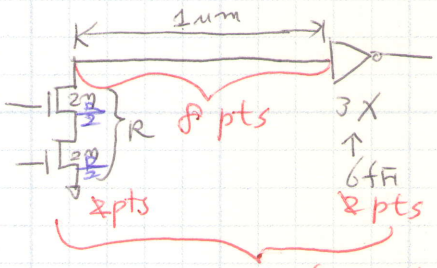
2016 Fall VLSI Systems Designs
Midterm Exam Sols.

1. $2\lambda = 40nm$, '1' → '0' transition.

(10)

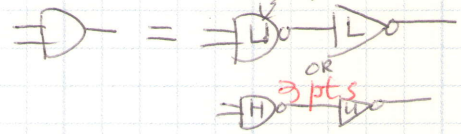


2pts (including Elmore delay model equation)

many other combinations

2.

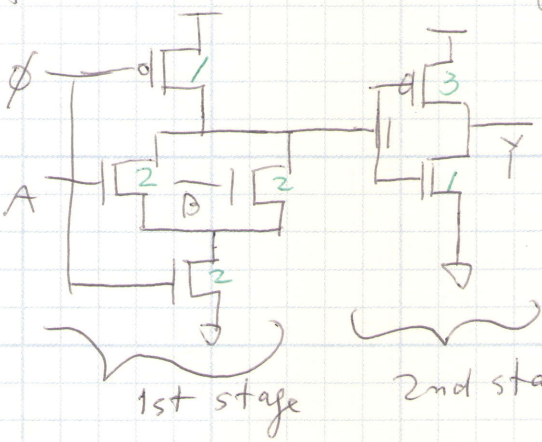
(17)



, $g_D < g_U$ 4pts

3. footed or unfooted Dynamic gate + H, $G = g_1 \cdot g_2$, $P = p_1 + p_2$

(13)



- TR level ckt: 3pts
- sizing: 4pts
- G: 3~~4~~pts } during $\phi = \phi$.
- P: 3~~4~~pts } or average

4. Symptom: ② can be stuck at '1' 3pts

(10)

principle: Leakage 3pts

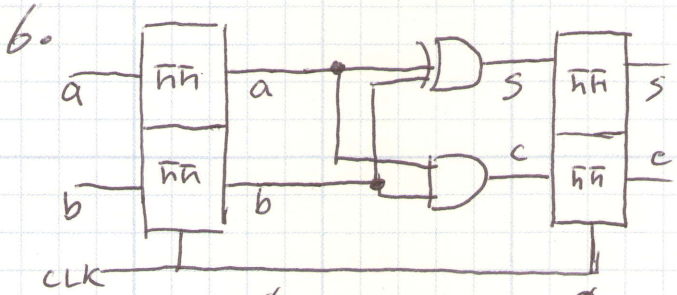
Solution: a feedback Latch. at the output 4pts

5. timing diagram 1pt

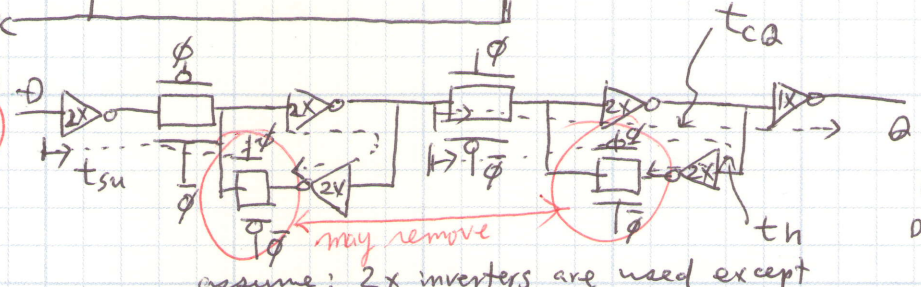
(10)

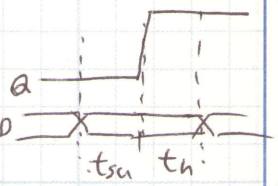
equation 5pts

6.



a)





assume: 2x inverters are used except the output inverter of Q (∵ load !!)

diffusion

b) t_{cq}

4pts = delay (Σ(Tgate + 2x inverter + 1x inverter))

- Tgate delay = $\frac{\text{channel length}}{\text{carrier velocity}} = \frac{45nm}{10^5 cm/s} = 4.5 \times 10^{-11} m/s$ = 45ps
- 2x inverter = $\frac{4R}{2}(6c + 3c + 6c) = \frac{15}{2}Rc = \frac{15}{2}ps = 7.5ps$
- 1x inverter = $3Rc = 3ps$

$= (45 + 7.5 + 3)ps = 55.5ps$

thold ⇒ delay (Σ Tgate + 2x inverter + 2x inverter (feedback loop))

5pts

- delay of 2x inverter at the feedback loop

$= \frac{R}{2}(6c + 10c) = 8ps$

∴ thold = $(45 + 7.5 + 8)ps = 60.5ps$

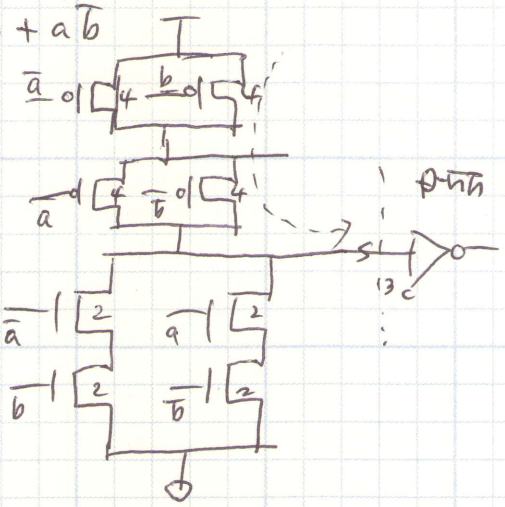
t_{su} = delay (Σ 2x inverter + Tgate + 2x inverter) + 2x inverter (feedback)

5pts

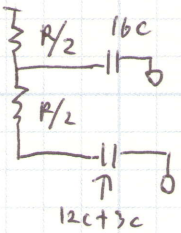
- 2x inverter (front) = $\frac{R}{2}(6c + 10c) = 8ps$
- 2x inverter (back) = $\frac{R}{2}(6c + 10c + 6c) = 11ps$
- 2x inverter (feedback) = $\frac{R}{2}(6c + 10c) = 8ps$

∴ t_{su} = 27ps + 45ps = 82ps

c) $S = \bar{a}b + a\bar{b}$ (14)



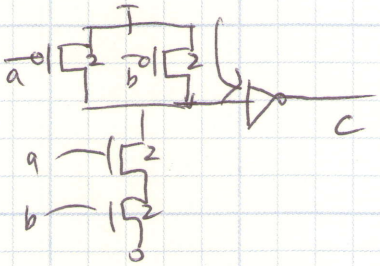
$t_{pd(r)}$ =



inv

$\Rightarrow 8Rc + 15Rc = 23Rc + 3Rc$
$= 26ps$

C =



$t_{pd(r)} = R \cdot (6c + 3c) = 9ps$

∴ t_{pd} of HA = 26 ps 7 pts
t_{cd} of HA = 9 ps 7 pts

d) (7) $f_{max} = \frac{1}{t_{ccq} + t_{pd} + t_{su}} = \frac{1}{(55 + 26 + 82)\,ps} = \frac{1}{163\,ps} = 6.14MHz$

e) (7) $t_{cd} \geq t_{hold} - t_{ccq}$

$26ps > 60.5ps - 55.5ps = 5ps$

∴ this block (does not have) the hold time constraint satisfies