VLSI Systems Designs: Quiz1 (2017 Fall)

3:00-4:30PM, 10/16/2017, Prof. Jinsang Kim

Assume that a matched unit inverter has widths of 45nm for nMOS and 90nm for pMOS, respectively. Assume that the 45nm process technology uses the followings unless stated otherwise:

$V_{DD} = 1\,V,\ Vto = 0.3\,V,\ \beta_n = 1mA/V^2,\ \Phi_s = 0.6\,V,\ \gamma = 0.3\,V^{0.5},\ \lambda = 0.02,\ \tau = 3RC = 1.0ps$

1. (15pts) A transmission gate (T-gate) output terminal is connected to an inverter. When the T-gate is ON, the input is changed from '1' to '0'. Calculate the current of the T-gate right after this input signal transition. Also, estimate the delay of the T-gate.

2. (40pts) Given a boolean equation of $\overline{Y}$= AB+CD(A+B)
   a) draw a transistor-level compound CMOS logic gate (6pts)
   b) determine the sizes of all transistors (6pts)
   d) layout the circuit (ignore design rule) which produces minimum delay as possible (9pts)
   c) estimate the rising propagation delay when the load is a 2 input NOR gate (7pts).
   d) estimate the falling propagation delay when the load is 4 matched inverters (7pts).
   f) compute the parasitic effort of the circuit (5pts)

3. (15pts) Explain the physical mechanisms of threshold shifts in short channels as many as possible.

4. (30pts) If the following description is correct, choose TRUE. Otherwise, choose FALSE. You should briefly specify the technical reasons of your choice. Deduct the point if the reason is not correct (each 5 pts).
   ① High-K dielectric material between the gate and channel is useful for reducing the tunneling effect of the dielectric insulator.
   ② Subshreshold leakage due to the weak inversion of a planner channel can be reduced using 3D-type transistors.
   ③ NBTI can be reduced by decreasing the number of dangling bonds and the trapped charge at the oxide.
   ④ IF the charging current is larger than the discharging current, high noise margin is larger than low noise margin.
   ⑤ The hot carrier effect can be reduced by applying higher drain voltage.
   ⑥ When the diffusion and substrate diodes become forward-biased, the latchup can be greatest. -- END --