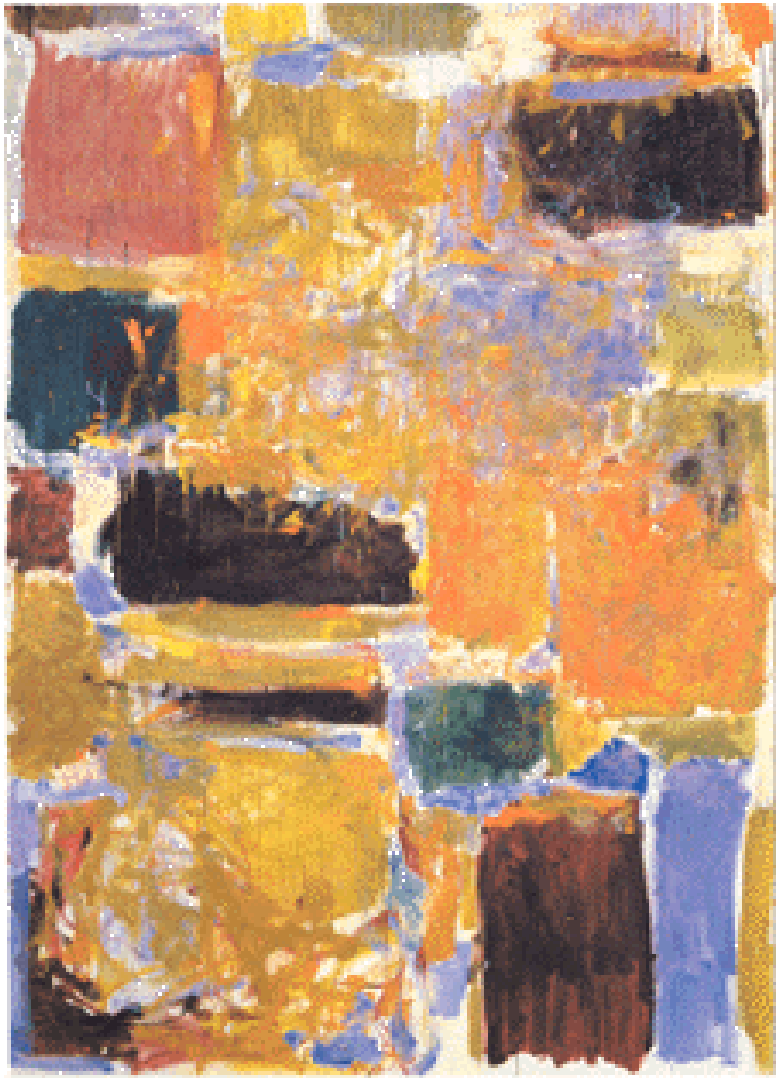


Digital Integrated Circuits
A Design Perspective

Jan M. Rabaey
Anantha Chandrakasan
Borivoje Nikolic

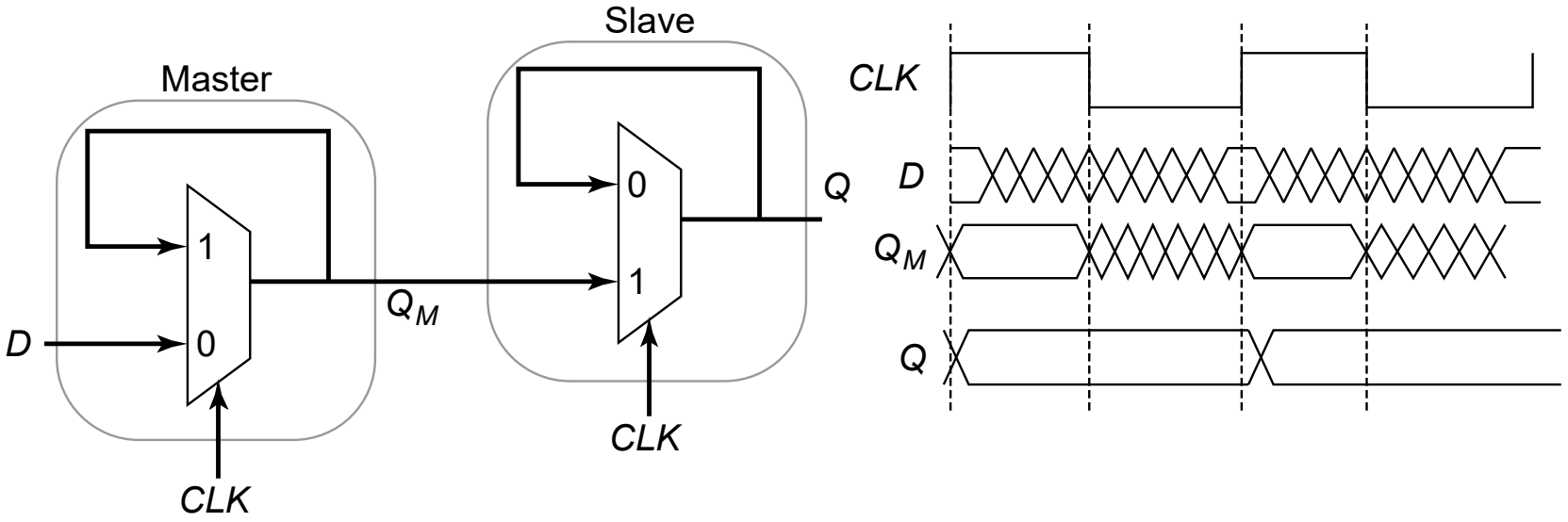
Designing Sequential Logic Circuits

April 15, 2004

Class Notes

- Pls. Respond to “Move Final” email
- Pls. Don’t fall behind on project.
- Policy on Project Collaboration
  - Discussions welcome!
  - Reverse-engineering welcome!
  - Copying binary layouts NOT welcome!
  - We will compare your final cell layouts

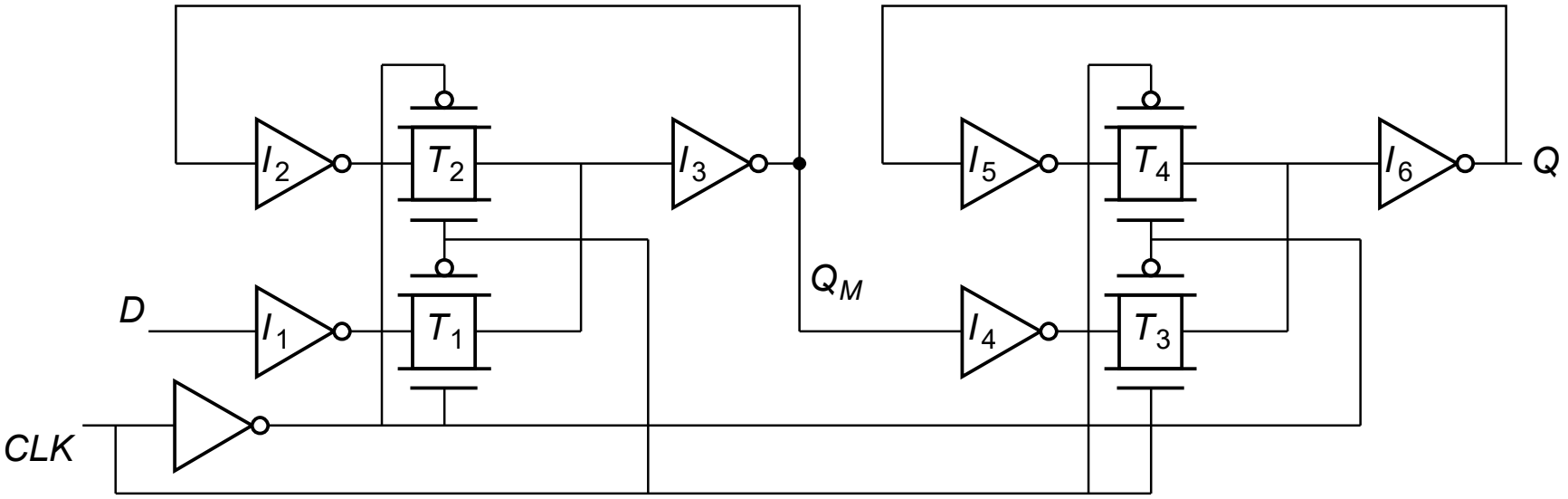
Master-Slave (Edge-Triggered) Register



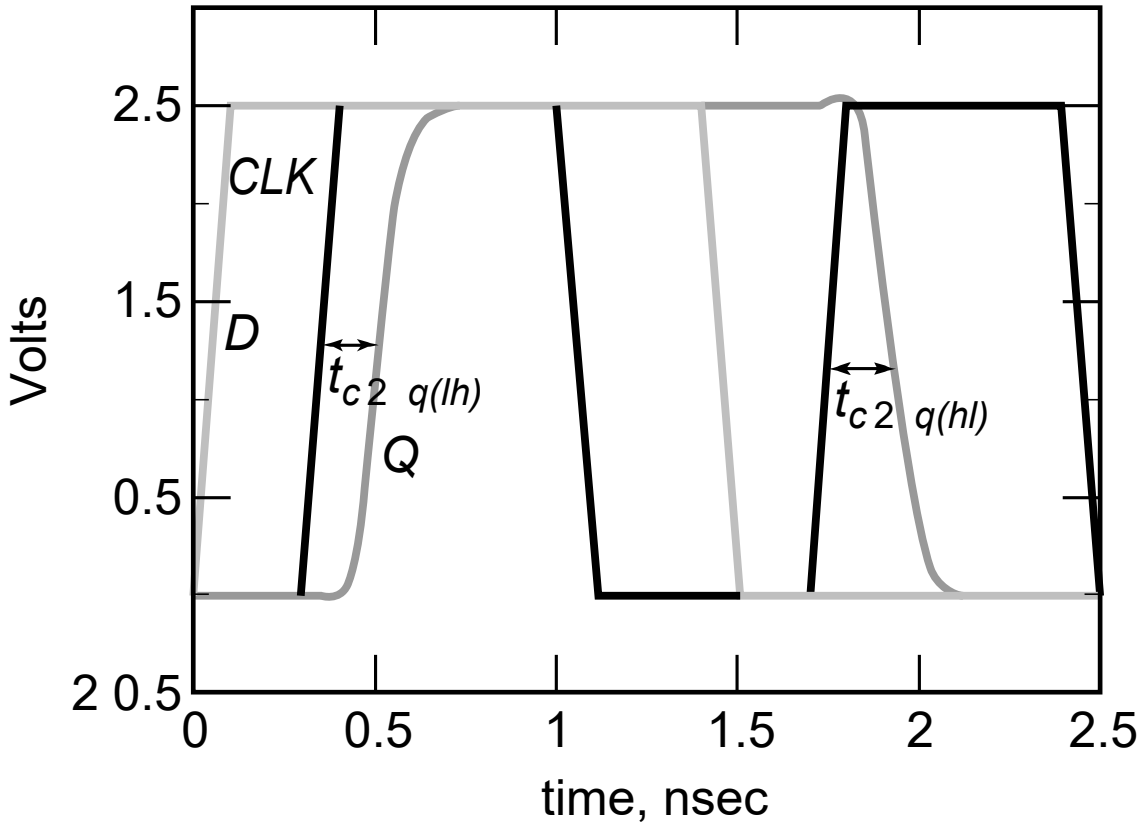
Two opposite latches trigger on edge
Also called master-slave latch pair

Master-Slave Register

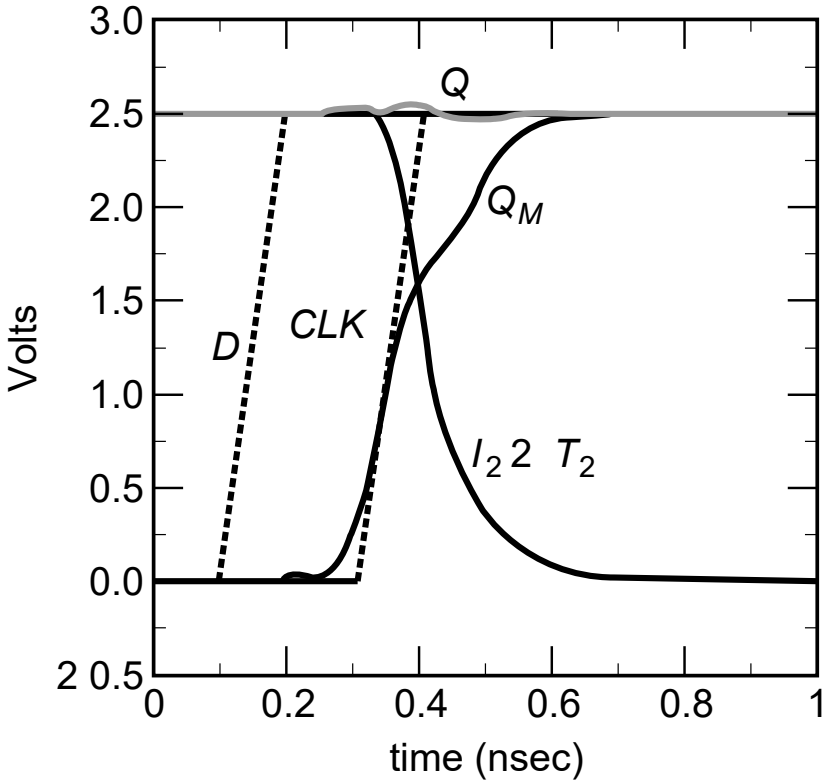
Multiplexer-based latch pair



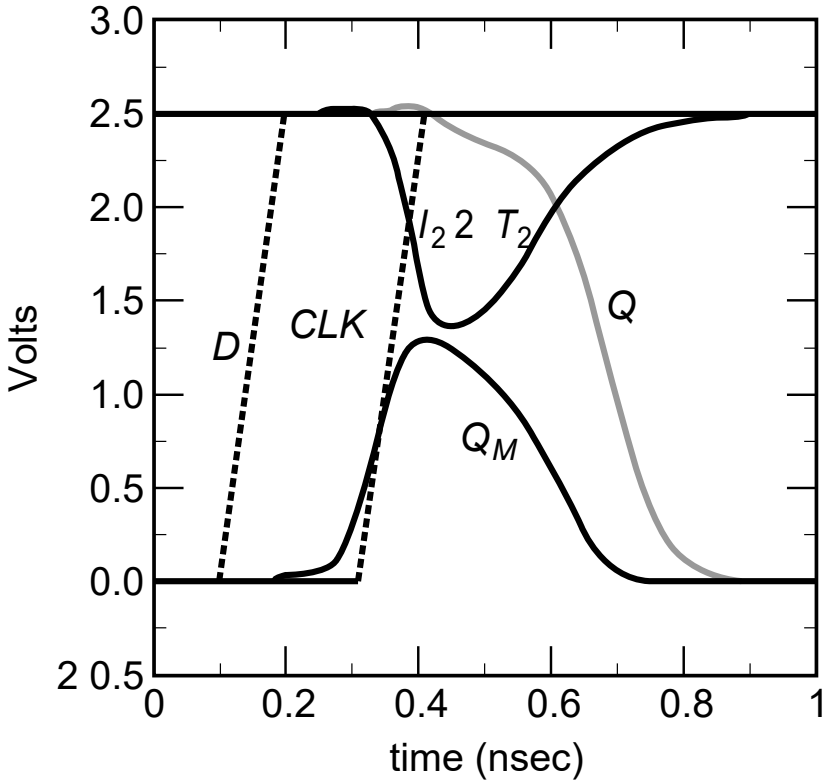
Clk-Q Delay



Setup Time

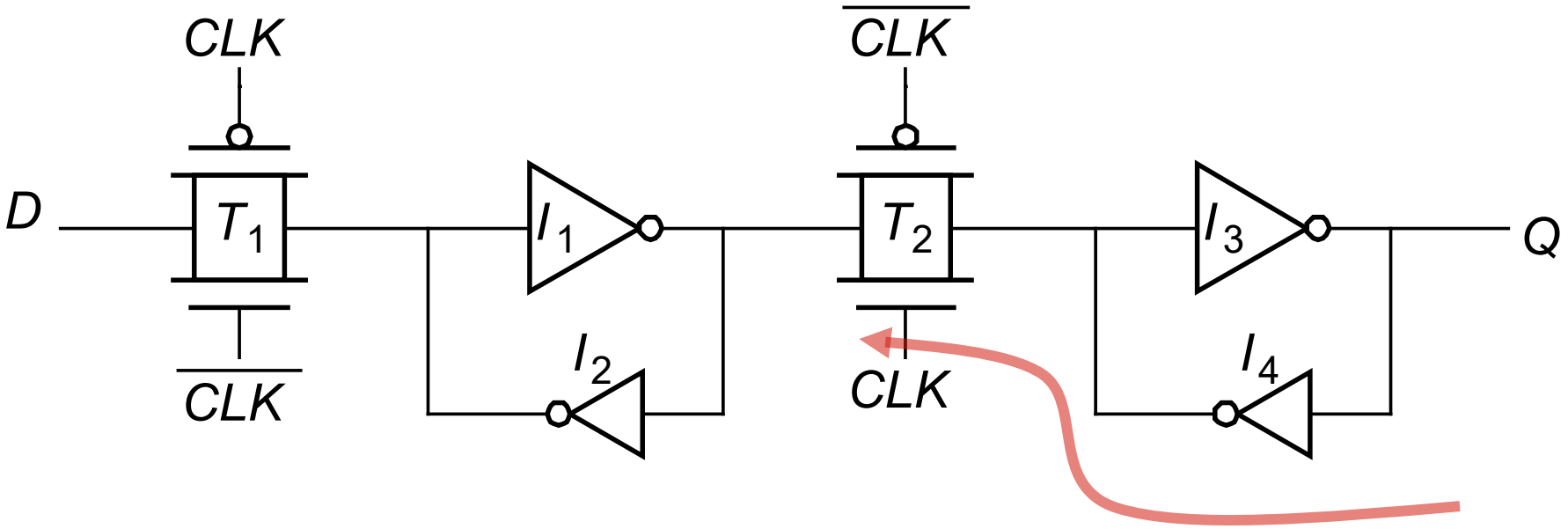


(a) T_{setup} 5 0.21 nsec

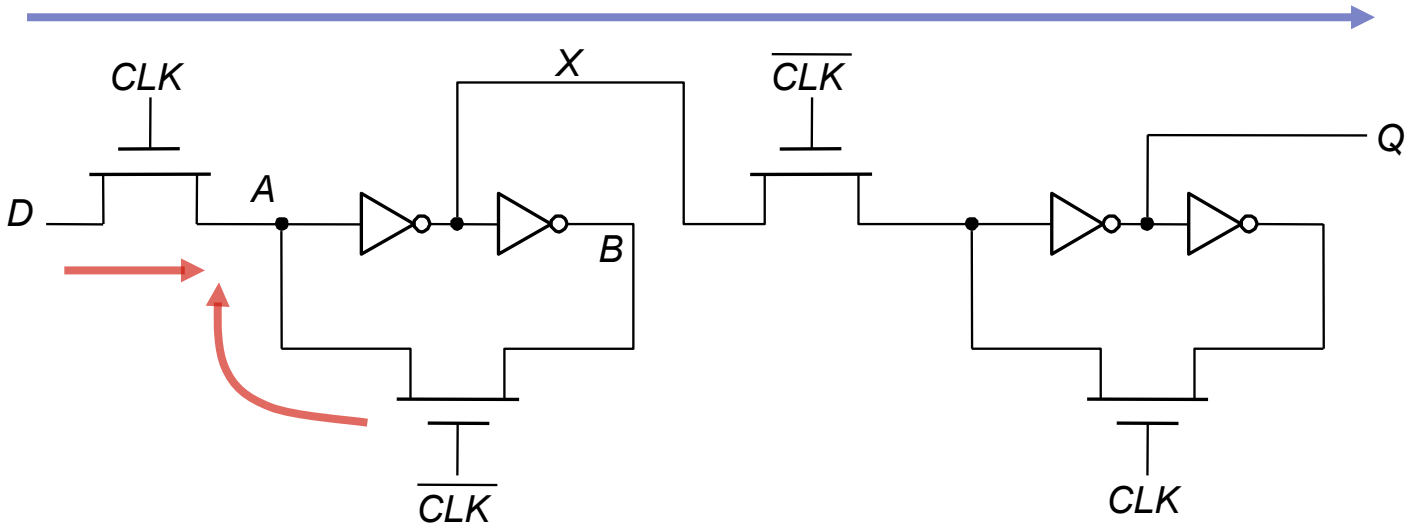


(b) T_{setup} 5 0.20 nsec

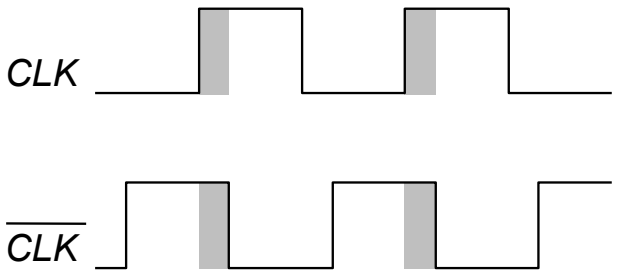
Reduced Clock Load Master-Slave Register



Avoiding Clock Overlap



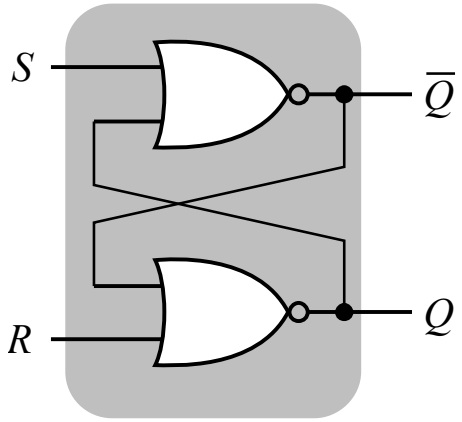
(a) Schematic diagram

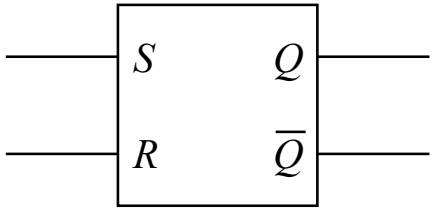


(b) Overlapping clock pairs

Overpowering the Feedback Loop — Cross-Coupled Pairs

NOR-based set-reset



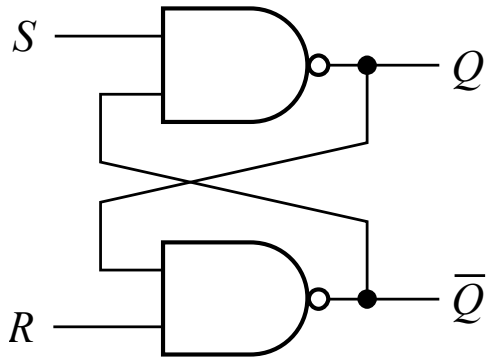


S	R	Q	$\overline{Q}$
0	0	Q	$\overline{Q}$
1	0	1	0
0	1	0	1
1	1	0	0

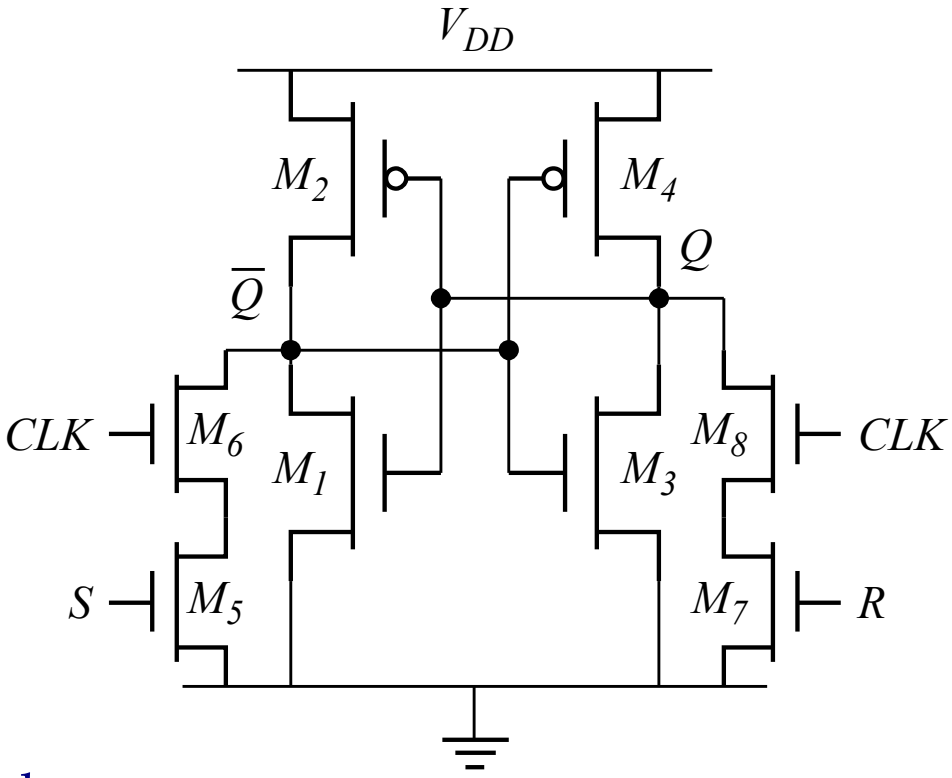
Forbidden State

Cross-Coupled NAND

Cross-coupled NANDs

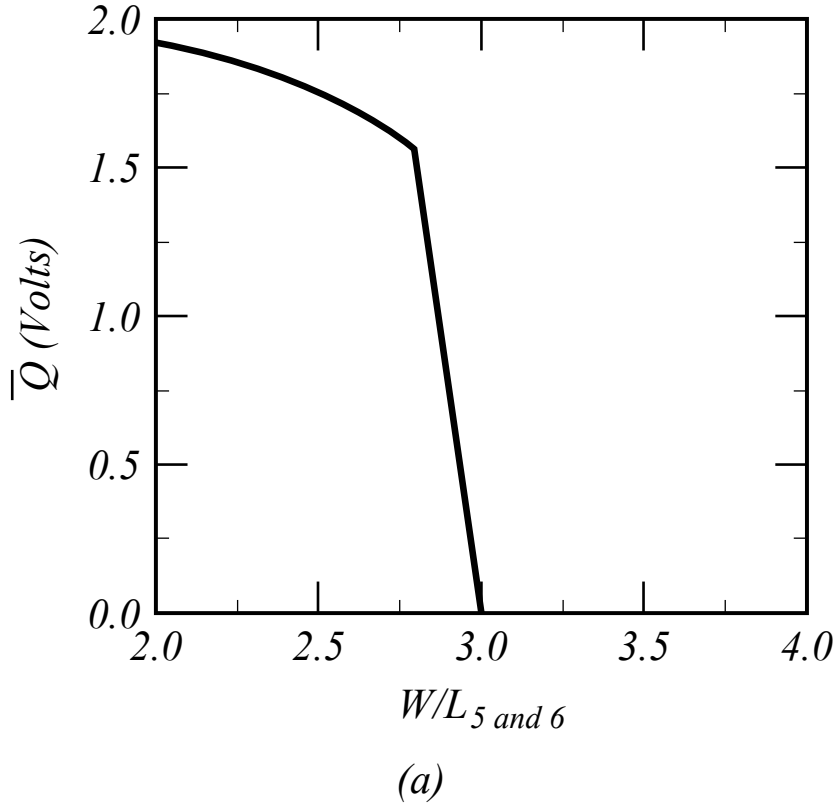


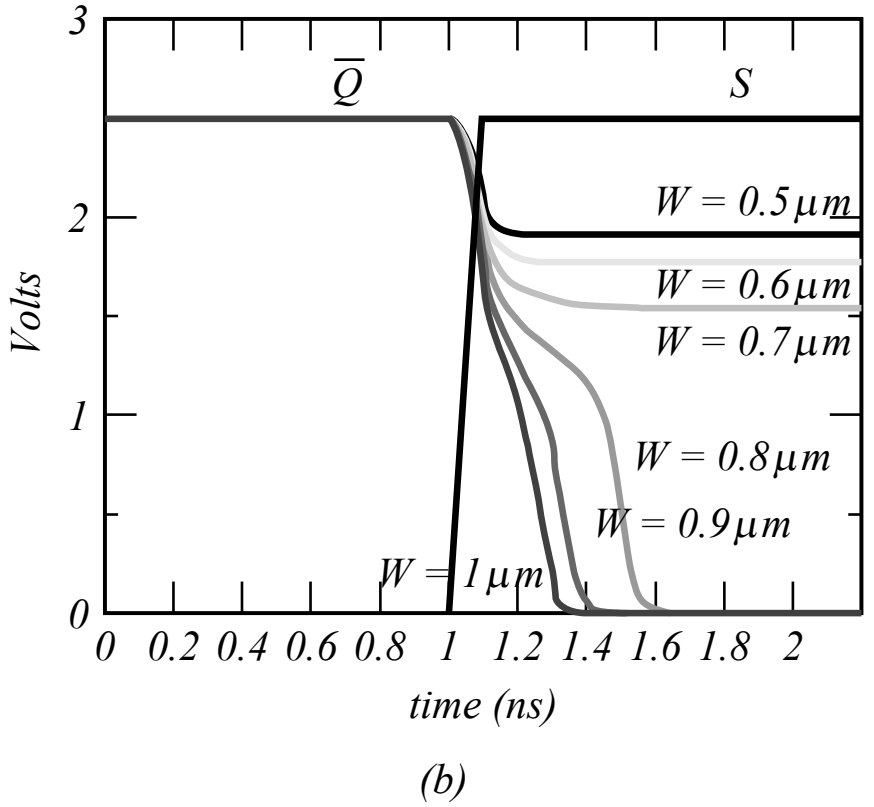
Added clock



This is not used in datapaths any more, but is a basic building memory cell

Sizing Issues



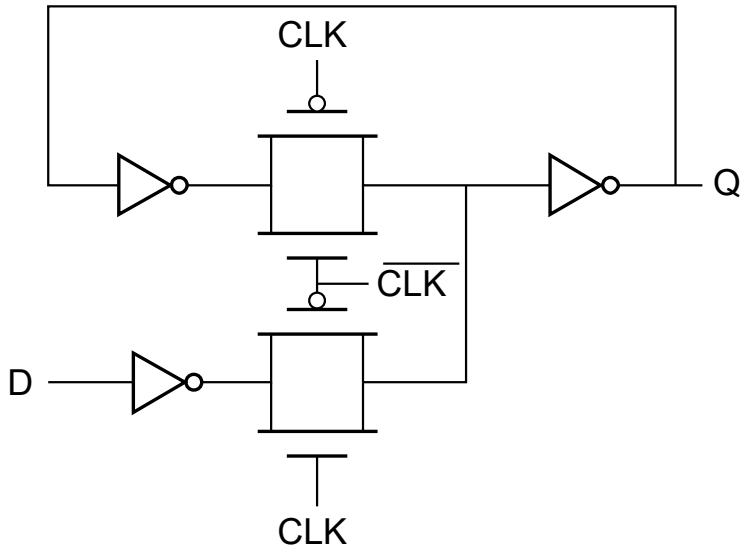


Output voltage dependence on transistor width

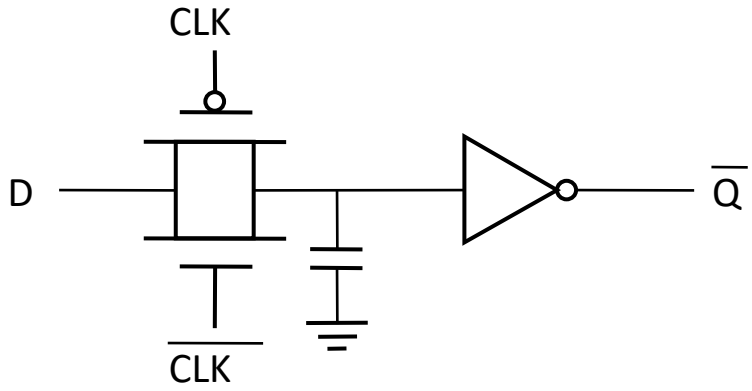
Transient response

Storage Mechanisms

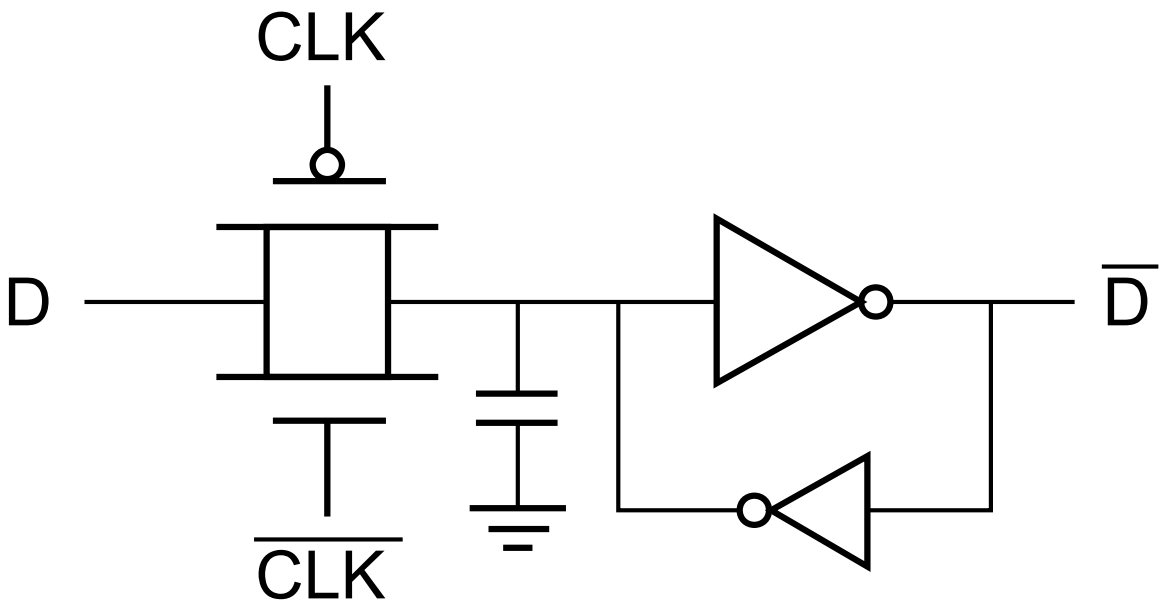
Static



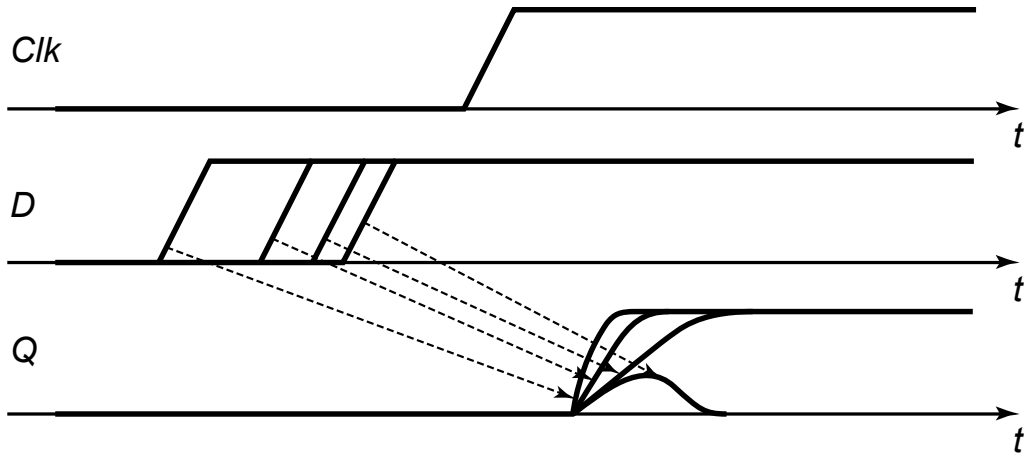
Dynamic (charge-based)



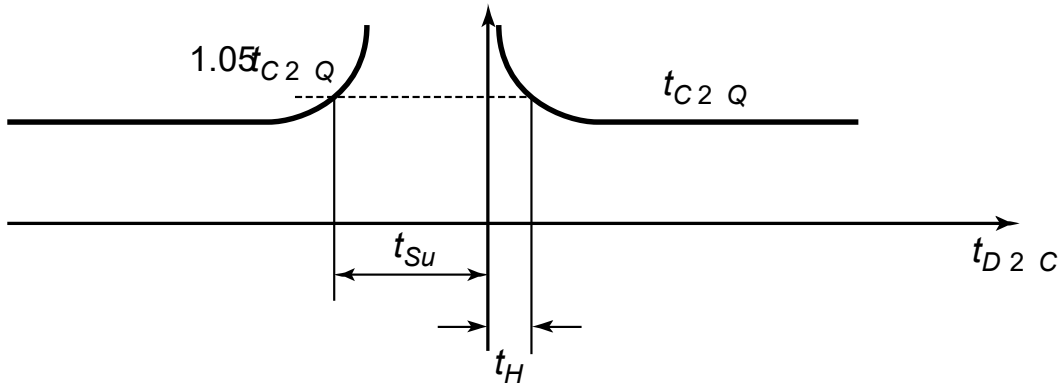
Making a Dynamic Latch Pseudo-Static



More Precise Setup Time



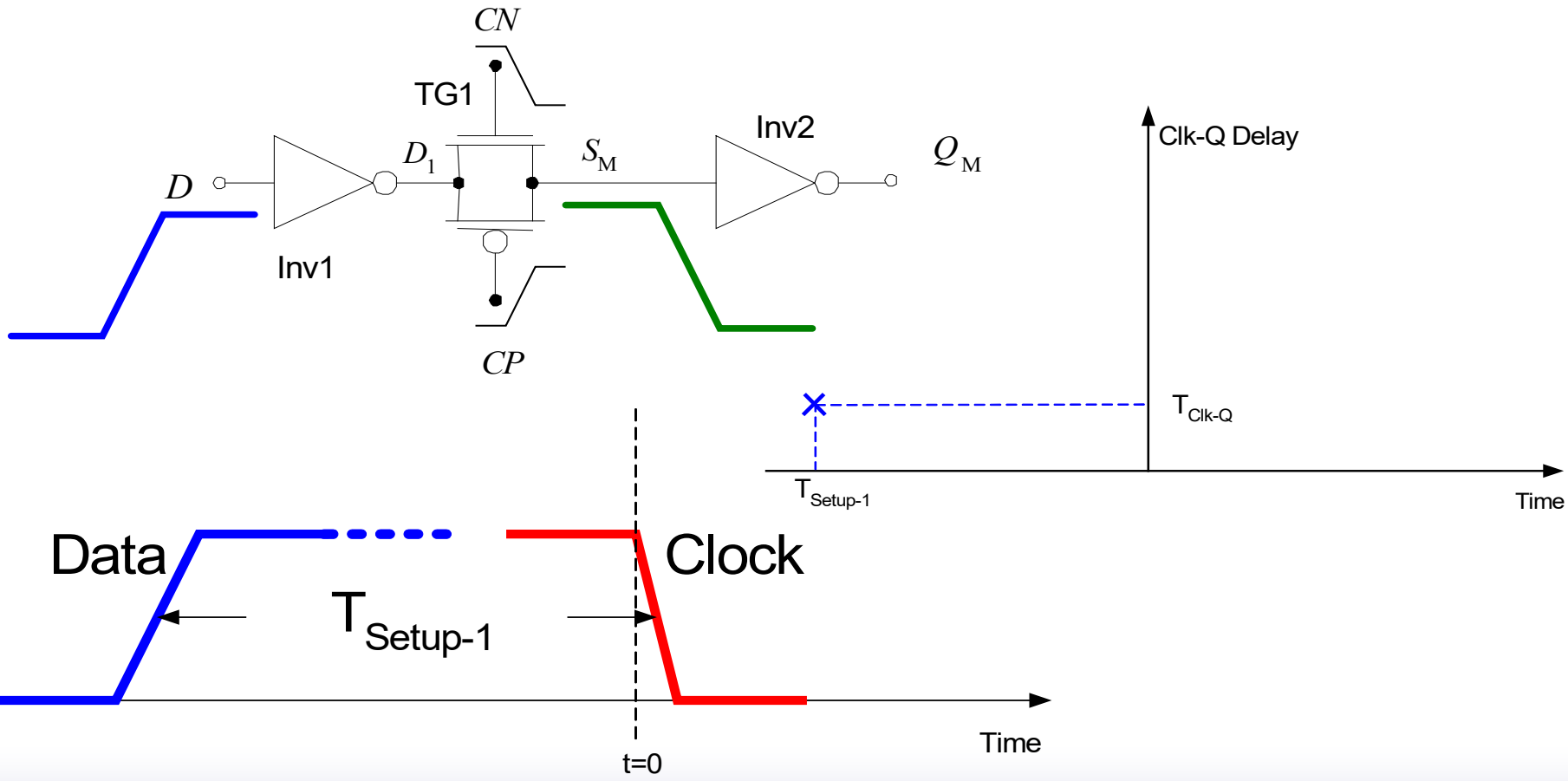
(a)



(b)

Setup/Hold Time Illustrations

Circuit before clock arrival (Setup-1 case)



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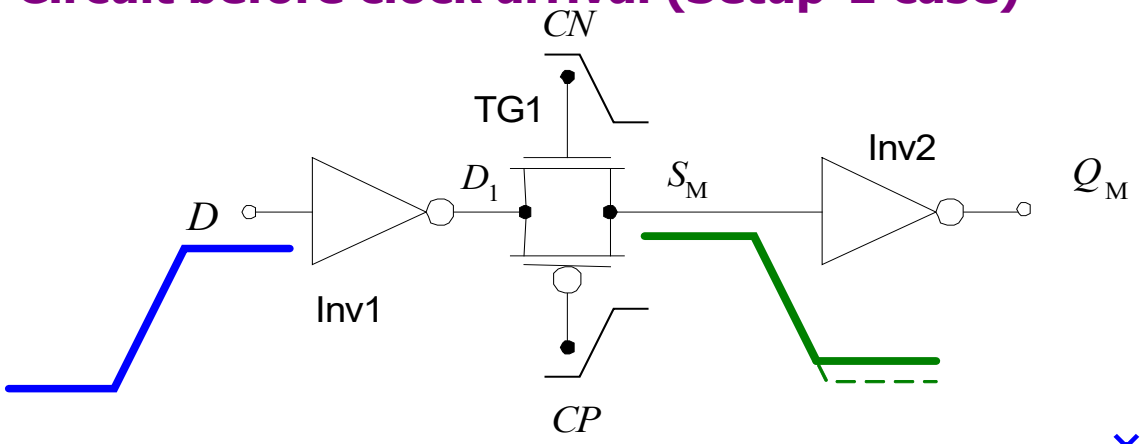

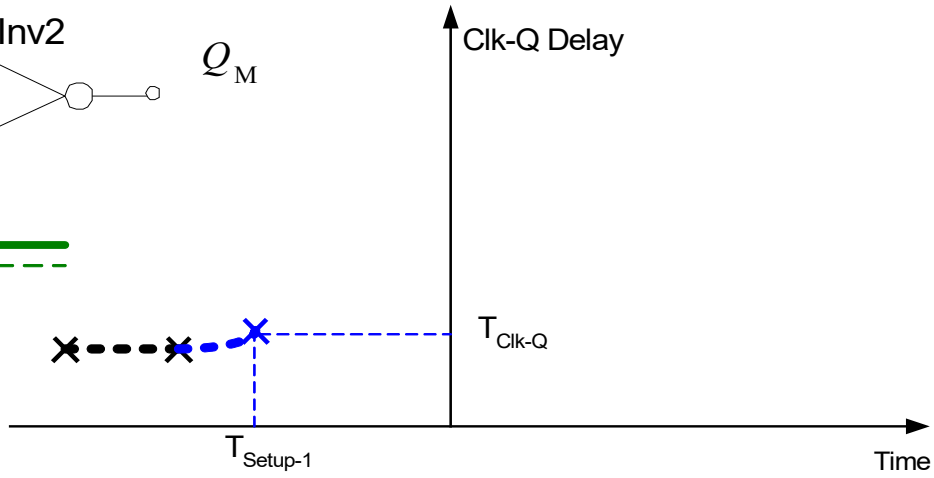

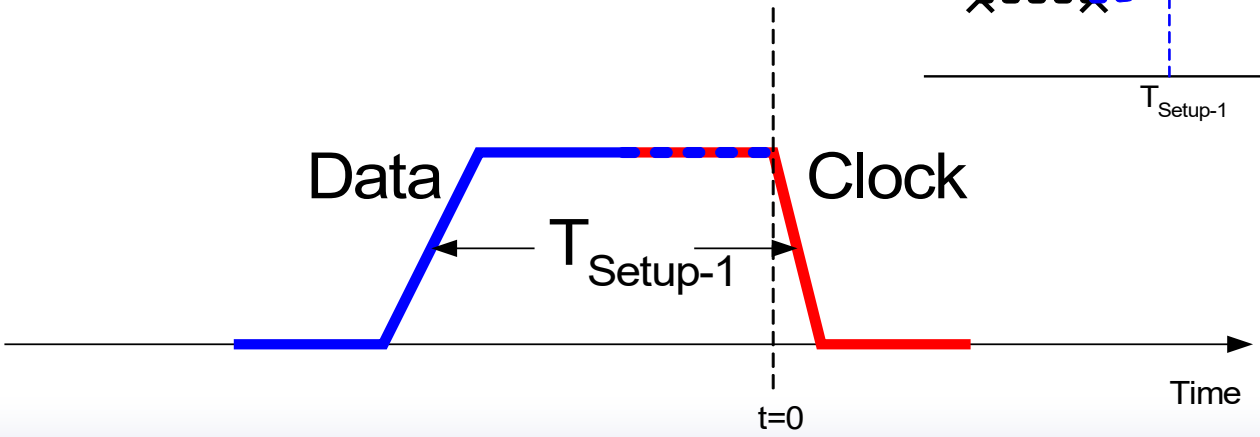

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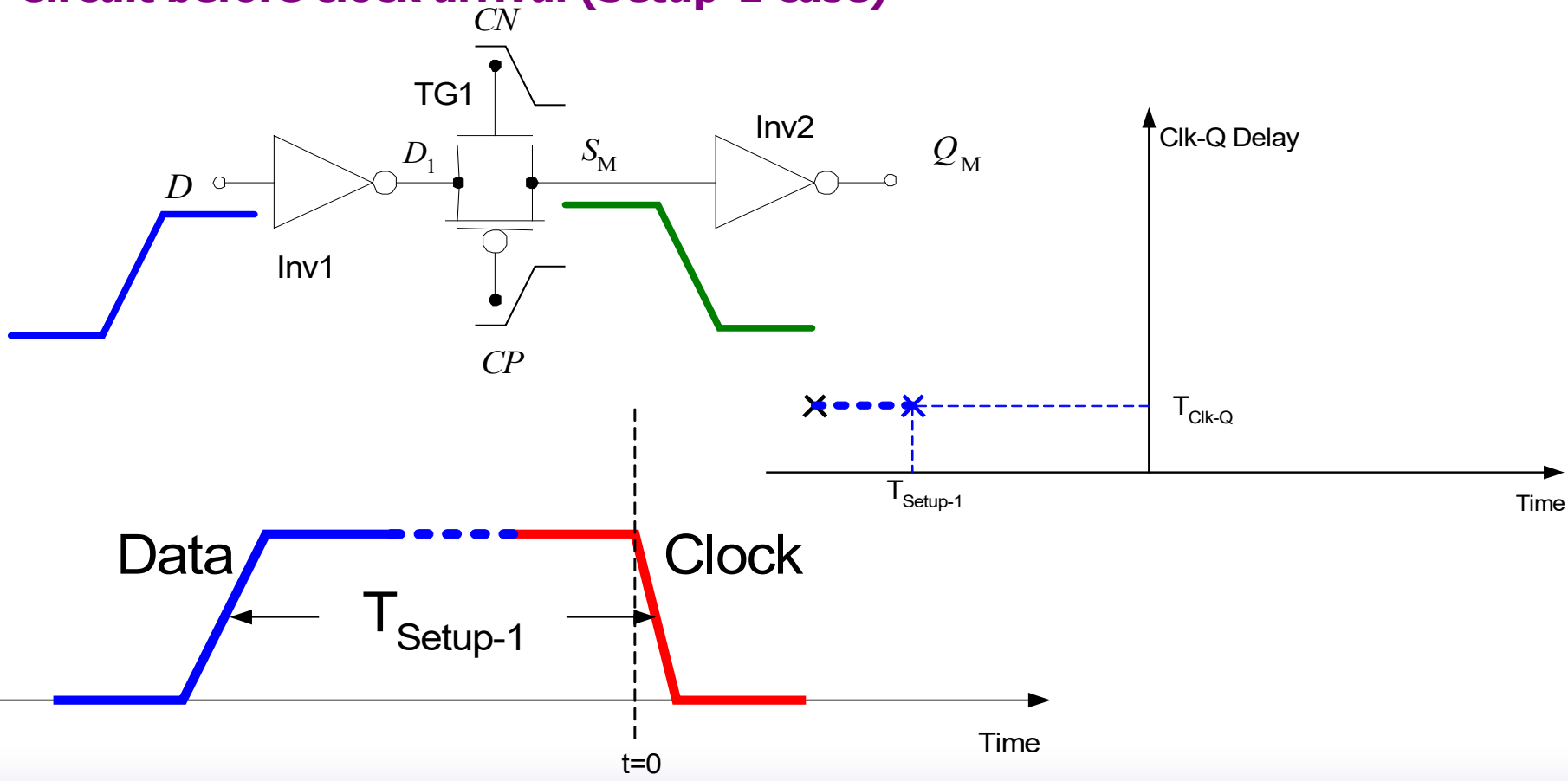
Circuit before clock arrival (Setup-1 case)



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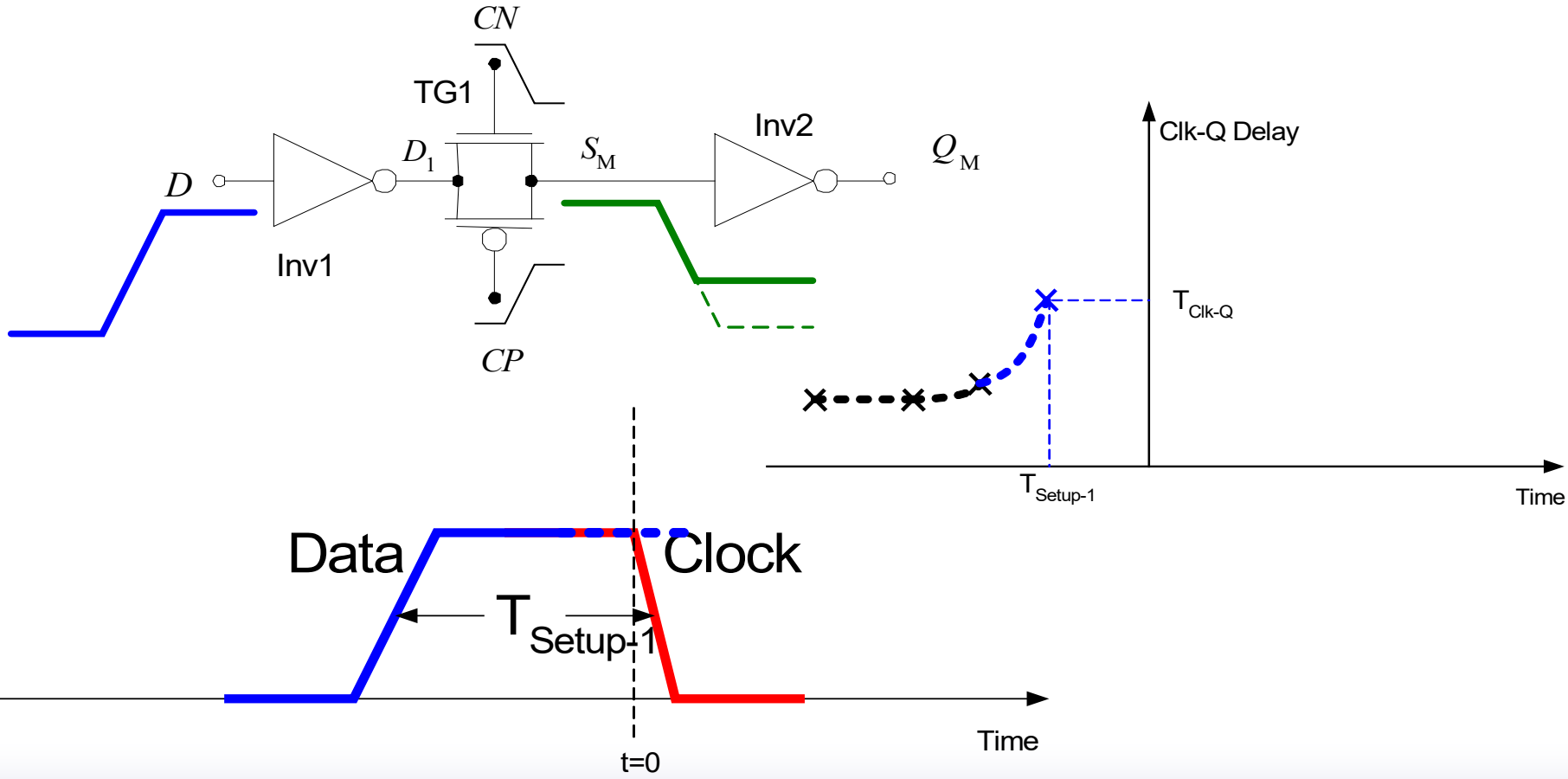
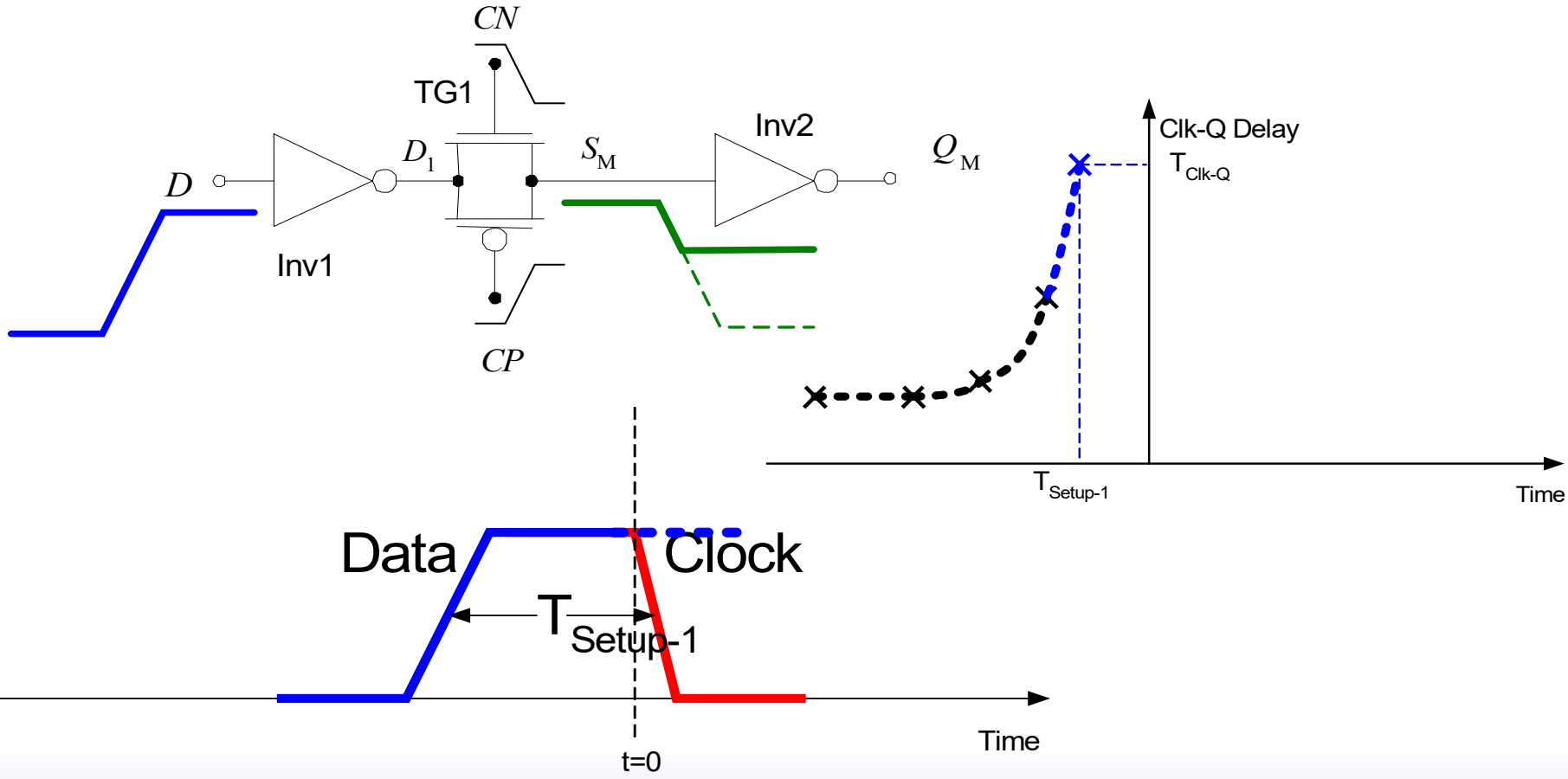
Circuit before clock arrival (Setup-1 case)

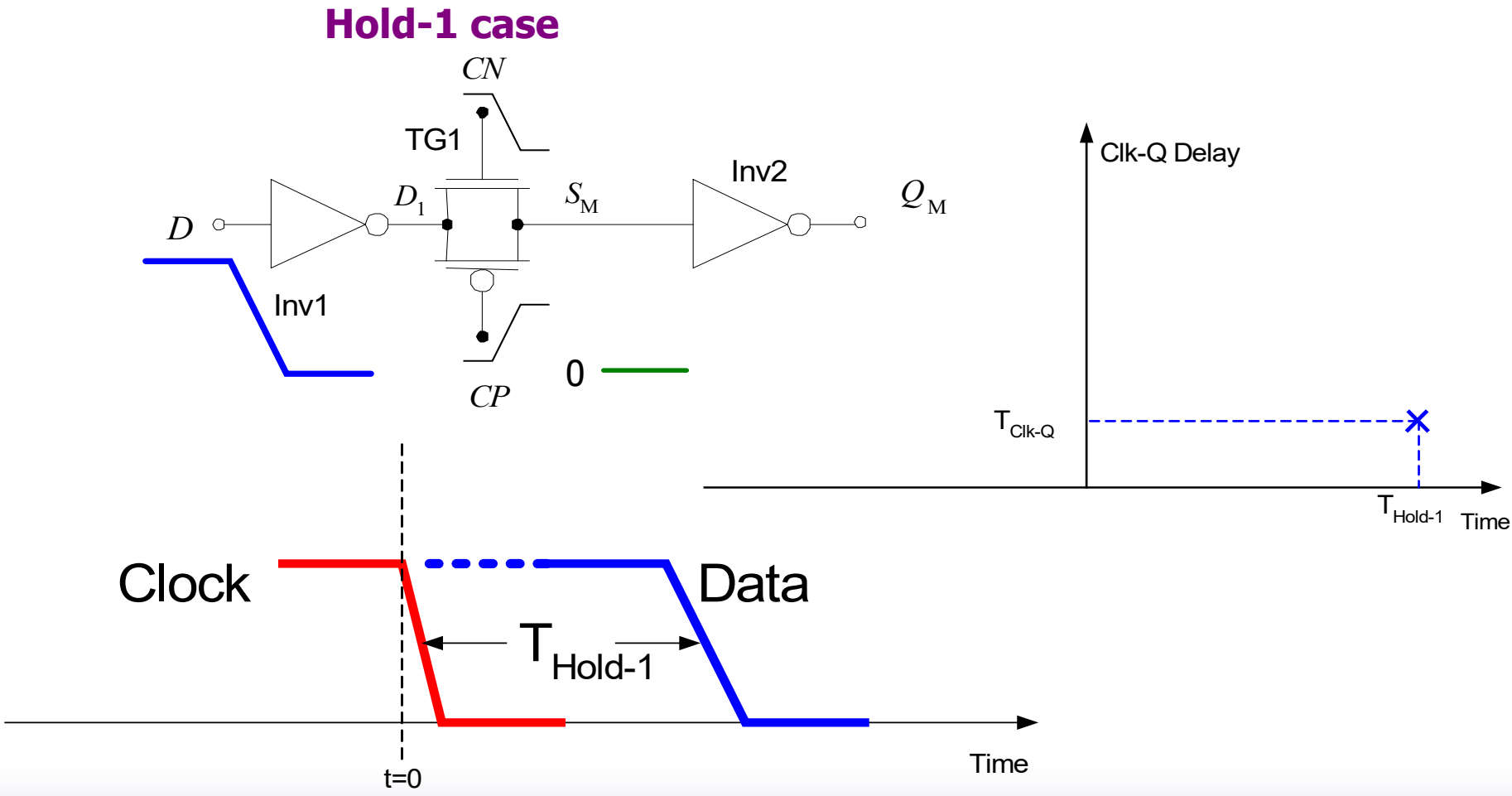


Setup/Hold Time Illustrations

Circuit before clock arrival (Setup-1 case)



Setup/Hold Time Illustrations



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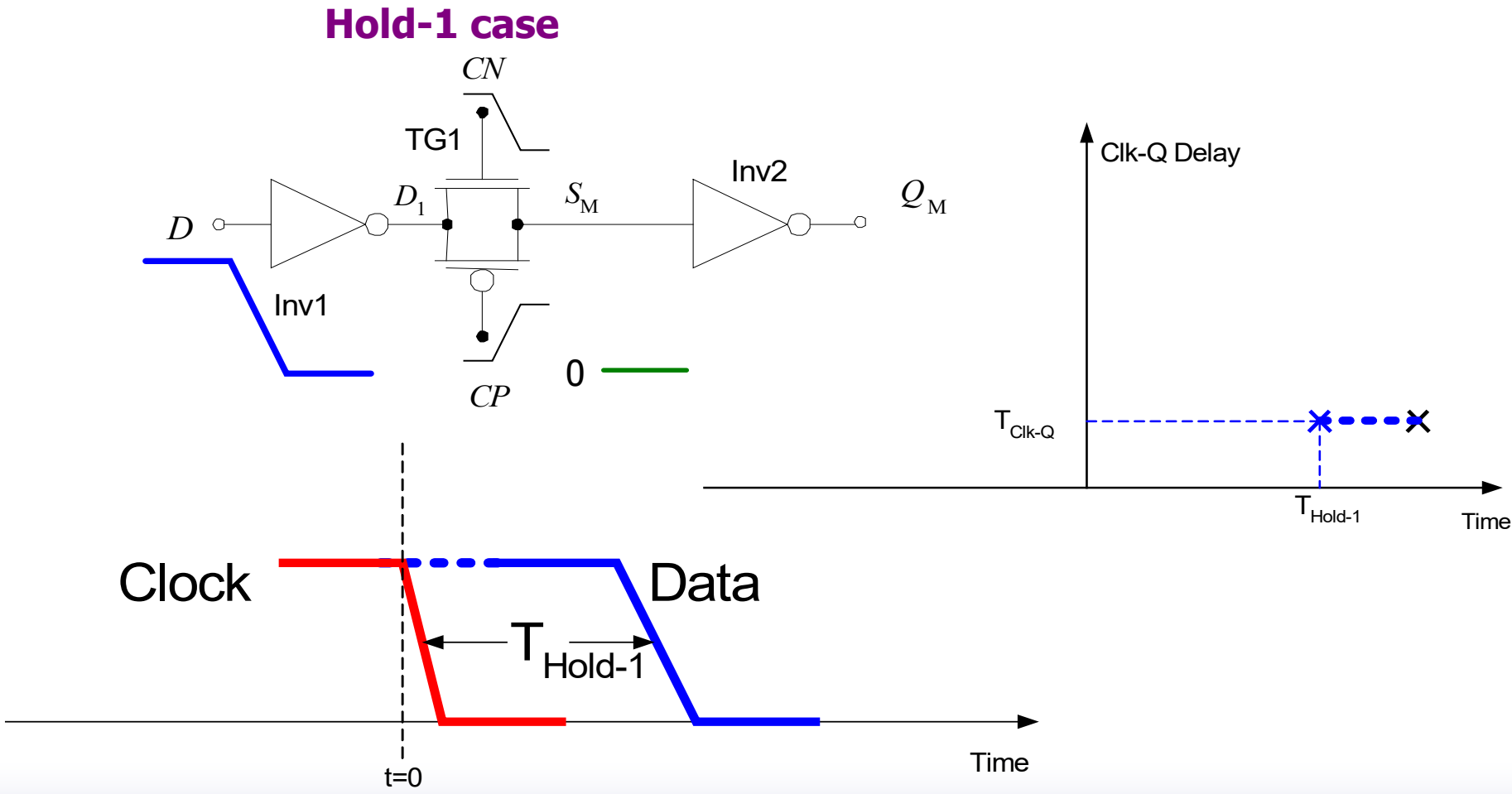
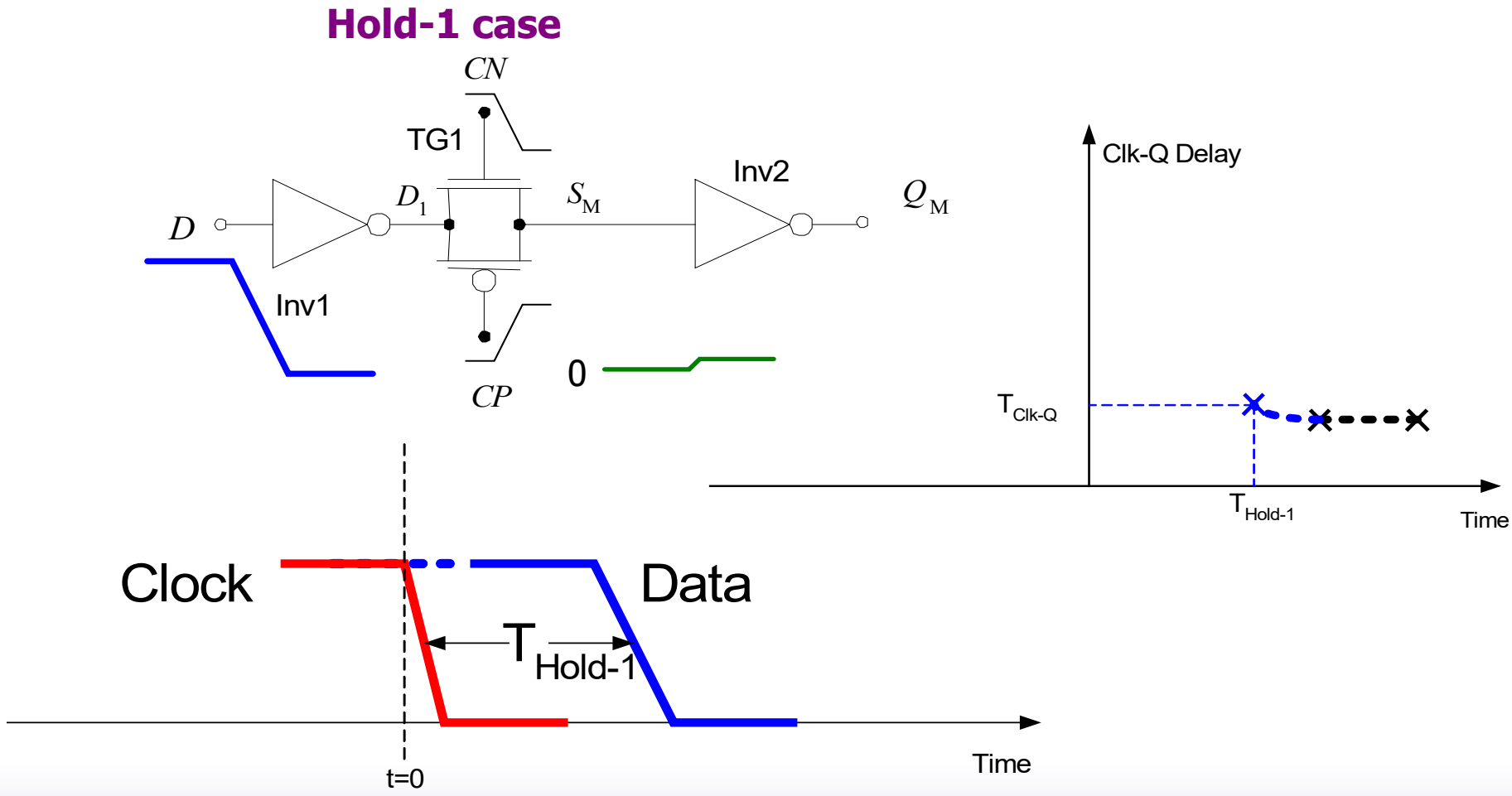
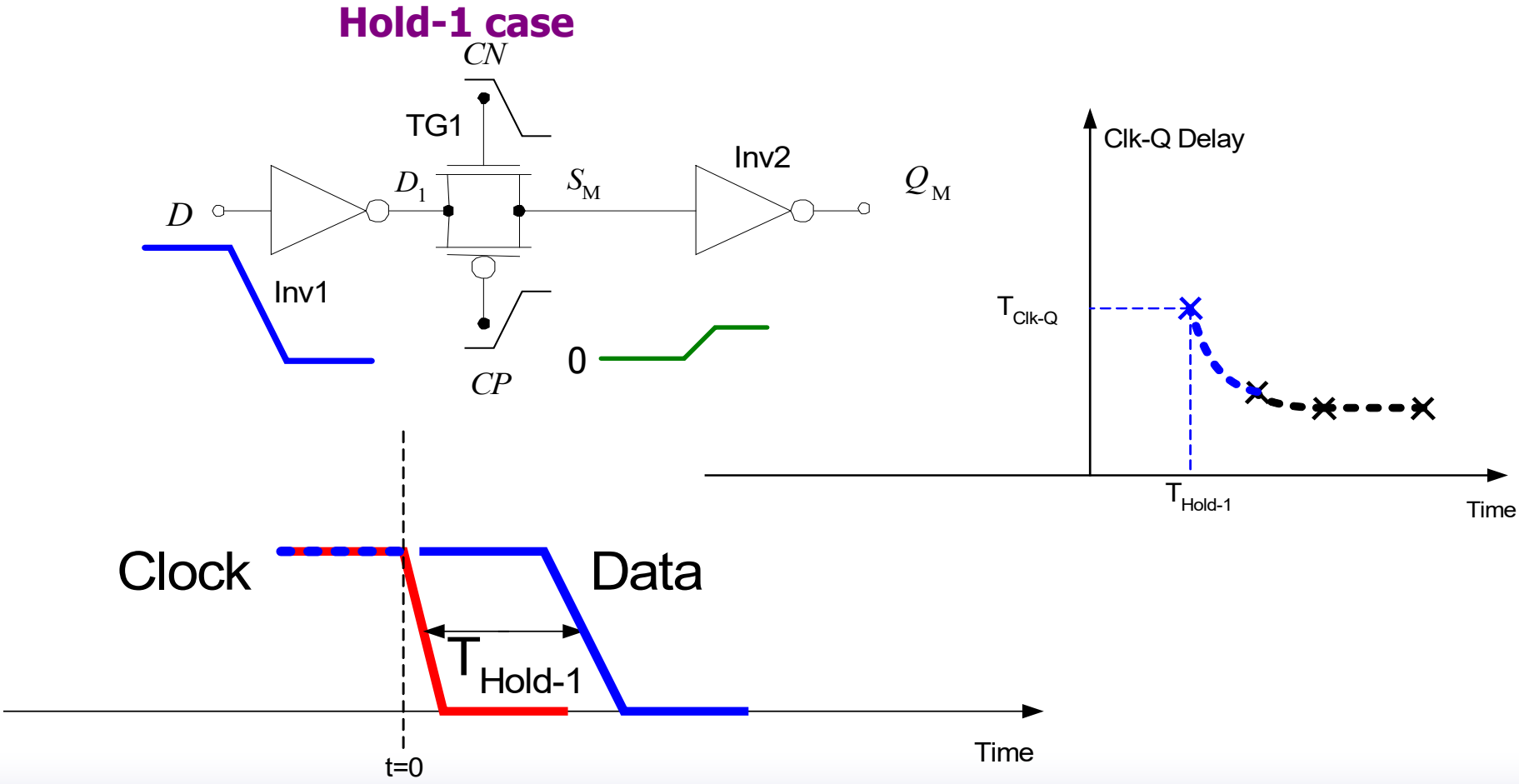


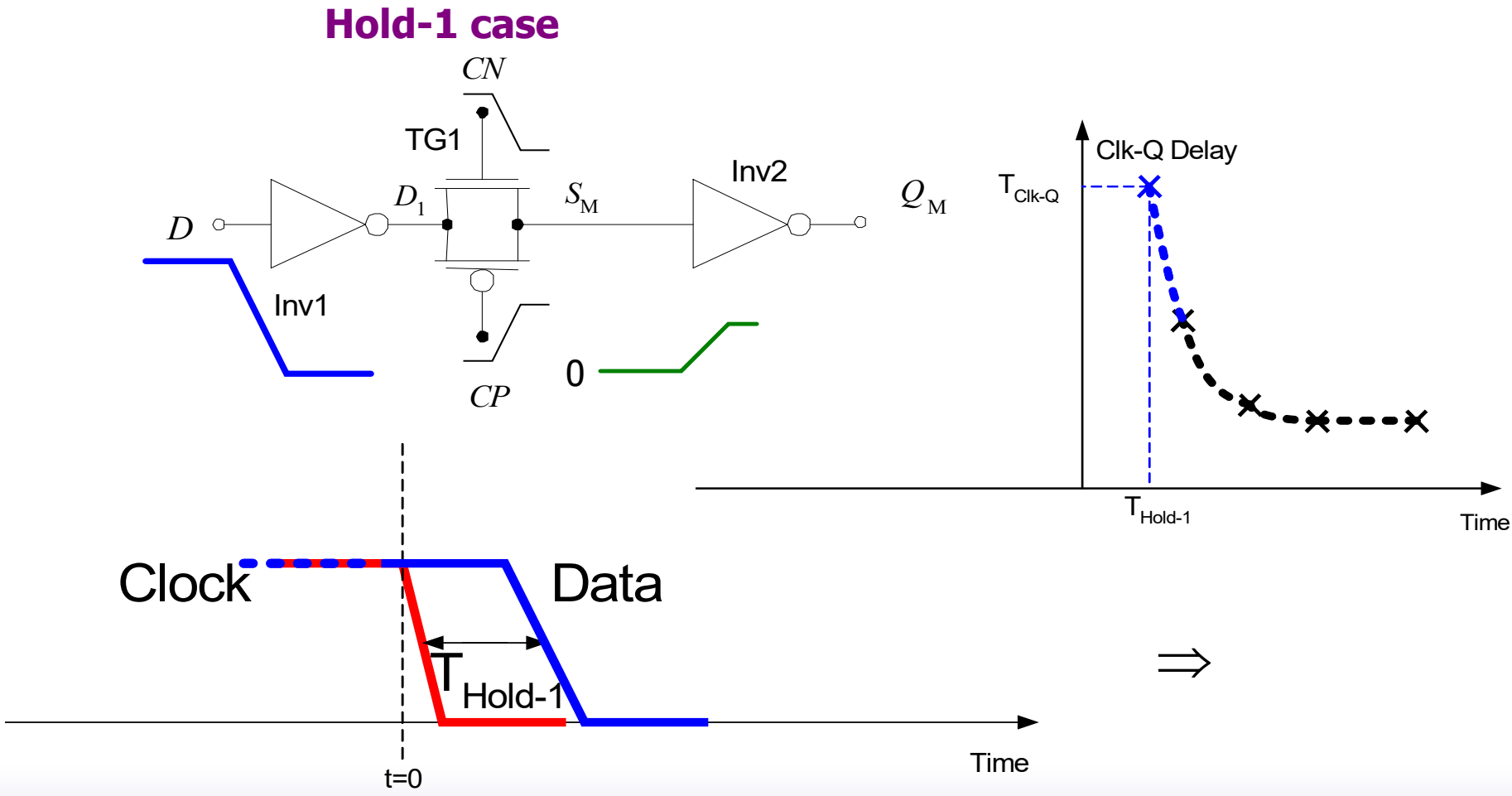
Setup/Hold Time Illustrations



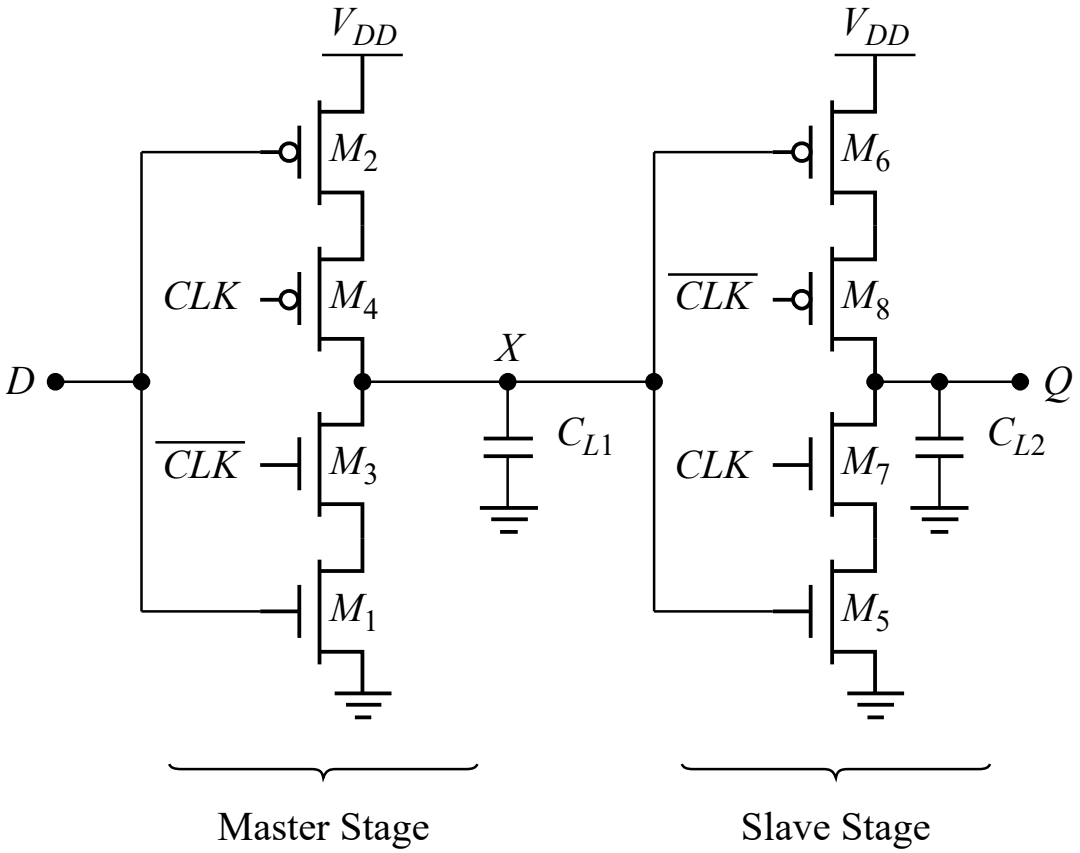
Setup/Hold Time Illustrations



Setup/Hold Time Illustrations

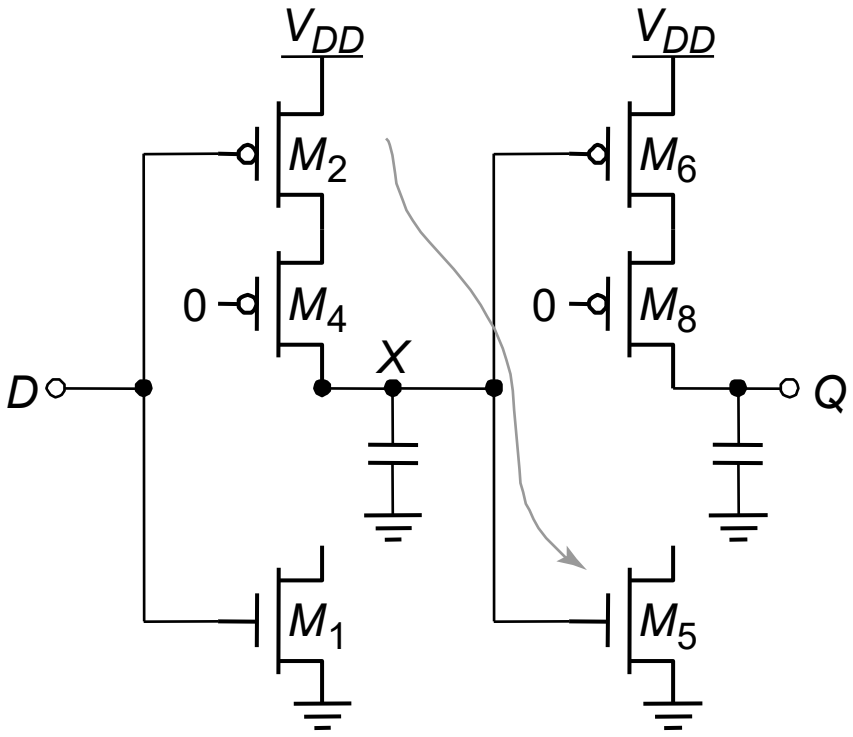


Other Latches/Registers: C²MOS

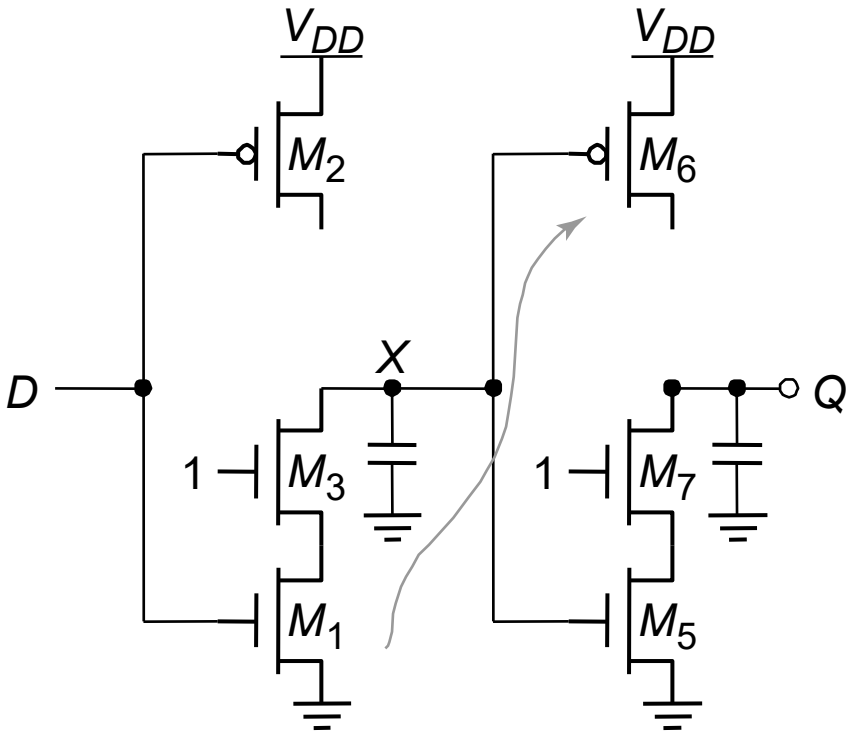


"Keepers" can be added to make circuit pseudo-static

Insensitive to Clock-Overlap

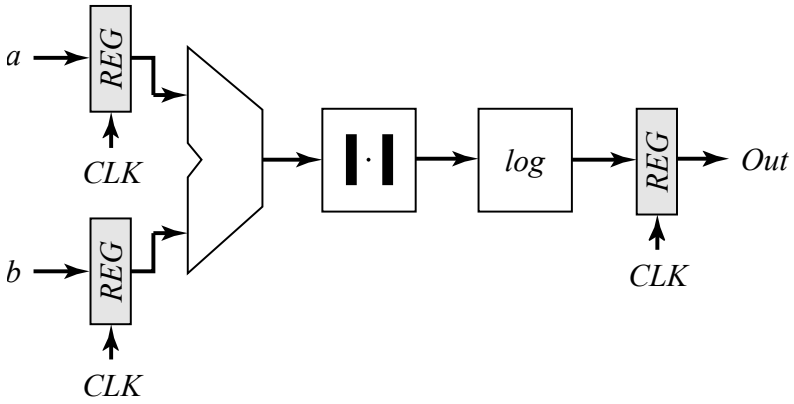


(a) (0-0) overlap

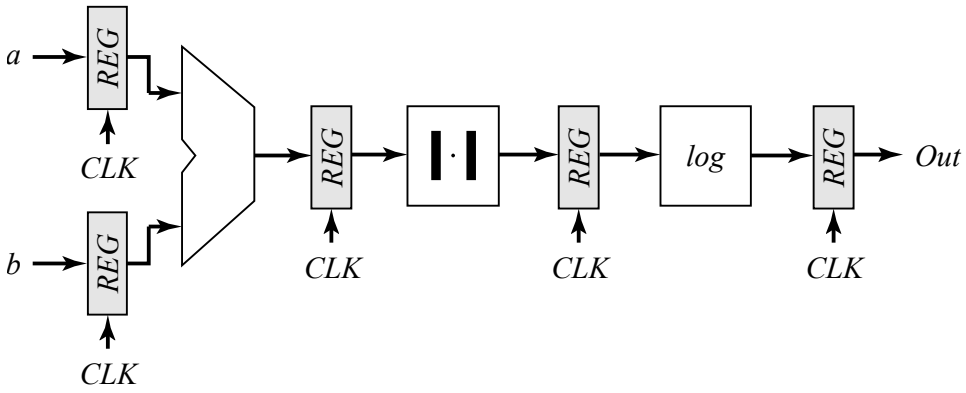


(b) (1-1) overlap

Pipelining



Reference



Pipelined

Clock Period	Adder	Absolute Value	Logarithm
1	$a_1 + b_1$		
2	$a_2 + b_2$	$\lvert a_1 + b_1 \rvert$	
3	$a_3 + b_3$	$\lvert a_2 + b_2 \rvert$	$\log(\lvert a_1 + b_1 \rvert)$
4	$a_4 + b_4$	$\lvert a_3 + b_3 \rvert$	$\log(\lvert a_2 + b_2 \rvert)$
5	$a_5 + b_5$	$\lvert a_4 + b_4 \rvert$	$\log(\lvert a_3 + b_3 \rvert)$