EE714 Final Exam (2019 Fall)

(105)

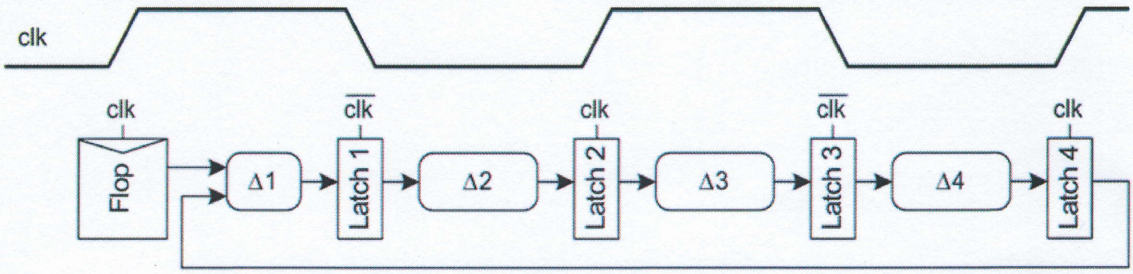
15:00 ~ 16:30, 17/12/2019, Prof. Jinsang Kim

1. (12pts) Design an asymmetric and high-skewed two input NAND gate at which the logical effort of a critical input can approaches 1.
NAND gate ckt: (2) asym: (3) HS: (3) logical Effort: (4)
2. (15pts) Design a domino two input NAND gate including the size information of all transistors. Also, compute the logical efforts of both inputs. The gate should not have any side effects as possible.
Domino NAND (dual rail) ckt: (5) Sizes: (3) LEs: (4) side effects: (3)

Use the following parameters for the following two questions.

	setup time	clk-to-Q delay	D-to-Q delay	contamination delay	hold time	clock skew
FF	65 ps	50 ps	n/a	35 ps	30 ps	50 ps
latches	25 ps	50 ps	40 ps	35 ps	30 ps	50 ps

3. (15pts) For each of the following sequencing styles, determine the maximum logic propagation delay within 600 ps clock cycle (or half-cycle, for two-phase latches).
a) FFs (8)
b) two-phase transparent latches with 60ps of nonoverlap between phases (7)
4. (15pts) For the path in the following figure, determine which latches borrow time and if any setup time violations occur. Repeat for cycle times of 1400 and 700 ps. Assume that the latch delays are accounted for in the propagation delay $\Delta's$
a) $\Delta 1 = 550\,ps; \Delta 2 = 480\,ps; \Delta 3 = 350\,ps; \Delta 4 = 200\,ps;$ (4) (+1)
b) $\Delta 1 = 200\,ps; \Delta 2 = 500\,ps; \Delta 3 = 300\,ps; \Delta 4 = 450\,ps;$ (3)



5. (18pts) Draw both a transistor-level SRAM cell including both column conditioning and sense amplifier circuits. Also, draw the waveforms of write of '1' when the cell stores '0'. Discuss the sizes of all transistors at the SRAM cell as well.
ckt: cell (4) column (2) SA (2) write: (6) size: (4)
6. (12pts) Try to show mathematically why a transistor of flash memory can have different threshold values.
transistor cap. model: (4) equations: (8)
7. (18pts) Draw the architecture of a PLL, and express it at S domain including the transfer function. Also, draw the corresponding circuits.
Architecture: (5) T(s): (5) ckts: (8)

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