VLSI Systems Designs: Home Work #1 (2019 Fall)

Upload at KLAS, Due **10/23/2019,** Prof. Jinsang Kim

Assume that a matched unit inverter has widths of 45nm for nMOS and 90nm for pMOS, respectively. Assume that the 45nm process technology uses the followings unless stated otherwise:

$V_{DD} = 1\,V,\ Vto = 0.3\,V, \beta_n = 1mA/\,V^2, \Phi_s = 0.6\,V, \gamma = 0.3\,V^{0.5}, \lambda = 0.02, \tau = 3RC = 0.5ps$

1. (10pts) Explain why the mobility of electron is larger than that of hole using effective mass. Also explain Fermi function and its level.

2. (15pts) Summarize the photolithography device fabrication technology from bare wafer, oxidation, photo processing, etching, deposition, to packaging. Also, you should enumerate the corresponding equipments at each stage.

3. (20pts) Given a 2-input CMOS NOR gate using non-ideal transistors,
   a) calculate the discharging current when the initial output is V_{DD} and one of the input signal is 0.7V and the other is 0V (8pts).
   b) calculate the I_{ds} current of pMOS transistor connected to the NOR gate output terminal when the 0V is applied to the input gate and V_{DD} is applied to the other input gate. Assume that V_s of the pMOS are 0.5V and the NOR gate output is 0.1V (12pts).

4. (15pts) Explain the mechanism or physics of the following nonideal MOSFET behaviors.
   a) DIBL
   b) GIDL
   c) Subthreshold leakage

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