HSPICE LAB (VLSI Systems Design: 2018 Spring) (100pts)

Due: 11:59 PM, 04/22/2017 (upload to KLAS website) Prof. Jinsang Kim

1. (30 pts) Simulate and layout a two-input NOR gate. Also, run corner simulations and measure propagation delays and contamination delays.

   30 pts: simulation (5), corner (5), layout (15) Analysis&Comments (5)

2.

   a) (50 pts) Simulate and layout a CMOS D Flip-Flop. Also, try to analyze the setup time and the hold time.

   50 pts: simulation (5) & layout (30), setup & hold time (10), Analysis&Comments (5)

   b) (20 pts) Simulate a back-to-back CMOS D Flip-Flop circuit in case there is clock skew. Also, try to show the race condition and measure the hold time. Also, add the above two-input NOR gate between the two FFs and show the race condition can be solved.

   20 pts: simulation (5), hold time & race condtion (10), Analysis&Comments (5)