Introduction to CMOS VLSI Design

Lecture 5: SPICE Simulation

Outline

- Introduction to SPICE
- DC Analysis
- Transient Analysis
- Subcircuits
- Optimization
- Power Measurement
- Logical Effort Characterization

Introduction to SPICE

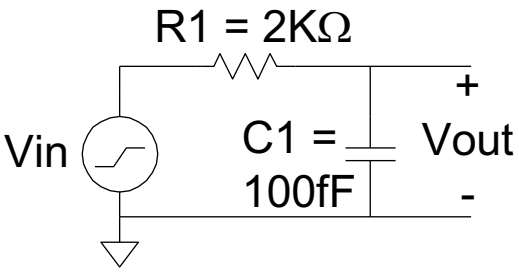
- **S**imulation **P**rogram with **I**ntegrated **C**ircuit **E**mphasis
  - Developed in 1970's at Berkeley
  - Many commercial versions are available
  - HSPICE is a robust industry standard
    - Has many enhancements that we will use
- Written in FORTRAN for punch-card machines
  - Circuits elements are called *cards*
  - Complete description is called a SPICE *deck*

Writing Spice Decks

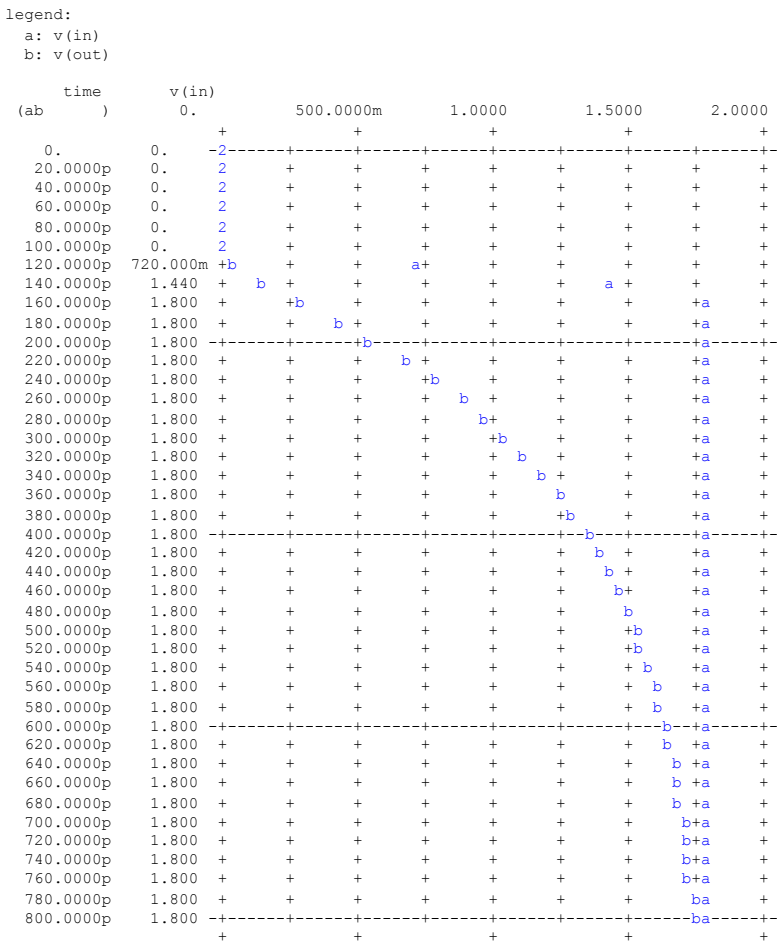
- Writing a SPICE deck is like writing a good program
  - Plan: sketch schematic on paper or in editor
    - Modify existing decks whenever possible
  - Code: strive for clarity
    - Start with name, email, date, purpose
    - Generously comment
  - Test:
    - Predict what results should be
    - Compare with actual
    - *Garbage In, Garbage Out!*

Example: RC Circuit

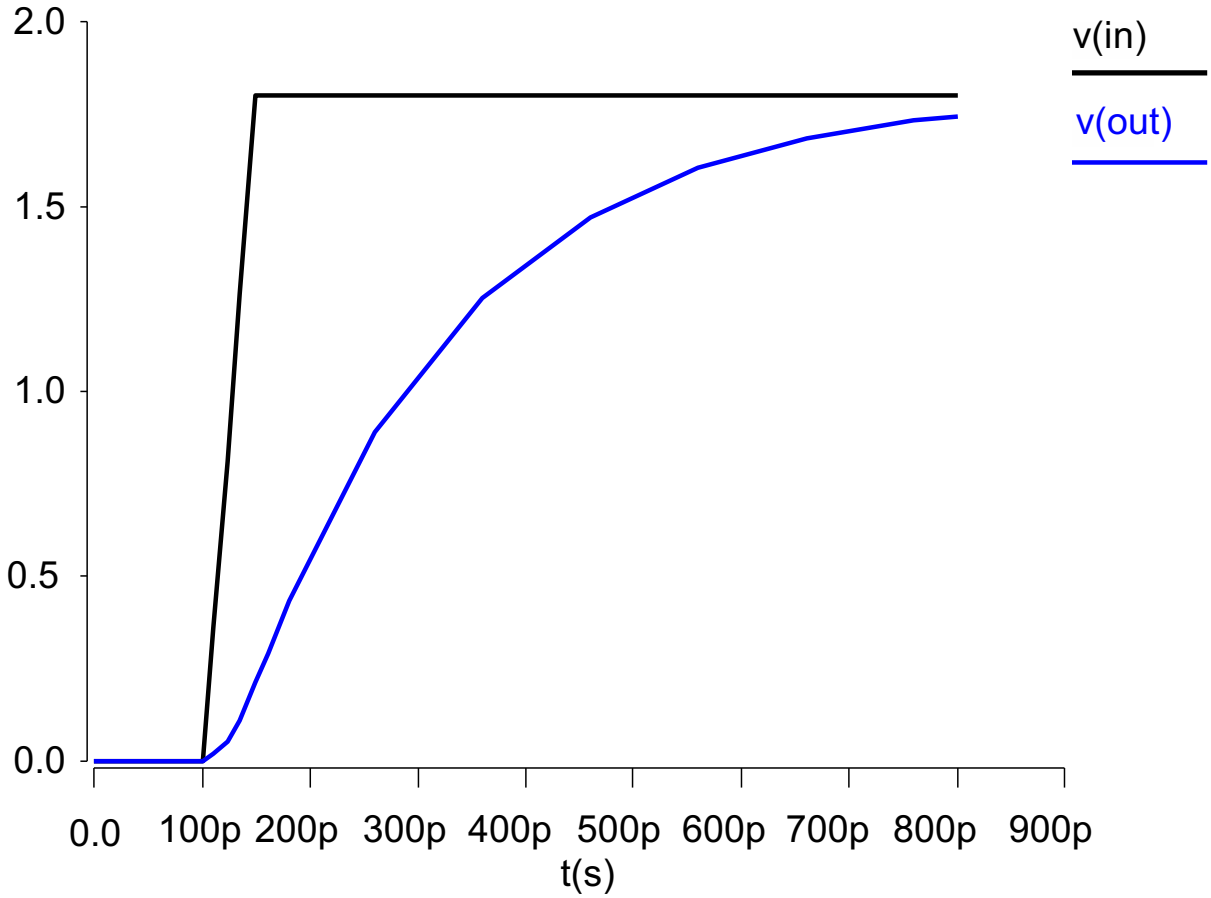
```
* rc.sp
* David_Harris@hmc.edu 2/2/03
* Find the response of RC circuit to rising input

*-------------------------------------------------
* Parameters and models
*-------------------------------------------------
.option post

*-------------------------------------------------
* Simulation netlist
*-------------------------------------------------
Vin      in       gnd      pwl      0ps 0 100ps 0 150ps 1.8 800ps 1.8
R1       in       out      2k
C1       out      gnd      100f

*-------------------------------------------------
* Stimulus
*-------------------------------------------------
.tran 20ps 800ps
.plot v(in) v(out)
.end
```



Result (Textual)



Result (Graphical)



Sources

- *DC* Source

```
Vdd vdd gnd 2.5
```

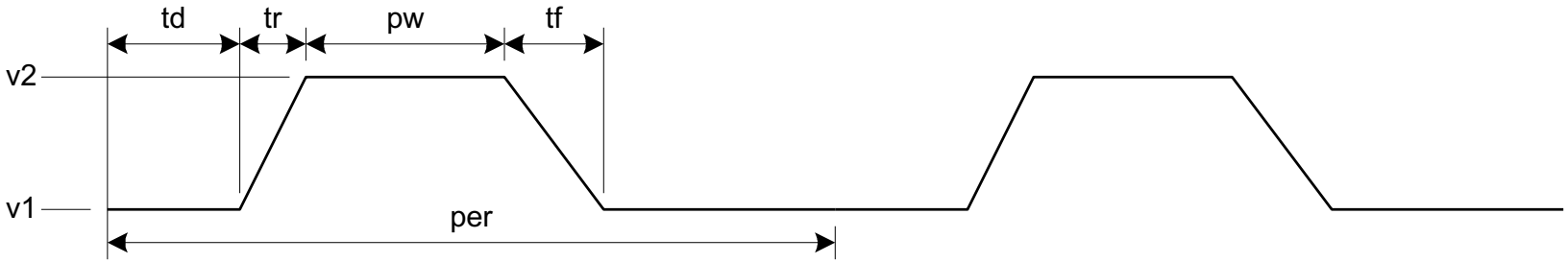
- *Piecewise Linear* Source

```
Vin in gnd pwl 0ps 0 100ps 0 150ps 1.8 800ps 1.8
```

- *Pulsed* Source

```
Vck clk gnd PULSE 0 1.8 0ps 100ps 100ps 300ps 800ps
```

PULSE v1 v2 td tr tf pw per



SPICE Elements

Letter	Element
R	Resistor
C	Capacitor
L	Inductor
K	Mutual Inductor
V	Independent voltage source
I	Independent current source
M	MOSFET
D	Diode
Q	Bipolar transistor
W	Lossy transmission line
X	Subcircuit
E	Voltage-controlled voltage source
G	Voltage-controlled current source
H	Current-controlled voltage source
F	Current-controlled current source

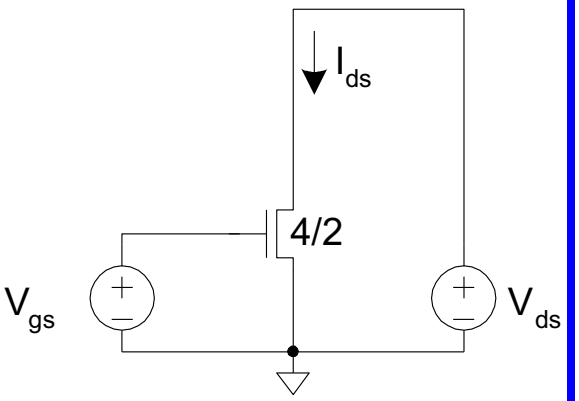
Units

Letter	Unit	Magnitude
a	atto	10^{-18}
f	fempto	10^{-15}
p	pico	10^{-12}
n	nano	10^{-9}
u	micro	10^{-6}
m	mili	10^{-3}
k	kilo	10^{3}
x	mega	10^{6}
g	giga	10^{9}

Ex: 100 femptofarad capacitor = 100fF, 100f, 100e-15

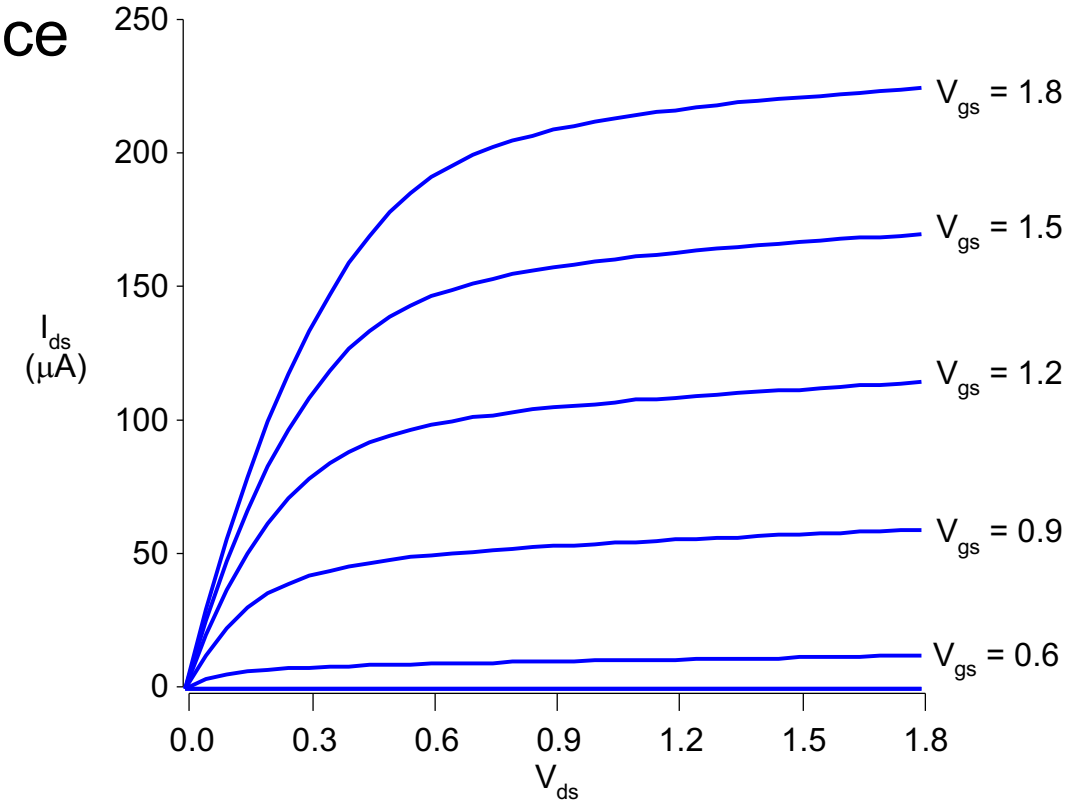
DC Analysis

```
* mosiv.sp

*-------------------------------------------------
* Parameters and models
*-------------------------------------------------
.include '../models/tsmc180/models.sp'
.temp 70
.option post

*-------------------------------------------------
* Simulation netlist
*-------------------------------------------------
*nmos
Vgs       g         gnd       0
Vds       d         gnd       0
M1        d         g         gnd       gnd       NMOS      W=0.36u  L=0.18u

*-------------------------------------------------
* Stimulus
*-------------------------------------------------
.dc Vds 0 1.8 0.05 SWEEP Vgs 0 1.8 0.3
.end
```



I-V Characteristics

- nMOS I-V
  - V_{gs} dependence
  - Saturation



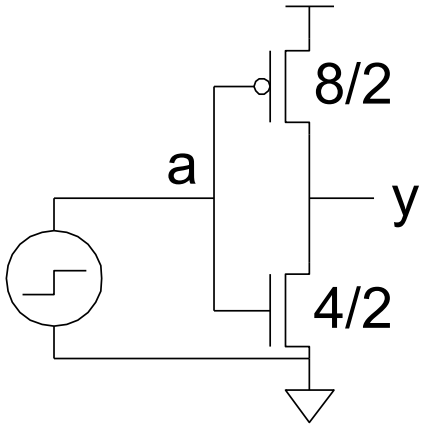
MOSFET Elements

M element for MOSFET

```
Mname drain gate source body type
+ W=<width> L=<length>
+ AS=<area source> AD = <area drain>
+ PS=<perimeter source> PD=<perimeter drain>
```

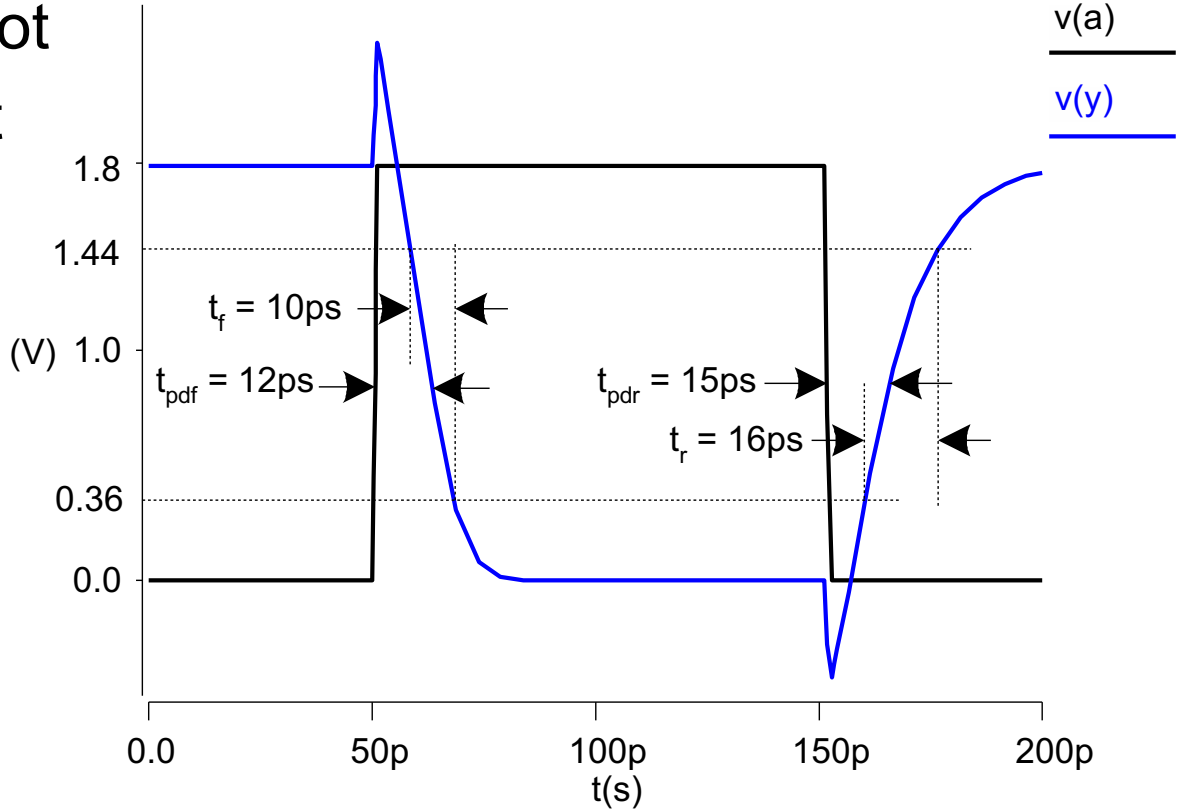
Transient Analysis

```
* inv.sp

* Parameters and models
*-----------------------------------------------
.param SUPPLY=1.8
.option scale=90n
.include '../models/tsmc180/models.sp'
.temp 70
.option post

* Simulation netlist
*-----------------------------------------------
Vdd      vdd      gnd      'SUPPLY'
Vin      a        gnd      PULSE    0 'SUPPLY' 50ps 0ps 0ps 100ps 200ps
M1       y        a        gnd      gnd      NMOS     W=4      L=2
+ AS=20 PS=18 AD=20 PD=18
M2       y        a        vdd      vdd      PMOS     W=8      L=2
+ AS=40 PS=26 AD=40 PD=26

* Stimulus
*-----------------------------------------------
.tran 1ps 200ps
.end
```



Transient Results

- Unloaded inverter
  - Overshoot
  - Very fast edges

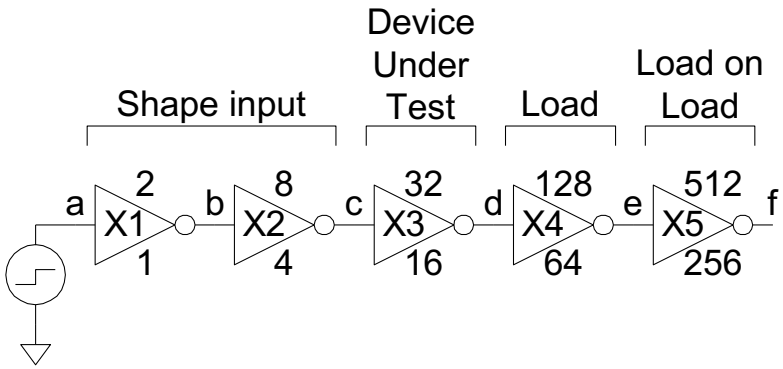


Subcircuits

- Declare common elements as subcircuits

```
.subckt inv a y N=4 P=8
M1 y a gnd gnd NMOS W='N' L=2
+ AS='N*5' PS='2*N+10' AD='N*5' PD='2*N+10'
M2 y a vdd vdd PMOS W='P' L=2
+ AS='P*5' PS='2*P+10' AD='P*5' PD='2*P+10'
.ends
```

- Ex: Fanout-of-4 Inverter Delay
  - Reuse inv
  - Shaping
  - Loading



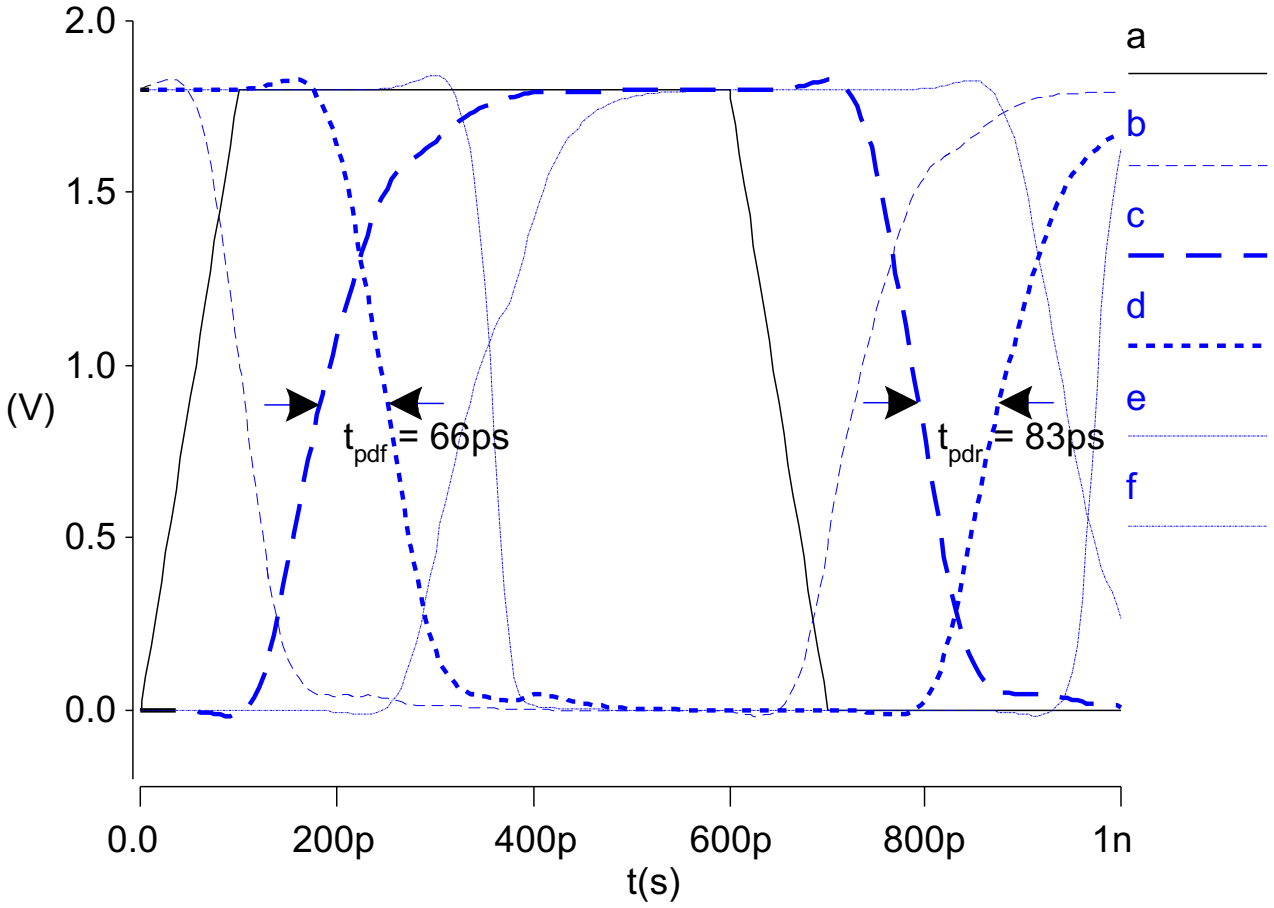
FO4 Inverter Delay

```
* fo4.sp

* Parameters and models
*-----------------------------------------------------------------
.param SUPPLY=1.8
.param H=4
.option scale=90n
.include '../models/tsmc180/models.sp'
.temp 70
.option post

* Subcircuits
*-----------------------------------------------------------------
.global vdd gnd
.include '../lib/inv.sp'

* Simulation netlist
*-----------------------------------------------------------------
Vdd      vdd      gnd      'SUPPLY'
Vin      a        gnd      PULSE    0 'SUPPLY' 0ps 100ps 100ps 500ps 1000ps
X1       a        b        inv                 * shape input waveform
X2       b        c        inv      M='H'      * reshape input waveform
```

FO4 Inverter Delay Cont.

```
X3      c       d       inv     M='H**2' * device under test
X4      d       e       inv     M='H**3' * load
x5      e       f       inv     M='H**4' * load on load

* Stimulus
*-------------------------------------------------------------------
.tran 1ps 1000ps
.measure tpdr                                   * rising prop delay
+     TRIG v(c)  VAL='SUPPLY/2' FALL=1
+     TARG v(d)  VAL='SUPPLY/2' RISE=1
.measure tpdf                                   * falling prop delay
+     TRIG v(c)  VAL='SUPPLY/2' RISE=1
+     TARG v(d)  VAL='SUPPLY/2' FALL=1
.measure tpd param='(tpdr+tpdf)/2'               * average prop delay
.measure trise                                          * rise time
+       TRIG v(d)       VAL='0.2*SUPPLY' RISE=1
+       TARG v(d)       VAL='0.8*SUPPLY' RISE=1
.measure tfall                                          * fall time
+       TRIG v(d)       VAL='0.8*SUPPLY' FALL=1
+       TARG v(d)       VAL='0.2*SUPPLY' FALL=1
.end
```

FO4 Results


2.0
1.5
1.0
0.5
0.0
(V)
a
b
c
d
e
f
t_{pdf} = 66ps
t_{pdr} = 83ps
0.0
200p
400p
600p
800p
1n
t(s)

Optimization

- HSPICE can automatically adjust parameters
  - Seek value that optimizes some measurement
- Example: Best P/N ratio
  - We've assumed 2:1 gives equal rise/fall delays
  - But we see rise is actually slower than fall
  - What P/N ratio gives equal delays?
- Strategies
  - (1) run a bunch of sims with different P size
  - (2) let HSPICE optimizer do it for us

P/N Optimization

```
* fo4opt.sp

* Parameters and models
*-----------------------------------------------------------------------
.param SUPPLY=1.8
.option scale=90n
.include '../models/tsmc180/models.sp'
.temp 70
.option post

* Subcircuits
*-----------------------------------------------------------------------
.global vdd gnd
.include '../lib/inv.sp'

* Simulation netlist
*-----------------------------------------------------------------------
Vdd      vdd      gnd      'SUPPLY'
Vin      a        gnd      PULSE    0 'SUPPLY' 0ps 100ps 100ps 500ps 1000ps
X1       a        b        inv      P='P1'             * shape input waveform
X2       b        c        inv      P='P1'   M=4      * reshape input
X3       c        d        inv      P='P1'   M=16     * device under test
```

P/N Optimization

```
X4       d        e        inv      P='P1'   M=64     * load
X5       e        f        inv      P='P1'   M=256    * load on load

* Optimization setup
*-----------------------------------------------------------------------
.param P1=optrange(8,4,16)                    * search from 4 to 16, guess 8
.model optmod opt itropt=30                   * maximum of 30 iterations
.measure bestratio param='P1/4'               * compute best P/N ratio

* Stimulus
*-----------------------------------------------------------------------
.tran 1ps 1000ps SWEEP OPTIMIZE=optrange RESULTS=diff MODEL=optmod
.measure tpdr                                 * rising propagation delay
+       TRIG v(c) VAL='SUPPLY/2' FALL=1
+       TARG v(d)         VAL='SUPPLY/2' RISE=1
.measure tpdf                                 * falling propagation delay
+       TRIG v(c)         VAL='SUPPLY/2' RISE=1
+       TARG v(d)         VAL='SUPPLY/2' FALL=1
.measure tpd param='(tpdr+tpdf)/2' goal=0     * average prop delay
.measure diff param='tpdr-tpdf' goal = 0      * diff between delays
.end
```

P/N Results

- P/N ratio for equal delay is 3.6:1
  - $t_{pd} = t_{pdr} = t_{pdf} = 84$ ps (slower than 2:1 ratio)
  - Big pMOS transistors waste power too
  - Seldom design for exactly equal delays
- What ratio gives lowest average delay?

```
.tran 1ps 1000ps SWEEP OPTIMIZE=optrange RESULTS=tpd MODEL=optmod
```

  - P/N ratio of 1.4:1
  - $t_{pdr} = 87$ ps, $t_{pdf} = 59$ ps, $t_{pd} = 73$ ps

Power Measurement

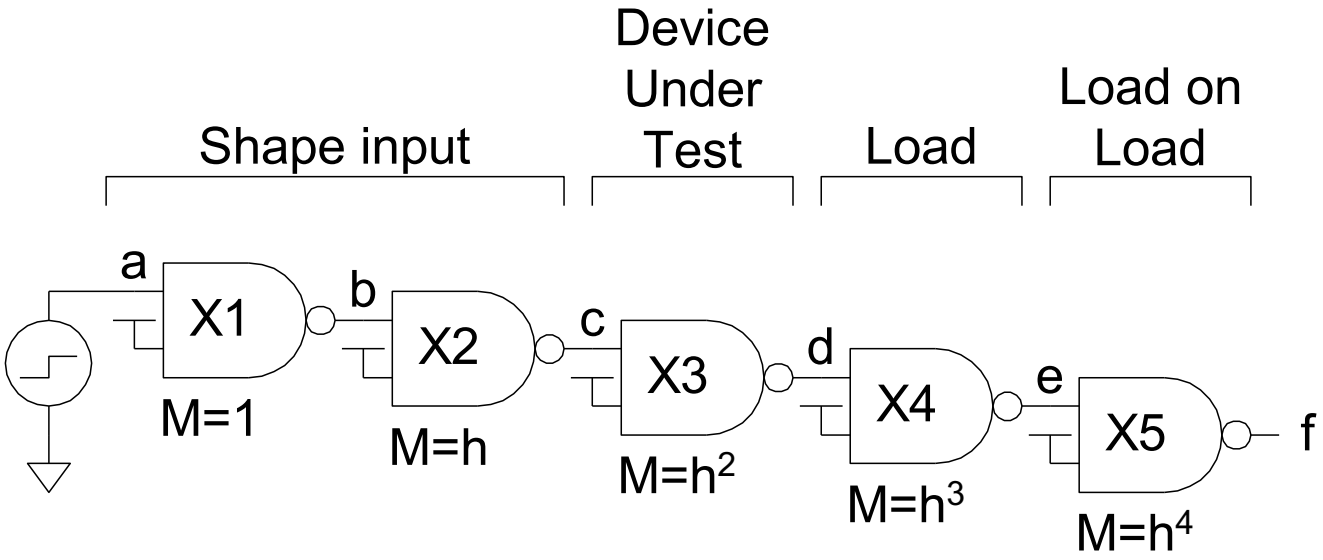
- HSPICE can measure power
  - Instantaneous P(t)
  - Or average P over some interval

```
.print P(vdd)
.measure pwr AVG P(vdd) FROM=0ns TO=10ns
```

- Power in single gate
  - Connect to separate V_{DD} supply
  - Be careful about input power

Logical Effort

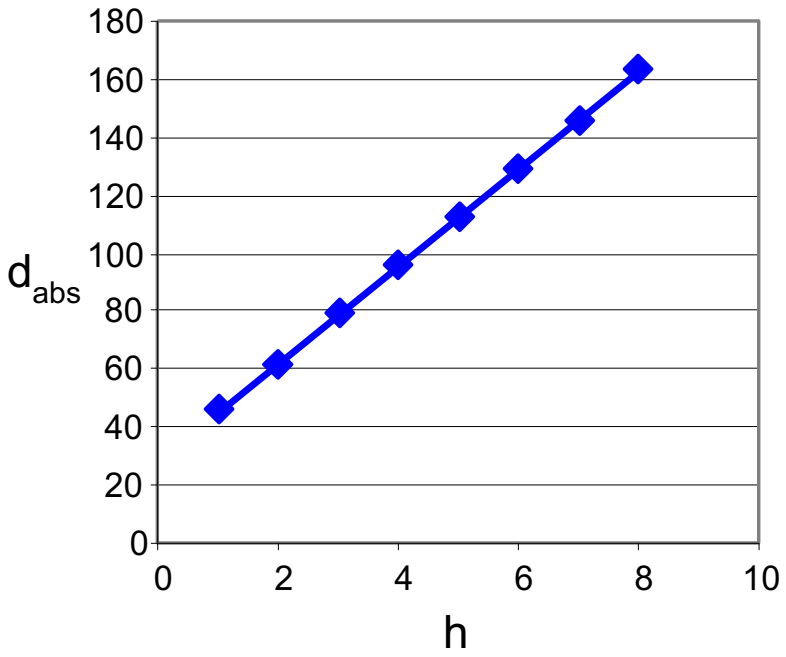
- Logical effort can be measured from simulation
  - As with FO4 inverter, shape input, load output



Logical Effort Plots

- Plot t_{pd} vs. h
  - Normalize by τ
  - y-intercept is parasitic delay
  - Slope is logical effort
- Delay fits straight line very well in any process as long as input slope is consistent

τ = 15 ps



Logical Effort Data

- For NAND gates in TSMC 180 nm process:

# of inputs	Input	Rising Logical Effort g_u	Falling Logical Effort g_u	Average Logical Effort g	Rising Parasitic Delay p_u	Falling Parasitic Delay p_d	Average Parasitic Delay p
2	*A*	1.45	0.82	**1.14**	2.37	1.42	**1.90**
	B	1.36	0.97	**1.17**	1.60	1.22	**1.41**
3	*A*	1.82	0.80	**1.31**	4.90	2.11	**3.51**
	B	1.73	0.95	**1.34**	3.94	1.86	**2.90**
	C	1.63	1.10	**1.36**	2.60	1.54	**2.07**
4	*A*	1.96	0.89	**1.42**	6.54	3.08	**4.81**
	B	1.86	1.02	**1.44**	5.71	2.84	**4.28**
	C	1.80	1.14	**1.47**	4.69	2.42	**3.56**
	D	1.71	1.28	**1.49**	3.26	1.97	**2.62**

- Notes:
  - Parasitic delay is greater for outer input
  - Average logical effort is better than estimated

Comparison

Vendor		Orbit	AMI	HP	HP	AMI	AMI	TSMC	TSMC	TSMC	TSMC
Model		MOSIS	MOSIS	MOSIS	MOSIS	MOSIS	MOSIS	MOSIS	MOSIS	MOSIS	TSMC
Feature Size f	nm	2000	1600	800	800	600	600	350	250	180	180
V_{DD}	V	5	5	5	3.3	5	3.3	3.3	2.5	1.8	1.8
FO4 inv delay	ps	856	717	297	427	230	312	210	153	99.4	75.6
τ	ps	170	143	59	84	45	60	40	30	20	15
Logical Effort											
Inverter		1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00
NAND2		1.13	1.07	1.07	1.09	1.05	1.08	1.12	1.12	1.17	1.14
NAND3		1.32	1.22	1.21	1.25	1.19	1.24	1.29	1.29	1.36	1.31
NAND4		1.48	1.35	1.33	1.37	1.33	1.38	1.44	1.43	1.49	1.42
NOR2		1.57	1.62	1.59	1.58	1.58	1.60	1.52	1.50	1.46	1.50
NOR3		2.16	2.32	2.23	2.23	2.23	2.30	2.07	2.02	1.94	2.00
NOR4		2.55	2.7	2.61	2.64	2.57	2.68	2.46	2.37	2.27	2.38
Parasitic Delay											
Inverter		1.08	1.05	1.05	1.13	1.18	1.25	1.33	1.18	0.95	1.03
NAND2		1.87	1.79	1.85	2.05	1.92	2.10	2.28	2.07	1.74	1.90
NAND3		3.34	3.22	3.30	3.75	3.40	3.79	4.15	3.65	3.08	3.51
NAND4		4.64	4.42	4.54	5.12	4.70	5.23	5.75	5.01	4.26	4.81
NOR2		2.86	2.97	2.91	3.13	3.29	3.56	3.52	2.95	2.41	2.85
NOR3		5.65	6.22	6.05	6.47	7.02	7.70	6.89	5.61	4.49	5.57
NOR4		7.92	8.71	8.48	9.14	9.68	10.67	9.71	7.93	6.38	7.98