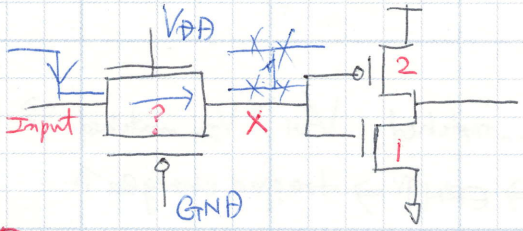
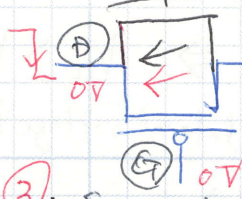
VLSI Systems Design Quiz (2017 Fall)

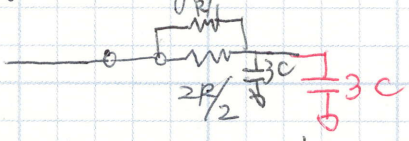
1. (15)



(10)
(a) T-gate current after this transit. (right)



(b) (5) assume the size of pMOS and nMOS at the T-gate is 2R and R



delay = $\frac{2R}{2} \cdot 3C \cdot \frac{1}{2} = 3RC$

= ~~0.5~~ ps

1.0 ps

(3) - Source is V_{DD} → No body effect

(4) - operation region: $V_{gs} < V_{ds} - V_{tp}$

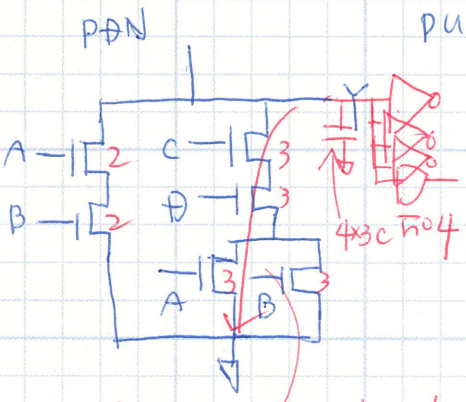
$-V_{DD} \quad -V_{DD} - 0.3$

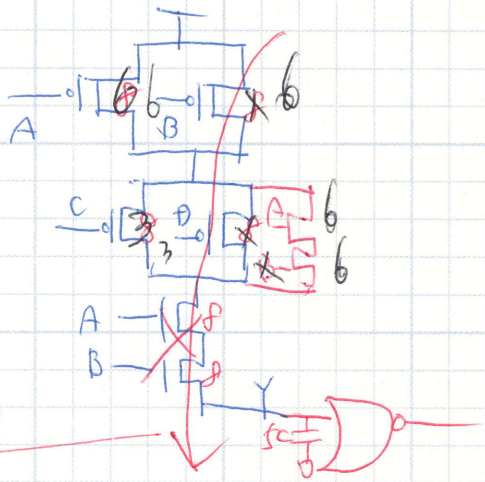
∴ Saturation region

(3) - $I_{dsp} = \frac{\beta}{2}(V_{gsp} - V_{tp})(1 + \lambda V_{dsp})$

* same as I_{dsn} → $I = 2 \cdot |I_{dsp}|$

2. a) b) (6) (6)





c) (9) layout (smaller contacts, taps)

d) (7) load = 5C, unit: time

e) (7) load = 4x3C, unit: time

f) (5) (2+3+3+2)C

3. (15) Vt shifts by (a) body effect
(b) PBTI
(c) GIDL
(d) NBTI
(e) Hot electrons
(f) short channel effect
⋮

(15) = x3 at least 5 including causes + phenomenon + re

4 ① F, high k ⇒ tox↑ ⇒ leakage current↓ (~~independs on~~)

② T, effective channel length↑ ⇒ leakage↓↓

③ F, trapped charge↑ ⇒ Vt↑

④ F, $\beta_P > \beta_N$ ⇒ $V_{IL} > V_{IL\_matched}$, $V_{IH} > V_{IH\_matched}$ ⇒ $NM_H < NM_L$

⑤ F, Vds↑ ⇒ lateral voltage↑ ⇒ EPH↑ ⇒ trapped charges↑

⑥ T, Latchup↑ ⇐ currents in the silicon body↑