EE 714 Digital IC Design Term Project

2020, Fall

Prof. Jinsang Kim

In this project, we design a digital IC chip using standard cell-based front-end and back-end Synopsys CAD tools. The CAD manuals can be downloaded from the e-campus classs website. You may use existing Verilog codes at your lab or write them by yourself. **But you should understand all the codes and cannot use Verilog codes used for previous MPW projects or projects done in the previous classes.**

1. For this project, each group consists of maximum two student. The minimum design complexity is 40K gates/student.
2. The following should be included, but not limited
   A. Should explain the algorithm of your design and draw the functional block diagram.
   B. Do RTL synthesis and analyze performances such as the number of gates, timing and power consumption.
   C. Do floorplaning the chip and P&R and add IO pads.
   D. Write the report, present, and demonstrate your design including
      i. Algorithm & architecture
      ii. Verilog HDL codes
      iii. Your design methodology from the front-end to back-end
      iv. Experimental results and analysis at every step
      v. Datasheet of your design
   E. Each student should show me that he/she knows all the steps for this design.
   F. A sample FFT Verilog code will be given so that you can exercise all the details steps.
3. Important dates: upload at KLAS website
   A. 11/10/2020: design proposal (team leader only)
   B. 11/24/2020: exercise report using the sample FFT codes (all the students, individual report). ←
   C. 12/01/2020: intermediate report (team leader only) of the front-end design.
   D. 12/15/2019: Submit the final report and all sources (zipped) by email.
   E. 12/15/2019: demo and final presentation & Final Exam