# VLSI Systems Designs: Quiz1 (2016 Fall)

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*Assume that a matched unit inverter has widths of 45nm for nMOS and 90nm for pMOS, respectively. Assume that the 45nm process technology uses the followings unless stated otherwise:*

$V_{DD} = 1\,V,\ Vto = 0.3\,V, \beta_n = 1mA/\,V^2, \Phi_s = 0.6\,V, \gamma = 0.3\,V^{0.5}, \lambda = 0.02, \tau = 3RC = 0.5ps$

1. **(47pts)** Given a boolean equation of $\overline{Y}$= (ABC+D)EF,
   a) draw a transistor-level CMOS circuit diagram (6pts)
   b) determine the size of all transistors (6pts)
   d) layout the circuit (ignore design rule) (10pts)
   c) estimate the rising propagation delay when the load is the 4 matched inverter (7pts).
   d) estimate the falling contamination delay when the load is the 4 matched inverter (7pts).
   e) compute the logical efforts of the signal A, D and E. (6pts).
   f) compute the parasitic effort of the circuit (5pts)

2. **(20pts)** Given a 2-input NOR gate using non-ideal transistors,
   a) calculate the discharging current when the initial output is $V_{DD}$ and one of the input signal is 0.7V and the other is 0V (8pts).
   b) calculate the $I_{ds}$ current of pMOS transistor connected to the NOR gate output terminal when the 0V is applied to the input gate and $V_{DD}$ is applied to the other input gate. Assume that $V_s$ of the pMOS are 0.5V and the NOR gate output is 0.1V (12pts).

3. **(13pts)** Determine the minimum number of inverters between FFs in order to prevent the race condition of the back-to-back FFs. Assume that the clock skew is 1.3ps.

4. (20pts) If the following description is correct, answer TRUE. Otherwise, answer FALSE. You should briefly add your reason. Deduct the point if the reason is not correct (each 4 pts).
   ① As n-type dopants density is increased by adding As on pure silicon, the resistance of the n-type material is decreased.
   ② Cascading drain(source) to drain(source) terminals in the pass transistor circuit is worse than the cascading drain(source) to gate terminal in terms of voltage drop.
   ③ Subshreshold leakage is decreased when the hot electron aging occurs.
   ④ Process corner of 'F' should be checked for temperature behavior of circuits.
   ⑤ The substrate leakage current at the drain of a transistor is larger than that at the source when the electrons are hot near the drain. -- END --