EE714 VLSI Systems Designs Quiz #1 (2020 Fall)

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1. (15pts) Calculate the current of the bottom pMOS transistor of 2-input gate when the output voltage is 0.7V

ANS: To begin with, output voltage is neither full V_{DD} (High=1) nor full GND (Low=0), so it means that the current is flowing, and at least two of pMOS transistors (serial) and one of nMOS transistors are not cut off (parallel)

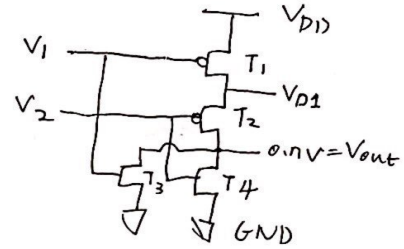
Consequently, we can make two assumptions

1. $V_{ds}>0$, $|V_{sd}|>0$
2. $V_{gs}>V_{to}$, $V_{sg}>|V_{to}|$

From assumption 1, we can set

$V_{out} < V_{D1} < V_{DD} \Rightarrow 0.1V < V_{D1} < 1V$

(all of the bodies is connected to its source)



[Fig 1. 2-input NOR Gate)

With considering the truth table of 2-input NOR gate, the two cases in the given situation can be existed : one or both nMOS transistors are on-state.

:) one nMOS transistor is on-state

assume that $V_1>0V$, $V_2=0V$, all of currents flows through T_3 (∵ KCL)
Thus, the current of the bottom pMOS transistor is equal to T_3's current.

assume that T_1 is on saturation region.

T_1 :

$V_{sg} = V_{DD}-V_1 > |V_{to}| = 0.3V \Rightarrow V_1 < 0.1V$

$V_{sd} = V_{DD}-V_{D1} > V_{DD}-V_1-|V_{to}| \Rightarrow V_1+0.3V > V_{D1}$

T_2 :

$V_{sg} = V_{D1}-V_2 > |V_{to}| = 0.3V \Rightarrow V_{D1} > 0.3V$

assume Sat

$V_{sd} = V_{D1}-0.1V > V_{D1}-V_2-|V_{to}| \Rightarrow V_{D1}-0.1V > V_{D1}-0.3$ (X)

∴ T_2 is linear

$V_{sd} = V_{D1}-0.1V < V_{D1}-V_2-|V_{to}| \Rightarrow V_{D1}-0.1V < V_{D1}-0.3V$

T_3 :

$V_{gs} = V_1 > V_{to} = 0.3V$

assume ~~sat~~ linear (X) (T_1 off)

$V_{ds} = 0.1V \not> V_{gs}-V_{to} \Rightarrow V_1 > 1V$ (contradict with that all of pMOS transistors is on-state)

∴ T_3 is saturation

$V_{ds} = 0.1V > V_{gs}-V_{to} \Rightarrow V_1 < 1V$

To sum up,

$0.3V < V_1 < 0.4V \rightarrow$ T_1 linear, T_2 linear, T_3 saturation, T_4 cut-off

$0.4V < V_1 < 0.1V \rightarrow$ T_1 saturation, T_2 linear, T_3 saturation, T_4 cut-off

Regardless of T_1's region, the amount of current is equivalent to nMOS (T_3)'s current (KCL)

$I = \frac{\beta_n}{2}(V_1-V_{to})^2(1+\lambda V_{out})$ $(0.3V < V_1 < 0.4V)$

∴ $0 < I < 0.0311 2mA$

!!) both of nMOS transistors are in on-state

assume that $V_1 = V_2$

T_1

$V_{sg} = V_{DD} - V_1 > 0.3V \Rightarrow V_1 < 0.7V$

assume sat (X)

$V_{sd} = V_{DD} - V_{D1} > V_{DD} - V_1 - 0.3V \Rightarrow V_1 + 0.3V > V_{D1}$

$\therefore T_1$ is linear region

$V_{sd} = V_{DD} - V_{D1} < V_{DD} - V_1 - 0.3V \Rightarrow V_1 + 0.3V < V_{D1}$

T_2

$V_{sg} = V_{D1} - V_2 = V_{D1} - V_1 > 0.3V \Rightarrow V_1 + 0.3V < V_{D1}$

contradiction

T_3, T_4

$V_1 = V_2 = V_{gs} > 0.3V \Rightarrow V_1 > 0.3V$

assume linear (X)

$V_{ds} = 0.1V < V_{gs} - V_{t0} \Rightarrow V_1, V_2 > 1V$ (T_1, T_2 off) (X)

$\therefore$ T_3, T_4 are saturation region

$V_1, V_2 < 1V$

To sum up,

$0.3V < V_1, V_2 < 0.4V$

T_1 linear
T_2 linear
T_3 saturation
T_4 saturation

Regardless of T_2's region, the amount of the current is equivalent to two nMOS transistors' current ($\because$ KCL) (T_3, T_4)

$0.4V < V_1, V_2 < 0.7V$

T_1 linear
T_2 saturation
T_3 saturation
T_4 saturation

$I = 2 \times \frac{\beta_n}{2} (V_1 - V_{t0})^2 (1 + \lambda V_{out}) \quad (0.3V < V_{1,2} < 0.4V)$

$0 < I < 0.16224\,mA$

$\therefore$ $0mA < I < 0.16224\,mA$

2. (15pts) Explain the 2nd order effects of MOSFETs.

As the technology scaling reaches channel lengths less than $1um$, second order effects, which include velocity saturation, threshold voltage variation, hot carrier effects, and other non-idealities, become important and have a negative impact on MOSFETs' performance, whereas long-channel, ideal, first order, or Shockley model had not taken an issue. With taking account of second order effect, I-V Curve do not follow that of the ideal, first order model.

3. (15pts) Explain the aging effects and their solutions of MOSFETs.

MOSFETs are age over time like humans, and this phenomenon is called "Aging". "Aging effects" are directly related to the reliability of MOSFETs. The reliability is dependent on a lot of factors, but "Fault" in physics domain is mainly considered when discussing "Aging". Aging is caused when the MOSFETs are subjected to electric stress, such as higher than normal voltage and temperature. Aging effects frequently are divided two sections: Semiconductors and Wires. Wires wearout, which is Electromigration and Self-heating, is also important in aging effects, however, I will only consider aging of MOSFETs.

The three issues that make transistor vulnerable are:

1) Hot Carrier Injection - As transistors switch the voltage fast enough, the electrons have high velocity and can embed themselves into the gate oxide, consequently become trapped there. The trapped carrier effects on threshold voltage, which yields reducing current in nMOS and it means that transistors become slower.

2) Negative Bias Temperature Instability (NBTI) - Having a static voltage applied across the oxide for a long enough time yields an increase in "traps", and it cause the slower transistor by increasing threshold voltage. Especially, with high temperature combined with a negative bias on a pMOS (Gate voltage is 0, and Source voltage is V_{DD}) the NBTI plays a crucial role in aging device.

3) Time-dependent dielectric breakdown (TDDB) - Gradual increase in gate leakage stress the oxide and lead to breakdown of MOSFETs subsequently. TDDB is dangerous since the breakdown can be caused by the prolonged exposure to moderate fields close to the regular operating voltage.

Actually, the solutions of three effects of aging should be separated to analog and digital, but I will only state the digital case due to the object of the class.

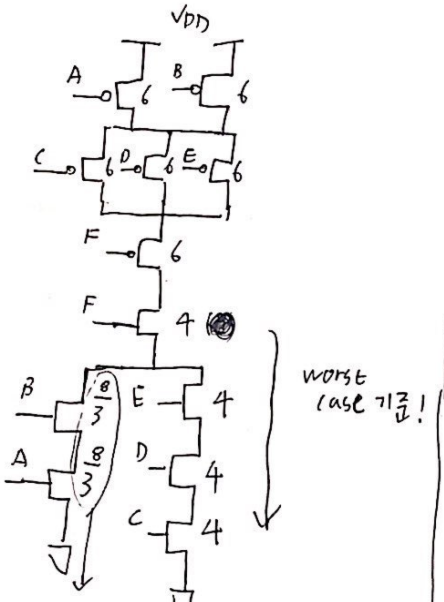
The aging effects are unavoidable, as the technology scaling reaches few nanometers, it cannot be prevented intentionally. Thus, the simplest solution is setting enough margin(timing slack) of devices with considering the degradation of speed. Or, using the digital characteristic that is that currents only flow for a very limited amount of time, make the long non-activity intervals until the next cycle of the clock. Lastly, with considering that applied electrical fields are main factor of aging, use the power gating to turn off the power supply during sleep(non-activity).

4. (40pts) Given $Y = \overline{(AB + CDE)F}$ (Complementary inputs are available.

a) draw a one-stage transistor-level CMOS circuit diagram
b) determine the size of all transistors
c) show the layout of this circuit
d) estimate the rising propagation delay when the load is a 2-input NOR gate. Explain the details of the delay components.
e) estimate the falling contamination delay when the load is a 2-input NOR gate. Explain the details of the delay components.

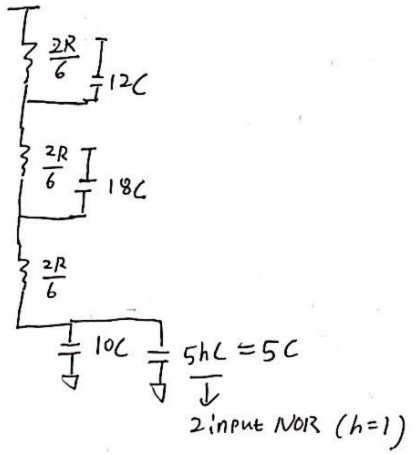
(a), (b)

$Y = \overline{(AB+CDE)F}$



(c)

(d) rising propagation delay



Elmore delay

$t_d = \sum_i R_i C_i$

C_i : each node i of the capacitance C_i on the node

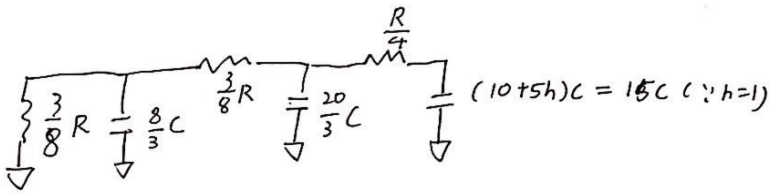
R_i : effective resistance on the shared path from the source to the node and the leaf

$t_{pdr} = (\frac{2R}{6})(12C) + (\frac{2R}{6}+\frac{2R}{6})(18C) + (\frac{2R}{6}+\frac{2R}{6}+\frac{2R}{6})\cdot(15C)$

$= 4RC + 12RC + 15RC$

$= 31RC \simeq 31ps$ ($\because 3RC = \tau = 3ps$)

(e) falling contamination delay



$t_{cdf} = (\frac{3}{8}R)(\frac{8}{3}C) + (\frac{3}{8}R+\frac{3}{8}R)(\frac{20}{3}C) + (\frac{3}{8}R+\frac{3}{8}R+\frac{R}{4})(15C)$

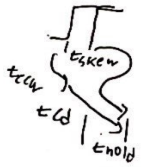
$= RC + 5RC + 15RC = 21RC \simeq 21ps$ ($\because$ ~~2R~~ $3RC = \tau = 3ps$)

5. (15pts) A back-to-back flip-flop circuit suffers from the race condition if there is clock skew between flip-flops. One of the solutions to this problem is that the use of buffer chain. Decide how many inverters are needed by assuming that the clock skew is 5ps.
(+ assume that CLK has no transition time)

5. To avoiding hold-time violation, the equation below must be satisfied

$t_{ccq} + t_{cd} \geq t_{hold} + t_{skew}$

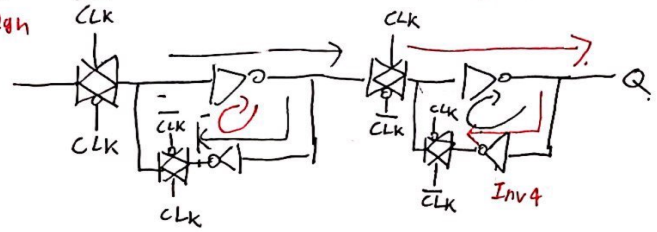
(assume that wire has zero delay)



t_{ccq} clock-to-q contamination delay

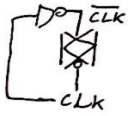
t_{cd} logic contamination delay

— CLK is Low
— CLK is High



(assume that Flip-Flop's schematic is ~~the level shifter~~ the picture on the left side)

(assume that $\overline{CLK}$ is connected to the inverter which is the source of CLK)



t_{setup} = 2x(inverter) + 1x(transmission gate)

$t_{CLK\text{-}to\text{-}q}$ = 1x(transmission gate) + 1x(inverter)

t_{hold} = Hold time can be viewed as two ways. one is the Inv4 delay for feedback of the memory, another is the delay between CLK and $\overline{CLK}$ (1 inverter delay). Thus, to sum up, regardless of ways viewed, the hold time will be 1 inverter delay.

inverter delay without load = 3RC = 3PS

previously, we assume that wire has zero delay, which means that wire does not have resistance and capacitance. Thus, transmission gate delay without wire capacitance is 0.

$t_{ccq} = 3RC = 3PS$

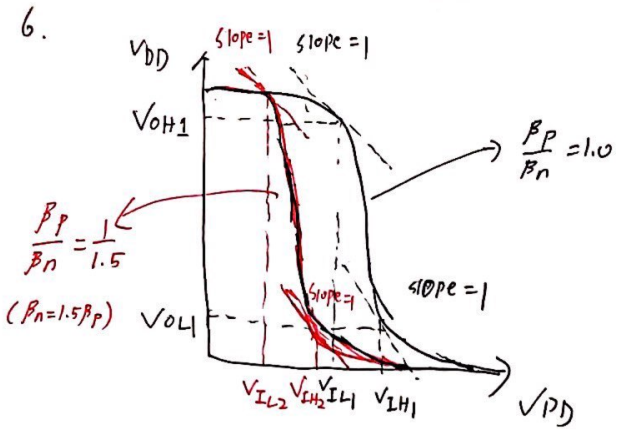
$t_{hold} = 3RC = 3PS$

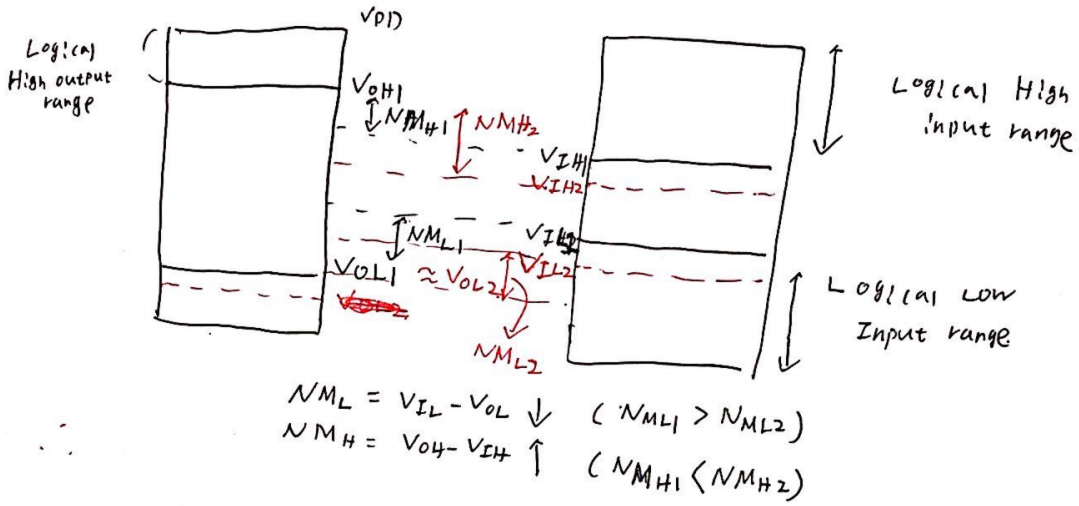
$t_{skew} = 5PS$

$t_{cd} \geq t_{hold} + t_{skew} - t_{ccq} = 5PS$

∴ at least 2 inverters (1 buffer) is needed for avoiding hold time violation

6. (15pts) Try to graphically estimate the two noise margins of a skewed inverter of $B_n = 1.5B_p$





$NM_L = V_{IL} - V_{OL}$ ↓ $(NM_{L1} > NM_{L2})$

$NM_H = V_{OH} - V_{IH}$ ↑ $(NM_{H1} < NM_{H2})$

∴ If Beta ratio $(\frac{\beta_p}{\beta_n})$ is less than 1, NM_L is decreased and NM_H is increased.