VLSI Systems Designs: Midterm Exam (2015 Fall)

11/14/2014, Prof. Jinsang Kim

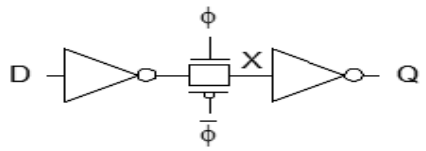
Assume that a matched unit inverter has widths of 45nm for nMOS and 90nm for pMOS, respectively. The 45nm process technology uses the followings unless stated otherwise: $V_{DD} = 1\,V,\ Vto = 0.3\,V, \beta_n = 1mA/\,V^2, \Phi_s = 0.6\,V, \gamma = 0.3\,V^{0.5}, \lambda = 0.02, \tau = 3RC = 3ps,$ $electron velocity = 10^5 cm/s$

1. (10 pts) A metal2 wire is 1um long and 2λ wide with $R = 0.08\ \Omega/\square$, $C_{permicron}$ =0.2 fF/μm . A two-input NAND gate drives a 3X receiver inverter through the above wire. Estimate the delay between two gates when the output of the NAND gate changes from '1' to '0'. Gate capacitance of a unit inverter is C=2fF/um and resistances of both nMOS and pMOS are $R = 2.5\,K\Omega \cdot \mu m$.

2. (7pts) Design a low-skewed two input CMOS AND gate. Also, verify why the gate is low-skewed.

3. (13pts) Design a high skewed two input domino OR gate and decide the logical effort and the parasitic delay.

4. (10pts) Analyze the symptom and its principle. Also, suggest a solution.



5. (10pts) Show that how much time we can borrow by drawing the timing corresponding diagram when we use 2-phase latches.

6. (50pts) Let's design a simple half adder sequencing block using buffered flip-flops. And then, analyze the timing information. Assume that there is no clock skew and T-gate input capacitance is 10C. Let's take a step-by-step approach as followings.
   a) (8pts) design the buffered FF at the transistor level.
   b) (14pts) estimate the clock-to-Q delay, setup time and hold time of the FF. T-gate delay can be simply modeled as the traveling time of main carriers between source and drain of the nMOS transistor.
   c) (14pts) design the half adder (S=a XOR b, C= a AND b) at the transistor level and estimate the propagation delay and the contamination delay. Inverted inputs are not available.
   d) (7pts) determine the maximum operating frequency of this block.
   e) (7pts) show that this block satisfies the hold time constraint or not.

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