EE714 Final Exam (2018 Spring)

09:00 ~ 10:30, 06/12/2018, Prof. Jinsang Kim

1. (10pts) In the design requirement, the maximum capacitance of a bitline of an array subsytem is 2 fP. If the subsystem has both 16 bit addresses and 16 bit I/Os, decide how many address bits are used for a column decoder. Assume that the capacitance of a bitline is 10 fP without a column decoder.

2. (10pts) Draw both a transistor-level SRAM cell and the wave forms of write of '0' when the cell stores '1'. Also, discuss the sizes of all transistors.

3. (10pts) Design both a SRAM column conditioning circuit and a large signal read SRAM circuit including operational wave forms.

4. (10pts) Design a low-power small-signal sense amplifier and then discuss its operations.

5. (10pts) Explain the detailed steps for DRAM refreshing including whys and hows.

6. (10pts) Design a pseudo-nMOS 3x8 decoder from logic level to transistor level including size information.

7. (10pts) Design a 2x2 CAM subsystem and its conditioning circuits at the transistor level. Also explain its operations.

8. (10pts) Design a ROM subsystem at the transistor level which implements 3^n table ($0 <= n <= 4$).

9. (10pts) Draw the equation of the threshold difference at the flash memory cell.

10. (10pts) Design the one bit circuit of a four-word NAND flash memory cell and explain how to program and read the third word line.

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