Digital IC Design Term Project

2016, Fall

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In this project, we design digital IC chips using front-end and back-end Synopsys CAD tools. The CAD manuals can be downloaded from the KLAS website. The starting point is a Verilog HDL model. You may use the existing Verilog code at your lab or download or write by yourself. **But you should understand all the codes and cannot use Verilog codes used for previous MPW projects or projects done in this class.**

1. For this project, each student does his/her own project. The minimum design complexity is 20K gates/student.

2. The following should be included, but not limited
    A. Should explain the algorithm of your design and draw the functional block diagram.
    B. Do RTL synthesis and analyze performances such as the number of gates, timing and power consumption.
    C. Do floorplaning the chip and P&R and add IO pads.
    D. Write the report, present, and demonstrate your design including
        i.   Algorithm & architecture
        ii. Verilog HDL codes
        iii. Your design methodology from the front-end to back-end
        iv. The experimental result and analysis at each step of your design methodology
        v.   Datasheet of your design
    E. Each student should show me that he/she knows all the steps for this design.
    F. A sample FFT Verilog code will be given so that you can finish all the details steps. Also, you should report the exercise report including results and analysis of all the intermediate (interchange formats) files of each step as possible.

3. Important dates
    A. 11/28/2016: one-page report about target design and the exercise report
    B. 12/12/2016: demo and final presentation. Submit the final report and all sources (zipped) at the KLAS website.