1.a) (6) g_{ND3} (2), g_{NR2} (2), g_I (2)

1.b) (6) G_2 (2), H_2 (2), $\bar{H}_3$ (3)

1.c) (3) $\hat{f} = \bar{H}^{\frac{1}{3}}$ (3)

1.d) (4) Width of ND3, NR2, and I (2) (2) (2)

1.e) (14) $\bar{Z} = ABC\bar{D}$, assume $\bar{D}$ is available, and Rc delay model is applied. (3)

$D = N\hat{f} + P$ for 1-stage logic (5)

ckt and sizing (3)

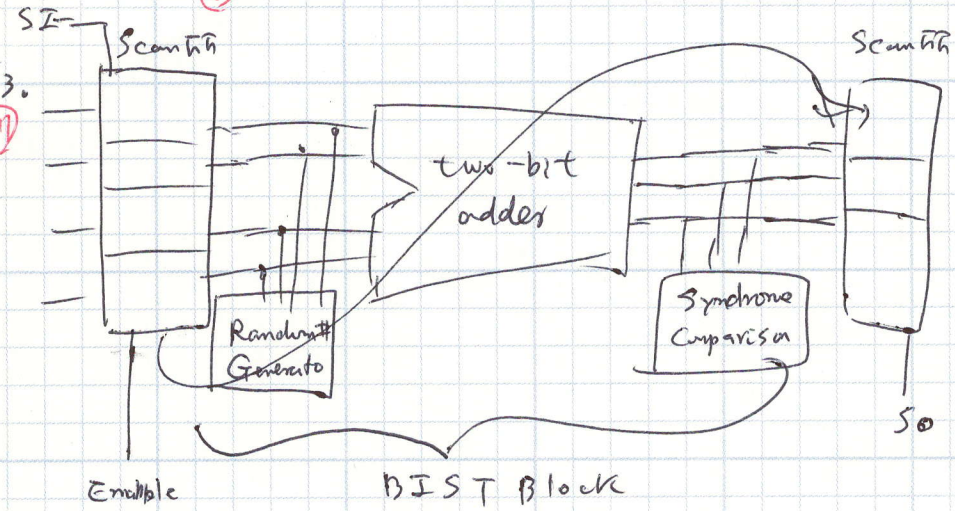
$d = gh + p$ using logical effort

comparison (3)

2.a) (15) This (7)

Latches (8)

3. (17)



Architecture (5)

Scan FF chain (6)

BIST (6)

4. (5)

test Vector

D: ~~0~~ 0

ϕ: 0

$\bar{\phi}$: 1 (5)

Normal : node X ~~V_{DD}~~ floating → '0'

SA1 : $V_{DD} - V_t$

5. (28)

Architecture (8) equ. (3) circuit (3)

PFD (5)

LF (5)

VCO (5)

N Counter (5)