**EE714 VLSI Systems Designs Quiz #1 (2020 Fall)**

2015104027 박정진

1. (15pts) Calculate the current of the bottom pMOS transistor of 2-input gate when the output voltage is 0.7V

Text

Description automatically generated

A picture containing text

Description automatically generated

2. (15pts) Explain the 2nd order effects of MOSFETs.

As the technology scaling reaches channel lengths less than , second order effects, which include velocity saturation, threshold voltage variation, hot carrier effects, and other non-idealities, become important and have a negative impact on MOSFETs' performance, whereas long-channel, ideal, first order, or Shockley model had not taken an issue. With taking account of second order effect, I-V Curve do not follow that of the ideal, first order model.

3. (15pts) Explain the aging effects and their solutions of MOSFETs.

MOSFETs are age over time like humans, and this phenomenon is called "Aging". "Aging effects" are directly related to the reliability of MOSFETs. The reliability is dependent on a lot of factors, but "Fault" in physics domain is mainly considered when discussing "Aging". Aging is caused when the MOSFETs are subjected to electric stress, such as higher than normal voltage and temperature. Aging effects frequently are divided two sections: Semiconductors and Wires. Wires wearout, which is Electromigration and Self-heating, is also important in aging effects, however, I will only consider aging of MOSFETs.

The three issues that make transistor vulnerable are:

1) Hot Carrier Injection - As transistors switch the voltage fast enough, the electrons have high velocity and can embed themselves into the gate oxide, consequently become trapped there. The trapped carrier effects on threshold voltage, which yields reducing current in nMOS and it means that transistors become slower.

2) Negative Bias Temperature Instability (NBTI) - Having a static voltage applied across the oxide for a long enough time yields an increase in "traps", and it cause the slower transistor by increasing threshold voltage. Especially, with high temperature combined with a negative bias on a pMOS (Gate voltage is 0, and Source voltage is ) the NBTI plays a crucial role in aging device.

3) Time-dependent dielectric breakdown (TDDB) - Gradual increase in gate leakage stress the oxide and lead to breakdown of MOSFETs subsequently. TDDB is dangerous since the breakdown can be caused by the prolonged exposure to moderate fields close to the regular operating voltage.

Actually, the solutions of three effects of aging should be separated to analog and digital, but I will only state the digital case due to the object of the class.

The aging effects are unavoidable, as the technology scaling reaches few nanometers, it cannot be prevented intentionally. Thus, the simplest solution is setting enough margin(timing slack) of devices with considering the degradation of speed. Or, using the digital characteristic that is that currents only flow for a very limited amount of time, make the long non-activity intervals until the next cycle of the clock. Lastly, with considering that applied electrical fields are main factor of aging, use the power gating to turn off the power supply during sleep(non-activity).

4. (40pts) Given (Complementary inputs are available.

a) draw a one-stage transistor-level CMOS circuit diagram

b) determine the size of all transistors

c) show the layout of this circuit

d) estimate the rising propagation delay when the load is a 2-input NOR gate. Explain the details of the delay components.

e) estimate the falling contamination delay when the load is a 2-input NOR gate. Explain the details of the delay components.

Diagram, schematic

Description automatically generated

5. (15pts) A back-to-back flip-flop circuit suffers from the race condition if there is clock skew between flip-flops. One of the solutions to this problem is that the use of buffer chain. Decide how many inverters are needed by assuming that the clock skew is 5ps.

(+ assume that CLK has no transition time)

Diagram, text, letter

Description automatically generated

6. (15pts) Try to graphically estimate the two noise margins of a skewed inverter of

Diagram

Description automatically generated