**EE 714 Digital IC Design Term Project**

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**Design Proposal: Comparison between MIPS and RISC-V**

**I. Introduction:**

The era of rapid transistor performance improvement by aggressive scaling down allows unprecedented development of computers on a single chip. For the sake of improving power efficiency, RISC, *Reduced Instruction Set Computer*, which was coined by David A. Patterson, UC Berkeley, came out.[1] Unlike CISC, *Complex Instruction Set Computer*, a conventional design in the early 1960s and onwards, RISC places emphasis on simplicity and efficiency. The below lists are distinct features of RISC.[2]

RISC Features:

1. Large register file

-Variables and intermediate results can be stored in registers and do not require repeated loads and stores from/to memory

- All local variables of procedures and the passed parameters can be stored in registers.

2. Emphasis on register-oriented operations (Register-to-register operations)

3. Instructions that primarily execute in a single cycle

4. Simple LOAD/STORE instructions for memory access

5. Limited addressing modes

- Most RISC instructions use simple register addressing. Complex modes can be optimized and simplified in the compiler.

6. Simple and fixed-length instructions

- Decoding is simplified since the opcode and address fields are located in the same index for all instructions. Hence, simple and small decode and execution hardware are required, and it takes up less area, which means runs faster.

7. Pipelined instruction cycle (typically uniform delay pipelines)

Under certain circumstances, such as mobile systems and portable devices, RISC has significant advantages over CISC. The below list is the potential advantages of RISC. [2]

RISC Potential advantages:

1. Fast instruction execution

2. Simple control unit

3. Fast decode

4. Faster processor design, development, and test (Reducing the time between designing and marketing)

5. Improved optimizing compiler support

Due to these advantages, RISC designs become the main trend in computer design. After the evolution of generation, which was RISC-I, II, III, IV in order, the RISC-V was presented in 2010. RISC-V is different from other CPUs in terms of proprietary. RISC-V is open-source and design without royalties. Therefore, the RTL code implementation of RISC-V is more comfortable than other architectures.

In the project, first, we will design MIPS, *Microprocessor without Interlocked Pipelined Stages*. MIPS is also RISC and is useful for academic purposes. The CSE203, Computer Architecture lecture at Kyung Hee University, also teaches MIPS and recommends implementing RTL code for a deep understanding of computer architecture. For MIPS design, we will follow steps described in a book, *Computer Organization and Design,* by David A. Patterson and John L. Hennessy. After accumulating fundamental knowledge about computer architecture, we will design the RISC-V CPU from scratch. Based on MIPS knowledge and comparison during implementation, we will try to find the main difference between MIPS and RISC-V and why RISC-V has become the main trend in computer architecture. Finally, through performance comparison, we will check that RISC-V has high performance than MIPS.

Steps

1. Design Single-Cycle MIPS

2. Design 5 stage Pipelined MIPS

3. Design Single-Cycle RISC-V

4. Design 5 stage Pipelined RISC-V

5. Performance Comparison (system clock frequency, throughput, power consumption, area)

6. Analysis - RISC-V features and advantages

**Reference:**

[1] Reilly, Edwin D., *Milestone in computer science and information technology*, Westport, CT, 2003

[2] A. D. George, "An overview of RISC vs. CISC," Proceedings. The Twenty-Second Southeastern Symposium on System Theory, Cookeville, TN, USA, 1990, pp. 436-438, doi: 10.1109/SSST.1990.138185.