SAMSUNG ELECTRONICS

STD150E
Design Kit Release Notes

For Synopsys Design-Compiler v1999.10 or later,
Power-Compiler v1999.10 or later,
PrimeTime v1999.10 or later, and
Formality v1999.10 or later.
(2005.0915, V3.1.0)

September 15, 2005

1.0 Introduction

SEC offers STD150E as a 0.13um CMOS standard cell library. The SEC's 0.13um cell based logic process(L13G) provides up to 7 layers of interconnect metal and 60um I/O pad-pitch.

This revision of STD150E library is for clearing some tuning issues. For more information, please refer to **4.0 New Features**.

2.0 Release History

2004/9/1 : The first release

2004/12/21 : The second release

2005/1/15 : The third release (primitives only)

2005/5/3 : The fourth release

2005/9/15 : The fifth release

3.0 Machine Requirements

Machine requirements for the STD150E library is as follows:

Sun® Workstation. SPARC® Station2, 10, 20, Ultra SPARC® or an equivalent.

Solaris® Version 2.5 / 2.6 / 2.7 / 2.8

Linux Redhat 7.3 kernel 2.4.18 or an equivalent

4.0 New Features

This revision of STD150E library is for clearing some tuning issues.

The negative hazard values in the last version caused some timing mismatch between sign-off and implementation tools, because sign-off tool makes negative hazard values to '0' in calculating delays, but implementation tools keep negative hazard values intact. So this revision makes all negative hazard values to '0'.

The Verilog model description of timing arcs for 'CK → GCK' in cglp*/cgln* cells contained positive edge qualifiers, but in real cases, this qualifiers are not needed. So this revision removes positive edge qualifiers of 'CK → GCK' timing arcs in cglp*/cgln* cells for Verilog DK.

PDT files are changed to support Cubic's new feature of OSC power seperation check.

5.0 Supported Memory Cores

The following table shows the memory generator that SEC provides with this release of the STD150E library. Memory generator generates a simulation model, SPC and a UDC (User Defined Cell) file. And in GUI environment, you can generate timing diagram, CLF, TLF files according to your intention.

Memory Type	Core Name	Description
High Density Type	SPSRAM_HD	High-density Single-Port Synchronous Static RAM
	SPSRAMBW_HD	High-density Single-Port Synchronous Static RAM with Bit-Write
	DPSRAM_HD	High-density Dual-Port Synchronous Static RAM
	DPSRAMBW_HD	High-density Dual-Port Synchronous Static RAM with Bit-Write
	SPSRAMR_HD	High-density Single-Port Synchronous Static RAM with Redundancy
	SRFRAM_HD	Multi-port synchronous register file
	SRFRAMBW_HD	Multi-port synchronous register file with bit-write
	VROM_HD	High-density Single-Port Synchronous Via-1 programmable ROM
	DPSRAMR_HD	High-density Dual-Port Synchronous Static RAM with Redundancy
	CAM_HD	High-density Single-Port Synchronous Binary CAM
	TCAM_HD	High-density Single-Port Synchronous Ternary CAM
Low Power Type	SPSRAM_LP	Low-power Single-Port Synchronous Static RAM
	SPSRAMR_LP	Low-power Single-Port Synchronous Static RAM with Redundancy
	SPSRAMBW_LP	Low-power Single-Port Synchronous Static RAM with Bit-Write
	DPSRAM_LP	Low-power Dual-Port Synchronous Static RAM
	DPSRAMR_LP	Low-power Dual-Port Synchronous Static RAM with Redundancy

	DPSRAMBW_LP	Low-power Dual-Port Synchronous Static RAM with Bit-Write

6.0 The Versions of SEC In-house Software and Technology Files

In-house Software & Technology Files	Version Number
CubicDelay	V1.750
CubicPower	V1.750
SATEST2	V2.3
WAVCHK	V1.1
STD150E Technology File	V3.1

7.0 On-line Documentation

On-line hyper-linked documentation is available.

The followings are the main contents.

- ✓ ASIC design kit manuals and release notes
- ✓ ASIC in-house software manuals
- ✓ ASIC design guidelines and application notes
- ✓ ASIC design kit tutorial

To use the on-line hyper-linked document, invoke Acrobat Reader and open *sec_document.pdf*.

8.0 More information

For more information about each SW specific release, please refer to the corresponding each Design Kit release notes.

9.0 Note

9.1 SDF Back-annotation in Design-Compiler

If your design includes asynchronous memory and you want to annotate a SDF file generated by CubicDelay to your design, you MUST translate your SDF file to SDF file be readable to Design-Compiler.

Why is this process needed?

Because Design Compiler have limitation. Design Compiler can not read SDF file including bracket in related_pin description.

If you want to annotate a SDF file using PrimTime for STA, you need not to translate.

SEC Synopsys design kit supports the script to translate SDF file. The script is $SEC_SYNOPSYS/aux/to_DC_sdf. The following command is usage of the script.

```
%> $SEC_SYNOPSYS/aux/to_DC_sdf target_sdf_file
```

If you get messages such as “Completed successfully!”, your SDF file is translated to

target_sdf_file.syn file. Read the translated SDF file "target_sdf_file.syn" using "read_timing" command.

10.0 To fix the design which have multiple ports

If your Design Compiler version is 1998.02 or later, notice the following description. SEC AISC flow does not allow feedthroughs or nets to connect with multiple output ports. You can fix this problem using the set_fix_multiple_port_nets command.

dc_shell> set_fix_multiple_port_nets -all -buffer_constants

Refer to "Design Compiler Reference Manual: Fundamentals Chapter3. Variables and Attributes" for detail.

11.0 PrimeTime & Formality

11.1 PrimeTime

1. SEC supports PrimeTime (TM). PrimeTime users MUST set the following variables in pt_shell for static timing analysis using SEC Synopsys technology library.

```
set dk_home [get_unix_variable {SEC_SYNOPSYS}]
set search_path [list . [format " %s%s" $dk_home {/syn/<library_name>}] ]
set link_path [list {*} <library_db_filename>]
```

The sample is found in the directory $SEC_SYNOPSYS/primetime/PTTutorial/setup.

2. PrimeTime software version should be v1999.10 or higher.

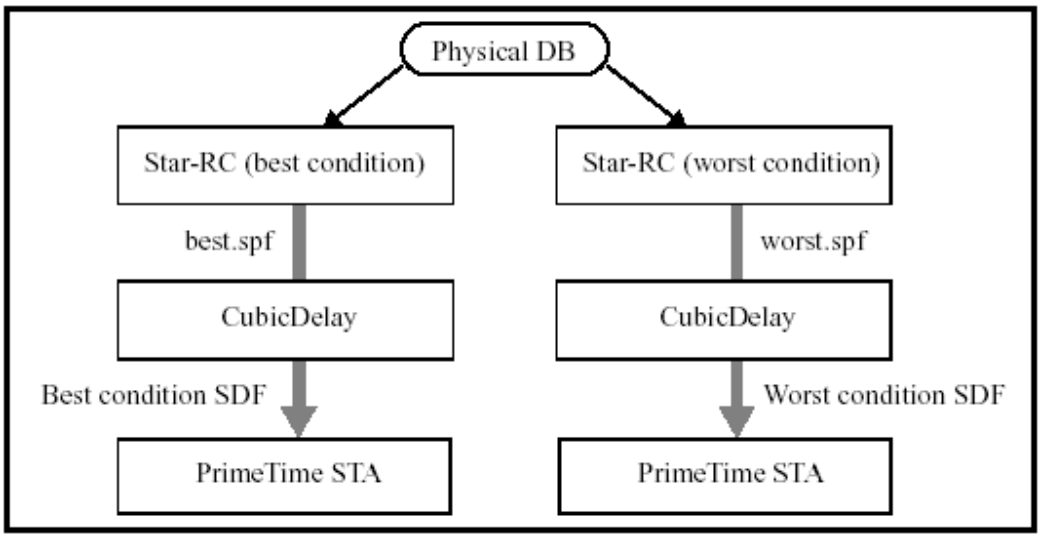
3. For SEC PrimeTime Design Kit users, PrimeTime STA requirements and guidelines are found in the directory $SEC_SYNOPSYS/primetime/doc/Guideline.

4. Demo circuits/scripts are provided to demonstrate PrimeTime's analysis for design cases.
Locate these circuits and pt_shell scripts in the directory $SEC_SYNOPSYS/primetime/demo_ckt. For each case, an application note is available in the directory $SEC_SYNOPSYS/primetime/doc/ApplNotes.

5. For PrimeTime STA, a tutorial is available. *$SEC_SYNOPSYS/primetime/PTTutorial/* contains the contents of tutorial. Read $SEC_SYNOPSYS/primetime/PTTutorial/README for more detailed information about the tutorial.

6. For SEC PrimeTime Design Kit users, the PrimeTime sample scripts for at-speed, scan-test, and bist-sta are found in the directory $SEC_SYNOPSYS/primetime/STA_scripts.

7. Final STA sign-off flow To better model PVT variation of wire capacitance and resistance, separate RC extractions for different operating conditions at post-layout signoff is required. To support this, separate Star-RC technology files are used for different process conditions. CubicDelay accepts various input files from various physical design tools and RC extraction tools to efficiently but accurately compute delays. A separate set of input files for delay calculation for CubicDelay and back-annotation for PrimeTime are necessary for each operating condition. For more details, refer to " Static Timing Analysis Signoff (with PrimeTime)" in the directory $SEC_SYNOPSYS/primetime/doc/STA_primesignoff-gl_v4.0.pdf. The following shows the final STA sign-off flow.



11.2 Formality

1. SEC supports Formality (TM). Formality users MUST set the following variables using SEC Synopsys technology library and SEC Formality utility.

   unix% setenv SEC_SYNOPSYS <installed_synopsys_design_kit_directory>
   unix% setenv SEC_FM $SEC_SYNOPSYS/formality
   fm_shell> source $env(SEC_FM)/synopsys_fm.setup

   Formality users also put $env(SEC_SYNOPSYS)/formality/synopsys_fm.setup file in user's home directory or working directory as .synopsys_fm.setup file.

2. For SEC Formality Design Kit users, a Formality guidelines is found in the directory $SEC_FM/docs

3. Demo circuits/scripts are provided to demonstrate Formality's equivalence the directory checking procedure for design cases. Locate these circuits and fm_shell scripts in the directory $SEC_FM/tutorial.

12.0 Power

1. Power Compiler(TM) software version should be 1999.10 or higher.

2. Power Compiler users MUST set the following variable to analyze and optimize the power consumption of their designs:

   search_path = { . synopsys_root + "/libraries/syn" dk_home + "/syn/<library_name>" dk_home_aux};

3. Power Compiler users can generate SAIF(Switching Activity Interchange Format) file from $SEC_SYNOPSYS/syn/<library_name>/library_db_filename using Synopsys product such as Design Compiler(TM).

4. For SEC Power Design Kit users, Power Compiler requirements and guidelines are found in the directory $SEC_SYNOPSYS/power/doc

5. For Power Compiler, a tutorial is available. $SEC_SYNOPSYS/power/tutorial contains the contents of tutorial.

6. SEC also has a gate level power analysis tool named CubicPower. If Power Compiler users want to analysis their design more accurately, use CubicPower. If Power Compiler users want to use CubicPower, please contact a local DC or HQ.

13.0 More information

For more information, please refer to '$SEC_SYNOPSYS/readme/README', '$SEC_SYNOPSYS/readme/SynopsysDKGuide.pdf', or contact a local SEC design center.

- '$SEC_SYNOPSYS/readme/README' describes design kit version, setting UNIX variables before using design kit, the contents of this design kit, and so on.
- '$SEC_SYNOPSYS/readme/SynopsysDKGuide.pdf' describes installation, design kit architecture, synthesis procedure, and so on.

NOTE

If you have any questions or comments, please contact Samsung for assistance:

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