33rd IEEE International Conference on Computer Design (ICCD)

18-21 October 2015
New York City, USA

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Welcome Message

Welcome to the 33rd edition of the IEEE International Conference on Computer Design (ICCD) being held for the first time in New York City. ICCD encompasses a wide range of topics in research, design, and implementation of computer systems and their components. Over the last 33 years, ICCD has been at the forefront of creating, nurturing and promoting new research directions in computer design, including ***secure computer design,*** the theme for this year.

ICCD 2015 received over 269 regular paper submissions -- 87 to the Computer Systems and Application Track, 39 to the Electronic Design Automation Track, 47 to the Logic and Circuit Design Track, 42 to the Processor Architecture Track, and 54 to Test, Verification and Security Track. The ICCD program committee has done an outstanding job in selecting a truly outstanding technical program with 83 regular papers for presentation (acceptance rate: 31%) and 29 posters.

ICCD 2015 also features three special sessions and two tutorials for presentations.

Owing to a limited number of presentation slots coupled with an un precedented number of high quality submissions -- regular papers, special session, and tutorials -- many excellent submissions could not be included in the ICCD 2015 program.

ICCD 2015 is delighted to host two top notch keynotes by Prof. Todd Austin of the University of Michigan and Mark Moraes of DE Shaw Research.

ICCD 2015 invites you to ***Something Rotten!*** and a pre-theater dinner ar Carmine's.

Welcome to New York! New York'a hoşgeldiniz ! न्यूयॉर्क में स्वागत है ! مرحبا بكم في نيويورك benvenuti a New York! Σας καλωσορίζουμε στη Νέα Υόρκη! Willkommen nach New York 欢迎你们到纽约！ニューヨークへようこそ！ 뉴욕에 오신 것을 환영합니다 van harte welkom in new york ! bem-vindo para Nova Iorque ! velkommen til new york Bienvenue à New York ! Добро пожаловать в Нью-Йорк ! Välkommen till new york !

Sincerely,
ICCD 2015 organizing, program and steering committee.

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MAP 18 - 20

Event Location

1) Kimmel Center
60, Washington Sq. South, New York City, NY-10010

2) NYU Abu Dhabi
19, Washington Sq. North, New York City, NY-10011

Wireless Access on the NYU Campus

The NYU campus has wireless accesss throughout its buildings. To login the service please look for the Wi-Fi network "NYUROAM" and use below details:

Guest Account:- guest123
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33rd IEEE International Conference on Computer Design

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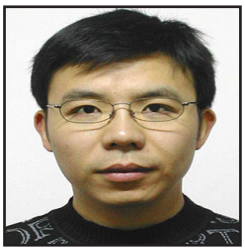

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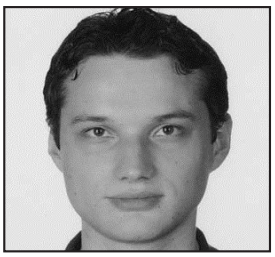

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Monday, October 19, 2015

Keynote

Eisner & Lubin Auditorium, 4th Floor, Kimmel Center

Todd Austin
University of Michigan

Ending the Tyranny of Amdahl's Law

ABSTRACT: If the computing industry wants to continue to make scalability the primary source of value in tomorrow's computing systems, we will have to quickly find new and productive ways to scale the serial portions of important applications. In this talk, I will highlight my work and the work of others to do just this through the application of heterogeneous parallel designs. Of course, we will want to address the scalability of sequential codes, but future scalability success will ultimately hinge on addressing how we address the scalability of future applications' through more affordable design and manufacturing techniques.

BIOGRAPHY: Todd Austin is a Professor of Electrical Engineering and Computer Science at the University of Michigan in Ann Arbor. His research interests include computer architecture, robust and secure system design, hardware and software verification, and performance analysis tools and techniques. Currently Todd is director of C–FAR, the Center for Future Architectures Research, a multi–university SRC/DARPA funded center that is seeking technologies to scale the performance and efficiency of future computing systems. Prior to joining academia, Todd was a Senior Computer Architect in Intel's Microcomputer Research Labs, a product–oriented research laboratory in Hillsboro, Oregon. Todd is the first to take credit (but the last to accept blame) for creating the Simple Scalar Tool Set, a popular collection of computer architecture performance analysis tools. Todd is co–author (with Andrew Tanenbaum) of the undergraduate computer architecture textbook, "Structured Computer Architecture, 6th Ed." In addition to his work in academia, Todd is founder and President of Simple Scalar LLC and co–founder of In Tempo Design LLC. In 2002, Todd was a Sloan Research Fellow, and in 2007 he received the ACM Maurice Wilkes Award for "Innovative contributions in Computer Architecture including the Simple Scalar Toolkit and the DIVA and Razor architectures." Todd received his PhD in Computer Science from the University of Wisconsin in 1996.

MONDAY, OCTOBER 19, 2015

08:00-08:30	**Breakfast**	*Eisner & Lubin Auditorium, 4th Floor, Kimmel Center*
08:30-10:00	**Opening & Keynote** **Ending the Tyranny of Amdahl's Law** *Todd Austin, University of Michigan*	*Eisner & Lubin Auditorium, 4th Floor, Kimmel Center*
10:00-10:15	**Break**	*Eisner & Lubin Auditorium, 4th Floor, Kimmel Center*

Session 1

10:15-11:35	**CSA 1 : NOC Design**	*405, Kimmel Center*
	Session Chair: Paul Gratz, *Texas A&M University*	
	Design of High-Performance, Power-Efficient Optical NoCs Using Silica-Embedded Silicon Nanophotonics *Elena Kakoulli, Vassos Soteriou, Charalambos Koutsides and Kyriacos Kalli*	
	A Fast and Energy Efficient Branch and Bound Algorithm for NoC Task Mapping *Jiashen Li and Yun Pan*	
	RoB-Router :Low Latency Network-on-Chip Router Microarchitecture Using Reorder Buffer *Cunlu Li and Dezun Dong*	
	PID Controlled Thermal Management of Photonic Network-on-Chip *Dharanidhar Dang, Rabi Mahapatra and Ej Kim*	
11:40-13:00	**CSA2: Energy and Performance Optimization**	*405, Kimmel Center*
	Session Chair: Mingoo Seok, *Columbia University*	
	Exploring multiple sleep modes in On/Off based Energy Efficient HPC Networks *Karthikeyan P. Saravanan, Paul Carpenter and Alex Ramirez*	
	Wide I/O or LPDDR? Exploration and Analysis of Performance, Power and Temperature Trade-offs of Emerging DRAM Technologies in Embedded MPSoCs *Mohammad Hossein Hajkazemi, Mohammad Khavari Tavana and Houman Homayoun*	
	Improving the Interface Performance of Synthesized Structural FAME Simulators through Scheduling *David Penry*	
	Using M/G/1 Queueing Models with Vacations to Analyze Virtualized Logic Computations *Michael Hall and Roger Chamberlain*	
13:00-14:00	**Lunch**	*Eisner & Lubin Auditorium, 4th Floor, Kimmel Center*
14:00-15:20	**CSA-3: Reliability and Memory Organization**	*405, Kimmel Center*
	Session Chair: Karthik Swaminathan, *IBM*	
	Clotho: Proactive Wearout Deceleration in Chip-Multiprocessor Interconnects *Arseniy Vitkovskiy, Paul Gratz and Vassos Soteriou*	
	DLB: Dynamic Lane Borrowing for Improving Bandwidth and Performance in Hybrid Memory Cube *Xianwei Zhang, Youtao Zhang and Jun Yang*	
	Memory Design for Selective Error Protection *Yanan Cao, Long Chen and Zhao Zhang*	
	POS: A Popularity-based Online Scaling Scheme for RAID-Structured Storage Systems *Si Wu, Yinlong Xu, Yongkun Li and Yunfeng Zhu*	
15:20-15:30	**Break**	*Eisner & Lubin Auditorium, 4th Floor, Kimmel Center*
15:30-16:30	**LCD - 1: Application Oriented Design**	*405, Kimmel Center*
	Session Chair: Jie Gu, *Northwestern University*	
	High-Speed Polynomial Multiplication Architecture for Ring-LWE Based Cryptosystems *Chaohui Du, Guoqiang Bai and Xingjun Wu*	
	A High-performance Dual-field Elliptic Curve Cryptographic Processor Based on a Systolic Array *Guoqiang Bai, Zhenwei Zhao and Gang Chen*	
	InvArch: A Hardware-Efficient Architecture for Matrix Inversion *Umer Cheema, Gregory Nash, Rashid Ansari and Ashfaq Khokhar*	

MONDAY, OCTOBER 19, 2015

Session 2

10:15-11:35	**TVS 1 : Verification**	*406, Kimmel Center*
	Session Chair: Masahiro Fujita, *University of Tokyo*	
	Power-Aware Multi-Voltage Custom Memory Models for Enhancing RTL and Low Power Verification *Vijay Kiran Kalyanam, Martin Saint-Laurent and Jacob Abraham*	
	Clustering-based Revision Debug in Regression Verification *Djordje Maksimovic, Andreas Veneris and Zissis Poulos*	
	SI-SMART: Functional Test Generation for RTL Circuits Using Loop Abstraction and Learning Recurrence Relationships *Prateek Puri and Michael Hsiao*	
	Emulation-Based Selection and Assessment of Assertion Checkers for Post-Silicon Validation *Pouya Taatizadeh and Nicola Nicolici*	
11:40-13:00	**EDA1: Error and Fault Tolerant Circuits**	*406, Kimmel Center*
	Session Chair: Donatella Sciuto, *Politecnico di Milano*	
	An Automated Design Flow for Approximate Circuits based on Reduced Precision Redundancy *Daniele Jahier Pagliari, Andrea Calimera, Enrico Macii and Massimo Poncino*	
	Logic Simplification by Minterm Complement for Error Tolerant Application *Hideyuki Ichihara, Tomoya Inaoka, Tsuyoshi Iwagaki and Tomoo Inoue*	
	Fault-Tolerant In-Memory Crossbar Computing using Quantified Constraint Solving *Alvaro Velasquez and Sumit Kumar Jha*	
	Improving Reliability, Performance, and Energy Efficiency of STT-MRAM with Dynamic Write Latency *Ali Ahari, Mojtaba Ebrahimi, Fabian Oboril and Mehdi Tahoori*	
13:00-14:00	**Lunch**	*Eisner & Lubin Auditorium, 4th Floor, Kimmel Center*
14:00-15:20	**PA-1: Optimizing Cache Access**	*406, Kimmel Center*
	Session Chair: Gang Quan, *Florida International University*	
	Immediate Sleep: Reducing Energy Impact of Peripheral Circuits in STT-MRAM Caches *Eishi Arima, Hiroki Noguchi, Takashi Nakada, Shinobu Miwa, Susumu Takeda, Shinobu Fujita and Hiroshi Nakamura*	
	Exploit Common Source-Line to Construct Energy Efficient Domain Wall Memory based Caches *Xianwei Zhang, Lei Zhao, Youtao Zhang and Jun Yang*	
	SCP: Synergistic Cache Compression and Prefetching *Bhargavraj Patel, Gokhan Memik and Nikos Hardavellas*	
	Application Behavior Aware Re-reference Interval Prediction for Shared LLC *Parth Lathigara, Shankar Balachandran and Virendra Singh*	
15:20-15:30	**Break**	*Eisner & Lubin Auditorium, 4th Floor, Kimmel Center*
15:30-16:30	**Special Session 1: Data Mining for Computer Design**	*406, Kimmel Center*
	Session Chair: Antonio Miele, *Politecnico di Milano*	
	Applied Statistical Inference for System Design and Management *Benjamin Lee, Duke University*	
	Exploiting GPU architectures for dynamic invariant mining *Nicola Bombieri, Federico Busato, Alessandro Danese, Luca Piccolboni and Graziano Pravadelli, University of Verona*	
	ItHELPS: Iterative High-accuracy Error Localization in Post-Silicon *Valeria Bertacco and Wade Bonkowski, University of Michigan*	

TUESDAY, OCTOBER 20, 2015

KEYNOTE

Eisner & Lubin Auditorium, 4th Floor, Kimmel Center

Mark Moraes
D. E. Shaw Research

Exploiting Hardware-Software Co-Design to Speed Up Molecular Dynamics Simulation

ABSTRACT: Anton 2 is the second generation of a family of massively parallel special-purpose supercomputers for molecular dynamics simulations. The embedded software that runs on the Anton machines is co-designed with the underlying hardware, allowing the code to exploit unique capabilities of the hardware, and the hardware to make careful trade-offs for maximum performance, while preserving flexibility and programmability. This closely coupled co-design is a major reason for Anton's large performance improvement–as much as two orders of magnitude–over commodity clusters and general-purpose supercomputers.

BIOGRAPHY: Mark Moraes is Head of Engineering at D. E. Shaw Research, where he leads the engineering and systems development work conducted at DESRES. Mark received an M.A.Sc. from the University of Toronto, and a B.Tech. from the Indian Institute of Technology, New Delhi, both in electrical engineering.

TUESDAY, OCTOBER 20, 2015

08:00-08:30	**Breakfast**	*Eisner & Lubin Auditorium, 4th Floor, Kimmel Center*
08:30-09:35	**Keynote** **Exploiting Hardware-Software Co-Design to Speed Up Molecular Dynamics Simulation** *Mark Moraes, D. E. Shaw Research*	*Eisner & Lubin Auditorium, 4th Floor, Kimmel Center*

Session 1

09:30-10:30	**CSA-4: Heterogeneous Computing Systems**	*405, Kimmel Center*
	Session Chair: Houman Homayoun, *George Mason University*	
	An orchestrated approach to efficiently manage resources in heterogeneous system architectures *Gabriele Pallotta, Gianluca Durelli, Antonio Miele, Cristiana Bolchini and Marco Domenico Santambrogio*	
	Energy-Efficient Execution of Data-Parallel Applications on Heterogeneous Mobile Platforms *Alok Prakash, Siqi Wang, Alexandru Eugen Irimiea and Tulika Mitra*	
	Sequential C-code to Distributed Pipelined Heterogeneous MPSoC Synthesis for Streaming Applications *Jude Angelo Ambrose, Jorgen Peddersen, Yusuke Yachide, Kapil Batra and Sri Parameswaran*	
10:30-10:50	**Break**	*Eisner & Lubin Auditorium, 4th Floor, Kimmel Center*
10:50-12:30	**EDA -2: Logic and Layout Synthesis**	*405, Kimmel Center*
	Session Chair: Kyle Rupnow, *Advanced Digital Sciences Center*	
	SOP Based Logic Synthesis for Memristive IMPLY Stateful Logic *Felipe Marranghello, Vinicius Callegaro, Andre Reis and Renato Ribas*	
	CSL: Coordinated and Scalable Logic Synthesis Techniques for Effective NBTI Reduction *Chen-Hsuan Lin, Subhendu Roy, Chun-Yao Wang, David Z. Pan and Deming Chen*	
	A Pre-search Assisted ILP Approach to Analog Integrated Circuit Routing *Chia-Yu Wu, Helmut Graeb and Jiang Hu*	
	Trace-Based Automated Logical Debugging for High-Level Synthesis Generated Circuits *Pietro Fezzardi, Michele Castellana and Fabrizio Ferrandi*	
	Physical Synthesis of DNA Circuits with Spatially Localized Gates *Jinwook Jung, Daijoon Hyun and Youngsoo Shin*	
12:30-13:50	**Lunch**	*Eisner & Lubin Auditorium, 4th Floor, Kimmel Center*
13:50-15:30	**PA-2: Optimization for Power and Speed**	*405, Kimmel Center*
	Session Chair: Nikos Hardavellas, *Northwestern Universiy*	
	Comparison of Single-ISA Heterogeneous versus Wide Dynamic Range Processors for Mobile Applications *Hamid Reza Ghasemi, Ulya R. Karpuzcu and Nam Sung Kim*	
	A Low-Cost and Low-Latency Heterogeneous Ring-Chain Network for GPGPUs *Xia Zhao, Sheng Ma, Chen Li, Lu Wang and Zhiying Wang*	
	Effective Hardware-Level Thread Synchronization for High Performance and Power Efficiency in Application Specific Multithreaded Embedded Processors *Mahanama Wickramasinghe and Hui Guo*	
	Dynamic Core Scaling: Trading off Performance and Energy Beyond DVFS *Wei Zhang, Hang Zhang and John Lach.*	
	Online Mechanism for Reliability and Power-Efficiency Management of a Dynamically Reconfigurable Core *Sudarshan Srinivasan, Israel Koren and Sandip Kundu*	
15:30-16:30	**Poster Session**	*Eisner & Lubin Auditorium, 4th Floor, Kimmel Center*
16:30-21:30	**Social Event**	

POSTER SESSION -TUESDAY, OCTOBER 20, 2015

1	**Power Management of Pulsed-Index Communication Protocols** *Shahzad Muzaffar and Ibrahim (Abe) M. Elfadel*
2	**Big Data on Low Power Cores Are Low Power Embedded Processors a good fit for the Big Data Workloads?** *Maria Malik and Houman Homayoun*
3	**Energy-Optimal Voltage Model Supporting a Wide Range of Nodal Switching Rates for Early Design-Space Exploration** *Doyun Kim, Jiangyi Li and Mingoo Seok*
4	**On the Conditions of Guaranteed k-Fault Tolerant Systems Supporting On-The-Fly Repairs** *Soumya Banerjee and Wenjing Rao*
5	**Exploring the Viability of Stochastic Computing** *Joao Marcos de Aguiar and Sunil P. Khatri*
6	**A new encoding mechanism for low power inter-chip serial communication in asynchronous circuits** *Tomohiro Yoneda and Masashi Imai*
7	**Energy-Efficient Data Movement with Sparse Transition Encoding** *Yanwei Song, Mahdi Nazm Bojnordi and Engin Ipek*
8	**A Low Power Buffer-Aided Vector Register File for LTE Baseband Signal Processing** *Liu Zhiguo, Zhu Ziyuan, Shi Jinglin, Liu Jinbao and Li Shiqiang*
9	**An Aging-Aware Battery Charge Scheme for Mobile Devices Exploiting Plug-in Time Patterns** *Alberto Bocca, Alessandro Sassone, Alberto Macii, Enrico Macii and Massimo Poncino*
10	**Analytic Processor Model for Fast Design-Space Exploration** *Rik Jongerius, Giovanni Mariani, Andreea Simona Anghel, Gero Dittmann, Erik Vermij and Henk Corporaal*
11	**A Pair Selection Algorithm for Robust RO-PUF Against Environmental Variations and Aging** *Md. Tauhidur Rahman, Domenic Forte, Fahim Rahman and Mark Tehranipoor*
12	**Chameleon: Adaptive Energy-Efficient Heterogeneous Network-on-Chip** *Ji Wu, Dezun Dong, Xiangke Liao and Li Wang*
13	**Combative Cache Efficacy Techniques: Analysis of cache replacement in the context of independent prefetching in last level cache** *Cesar Gomes and Mark Hempstead*
14	**Shift-Aware Racetrack Memory** *Ehsan Atoofian and Ahsan Saghir*
15	**ROST-C: Reliability driven Optimisation and Synthesis Techniques for Combinational Circuits** *Satish Grandhi, David McCarthy, Christian Spagnol, Emanuel Popovici and Sorin Cotofana*

POSTER SESSION -TUESDAY, OCTOBER 20, 2015

16	**Data-Driven Logic Synthesizer for Acceleration of Forward Propagation in Artificial Neural Networks** *Khaled Z. Mahmoud, William E. Smith, Mark Fishkin and Timothy N. Miller*
17	**Fixed-Function Hardware Sorting Accelerators for Near Data MapReduce Execution** *Seth H. Pugsley, Arjun Deb, Rajeev Balasubramonian and Feifei Li*
18	**Energy-Efficient Reconstruction of Compressively Sensed Bioelectrical Signals with Stochastic Computing Circuits** *Yufei Ma, Minkyu Kim, Yu Cao, Jae-Sun Seo and Sarma Vrudhula*
19	**Exploiting Request Characteristics and Internal Parallelism to Improve SSD Performance** *Bo Mao and Suzhen Wu*
20	**FDRAM: DRAM Architecture Flexible in Successive Row and Column Accesses** *Jeongjae Yu and Wooyoung Jang*
21	**Runtime Multi-Optimizations for Energy Efficient On-chip Interconnections** *Yuan He, Masaaki Kondo, Takashi Nakada, Hiroshi Sasaki, Shinobu Miwa and Hiroshi Nakamura*
22	**A Hardware-based Multi-objective Thread Mapper for Tiled Manycore Architectures** *Ravi Kumar Pujari, Thomas Wild and Andreas Herkersdorf*
23	**Automatic identification of assertions and invariants with small numbers of test vectors** *Masahiro Fujita*
24	**A Novel 3D Graphics DRAM Architecture for High-Performance and Low-Energy Memory Accesses** *Ishan G Thakkar and Sudeep Pasricha*
25	**M-MAP: Multi-Factor Memory Authentication for Secure Embedded Processors** *Syed Kamran Haider, Masab Ahmad, Farrukh Hijaz, Astha Patni, Ethan Johnson, Matthew Seita, Omer Khan and Marten van Dijk*
26	**Acceleration of Microwave Imaging Algorithms for Breast Cancer Detection via High-Level Synthesis** *Daniele Jahier Pagliari, Mario R. Casu and Luca P. Carloni*
27	**Power and Performance Characterization, Analysis and Tuning for Energy-efficient Edge Detection on Atom and ARM based Platforms** *Paul Otto, Maria Malik, Nima Akhlaghi, Rebel Sequeira, Houman Homayoun and Siddhartha Sikdar*
28	**Security Implications of Cyberphysical Digital Microfluidic Biochips** *Sk Subidh Ali, Mohamed Ibrahim, Ozgur Sinanoglu, Krishnendu Chakrabarty and Ramesh Karri*
29	**Hardware Support for Production Run Diagnosis of Performance Bugs** *Abdullah Muzahid*
30	**Pre-Promotion: Synergizing Prefetching and Anti-thrashing Replacement Policy [Work in Progress]** *Midoriko Chikara, Hidetsugu Irie, Makoto Sahoda, Masato Yoshimi and Tsutomu Yoshinaga*

TUESDAY, OCTOBER 20, 2015

Session 2

09:30-10:30	**Special Session 2: Cyber-physical Integration and Design Automation for Microfluidic Biochips** *406, Kimmel Center*
	Session Chair: Jiang Hu, *Texas A&M University*
	Wet Computers: The Need for Design Automation and Programmability in Microfluidics *William Grover, University of California at Riverside*
	Cyber-physical Adaptation in Digital Microfluidic Biochips *Tsung-Yi Ho, William Grover, Shiyan Hu and Krishnendu Chakrabarty, Duke University*
	Physical Design for Cyber-physical Microfluidic Biochips: Co-Optimization and Co-Scheduling of Biochemical Operations and On-Chip Sensors *Tsung-Yi Ho, National Tsinghua University*
10:30-10:50	**Break** *Eisner & Lubin Auditorium, 4th Floor, Kimmel Center*
10:50-12:30	**TVS-2: Security** *406, Kimmel Center*
	Session Chair: Simha Sethumadhavan, *Columbia University*
	Deep Packet Field Extraction Engine (DPFEE): A Pre-processor for Network Intrusion Detection and Denial-of-Service Detection Systems *Vinayaka Jyothi, Sateesh K. Addepalli and Ramesh Karri*
	3D Integration: New Opportunities in Defense Against Cache-timing Side-channel Attacks *Chongxi Bao and Ankur Srivastava*
	Side-Channel Power Analysis of a GPU AES Implementation *Chao Luo, Yunsi Fei, Pei Luo, Saoni Mukherjee and David Kaeli*
	Performance Optimization for On-Chip Sensors to Detect Recycled Ics *Bicky Shakya, Ujjwal Guin, Mark Tehranipoor and Domenic Forte*
	From Theory to Practice of Private Circuit: A Cautionary Note *Debapriya Basu Roy, Shivam Bhasin, Sylvain Guilley, Jean-Luc Danger and Debdeep Mukhopadhyay*
12:30-13:50	**Lunch** *Eisner & Lubin Auditorium, 4th Floor, Kimmel Center*
13:50-15:30	**LCD-2: Resistive Memories** *406, Kimmel Center*
	Session Chair: Sankar Basu, *NSF*
	Fast Boolean Logic Mapped on Memristor Crossbar *Lei Xie, Hoang Anh Du Nguyen, Mottaqiallah Taouil, Said Hamdioui and Koen Bertels*
	Reliable and High Performance STT-MRAM Architectures based on Controllable-Polarity Devices *Kaveh Shamsi, Yu Bi, Yier Jin, Pierre-Emmanuel Gaillardon, Michael Niemier and X. Sharon Hu*
	Increasing Reconfigurability with Memristive Interconnects *John Demme, Steven Nowick, Bipin Rajendran and Simha Sethumadhavan*
	Optimizing Latency, Energy, and Reliability of 1T1R Reram Through Appropriate Voltage Settings *Manqing Mao, Yu Cao, Shimeng Yu and Chaitali Chakrabarti*
	A Thermal Adaptive Scheme for Reliable Write Operation on RRAM Based Architectures *Fernando García-Redondo, Marisa Lopez-Vallejo and Pablo Ituero*
15:30-16:30	**Poster Session** *Eisner & Lubin Auditorium, 4th Floor, Kimmel Center*
16:30-21:30	**Social Event**

Tuesday, October 20, 2015

Social Event

Pre-Theatre Dinner @ 5:00 pm

CARMINE'S SM

Location: 200 W 44th St, New York, NY 10036
Phone:(212) 221-0242

BROADWAY SHOW @ 7:30 pm

Location: St. James Theatre
246 West 44th Street Between 7th & 8th Avenue

WEDNESDAY, OCTOBER 21, 2015

08:00-08:30	**Breakfast**	*Eisner & Lubin Auditorium, 4th Floor, Kimmel Center*

Session 1

08:30-10:10	**LCD-3: Design of Special Function Circuit**	*405, Kimmel Center*
	Session Chair: Bo Yuan, *City College NY*	
	A Methodology for Power Characterization of Associative Memories *Dawei Li, Siddhartha Joshi, Seda Ogrenci-Memik, James Hoff, Sergo Jindariani, Tiehui Liu, Jamieson Olsen and Nhan Tran*	
	Exploring Well Configurations for Voltage Level Converter Design in 28nm UTBB FDSOI technology *Pasquale Corsonello, Stefania Perri and Fabio Frustaci*	
	A Wirelessly Powered System with Charge Recovery Logic *Leo Filippini, Emre Salman and Baris Taskin*	
	Reactive Clocks with Variability-Tracking Jitter *Jordi Cortadella, Luciano Lavagno, Pedro López, Marc Lupon, Alberto Moreno, Antoni Roca and Sachin S. Sapatnekar.*	
	Methods for Analysing and Improving the Fault Resilience of Delay-Insensitive Codes *Jakob Lechner, Andreas Steininger and Florian Huemer*	
10:10-10:30	**Break**	*Eisner & Lubin Auditorium, 4th Floor, Kimmel Center*
10:30-12:10	**CSA-5: Managing Multi-Core Systems**	*405, Kimmel Center*
	Session Chair: Ann Gordon-Ross, *University of Florida*	
	Pool Directory: Efficient Coherence Tracking with Dynamic Directory Allocation in Many-core Systems *Sudhanshu Shukla and Mainak Chaudhuri*	
	A Multicore Vacation Scheme for Thermal-Aware Packet Processing *Chih-Hsun Chou and Laxmi Bhuyan*	
	Dark Silicon Aware Runtime Mapping for Many-core Systems: A Patterning Approach *Anil Kanduri, Mohammad-Hashem Haghbayan, Amir-Mohammad Rahmani, Axel Jantsch, Pasi Liljeberg and Hannu Tenhunen*	
	Realizing Complexity-Effective On-Chip Power Delivery for Many-Core Platforms by Exploiting Optimized Mapping *Mohammad Khavari Tavana, Divya Pathak, Mohammad Hossein Hajkazemi, Maria Malik, Ioannis Savidis and Houman Homayoun*	
	Cache Allocation for Fixed-Priority Real-Time Scheduling on Multi-Core Platforms *Gustavo A. Chaparro-Baquero, Soamar Homsi, Omara Vichot, Shaolei Ren, Gang Quan and Shangping Ren*	
12:10-13:30	**Lunch**	*Eisner & Lubin Auditorium, 4th Floor, Kimmel Center*
13:30-15:10	**CSA-6: Performance Monitoring and Characterization**	*405, Kimmel Center*
	Session Chair: Sisu Xi, *Two Sigma Securities*	
	RAPITIMATE: Rapid Performance Estimation of Pipelined Processing Systems Containing Shared Memory *Su Shwe, Kapil Batra, Yusuke Yachide, Jorgen Peddersen and Sri Parameswaran*	
	Power Agility Metrics: Measuring Dynamic Characteristics of Energy Proportionality *Rizwana Begum and Mark Hempstead*	
	VPM: Virtual Power Meter Tool for Low-Power Many-Core/Heterogeneous Data Center Prototype *Santhosh Kumar Rethinagiri, Oscar Palomar, Javier Arias Moreno, Osman Unsal and Adrian Cristal*	
	TriState-SET: Proactive SET for Improved Performance of MLC Phase Change Memories *Xianwei Zhang, Youtao Zhang and Jun Yang*	
	OpenNVM: An Open-Sourced FPGA-based NVM Controller for Low Level Memory Characterization *Jie Zhang, Gieseo Park, David Donofrio, Mustafa Shihab, John Shalf and Myoungsoo Jung*	
15:10-15:30	**Break**	*Eisner & Lubin Auditorium, 4th Floor, Kimmel Center*
15:30-16:30	**CSA-7: Application-Specific Computation**	*405, Kimmel Center*
	Session Chair: Jiang Li, *Shanghai Jiao Tong University*	
	Energy-Efficient Implementations of GF(p) and GF(2^m) Elliptic Curve Cryptography *Andrew Targhetta, Donald Owen, Francis Israel and Paul Gratz*	
	Hybrid Sratchpad and Cache Memory Management for Energy-Efficient Parallel HEVC Encoding *Chang Song, Lei Ju and Zhiping Jia*	
	Mobile Ecosystem Driven Application-Specific Low-Power Control Microarchitecture *Garo Bournoutian and Alex Orailoglu*	

WEDNESDAY, OCTOBER 21, 2015

Session 2

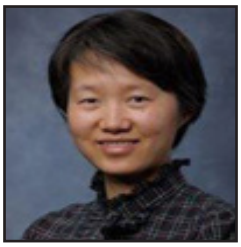
08:30-10:10	**PA-3: Architecting Processors Using New Circuit Technologies and Topologies** *406, Kimmel Center*
	Session Chair: Shinobu Miwa, *The University of Electro-Communications*
	Architecting a MOS Current Mode Logic (MCML) Processor for Fast, Low Noise and Energy-Efficient Computing in the Near-Threshold Regime *Yuxin Bai, Yanwei Song, Mahdi Nazm Bojnordi, Alex Shapiro, Engin Ipek and Eby Friedman*
	VLSI Implementation of High-Throughput, Low-Energy, Configurable MIMO Detector *Pierce I-Jen Chuang, Manoj Sachdev and Vincent Gaudet*
	A Novel Approach to Control Reconvergence Prediction *Walid J. Ghandour and Nadine J. Ghandour*
	Exploring Early & Late ALUs for Single-Issue In-Order Pipelines *Alen Bardizbanyan and Per Larsson-Edefors*
	Improving Memristor Memory with Sneak Current Sharing *Manjunath Shevgoor, Naveen Muralimanohar, Rajeev Balasubramonian and Yoocharn Jeon*
10:10-10:30	**Break** *Eisner & Lubin Auditorium, 4th Floor, Kimmel Center*
10:30-12:10	**TVS-3: Test Optimization** *406, Kimmel Center*
	Session Chair: Adit Singh, *Auburn University*
	A Novel TSV Probing Technique with Adhesive Test Interposer *Li Jiang, Xiangwei Huang, Hongfeng Xie, Qiang Xu, Chao Li, Xiaoyao Liang and Huiyun Li*
	A Methodology To Generate Evenly Distributed Input Stimuli By Clustering Of Variable Domain *Jomu George Mani Paret and Otmane Ait Mohamed*
	A Scan Chain Optimization Method for Diagnosis *Huajun Chen, Zichu Qi, Lin Wang and Chao Xu*
	A One-Pass Test-Selection Method for Maximizing Test Coverage *Cheng Xue and R. D. Shawn Blanton*
	Non-Enumerative Correlation-Aware Path Selection *Ahish Mysore Somashekar, Spyros Tragoudas and Rathish Jayabharathi*
12:10-13:30	**Lunch** *Eisner & Lubin Auditorium, 4th Floor, Kimmel Center*
13:30-15:10	**EDA-3: Improving Computational Efficiency of Circuit Analysis** *406, Kimmel Center*
	Session Chair: Tsung-Yi Ho, *National Cheng Kung University*
	3DCAM: A Low Overhead Crosstalk Avoidance Mechanism for TSV-Based 3D Ics *Reza Mirosanlou, Mohammadkazem Taram, Zahra Shirmohammadi and Seyed-Ghassem Miremadi*
	GPU Acceleration for PCA-Based Statistical Static Timing Analysis *Yiren Shen and Jiang Hu*
	Bottom-up disjoint-support decomposition based on cofactor and Boolean difference analysis *Vinicius Callegaro, Felipe Marranghello, Mayler Martins, Renato Ribas and Andre Reis*
	Optimized Local Control Strategy for Voice-based Interaction-tracking Badges for Social Applications *Xiaowei Liu, Alex Doboli and Fan Ye*
	FPGA-SPICE: A Simulation-based Power Estimation Framework for FPGAs *Xifan Tang, Pierre-Emmanuel Gaillardon and Giovanni De Micheli*
15:10-15:30	**Break** *Eisner & Lubin Auditorium, 4th Floor, Kimmel Center*
15:30-16:30	**Special Session 3: Reliable and Secure Mobile Cognition** *406, Kimmel Center*
	Session Chair: Karthik Swaminathan, *IBM T. J. Watson*
	Resilient Mobile Cognition: Algorithms,Innovations, and Architectures *R. Viguier, C-C. Lin, K. Swaminathan, A. Vega, A. Buyuktosunoglu, S. Pankanti, P. Bose, H. Akbarpour, F. Bunyak, K. Palaniappan, G. Seetharaman*
	A Testing Platform for On-drone Computation *Wang Zhou, Dhruv Nair, Oki Gunawan, Theodore van Kessel and Hendrik F. Hamann*
	Resilient, UAV-Embedded Real-Time Computing *Augusto Vega, Chung-Ching Lin, Karthik Swaminathan, Alper Buyuktosunoglu, Sharathchandra Pankanti and Pradip Bose*

Notes

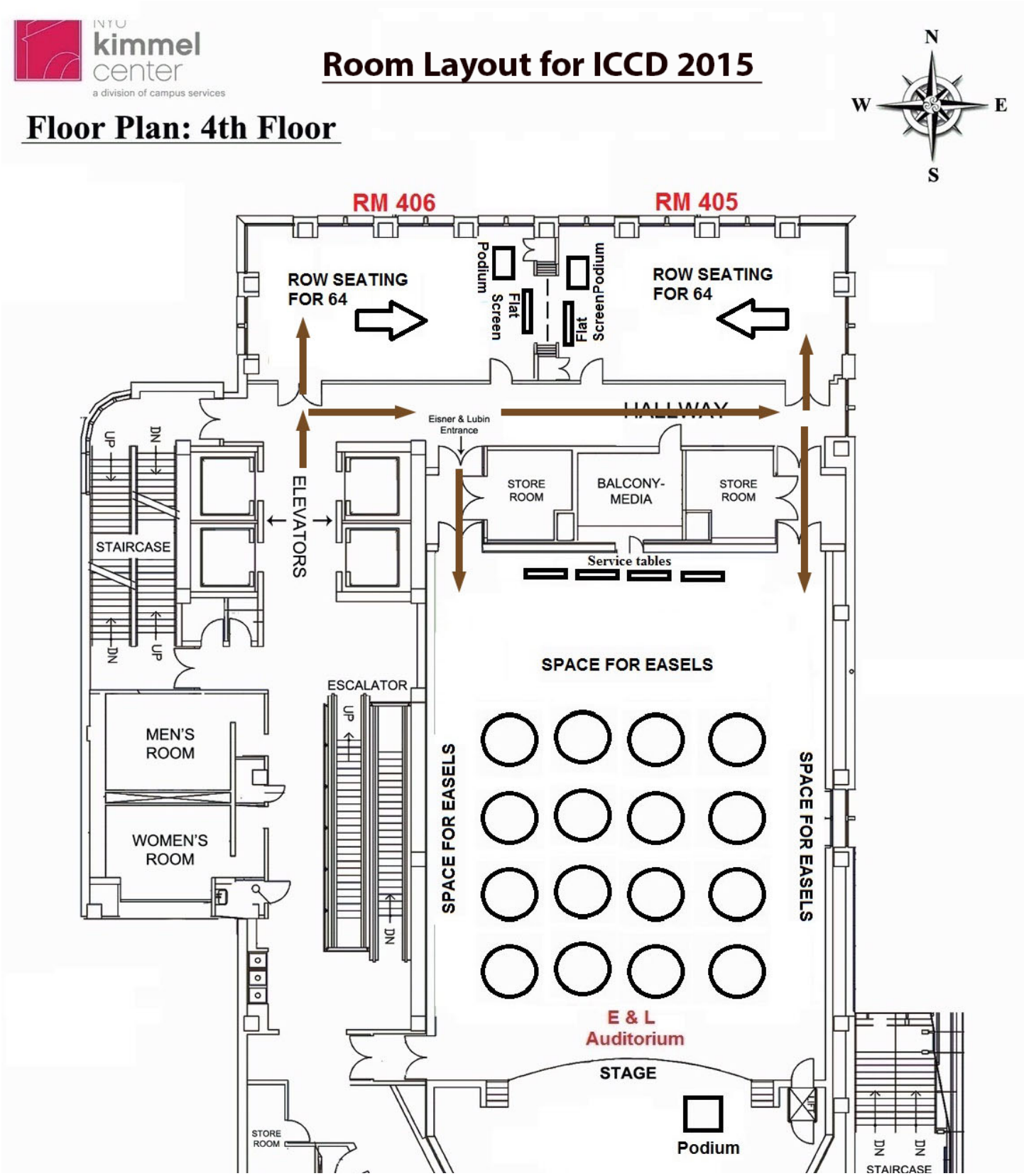
WEDNESDAY, OCTOBER 21, 2015

Session 3

IEEE Women in Engineering Workshop at ICCD 2015 *Eisner & Lubin Auditorium, 4th Floor, Kimmel Center*

13:00	Welcome remarks by Organizers Dr. Eren Kursun & Prof. Ann Gordon Ross	
13:00-13:45	 **Radha Ratnaparkhi** *Vice President IBM*	**Opening Speech** Radha Ratnaparkhi is currently the Vice President of Research Impact where she is building Research teams in strategic areas for IBM Research. Prior to this role Radha was the Vice President for Software Defined Environments where she led a world wide research team in the area of OpenStack based Hybrid Clouds. Her earlier roles include, being Vice President of IT and Wireless Convergence at IBM Research, Director of Commercial Systems, leadership of a high-end text analytics solution called WebFountain. Radha's experience at IBM also includes her development leadership effort for IBM's flagship database product DB2 on the mainframe. Prior to IBM, Radha was leading the Java products development team at Informix Software. She started her career in Mumbai, India with Tata Consultancy Services (TCS) – India's premier services consulting firm, after completing her Masters of Technology degree from the Indian Institute of Technology (IIT) in Delhi.
13:45-14:10	 **Professor Jun Yang** *University of Pittsburg*	Jun Yang received her PhD degree from the Computer Science Department, The University of Arizona. Prior to joining Pitt in Fall 2006, she was an assistant professor of Computer Science and Engineering at University of California, Riverside from 2002 to 2006. Dr. Yang has received a best paper award in ICCD 2007, and co-authored a paper that was nominated for best paper award in HPCA-15, 2009. Dr. Yang is a recipient of NSF CAREER award in 2008. She is a member of ACM and IEEE. Jun Yang's research interests include computer architecture, microprocessors, power and thermal management techniques, memory hierarchy, chip multiprocessors, network-on-chip, and 3D chip integration. Specifically, her recent projects have focused on emerging memory technologies, interconnection networks for many-core on chip, 3D integration, reliability, and power and thermal management for CMPs.
14:10-14:35	 **Dr. Mukta Farooq** *Global Foundries*	Mukta Farooq is a metallurgist/materials scientist, with over 27 years of experience and expertise in 3D integration and reliability, wafer thinning, die stacking, CMOS FET BEOL, C4 / BGA / CGA, lead-free alloys, chip package interaction and packaging technology. She is currently the 3D Technical Team Leader at Globalfoundries, NY. Prior to July 2015, she was Senior Technical Staff Member at IBM, and a founding member of IBM's 3D Technology Program. She led the development and technology qualification for 32SOI 3D memory controllers, resulting in volume shipment of 3D wafers for the Hybrid Memory Cube. She received an Outstanding Technical Innovation Award for her leadership in this technology. Mukta is an IBM Lifetime Master Inventor with over 180 issued US and international patents, was Chair of the IBM Master Inventor Program, and a member of the IBM Academy of Technology. She has 29 external publications, has given numerous invited talks at conferences and universities, and taught short courses at leading international conferences (IEEE IEDM, IEEE SOI-3D-SubVt and others). She has received numerous innovation and high value patent awards at IBM, which recognize her sustained contribution to both technology and intellectual property. Mukta is also very active in mentoring young professionals, especially women in technology fields. She has been an invited speaker at the South Asian Women's Leadership Forum and at events for Women in Technology. Mukta is an IEEE EDS Distinguished Lecturer, serves on the IEEE EDS Board of Governors and is the Northeast US Regional Editor of the EDS Newsletter. She is a founding member of the annual Semiconductor Technology Symposium, and Chair of the EDS Mid-Hudson Chapter which won the 2014 EDS Chapter of the Year Award. Mukta received her B. Tech from IIT Bombay, M. S. from Northwestern University, and Ph.D. from Rensselaer Polytechnic Institute.
14:35-15:00	 **Professor Sonia Lopez Alarcon** *Rochester Institute of Technology*	Sonia Lopez Alarcon was born in Madrid, Spain. She received a Bachelor of Physic degree in Physic and Master degree in Electronic in 2002 from the University Complutense of Madrid. In her latest college years she worked at Lucent Technologies, Madrid, and Fundetel at Polytechnic University of Madrid, were she became familiar with the design and fabrication process of integrated circuits. In 2003 she started working toward a PhD degree in Computer Engineering at the University Complutense of Madrid, working on cache hierarchy in simultaneous multithreaded architectures. In 2004 she started her cooperative research with Professor David H. Albonesi, at the University of Rochester and, later on, at Cornell University. She graduated in 2009, and she joined the Department of Computer Engineering at the Rochester Institute of Technology in the fall of 2009. Her current research interest is on cache optimization, GPU architecture, and heterogeneous hardware solutions. She's also actively involved with WE@RIT (Women in Engineering program at RIT) and in promoting inclusive engineering for women students and faculty in her college.
15:00-15:25	 **Professor Ulya Karpuzcu** *University of Minnesota*	Ulya R. Karpuzcu has been serving as an assistant professor at the Department of Electrical and Computer Engineering of University of Minnesota, Twin Cities, since Fall 2012. She received the Ph.D. and M.S. degrees in Electrical and Computer Engineering from University of Illinois, Urbana-Champaign. She is a Fulbright scholar. Her research focuses on the impact of process technology on computer architecture, with the current emphasis being on boosting the energy efficiency of computing.
15:25-16:00	Panel Session, Q&A	

KIMMEL CENTER FLOOR PLAN

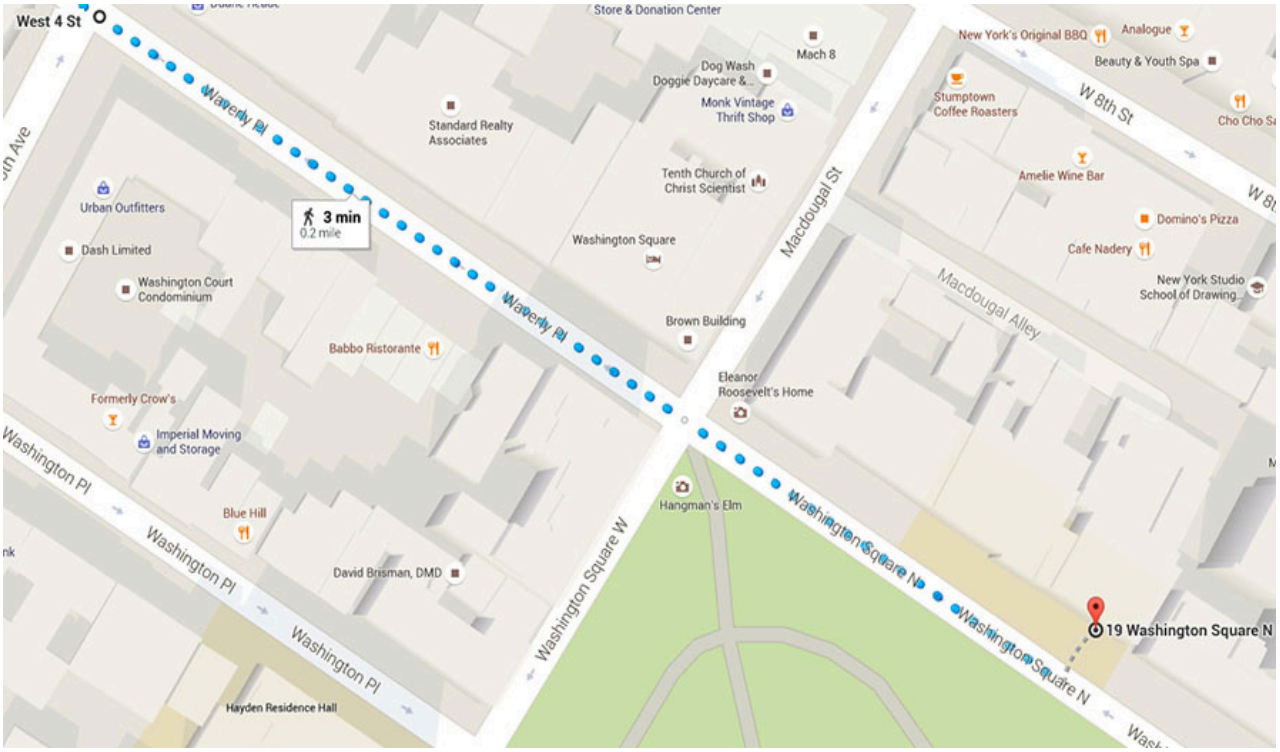


Path From Elevators to Rooms

SUNDAY, OCTOBER 18, 2015

14:00-15:30	**Tutorial 1: Synthesis and Verification of Arithmetic Circuits** *19, Washington Square North, New York*	
	Organizers	Luca Amaru, *EPFL*, Maciej Ciesielski, *University of Massachusetts, Amherst*, Pierre-Emmanuel Gaillardon, *EPFL* and Giovanni De Micheli, *EPFL*
	Speakers	Luca Amaru, *EPFL* and Maciej Ciesielski, *University of Massachusetts, Amherst*
15:30-15:45	**Break**	
15:45-17:30	**Tutorial 2: Sigil and SynchroTrace: Communication-Aware Workload Profiling and Memory-NoC Simulation** *19, Washington Square North, New York*	
	Organizers	Mark Hempstead, *Tufts University* and Baris Taskin, *Drexel University*
	Speakers	Baris Taskin, *Drexel University*, Mark Hempstead, *Tufts University* and Michael Lui, *Drexel University*, Stephan Diestelhorst, *ARM Research*
18:00-19:00	**Reception** *Saadiyat Room*	

From West 4 Station (A, B, C, D, E, F, M) to 19, Washington Square North, New York



Map - Subway Station to Kimmel Center

From West 4 Station (A, B, C, D, E, F, M) to Kimmel Center

From Astor Station (6) & 8 St. NYU Station (R) to Kimmel Center