Final Project Report First Page. Must match this format (Title)

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Delay (ns to run provided provided example). 31,290 Clock period: 35ns # cycles": 894 cycles	Logic Area: (um^2) 29092.4203 Memory: N/A	1/(delay.area) ($ns^{-1}.um^{-2}$) 1/(Clk_per*cycle*logic) 1/(35*894*29092.4203) = 9.859E-10 ($ns^{-1}.um^{-2}$)
Delay (TA provided example. TA to complete)		1/(delay.area) (TA)

Abstract

The quantum computing emulator performs matrix multiplication of real numbers with a set number of qubits. Given an input of an initial state vector matrix and operator matrices the emulator will output a final state vector matrix that represents the result of matrix multiplication. The DUT (device under test) will communicate with multiple SRAMs to receive signals and matrices used in the simulation. The DUT will write back the final state vector matrix and their addresses to the SRAM and send a signal indicating the DUT is ready to perform another calculation.

The emulator was implemented with a top module using a finite state machine (FSM) for the control path paired with many muxes and registers used to store and manipulate the signals in the data path. Within the top module, a floating-point multiply-and-add (DW_fp_mac) module was used to perform floating-point multiplication for the elements within and between matrices.

The emulator outputs correct results, verified by the testbench used. Slack is met on all timing reports when ran with a 35 ns clock period. The area achieved is 29092.4203 um^2.

ECE 464 – Quantum Computing Emulator

Jack Maxwell

1. Introduction

A quantum computing emulator has been designed to perform matrix multiplication of real numbers. Given an input of an initial state vector matrix and operator matrices the emulator will output a final state vector matrix that represents the result of matrix multiplication.

The emulator outputs correct results, verified by the testbench used. Slack is met on all timing reports when ran with a 35 ns clock period. The area achieved is 29092.4203 um^2.

This report will give an in-depth analysis of the micro-architecture, interface specification, technical implementation, verification process, and results achieved.

2. Micro-Architecture

Two modules were used to implement the emulator. The main module, named "MyDesign", contained the control path consisting of a 15 state FSM, and a data path consisting of functional blocks including registers, multiplexors, counters, and adders. This module was used to manipulate the data signals received from and sent to the SRAM. MyDesign sends the SRAMs addresses, receives the data from the respective addresses sent, and either stores the data in registers for later manipulation, or passes the data received to the instanced second module for matrix multiplication.

A second module, DW_fp_mac, was used inside the main module. This module was instanced once in the main module and has a function of floating-point multiply-and-add. This module was used solely for matrix multiplication.

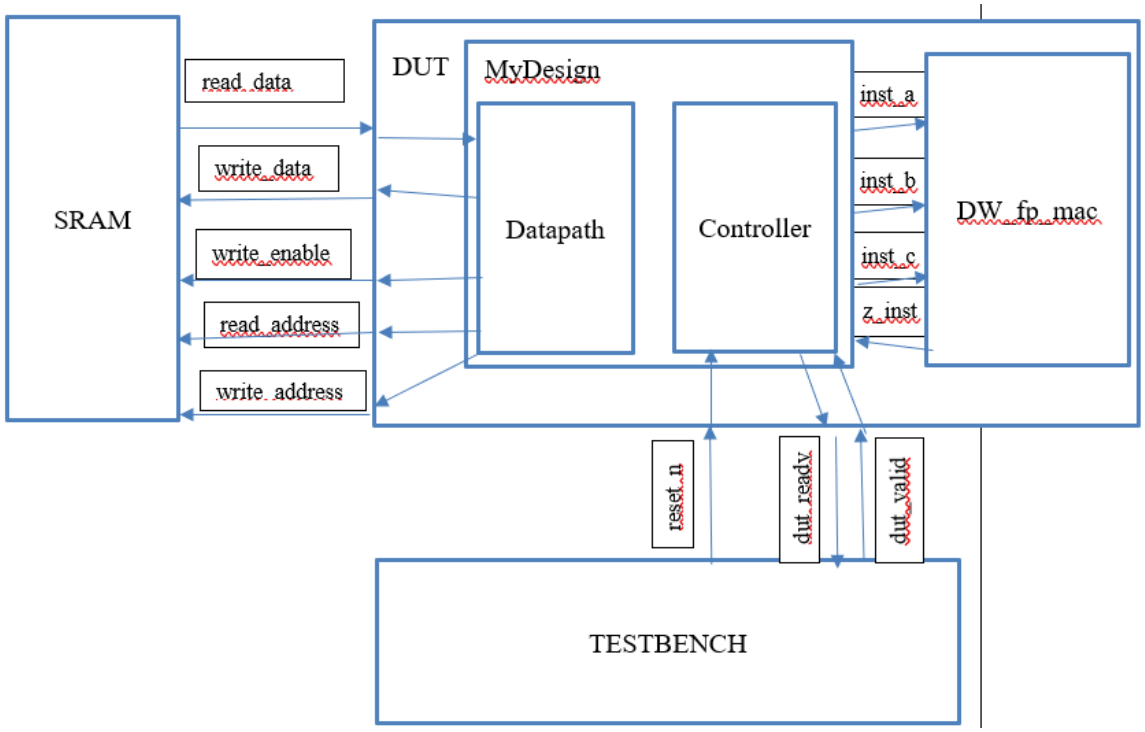


Figure 1: High Level Diagram

3. Interface Specification

To begin a simulation, the testbench or another connected device will produce a dut_valid signal. The dut_valid signal indicates there is another calculation needed to be performed.

Once the dut_valid signal goes high, the DUT will put the dut_ready signal low, indicating a calculation is in progress. The DUT then performs the matrix multiplication and sets the q_state_output_sram_write_enable signal high in order to write the output back to the q_state_output SRAM. While this signal is high, the q_state_output_sram_write_address is incremented in parallel with each data that is written back over q_state_output_sram_write_data output. Once all elements of the final computation have been written back to the q_state_output SRAM, the write enable signal goes low again, and the dut_ready goes high, signalling the DUT is ready for a new calculation.

Each SRAM has 4 inputs and an output. The 4 inputs include a write_enable, write_address, write_data, and read_address. The output signal is read_data. In order to write new data to a SRAM, the write_enable needs to be set high. Once high, data can be sent over the write_data signal paired with a write_address signal. The SRAM will then store the data at the respective address in memory. The SRAM also outputs data stored at a certain address in memory when a memory request is sent over read_address. The data stored at the read_address signal is output over the read_data signal.

Device	Signal	Width	Direction (in relation to the DUT)	Function
Test Fixture -> DUT	reset_n	1 bit	input	resets DUT into a known state
Test Fixture -> DUT	clk	1 bit	input	clock from the test fixture
Test Fixture -> DUT	dut_valid	1 bit	input	Signals that a valid input can be computed from the SRAM
DUT -> Test Fixture	dut_ready	1 bit	output	Signals that the DUT is ready to do its computation. DUT should hold the dut_ready low when a dut_valid high is detected until it has fully populated the result value back in the q_state_output SRAM.
DUT -> SRAM	q_state_input_sram_write_enable	1bit	output	Signals the DUT wants to write to the q_state_input SRAM memory
DUT -> SRAM	q_state_input_sram_write_address	32 bits	output	signal containing SRAM memory address to store write_data signal
DUT -> SRAM	q_state_input_sram_write_data	128 bits	output	output memory data sent to the q_state_input SRAM for stoarge
DUT -> SRAM	q_state_input_sram_read_address	32 bits	output	signal containing SRAM memory address of data needed to be sent to the DUT through read_data
SRAM -> DUT	q_state_input_sram_read_data	128 bits	input	input memory data from the q_state_input SRAM
DUT -> SRAM	q_state_output_sram_write_enable	1bit	output	Signals the DUT wants to write to the q_state_output SRAM memory
DUT -> SRAM	q_state_output_sram_write_address	32 bits	output	signal containing SRAM memory address to store write_data signal
DUT -> SRAM	q_state_output_sram_write_data	128 bits	output	output memory data sent to the q_state_output SRAM for stoarge
DUT -> SRAM	q_state_output_sram_read_address	32 bits	output	signal containing SRAM memory address of data needed to be sent to the DUT through read_data
SRAM -> DUT	q_state_output_sram_read_data	128 bits	input	input memory data from the q_state_output SRAM
DUT -> SRAM	q_gates_sram_write_enable	1bit	output	Signals the DUT wants to write to the q_gates SRAM memory
DUT -> SRAM	q_gates_sram_write_address	32 bits	output	signal containing SRAM memory address to store write_data signal
DUT -> SRAM	q_gates_sram_write_data	128 bits	output	output memory data sent to the q_gatesSRAM for stoarge
DUT -> SRAM	q_gates_sram_read_address	32 bits	output	signal containing SRAM memory address of data needed to be sent to the DUT through read_data
SRAM -> DUT	q_gates_sram_read_data	128 bits	input	input memory data from the q_gates SRAM
DUT -> SRAM	scratchpad_sram_write_enable	1bit	output	Signals the DUT wants to write to the scratchpad SRAM memory
DUT -> SRAM	scratchpad_sram_write_address	32 bits	output	signal containing SRAM memory address to store write_data signal
DUT -> SRAM	scratchpad_sram_write_data	128 bits	output	output memory data sent to the scratchpad SRAM for stoarge
DUT -> SRAM	scratchpad_sram_read_address	32 bits	output	signal containing SRAM memory address of data needed to be sent to the DUT through read_data
SRAM -> DUT	scratchpad_sram_read_data	128 bits	input	input memory data from the scratchpad SRAM

Figure 2: Signals Table

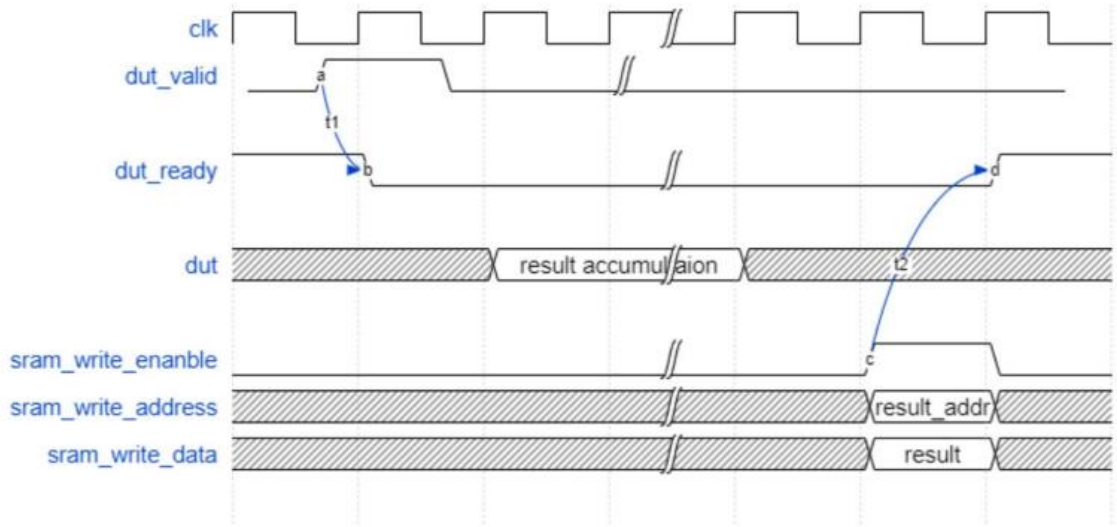


Figure 3: Top Level Interface Timing Diagram

4. Technical Implementation

- Discussion of high level modeling (if used) and results achieved

No true hierarchal design was used for this implementation, as only two independent modules were used to create the emulator. The testbench, however, had a hierarchal design.

There were two modules used in the emulator implementation. The main module contained the data path and control path. The second module, which was instanced in the main module, was a DW_fp_mac module used for multiplication accumulation. Within the testbench created, there were 4 instances of an SRAM module within the testbench code.

5. Verification

A testbench was created to verify correctness of the emulator with 2 different simulation tests. The testbench had two different data sets used for different simulations. The first simulation had 4 different calculations sent to the DUT and 16 tests that needed to be passed. The second simulation had 8 calculations with 32 tests.

Within the test bench, there were 4 instances of an SRAM module for simulation. 2 of the SRAMs contained data used in the simulation and output the data when given a memory address from the DUT. The third SRAM received and stored the final state vector matrix and its elements' addresses from the DUT. The fourth SRAM is used to offload unused memory to reduce area.

6. Results Achieved

The emulator was simulated with a clock period of 35 ns. All 16 tests passed on the first testbench simulation, and all 32 tests passed on the second testbench simulation.

Slack was met on all three reports (timing_max_slow_hold, timing_min_fast_check, and timing_max_slow) by at least 0.0218 ns. With a clock period of 35 ns, the logic area achieved was 29092.4203 um^2.

7. Conclusions

In this project, a quantum computing emulator was designed and implemented. The emulator performed matrix multiplication of real numbers. Given an input of an initial state vector matrix and operator matrices the emulator will output a final state vector matrix that represents the result of matrix multiplication.

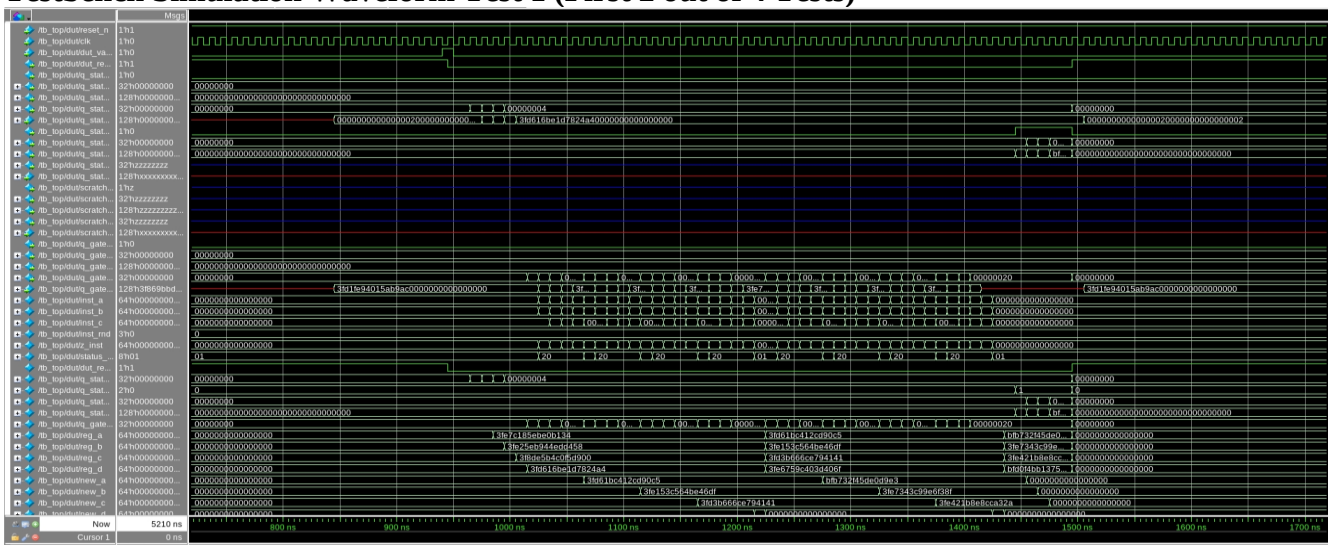
The emulator performs and outputs correct calculations, as verified by the testbench through two different simulations.

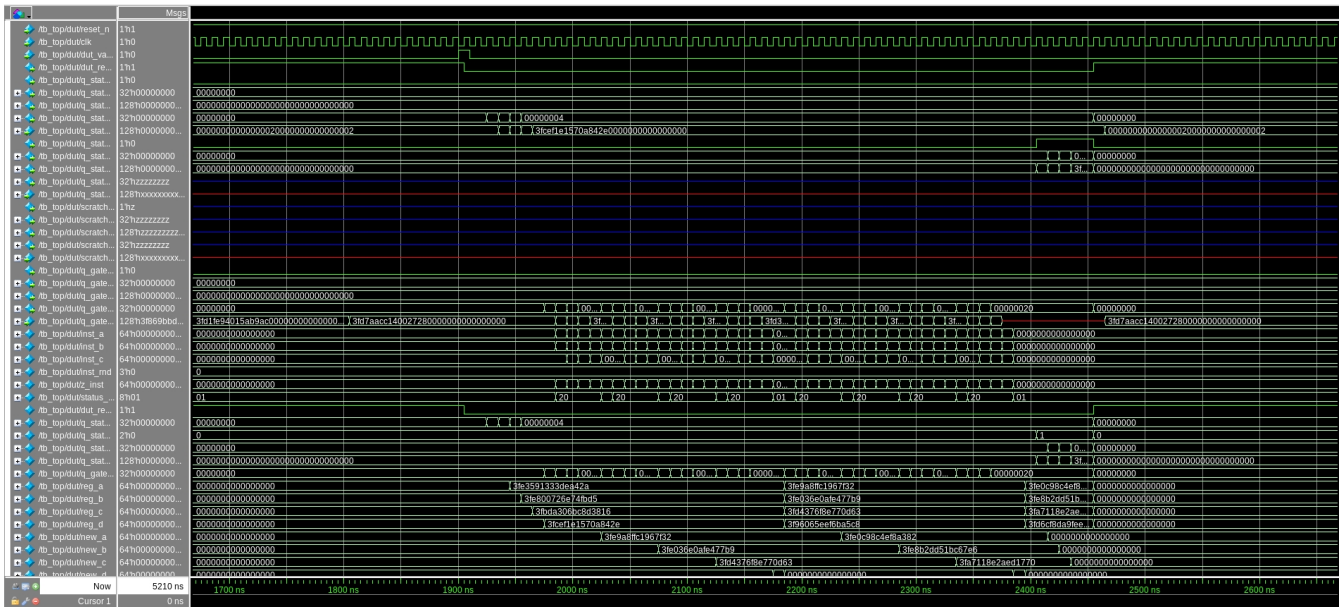
With a clock period of 35 nanoseconds, the emulator had a logic area of 29092.4203 $um^{2.}$ Slack was met on all constraints and there were no errors when synthesized.

Testbench Simulation Output Log Test 1

```
# //  ModelSim SE 2021.2 Apr 14 2021 Linux 3.10.0-1160.102.1.el7.x86_64
# //  ModelSim SE and its associated documentation contain trade
# //  secrets and commercial or financial information that are the property of
# //  Mentor Graphics Corporation and are privileged, confidential,
# //  and exempt from disclosure under the Freedom of Information Act,
# //  5 U.S.C. Section 552. Furthermore, this information
# //  is prohibited from disclosure under the Trade Secrets Act,
# //  18 U.S.C. Section 1905.
# //
# vsim -voptargs="+acc" tb_top "+TIMEOUT=1000000000" "+num_of_testcases=4" "+epsilon_mult=3.0" "+input_dir=../inputs/input1"
"+output_dir=../inputs/output1"
# Start time: 15:42:38 on Nov 14,2023
# ** Note: (vsim-3813) Design is being optimized due to module recompilation...
# ** Note: (vopt-143) Recognized 1 FSM in module "MyDesign(fast)".
# Loading sv_std.std
# Loading work.tb_top(fast)
# Loading work.sram(fast)
# Loading work.sram(fast__1)
# Loading work.sram(fast__2)
# Loading work.MyDesign(fast)
# Loading work.DW_fp_mac_inst(fast)
# Loading work.DW_fp_mac(fast)
# Loading work.DW_fp_dp2(fast)
log -r *
run 20000ns
# INFO: number of testcases:          4
# +CLASS+464
# INFO: DONE WITH RESETING DUT
# INFO: ######## Running Test: 1 ########
# INFO: Reading memory file: ../inputs/input1/test1_B.dat
# INFO: Reading memory file: ../inputs/input1/test1_A.dat
# INFO: reading ../inputs/output1/test1_C.dat
# INFO: Number of cases       : 4
# INFO: Number of passed cases : 4
# INFO: presentage passed     :  100.00
# INFO: Test: 1, Result:  100.00
#
# INFO: ######## Running Test: 2 ########
# INFO: Reading memory file: ../inputs/input1/test2_B.dat
# INFO: Reading memory file: ../inputs/input1/test2_A.dat
# INFO: reading ../inputs/output1/test2_C.dat
# INFO: Number of cases       : 4
# INFO: Number of passed cases : 4
# INFO: presentage passed     :  100.00
# INFO: Test: 2, Result:  100.00
#
# INFO: ######## Running Test: 3 ########
# INFO: Reading memory file: ../inputs/input1/test3_B.dat
# INFO: Reading memory file: ../inputs/input1/test3_A.dat
# INFO: reading ../inputs/output1/test3_C.dat
# INFO: Number of cases       : 4
# INFO: Number of passed cases : 4
# INFO: presentage passed     :  100.00
# INFO: Test: 3, Result:  100.00
#
# INFO: ######## Running Test: 4 ########
# INFO: Reading memory file: ../inputs/input1/test4_B.dat
# INFO: Reading memory file: ../inputs/input1/test4_A.dat
# INFO: reading ../inputs/output1/test4_C.dat
# INFO: Number of cases       : 4
# INFO: Number of passed cases : 4
# INFO: presentage passed     :  100.00
# INFO: Test: 4, Result:  100.00
#
# INFO: Total number of cases  : 16
# INFO: Total number of passes : 16
# INFO: Finial Results        : 100.00
# INFO: Finial Time Result    : 4470 ns
# INFO: Finial Cycle Result   : 894 cycles
#
# ** Note: $finish    : ../testbench/testbench.sv(348)
#    Time: 5210 ns  Iteration: 1  Instance: /tb_top
# 1
# Break in Module tb_top at ../testbench/testbench.sv line 348
# End time: 15:43:12 on Nov 14,2023, Elapsed time: 0:00:34
# Errors: 0, Warnings: 0
```

Testbench Simulation Waveform Test 1 (First 2 out of 4 Tests)

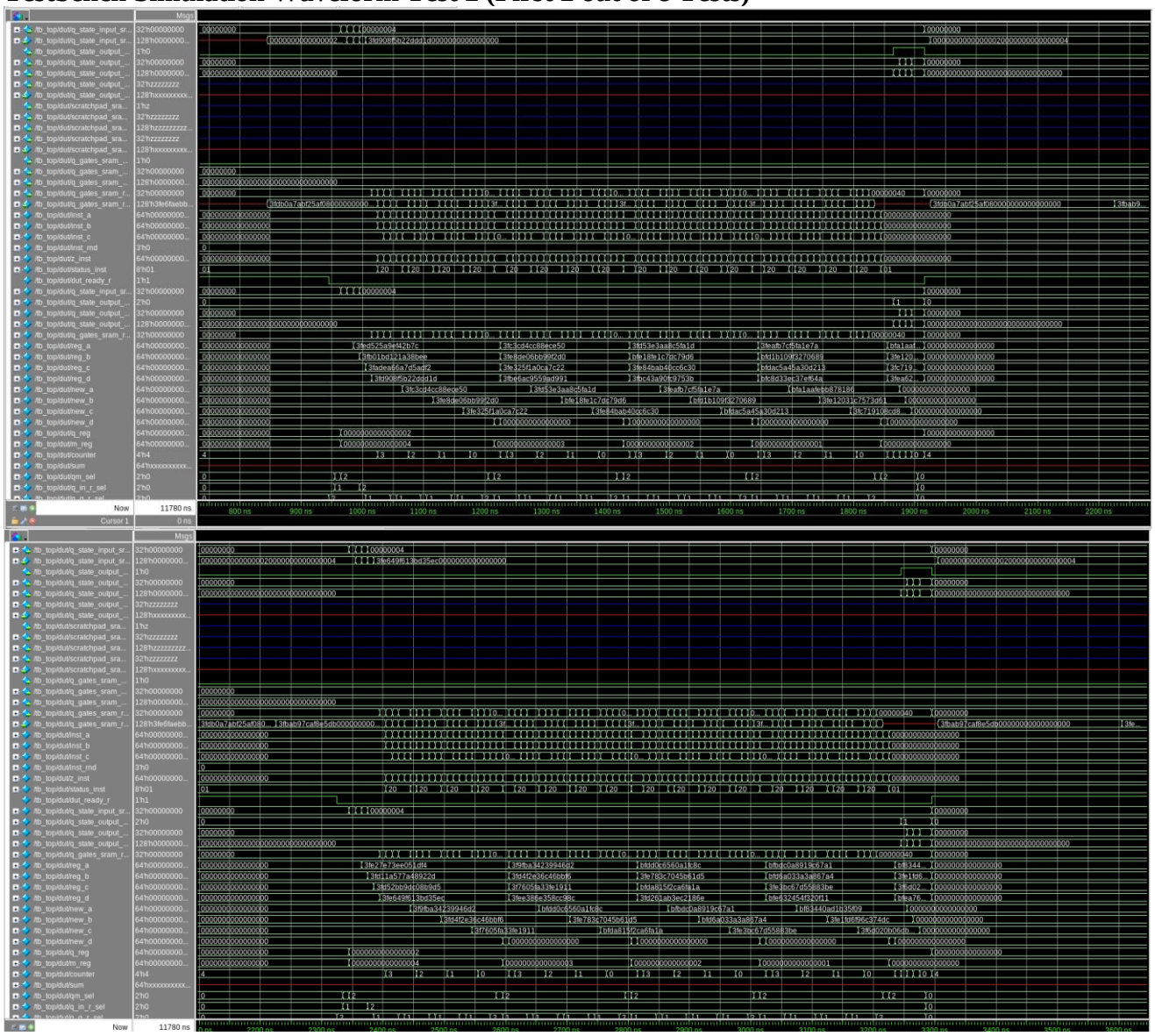




Testbench Simulation Output Log Test 2

```
# INFO: number of testcases:           8
# +CLASS+464
# INFO: DONE WITH RESETING DUT
# INFO: ######## Running Test: 1 ########
# INFO: Reading memory file: ../inputs/input2/test1_B.dat
# INFO: Reading memory file: ../inputs/input2/test1_A.dat
# INFO: reading ../inputs/output2/test1_C.dat
# INFO: Number of cases       : 4
# INFO: Number of passed cases : 4
# INFO: presentage passed     :  100.00
# INFO: Test: 1, Result:  100.00
# INFO: ######## Running Test: 2 ########
# INFO: Reading memory file: ../inputs/input2/test2_B.dat
# INFO: Reading memory file: ../inputs/input2/test2_A.dat
# INFO: reading ../inputs/output2/test2_C.dat
# INFO: Number of cases       : 4
# INFO: Number of passed cases : 4
# INFO: presentage passed     :  100.00
# INFO: Test: 2, Result:  100.00
# INFO: ######## Running Test: 3 ########
# INFO: Reading memory file: ../inputs/input2/test3_B.dat
# INFO: Reading memory file: ../inputs/input2/test3_A.dat
# INFO: reading ../inputs/output2/test3_C.dat
# INFO: Number of cases       : 4
# INFO: Number of passed cases : 4
# INFO: presentage passed     :  100.00
# INFO: Test: 3, Result:  100.00
# INFO: ######## Running Test: 4 ########
# INFO: Reading memory file: ../inputs/input2/test4_B.dat
# INFO: Reading memory file: ../inputs/input2/test4_A.dat
# INFO: reading ../inputs/output2/test4_C.dat
# INFO: Number of cases       : 4
# INFO: Number of passed cases : 4
# INFO: presentage passed     :  100.00
# INFO: Test: 4, Result:  100.00
# INFO: ######## Running Test: 5 ########
# INFO: Reading memory file: ../inputs/input2/test5_B.dat
# INFO: Reading memory file: ../inputs/input2/test5_A.dat
# INFO: reading ../inputs/output2/test5_C.dat
# INFO: Number of cases       : 4
# INFO: Number of passed cases : 4
# INFO: presentage passed     :  100.00
# INFO: Test: 5, Result:  100.00
# INFO: ######## Running Test: 6 ########
# INFO: Reading memory file: ../inputs/input2/test6_B.dat
# INFO: Reading memory file: ../inputs/input2/test6_A.dat
# INFO: reading ../inputs/output2/test6_C.dat
# INFO: Number of cases       : 4
# INFO: Number of passed cases : 4
# INFO: presentage passed     :  100.00
# INFO: Test: 6, Result:  100.00
# INFO: ######## Running Test: 7 ########
# INFO: Reading memory file: ../inputs/input2/test7_B.dat
# INFO: Reading memory file: ../inputs/input2/test7_A.dat
# INFO: reading ../inputs/output2/test7_C.dat
# INFO: Number of cases       : 4
# INFO: Number of passed cases : 4
# INFO: presentage passed     :  100.00
# INFO: Test: 7, Result:  100.00
# INFO: ######## Running Test: 8 ########
# INFO: Reading memory file: ../inputs/input2/test8_B.dat
# INFO: Reading memory file: ../inputs/input2/test8_A.dat
# INFO: reading ../inputs/output2/test8_C.dat
# INFO: Number of cases       : 4
# INFO: Number of passed cases : 4
# INFO: presentage passed     :  100.00
# INFO: Test: 8, Result:  100.00
# INFO: Total number of cases  : 32
# INFO: Total number of passes : 32
# INFO: Finial Results        : 100.00
# INFO: Finial Time Result    : 11040 ns
# INFO: Finial Cycle Result   : 2208 cycles
# ** Note: $finish    : ../testbench/testbench.sv(348)
#    Time: 11780 ns  Iteration: 1  Instance: /tb_top
```

Testbench Simulation Waveform Test 2 (First 2 out of 8 Tests)



Timing_Max_Slow

Information: Updating design information... (UID-85)

```
****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : MyDesign
Version: T-2022.03-SP4
Date   : Thu Nov 16 10:47:41 2023
****************************************

Operating Conditions: slow   Library: NangateOpenCellLibrary_PDKv1_2_v2008_10_slow_nldm
Wire Load Model Mode: top

  Startpoint: inst_c_reg[23]
              (rising edge-triggered flip-flop clocked by clk)
  Endpoint: new_c_reg[62]
            (rising edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: max

  Point                                    Incr       Path
  -----------------------------------------------------------
  clock clk (rise edge)                  0.0000     0.0000
  clock network delay (ideal)            0.0000     0.0000
  inst_c_reg[23]/CK (DFF_X1)             0.0000     0.0000 r
  inst_c_reg[23]/Q (DFF_X1)              0.6206     0.6206 f
  U5826/ZN (NOR2_X1)                     0.2195     0.8401 r
  U5827/ZN (NAND3_X1)                    0.0898     0.9299 f
  U5828/ZN (NOR2_X1)                     0.2065     1.1364 r
  U3016/ZN (AND4_X1)                     0.2379     1.3744 r
  U3002/ZN (AND3_X1)                     0.2366     1.6109 r
  U5858/ZN (NOR2_X1)                     0.0850     1.6960 f
  U2994/ZN (INV_X1)                      0.2716     1.9676 r
  U6018/S (FA_X1)                        0.7498     2.7173 f
  U6050/CO (FA_X1)                       0.5161     3.2334 f
  U6054/CO (FA_X1)                       0.5172     3.7507 f
  U6062/CO (FA_X1)                       0.5172     4.2679 f
  U6067/CO (FA_X1)                       0.5172     4.7851 f
  U6100/CO (FA_X1)                       0.5172     5.3024 f
  U6046/CO (FA_X1)                       0.5172     5.8196 f
  U6031/CO (FA_X1)                       0.4882     6.3078 f
  U6032/Z (XOR2_X1)                      0.2828     6.5907 r
  U6035/ZN (NAND2_X1)                    0.0972     6.6879 f
  U6036/ZN (NOR2_X1)                     0.4514     7.1392 r
  U6041/ZN (NOR2_X1)                     0.1254     7.2646 f
  U8331/ZN (INV_X1)                      0.1028     7.3675 r
  U8332/ZN (NOR2_X1)                     0.0807     7.4482 f
  U8333/ZN (INV_X4)                      0.3591     7.8072 r
  U8334/ZN (OR2_X2)                      0.4414     8.2487 r
  U4196/ZN (OR2_X1)                      0.6477     8.8963 r
  U4200/ZN (INV_X1)                      0.3046     9.2009 f
  U10232/ZN (AOI22_X1)                   0.5098     9.7107 r
  U10234/ZN (OAI211_X1)                  0.2500     9.9607 f
  U10412/S (FA_X1)                       0.6925    10.6532 f
  U10414/ZN (NOR2_X1)                    0.2489    10.9021 r
  U10964/ZN (OAI21_X1)                   0.1284    11.0304 f
  U10965/ZN (AOI21_X1)                   0.3050    11.3354 r
  U10966/ZN (OAI21_X1)                   0.1314    11.4668 f
  U10967/ZN (AOI21_X1)                   0.3788    11.8456 r
  U10968/ZN (OAI21_X1)                   0.1831    12.0287 f
  U10979/ZN (AOI21_X1)                   0.2448    12.2735 r
  U11831/ZN (OAI21_X1)                   0.1445    12.4179 f
  U2321/ZN (AOI21_X2)                    0.3252    12.7431 r
  U12582/ZN (OAI21_X1)                   0.1410    12.8841 f
  U12601/ZN (AOI21_X1)                   0.2889    13.1730 r
  U12607/ZN (OAI21_X1)                   0.1847    13.3577 f
  U2333/ZN (AOI21_X2)                    0.2143    13.5719 r
  U2334/ZN (INV_X4)                      0.0562    13.6281 f
  U12631/CO (FA_X1)                      0.4832    14.1113 f
  U12639/CO (FA_X1)                      0.5172    14.6286 f
  U12649/CO (FA_X1)                      0.5241    15.1527 f
  U2308/ZN (NAND2_X2)                    0.1339    15.2866 r
  U2306/ZN (NAND2_X2)                    0.0717    15.3583 f
  U12659/CO (FA_X1)                      0.4800    15.8383 f
  U12661/CO (FA_X1)                      0.4850    16.3233 f
  U12663/ZN (XNOR2_X1)                   0.4161    16.7394 r
```

U2323/ZN (INV_X4) 0.1070 16.8464 f
U12664/ZN (XNOR2_X1) 0.2699 17.1163 f
U12665/ZN (NOR2_X1) 0.2422 17.3586 r
U12666/ZN (NAND2_X1) 0.1124 17.4710 f
U13065/ZN (AOI21_X1) 0.3692 17.8402 r
U13066/ZN (OAI21_X1) 0.1714 18.0116 f
U13067/ZN (AOI21_X1) 0.3749 18.3865 r
U13068/ZN (OAI21_X1) 0.2594 18.6459 f
U2442/ZN (INV_X1) 0.5521 19.1981 r
U2693/ZN (OR2_X2) 0.2495 19.4475 r
U13427/ZN (NAND2_X1) 0.0696 19.5172 f
U13428/ZN (XNOR2_X1) 0.4698 19.9869 r
U2685/ZN (INV_X1) 0.1496 20.1366 f
U13429/S (FA_X1) 0.7073 20.8439 f
U13449/CO (FA_X1) 0.6179 21.4618 f
U13448/CO (FA_X1) 0.6017 22.0635 f
U13447/CO (FA_X1) 0.5172 22.5808 f
U13446/CO (FA_X1) 0.5172 23.0980 f
U13444/CO (FA_X1) 0.5238 23.6218 f
U2376/ZN (NAND2_X1) 0.2115 23.8333 r
U2324/ZN (NAND3_X2) 0.1172 23.9505 f
U13442/CO (FA_X1) 0.4889 24.4394 f
U13441/CO (FA_X1) 0.5172 24.9566 f
U13486/S (FA_X1) 0.7806 25.7372 r
U2304/ZN (NOR2_X2) 0.0976 25.8348 f
U13483/ZN (NOR2_X1) 0.3711 26.2059 r
U2675/ZN (INV_X1) 0.1048 26.3106 f
U13574/ZN (OAI21_X1) 0.4105 26.7211 r
U2302/ZN (INV_X4) 0.0309 26.7520 f
U2289/ZN (OAI21_X1) 0.4194 27.1714 r
U3614/ZN (NAND2_X2) 0.3186 27.4900 f
U4816/ZN (INV_X1) 0.6378 28.1278 r
U4589/ZN (AND2_X1) 0.6655 28.7933 r
U2662/ZN (INV_X1) 0.1480 28.9413 f
U4573/ZN (OR2_X1) 0.3206 29.2619 f
U16758/ZN (NAND3_X1) 0.3137 29.5756 r
U16759/ZN (NAND2_X1) 0.1065 29.6821 f
U2605/ZN (AND4_X1) 0.4300 30.1120 f
U2588/ZN (OR2_X1) 0.2119 30.3239 f
U2580/ZN (AND2_X2) 0.2065 30.5304 f
U17546/ZN (NAND3_X1) 0.1105 30.6409 r
U17547/ZN (NOR2_X1) 0.0966 30.7374 f
U17548/ZN (AND3_X1) 0.2914 31.0288 f
U2539/ZN (AND4_X1) 0.3804 31.4092 f
U2536/ZN (AND3_X1) 0.2666 31.6758 f
U17666/ZN (AOI21_X1) 0.3045 31.9803 r
U2535/ZN (AND3_X1) 0.5814 32.5617 r
U18023/ZN (AOI21_X1) 0.1754 32.7370 f
U18024/Z (XOR2_X1) 0.3958 33.1328 f
U4691/ZN (OR2_X1) 0.2160 33.3488 f
U18070/ZN (AOI22_X1) 0.4345 33.7833 r
U18074/ZN (OAI22_X1) 0.2170 34.0002 f
new_c_reg[62]/D (DFF_X1) 0.0000 34.0002 f
data arrival time 34.0002

clock clk (rise edge) 35.0000 35.0000
clock network delay (ideal) 0.0000 35.0000
clock uncertainty -0.0500 34.9500
new_c_reg[62]/CK (DFF_X1) 0.0000 34.9500 r
library setup time -0.3584 34.5916
data required time 34.5916
---
data required time 34.5916
data arrival time -34.0002
---
slack (MET) 0.5914

Timing_Max_SlowHoldFixed_Tut1

```
****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : MyDesign
Version: T-2022.03-SP4
Date   : Thu Nov 16 10:47:59 2023
****************************************

Operating Conditions: slow   Library: NangateOpenCellLibrary_PDKv1_2_v2008_10_slow_nldm
Wire Load Model Mode: top

  Startpoint: inst_c_reg[23]
              (rising edge-triggered flip-flop clocked by clk)
  Endpoint: new_c_reg[62]
            (rising edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: max

  Point                                   Incr       Path
  -----------------------------------------------------------
  clock clk (rise edge)                   0.0000     0.0000
  clock network delay (ideal)             0.0000     0.0000
  inst_c_reg[23]/CK (DFF_X1)              0.0000     0.0000 r
  inst_c_reg[23]/Q (DFF_X1)               0.6206     0.6206 f
  U5826/ZN (NOR2_X1)                      0.2195     0.8401 r
  U5827/ZN (NAND3_X1)                     0.0898     0.9299 f
  U5828/ZN (NOR2_X1)                      0.2065     1.1364 r
  U3016/ZN (AND4_X1)                      0.2379     1.3744 r
  U3002/ZN (AND3_X1)                      0.2366     1.6109 r
  U5858/ZN (NOR2_X1)                      0.0850     1.6960 f
  U2994/ZN (INV_X1)                       0.2716     1.9676 r
  U6018/S (FA_X1)                         0.7498     2.7173 f
  U6050/CO (FA_X1)                        0.5161     3.2334 f
  U6054/CO (FA_X1)                        0.5172     3.7507 f
  U6062/CO (FA_X1)                        0.5172     4.2679 f
  U6067/CO (FA_X1)                        0.5172     4.7851 f
  U6100/CO (FA_X1)                        0.5172     5.3024 f
  U6046/CO (FA_X1)                        0.5172     5.8196 f
  U6031/CO (FA_X1)                        0.4882     6.3078 f
  U6032/Z (XOR2_X1)                       0.2828     6.5907 r
  U6035/ZN (NAND2_X1)                     0.0972     6.6879 f
  U6036/ZN (NOR2_X1)                      0.4514     7.1392 r
  U6041/ZN (NOR2_X1)                      0.1254     7.2646 f
  U8331/ZN (INV_X1)                       0.1028     7.3675 r
  U8332/ZN (NOR2_X1)                      0.0807     7.4482 f
  U8333/ZN (INV_X4)                       0.3591     7.8072 r
  U8334/ZN (OR2_X2)                       0.4414     8.2487 r
  U4196/ZN (OR2_X1)                       0.6477     8.8963 r
  U4200/ZN (INV_X1)                       0.3046     9.2009 f
  U10232/ZN (AOI22_X1)                    0.5098     9.7107 r
  U10234/ZN (OAI211_X1)                   0.2500     9.9607 f
  U10412/S (FA_X1)                        0.6925    10.6532 f
  U10414/ZN (NOR2_X1)                     0.2489    10.9021 r
  U10964/ZN (OAI21_X1)                    0.1284    11.0304 f
  U10965/ZN (AOI21_X1)                    0.3050    11.3354 r
  U10966/ZN (OAI21_X1)                    0.1314    11.4668 f
  U10967/ZN (AOI21_X1)                    0.3788    11.8456 r
  U10968/ZN (OAI21_X1)                    0.1831    12.0287 f
  U10979/ZN (AOI21_X1)                    0.2448    12.2735 r
  U11831/ZN (OAI21_X1)                    0.1445    12.4179 f
  U2321/ZN (AOI21_X2)                     0.3252    12.7431 r
  U12582/ZN (OAI21_X1)                    0.1410    12.8841 f
  U12601/ZN (AOI21_X1)                    0.2889    13.1730 r
  U12607/ZN (OAI21_X1)                    0.1847    13.3577 f
  U2333/ZN (AOI21_X2)                     0.2143    13.5719 r
  U2334/ZN (INV_X4)                       0.0562    13.6281 f
  U12631/CO (FA_X1)                       0.4832    14.1113 f
  U12639/CO (FA_X1)                       0.5172    14.6286 f
  U12649/CO (FA_X1)                       0.5241    15.1527 f
  U2308/ZN (NAND2_X2)                     0.1339    15.2866 r
  U2306/ZN (NAND2_X2)                     0.0717    15.3583 f
  U12659/CO (FA_X1)                       0.4800    15.8383 f
  U12661/CO (FA_X1)                       0.4850    16.3233 f
  U12663/ZN (XNOR2_X1)                    0.4490    16.7723 r
  U2323/ZN (INV_X4)                       0.0952    16.8675 f
  U12664/ZN (XNOR2_X1)                    0.2706    17.1381 f
```

U12665/ZN (NOR2_X1) 0.2422 17.3804 r
U12666/ZN (NAND2_X1) 0.1124 17.4928 f
U13065/ZN (AOI21_X1) 0.3692 17.8620 r
U13066/ZN (OAI21_X1) 0.1714 18.0334 f
U13067/ZN (AOI21_X1) 0.3749 18.4083 r
U13068/ZN (OAI21_X1) 0.2594 18.6678 f
U2442/ZN (INV_X1) 0.5518 19.2196 r
U2693/ZN (OR2_X2) 0.2494 19.4689 r
U13427/ZN (NAND2_X1) 0.0696 19.5386 f
U13428/ZN (XNOR2_X1) 0.4698 20.0084 r
U2685/ZN (INV_X1) 0.1496 20.1580 f
U13429/S (FA_X1) 0.7073 20.8653 f
U13449/CO (FA_X1) 0.6179 21.4832 f
U13448/CO (FA_X1) 0.6017 22.0849 f
U13447/CO (FA_X1) 0.5172 22.6022 f
U13446/CO (FA_X1) 0.5172 23.1194 f
U13444/CO (FA_X1) 0.5238 23.6432 f
U2376/ZN (NAND2_X1) 0.2115 23.8547 r
U2324/ZN (NAND3_X2) 0.1172 23.9719 f
U13442/CO (FA_X1) 0.4889 24.4608 f
U13441/CO (FA_X1) 0.5172 24.9780 f
U13486/S (FA_X1) 0.7806 25.7586 r
U2304/ZN (NOR2_X2) 0.0976 25.8562 f
U13483/ZN (NOR2_X1) 0.3711 26.2273 r
U2675/ZN (INV_X1) 0.1048 26.3321 f
U13574/ZN (OAI21_X1) 0.4105 26.7425 r
U2302/ZN (INV_X4) 0.0309 26.7734 f
U2289/ZN (OAI21_X1) 0.4640 27.2374 r
U3614/ZN (NAND2_X2) 0.3383 27.5757 f
U4816/ZN (INV_X1) 0.6469 28.2226 r
U4589/ZN (AND2_X1) 0.6655 28.8880 r
U2662/ZN (INV_X1) 0.1480 29.0360 f
U4573/ZN (OR2_X1) 0.3206 29.3566 f
U16758/ZN (NAND3_X1) 0.3137 29.6703 r
U16759/ZN (NAND2_X1) 0.1065 29.7768 f
U2605/ZN (AND4_X1) 0.4300 30.2068 f
U2588/ZN (OR2_X1) 0.2119 30.4187 f
U2580/ZN (AND2_X2) 0.2065 30.6251 f
U17546/ZN (NAND3_X1) 0.1105 30.7356 r
U17547/ZN (NOR2_X1) 0.0966 30.8322 f
U17548/ZN (AND3_X1) 0.2914 31.1236 f
U2539/ZN (AND4_X1) 0.3804 31.5039 f
U2536/ZN (AND3_X1) 0.2666 31.7705 f
U17666/ZN (AOI21_X1) 0.3045 32.0751 r
U2535/ZN (AND3_X1) 0.5814 32.6564 r
U18023/ZN (AOI21_X1) 0.1754 32.8318 f
U18024/Z (XOR2_X1) 0.3958 33.2275 f
U4691/ZN (OR2_X1) 0.2160 33.4435 f
U18070/ZN (AOI22_X1) 0.4345 33.8780 r
U18074/ZN (OAI22_X1) 0.2170 34.0950 f
new_c_reg[62]/D (DFF_X1) 0.0000 34.0950 f
data arrival time 34.0950

clock clk (rise edge) 35.0000 35.0000
clock network delay (ideal) 0.0000 35.0000
clock uncertainty -0.0500 34.9500
new_c_reg[62]/CK (DFF_X1) 0.0000 34.9500 r
library setup time -0.3584 34.5916
data required time 34.5916
---
data required time 34.5916
data arrival time -34.0950
---
slack (MET) 0.4966

Timing_Min_Fast_HoldCheck_Tut1

```
****************************************
Report : timing
        -path full
        -delay min
        -max_paths 1
Design : MyDesign
Version: T-2022.03-SP4
Date   : Thu Nov 16 10:47:51 2023
****************************************

Operating Conditions: fast   Library: NangateOpenCellLibrary_PDKv1_2_v2008_10_fast_nldm
Wire Load Model Mode: top

  Startpoint: m_reg_reg[9]
              (rising edge-triggered flip-flop clocked by clk)
  Endpoint: m_reg_reg[9]
            (rising edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: min

  Point                                   Incr       Path
  -----------------------------------------------------------
  clock clk (rise edge)                   0.0000     0.0000
  clock network delay (ideal)             0.0000     0.0000
  m_reg_reg[9]/CK (DFF_X1)                0.0000     0.0000 r
  m_reg_reg[9]/Q (DFF_X1)                 0.0546     0.0546 r
  U19787/ZN (OAI21_X1)                    0.0177     0.0723 f
  m_reg_reg[9]/D (DFF_X1)                 0.0000     0.0723 f
  data arrival time                                  0.0723

  clock clk (rise edge)                   0.0000     0.0000
  clock network delay (ideal)             0.0000     0.0000
  clock uncertainty                       0.0500     0.0500
  m_reg_reg[9]/CK (DFF_X1)                0.0000     0.0500 r
  library hold time                       0.0006     0.0506
  data required time                                 0.0506
  -----------------------------------------------------------
  data required time                                 0.0506
  data arrival time                                 -0.0723
  -----------------------------------------------------------
  slack (MET)                                        0.0218
```