7. Recommendations for Future Initiatives for Japan to improve Digital Transformation in the Electronics/Semiconductor industry.

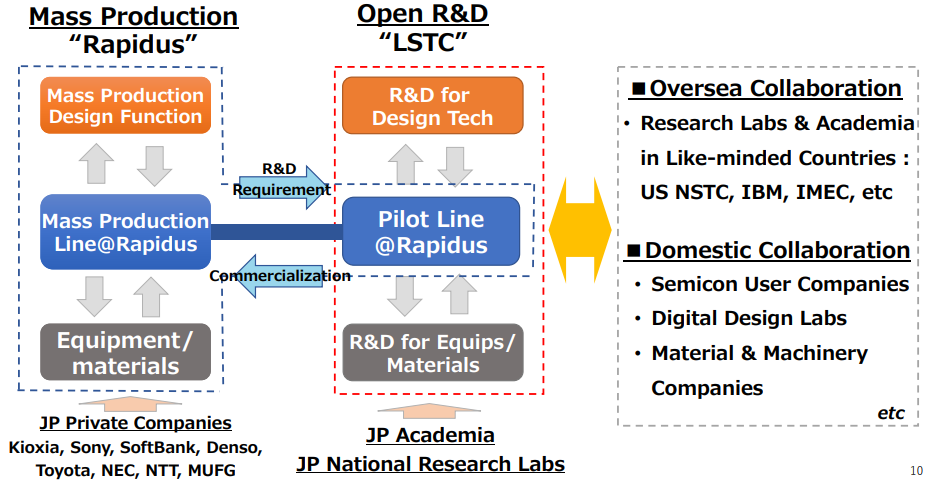
In this section, we will cover the current strategy that Japan government has outlined to resurrect their semiconductor industry. Then we will discuss about the 5 dimensions for agility (Technology, Organization Design, People, Leadership, Culture) for Japanese semiconductor/electronics MNC to adopt. Agility is crucial as the global semiconductor industry is extremely fast paced and Japan does not have the reputation of a fast-changing environment. Next, we will discuss the recommendations for Japanese SMEs for digital transformation.

Current Strategy:

In June 2021, Japan’s Ministry of Economy, Trade and Industry (METI) outlined a core strategy for their semiconductor and digital industries with the following measures:

* Formation of a partnership with the United States and Taiwan. Japan’s most advanced fabs are operating at the 40nm design, which is 10 years behind world leaders TSMC and Samsung. Through collaboration with other countries, Japan might be able to achieve the design and production of next generation chips (2nm and below) by the late 2020s. This objective will be pursued through the formation of Rapidus, a consortium of Japanese semiconductor companies in collaborating with IBM and European research organization IMEC
* Development of “game-changing” future semiconductor technologies. Japan is establishing the Leading-Edge Semiconductor Technology Center (LSTC), a government-supported R&D center for advanced chip research.
* Establishment of new chip manufacturing bases to make legacy devices. Japan is providing subsidies to entice Taiwan’s TSMC to form a joint venture with Japanese firms to build advanced fab plants in Japan.
* Subsidies for domestic chip manufacturing. Japanese government is inclined to subsidize up to 1/3 of the capital costs incurred by domestic and foreign manufacturers to produced designated types of semiconductor devices, equipment, and raw materials.

To achieve this strategy and outcome that Japan government has outlined, Japanese MNCs semiconductor companies would need to address the 5 key factors (Technology, Organization Design, People, Leadership, Culture) to digitally transform themselves and be agile to anticipate the future and fast changing semiconductor/electronics that the global market needs.



Technology Dimension of Agility:

In the *Unlocking Agility*, Technology in this context is meant to represent “tools, techniques, or methods assisting in unlocking agility in Japanese semiconductor companies. We defined agility as the ability to build the right thing, build the thing right and build at the right speed.

* To build the right thing: In this context, Japanese semiconductor companies has already defined what is the right thing to build, and the right thing is the 2nm chip technology. However, 2nm chip technology comes in various forms of engineering design principles. What is important is the how Japanese semiconductors going to use the Lean Startup methodology to find the right design 2nm chip technology that works for them, and also compete with other global companies. The Lean Startup methodology is about the continual and circular process of building experiments, measure metrics and learn assumptions. Therefore, it is crucial that LSTC (being a R&D center) adopt to this methodology. One of the key outcomes of LSTC as an organization is to fail fast and learn fast. Once they have a minimum viable product, they will then port it over to Rapidus for mass production/commercialization.
* To build the thing right: During mass production at Rapidus, there will be a New Product Introduction (NPI) phase before High Volume Manufacturing (HVM). During the NPI stage, it is critical that Rapidus uses Scrum-like process manner to drive the yield from 10% to mature yield 80-90%. The key thing is it is critical Rapidus embraces validated learning through frequent feedback loops. To achieve that, Rapidus have to set up the right AI/Machine Learning/Data Analysis infrastructure, skills set to quickly generate data insights on the issues that are hindering mature yield. Once these data insights are being generated, it will be much faster for the new chip technology to achieve mature yield.
* To build at the right speed: In most cases in semiconductor industries, it is takes about 12 months for a new chip technology from R&D stage to High Volume Manufacturing (HVM) stage with mature yield. Therefore, it is essential that both Rapidus and LSTC work hand in hand to ensure that from the R&D period to the HVM stage, it does not take more than 12 months, they may uses tools such as Value Stream Mapping (VSM) to ensure smooth product delivery.