CHAPTER 4.

Digital Signals

4.1 Digital signals

- Most sensors have analog output : need to be converted from analog to digital → A/D
- Most actuators have analog input : need to be converted from digital to analog → D/A

4.4.1 Binary numbers

- Binary system: 0, 1 = 0V, 5V

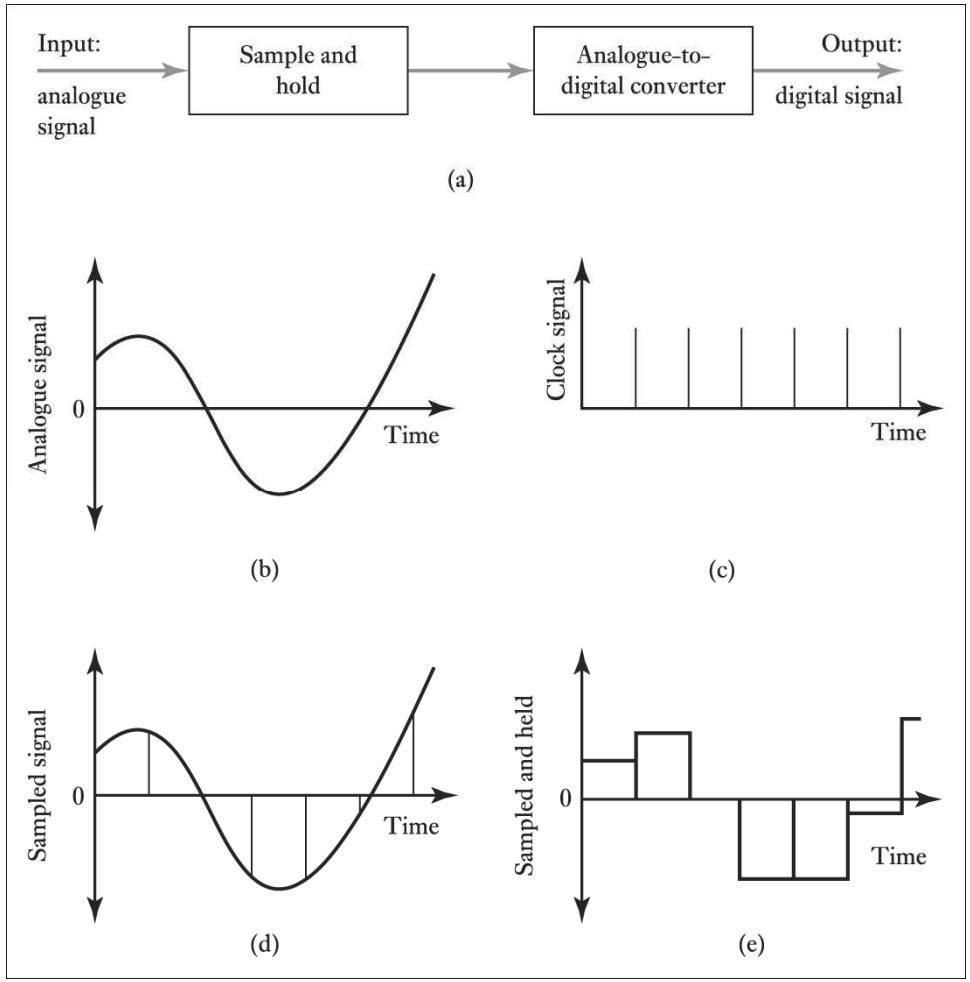
- Ex) 4bit word

MSB			LSB
2^3	2^2	2^1	2^0
bit 3	bit 2	bit 1	bit 0

- Ex) $10_{(10)}=1010_{(2)}=1X2^3+0X2^2+1X2^1+0X2^0$

4.2 Analogue and digital signals

- Analogue-to-Digital Conversion, ADC, A/D:
  - Analogue signal → Binary digit



Analogue signal
→ Clock
→ Sample & hold
→ Quantization

Figure 4.1

(a) Analogue-to-digital conversion

(b) analogue input

(c) clock signal

(d) sampled signal

(e) sampled and held signal

4.2 Analogue and digital signals

- Ex) 3 bit ADC :
  - 3 bit = 2^3 = 8 levels
  - 8 Quantization level
  - Quantization interval: voltage difference between the levels
  - Quantization error: difference between the actual and the level voltage

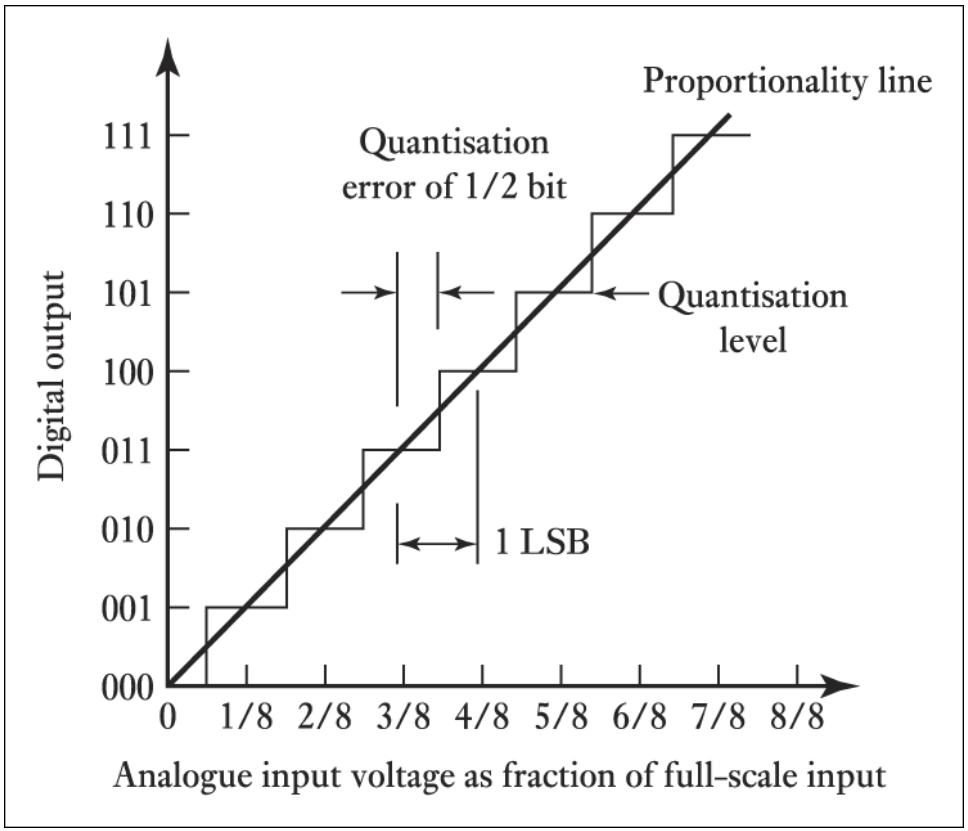


Figure 4.2 Input/output for an ADC

4.2.1 Sampling theorem

- Nyquist criterion or Shannon's sampling theorem
  - When the signal is reconstructed from the samples, it is only when the sampling rate is at least twice that of the highest frequency in the analogue signal that the sample gives the original form of signal.

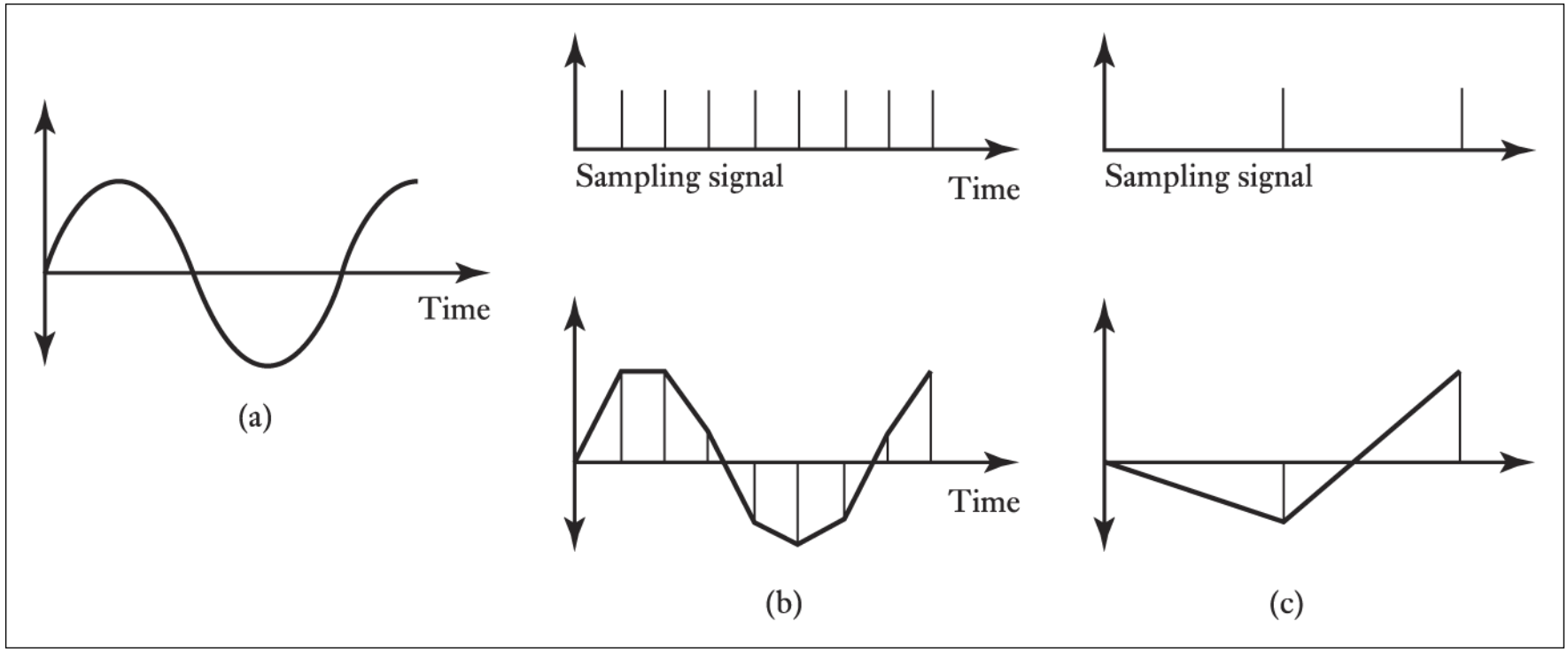


Figure 4.3 Effect of sampling frequency: (a) analogue signal, (b) sampled signal, (c) sampled signal

4.2.1 Sampling theorem

- Aliasing : the problem comes from the low speed sampling
- Ex) The TV advertisement of Genesis, Hyundai

4.2.2 Digital-to-analogue conversion

- Ex) When the D/A converter has 8 bit word and the maximum output voltage is 6V, then the digital value is 11111111 and the analogue signal has 6V. What will be the output voltage for a change of 1 bit?
- Ex)

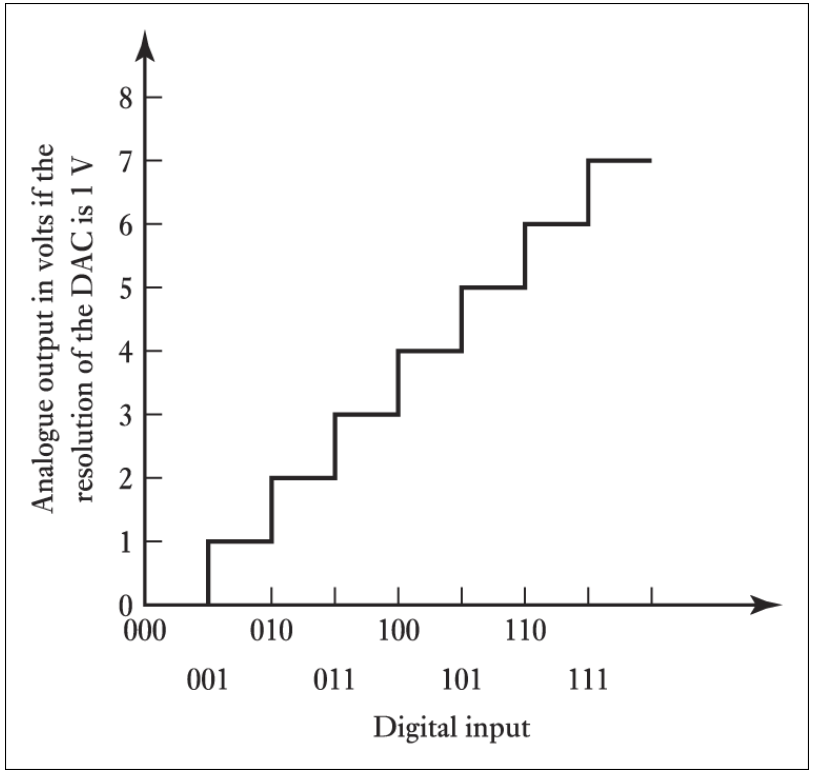


Figure 4.4 Input/output for a DAC

4.3 Digital-to-analogue and analogue-to-digital converters

4.3.1 DACs

- Weighted-resistor DAC: accurate resistances are required.

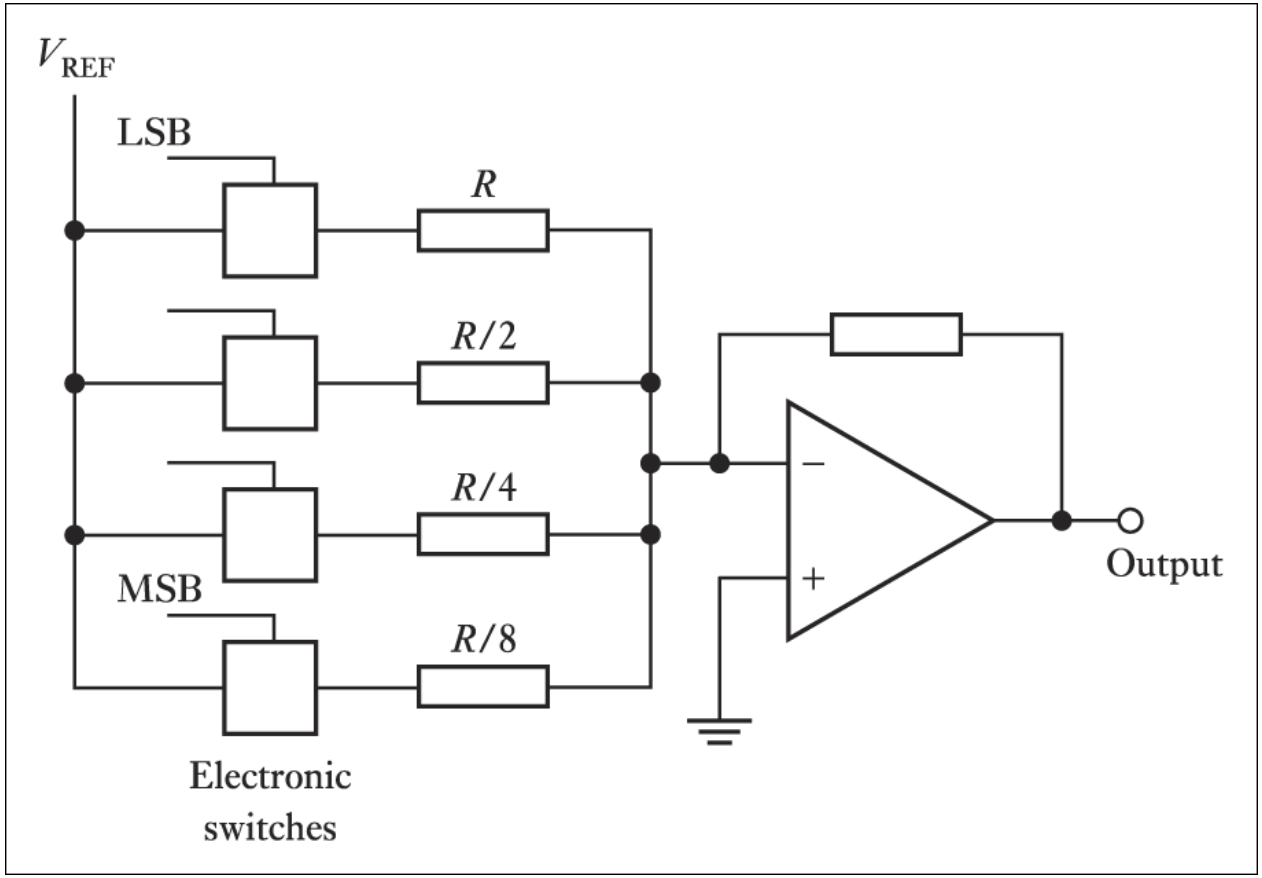


Figure 4.5 Weighted-resistor DAC

4.3 Digital-to-analogue and analogue-to-digital converters

4.3.1 DACs

- R-2R ladder network: Only 2 values of resistance are required.

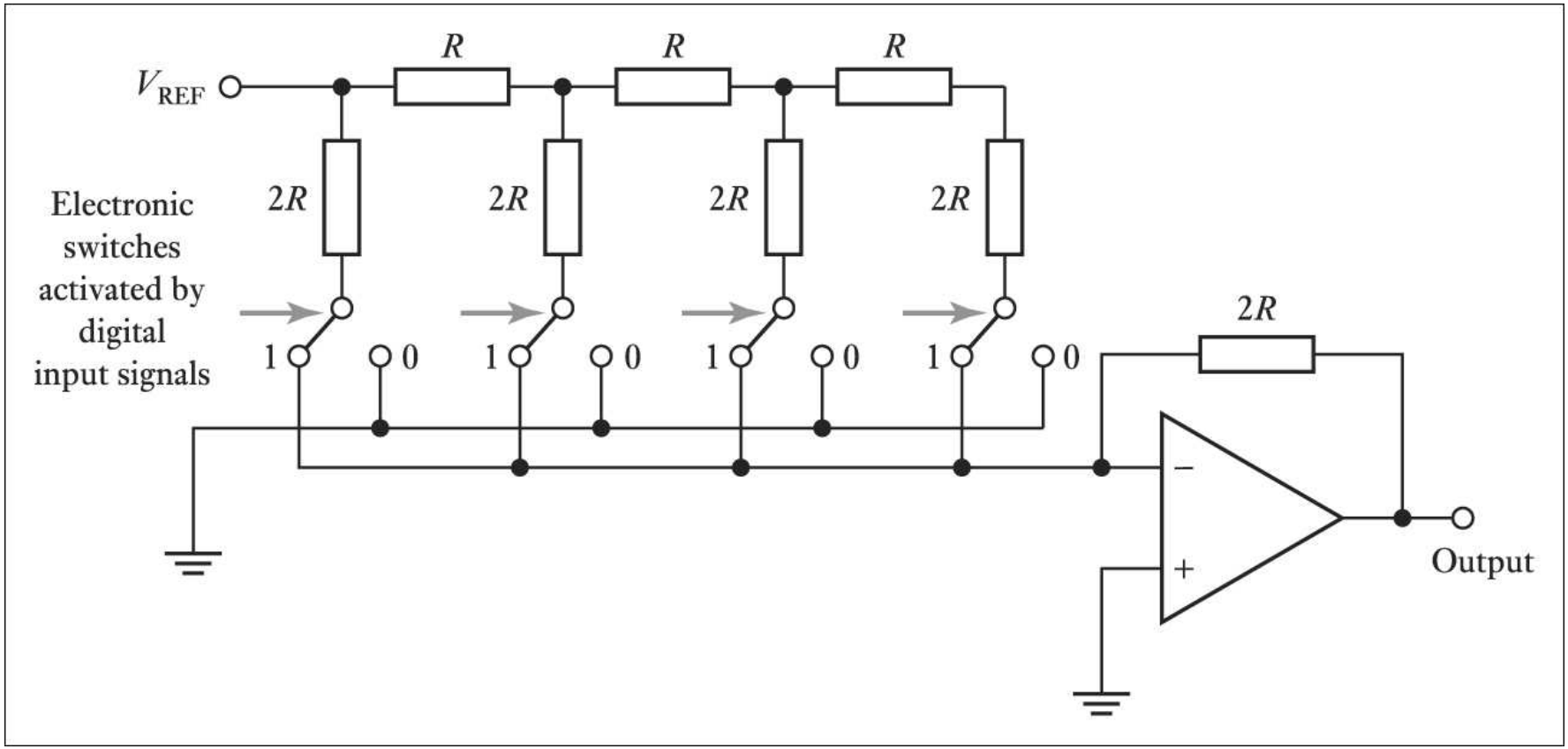


Figure 4.6 *R*–2*R* ladder DAC

4.3 Digital-to-analogue and analogue-to-digital converters

4.3.1 DACs

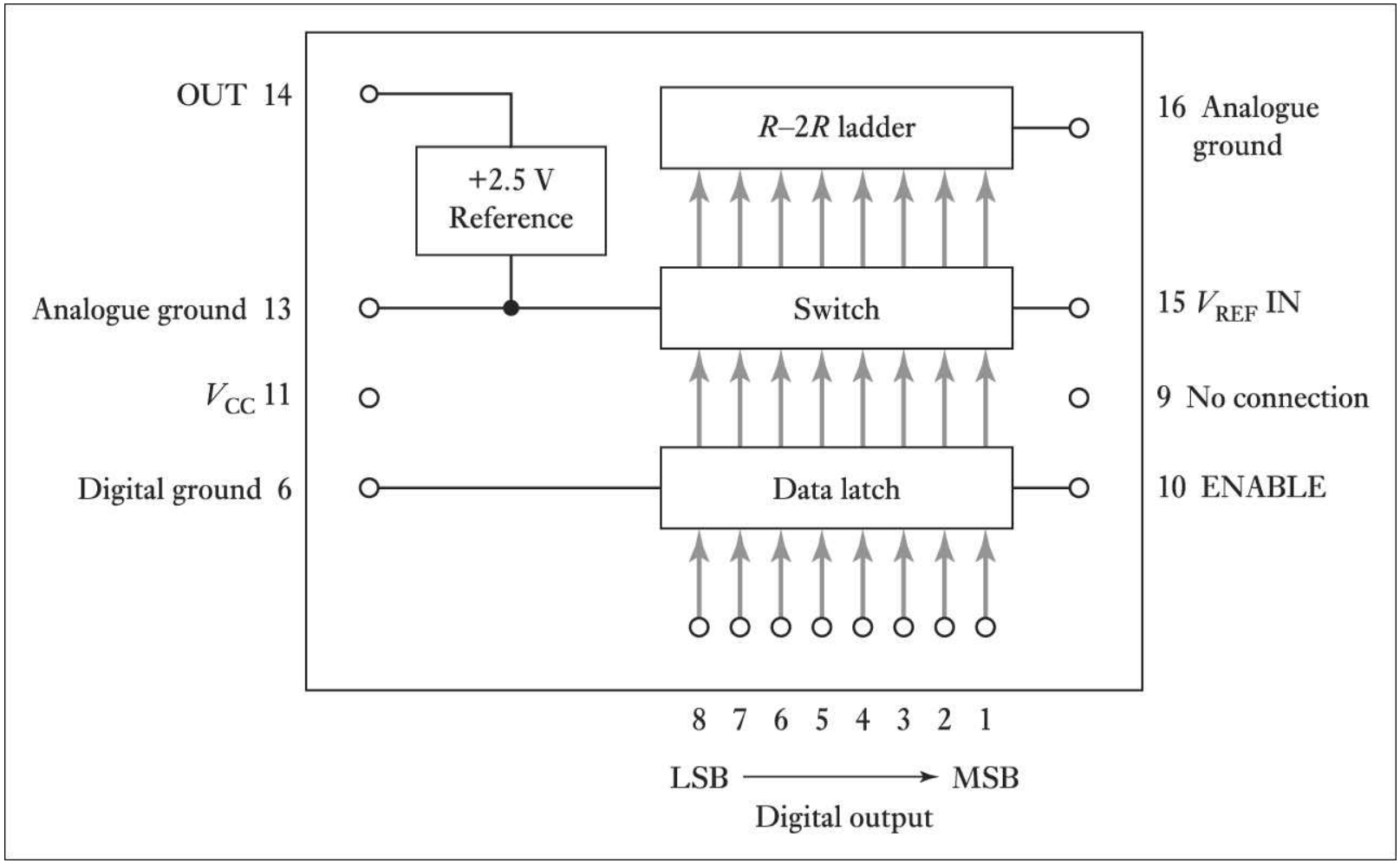


Figure 4.7 ZN558D DAC

4.3 Digital-to-analogue and analogue-to-digital converters

4.3.1 DACs

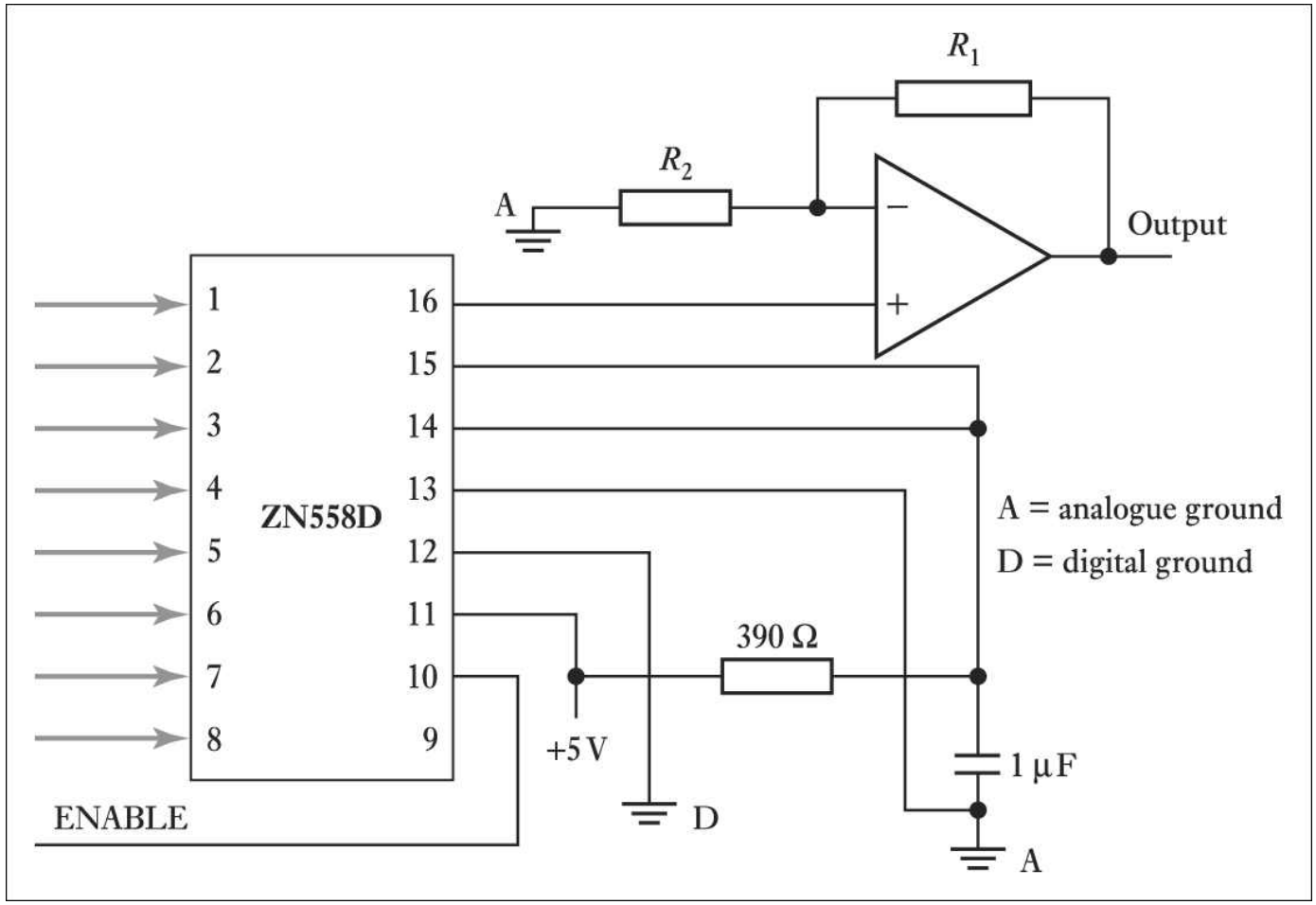


Figure 4.8 Unipolar operation

- DAC specification contains following issues.

- 1. Full-scale output :
  - When the all bits of input word has '1' value, the output voltage is called full-scale output.

- 2. Resolution :
  - ex) When we have 8 bit D/A, the output voltage has 256 levels.

- 3. Settling time :
  - The time taken by DAC to reach within ½ LSB of its new voltage after a binary change.

- 4. Linearity :
  - The maximum deviation from the straight line through zero and the full range of the output.

4.3.2 ADCs

Approaches

- Successive approximation
- Ramp
- Dual ramp
- Flash

4.3.2 ADCs

- Successive approximation

-Most commonly used

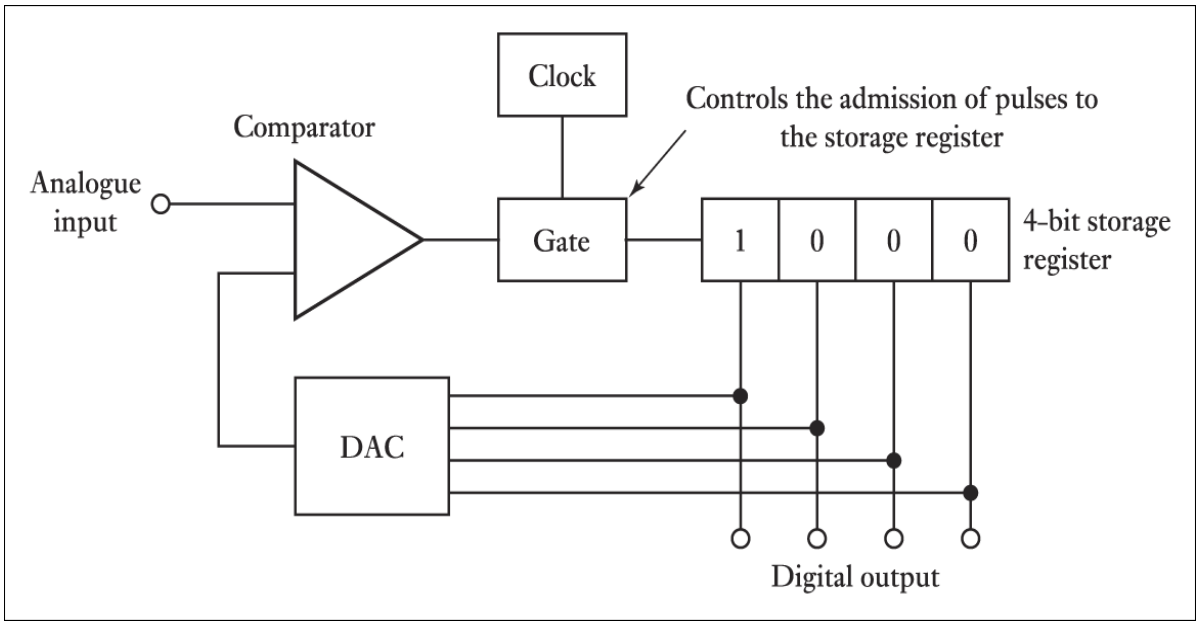


Figure 4.9 Successive approximations ADC

- Clock
→ Counting the clock
→ Storage resister
→ DAC
→ Increase the analogue signal of DAC
→ Compare with the input analogue signal and DAC output signal
→ If the DAC signal has higher voltage than the input signal, stop the gate and the clock counting
→ Read the DAC input value

- Slow

4.3.2 ADCs

- Successive approximation

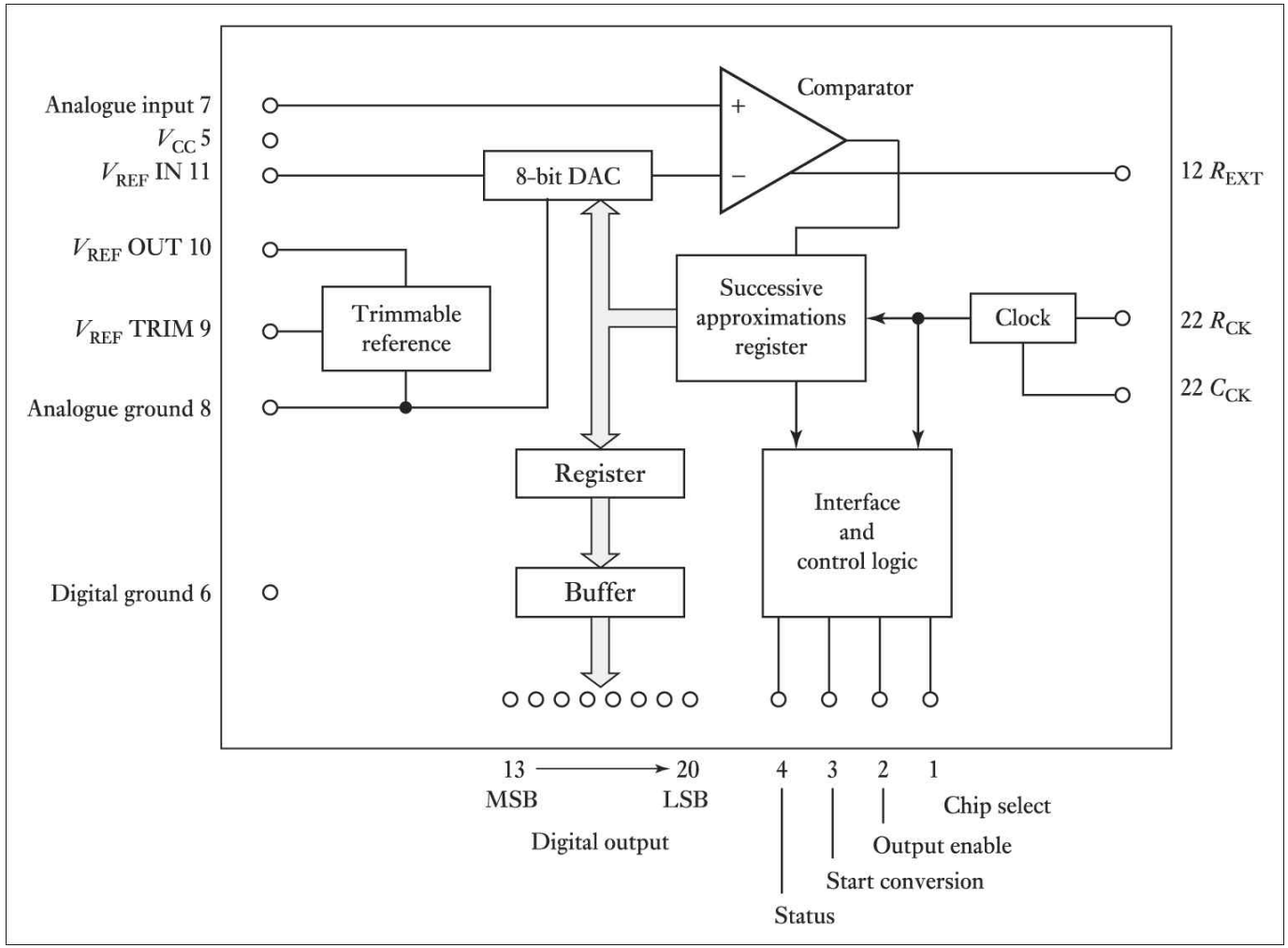


Figure 4.10 ZN439 ADC

4.3.2 ADCs

- Successive approximation

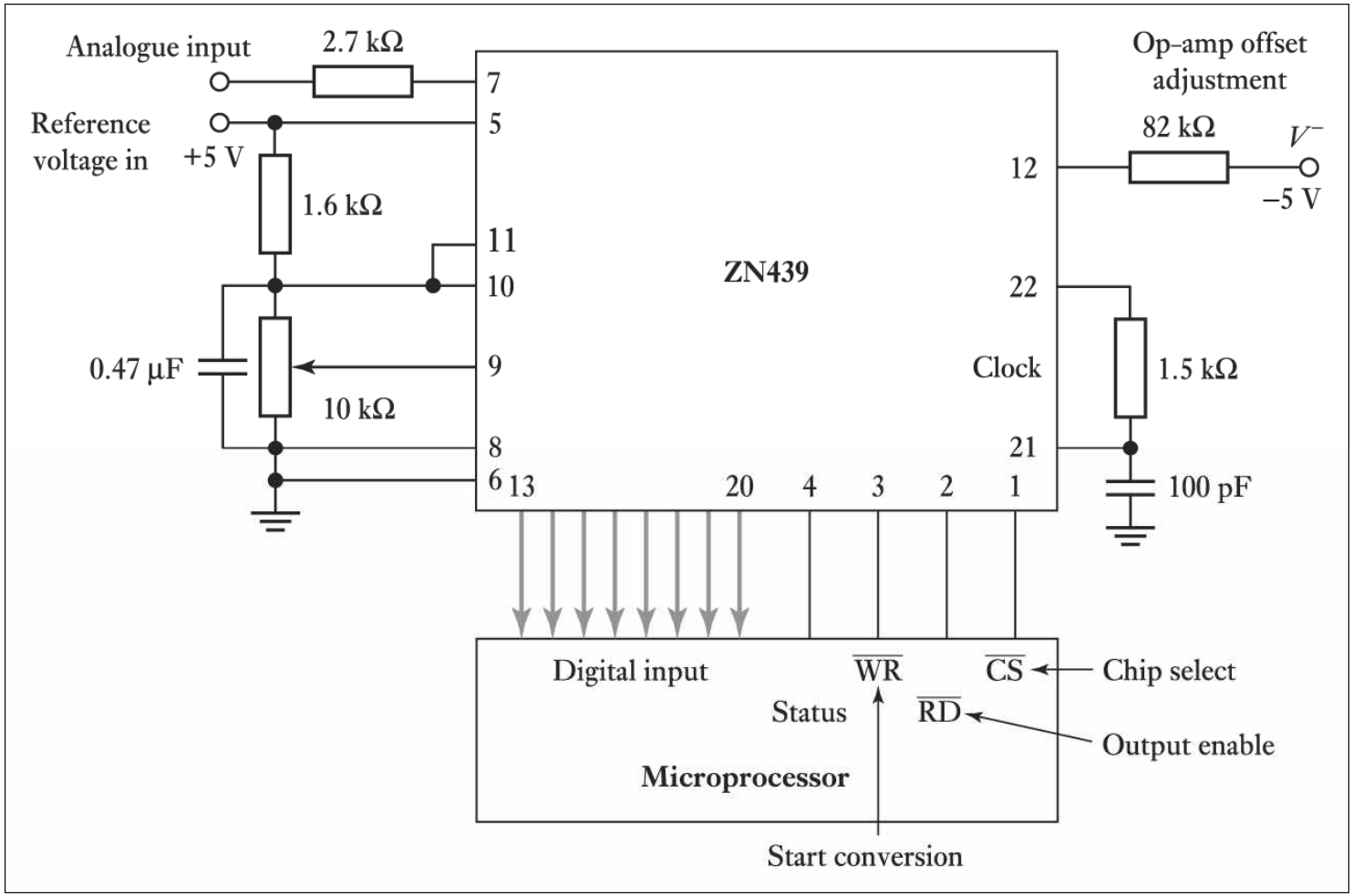


Figure 4.11 **ZN439 connected to a microprocessor**

4.3.2 ADCs

- Ramp

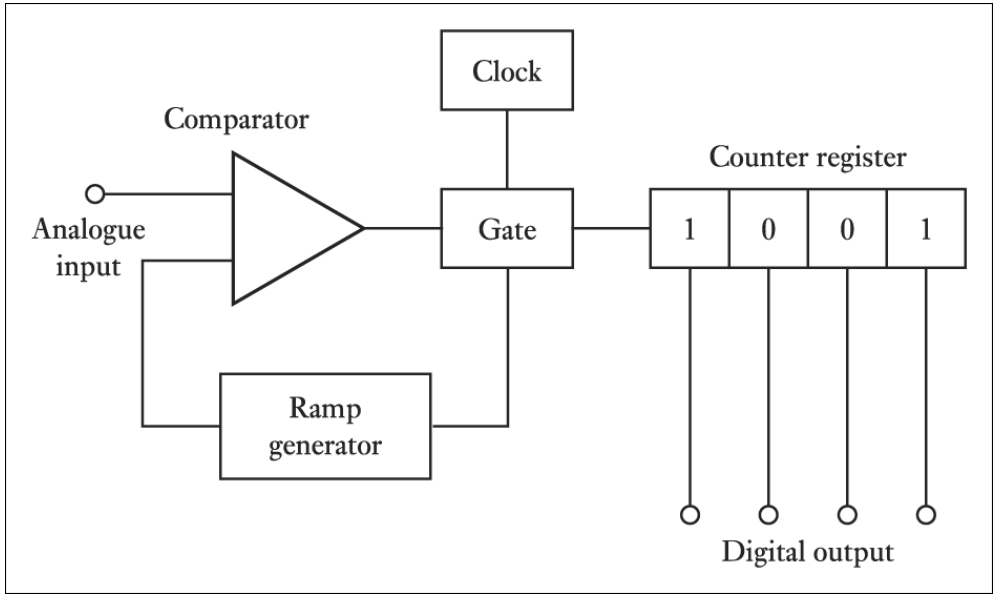


Figure 4.12 Ramp ADC

- Use ramp signal instead of DAC

→ Start the ramp signal and clock counting

→ Compare the input analogue signal with the ramp signal

→ If compare matches, stop the ramp signal generating and the clock counting

→ The counted clock data is the ADC result.

→ Reset the counter and the ramp generator.

4.3.2 ADCs

- Dual ramp
  - The analogue voltage is applied to an integrator → comparator → AND gate passes the clock pulse → counting the clock pulse until it overflows → switching the input to the reference input, which has opposite polarity of the input voltage → reset the counter and count again the clock → when the comparator signal falls down stop the counting → the counted data is the result of A/D.

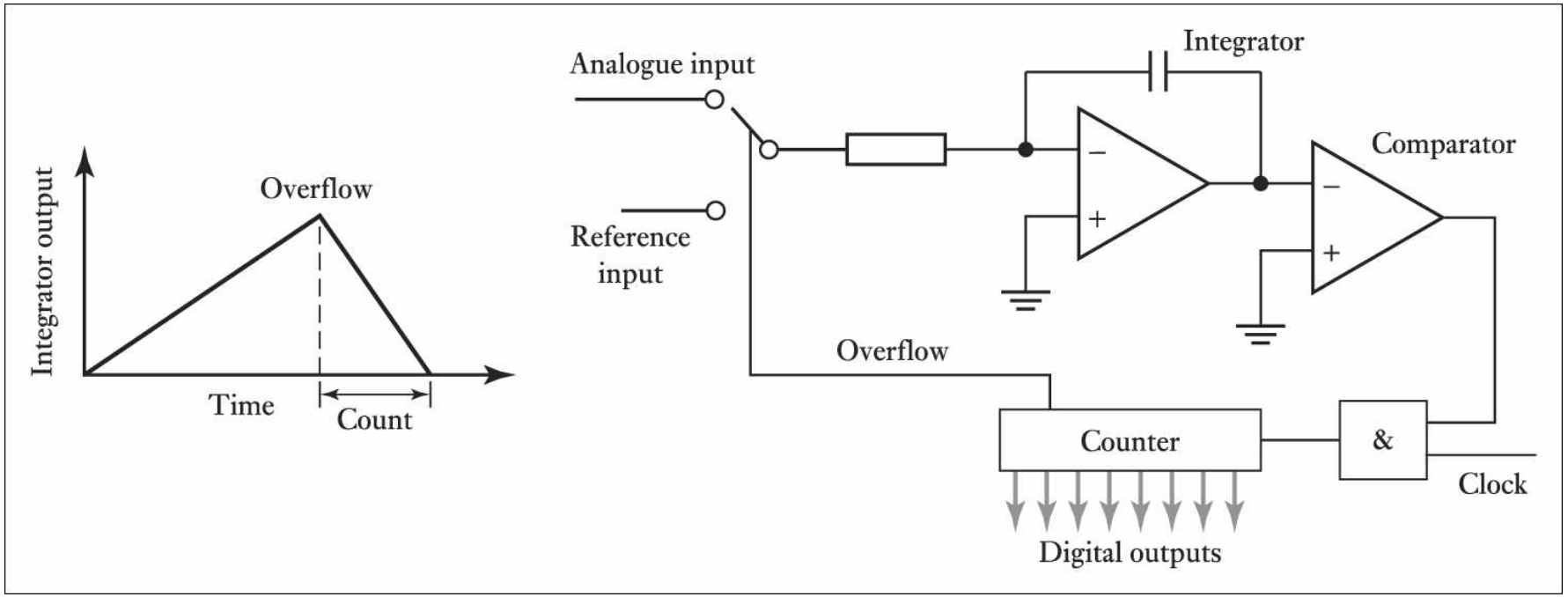


Figure 4.13 Dual ramp ADC

4.3.2 ADCs

- Flash: Very fast ADC

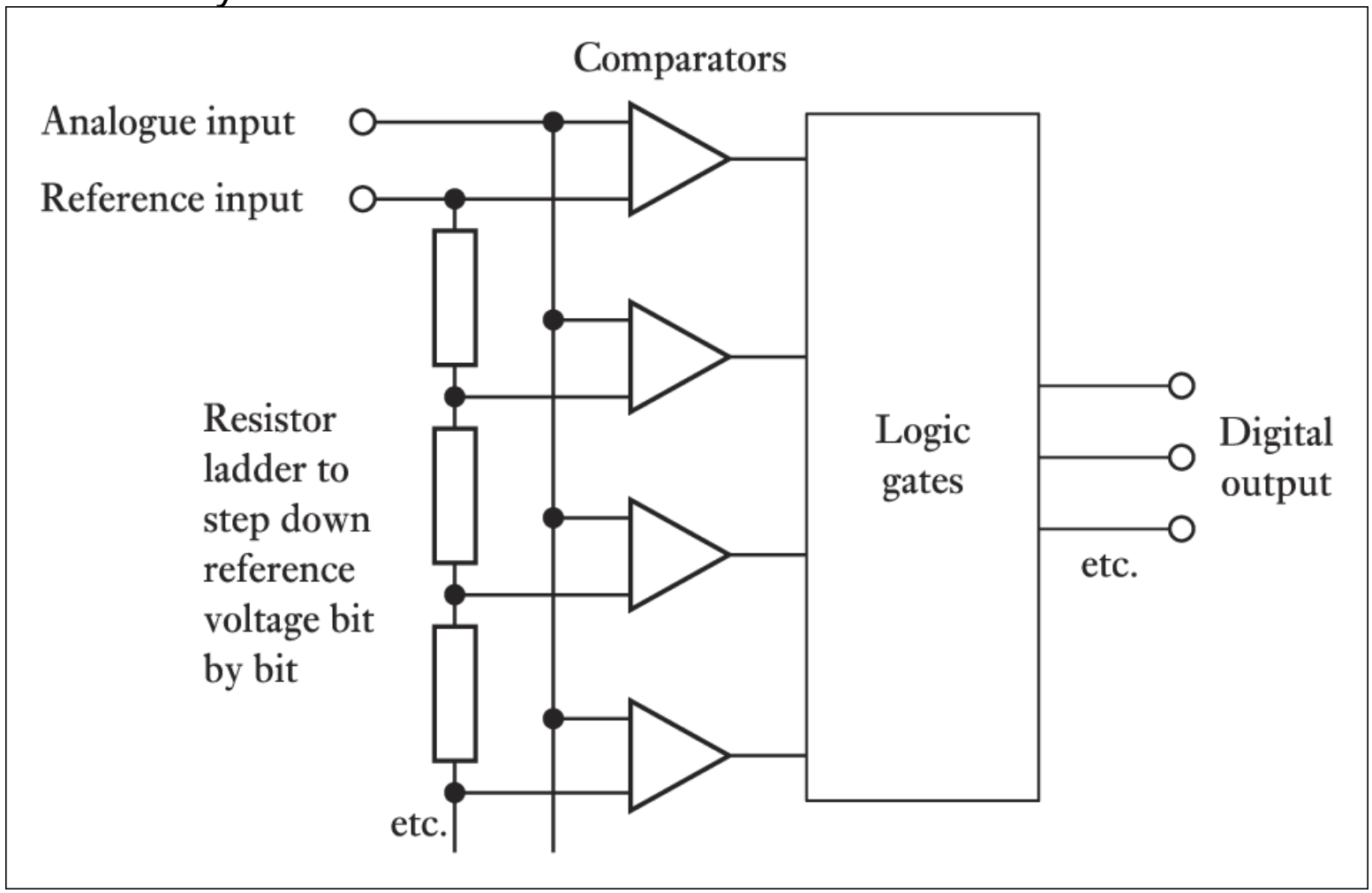


Figure 4.14 Flash ADC

In considering the specifications of ADCs …

- 1. Conversion time :
  - The time required to complete a conversion of the input signal. It establishes the upper signal frequency that can be sampled without aliasing.
  - The maximum frequency is 1/(2Xconversion time).

- 2. Resolution :
  - The full-scale signal divided by 2^n, where n is the number of bits.
  - Often specified by the number of bit

- 3. Linearity error :
  - The deviation from a straight line drawn through zero and full-scale.
  - It is a maximum of ±1/2 LSB.

ADC	Type	Resolution (bits)	Conversion time (ns)	Linearity error (LSB)
ZN439	SA	8	5 000	±1/2
ZN448E	SA	8	9 000	±1/2
ADS7806	SA	12	20 000	±1/2
ADS7078C	SA	16	20 000	±1/2
ADC302	F	8	20	±1/2

SA = successive approximations, F = flash.

Table 4.1 ADCs

4.3.3 Sample and hold amplifiers

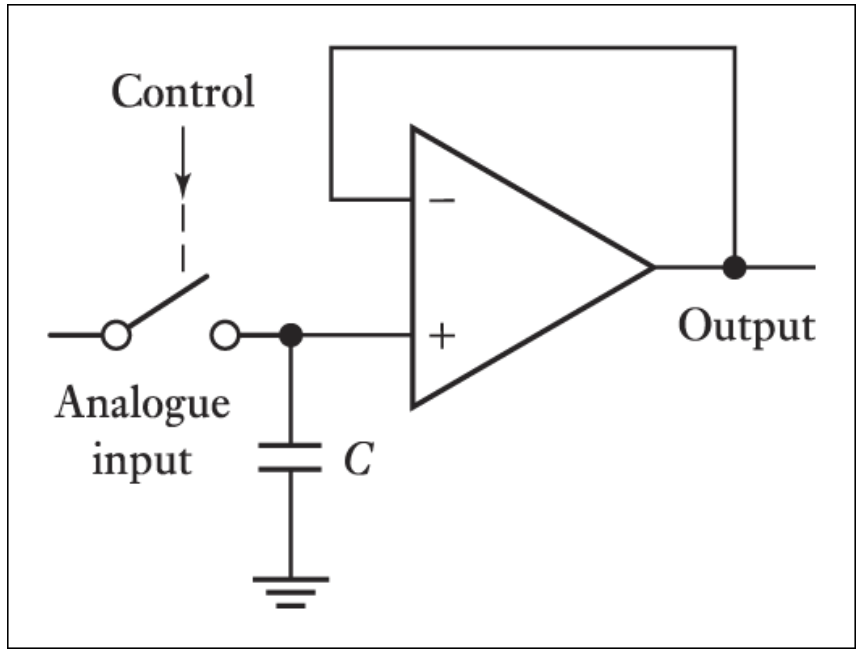


Figure 4.15 Sample and hold amplifier

4.4 Multiplexers : Analogue switch (selects the channel)

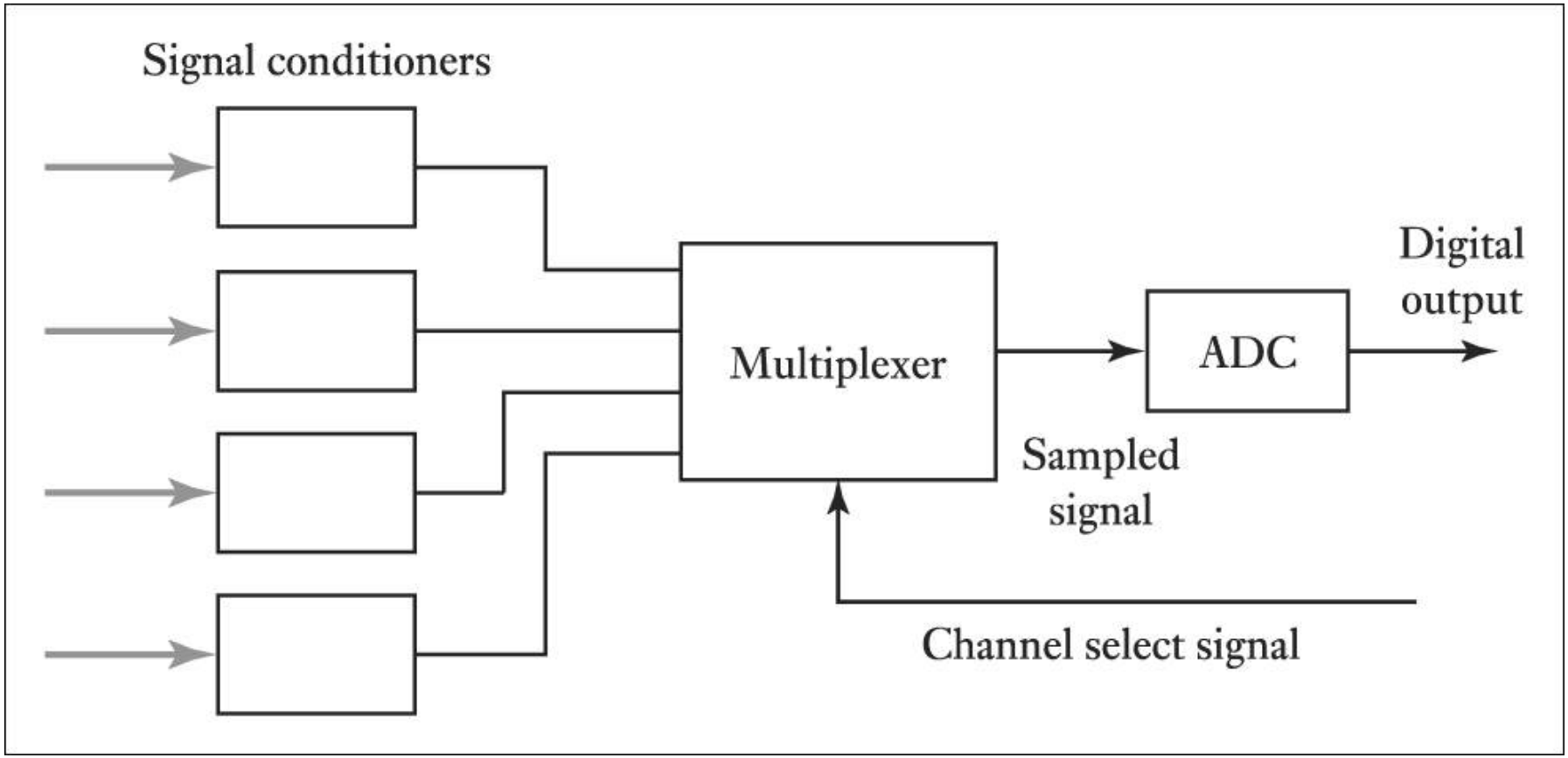


Figure 4.16 Multiplexer

4.4.1 Digital multiplexer

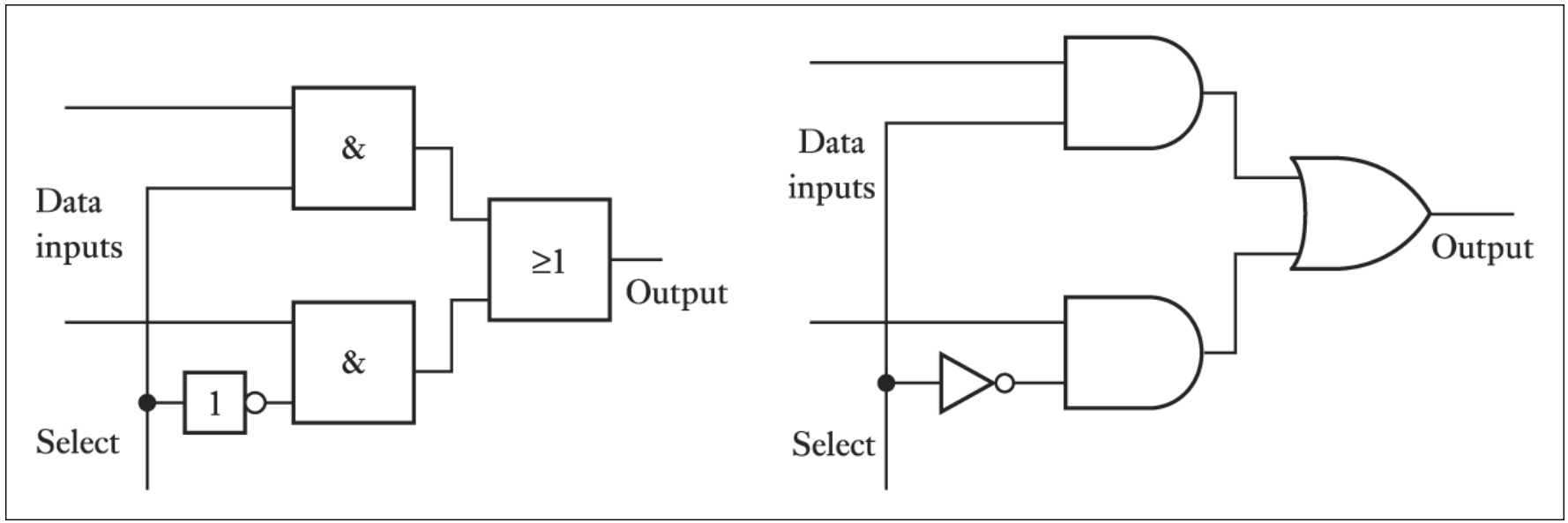


Figure 4.17 Two-channel multiplexer

4.4.2 Time division multiplexing

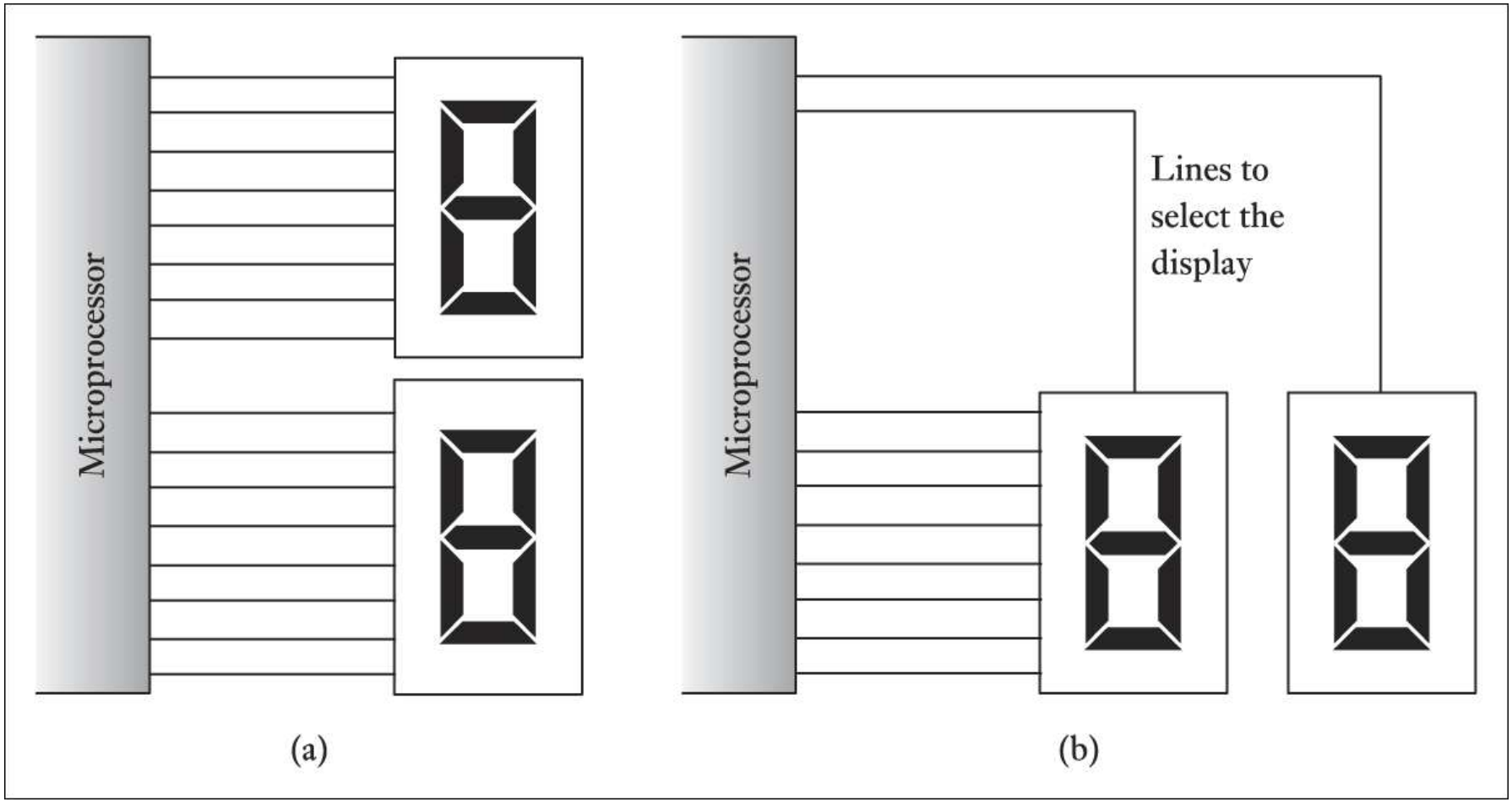


Figure 4.18 Time division multiplexing: (a) the system is not time multiplexed, (b) t he system is time multiplexed

4.5 Data acquisition (DAQ)

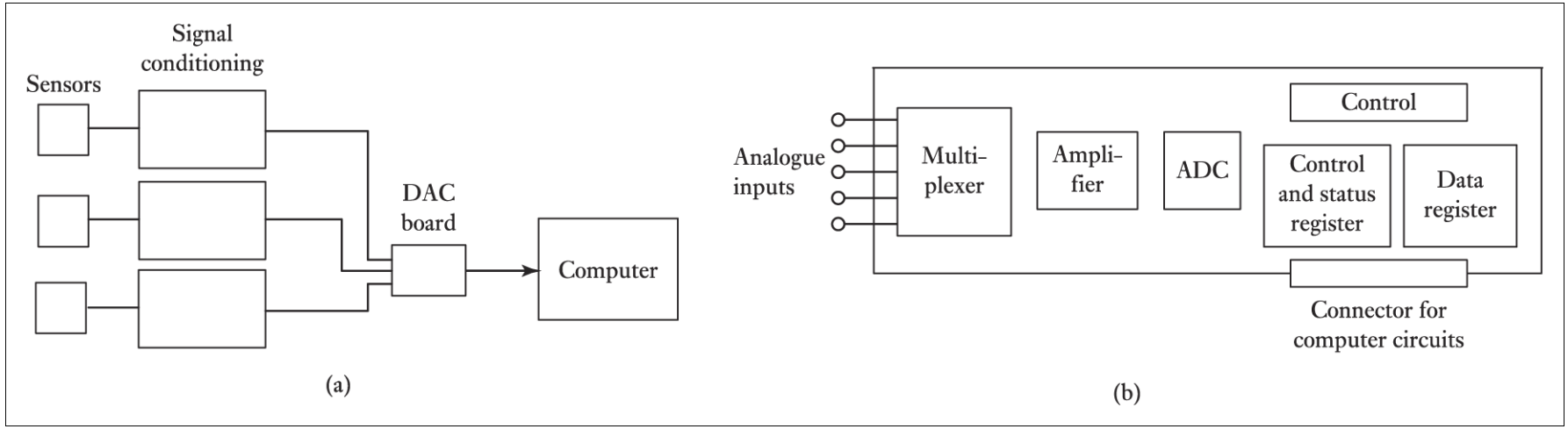


Figure 4.19 DAQ system

4.5 Data acquisition (DAQ)

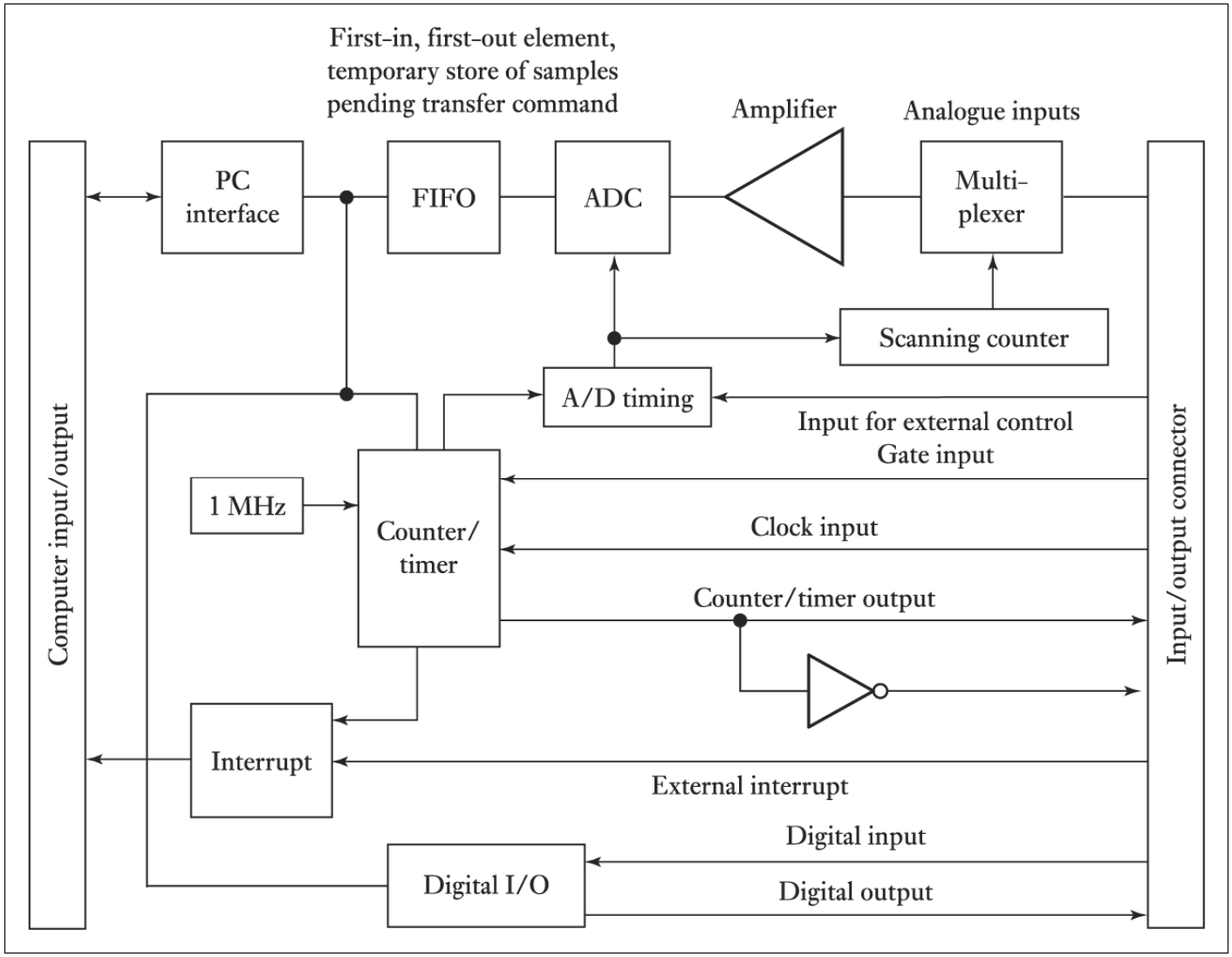


Figure 4.20 PC-LPM-16 DAQ board

4.5.1 Data accuracy

- An advantage of digital signal processing is that two voltage ranges are used rather than two exact voltage levels to distinguish between the two binary states for each bit.
- Thus data accuracy is less affected by noise, drift, component tolerances, and other factors causing fluctuations in voltages which would be critical for transmission as analogue voltages.

4.5.2 Parity method for error detection

- A parity bit is an extra 0 or 1 bit attached to a code group at transmission.
- Even parity:
  - Make the total number of '1' including parity bit be even.
- Odd parity:
  - Make the total number of '1' including parity bit be odd.

4.6 Digital signal processing

- Difference equation

  y[k]=x[k]+y[k-1]

- Tustin's approximation for integration

  y[k]=y[k-1]+(T/2)*(x[k]+x[k-1])

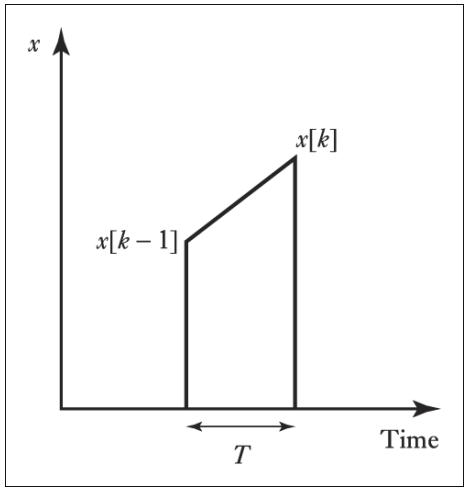


Figure 4.21 Integration

- Differentiation

  y[k]=(x[k]-x[k-1])/T