TWO-STAGE DUAL-CHANNEL HEADPHONE AMPLIFIER

William Knoff, Ethan Lin

ABSTRACT

We developed a two-stage, dual-channel audio amplifier targeted for the Sennheiser HD650 headphones with 300Ω impedance and 98 mW/dB sensitivity. HSPICE testing demonstrates that it meets the expected design specifications for gain, 3dB midband, input & output impedance, noise, and power output. Measurements made on a soldered version of our design match up with expectations.

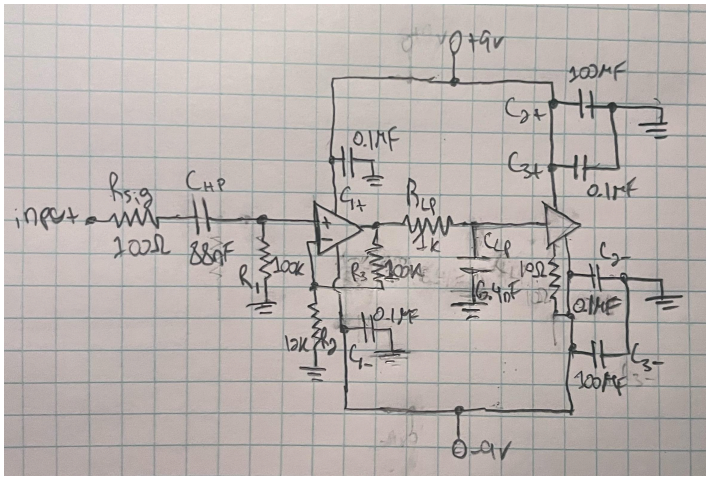
DESIGN

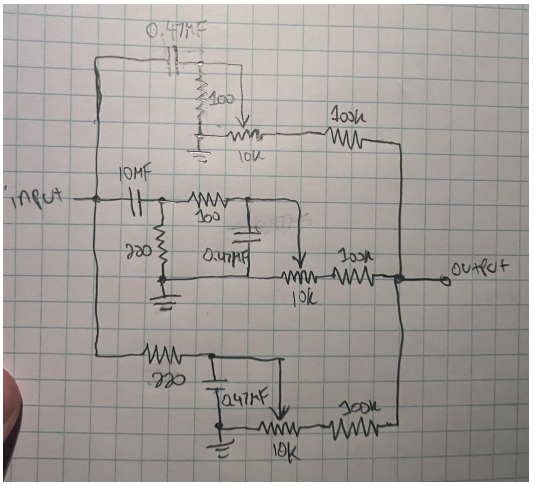
Our functional design is a two-stage amplifier consisting of a voltage gain stage and a unity-gain buffer stage. The voltage gain stage uses an OPA1656 op-amp and a negative feedback loop to achieve a closed loop voltage gain of 11.8. The second stage utilizes a BUF634A to decrease output impedance and increase current to the load. We implemented a high pass filter between the input and the op-amp, ensuring the midband starts at 18Hz, and a low pass filter between the op-amp and the buffer, capping the midband at 25Khz. Out design has capacitors in the positive and negative power supply lines for both chips to filter out high-frequency noise from the power supply and help stabilize the circuit from fluctuations that occur in real-life operation.

We chose the OPA1656 for our voltage gain stage due to its dual channels, low noise, and low distortion. For our unity-gain buffer we use the BUF634A, which is high-speed, high-current, and has a resistor-adjustable bandwidth. It has a low output impedance of <5Ω and a wide-bandwidth mode (210MHz) which we enabled. Both chips have a power supply range from ±2.25V to ±18V which accommodates for the 9v bolt batteries we used for the positive and negative lines.

We soldered the functional design to a perfboard for measurements. However, we also designed a three-band equalizer in HSPICE that we were unable to implement in real life due to time constraints. The EQ design allows for the adjustment of the bass (<72Hz), mid (72Hz - 3.4KHz), and treble (>3.4KHz). The equalizer works by utilizing a low pass, high pass, and band-pass filter to allow attenuation of each band, thus changing the ratio of each band in the frequency response.

SCHEMATICS





NETLISTS

```
.SUBCKT DUT in out vdd vss

* Include our op-amps
.include 'OPA1656.hsp'
.include 'buf634a_a.hsp'

* Resistors
Rsig in N1 100
R1 N2 0 100k
R2 N3 0 12k
R3 N3 N41 100k
Rlp N41 N42 1k

* Capacitors
Chp N1 N2 88n
C1plus vdd 0 0.1u
C2plus vdd 0 100u
C3plus vdd 0 0.1u
Clp N42 0 6.4n

C1minus vss 0 0.1u
C2minus vss 0 100u
C3minus vss 0 0.1u

* Op-Amps
X1 N2 N3 vdd vss N41 OPA165
X2 N42 out vdd vss BUF634A

.ENDS DUT
```

Fig 1. Amplifier Netlist

```
.SUBCKT EQ IN OUT BASS=0.5 MID=0.5 TREBLE=0.5

* Include the potentiometer
.INCLUDE 'POT.hsp'

* High pass filter (Treble)
C6 IN E1 0.47u
R4 E1 0 100
X1 0 E1 E2 POT VALUE=10k SET='TREBLE'
R2 E2 OUT 100k

* Band-Pass filter (Mid)
C7 IN E3 10u
R5 E3 0 220
R8 E3 E4 100
C9 E4 0 0.47u
X2 0 E4 E5 POT VALUE=10k SET='MID'
R1 E5 OUT 100k

* Low Pass Filter (BASS)
R6 IN E6 220
C8 E6 0 10u
X3 0 E6 E7 POT VALUE=10k SET='BASS'
R10 E7 OUT 100k

.ENDS EQ
```

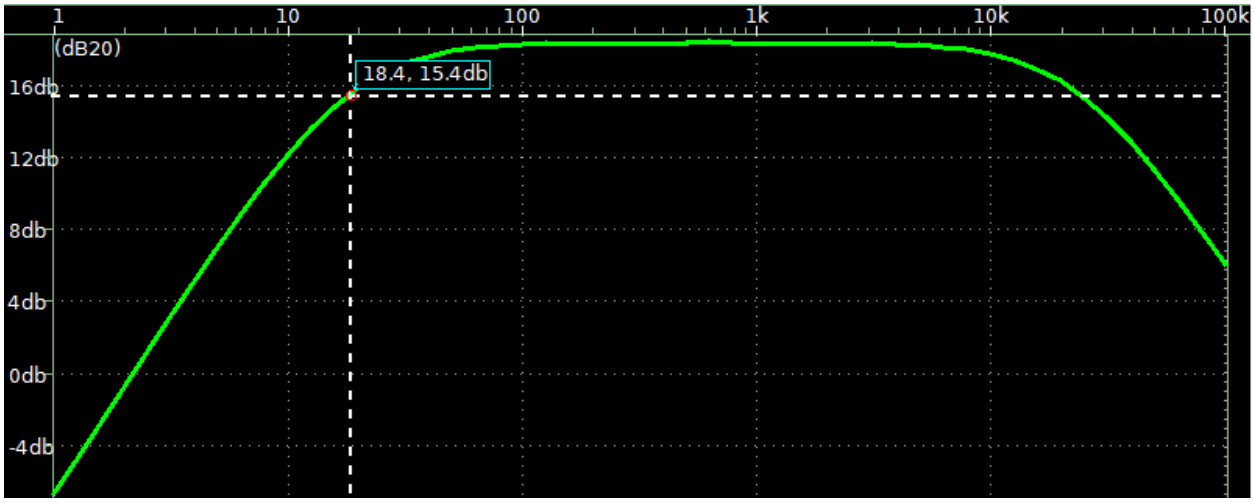
Fig 2. Equalizer (EQ) Netlist

```
* Define the potentiometer subcircuit
.SUBCKT POT 1 T 2 VALUE=10K SET=0.5
RT 1 T 'VALUE*(1-SET)+.001'
RB T 2 'VALUE*SET+.001'
.ENDS POT
```

Fig 3. Potentiometer Netlist (in EQ)

SIMULATION ANALYSIS

Test 1a yielded the following results: `gain_mid=  9.2505  at= 100.0000k` which indicates an appropriate gain from the first stage. Test 1b demonstrates the 3dB bandwidth of 18Hz-25KHz. Midband gain is 8.29.



Tests 2 indicates that the input impedance, 100kΩ, exceeds the desired value of 10kΩ. Test 3 indicates that the output impedance, 3.9Ω, is below the desired threshold of 5Ω. Test 4 results show that output power (188mW) is above the required 100mW. However, the I_{SS} peak is slightly above the desired value.

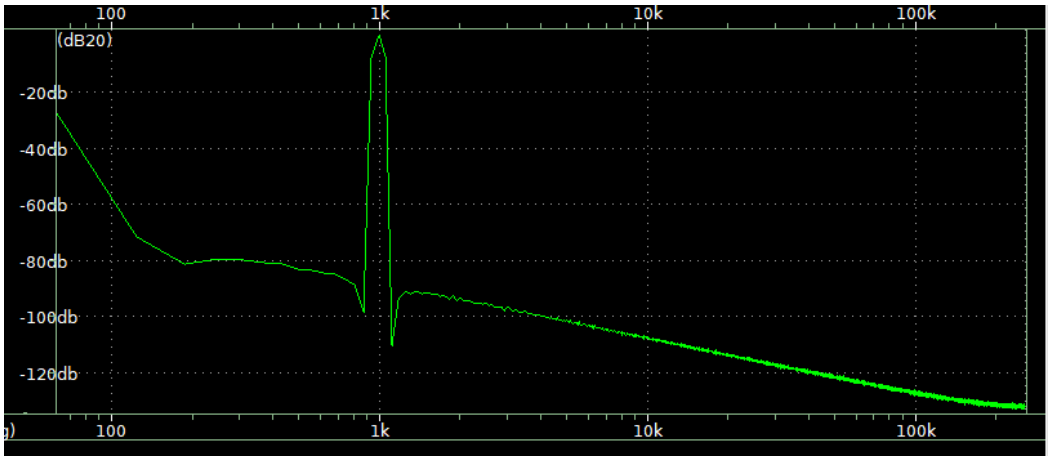
```
zin_1k= 100.1185k
zin_5k= 100.1034k
zin_10k= 100.1075k
zin_15k= 100.1075k
zin_20k= 100.1114k
```

```
zout_1k=    3.9288
zout_5k=    3.9348
zout_10k=   3.9386
zout_15k=   3.9386
zout_20k=   3.9406
```

```
vout_peak=    3.5949      at=    1.2539m
                 from=    1.0000m     to=    2.0000m
vout_pp=      6.9542     from=    1.0000m     to=    2.0000m
pout_rms= 188.9099m
idd_avg= -41.6653m   from=    1.0000m     to=    2.0000m
iss_avg=   38.0003m  from=    1.0000m     to=    2.0000m
idd_peak=-117.6288m     at=    1.2540m
                 from=    1.0000m     to=    2.0000m
iss_peak= 110.2651m     at=    1.7536m
                 from=    1.0000m     to=    2.0000m
```

Test 5 shows that our circuit operates with low total harmonic distortion of -89dB. This is lower than the maximum threshold of -60dB.

```
thd_db= -89.5445  up to the harmonic:   40
sndr_db=    4.3801
```



MEASURED RESULTS

When we tested our soldered design using 9v batteries, a signal generator, and an oscilloscope, we recorded the following results. 3dB bandwidth: 18Hz - 25KHz with a midband gain of 8.1. The input impedance was 101kΩ and the output impedance was 3.95Ω. The output power reached 171mW RMS. Our THD was measured to be -82dB. The discrepancy in output power is likely because our simulated I_{SS} exceeds the value achievable by 9v batteries, leading to attenuated output power in real life. The THD is also slightly greater than simulated, likely due to human error in soldering and imperfections in the audio cable and jacks.