TODO

Lab1:

1. Display entire reg file on the vga
   1. Completed with CMN push on 11/26
      1. Need to test with changing reg file values once datapath is fixed
2. Fix the damn thing, honestly it is very difficult to know where it went wrong

Lab2:

1. Send characters over UART, maybe with a FIFO (created 128 deep)
   1. Create FSM to write one char of output to FIFO from bus output
   2. a way to send the ALU/Benchmark results over UART, or really any character
   3. a way to send the RegFile over UART when halt is triggered
   4. a way to insert a /r when /n is entered automatically
   5. show the entered/received character from UART (maybe display on 7seg)
2. Ensure that UART is being received, IE some form of indicator that UART was received
   1. Complete via UART LED

Lab3:

1. Clock gating
   1. gate everything that doesn’t have an FSM to start with
2. Other than that I am not sure what can be done, it seems very difficult to multiplex anything
   1. Route the ALU mode through the actual ALU? And maybe the matrix mac part