APB SRAM Core Verification Plan

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# Introduction

## About APB Verification Environment

A standalone APB master verification IP is developed for using it as testbench with APB SRAM Core. The UVM testbench structure is shown in the following figure:

Top

Tests

Sequences

Agent\_Config

Scoreboard

Environment

Coverage Monitor

Sequencer

Agent

Env\_Config

Monitor

Driver

Seq\_item

APB\_SRAM (DUT)