1 Introduction

Today, the most modern method for providing telephony is IP-telephony. But communication via the Internet isn't always possible, or you need to connect to the phone, that is connected to the traditional phone network, not to the IP-network. So in such cases, the use of the VoIP-gateway is actual.

VoIP-gateway — a gateway, designed to transfer voice traffic between the networks of traditional telephony and data network. The article studies digital VoIP-gateway that is joined to the E1-carrier. Existing implementation of the gateway based on the DSP was analyzed. The reasons of switching the hardware basis for the gateway from DSP to FPGA were stated. The VoIP-gateway implantation to the system was also examined and analyzed.

The purpose of work is to design and to implement on FPGA gateway for transformation of the audio data from packet-switching network to circuit-switching network. The designing device will be a part of VoIP-gateway. The device should work in the specific conditions that are determined.

2 Analysis of existing implementation

DSP Texas Instruments TMS320C6455CTZ with clock frequency 1 GHz employs at existing implementation of the E1 interface board. Functional diagram of the gateway is shown in figure 1. Software for DSP is written in C. It works under control of DSP-BIOS operating system.

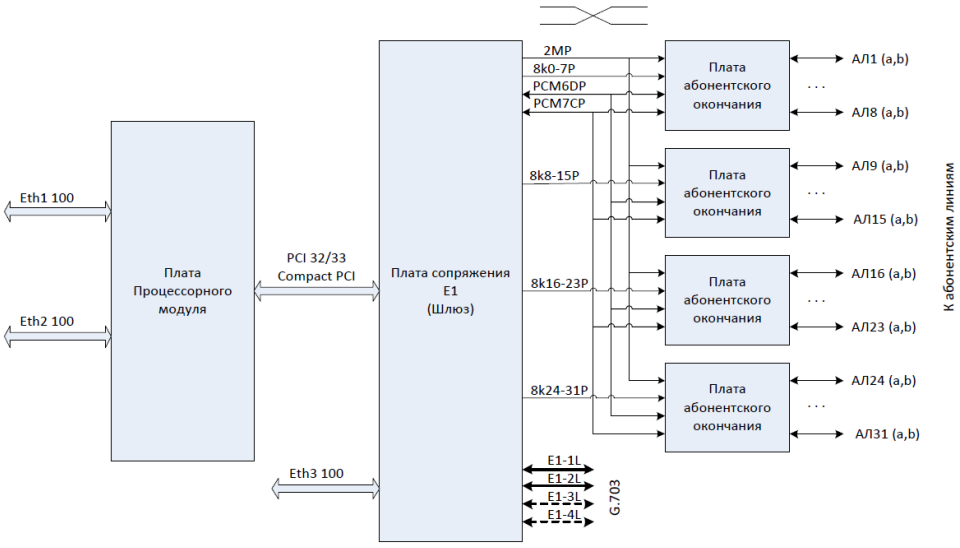

Fig.1

DSP processes incoming from the processor module packages, determines their types, allocates by channels data and control signals and sends them to the appropriate PCM tracts. Also DSP forms packages of different types receiving data from PCM tracts, including RTP-packages, and sends them to processor module on the PCI bus. In addition to these tasks on DSP interrupt handlers, timers and watchdog timer, logger task for monitoring processor status and various functions library are implemented.

At the moment, some of the functions performed by E1interface board are excess:

- No need to use external telephone lines;
- No need of echo cancellation function and conversion of voice data in different formats;
- Use of DSP and additional switch chip is unjustified.

Hence follows the need to change the hardware basis for the E1 interface board and to remove unnecessary elements of this board. New chosen basis is FPGA Altera. The reasons for the change of DSP to FPGA and for modification of element base are:

- Price reduction of project base;

- Simplification of the software certification using FPGA;
- Device optimization;
- Reducing weight and size characteristics of the board.

3 Gateway developing

The general scheme of the developed device from the environment Quartus II is shown in Figure 2. The scheme contains the following blocks:

- Data receiving block from the CPU clipboard (buff);
- Data sending block via PCM (snd);
- Data receiving block from PCM (rcv);
- Channel control block (control);
- PLL megafunction.

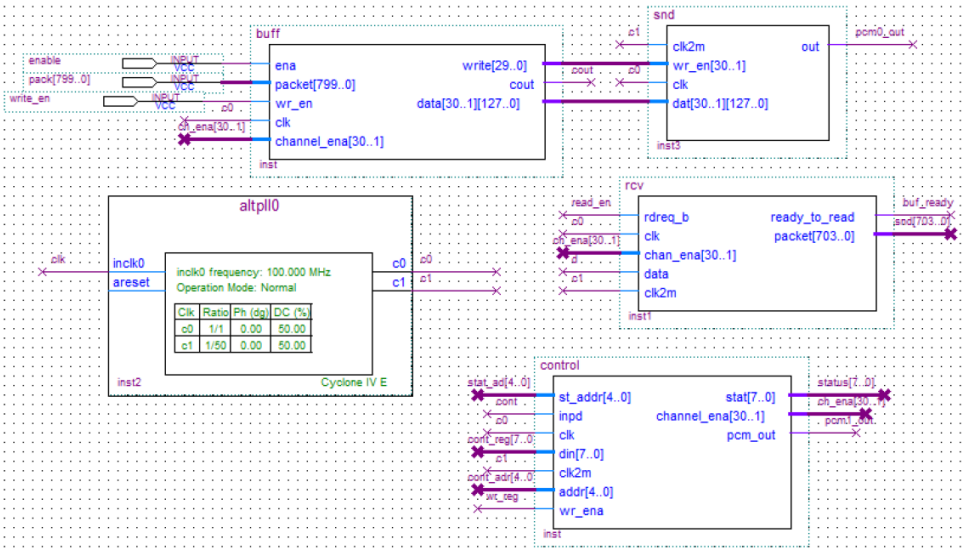

Fig.2

As a result gateway for transformation of the audio data from packet-switching network to circuit-switching network was developed. Gateway consists

of IP blocks implemented in hardware description language Verilog HDL. Gateway contains 2 digital E1 carriers. Data is transmitted by one carrier, control signals — by another.

4 Device testing

The developed device was tested on the evaluation board miniDiLaB-CIV. Tests showed that the device works correctly, specifically control signaling channels and data transfer channels. Also, the interaction with the processor module was simulated. Received from the „processor module“packages were successfully passed through data transmission loop and then correctly formed at the exit of the developed device.

5 Conclusion

Based on the hardware expenses obtained by compilation of the project, as a new hardware basis for the gateway Altera FPGA of Cyclone V series 5CEBA4F17I7N was selected. This FPGA contains 3 464 192 bits (422 KB) of built-in memory and 49 000 built-in logic elements. The cost of this FPGA is 74$. This is approximately three times less than the cost of DSP.

Further development of the project involves the optimization of device designed for a specific FPGA (namely 5CEBA4F17I7N), prototyping board design and verification of the device on the breadboard with a connection to the processing unit via the PCI bus.