POWERTIP TECH. CORP.

DISPLAY DEVICES FOR BETTER ELECTRONIC DESIGN

Specification For Approval

Customer : _____

Model Type : LCD Module

Sample Code : _____

Mass Production Code : PG12864LRS-ANN-B

Edit : 0

Customer Sign	Sales Sign	Approved By	Prepared By

CONTENTS

1. SPECIFICATIONS

1.1 Features

- Full dot-matrix structure with 128 dots *64 dots
- 1/64 Duty, 1/9 bias
- STN LCD, positive, gray
- Transflective LCD
- 6 o'clock viewing angle
- 8 bits parallel data input ,without controller IC
- Built-in negative voltage and LED backlight

1.2 Mechanical Specifications

- Outline dimension : 93.0mm(L) *70.0mm(W)*14.0mm max.(H)
- Viewing area : 72.0mm *40.0mm
- Active area : 66.52mm *33.24mm
- Dot size : 0.48mm *0.48mm
- Dot pitch : 0.52mm *0.52mm

1.3 Absolute Maximum Ratings

Item	Symbol	Conditions	Min.	Max.	Unit
Power supply Voltage	VDD	-	4.5	5.5	V
LCD drive Supply voltage	VDD-VEE	-	8.0	17	V
Input voltage	VIN	-	-0.3	VDD+0.3	V
Operating temperature	TOPR	-	0	40	°C
Storage temperature	TSTG	-	-20	60	°C
Humidity*1	HD	-	-	90	%RH

1.4 DC Electrical Characteristics

VDD=+5V±10%,VSS=0V,TA=25°C

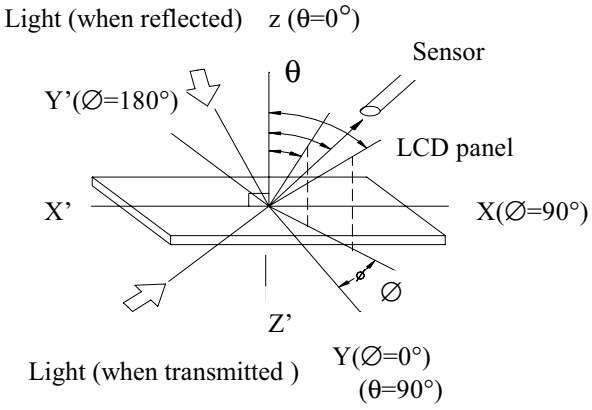
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Logic Supply voltage	VDD	-	4.5	5	5.5	V
"H" input voltage	VIH	-	0.7VDD	-	VDD	V
"L" input voltage	VIL	-	0	-	0.3VDD	V
"H" output voltage	VOH	-	VDD-0.4	-	-	V
"L" output voltage	VOL	-	-	-	0.4	V
Supply current	IDD	VDD=5V	-	-	13	mA
LCD driving voltage	VOP	VDD-VO	-	9.4	-	V

1.5 Optical Characteristics

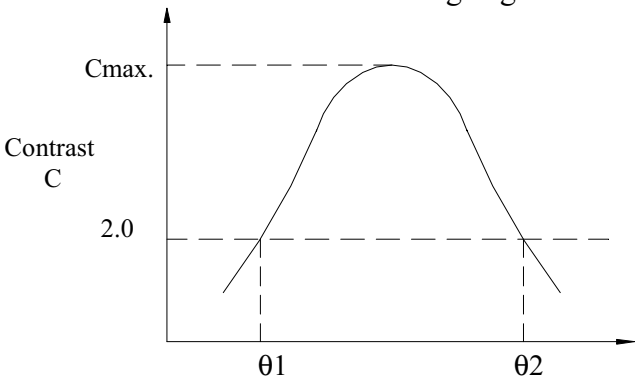
1/64 duty, 1/9 bias, Vopr=9.5V, Ta=25°C

Item	Symbol	Conditions	Min.	Typ.	Max	Reference
Viewing angle	θ	C≥2.0,∅=0°C	35°	-	-	Notes 1 & 2
Contrast	C	θ=5°, ∅=0°	-	3	-	Note 3
Response time(rise)	tr	θ=5°, ∅=0°	-	130ms	200ms	Note 4
Response time(fall)	tf	θ=5°, ∅=0°	-	300ms	500ms	Note 4

Note 1: Definition of angles θ and ∅



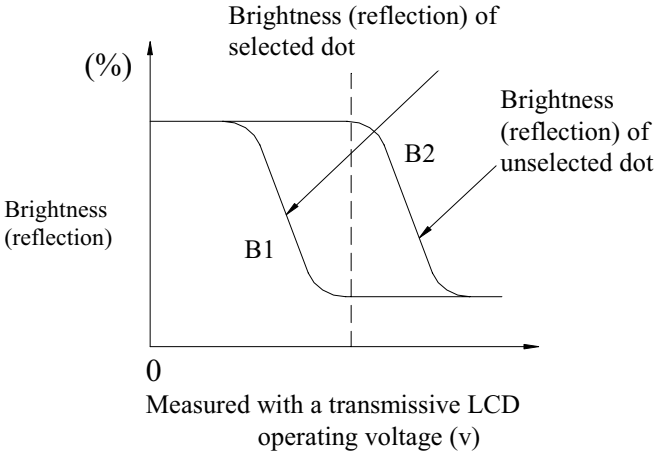
Note 2: Definition of viewing angles θ1 and θ2



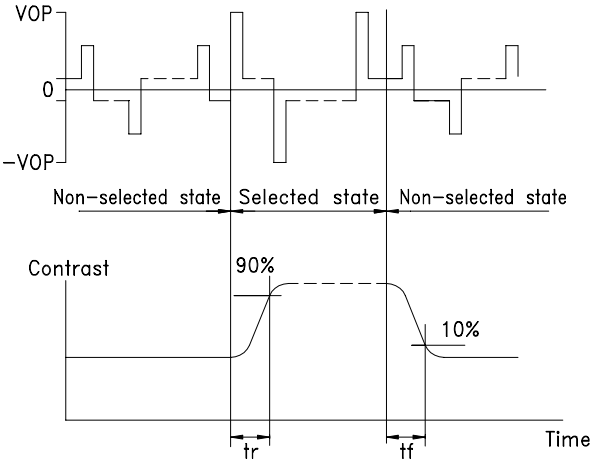
Note : Optimum viewing angle with the naked eye and viewing angle θ at Cmax. Above are not always the same

Note 3: Definition of contrast C

$$C = \frac{\text{Brightness (reflection) of unselected dot (B2)}}{\text{Brightness (reflection) of selected dot (B1)}}$$



Note 4: Definition of response time



Note:

panel which is displayed 1 cm^2

V_{OPR} : Operating voltage f_{FRM} : Frame frequency

t_r : Response time (rise) t_f : Response time (fall)

1.6 Backlight Characteristic

The LCD Module is using a LED backlight

•.Maximum Ratings

Item	Symbol	Conditions	Min.	Max.	Unit
Forward current	IF	TA=25°C	-	975	mA
Reverse voltage	VR	TA=25°C	-	8	V
Power dissipation	PO	TA=25°C	-	4.5	W
Operating Temperature	TOPR	-	-20	70	°C
Storage temperature	TSTG	-	-40	80	°C

•.Electrical Ratings

TA=25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Forward voltage	VF	IF=390mA	-.	4.2	4.6	V
Reverse current	IR	VR=8V	-	-	0.2	mA
Luminous intensity	IV	IF=390mA	184	230	-	cd/m^2
Wavelength	λp	IF=390mA	565	-	571	nm
Color	Yellow Green					

2. MODULE STRUCTURE

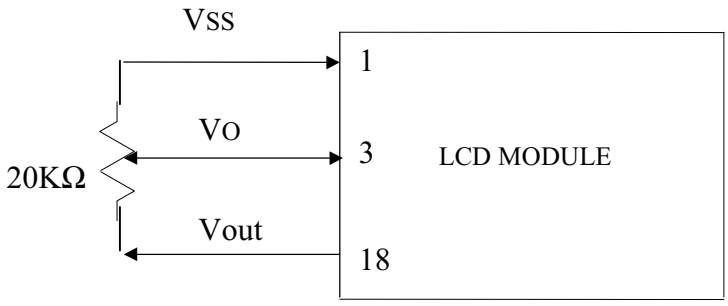
2.1 Counter Drawing

*See Appendix

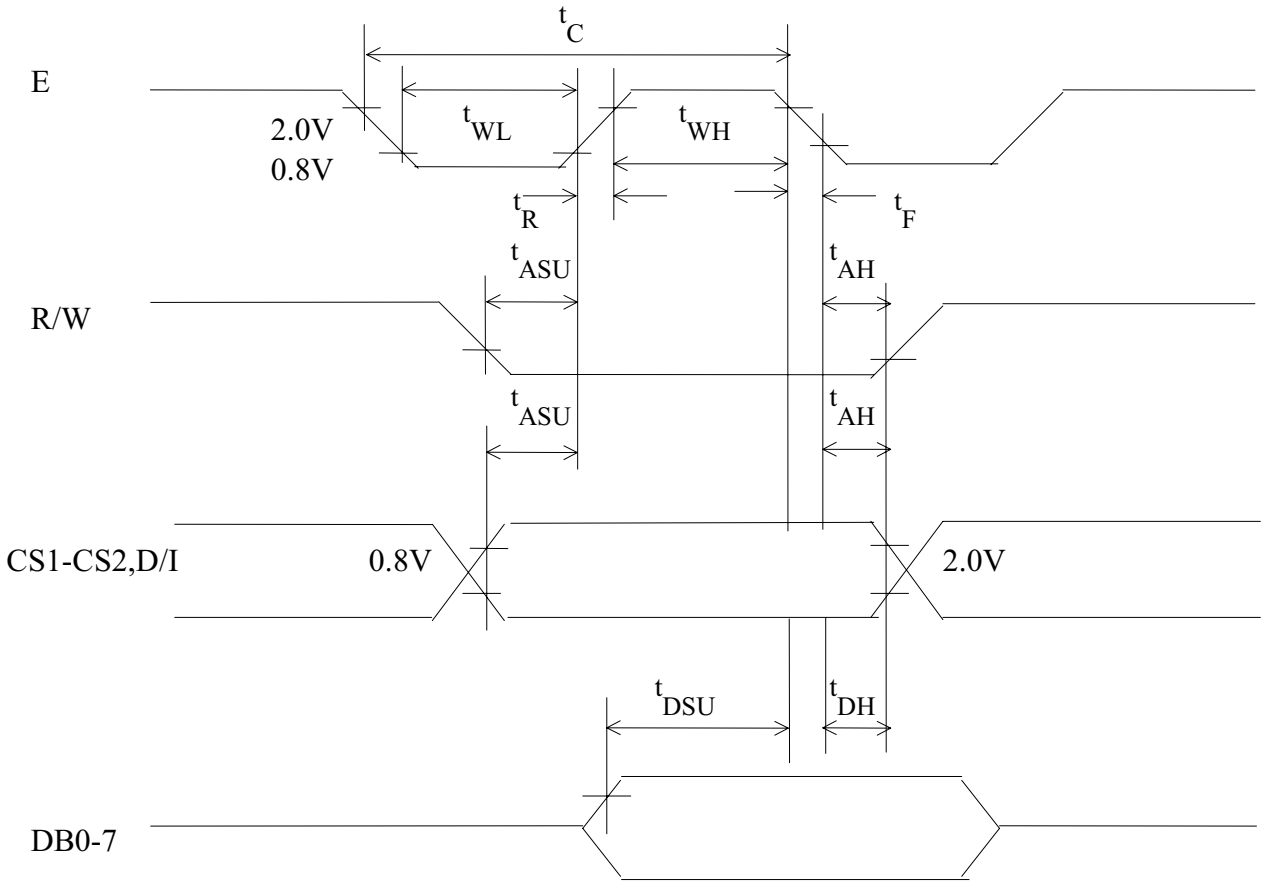
2.2 Interface Pin Description

Pin No.	Symbol	Function
1	VSS	Signal ground (GND)
2	VDD	Power supply for logic (+5V)
3	Vo	Operating voltage for LCD (variable)
4	D/$\overline{I}$	Register selection input High =Data register Low =Instruction register (for write) Busy flag address counter (for read)
5	R/$\overline{W}$	R/W signal input is used to select the read/write mode High =Read mode, Low =Write mode
6	E	Start enable signal to read or write the data
7-10	DB0~ DB3	Four low order bi-directional three-state data bus lines. Use for data transfer between the MPU and the LCD module. These four are not used during 4-bit operation.
11-14	DB4~ DB7	For high order bi-directional three-state data bus lines. Used for data transfer between the MPU and the LCD module. DB7 can be used as a busy flag.
15	CS1	Chip enable for D2 (segment 1 to segment 64)
16	CS2	Chip enable for D3 (segment 65 to segment 128)
17	$\overline{RST}$	Reset signal
18	Vout	Negative voltage power supply
19	A	Power supply for LED backlight (+)
20	K	Power supply for LED backlight (-)

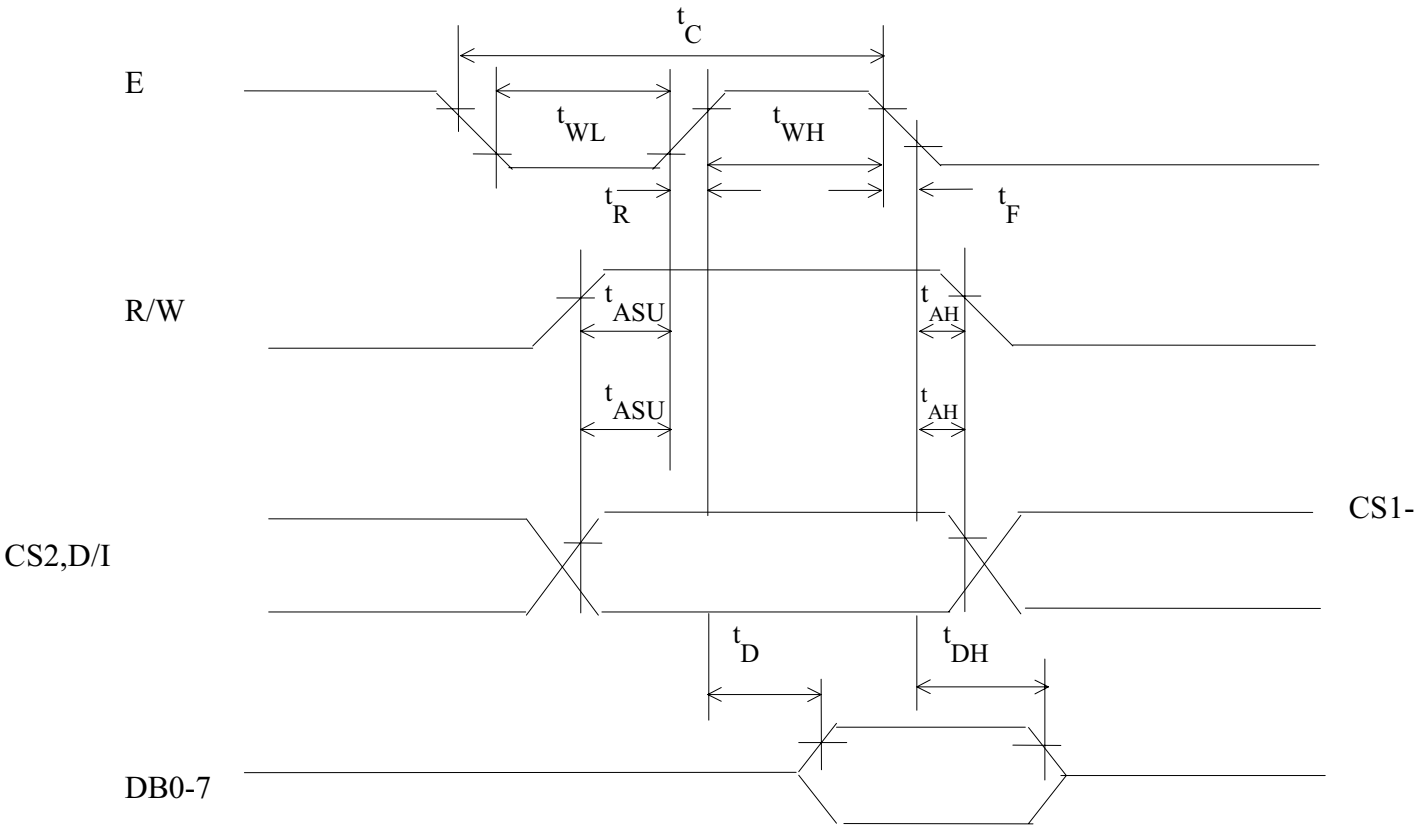
Contrast Adjust



2.3 Timing Characteristics



MPU write timing



MPU read timing

Characteristic	Symbol	Min.	Typ	Max	Unit
E Cycle	tC	1000	-	-	ns
E High Level Width	tWH	450	-	-	ns
E Low Level Width	tWL	450	-	-	ns
E Rise Time	tR	-	-	25	ns
E Fall Time	tF	-	-	25	ns
Address Set-Up time	tASU	140	-	-	ns
Address Hold Time	tAH	10	-	-	ns
Data Set-Up Time	tSU	200		-	ns
Data Delay Time	tD	-	-	320	ns
Data Hold Time (Write)	tDHW	10	-	-	ns
Data Hold Time (Read)	tDHR	20	-	-	ns

2.4 Display command

Instructions	Code R/W	D/I	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Functions	
Display on/off	0	0	0	0	1	1	1	1	1	1/0	Controls display on/off. RAM data and internal status are not affected.	
Display start line	0	0	1	1	Display start line (0-63)						Specifies the RAM line displayed at the top of the screen.	
Set Page (x address)	0	0	1	0	1	1	1	Page (0-7)			Sets the page (X address) of RAM at the page (X address) register.	
Set Y address	0	0	0	1	Y address (0-63)						Sets the Y address in the Y address in the counter.	
Status read	1	0	Busy	0	ON/ OFF	Reset	0	0	0	0	Reads the status. Reads 1: Reset 0: Normal ON/OFF 1: Display off 0: Display on Busy 1: Internal operation 0: Ready	
Write display data	0	1	Write data								Writes data DB0 (LSB) to DB7 (MSB) on the data bus into display RAM.	Has access to the address of the display RAM specified in advance. After the access, Y address is increased by 1.
Read display data	1	1	Read data								Reads data DB0 (LSB) to DB7 (MSB) from the display RAM to the data bus.	

Detailed Explanation

Display On/Off

	R/W	D/I	DB7							DB0
Code	0	0	0	0	1	1	1	1	1	D
			MSB							LSB

The display data appears when D is 1 and disappears when D is 0. Though the data is not on the screen with D=0, it remains in the display data RAM. Therefore, you can make it appear by changing D=0 into D=1.

Display Start Line

	R/W	D/I	DB7							DB0
Code	0	0	1	1	A	A	A	A	A	A
			MSB							LSB

Z address AAAAAA (binary) of the display data RAM is set in the display start line register and displayed at the top of the screen. Figure 1 shows examples of display (1/64 duty cycle) when the start line=0-3. When the display duty cycle is 1/64 or more (ex. 1/32, 1/24 etc.), the data of total line number of LCD screen, from the line specified by display start line instruction, is displayed.
See figure 1.

Set page (X address)

	R/W	D/I	DB7							DB0
Code	0	0	1	0	1	1	1	A	A	A
			MSB							LSB

X address AAA (binary) of the display data RAM is set in the X address register. After that, writing or reading to or from MPU is executed in this specified page until the next page is set. See figure 2.

Set Y Address

	R/W	D/I	DB7							DB0
Code	0	0	0	1	A	A	A	A	A	A
			MSB							LSB

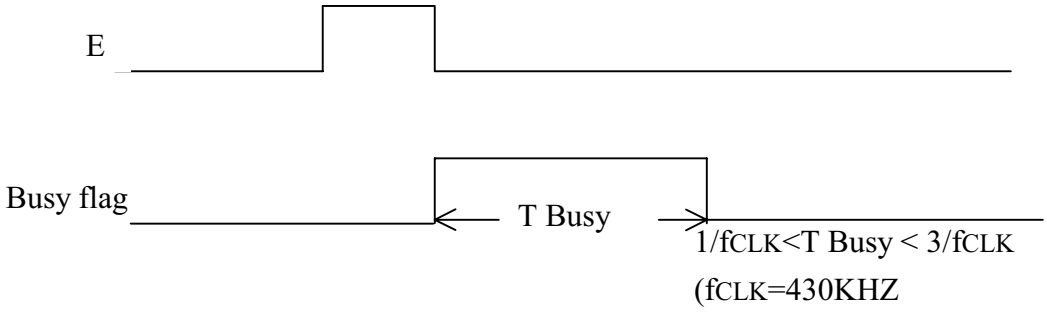
Y address AAAAAA (binary) of the display data RAM is set in the Y address Counter. After that, Y address counter is increased by 1 every time the data is written or read to or from MPU.

Status Read

	R/W	D/I	DB7							DB0
Code	1	0	BUSY	0	ON/OFF	REST	0	0	0	0
			MSB							LS

• Busy
When busy is 1, the LSI is executing internal operations. No instructions are accepted while busy is 1,

so you should make sure that busy is 0 before writing the next instruction.



• ON/OFF

Shows the liquid crystal display conditions: on condition or off condition.

When on/off is 1, the display is in off condition.
When on/off is 0, the display is in on condition.

• RESET

RESET=1 shows that the system is being initialized. In this condition, no instructions except status read can be accepted.
RESET=0 shows that initializing has finished and the system is in the usual operation condition.

Write Display Data

	R/W	D/I	DB7……	….						DB0
Code	0	1	D	D	D	D	D	D	D	D
			MSB							LSB

Write 8-bit data DDDDDDDD (binary) into the display data RAM. Then Y address is increased by 1 automatically.

Read Display Data

	R/W	D/I	DB7……							DB0
Code	1	1	D	D	D	D	D	D	D	D
			MSB							LSB

Reads out 8-bit data DDDDDDDD (binary) from the display data RAM. Then Y address is increased by 1 automatically.
One dummy read is necessary right after the address setting. For details, refer to the explanation of output register in “Function of Each Block”.

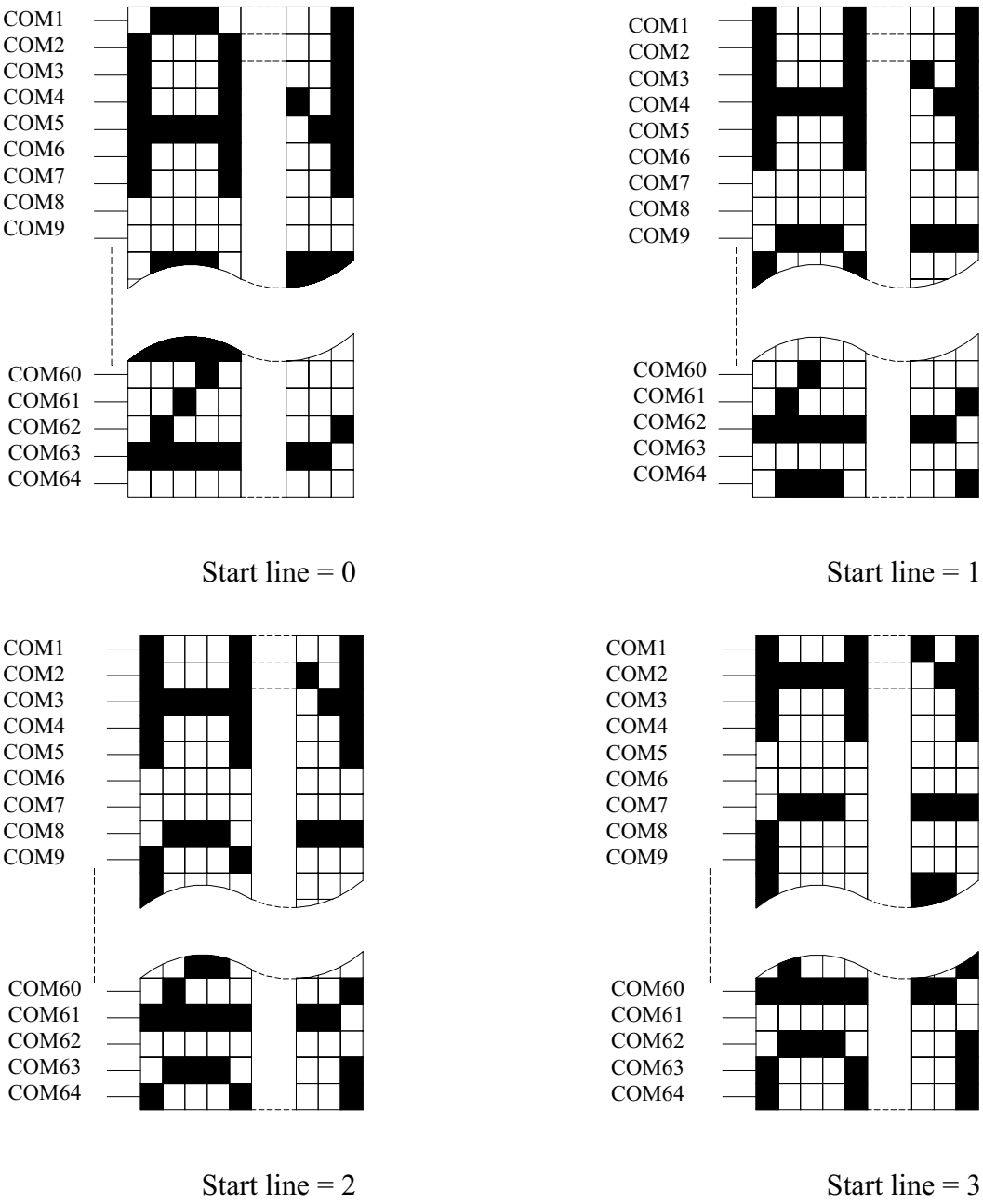


Figure 1 Relation between Start Line and Display

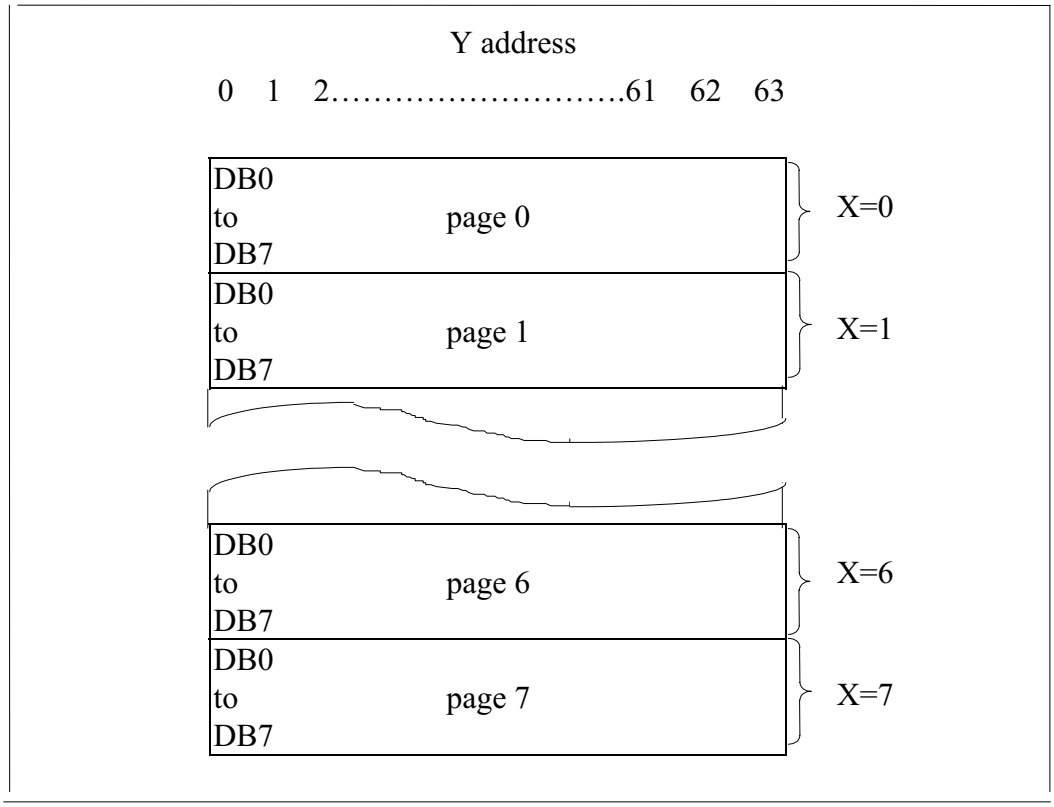


Figure 2 Address Configuration of Display Data RAM

Note: “128*64” consist of 2 “64*64”

CS1⇒ Chip enable for left 64*64 (segment1 to segment 64)

CS2⇒ Chip enable for right 64*64 (segment 65 to segment 128)