**[如何分析 Linux 核心 RISC-V 架構相關程式碼](https://tinylab.org/riscv-linux-quickstart/)**

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By Falcon of [TinyLab.org](https://tinylab.org/) Mar 09, 2022

**1 背景簡介**

本次 **RISC-V Linux 核心剖析** 活動的主要目標是分析 Linux 核心對 RISC-V 架構的相關支援，因此，重點是分析 Linux 核心的 arch/riscv 目錄。

有兩個方向可以去分析，一個是直接分析 arch/riscv 的目錄結構，另外一個是分析 arch/riscv 相關的歷史改動。

但是通常可以把兩者結合起來，如果把現有的 arch/riscv 目錄結構比作一棟建好的房子，那 arch/riscv 歷史改動能呈現房子的建設過程，地基怎麼打，骨架怎麼放，一磚一瓦如何新增進去，都有完整的記錄和描述。

本次活動的目標核心版本是 Linux v5.17，由於 v5.17 還未發佈，本文先以 v5.16 為例，待 v5.17 正式版本發佈以後，後續輸出以 v5.17 為基準。另外，本次活動以 riscv64 為主。

**2 準備好 Linux 核心程式碼倉庫**

由於 Linux 核心程式碼很大，特別是本次活動需要用到 git 倉庫，下載體驗無法保障，不建議自行去下載。

可以考慮用本次活動推薦的 [Linux Lab](https://gitee.com/tinylab/linux-lab) 實驗環境，已經對下載做了透明加速，直接用 make kernel-download 直接下載。

也可以直接在某寶選購免安裝即插即用的 Linux Lab Disk 智能隨身繫統盤，已經預先幫忙下載好了較新的核心原始碼（v5.16, v5.17-rcX），僅需通過 git fetch --all 更新到後續的 v5.17 正式版。

Linux Lab 或 Linux Lab Disk 還提供了本活動後續要用到的 RISC-V Linux 核心編譯和運行環境。

在 Linux Lab Disk 下，可以用桌面的 Linux Lab Shell 登陸，登陸後默認就在 /labs/linux-lab 工作目錄。對於自行安裝的情況，請參考使用手冊用 tools/docker/bash 登陸。

接下來，需要切換到 riscv64/virt 虛擬開發板並克隆出一套 v5.16 組態。

1. **$ make BOARD=riscv64/virt**
2. **$ make kernel-clone LINUX\_NEW=v5.16**

**說明**：riscv64/virt 虛擬開發板僅向活動參與者開放，其他使用者可在選購 Linux Lab Disk 後申請內建。

Linux Lab 默認把 Linux 核心原始碼放置在 src/linux-stable 目錄：

1. **$ make kernel-download**
2. **$ cd src/linux-stable**

為了聚焦本次活動，基礎環境的搭建部分將不再過多介紹，請參考 [相關手冊](https://gitee.com/link?target=https%3A%2F%2Ftinylab.org%2Fpdfs%2Flinux-lab-v0.9-manual-zh.pdf) 和 [演示視訊](https://www.cctalk.com/m/group/88948325)。

**3 arch/riscv 目錄結構**

這裡用 tree 工具展示一下整體的結構，大概瞭解一下框架和位置就行：

1. **$ tree arch/riscv/**
2. **├── boot**
3. **│   ├── dts *# device tree support***
4. **│   │   ├── canaan**
5. **│   │   │   ├── canaan\_kd233.dts**
6. **│   │   │   ├── k210.dtsi**
7. **│   │   │   ├── k210\_generic.dts**
8. **│   │   │   ├── Makefile**
9. **│   │   │   ├── sipeed\_maix\_bit.dts**
10. **│   │   │   ├── sipeed\_maix\_dock.dts**
11. **│   │   │   ├── sipeed\_maixduino.dts**
12. **│   │   │   └── sipeed\_maix\_go.dts**
13. **│   │   ├── Makefile**
14. **│   │   ├── microchip**
15. **│   │   │   ├── Makefile**
16. **│   │   │   ├── microchip-mpfs.dtsi**
17. **│   │   │   └── microchip-mpfs-icicle-kit.dts**
18. **│   │   └── sifive**
19. **│   │   ├── fu540-c000.dtsi**
20. **│   │   ├── fu740-c000.dtsi**
21. **│   │   ├── hifive-unleashed-a00.dts**
22. **│   │   ├── hifive-unmatched-a00.dts**
23. **│   │   └── Makefile**
24. **│   ├── install.sh**
25. **│   ├── loader.lds.S**
26. **│   ├── loader.S**
27. **│   └── Makefile**
28. **├── configs *# default configuration***
29. **│   ├── defconfig**
30. **│   ├── nommu\_k210\_defconfig**
31. **│   ├── nommu\_k210\_sdcard\_defconfig**
32. **│   ├── nommu\_virt\_defconfig**
33. **│   └── rv32\_defconfig**
34. **├── errata *# errata (cpu bug fixup)***
35. **│   ├── alternative.c**
36. **│   ├── Makefile**
37. **│   └── sifive**
38. **│   ├── errata.c**
39. **│   ├── errata\_cip\_453.S**
40. **│   └── Makefile**
41. **├── include *# headers***
42. **│   ├── asm**
43. **│   │   ├── alternative.h**
44. **│   │   ├── alternative-macros.h**
45. **│   │   ├── asm.h**
46. **│   │   ├── asm-offsets.h**
47. **│   │   ├── asm-prototypes.h**
48. **│   │   ├── atomic.h**
49. **│   │   ├── barrier.h**
50. **│   │   ├── bitops.h**
51. **│   │   ├── bug.h**
52. **│   │   ├── cacheflush.h**
53. **│   │   ├── cache.h**
54. **│   │   ├── cacheinfo.h**
55. **│   │   ├── clint.h**
56. **│   │   ├── clocksource.h**
57. **│   │   ├── cmpxchg.h**
58. **│   │   ├── cpu\_ops.h**
59. **│   │   ├── csr.h**
60. **│   │   ├── current.h**
61. **│   │   ├── delay.h**
62. **│   │   ├── efi.h**
63. **│   │   ├── elf.h**
64. **│   │   ├── errata\_list.h**
65. **│   │   ├── fence.h**
66. **│   │   ├── fixmap.h**
67. **│   │   ├── ftrace.h**
68. **│   │   ├── futex.h**
69. **│   │   ├── gdb\_xml.h**
70. **│   │   ├── hugetlb.h**
71. **│   │   ├── hwcap.h**
72. **│   │   ├── image.h**
73. **│   │   ├── io.h**
74. **│   │   ├── irqflags.h**
75. **│   │   ├── irq.h**
76. **│   │   ├── irq\_work.h**
77. **│   │   ├── jump\_label.h**
78. **│   │   ├── kasan.h**
79. **│   │   ├── Kbuild**
80. **│   │   ├── kdebug.h**
81. **│   │   ├── kexec.h**
82. **│   │   ├── kgdb.h**
83. **│   │   ├── kprobes.h**
84. **│   │   ├── linkage.h**
85. **│   │   ├── mmio.h**
86. **│   │   ├── mmiowb.h**
87. **│   │   ├── mmu\_context.h**
88. **│   │   ├── mmu.h**
89. **│   │   ├── mmzone.h**
90. **│   │   ├── module.h**
91. **│   │   ├── module.lds.h**
92. **│   │   ├── numa.h**
93. **│   │   ├── page.h**
94. **│   │   ├── parse\_asm.h**
95. **│   │   ├── patch.h**
96. **│   │   ├── pci.h**
97. **│   │   ├── perf\_event.h**
98. **│   │   ├── pgalloc.h**
99. **│   │   ├── pgtable-32.h**
100. **│   │   ├── pgtable-64.h**
101. **│   │   ├── pgtable-bits.h**
102. **│   │   ├── pgtable.h**
103. **│   │   ├── probes.h**
104. **│   │   ├── processor.h**
105. **│   │   ├── ptdump.h**
106. **│   │   ├── ptrace.h**
107. **│   │   ├── sbi.h**
108. **│   │   ├── seccomp.h**
109. **│   │   ├── sections.h**
110. **│   │   ├── set\_memory.h**
111. **│   │   ├── smp.h**
112. **│   │   ├── soc.h**
113. **│   │   ├── sparsemem.h**
114. **│   │   ├── spinlock.h**
115. **│   │   ├── spinlock\_types.h**
116. **│   │   ├── stackprotector.h**
117. **│   │   ├── stacktrace.h**
118. **│   │   ├── string.h**
119. **│   │   ├── switch\_to.h**
120. **│   │   ├── syscall.h**
121. **│   │   ├── thread\_info.h**
122. **│   │   ├── timex.h**
123. **│   │   ├── tlbflush.h**
124. **│   │   ├── tlb.h**
125. **│   │   ├── uaccess.h**
126. **│   │   ├── unistd.h**
127. **│   │   ├── uprobes.h**
128. **│   │   ├── vdso**
129. **│   │   │   ├── clocksource.h**
130. **│   │   │   ├── gettimeofday.h**
131. **│   │   │   ├── processor.h**
132. **│   │   │   └── vsyscall.h**
133. **│   │   ├── vdso.h**
134. **│   │   ├── vendorid\_list.h**
135. **│   │   ├── vermagic.h**
136. **│   │   ├── vmalloc.h**
137. **│   │   └── word-at-a-time.h**
138. **│   └── uapi**
139. **│   └── asm**
140. **│   ├── auxvec.h**
141. **│   ├── bitsperlong.h**
142. **│   ├── bpf\_perf\_event.h**
143. **│   ├── byteorder.h**
144. **│   ├── elf.h**
145. **│   ├── hwcap.h**
146. **│   ├── Kbuild**
147. **│   ├── perf\_regs.h**
148. **│   ├── ptrace.h**
149. **│   ├── sigcontext.h**
150. **│   ├── ucontext.h**
151. **│   └── unistd.h**
152. **├── Kbuild *# Build support with configurations enabled in Kconfig***
153. **├── Kconfig *# Configuration support for defconfig, menuconfig ...***
154. **├── Kconfig.debug**
155. **├── Kconfig.erratas**
156. **├── Kconfig.socs**
157. **├── kernel**
158. **│   ├── asm-offsets.c *# tasks support, required to generate asm-offsets.h, see Documentation/kbuild/makefiles.rst and Kbuild***
159. **│   ├── cacheinfo.c *# cache support***
160. **│   ├── cpu.c *# /proc/cpuinfo***
161. **│   ├── cpufeature.c *# hwcap***
162. **│   ├── cpu-hotplug.c *# cpu hotplug***
163. **│   ├── cpu\_ops.c**
164. **│   ├── cpu\_ops\_sbi.c**
165. **│   ├── cpu\_ops\_spinwait.c**
166. **│   ├── crash\_dump.c *# crash support***
167. **│   ├── crash\_save\_regs.S**
168. **│   ├── efi.c *# UEFI boot support***
169. **│   ├── efi-header.S**
170. **│   ├── entry.S *# entries for exceptions and interrupts***
171. **│   ├── fpu.S *# fpu***
172. **│   ├── ftrace.c *# ftrace***
173. **│   ├── head.h**
174. **│   ├── head.S *# boot code***
175. **│   ├── image-vars.h**
176. **│   ├── irq.c *# irqs***
177. **│   ├── jump\_label.c *# [jump\_label](https://lwn.net/Articles/412072/), required by tracepoint***
178. **│   ├── kexec\_relocate.S *# kexec***
179. **│   ├── kgdb.c *# kgdb***
180. **│   ├── machine\_kexec.c *# kexec***
181. **│   ├── Makefile**
182. **│   ├── mcount-dyn.S *# ftrace***
183. **│   ├── mcount.S**
184. **│   ├── module.c *# module support***
185. **│   ├── module-sections.c**
186. **│   ├── patch.c**
187. **│   ├── perf\_callchain.c *# perf***
188. **│   ├── perf\_event.c**
189. **│   ├── perf\_regs.c**
190. **│   ├── probes *# kprobes & uprobes***
191. **│   │   ├── decode-insn.c**
192. **│   │   ├── decode-insn.h**
193. **│   │   ├── ftrace.c**
194. **│   │   ├── kprobes.c**
195. **│   │   ├── kprobes\_trampoline.S**
196. **│   │   ├── Makefile**
197. **│   │   ├── simulate-insn.c**
198. **│   │   ├── simulate-insn.h**
199. **│   │   └── uprobes.c**
200. **│   ├── process.c *# scheduling***
201. **│   ├── ptrace.c *# ptrace***
202. **│   ├── reset.c *# reboot***
203. **│   ├── riscv\_ksyms.c**
204. **│   ├── sbi.c *# sbi***
205. **│   ├── setup.c *# setup\_arch (dtb parse, ioremap setup, jump label init, efi init, paging init, mem init, res init, sbi init, kasan init, setup smp)***
206. **│   ├── signal.c *# signal***
207. **│   ├── smpboot.c *# smp***
208. **│   ├── smp.c**
209. **│   ├── soc.c *# soc init***
210. **│   ├── stacktrace.c *# stacktrace***
211. **│   ├── syscall\_table.c *# syscall***
212. **│   ├── sys\_riscv.c**
213. **│   ├── time.c *# time***
214. **│   ├── traps.c *# traps***
215. **│   ├── traps\_misaligned.c**
216. **│   ├── vdso *# vdso***
217. **│   │   ├── flush\_icache.S**
218. **│   │   ├── getcpu.S**
219. **│   │   ├── Makefile**
220. **│   │   ├── note.S**
221. **│   │   ├── rt\_sigreturn.S**
222. **│   │   ├── so2s.sh**
223. **│   │   ├── vdso.lds.S**
224. **│   │   ├── vdso.S**
225. **│   │   └── vgettimeofday.c**
226. **│   ├── vdso.c**
227. **│   ├── vmlinux.lds.S *# vmlinux linker script***
228. **│   └── vmlinux-xip.lds.S *# xip support***
229. **├── lib *# libs***
230. **│   ├── delay.c**
231. **│   ├── error-inject.c**
232. **│   ├── Makefile**
233. **│   ├── memcpy.S**
234. **│   ├── memmove.S**
235. **│   ├── memset.S**
236. **│   ├── tishift.S**
237. **│   └── uaccess.S**
238. **├── Makefile**
239. **├── mm *# memory management***
240. **│   ├── cacheflush.c**
241. **│   ├── context.c**
242. **│   ├── extable.c *# extable***
243. **│   ├── fault.c**
244. **│   ├── hugetlbpage.c *# hugetlb***
245. **│   ├── init.c**
246. **│   ├── kasan\_init.c *# kasan***
247. **│   ├── Makefile**
248. **│   ├── pageattr.c**
249. **│   ├── physaddr.c**
250. **│   ├── ptdump.c**
251. **│   └── tlbflush.c**
252. **└── net**
253. **├── bpf\_jit\_comp32.c *# eBPF***
254. **├── bpf\_jit\_comp64.c**
255. **├── bpf\_jit\_core.c**
256. **├── bpf\_jit.h**
257. **└── Makefile**
258. **19 directories, 237 files**

涉及到具體程式碼檔案和程式碼行改動的時候，可以用 git log 和 git blame 輔助查看。

1. **$ git log arch/riscv/kernel/mcount.S**
2. **$ git blame -L 103,103 arch/riscv/kernel/mcount.S**

涉及到程式碼函數定義的尋找部分可以參考本文後續章節介紹的 cscope 用法。

**4 arch/riscv 歷史改動**

可以直接通過 git log arch/riscv 查看 arch/riscv 目錄的所有改動。

首先找出來 arch/riscv 的第一筆改動：

1. **$ git log --oneline arch/riscv**
2. **...**
3. **fab957c11efe RISC-V: Atomic and Locking Code**
4. **76d2a0493a17 RISC-V: Init and Halt Code**

因為內容比較多，下面的指令只列出每個 Commit 的標題（--oneline），並按照逆序的方式排列（--reverse），也過濾掉了部分非核心的程式碼（egrep），從而方便從頭開始一筆一筆分析。

1. **$ git rev-list --oneline 76d2a0493a17^..v5.16 --reverse arch/riscv \**
2. **| egrep -v " Merge | Backmerge | dts| kbuild| asm-generic| firmware| include| Documentation| Revert| drivers | config | Rename"**
3. **76d2a0493a17 RISC-V: Init and Halt Code**
4. **fab957c11efe RISC-V: Atomic and Locking Code**
5. **5d8544e2d007 RISC-V: Generic library routines and assembly**
6. **2129a235c098 RISC-V: ELF and module implementation**
7. **7db91e57a0ac RISC-V: Task implementation**
8. **6d60b6ee0c97 RISC-V: Device, timer, IRQs, and the SBI**
9. **07037db5d479 RISC-V: Paging and MMU**
10. **e2c0cdfba7f6 RISC-V: User-facing API**
11. **fbe934d69eb7 RISC-V: Build Infrastructure**
12. **b7e5a591502b RISC-V: Remove \_\_vdso\_cmpxchg{32,64} symbol versions**
13. **28dfbe6ed483 RISC-V: Add VDSO entries for clock\_get/gettimeofday/getcpu**
14. **4650d02ad2d9 RISC-V: Remove unused arguments from ATOMIC\_OP**
15. **8286d51a6c24 RISC-V: Comment on why {,cmp}xchg is ordered how it is**
16. **61a60d35b7d1 RISC-V: Remove \_\_smp\_bp\_\_{before,after}\_atomic**
17. **3343eb6806f3 RISC-V: Remove smb\_mb\_\_{before,after}\_spinlock()**
18. **9347ce54cd69 RISC-V: \_\_test\_and\_op\_bit\_ord should be strongly ordered**
19. **21db403660d1 RISC-V: Add READ\_ONCE in arch\_spin\_is\_locked()**
20. **c901e45a999a RISC-V: `sfence.vma` orderes the instruction cache**
21. **bf7305527343 RISC-V: remove spin\_unlock\_wait()**
22. **5ddf755e4439 RISC-V: use generic serial.h**
23. **5e6f82b0fe7b RISC-V: use RISCV\_{INT,SHORT} instead of {INT,SHORT} for asm macros**
24. **fe2726af9fdc RISC-V: io.h: type fixes for warnings**
25. **83e7b8769a08 RISC-V: move empty\_zero\_page definition to C and export it**
26. **24948b7ec0f3 RISC-V: Export some expected symbols for modules**
27. **4bde63286a6c RISC-V: Provide stub of setup\_profiling\_timer()**
28. **4a41d5dbb0bb RISC-V: Use define for get\_cycles like other architectures**
29. **08f051eda33b RISC-V: Flush I$ when making a dirty page executable**
30. **921ebd8f2c08 RISC-V: Allow userspace to flush the instruction cache**
31. **da894ff100be RISC-V: \_\_io\_writes should respect the length argument**
32. **07f8ba7439f9 RISC-V: User-Visible Changes**
33. **7382fbdeae0d RISC-V: \_\_io\_writes should respect the length argument**
34. **3b62de26cf5e RISC-V: Fixes for clean allmodconfig build**
35. **5e454b5457b5 riscv: use linux/uaccess.h, not asm/uaccess.h...**
36. **c895f6f703ad bpf: correct broken uapi for BPF\_PROG\_TYPE\_PERF\_EVENT program type**
37. **86ad5c97ce5c RISC-V: Logical vs Bitwise typo**
38. **3cfa5008081d RISC-V: Resurrect smp\_mb\_\_after\_spinlock()**
39. **27b017452532 RISC-V: Remove unused CONFIG\_HVC\_RISCV\_SBI code**
40. **33c57c0d3c67 RISC-V: Add a basic defconfig**
41. **9e49a4ed072a RISC-V: Make \_\_NR\_riscv\_flush\_icache visible to userspace**
42. **c163fb38ca34 riscv: remove CONFIG\_MMU ifdefs**
43. **1125203c13b9 riscv: rename SR\_\* constants to match the spec**
44. **b8ee205af46c riscv: remove the unused dma\_capable helper**
45. **0500871f21b2 Construct init thread stack in the linker script rather than by union**
46. **c5cd037d1c80 dma-mapping: provide a generic asm/dma-mapping.h**
47. **002e67454f61 dma-direct: rename dma\_noop to dma\_direct**
48. **3e076a7e0492 RISC-V: Remove duplicate command-line parsing logic**
49. **5d44bf2065e1 RISC-V: Remove mem\_end command line processing**
50. **10626c32e382 riscv/ftrace: Add basic support**
51. **0b5030c8c052 riscv: remove unused \_\_ARCH\_HAVE\_MMU define**
52. **509009ccfa53 riscv: remove redundant unlikely()**
53. **fe9b842f7292 riscv: disable SUM in the exception handler**
54. **f1b65f20fb05 RISC-V: Limit the scope of TLB shootdowns**
55. **5ec9c4ff0430 riscv: add ZONE\_DMA32**
56. **0ca7a0b7c13e riscv: remove the unused current\_pgdir function**
57. **372def1f9341 riscv: don't read back satp in paging\_init**
58. **7549cdf59d9f riscv: rename sptbr to satp**
59. **4889dec6c87d riscv: inline set\_pgdir into its only caller**
60. **ab0dc41b7324 riscv: Remove ARCH\_WANT\_OPTIONAL\_GPIOLIB select**
61. **2aaa2dc31bee riscv: kconfig: Remove RISCV\_IRQ\_INTC select**
62. **89a4b4441206 riscv: Remove ARCH\_HAS\_ATOMIC64\_DEC\_IF\_POSITIVE select**
63. **bcae803a2131 RISC-V: Enable IRQ during exception handling**
64. **ab4af6053410 riscv/barrier: Define \_\_smp\_{mb,rmb,wmb}**
65. **cc6c98485f8e RISC-V: Move to the new GENERIC\_IRQ\_MULTI\_HANDLER handler**
66. **a90f590a1bee mm: add ksys\_mmap\_pgoff() helper; remove in-kernel calls to sys\_mmap\_pgoff()**
67. **a1d2a6b4cee8 riscv/ftrace: Add RECORD\_MCOUNT support**
68. **c15ac4fd60d5 riscv/ftrace: Add dynamic function tracer support**
69. **bc1a4c3a8425 riscv/ftrace: Add dynamic function graph tracer support**
70. **71e736a7d655 riscv/ftrace: Add ARCH\_SUPPORTS\_FTRACE\_OPS support**
71. **aea4c671fb98 riscv/ftrace: Add DYNAMIC\_FTRACE\_WITH\_REGS support**
72. **b785ec129bd9 riscv/ftrace: Add HAVE\_FUNCTION\_GRAPH\_RET\_ADDR\_PTR support**
73. **8d235b174af5 riscv/barrier: Define \_\_smp\_{store\_release,load\_acquire}**
74. **0123f4d76ca6 riscv/spinlock: Strengthen implementations with fences**
75. **5ce6c1f3535f riscv/atomic: Strengthen implementations with fences**
76. **ab1ef68e5401 RISC-V: Add sections of PLT and GOT for kernel module**
77. **b8bde0ef12bd RISC-V: Add section of GOT.PLT for kernel module**
78. **da975dd4818c RISC-V: Support GOT\_HI20/CALL\_PLT relocation type in kernel module**
79. **e1910c72bdc4 RISC-V: Support CALL relocation type in kernel module**
80. **e7456e696bff RISC-V: Support HI20/LO12\_I/LO12\_S relocation type in kernel module**
81. **56ea45ae2392 RISC-V: Support RVC\_BRANCH/JUMP relocation type in kernel modulewq**
82. **29e405cd88c3 RISC-V: Support ALIGN relocation type in kernel module**
83. **8e691b16769d RISC-V: Support ADD32 relocation type in kernel module**
84. **4aad074c9c1d RISC-V: Support SUB32 relocation type in kernel module**
85. **4a632cec8884 RISC-V: Enable module support in defconfig**
86. **e21d54219c7a RISC-V: Add definition of relocation types**
87. **2c9046b71bb6 RISC-V: Assorted memory model fixes**
88. **7a8e7da42250 RISC-V: Fixes to module loading**
89. **86e11757d8b2 riscv: select DMA\_DIRECT\_OPS instead of redefining it**
90. **5b7252a26870 riscv: there is no <asm/handle\_irq.h>**
91. **85602bea297f RISC-V: build vdso-dummy.o with -no-pie**
92. **3eb0f5193b49 signal: Ensure every siginfo we send has all bits initialized**
93. **4d6a20b13558 signal/riscv: Use force\_sig\_fault where appropriate**
94. **7ff3a7621dda signal/riscv: Replace do\_trap\_siginfo with force\_sig\_fault**
95. **325ef1857fff PCI: remove PCI\_DMA\_BUS\_IS\_PHYS**
96. **6e88628d03dd dma-debug: remove CONFIG\_HAVE\_DMA\_API\_DEBUG**
97. **2ff075c7dfd4 drivers: base: cacheinfo: setup DT cache properties early**
98. **c3e4ed012ba7 riscv: simplify Kconfig magic for 32-bit vs 64-bit kernels**
99. **f1306f0423ec riscv: only enable ZONE\_DMA32 for 64-bit**
100. **10314e09d044 riscv: add swiotlb support**
101. **ebcbd75e3962 riscv: Fix the bug in memory access fixup code**
102. **178e9fc47aae perf: riscv: preliminary RISC-V support**
103. **32c81bced356 RISC-V: Preliminary Perf Support**
104. **2861ae302f6b riscv: use NULL instead of a plain 0**
105. **9bf97390b303 riscv: no \_\_user for probe\_kernel\_address()**
106. **3010a5ea665a mm: introduce ARCH\_HAS\_PTE\_SPECIAL**
107. **86406d51d360 riscv: split the declaration of \_\_copy\_user**
108. **889d746edd02 riscv: add riscv-specific predefines to CHECKFLAGS**
109. **1dd985229d5f riscv/ftrace: Export \_mcount when DYNAMIC\_FTRACE isn't set**
110. **77aa85de16ae RISC-V: Handle R\_RISCV\_32 in modules**
111. **e0e0c87c022b RISC-V: Make our port sparse-clean**
112. **24a130ccfe58 RISC-V: Add CONFIG\_HVC\_RISCV\_SBI=y to defconfig**
113. **8b47038e6d34 atomics/treewide: Remove redundant atomic\_inc\_not\_zero() definitions**
114. **bef828204a1b atomics/treewide: Make atomic64\_inc\_not\_zero() optional**
115. **eccc2da8c03f atomics/treewide: Make atomic\_fetch\_add\_unless() optional**
116. **2b523f170e39 atomics/riscv: Define atomic64\_fetch\_add\_unless()**
117. **18cc1814d4e7 atomics/treewide: Make test ops optional**
118. **9837559d8eb0 atomics/treewide: Make unconditional inc/dec ops optional**
119. **d5fad48cfb4b RISC-V: Add conditional macro for zone of DMA32**
120. **8f79125d285d RISC-V: Select GENERIC\_UCMPDI2 on RV32I**
121. **c480d8911fda RISC-V: Add definiion of extract symbol's index and type for 32-bit**
122. **7df85002178e RISC-V: Change variable type for 32-bit compatible**
123. **781c8fe2da3d RISC-V: fix R\_RISCV\_ADD32/R\_RISCV\_SUB32 relocations**
124. **f67f10b8a6c9 riscv: remove unnecessary of\_platform\_populate call**
125. **1db9b80980d2 RISC-V: Fix PTRACE\_SETREGSET bug.**
126. **9a6a51154f8b RISC-V: Fix the rv32i kernel build**
127. **fd2efaa4eb53 locking/atomics: Rework ordering barriers**
128. **06ec64b84c35 Kconfig: consolidate the "Kernel hacking" menu**
129. **4938c79bd0f5 RISC-V: Use KBUILD\_CFLAGS instead of KCFLAGS when building the vDSO**
130. **a89757daf25c RISC-V: implement \_\_lshrti3.**
131. **758914fea278 RISC-V: Don't increment sepc after breakpoint.**
132. **5b5c2a2c44d7 RISC-V: Add early printk support via the SBI console**
133. **b9490350f751 RISC-V: remove timer leftovers**
134. **b9d5535746e3 RISC-V: simplify software interrupt / IPI code**
135. **4b40e9ddc892 RISC-V: remove INTERRUPT\_CAUSE\_\* defines from asm/irq.h**
136. **bec2e6ac353d RISC-V: add a definition for the SIE SEIE bit**
137. **6ea0f26a7913 RISC-V: implement low-level interrupt handling**
138. **62b019436814 clocksource: new RISC-V SBI timer driver**
139. **94f592f0e5b9 RISC-V: Add the directive for alignment of stvec's value**
140. **8237f8bc4f6e irqchip: add a SiFive PLIC driver**
141. **4c42ae4f6ab7 RISC-V: Fix !CONFIG\_SMP compilation error**
142. **50a7ca3c6fc8 mm: convert return type of handle\_mm\_fault() caller to vm\_fault\_t**
143. **7847e7052fc3 RISC-V: Define sys\_riscv\_flush\_icache when SMP=n**
144. **66eb957df4c7 riscv: Delete asm/compat.h**
145. **7a3b1bf70b37 RISC-V: Fix sys\_riscv\_flush\_icache**
146. **0ce5671c4450 riscv: tlb: Provide definition of tlb\_flush() before including tlb.h**
147. **47d80a68f10d RISC-V: Use a less ugly workaround for unused variable warnings**
148. **e866d3e84eb7 riscv: Do not overwrite initrd\_start and initrd\_end**
149. **67314ec7b025 RISC-V: Request newstat syscalls**
150. **ef1f2258748b RISCV: Fix end PFN for low memory**
151. **f28380185193 signal: Remove the need for \_\_ARCH\_SI\_PREABLE\_SIZE and SI\_PAD\_SIZE**
152. **e68ad867f77e Extract FPU context operations from entry.S**
153. **007f5c358957 Refactor FPU code in signal setup/return procedures**
154. **e8be53023302 Cleanup ISA string setting**
155. **9671f7061433 Allow to disable FPU support**
156. **9411ec60c23d Auto-detect whether a FPU exists**
157. **7f47c73b355f RISC-V: Build tishift only on 64-bit**
158. **51858aaf9bea RISC-V: Use swiotlb on RV64 only**
159. **757331db9214 RISC-V: Select GENERIC\_LIB\_UMODDI3 on RV32**
160. **827a438156e4 RISC-V: Avoid corrupting the upper 32-bit of phys\_addr\_t in ioremap**
161. **1ed4237ab616 RISC-V: No need to pass scause as arg to do\_IRQ()**
162. **566d6c428ead RISC-V: Don't set cacheinfo.{physical\_line\_partition,attributes}**
163. **19ccf29bb18f RISC-V: Filter ISA and MMU values in cpuinfo**
164. **b18d6f05252d RISC-V: Comment on the TLB flush in smp\_callin()**
165. **6db170ff4c08 RISC-V: Disable preemption before enabling interrupts**
166. **9639a44394b9 RISC-V: Provide a cleaner raw\_smp\_processor\_id()**
167. **46373cb442c5 RISC-V: Use mmgrab()**
168. **a37d56fc4011 RISC-V: Use WRITE\_ONCE instead of direct access**
169. **6825c7a80f18 RISC-V: Add logical CPU indexing for RISC-V**
170. **f99fb607fb2b RISC-V: Use Linux logical CPU number instead of hartid**
171. **4b26d22fdff1 RISC-V: Show CPU ID and Hart ID separately in /proc/cpuinfo**
172. **8b20d2db0a6d RISC-V: Show IPI stats**
173. **1760debb51f7 RISC-V: Don't set cacheinfo.{physical\_line\_partition,attributes}**
174. **86e581e31078 RISC-V: Mask out the F extension on systems without D**
175. **b8c8a9590e4f RISC-V: Add FP register ptrace support for gdb.**
176. **b90edb33010b RISC-V: Add futex support.**
177. **f31b8de98853 RISC-V: remove the unused return\_to\_handler export**
178. **ee5928843a93 riscv: move GCC version check for ARCH\_SUPPORTS\_INT128 to Kconfig**
179. **aef53f97b505 RISC-V: Cosmetic menuconfig changes**
180. **4e4101cfefd3 riscv: Add support to no-FPU systems**
181. **a6de21baf637 RISC-V: Fix some RV32 bugs and build failures**
182. **d26c4bbf9924 RISC-V: SMP cleanup and new features**
183. **de0d22e50cd3 treewide: remove current\_text\_addr**
184. **b4a991ec584b mm: remove CONFIG\_NO\_BOOTMEM**
185. **aca52c398389 mm: remove CONFIG\_HAVE\_MEMBLOCK**
186. **c6ffc5ca8fb3 memblock: rename free\_all\_bootmem to memblock\_free\_all**
187. **732e8e4130ff RISC-V: properly determine hardware caps**
188. **9b4789eacb65 Move EM\_RISCV into elf-em.h**
189. **ef70696a63c7 lib: Remove umoddi3 and udivmoddi4**
190. **ba1f0d955769 RISC-V: refresh defconfig**
191. **4ab49461d9d9 RISC-V: defconfig: Enable printk timestamps**
192. **10febb3ecace riscv: fix spacing in struct pt\_regs**
193. **f157d411a9eb riscv: add missing vdso\_install target**
194. **85d90b91807b RISC-V: lib: Fix build error for 64-bit**
195. **ef3a61406618 RISC-V: Silence some module warnings on 32-bit**
196. **21f70d4abf9e RISC-V: Fix raw\_copy\_{to,from}\_user()**
197. **c0fbcd991860 RISC-V: Build flat and compressed kernel images**
198. **0138ebb90c63 riscv: fix warning in arch/riscv/include/asm/module.h**
199. **27f8899d6002 riscv: add asm/unistd.h UAPI header**
200. **5d8f81ba1da5 RISC-V: recognize S/U mode bits in print\_isa**
201. **e949b6db51dc riscv/function\_graph: Simplify with function\_graph\_enter()**
202. **3731c3d4774e dma-mapping: always build the direct mapping code**
203. **55897af63091 dma-direct: merge swiotlb\_dma\_ops into the dma\_direct code**
204. **2b3f786408c5 RISC-V: defconfig: Enable RISC-V SBI earlycon support**
205. **7ba12bb676c2 RISC-V: Remove EARLY\_PRINTK support**
206. **8636a1f9677d treewide: surround Kconfig file paths with double quotes**
207. **8b699616f399 riscv, atomic: Add #define's for the atomic\_{cmp,}xchg\_\*() variants**
208. **94f9bf118f1e RISC-V: Fix of\_node\_\* refcount**
209. **cd378dbb3daf RISC-V: add of\_node\_put()**
210. **397182e0db56 riscv: remove unused variable in ftrace**
211. **3aed8c43267e RISC-V: Update Kconfig to better handle CMDLINE**
212. **358f3fff5271 RISC-V: Move from EARLY\_PRINTK to SBI earlycon**
213. **a266cdba17b3 RISC-V: lib: minor asm cleanup**
214. **9b9afe4a0ef1 RISC-V: Select GENERIC\_SCHED\_CLOCK for clocksource drivers**
215. **96d4f267e40f Remove 'type' argument from access\_ok() function**
216. **4cf58924951e mm: treewide: remove unused address argument from pte\_alloc functions**
217. **8c4fa8b8d483 riscv: remove redundant kernel-space generic-y**
218. **d4ce5458ea1b arch: remove stale comments "UAPI Header export list"**
219. **d6e4b3e326d8 arch: remove redundant UAPI generic-y defines**
220. **22e6a2e14cb8 RISC-V: Make BSS section as the last section in vmlinux.lds.S**
221. **8fd6e05c7463 arch: riscv: support kernel command line forcing when no DTB passed**
222. **37a107ff6dcd riscv: don't stop itself in smp\_send\_stop**
223. **2cffc9569050 RISC-V: Support MODULE\_SECTIONS mechanism on RV32**
224. **efe75c494f57 riscv: add audit support**
225. **0aea89430a4c riscv: audit: add audit hook in do\_syscall\_trace\_enter/exit()**
226. **45ef1aa8a0e3 riscv: define NR\_syscalls in unistd.h**
227. **008e901b7028 riscv: define CREATE\_TRACE\_POINTS in ptrace.c**
228. **775800b0f1d7 riscv: fix trace\_sys\_exit hook**
229. **5aeb1b36cedd riscv: add HAVE\_SYSCALL\_TRACEPOINTS to Kconfig**
230. **801009424e05 Fix a handful of audit-related issue**
231. **99fd6e875d0c RISC-V: Add \_TIF\_NEED\_RESCHED check for kernel thread when CONFIG\_PREEMPT=y**
232. **2bb10639f12c RISC-V: fix bad use of of\_node\_put**
233. **8581f38742cf RISC-V: asm/page.h: fix spelling mistake "CONFIG\_64BITS" -> "CONFIG\_64BIT"**
234. **86cca81a31cd RISC-V: Kconfig: fix spelling mistake "traget" -> "target"**
235. **a37ead8f2efb RISC-V: defconfig: Move CONFIG\_PCI{,E\_XILINX}**
236. **e4cf9e47ab24 RISC-V: defconfig: Enable Generic PCIE by default**
237. **2a200fb9fb12 RISC-V: defconfig: Add CRYPTO\_DEV\_VIRTIO=y**
238. **28198c4639b3 riscv: fixup max\_low\_pfn with PFN\_DOWN.**
239. **ae662eec8a51 riscv: Adjust mmap base address at a third of task size**
240. **2353ecc6f91f bpf, riscv: add BPF JIT for RV64G**
241. **e3613bb8afc2 riscv: Add pte bit to distinguish swap from invalid**
242. **7265d103902c riscv: add missing newlines to printk messages**
243. **e1b1381b3179 riscv: use pr\_info and friends**
244. **149820c6cf3c riscv: fix riscv\_of\_processor\_hartid() comment**
245. **e3d794d555cd riscv: treat cpu devicetree nodes without status as enabled**
246. **dd81c8ab819d riscv: use for\_each\_of\_cpu\_node iterator**
247. **79a47bad61bb riscv: remove the HAVE\_KPROBES option**
248. **ff4c25f26a71 dma-mapping: improve selection of dma\_declare\_coherent availability**
249. **680f9b8e6c56 RISC-V: Setup init\_mm before parse\_early\_param()**
250. **0651c263c8e3 RISC-V: Move setup\_bootmem() to mm/init.c**
251. **6f1e9e946f0b RISC-V: Move setup\_vm() to mm/init.c**
252. **f2c17aabc917 RISC-V: Implement compile-time fixed mappings**
253. **823900cd0130 RISC-V: Free-up initrd in free\_initrd\_mem()**
254. **d4c08b9776b3 riscv: Use latest system call ABI**
255. **ce246c444a08 riscv: io: Update \_\_io\_[p]ar() macros to take an argument**
256. **e15c6e37066e RISC-V: Do not wait indefinitely in \_\_cpu\_up**
257. **78d1daa36489 RISC-V: Move cpuid to hartid mapping to SMP.**
258. **ba15c86185e9 RISC-V: Remove NR\_CPUs check during hartid search from DT**
259. **dd641e268673 RISC-V: Allow hartid-to-cpuid function to fail.**
260. **291debb38dbb RISC-V: Compare cpuid with NR\_CPUS before mapping.**
261. **fbdc6193dc70 RISC-V: Assign hwcap as per comman capabilities.**
262. **736706bee329 get rid of legacy 'get\_ds()' function**
263. **f7ccc35aa3bd arch: riscv: fix logic error in parse\_dtb**
264. **13fd5de06514 RISC-V: Fixmap support and MM cleanups**
265. **795c230604cb riscv/vdso: don't clear PG\_reserved**
266. **16add411645c syscall\_get\_arch: add "struct task\_struct \*" argument**
267. **dbee9c9c4584 riscv: fix accessing 8-byte variable from RV32**
268. **387181dcdb6c RISC-V: Always compile mm/init.c with cmodel=medany and notrace**
269. **ff0e2a7bd13f RISC-V: Fix FIXMAP\_TOP to avoid overlap with VMALLOC area**
270. **da4ed3787391 RISC-V: Use IS\_ENABLED(CONFIG\_CMODEL\_MEDLOW)**
271. **390a0c62c23c locking/rwsem: Remove rwsem-spinlock.c & use rwsem-xadd.c for all archs**
272. **10a16997db3d riscv: Fix syscall\_get\_arguments() and syscall\_set\_arguments()**
273. **b35f549df1d7 syscalls: Remove start and number from syscall\_get\_arguments() args**
274. **32d92586629a syscalls: Remove start and number from syscall\_set\_arguments() args**
275. **1b937e8faa87 RISC-V: Add separate defconfig for 32bit systems**
276. **f05badde4e20 RISC-V: Fix Maximum Physical Memory 2GiB option for 64bit systems**
277. **fa9833992d5f riscv/stacktrace: Remove the pointless ULONG\_MAX marker**
278. **7a64f3f1cffd riscv/signal: Fixup additional syscall restarting**
279. **5cfade5fdcc9 riscv: turn mm\_segment\_t into a struct**
280. **e28dcc77e8e8 riscv: remove unreachable big endian code**
281. **09afac77b6e8 riscv: remove CONFIG\_RISCV\_ISA\_A**
282. **df16c40cbfb4 riscv: clear all pending interrupts when booting**
283. **c637b911e066 riscv: simplify the stack pointer setup in head.S**
284. **ba9c0141941c riscv: cleanup the parse\_dtb calling conventions**
285. **877425424d6c riscv: remove unreachable !HAVE\_FUNCTION\_GRAPH\_RET\_ADDR\_PTR code**
286. **6ab77af4b0ee riscv: remove duplicate macros from ptrace.h**
287. **bed137870663 riscv: print the unexpected interrupt cause**
288. **bf0102a0fdd9 riscv: call pm\_power\_off from machine\_halt / machine\_power\_off**
289. **fd7f744caed8 riscv: vdso: drop unnecessary cc-ldoption**
290. **70114560b285 RISC-V: Add RISC-V specific arch\_match\_cpu\_phys\_id**
291. **ab3d26500547 RISC-V: Implement nosmp commandline option.**
292. **0d7b4a607d8f riscv: switch over to generic free\_initmem()**
293. **8b4302a442af RISC-V: Support nr\_cpus command line option.**
294. **f1f47c6ca34b RISC-V: Fix minor checkpatch issues.**
295. **196a14d45161 RISC-V: Use tabs to align macro values in asm/csr.h**
296. **6dcaf00487ca RISC-V: Add interrupt related SCAUSE defines in asm/csr.h**
297. **a3182c91ef4e RISC-V: Access CSRs using CSR numbers**
298. **58de77545e53 riscv: move flush\_icache\_{all,mm} to cacheflush.c**
299. **f6635f873a60 riscv: move switch\_mm to its own file**
300. **a21344dfc6ad riscv: fix sbi\_remote\_sfence\_vma{,\_asid}.**
301. **d18ebc274ca7 riscv: support trap-based WARN()**
302. **ee72e0e70cf7 riscv: Add the support for c.ebreak check in is\_valid\_bugaddr()**
303. **9a6e7af02f7f riscv: Support BUG() in kernel module**
304. **4c3aeb82a0f4 RISC-V: Avoid using invalid intermediate translations**
305. **a967a289f169 RISC-V: sifive\_l2\_cache: Add L2 cache controller driver for SiFive SoCs**
306. **8fef9900d43f riscv: fix locking violation in page fault handler**
307. **ec8f24b7faaf treewide: Add SPDX license identifier - Makefile/Kconfig**
308. **fe121ee531d1 bpf, riscv: clear target register high 32-bits for and/or/xor on ALU32**
309. **b4d0d230ccfb treewide: Replace GPLv2 boilerplate/reference with SPDX - rule 36**
310. **588cb88cedd5 treewide: Replace GPLv2 boilerplate/reference with SPDX - rule 120**
311. **66d0d5a854a6 riscv: bpf: eliminate zero extension code-gen**
312. **3cf5d076fb4d signal: Remove task parameter from force\_sig**
313. **6f25a967646a signal/riscv: Remove tsk parameter from do\_trap**
314. **351b6825b3a9 signal: Explicitly call force\_sig\_fault on current**
315. **2e1661d26736 signal: Remove the task parameter from force\_sig\_fault**
316. **2874c5fd2842 treewide: Replace GPLv2 boilerplate/reference with SPDX - rule 152**
317. **c942fddf8793 treewide: Replace GPLv2 boilerplate/reference with SPDX - rule 157**
318. **1802d0beecaf treewide: Replace GPLv2 boilerplate/reference with SPDX - rule 174**
319. **96ac6d435100 treewide: Add SPDX license identifier - Kbuild**
320. **1e692f09e091 bpf, riscv: clear high 32 bits for ALU32 add/sub/neg/lsh/rsh/arsh**
321. **33e42ef57197 locking/atomic, riscv: Fix atomic64\_sub\_if\_positive() offset argument**
322. **0754211847d7 locking/atomic, riscv: Use s64 for atomic64**
323. **50acfb2b76e1 treewide: Replace GPLv2 boilerplate/reference with SPDX - rule 286**
324. **bd305f259cd3 kconfig: make arch*/\*/configs/defconfig the default of KBUILD\_DEFCONFIG***
325. ***3b025f2bc989 RISC-V: defconfig: enable clocks, serial console***
326. ***405945588fee riscv: export pm\_power\_off again***
327. ***d0e1f2110a5e riscv: Fix udelay in RV32.***
328. ***8d4e048d60bd arch: riscv: add support for building DTB files from DT source data***
329. ***bf587caae305 riscv: mm: synchronize MMU after pte change***
330. ***259931fd3b96 riscv: remove unused barrier defines***
331. ***caab277b1de0 treewide: Replace GPLv2 boilerplate/reference with SPDX - rule 234***
332. ***d2912cb15bdd treewide: Replace GPLv2 boilerplate/reference with SPDX - rule 500***
333. ***91abaeaaff35 EDAC/sifive: Add EDAC platform driver for SiFive SoCs***
334. ***ad97f9df0fee riscv: add binfmt\_flat support***
335. ***ff8391e1b7d2 RISC-V: defconfig: enable MMC & SPI for RISC-V***
336. ***0db7f5cd4aeb riscv: mm: Fix code comment***
337. ***6dd91e0eacff RISC-V: defconfig: Enable NO\_HZ\_IDLE and HIGH\_RES\_TIMERS***
338. ***556024d41f39 riscv: Remove gate area stubs***
339. ***bbc5dc5155aa riscv: defconfig: enable SOC\_SIFIVE***
340. ***d90d45d7dcb7 RISC-V: Fix memory reservation in setup\_bootmem()***
341. ***9e953cda5cdf riscv: Introduce huge page support for 32/64bit kernel***
342. ***df7e9059cf6b riscv: ccache: Remove unused variable***
343. ***2ebca1cbb4a5 riscv: remove free\_initrd\_mem***
344. ***46dd3d7d287b bpf, riscv: Enable zext optimization for more RV64G ALU ops***
345. ***671f9a3e2e24 RISC-V: Setup initial page tables in two stages***
346. ***0f327f2aaad6 RISC-V: Add an Image header that boot loader can parse.***
347. ***d1b46fe50c8b riscv: switch to generic version of pte allocation***
348. ***b74c0cad3d5f riscv: drop unneeded -Wall addition***
349. ***2d69fbf3d01a riscv: fix build break after macro-to-function conversion in generic cacheflush.h***
350. ***56ac5e213933 riscv: enable sys\_clone3 syscall for rv64***
351. ***03f11f03dbfe RISC-V: Parse cpu topology during boot.***
352. ***d9c525229521 treewide: add "WITH Linux-syscall-note" to SPDX tag of uapi headers***
353. ***b399abe7c21e riscv: Fix perf record without libelf support***
354. ***b7edabfe8438 riscv: defconfig: align RV64 defconfig to the output of "make savedefconfig"***
355. ***66cc016ab7c7 riscv: delay: use do\_div() instead of \_\_udivdi3()***
356. ***81a48ee41738 RISC-V: Remove udivdi3***
357. ***eb93685847a9 riscv: fix flush\_tlb\_range() end address for flush\_tlb\_page()***
358. ***500bc2c1f48a riscv: rv32\_defconfig: Update the defconfig***
359. ***d568cb3f9351 riscv: defconfig: Update the defconfig***
360. ***8ac71d7e46b9 riscv: Correct the initialized flow of FP register***
361. ***69703eb9a8ae riscv: Make \_\_fstate\_clean() work correctly.***
362. ***a256f2e329df RISC-V: Fix FIXMAP area corruption on RV32 systems***
363. ***4f3f90084673 riscv: Using CSR numbers to access CSRs***
364. ***d95f1a542c3d RISC-V: Implement sparsemem***
365. ***909548d6c578 riscv: add arch/riscv/Kbuild***
366. ***dbeb90b0c1eb riscv: Add perf callchain support***
367. ***98a93b0b561c riscv: Add support for perf registers sampling***
368. ***7e0e50895fdf riscv: refactor the IPI code***
369. ***1db7a7ca5ac5 riscv: cleanup send\_ipi\_mask***
370. ***e11ea2a02b93 riscv: optimize send\_ipi\_single***
371. ***f5bf645d10f2 riscv: cleanup riscv\_cpuid\_to\_hartid\_mask***
372. ***2f12dbf190d9 riscv: don't use the rdtime(h) pseudo-instructions***
373. ***95594cb40c6e riscv: move the TLB flush logic out of line***
374. ***474efecb65dc riscv: modify the Image header to improve compatibility with the ARM64 header***
375. ***b6f2b2e600a2 RISC-V: Fix building error when CONFIG\_SPARSEMEM\_MANUAL=y***
376. ***b47613da3b71 arch/riscv: disable excess harts before picking main boot hart***
377. ***d3d7a0ce020e RISC-V: Export kernel symbols for kvm***
378. ***c82dd6d078a2 riscv: Avoid interrupts being erroneously enabled in handle\_exception()***
379. ***13224794cb08 mm: remove quicklist page table caches***
380. ***782de70c4293 mm: consolidate pgtable\_cache\_init() and pgd\_cache\_init()***
381. ***54c95a11cc1b riscv: make mmap allocation top-down by default***
382. ***b4ed71f557e4 mm: treewide: clarify pgtable\_page\_{ctor,dtor}() naming***
383. ***18856604b3e7 RISC-V: Clear load reservations while restoring hart contexts***
384. ***922b0375fc93 riscv: Fix memblock reservation for device tree blob***
385. ***8b04825ed205 riscv: avoid kernel hangs when trapped in BUG()***
386. ***e0c0fc18f10d riscv: avoid sending a SIGTRAP to a user thread trapped in WARN()***
387. ***8bb0daef64e5 riscv: Correct the handling of unexpected ebreak in do\_trap\_break()***
388. ***cd9e72b80090 RISC-V: entry: Remove unneeded need\_resched() loop***
389. ***2f01b7864188 riscv: remove the switch statement in do\_trap\_break()***
390. ***4c8eb19cf9dc riscv: tlbflush: remove confusing comment on local\_flush\_tlb\_all()***
391. ***5bf4e52ff031 RISC-V: fix virtual address overlapped in FIXADDR\_START and VMEMMAP\_START***
392. ***04ce8d3f40cd riscv: Use pr\_warn instead of pr\_warning***
393. ***90db7b220c9a riscv: fix fs/proc/kcore.c compilation with sparsemem enabled***
394. ***62103ece5236 riscv: Fix implicit declaration of 'page\_to\_section'***
395. ***9fe57d8c575d riscv: Fix undefined reference to vmemmap\_populate\_basepages***
396. ***a6d9e2672609 riscv: cleanup <asm/bug.h>***
397. ***e8f44c50dfe7 riscv: cleanup do\_trap\_break***
398. ***ffaee2728f9b riscv: add prototypes for assembly language functions from head.S***
399. ***6a527b6785ba riscv: init: merge split string literals in preprocessor directive***
400. ***bf6df5dd25b7 riscv: mark some code and data as file-static***
401. ***a48dac448d85 riscv: fp: add missing \_\_user pointer annotations***
402. ***f307307992bf riscv: for C functions called only from assembly, mark with \_\_visible***
403. ***00a5bf3a8ca3 RISC-V: Add PCIe I/O BAR memory mapping***
404. ***1edd28b7e85d RISC-V: Remove unsupported isa string info print***
405. ***5340627e3fe0 riscv: add support for SECCOMP and SECCOMP\_FILTER***
406. ***6384423f49c8 RISC-V: Do not invoke SBI call if cpumask is empty***
407. ***31738ede9b33 RISC-V: Issue a local tlbflush if possible.***
408. ***6efb16b1d551 RISC-V: Issue a tlb page flush if possible***
409. ***eaf937075c9a vmlinux.lds.h: Move NOTES into RO\_DATA***
410. ***93240b327929 vmlinux.lds.h: Replace RO\_DATA\_SECTION with RO\_DATA***
411. ***c9174047b48d vmlinux.lds.h: Replace RW\_DATA\_SECTION with RW\_DATA***
412. ***86fe639a1c16 riscv: enter WFI in default\_power\_off() if SBI does not shutdown***
413. ***0c3ac28931d5 riscv: separate MMIO functions into their own header file***
414. ***a4c3733d32a7 riscv: abstract out CSR names for supervisor vs machine mode***
415. ***38af57825313 riscv: use the generic ioremap code***
416. ***0fdc636cd95c riscv: Use PMD\_SIZE to replace PTE\_PARENT\_SIZE***
417. ***6b57ba8ed48a riscv: clean up the macro format in each header file***
418. ***8083c629dc31 RISC-V: Add multiple compression image format.***
419. ***3b03ac6bbd6e riscv: poison SBI calls for M-mode***
420. ***3320648ecc38 riscv: cleanup the default power off implementation***
421. ***8bf90f320d9a riscv: implement remote sfence.i using IPIs***
422. ***4f9bbcefa142 riscv: add support for MMIO access to the timer registers***
423. ***c12d3362a74b int128: move \_\_uint128\_t compiler test to Kconfig***
424. ***fcdc65375186 riscv: provide native clint access for M-mode***
425. ***accb9dbc4aff riscv: read the hart ID from mhartid on boot***
426. ***9e80635619b5 riscv: clear the instruction cache and all registers when booting***
427. ***6bd33e1ece52 riscv: add nommu support***
428. ***405fe7aa0dba riscv: provide a flat image loader***
429. ***de29fe308de7 riscv: Fix Kconfig indentation***
430. ***f2c5fd9e4c05 riscv: defconfigs: enable debugfs***
431. ***2e06b2717535 riscv: defconfigs: enable more debugging options***
432. ***2cc6c4a0da4a RISC-V: Add address map dumper***
433. ***29ff64929e6c sched/rt, riscv: Use CONFIG\_PREEMPTION***
434. ***0e72a2f9c1a3 riscv: Fix build dependency for loader***
435. ***bc3e8f5d42d5 riscv: only select serial sifive if TTY is enabled***
436. ***1f059dfdf5d1 mm/vmalloc: Add empty <asm/vmalloc.h> headers and use them from <linux/vmalloc.h>***
437. ***96bc4432f5ad bpf, riscv: Limit to 33 tail calls***
438. ***f1003b787c00 riscv, bpf: Fix broken BPF tail calls***
439. ***7d1ef13fea2b riscv, bpf: Add support for far branching***
440. ***29d92edd9ee8 riscv, bpf: Add support for far branching when emitting tail call***
441. ***33203c02f2f8 riscv, bpf: Add support for far jumps and exits***
442. ***fe8322b866d5 riscv, bpf: Optimize BPF tail calls***
443. ***7f3631e88ee6 riscv, bpf: Provide RISC-V specific JIT image alloc/free***
444. ***e368b64f8b0c riscv, bpf: Optimize calls***
445. ***eb9928bed003 riscv, bpf: Add missing uapi header for BPF\_PROG\_TYPE\_PERF\_EVENT programs***
446. ***34bfc10a6e7e riscv, perf: Add arch specific perf\_arch\_bpf\_user\_pt\_regs***
447. ***1d5c17e47028 RISC-V: Typo fixes in image header and documentation.***
448. ***d411cf02ed02 riscv: fix scratch register clearing in M-mode.***
449. ***01f52e16b868 riscv: define vmemmap before pfn\_to\_page calls***
450. ***9209fb51896f riscv: move sifive\_l2\_cache.c to drivers/soc***
451. ***4d47ce158efb riscv: fix compile failure with EXPORT\_SYMBOL() & !MMU***
452. ***556f47ac6083 riscv: reject invalid syscalls below -1***
453. ***1833e327a5ea riscv: export flush\_icache\_all to modules***
454. ***ac51e005fe14 riscv: mm: use \_\_pa\_symbol for kernel symbols***
455. ***0da310e82d3a riscv: gcov: enable gcov for RISC-V***
456. ***1d8f65798240 riscv: ftrace: correct the condition logic in function graph tracer***
457. ***2f3035da4019 riscv: prefix IRQ\_ macro names with an RV\_ namespace***
458. ***20bda4ed62f5 riscv: Implement copy\_thread\_tls***
459. ***dc6fcba72f04 riscv: Fixup obvious bug for fp-regs reset***
460. ***2680e04c1874 arch/riscv/setup: Drop dummy\_con initialization***
461. ***20d2292754e7 riscv: make sure the cores stay looping in .Lsecondary\_park***
462. ***95f4d9cced96 riscv: delete temporary files***
463. ***fc585d4a5cf6 riscv: Less inefficient gcc tishift helpers (and export their symbols)***
464. ***8ad8b72721d0 riscv: Add KASAN support***
465. ***fc76324fa27f riscv: keep 32-bit kernel to 32-bit phys\_addr\_t***
466. ***6435f773d81f riscv: mm: add support for CONFIG\_DEBUG\_VIRTUAL***
467. ***af6513ead046 riscv: mm: add p?d\_leaf() definitions***
468. ***c68a9032299e riscv: set pmp configuration if kernel is running in M-mode***
469. ***6a1ce99dc4bd RISC-V: Don't enable all interrupts in trap\_init()***
470. ***e7167043ee50 riscv: Fix gitignore***
471. ***a0a31fd84f8f riscv: allocate a complete page size for each page table***
472. ***8458ca147c20 riscv: adjust the indent***
473. ***0cff8bff7af8 riscv: avoid the PIC offset of static percpu data in module beyond 2G limits***
474. ***aad15bc85c18 riscv: Change code model of module to medany to improve data accessing***
475. ***ab70a73aa45b riscv: Use flush\_icache\_mm for flush\_icache\_user\_range***
476. ***2fab7a15604c riscv: Delete CONFIG\_SYSFS\_SYSCALL from defconfigs***
477. ***aff7783392e0 riscv: force hart\_lottery to put in .sdata section***
478. ***064223b947a8 RISC-V: Stop putting .sbss in .sdata***
479. ***52e7c52d2ded RISC-V: Stop relying on GCC's register allocator's hueristics***
480. ***fdff9911f266 RISC-V: Inline the assembly register save/restore macros***
481. ***abc71bf0a703 RISC-V: Stop using LOCAL for the uaccess fixups***
482. ***aa2734202acc riscv: Force flat memory model with no-mmu***
483. ***a160eed4b783 riscv: Fix range looking for kernel image memblock***
484. ***ca6cb5447cec riscv, bpf: Factor common RISC-V JIT code***
485. ***5f316b65e99f riscv, bpf: Add RV32G eBPF JIT***
486. ***759bdc168181 RISC-V: Add kconfig option for QEMU virt machine***
487. ***a4485398b6b8 RISC-V: Enable QEMU virt machine support in defconfigs***
488. ***81e2d3c52c0e RISC-V: Select SYSCON Reboot and Poweroff for QEMU virt machine***
489. ***d2047aba2e68 RISC-V: Select Goldfish RTC driver for QEMU virt machine***
490. ***3133287b53ee riscv: Use p\*d\_leaf macros to define p\*d\_huge***
491. ***af33d2433b03 riscv: fix seccomp reject syscall code path***
492. ***9f40b6e77d2f RISC-V: Move all address space definition macros to one place***
493. ***ccbe80bad571 irqchip/sifive-plic: Enable/Disable external interrupts upon cpu online/offline***
494. ***adccfb1a805e riscv: uaccess should be used in nommu mode***
495. ***3384b043ea15 riscv: fix the IPI missing issue in nommu mode***
496. ***d198b34f3855 .gitignore: add SPDX License Identifier***
497. ***d3ab332a5021 riscv: add ARCH\_HAS\_SET\_MEMORY support***
498. ***395a21ff859c riscv: add ARCH\_HAS\_SET\_DIRECT\_MAP support***
499. ***5fde3db5eb02 riscv: add ARCH\_SUPPORTS\_DEBUG\_PAGEALLOC support***
500. ***bd3d914d16aa riscv: move exception table immediately after RO\_DATA***
501. ***00cb41d5ad31 riscv: add alignment for text, rodata and data sections***
502. ***d27c3c90817e riscv: add STRICT\_KERNEL\_RWX support***
503. ***b42d763a2d41 riscv: add macro to get instruction length***
504. ***043cb41a85de riscv: introduce interfaces to patch kernel code***
505. ***8fdddb2eae73 riscv: patch code by fixmap mapping***
506. ***59c4da8640cc riscv: Add support to dump the kernel page tables***
507. ***88d110382555 riscv: Use macro definition instead of magic number***
508. ***2191b4f298fa RISC-V: Move all address space definition macros to one place***
509. ***a08971e9488d futex: arch\_futex\_atomic\_op\_inuser() calling conventions change***
510. ***8446923ae4d7 RISC-V: Mark existing SBI as 0.1 SBI.***
511. ***b9dcd9e41587 RISC-V: Add basic support for SBI v0.2***
512. ***ecbacc2a3efd RISC-V: Add SBI v0.2 extension definitions***
513. ***1ef46c231df4 RISC-V: Implement new SBI v0.2 extensions***
514. ***e011995e826f RISC-V: Move relocate and few other functions out of \_\_init***
515. ***2875fe056156 RISC-V: Add cpu\_ops and modify default booting method***
516. ***f90b43ce176c RISC-V: Export SBI error to linux error mapping function***
517. ***db5a79460315 RISC-V: Add SBI HSM extension definitions***
518. ***cfafe2601374 RISC-V: Add supported for ordered booting method using HSM***
519. ***f1e58583b9c7 RISC-V: Support cpu hotplug***
520. ***4ef873226ceb mm: introduce fault\_signal\_pending()***
521. ***dde160724832 mm: introduce FAULT\_FLAG\_DEFAULT***
522. ***4064b9827063 mm: allow VM\_FAULT\_RETRY for multiple times***
523. ***93bbb2555b65 riscv, bpf: Remove BPF JIT for nommu builds***
524. ***956d705dd279 riscv: Unaligned load/store handling for M\_MODE***
525. ***335b139057ef riscv: Add SOC early init support***
526. ***c48c4a4c7ead riscv: Add Kendryte K210 SoC support***
527. ***5ba568f57f0a riscv: Add Kendryte K210 device tree***
528. ***aa10eb6bb8a9 riscv: Kendryte K210 default config***
529. ***37809df4b1c8 riscv: create a loader.bin boot image for Kendryte SoC***
530. ***489553dd13a8 riscv, bpf: Fix offset range checking for auipc+jalr on RV64***
531. ***c62da0c35d58 mm/vma: define a default value for VM\_DATA\_DEFAULT\_FLAGS***
532. ***af2bdf828f79 RISC-V: stacktrace: Declare sp\_in\_global outside ifdef***
533. ***3c1918c8f541 riscv: fix vdso build with lld***
534. ***72df61d9d66e riscv: sbi: Correct sbi\_shutdown() and sbi\_clear\_ipi() export***
535. ***7d0ce3b2b483 riscv: sbi: Fix undefined reference to sbi\_shutdown***
536. ***62d0fd591db1 arch: split MODULE\_ARCH\_VERMAGIC definitions out to <asm/vermagic.h>***
537. ***a5fe13c7b494 riscv: select ARCH\_HAS\_STRICT\_KERNEL\_RWX only if MMU***
538. ***745abfaa9eaf bpf, riscv: Fix tail call count off by one in RV32 BPF JIT***
539. ***91f658587a96 bpf, riscv: Fix stack layout of JITed code on RV32***
540. ***7391efa48d88 RISC-V: Export riscv\_cpuid\_to\_hartid\_mask() API***
541. ***6bcff51539cc RISC-V: Add bitmap reprensenting ISA features common across CPUs***
542. ***a2da5b181f88 RISC-V: Remove N-extension related defines***
543. ***c749bb2d5548 riscv: set max\_pfn to the PFN of the last page***
544. ***0a9f2a6161dc riscv: add Linux note to vdso***
545. ***d6d5161280b3 riscv: force \_\_cpu\_up\_ variables to put in data section***
546. ***73cb8e2a5863 RISC-V: Remove unused code from STRICT\_KERNEL\_RWX***
547. ***0224b2acea0f bpf, riscv: Enable missing verifier\_zext optimizations on RV64***
548. ***21a099abb765 bpf, riscv: Optimize FROM\_LE using verifier\_zext on RV64***
549. ***ca349a6a104e bpf, riscv: Optimize BPF\_JMP BPF\_K when imm == 0 on RV64***
550. ***073ca6a0369e bpf, riscv: Optimize BPF\_JSET BPF\_K using andi on RV64***
551. ***e7b146a8bfba riscv: perf\_event: Make some funciton static***
552. ***48084c3595cb riscv: perf: RISCV\_BASE\_PMU should be independent***
553. ***ab7fbad0c7d7 riscv: Fix unmet direct dependencies built based on SOC\_VIRT***
554. ***0502bee37cde riscv: stacktrace: Fix undefined reference to `walk\_stackframe'***
555. ***fa8174aa225f riscv: Add pgprot\_writecombine/device and PAGE\_SHARED defination if NOMMU***
556. ***21e2414083e2 riscv: Disable ARCH\_HAS\_DEBUG\_VIRTUAL if NOMMU***
557. ***69868418e148 riscv: Make SYS\_SUPPORTS\_HUGETLBFS depends on MMU***
558. ***9a6630aef933 riscv: pgtable: Fix \_\_kernel\_map\_pages build error if NOMMU***
559. ***ed1ed4c0da54 riscv: mmiowb: Fix implicit declaration of function 'smp\_processor\_id'***
560. ***2d2682512f0f riscv: Allow device trees to be built into the kernel***
561. ***8bb661742776 riscv: K210: Add a built-in device tree***
562. ***045c654220e5 riscv: K210: Update defconfig***
563. ***eb077c9c387f RISC-V: Skip setting up PMPs on traps***
564. ***fe89bd2be866 riscv: Add KGDB support***
565. ***d96575709cc7 riscv: Use the XML target descriptions to report 3 system registers***
566. ***edde5584c7ab riscv: Add SW single-step support for KDB***
567. ***b80b3d582ebd riscv: Remove the 'riscv\_' prefix of function name***
568. ***5303df244cbf riscv: Use NOKPROBE\_SYMBOL() instead of \_\_krpobes annotation***
569. ***0ff7c3b33127 riscv: Use text\_mutex instead of patch\_lock***
570. ***087958a17658 riscv: cacheinfo: Implement cache\_get\_priv\_group with a generic ops structure***
571. ***8fa3cdff05f0 riscv: Fix print\_vm\_layout build error if NOMMU***
572. ***8356c379cfba RISC-V: gp\_in\_global needs register keyword***
573. ***99395ee3f7b4 mm: ptdump: expand type of 'val' in note\_page()***
574. ***c3f896dcf1e4 mm: switch the test\_vmalloc module to use \_\_vmalloc\_node***
575. ***3f08a302f533 mm: remove CONFIG\_HAVE\_MEMBLOCK\_NODE\_MAP option***
576. ***9691a071aa26 mm: use free\_area\_init() instead of free\_area\_init\_nodes()***
577. ***ae94da898133 hugetlbfs: add arch\_hugetlb\_valid\_size***
578. ***359f25443a8d hugetlbfs: move hugepagesz= parsing to arch independent code***
579. ***38237830882b hugetlbfs: remove hugetlb\_add\_hstate() warning for existing hstate***
580. ***b0eae98c66fe mm/hugetlb: define a generic fallback for is\_hugepage\_only\_range()***
581. ***5be993432821 mm/hugetlb: define a generic fallback for arch\_clear\_hugepage\_flags()***
582. ***b422d28b2177 riscv: support DEBUG\_WX***
583. ***885f7f8e3046 mm: rename flush\_icache\_user\_range to flush\_icache\_user\_page***
584. ***2062a4e8ae9f kallsyms/printk: add loglvl to print\_ip\_sym()***
585. ***0b3d43657489 riscv: add show\_stack\_loglvl()***
586. ***9cb8f069deee kernel: rename show\_stack\_loglvl() => show\_stack()***
587. ***974b9b2c68f3 mm: consolidate pte\_index() and pte\_offset\_\*() definitions***
588. ***d8ed45c5dcd4 mmap locking API: use coccinelle to convert mmap\_sem rwsem call sites***
589. ***89154dd5313f mmap locking API: convert mmap\_sem call sites missed by coccinelle***
590. ***3e4e28c5a8f0 mmap locking API: convert mmap\_sem API comments***
591. ***c1e8d7c6a7a6 mmap locking API: convert mmap\_sem comments***
592. ***e8c7ef7d5819 RISC-V: Sort select statements alphanumerically***
593. ***5cf998ba8c7b RISC-V: self-contained IPI handling routine***
594. ***6b7ce8927b5a irqchip: RISC-V per-HART local interrupt controller driver***
595. ***033a65de7ece clocksource/drivers/timer-riscv: Use per-CPU timer interrupt***
596. ***24dc17005ca1 RISC-V: Remove do\_IRQ() function***
597. ***e71ee06e3ca3 RISC-V: Force select RISCV\_INTC for CONFIG\_RISCV***
598. ***4e0f9e3a6104 RISC-V: Don't mark init section as non-executable***
599. ***05589dde649c riscv: fix build warning of missing prototypes***
600. ***ad5d1122b82f riscv: use vDSO common flow to reduce the latency of the time-related functions***
601. ***01f76386b0ac riscv: set the permission of vdso\_data to read-only***
602. ***6c58f25e6938 riscv/atomic: Fix sign extension for RV64I***
603. ***fe557319aa06 maccess: rename probe\_kernel\_{read,write} to copy\_{from,to}\_kernel\_nofault***
604. ***25f12ae45fc1 maccess: rename probe\_kernel\_address to get\_kernel\_nofault***
605. ***e0d17c842c0f RISC-V: Don't allow write+exec only page mapping request in mmap***
606. ***0e2c09011d4d RISC-V: Acquire mmap lock before invoking walk\_page\_range***
607. ***a0fc3b32893b riscv: Add -fPIC option to CFLAGS\_vgettimeofday.o***
608. ***e93b327dbf3d riscv: Add extern declarations for vDSO time-related functions***
609. ***e05d57dcb8c7 riscv: Fixup \_\_vdso\_gettimeofday broke dynamic ftrace***
610. ***234e9d7a6200 riscv: Select ARCH\_SUPPORTS\_ATOMIC\_RMW by default***
611. ***a2693fe254e7 RISC-V: Use a local variable instead of smp\_processor\_id()***
612. ***140c8180eb7c arch: remove HAVE\_COPY\_THREAD\_TLS***
613. ***714acdbd1c94 arch: rename copy\_thread\_tls() back to copy\_thread()***
614. ***526fbaed33e8 riscv: Register System RAM as iomem resources***
615. ***fc0c769ffd92 riscv: enable the Kconfig prompt of STRICT\_KERNEL\_RWX***
616. ***f7fc752815f8 riscv: Fix "no previous prototype" compile warning in kgdb.c file***
617. ***def0aa218e6d kgdb: Move the extern declaration kgdb\_has\_hit\_break() to generic kgdb.h***
618. ***70ee5731a40b riscv: Avoid kgdb.h including gdb\_xml.h to solve unused-const-variable warning***
619. ***0cac21b02ba5 riscv: use 16KB kernel stack on 64-bit***
620. ***38b7c2a3ffb1 RISC-V: Upgrade smp\_mb\_\_after\_spinlock() to iorw,iorw***
621. ***4cb699d0447b riscv: kasan: use local\_tlb\_flush\_all() to avoid uninitialized \_\_sbi\_rfence***
622. ***002dff36acfb asm/rwonce: Don't pull <asm/barrier.h> into 'asm-generic/rwonce.h'***
623. ***bfabff3cb0fe bpf, riscv: Modify JIT ctx to support compressed instructions***
624. ***804ec72c68c8 bpf, riscv: Add encodings for compressed instructions***
625. ***18a4d8c97b84 bpf, riscv: Use compressed instructions in the rv64 JIT***
626. ***d0d8aae64566 RISC-V: Set maximum number of mapped pages correctly***
627. ***4400231c8acc RISC-V: Do not rely on initrd\_start/end computed during early dt parsing***
628. ***fa5a19835905 riscv: Parse all memory blocks to remove unusable memory***
629. ***2cb6cd495d17 riscv: switch to ->regset\_get()***
630. ***7ca8cf5347f7 locking/atomic: Move ATOMIC\_INIT into linux/types.h***
631. ***6184358da000 riscv: Fixup static\_obj() fail***
632. ***c15959921f8d riscv: Fixup lockdep\_assert\_held with wrong param cpu\_running***
633. ***3c4697982982 riscv: Enable LOCKDEP\_SUPPORT & fixup TRACE\_IRQFLAGS\_SUPPORT***
634. ***298447928bb1 riscv: Support irq\_work via self IPIs***
635. ***ed48b297fe21 riscv: Enable context tracking***
636. ***20d38f7c45a4 riscv: Allow building with kcov coverage***
637. ***cbb3d91d3bcf riscv: Add kmemleak support***
638. ***08b5985e7be5 riscv: Fix typo in asm/hwcap.h uapi header***
639. ***f2c9699f6555 riscv: Add STACKPROTECTOR supported***
640. ***8e0c02f27253 Replace HTTP links with HTTPS ones: RISC-V***
641. ***11a54f422b0d riscv: Support R\_RISCV\_ADD64 and R\_RISCV\_SUB64 relocs***
642. ***ebc00dde8a97 riscv: Add jump-label implementation***
643. ***3e7b669c6c53 riscv: Cleanup unnecessary define in asm-offset.c***
644. ***89b03cc1dff0 riscv: Use generic pgprot\_\* macros from <linux/pgtable.h>***
645. ***925ac7b6636b riscv: Select ARCH\_HAS\_DEBUG\_VM\_PGTABLE***
646. ***79b1feba5455 RISC-V: Setup exception vector early***
647. ***e3ef4d69456e riscv: Fix build warning for mm/init***
648. ***3843aca0521d riscv: fix build warning of mm/pageattr***
649. ***635093e306a3 RISC-V: Fix build warning for smpboot.c***
650. ***40284a072c42 riscv: disable stack-protector for vDSO***
651. ***4c5a116ada95 vdso/treewide: Add vdso\_data pointer argument to \_\_arch\_get\_hw\_counter()***
652. ***1d9cfee7535c mm/sparsemem: enable vmem\_altmap support in vmemmap\_populate\_basepages()***
653. ***c89ab04febf9 mm/sparse: cleanup the code surrounding memory\_present()***
654. ***428e2976a5bf uaccess: remove segment\_eq***
655. ***bce617edecad mm: do page fault accounting in handle\_mm\_fault***
656. ***5ac365a45890 mm/riscv: use general page fault accounting***
657. ***76d4467a97bd riscv: Setup exception vector for nommu platform***
658. ***cc7f3f72dc2a RISC-V: Add mechanism to provide custom IPI operations***
659. ***2bc3fc877aa9 RISC-V: Remove CLINT related code from timer and arch***
660. ***df561f6688fe treewide: Use fallthrough pseudo-keyword***
661. ***c604abc3f6e3 vmlinux.lds.h: Split ELF\_DETAILS from STABS\_DEBUG***
662. ***5e6e9852d6f7 uaccess: add infrastructure for kernel builds with set\_fs()***
663. ***66d18dbda846 RISC-V: Take text\_mutex in ftrace\_init\_nop()***
664. ***4363287178a8 riscv/mm: Simplify retry logic in do\_page\_fault()***
665. ***cac4d1dc85be riscv/mm/fault: Move no context handling to no\_context()***
666. ***a51271d99cdd riscv/mm/fault: Move bad area handling to bad\_area()***
667. ***ac416a724f11 riscv/mm/fault: Move vmalloc fault handling to vmalloc\_fault()***
668. ***bda281d5bfb7 riscv/mm/fault: Simplify fault error handling***
669. ***6c11ffbfd849 riscv/mm/fault: Move fault error handling to mm\_fault\_error()***
670. ***7a75f3d47a0b riscv/mm/fault: Simplify mm\_fault\_error()***
671. ***6747430197ed riscv/mm/fault: Move FAULT\_FLAG\_WRITE handling in do\_page\_fault()***
672. ***afb8c6fee8ce riscv/mm/fault: Move access error check to function***
673. ***baf7cbd94b56 riscv: Set more data to cacheinfo***
674. ***b5fca7c55f9f riscv: Define AT\_VECTOR\_SIZE\_ARCH for ARCH\_DLINFO***
675. ***38f5bd23deae riscv: Add cache information in AUX vector***
676. ***2baa6d9506f2 riscv/mm/fault: Fix inline placement in vmalloc\_fault() declaration***
677. ***a960c1323749 riscv/mm/fault: Set FAULT\_FLAG\_INSTRUCTION flag in do\_page\_fault()***
678. ***21190b74bcf3 riscv: Add sfence.vma after early page table changes***
679. ***f025d9d9934b riscv: Fix Kendryte K210 device tree***
680. ***d5be89a8d118 RISC-V: Resurrect the MMIO timer implementation for M-mode systems***
681. ***aa9887608e77 RISC-V: Check clint\_time\_val before use***
682. ***8f3a2b4a96dc RISC-V: Move DT mapping outof fixmap***
683. ***6262f661ff5d RISC-V: Add early ioremap support***
684. ***e8dcb61f2ade RISC-V: Implement late mapping page table allocation functions***
685. ***cb7d2dd5612a RISC-V: Add PE/COFF header for EFI stub***
686. ***d7071743db31 RISC-V: Add EFI stub support.***
687. ***b91540d52a08 RISC-V: Add EFI runtime services***
688. ***de22d2107ced RISC-V: Add page table dump support for uefi***
689. ***11129e8ed4d9 riscv: use memcpy based uaccess for nommu again***
690. ***f289a34811d8 riscv: refactor \_\_get\_user and \_\_put\_user***
691. ***d464118cdc41 riscv: implement \_\_get\_kernel\_nofault and \_\_put\_user\_nofault***
692. ***e8d444d3e98c riscv: remove address space overrides using set\_fs()***
693. ***a78c6f5956a9 RISC-V: Make sure memblock reserves the memory containing DT***
694. ***84814460eef9 riscv: Fixup bootup failure with HARDENED\_USERCOPY***
695. ***c8e470184a06 riscv: drop unneeded node initialization***
696. ***b10d6bca8720 arch, drivers: replace for\_each\_membock() with for\_each\_mem\_range()***
697. ***cc6de1680538 memblock: use separate iterators for memory and reserved regions***
698. ***3c532798ec96 tracehook: clear TIF\_NOTIFY\_RESUME in tracehook\_notify\_resume()***
699. ***33def8498fdd treewide: Convert macro and uses of \_\_section(foo) to \_\_section("foo")***
700. ***0774a6ed294b timekeeping: default GENERIC\_CLOCKEVENTS to enabled***
701. ***9d750c75bd2c risc-v: kernel: ftrace: Fixes improper SPDX comment style***
702. ***1bd14a66ee52 RISC-V: Remove any memblock representing unusable memory area***
703. ***79605f139426 riscv: Set text\_offset correctly for M-Mode***
704. ***bcacf5f6f239 riscv: fix pfn\_to\_virt err in do\_page\_fault().***
705. ***635e3f3e47f2 riscv: uaccess: fix \_\_put\_kernel\_nofault()***
706. ***1074dd44c5ba RISC-V: Use non-PGD mappings for early DTB access***
707. ***c2c81bb2f691 RISC-V: Fix the VDSO symbol generaton for binutils-2.35+***
708. ***76a4efa80900 perf/arch: Remove perf\_sample\_data::regs\_user\_copy***
709. ***00ab027a3b82 RISC-V: Add kernel image sections to the resource tree***
710. ***c18d7c17c005 riscv: Fix compressed Image formats build***
711. ***2c42bcbb95ec riscv: Clean up boot dir***
712. ***ae386e9d809c riscv: Ignore Image.\* and loader.bin***
713. ***cef397038167 arch: pgtable: define MAX\_POSSIBLE\_PHYSMEM\_BITS where needed***
714. ***673a11a7e415 riscv: Enable seccomp architecture tracking***
715. ***da815582cf45 riscv: Enable CMA support***
716. ***31564b8b6dba riscv: Add HAVE\_IRQ\_TIME\_ACCOUNTING***
717. ***99c168fccbfe riscv: Cleanup stacktrace***
718. ***9dd97064e21f riscv: Make stack walk callback consistent with generic code***
719. ***58c644ba512c sched/idle: Fix arch\_cpu\_idle() vs tracing***
720. ***e553fdc8105a riscv: Explicitly specify the build id style in vDSO Makefile again***
721. ***6134b110f971 RISC-V: Add missing jump label initialization***
722. ***30aca1bacb39 RISC-V: fix barrier() use in <vdso/processor.h>***
723. ***5cb0080f1bfd riscv: Enable ARCH\_STACKWALK***
724. ***62149f3564c5 RISC-V: Initialize SBI early***
725. ***b6566dc1acca RISC-V: Align the .init.text section***
726. ***19a00869028f RISC-V: Protect all kernel sections including init early***
727. ***b5b11a8ac4b5 RISC-V: Move dynamic relocation section under \_\_init***
728. ***54649911f31b efi: stub: get rid of efi\_get\_max\_fdt\_addr()***
729. ***04091d6c0535 riscv: provide memmove implementation***
730. ***ccbbfd1cbf36 RISC-V: Define get\_cycles64() regardless of M-mode***
731. ***772e1b7c4267 riscv: kernel: Drop unused clean rule***
732. ***3ae9c3cde51a riscv: Fixed kernel test robot warning***
733. ***78ed473c7619 RISC-V: Use the new generic devmem\_is\_allowed()***
734. ***7d95a88f9254 Add and use a generic version of devmem\_is\_allowed()***
735. ***24a31b81e383 riscv: add support for TIF\_NOTIFY\_SIGNAL***
736. ***5d6ad668f316 arch, mm: restore dependency of \_\_kernel\_map\_pages() on DEBUG\_PAGEALLOC***
737. ***32a0de886eb3 arch, mm: make kernel\_page\_present() always available***
738. ***28108fc8a056 clk: sifive: Use common name for prci configuration***
739. ***de043da0b9e7 RISC-V: Fix usage of memblock\_enforce\_memory\_limit***
740. ***87dbc209ea04 local64.h: make <asm/local64.h> mandatory***
741. ***641e8cd2cbf0 riscv: Cleanup sbi function stubs when RISCV\_SBI disabled***
742. ***21733cb51847 riscv/mm: Introduce a die\_kernel\_fault() helper function***
743. ***21855cac82d3 riscv/mm: Prevent kernel module to access user memory without uaccess routines***
744. ***cf7b2ae4d704 riscv: return -ENOSYS for syscall -1***
745. ***11f4c2e940e2 riscv: Fix kernel time\_init()***
746. ***643437b996ba riscv: Enable interrupts during syscalls with M-Mode***
747. ***d5805af9fe9f riscv: Fix builtin DTB handling***
748. ***0ea02c737752 riscv: Drop a duplicated PAGE\_KERNEL\_EXEC***
749. ***7cd1af107a92 riscv: Trace irq on only interrupt is enabled***
750. ***80709af7325d riscv: cacheinfo: Fix using smp\_processor\_id() in preemptible***
751. ***0aa2ec8a475f riscv: Fixup CONFIG\_GENERIC\_TIME\_VSYSCALL***
752. ***c25a053e1577 riscv: Fix KASAN memory mapping.***
753. ***0983834a8393 riscv: defconfig: enable gpio support for HiFive Unleashed***
754. ***08734e0581a5 riscv: Use vendor name for K210 SoC support***
755. ***93c2ce1ee77e riscv: Fix Canaan Kendryte K210 device tree***
756. ***5a2308da9f60 riscv: Add Canaan Kendryte K210 reset controller***
757. ***cbd34f4bb37d riscv: Separate memory init from paging init***
758. ***3e5b0bdb2a4d riscv: Add support pte\_protnone and pmd\_protnone if CONFIG\_NUMA\_BALANCING***
759. ***4f0e8eef772e riscv: Add numa support for riscv64 platform***
760. ***46ad48e8a28d riscv: Add machine name to kernel boot log and stack dump output***
761. ***dcdc7a53a890 RISC-V: Implement ptrace regs and stack API***
762. ***edfcf91fe4f8 riscv: Fixup compile error BUILD\_BUG\_ON failed***
763. ***67d945778099 riscv: Fixup wrong ftrace remove cflag***
764. ***5ad84adf5456 riscv: Fixup patch\_text panic in ftrace***
765. ***afc76b8b8011 riscv: Using PATCHABLE\_FUNCTION\_ENTRY instead of MCOUNT***
766. ***c22b0bcb1dd0 riscv: Add kprobes supported***
767. ***829adda597fe riscv: Add KPROBES\_ON\_FTRACE supported***
768. ***74784081aac8 riscv: Add uprobes supported***
769. ***ee55ff803b38 riscv: Add support for function error injection***
770. ***fea2fed201ee riscv: Enable per-task stack canaries***
771. ***091b9450858e riscv: Add dump stack in show\_regs***
772. ***da401e894532 riscv: Improve \_\_show\_regs***
773. ***f766f77a74f5 riscv/stacktrace: Fix stack output without ra on the stack top***
774. ***dec822771b01 riscv: stacktrace: Move register keyword to beginning of declaration***
775. ***797f0375dd2e RISC-V: Do not allocate memblock while iterating reserved memblocks***
776. ***abb8e86b2696 RISC-V: Set current memblock limit***
777. ***e557793799c5 RISC-V: Fix maximum allowed phsyical memory for RV32***
778. ***336e8eb2a3cf riscv: Fixup pfn\_valid error with wrong max\_mapnr***
779. ***2ab543823322 riscv: virt\_addr\_valid must check the address belongs to linear mapping***
780. ***f105ea9890f4 RISC-V: Fix .init section permission update***
781. ***eefb5f3ab2e8 riscv: Align on L1\_CACHE\_BYTES when STRICT\_KERNEL\_RWX***
782. ***de5f4b8f634b RISC-V: Define MAXPHYSMEM\_1GB only for RV32***
783. ***f105aa940e78 riscv: add BUILTIN\_DTB support for MMU-enabled targets***
784. ***aec33b54af55 riscv: Covert to reserve\_initrd\_mem()***
785. ***e178d670f251 riscv/kasan: add KASAN\_VMALLOC support***
786. ***5da9cbd2b200 arch/riscv:fix typo in a comment in arch/riscv/kernel/image-vars.h***
787. ***d4c34d09ab03 pinctrl: Add RISC-V Canaan Kendryte K210 FPIOA driver***
788. ***5dd671333171 RISC-V: probes: Treat the instruction stream as host-endian***
789. ***3449831d92fe RISC-V: remove unneeded semicolon***
790. ***65d4b9c53017 RISC-V: Implement ASID allocator***
791. ***4727dc20e042 arch: setup PF\_IO\_WORKER threads like PF\_KTHREAD***
792. ***4bb875632ad0 RISC-V: Add a non-void return for sbi v02 functions***
793. ***67d96729a9e7 riscv: Update Canaan Kendryte K210 device tree***
794. ***97c279bcf813 riscv: Add SiPeed MAIX BiT board device tree***
795. ***a40f920964c4 riscv: Add SiPeed MAIX DOCK board device tree***
796. ***8194f08bda18 riscv: Add SiPeed MAIX GO board device tree***
797. ***8f5b0e79f3e5 riscv: Add SiPeed MAIXDUINO board device tree***
798. ***62363a8e2f56 riscv: Add Kendryte KD233 board device tree***
799. ***aec3a94d951f riscv: Update Canaan Kendryte K210 defconfig***
800. ***7e09fd3994c5 riscv: Add Canaan Kendryte K210 SD card defconfig***
801. ***cc937cad14fb riscv: Remove unnecessary declaration***
802. ***f3d60f2a25e4 riscv: Disable KSAN\_SANITIZE for vDSO***
803. ***0f02de4481da riscv: Get rid of MAX\_EARLY\_MAPPING\_SIZE***
804. ***7899ed260c34 riscv: Improve kasan definitions***
805. ***9484e2aef45b riscv: Use KASAN\_SHADOW\_INIT define for kasan memory initialization***
806. ***d127c19c7bea riscv: Improve kasan population function***
807. ***d7fbcf40df86 riscv: Improve kasan population by using hugepages when possible***
808. ***f01e631cccab RISC-V: Make NUMA depend on SMP***
809. ***b122c7a32593 RISC-V: Enable CPU Hotplug in defconfigs***
810. ***dd2d082b5760 riscv: Cleanup setup\_bootmem()***
811. ***f6e5aedf470b riscv: Add support for memtest***
812. ***9530141455c9 riscv: Add ARCH\_HAS\_FORTIFY\_SOURCE***
813. ***6dd4879f59b0 RISC-V: correct enum sbi\_ext\_rfence\_fid***
814. ***030f1dfa8550 riscv: traps: Fix no prototype warnings***
815. ***004570c3796b riscv: irq: Fix no prototype warning***
816. ***56a6c37f6e39 riscv: sbi: Fix comment of \_\_sbi\_set\_timer\_v01***
817. ***e06f4ce1d4c6 riscv: ptrace: Fix no prototype warnings***
818. ***db2a8f9256e9 riscv: time: Fix no prototype for time\_init***
819. ***a6a58ecf98c3 riscv: syscall\_table: Reduce W=1 compilation warnings noise***
820. ***86b276c1dded riscv: process: Fix no prototype for show\_regs***
821. ***288f6775a089 riscv: ftrace: Use ftrace\_get\_regs helper***
822. ***0d7588ab9ef9 riscv: process: Fix no prototype for arch\_dup\_task\_struct***
823. ***6e9070dc2e84 riscv: fix bugon.cocci warnings***
824. ***2f100585d045 riscv: Enable generic clockevent broadcast***
825. ***bab1770a2ce0 ftrace: Fix spelling mistake "disabed" -> "disabled"***
826. ***fa59030bf855 riscv: Fix compilation error with Canaan SoC***
827. ***ce989f1472ae RISC-V: Fix out-of-bounds accesses in init\_resources()***
828. ***f3773dd031de riscv: Ensure page table writes are flushed when initializing KASAN vmalloc***
829. ***78947bdfd752 RISC-V: kasan: Declare kasan\_shallow\_populate() static***
830. ***a5406a7ff56e riscv: Correct SPARSEMEM configuration***
831. ***a0d8d552783b whack-a-mole: kill strlen\_user() (again)***
832. ***f35bb4b8d10a RISC-V: Don't print SBI version for all detected extensions***
833. ***2da073c19641 riscv: Cleanup KASAN\_VMALLOC support***
834. ***23c1075ae83a riscv: Drop const annotation for sp***
835. ***285a76bb2cf5 riscv: evaluate put\_user() arg before enabling user access***
836. ***ac8d0b901f00 riscv,entry: fix misaligned base for excp\_vect\_table***
837. ***9d8c7d92015e riscv: remove unneeded semicolon***
838. ***1adbc2941eee riscv: Make NUMA depend on MMU***
839. ***199fc6b8dee7 riscv: Fix spelling mistake "SPARSEMEM" to "SPARSMEM"***
840. ***2349a3b26e29 riscv: add do\_page\_fault and do\_trap\_break into the kprobes blacklist***
841. ***e31be8d343e6 riscv: kprobes/ftrace: Add recursion protection to the ftrace callback***
842. ***7ae11635ec90 riscv: keep interrupts disabled for BREAKPOINT exception***
843. ***09accc3a05f7 riscv: Disable data start offset in flat binaries***
844. ***183787c6fcc2 riscv: Add 3 SBI wrapper functions to get cpu manufacturer information***
845. ***6f4eea90465a riscv: Introduce alternative mechanism to apply errata solution***
846. ***1a0e5dbd3723 riscv: sifive: Add SiFive alternative ports***
847. ***800149a77c2c riscv: sifive: Apply errata "cip-453" patch***
848. ***bff3ff525460 riscv: sifive: Apply errata "cip-1200" patch***
849. ***7f3d349065d0 riscv: Use $(LD) instead of $(CC) to link vDSO***
850. ***7ce047715030 riscv: Workaround mcount name prior to clang-13***
851. ***adebc8817b5c riscv: Select HAVE\_DYNAMIC\_FTRACE when -fpatchable-function-entry is available***
852. ***2bfc6cd81bd1 riscv: Move kernel mapping outside of linear mapping***
853. ***0df68ce4c26a riscv: Prepare ptdump for vm layout dynamic addresses***
854. ***1987501b1130 riscv: add \_\_init section marker to some functions***
855. ***de31ea4a1181 riscv: Mark some global variables \_\_ro\_after\_init***
856. ***e6a302248cec riscv: Constify sys\_call\_table***
857. ***300f62c37d46 riscv: Constify sbi\_ipi\_ops***
858. ***cdd1b2bd358f riscv: kprobes: Implement alloc\_insn\_page()***
859. ***1d27d854425f riscv: bpf: Move bpf\_jit\_alloc\_exec() and bpf\_jit\_free\_exec() to core***
860. ***fc8504765ec5 riscv: bpf: Avoid breaking W^X***
861. ***5387054b986e riscv: module: Create module allocations without exec permissions***
862. ***a9451b8e1971 riscv: Set ARCH\_HAS\_STRICT\_MODULE\_RWX if MMU***
863. ***b1ebaa0e1318 riscv/kprobe: fix kernel panic when invoking sys\_read traced by kprobe***
864. ***e75e6bf47a47 riscv/mm: Use BUG\_ON instead of if condition followed by BUG.***
865. ***772d7891e8b3 riscv: vdso: fix and clean-up Makefile***
866. ***fba8a8674f68 RISC-V: Add kexec support***
867. ***ffe0e5261268 RISC-V: Improve init\_resources()***
868. ***e53d28180d4d RISC-V: Add kdump support***
869. ***5640975003d0 RISC-V: Add crash kernel support***
870. ***44c922572952 RISC-V: enable XIP***
871. ***99b3e3d41a03 RISC-V: Add Microchip PolarFire SoC kconfig option***
872. ***0fa6107eca41 RISC-V: Initial DTS for Microchip ICICLE board***
873. ***2951162094e6 RISC-V: Enable Microchip PolarFire ICICLE SoC***
874. ***1f9d03c5e999 mm: move mem\_init\_print\_info() into mm\_init()***
875. ***533b4f3a789d RISC-V: Fix error code returned by riscv\_hartid\_to\_cpuid()***
876. ***883fcb8ecaaf riscv: Fix 32b kernel build with CONFIG\_DEBUG\_VIRTUAL=y***
877. ***28252e08649f riscv: Remove 32b kernel mapping from page table dump***
878. ***f54c7b5898d3 RISC-V: Always define XIP\_FIXUP***
879. ***855f9a8e87fe mm: generalize SYS\_SUPPORTS\_HUGETLBFS (rename as ARCH\_SUPPORTS\_HUGETLBFS)***
880. ***8db6f937f4e7 riscv: Only extend kernel reservation if mapped read-only***
881. ***0e0d4992517f riscv: enable SiFive errata CIP-453 and CIP-1200 Kconfig only if CONFIG\_64BIT=y***
882. ***8d91b0973358 riscv: Consistify protect\_kernel\_linear\_mapping\_text\_rodata() use***
883. ***beaf5ae15a13 riscv: remove unused handle\_exception symbol***
884. ***f1a0a376ca0c sched/core: Initialize the idle task with preemption disabled***
885. ***f5397c3ee0a3 riscv: mm: add \_PAGE\_LEAF macro***
886. ***141682f5b9d6 riscv: mm: make pmd\_bad() check leaf condition***
887. ***c3b2d67046d2 riscv: mm: add param stride for \_\_sbi\_tlb\_flush\_range***
888. ***e88b333142e4 riscv: mm: add THP support on 64-bit***
889. ***eac2f3059e02 riscv: stacktrace: fix the riscv stacktrace when CONFIG\_FRAME\_POINTER enabled***
890. ***97a031082320 riscv: Select ARCH\_USE\_MEMTEST***
891. ***02ccdeed1817 riscv: kprobes: Fix build error when MMU=n***
892. ***bab0d47c0ebb riscv: kexec: Fix W=1 build warnings***
893. ***3332f4190674 riscv: mremap speedup - enable HAVE\_MOVE\_PUD and HAVE\_MOVE\_PMD***
894. ***8f3e136ff378 riscv: mm: Remove setup\_zero\_page()***
895. ***db756746807b riscv: enable generic PCI resource mapping***
896. ***f842f5ff6aaf riscv: Move setup\_bootmem into paging\_init***
897. ***50bae95e17c6 riscv: mm: Drop redundant \_sdata and \_edata declaration***
898. ***8237c5243a61 riscv: Optimize switch\_mm by passing "cpu" to flush\_icache\_deferred()***
899. ***37a7a2a10ec5 riscv: Turn has\_fpu into a static key if FPU=y***
900. ***9efbb3558310 locking/atomic: riscv: move to ARCH\_ATOMIC***
901. ***3c1885187bc1 locking/atomic: delete !ARCH\_ATOMIC remnants***
902. ***8c9f4940c27d riscv: kprobes: Remove redundant kprobe\_step\_ctx***
903. ***ec3a5cb61146 riscv: Use -mno-relax when using lld linker***
904. ***3df952ae2ac8 riscv: Add \_\_init section marker to some functions again***
905. ***010623568222 riscv: mm: init: Consolidate vars, functions***
906. ***7fa865f5640a riscv: TRANSPARENT\_HUGEPAGE: depends on MMU***
907. ***cba43c31f14b riscv: Use global mappings for kernel pages***
908. ***ec6aba3d2be1 kprobes: Remove kprobe::fault\_handler***
909. ***8a4102a0cf07 riscv: mm: Fix W+X mappings at boot***
910. ***b75db25c416b riscv: skip errata\_cip\_453.o if CONFIG\_ERRATA\_SIFIVE\_CIP\_453 is disabled***
911. ***da2d48808fbd RISC-V: Fix memblock\_free() usages in init\_resources()***
912. ***2e38eb04c95e kprobes: Do not increment probe miss count in the fault handler***
913. ***ff76e3d7c3c9 riscv: fix build error when CONFIG\_SMP is disabled***
914. ***5def4429aefe riscv: mm: Use better bitmap\_zalloc()***
915. ***efcec32fe84a riscv: Cleanup unused functions***
916. ***ae3d69bcc455 riscv: fix typo in init.c***
917. ***5e63215c2f64 riscv: xip: support runtime trap patching***
918. ***42e0e0b453bc riscv: code patching only works on !XIP\_KERNEL***
919. ***858cf860494f riscv: alternative: fix typo in macro name***
920. ***ce3aca0465e3 riscv: Only initialize swiotlb when necessary***
921. ***9b79878ced8f riscv: Remove CONFIG\_PHYS\_RAM\_BASE\_FIXED***
922. ***7094e6acaf7a riscv: Simplify xip and !xip kernel address conversion macros***
923. ***0ddd7eaffa64 riscv: Fix BUILTIN\_DTB for sifive and microchip soc***
924. ***5d2388dbf84a riscv32: Use medany C model for modules***
925. ***01f5315dd732 riscv: sifive: fix Kconfig errata warning***
926. ***c9811e379b21 riscv: Add mem kernel parameter support***
927. ***b03fbd4ff24c sched: Introduce task\_is\_running()***
928. ***314b781706e3 riscv: kasan: Fix MODULES\_VADDR evaluation due to local variables' name***
929. ***3a02764c372c riscv: Ensure BPF\_JIT\_REGION\_START aligned with PMD size***
930. ***a9ee6cf5c60e mm: replace CONFIG\_NEED\_MULTIPLE\_NODES with CONFIG\_NUMA***
931. ***63703f37aa09 mm: generalize ZONE\_[DMA|DMA32]***
932. ***70c7605c08c5 riscv: pass the mm\_struct to \_\_sbi\_tlb\_flush\_range***
933. ***3f1e782998cd riscv: add ASID-based tlbflushing methods***
934. ***47513f243b45 riscv: Enable KFENCE for riscv64***
935. ***c10bc260e7c0 riscv: Introduce set\_kernel\_memory helper***
936. ***e5c35fa04019 riscv: Map the kernel with correct permissions the first time***
937. ***fac7757e1fb0 mm: define default value for FIRST\_USER\_ADDRESS***
938. ***1c2f7d14d84f mm/thp: define default pmd\_pgtable()***
939. ***658e2c5125bb riscv: Introduce structure that group all variables regarding kernel mapping***
940. ***9eb4fcff2207 riscv: mm: fix build errors caused by mk\_pmd()***
941. ***70eee556b678 riscv: ptrace: add argn syntax***
942. ***31da94c25aea riscv: add VMAP\_STACK overflow detection***
943. ***ca6eaaa210de riscv: \_\_asm\_copy\_to-from\_user: Optimize unaligned memory access and pipeline stall***
944. ***7761e36bc722 riscv: Fix PTDUMP output now BPF region moved back to module region***
945. ***10cc32788391 riscv/Kconfig: make direct map manipulation options depend on MMU***
946. ***7bb7f2ac24a0 arch, mm: wire up memfd\_secret system call where relevant***
947. ***723a42f4f6b2 riscv: convert to setup\_initial\_init\_mm()***
948. ***9cf6fa245844 mm: rename pud\_page\_vaddr to pud\_pgtable and make it return pmd\_t \****
949. ***8633ef82f101 drivers/firmware: consolidate EFI framebuffer setup for all arches***
950. ***d0e4dae74470 riscv: Fix 32-bit RISC-V boot failure***
951. ***c79e89ecaa24 RISC-V: load initrd wherever it fits into memory***
952. ***b7d2be48cc08 riscv: kprobes: implement the auipc instruction***
953. ***67979e927dd0 riscv: kprobes: implement the branch instructions***
954. ***c09dc9e1cd3c riscv: Fix memory\_limit for 64-bit kernel***
955. ***c99127c45248 riscv: Make sure the linear mapping does not use the kernel mapping***
956. ***db6b84a368b4 riscv: Make sure the kernel mapping does not overlap with IS\_ERR\_VALUE***
957. ***76f5dfacfb42 riscv: stacktrace: pin the task's stack in get\_wchan***
958. ***6010d300f9f7 riscv: \_\_asm\_copy\_to-from\_user: Fix: overrun copy***
959. ***22b5f16ffeff riscv: \_\_asm\_copy\_to-from\_user: Fix: fail on RV32***
960. ***d4b3e0105e3c riscv: \_\_asm\_copy\_to-from\_user: Remove unnecessary size check***
961. ***ea196c548c0a riscv: \_\_asm\_copy\_to-from\_user: Fix: Typos in comments***
962. ***78d9d8005e45 riscv: stacktrace: Fix NULL pointer dereference***
963. ***f5e81d111750 bpf: Introduce BPF nospec instruction for mitigating Spectre v4***
964. ***13e47bebbe83 riscv: Implement thread\_struct whitelist for hardened usercopy***
965. ***a18b14d88866 riscv: Disable STACKPROTECTOR\_PER\_TASK if GCC\_PLUGIN\_RANDSTRUCT is enabled***
966. ***8165c6ae8e3a riscv: Allow forced irq threading***
967. ***bcf11b5e99b2 riscv: Enable idle generic idle loop***
968. ***ecd4916c7261 riscv: Enable GENERIC\_IRQ\_SHOW\_LEVEL***
969. ***6d7f91d914bc riscv: Get rid of CONFIG\_PHYS\_RAM\_BASE in kernel physical address conversion***
970. ***59a27e112213 riscv: Optimize kernel virtual address conversion macro***
971. ***0aba691a7443 riscv: Introduce va\_kernel\_pa\_offset for 32-bit kernel***
972. ***526f83df1d83 riscv: Get rid of map\_size parameter to create\_kernel\_page\_table***
973. ***6f3e5fd241c3 riscv: Use \_\_maybe\_unused instead of #ifdefs around variable declarations***
974. ***977765ce319b riscv: Simplify BUILTIN\_DTB device tree mapping handling***
975. ***fe45ffa4c505 riscv: Move early fdt mapping creation in its own function***
976. ***030d6dbf0c2e riscv: kexec: do not add '-mno-relax' flag if compiler doesn't support it***
977. ***fdf3a7a1e0a6 riscv: Fix comment regarding kernel mapping overlapping with IS\_ERR\_VALUE***
978. ***fb31f0a49933 riscv: fix the global name pfn\_base confliction error***
979. ***8ba1a8b77ba1 riscv: Support allocating gigantic hugepages using CMA***
980. ***4aae683f1327 tracing: Refactor TRACE\_IRQFLAGS\_SUPPORT in Kconfig***
981. ***aa3e1ba32e55 riscv: Fix a number of free'd resources in init\_resources()***
982. ***c4b2b7d150d2 block: remove CONFIG\_DEBUG\_BLOCK\_EXT\_DEVT***
983. ***2931ea847dcc riscv: Remove non-standard linux,elfcorehdr handling***
984. ***379eb01c2179 riscv: Ensure the value of FP registers in the core dump file is up to date***
985. ***7f85b04b08ca riscv: Keep the riscv Kconfig selects sorted***
986. ***8341dcfbd8dd riscv: Enable Undefined Behavior Sanitizer UBSAN***
987. ***fde9c59aebaf riscv: explicitly use symbol offsets for VDSO***
988. ***803930ee35fa riscv: use strscpy to replace strlcpy***
989. ***a290f510a178 RISC-V: Fix VDSO build for !MMU***
990. ***c24a19674258 riscv: add support for hugepage migration***
991. ***4b92d4add5f6 drivers: base: cacheinfo: Get rid of DEFINE\_SMP\_CALL\_CACHE\_FUNCTION()***
992. ***a7259df76702 memblock: make memblock\_find\_in\_range method private***
993. ***8350229ffceb riscv: only select GENERIC\_IOREMAP if MMU support is enabled***
994. ***8b097881b54c trap: cleanup trap\_init()***
995. ***3a87ff891290 riscv: defconfig: enable BLK\_DEV\_NVME***
996. ***efe1e08bca9a riscv: defconfig: enable NLS\_CODEPAGE\_437, NLS\_ISO8859\_1***
997. ***d5935537c825 riscv: Improve stack randomisation on RV64***
998. ***399c1ec8467c riscv: move the (z)install rules to arch/riscv/Makefile***
999. ***54fed35fd393 riscv: Enable BUILDTIME\_TABLE\_SORT***
1000. ***6f55ab36bef5 riscv: Move EXCEPTION\_TABLE to RO\_DATA segment***
1001. ***d20758951f8f riscv: remove Kconfig check for GCC version for ARCH\_RV64I***
1002. ***7962c2eddbfe arch: remove unused function syscall\_set\_arguments()***
1003. ***8aa0fb0fbb82 riscv: rely on core code to keep thread\_info::cpu updated***
1004. ***9c89bb8e3272 kprobes: treewide: Cleanup the error messages for kprobes***
1005. ***96fed8ac2bb6 kprobes: treewide: Remove trampoline\_address from kretprobe\_trampoline\_handler()***
1006. ***adf8a61a940c kprobes: treewide: Make it harder to refer kretprobe\_trampoline directly***
1007. ***bb4a23c994ae riscv/vdso: Refactor asm/vdso.h***
1008. ***78a743cd82a3 riscv/vdso: Move vdso data page up front***
1009. ***8bb0ab3ae7a4 riscv/vdso: make arch\_setup\_additional\_pages wait for mmap\_sem for write killable***
1010. ***3f2401f47d29 RISC-V: Add hypervisor extension related CSR defines***
1011. ***99cdc6c18c2d RISC-V: Add initial skeletal KVM support***
1012. ***a33c72faf2d7 RISC-V: KVM: Implement VCPU create, init and destroy functions***
1013. ***cce69aff689e RISC-V: KVM: Implement VCPU interrupts and requests handling***
1014. ***92ad82002c39 RISC-V: KVM: Implement KVM\_GET\_ONE\_REG/KVM\_SET\_ONE\_REG ioctls***
1015. ***34bde9d8b9e6 RISC-V: KVM: Implement VCPU world-switch***
1016. ***9f7013265112 RISC-V: KVM: Handle MMIO exits for VCPU***
1017. ***5a5d79acd7da RISC-V: KVM: Handle WFI exits for VCPU***
1018. ***fd7bb4a251df RISC-V: KVM: Implement VMID allocator***
1019. ***9d05c1fee837 RISC-V: KVM: Implement stage2 page table programming***
1020. ***9955371cc014 RISC-V: KVM: Implement MMU notifiers***
1021. ***3a9f66cb25e1 RISC-V: KVM: Add timer functionality***
1022. ***5de52d4a23ad RISC-V: KVM: FP lazy save/restore***
1023. ***4d9c5c072f03 RISC-V: KVM: Implement ONE REG interface for FP registers***
1024. ***dea8ee31a039 RISC-V: KVM: Add SBI v0.1 support***
1025. ***dffe11e280a4 riscv/vdso: Add support for time namespaces***
1026. ***f2928e224d85 riscv: set default pm\_power\_off to NULL***
1027. ***21ccdccd21e4 riscv: mm: don't advertise 1 num\_asid for 0 asid bits***
1028. ***59a4e0d5511b RISC-V: Include clone3() on rv32***
1029. ***5d4595db0e1c riscv: add rv32 and rv64 randconfig build targets***
1030. ***bb8958d5dc79 riscv: Flush current cpu icache before other cpus***
1031. ***6644c654ea70 ftrace: Cleanup ftrace\_dyn\_arch\_init()***
1032. ***42a20f86dc19 sched: Add wrapper for get\_wchan() to keep task blocked***
1033. ***bd2259ee458e riscv: Use of\_get\_cpu\_hwid()***
1034. ***8f04db78e4e3 bpf: Define bpf\_jit\_alloc\_exec\_limit for riscv JIT***
1035. ***2fe35f8ee726 irq: add a (temporary) CONFIG\_HANDLE\_DOMAIN\_IRQ\_IRQENTRY***
1036. ***7ecbc648102f irq: riscv: perform irqentry in entry code***
1037. ***0953fb263714 irq: remove handle\_domain\_{irq,nmi}()***
1038. ***f9ace4ede49b riscv: remove .text section size limitation for XIP***
1039. ***683b33f7e7ec riscv/vdso: Drop unneeded part due to merge issue***
1040. ***ce5e48036c9e ftrace: disable preemption when recursion locked***
1041. ***64a19591a293 riscv: fix misalgned trap vector base address***
1042. ***ffa7a9141bb7 riscv: defconfig: enable DRM\_NOUVEAU***
1043. ***252c765bd764 riscv, bpf: Add BPF exception tables***
1044. ***27de809a3d83 riscv, bpf: Fix potential NULL dereference***
1045. ***cf11d01135ea riscv: Do not re-populate shadow memory with kasan\_populate\_early\_shadow***
1046. ***54c5639d8f50 riscv: Fix asan-stack clang build***
1047. ***0a86512dc113 RISC-V: KVM: Factor-out FP virtualization into separate sources***
1048. ***7c8de080d476 RISC-V: KVM: Fix GPA passed to \_\_kvm\_riscv\_hfence\_gvma\_xyz() functions***
1049. ***7b161d9cab5d RISC-V: KVM: remove unneeded semicolon***
1050. ***bbd5ba8db766 RISC-V: KVM: fix boolreturn.cocci warnings***
1051. ***4b54214f39ff riscv, bpf: Increase the maximum number of iterations***
1052. ***f47d4ffe3a84 riscv, bpf: Fix RV32 broken build, and silence RV64 warning***
1053. ***3ecc68349bba memblock: rename memblock\_free to memblock\_phys\_free***
1054. ***4421cca0a3e4 memblock: use memblock\_free for freeing virtual pointers***
1055. ***0e2e64192100 riscv: kvm: fix non-kernel-doc comment block***
1056. ***37fd3ce1e64a KVM: RISC-V: Cap KVM\_CAP\_NR\_VCPUS by KVM\_CAP\_MAX\_VCPUS***
1057. ***12c484c12b19 RISC-V: Enable KVM in RV64 and RV32 defconfigs as a module***
1058. ***5a19c7e06236 riscv: fix building external modules***
1059. ***756e1fc16505 KVM: RISC-V: Unmap stage2 mapping when deleting/moving a memslot***
1060. ***74c2e97b0184 RISC-V: KVM: Fix incorrect KVM\_MAX\_VCPUS value***
1061. ***4bc5e64e6cf3 efi: Move efifb\_setup\_from\_dmi() prototype from arch headers***

當然，內容還是太多，1000 多條記錄，所以還是需要分解，我們目前基於上述的 Commits 以及收集的相關資料，整理出了一份[任務清單](https://gitee.com/tinylab/riscv-linux/blob/master/plan/README.md)。

任務清單中大體做了模組劃分，但是還比較粗糙，建議大家在分析的過程中直接提交 PR 進行修訂。

大家可結合自己的興趣認領感興趣的模組，比如說 Ftrace，認領後可以重點分析相關程式碼，這樣的話，可以用關鍵字 ftrace 過濾出這部分的 commits：

1. **$ git rev-list --oneline 76d2a0493a17^..v5.16 --reverse arch/riscv | grep -i ftrace**
2. **10626c32e382 riscv/ftrace: Add basic support**
3. **a1d2a6b4cee8 riscv/ftrace: Add RECORD\_MCOUNT support**
4. **c15ac4fd60d5 riscv/ftrace: Add dynamic function tracer support**
5. **bc1a4c3a8425 riscv/ftrace: Add dynamic function graph tracer support**
6. **71e736a7d655 riscv/ftrace: Add ARCH\_SUPPORTS\_FTRACE\_OPS support**
7. **aea4c671fb98 riscv/ftrace: Add DYNAMIC\_FTRACE\_WITH\_REGS support**
8. **b785ec129bd9 riscv/ftrace: Add HAVE\_FUNCTION\_GRAPH\_RET\_ADDR\_PTR support**
9. **1dd985229d5f riscv/ftrace: Export \_mcount when DYNAMIC\_FTRACE isn't set**
10. **57a489786de9 RISC-V: include linux/ftrace.h in asm-prototypes.h**
11. **397182e0db56 riscv: remove unused variable in ftrace**
12. **1d8f65798240 riscv: ftrace: correct the condition logic in function graph tracer**
13. **e05d57dcb8c7 riscv: Fixup \_\_vdso\_gettimeofday broke dynamic ftrace**
14. **66d18dbda846 RISC-V: Take text\_mutex in ftrace\_init\_nop()**
15. **9d750c75bd2c risc-v: kernel: ftrace: Fixes improper SPDX comment style**
16. **67d945778099 riscv: Fixup wrong ftrace remove cflag**
17. **5ad84adf5456 riscv: Fixup patch\_text panic in ftrace**
18. **829adda597fe riscv: Add KPROBES\_ON\_FTRACE supported**
19. **288f6775a089 riscv: ftrace: Use ftrace\_get\_regs helper**
20. **bab1770a2ce0 ftrace: Fix spelling mistake "disabed" -> "disabled"**
21. **e31be8d343e6 riscv: kprobes/ftrace: Add recursion protection to the ftrace callback**
22. **adebc8817b5c riscv: Select HAVE\_DYNAMIC\_FTRACE when -fpatchable-function-entry is available**
23. **6644c654ea70 ftrace: Cleanup ftrace\_dyn\_arch\_init()**
24. **ce5e48036c9e ftrace: disable preemption when recursion locked**

根據這些 Commits，又可以分析各個子功能又是如何一步一步新增的，對於一些簡單的 fixups 和 Comments 修訂，完全可以直接納入到某個子功能當中去，無需單獨輸出分析報告。

其他的特性功能也可以類似分析，比如 KVM，eBPF, kprobes 等等。

**5 閱讀具體程式碼**

接下來簡單介紹如何結合 vim 與 cscope 查閱程式碼。

首先，建立程式碼索引（如果系統記憶體不夠，可能會被Kill掉從而無法建立完整索引），方便閱讀時跳轉：

1. **$ cd /labs/linux-lab**
2. **$ make kernel cscope**

建立後，進入 Linux 建構目錄：

1. **$ cd build/riscv64/build-v5.16-virt/**
2. **$ vim**
3. **:cs add cscope.out**
4. **:cs find g setup\_arch**

以上即可找到 setup\_arch 的定義，如果手動不方便，可以參考 [把 VIM 打造成原始碼編輯器](https://tinylab.org/make-vim-source-code-editor/) 組態 cscope 的快件鍵，加速程式碼閱讀體驗。

在閱讀原始碼的過程中，建議參考 refs/README.md 中列出的官方 Spec 等資料進行更準確地解釋。

**6 程式碼修改實驗**

在分析的過程中，如果想調整程式碼以便觀察運行效果或者發現了 Bug 想驗證修訂與否，可以直接用 Linux Lab 或 Linux Lab Disk 運行：

1. **$ make boot**

**7 輸出分析成果**

在分析完某個模組以後，可以撰寫成類似本文的原始風格 markdown 格式（請注意段落層次、程式碼風格等，不要用複雜的 markdown 風格），並提交 PR 到 articles/ 目錄下。

如果某個模組還是比較大，可以細分成多個子模組進行分析和輸出。在完成度比較高的情況下，也可以製作成幻燈片進行視訊講解。

如涉及網路已存在的資料和圖片引用等，請直接用“連結”方式，如果是自己設計、繪製或者製作的圖片，可以上傳到 articles/images/your-article-short-title 目錄下。

**8 小結**

本文簡單介紹了如何分析 Linux 核心的 RISC-V 架構支援。