# L3G4200D

## MEMS motion sensor: three-axis digital output gyroscope

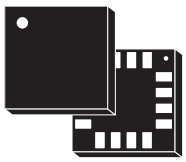
**Preliminary data**

## Features

- Three selectable full scales (250/500/2000 dps)
- $I^2C$/SPI digital output interface
- 16 bit-rate value data output
- 8-bit temperature data output
- Two digital output lines (interrupt and data ready)
- Integrated low- and high-pass filters with user-selectable bandwidth
- Embedded self-test
- Wide supply voltage: 2.4 V to 3.6 V
- Low voltage-compatible IOs (1.8 V)
- Embedded power-down and sleep mode
- Embedded temperature sensor
- 96 levels of 16-bit data output (FIFO)
- High shock survivability
- Extended operating temperature range (-40 °C to +85 °C)
- ECOPACK® RoHS and “Green” compliant

## Applications

- Gaming and virtual reality input devices
- Motion control with MMI (man-machine interface)
- GPS navigation systems
- Appliances and robotics



**LGA-16 (4x4x1.1 mm)**

## Description

The L3G4200D is a low-power three-axis angular rate sensor.

It includes a sensing element and an IC interface capable of providing the measured angular rate to the external world through a digital interface ($I^2C$/SPI).

The sensing element is manufactured using a dedicated micro-machining process developed by STMicroelectronics to produce inertial sensors and actuators on silicon wafers.

The IC interface is manufactured using a CMOS process that allows a high level of integration to design a dedicated circuit which is trimmed to better match the sensing element characteristics.

The L3G4200D has a full scale of ±250/±500/ ±2000 dps and is capable of measuring rates with a user-selectable bandwidth.

The L3G4200D is available in a plastic land grid array (LGA) package and can operate within a temperature range of -40 °C to +85 °C.

**Table 1. Device summary**

| Order code | Temperature range (°C) | Package | Packing |
|---|---|---|---|
| L3G4200D | -40 to +85 | LGA-16 (4x4x1.1 mm) | Tray |
| L3G4200DTR | -40 to +85 | LGA-16 (4x4x1.1 mm) | Tape and reel |

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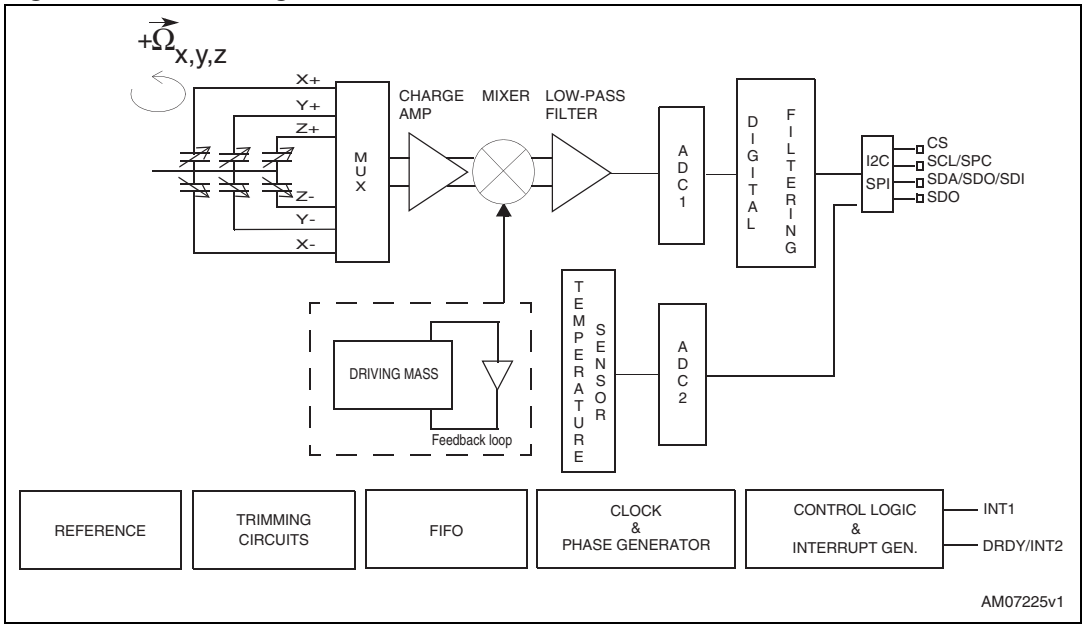
# 1 Block diagram and pin description

**Figure 1. Block diagram**




The vibration of the structure is maintained by drive circuitry in a feedback loop. The sensing signal is filtered and appears as a digital signal at the output.

## 1.1 Pin description

**Figure 2. Pin connection**

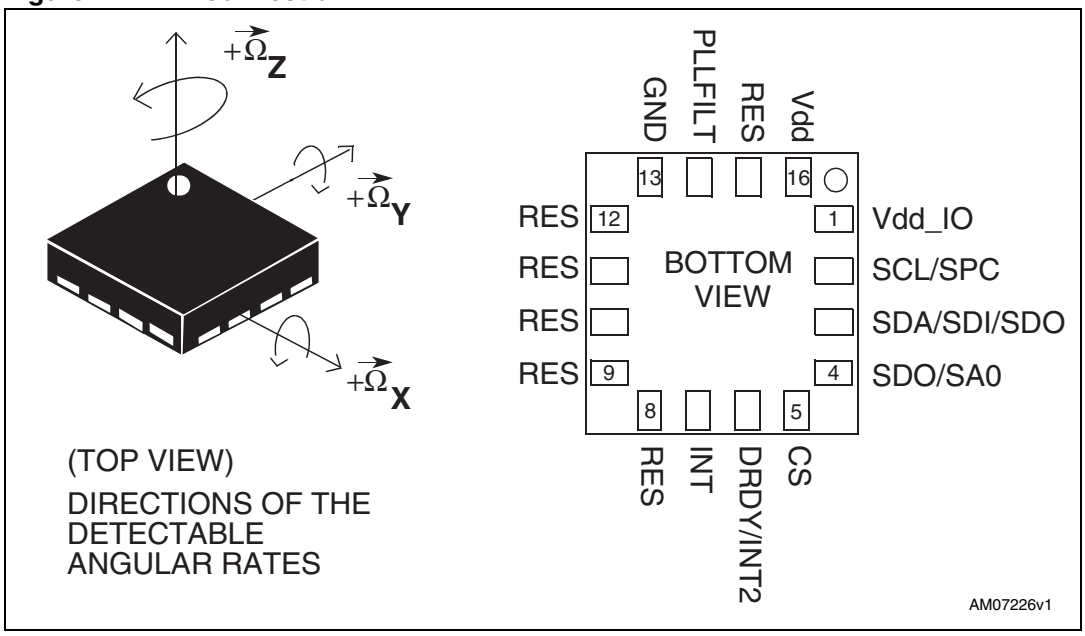
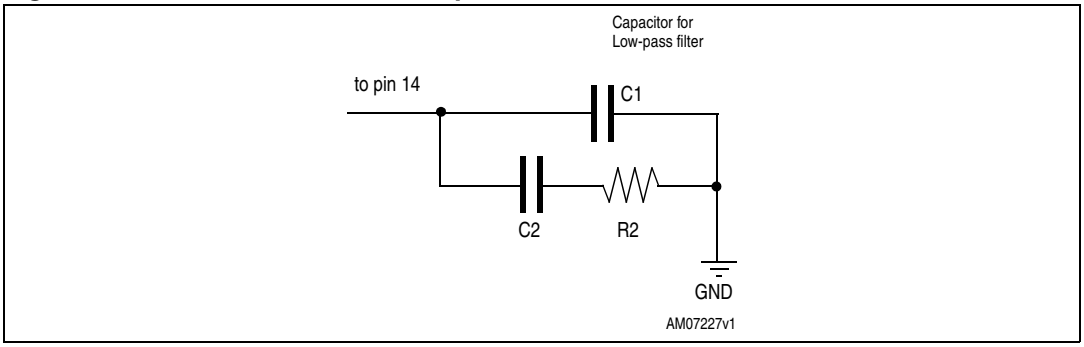


**Table 2. Pin description**

| Pin# | Name | Function |
|---|---|---|
| 1 | Vdd_IO | Power supply for I/O pins |
| 2 | SCL<br>SPC | $I^2C$ serial clock (SCL)<br>SPI serial port clock (SPC) |
| 3 | SDA<br>SDI<br>SDO | $I^2C$ serial data (SDA)<br>SPI serial data input (SDI)<br>3-wire interface serial data output (SDO) |
| 4 | SDO<br>SA0 | SPI serial data output (SDO)<br>$I^2C$ least significant bit of the device address (SA0) |
| 5 | CS | SPI enable<br>$I^2C$/SPI mode selection (1:$I^2C$ mode; 0: SPI enabled) |
| 6 | DRDY/INT2 | Data ready/FIFO interrupt |
| 7 | INT1 | Programmable interrupt |
| 8 | Reserved | Connect to GND |
| 9 | Reserved | Connect to GND |
| 10 | Reserved | Connect to GND |
| 11 | Reserved | Connect to GND |
| 12 | Reserved | Connect to GND |
| 13 | GND | 0 V supply |
| 14 | PLLFILT | Phase-locked loop filter (see *Figure 3*) |
| 15 | Reserved | Connect to Vdd |
| 16 | Vdd | Power supply |

**Figure 3. L3G4200D external low-pass filter values (a)**




a. Pin 14 PLLFILT maximum voltage level is equal to Vdd.

Table 3. Filter values

| Parameter | Typical value |
|---|---|
| C1 | 10 nF |
| C2 | 470 nF |
| R2 | 10 kΩ |

# 2 Mechanical and electrical characteristics

## 2.1 Mechanical characteristics

**Table 4. Mechanical characteristics @ Vdd = 3.0 V, T = 25 °C, unless otherwise noted(1)**

| Symbol | Parameter | Test condition | Min. | Typ.(2) | Max. | Unit |
|---|---|---|---|---|---|---|
| FS | Measurement range | User-selectable | | ±250 | | dps |
| | | | | ±500 | | |
| | | | | ±2000 | | |
| So | Sensitivity | FS = 250 dps | | 8.75 | | mdps/digit |
| | | FS = 500 dps | | 17.50 | | |
| | | FS = 2000 dps | | 70 | | |
| SoDr | Sensitivity change vs. temperature | From -40 °C to +85 °C | | ±2 | | % |
| DVoff | Digital zero-rate level | FS = 250 dps | | ±10 | | dps |
| | | FS = 500 dps | | ±15 | | |
| | | FS = 2000 dps | | ±75 | | |
| OffDr | Zero-rate level change vs. temperature(3) | FS = 250 dps | | ±0.03 | | dps/°C |
| | | FS = 2000 dps | | ±0.04 | | dps/°C |
| NL | Non linearity(4) | Best fit straight line | | 0.2 | | % FS |
| DST | Self-test output change | FS = 250 dps | | 130 | | dps |
| | | FS = 500 dps | | 200 | | |
| | | FS = 2000 dps | | 530 | | |
| Rn | Rate noise density | BW = 40 Hz | | 0.03 | | dps/ |
| ODR | Digital output data rate | | | 100/200/ 400/800 | | Hz |
| Top | Operating temperature range | | -40 | | +85 | °C |

1. The product is factory calibrated at 3.0 V. The operational power supply range is specified in *Table 5*.
2. Typical specifications are not guaranteed.
3. Min/max values have been estimated based on the measurements of the current gyros in production.
4. Guaranteed by design.

## 2.2 Electrical characteristics

**Table 5. Electrical characteristics @ Vdd =3.0 V, T=25 °C, unless otherwise noted(1)**

| Symbol | Parameter | Test condition | Min. | Typ.(2) | Max. | Unit |
|---|---|---|---|---|---|---|
| Vdd | Supply voltage | | 2.4 | 3.0 | 3.6 | V |
| Vdd_IO | I/O pins supply voltage(3) | | 1.71 | | Vdd+0.1 | V |
| Idd | Supply current | | | 6.1 | | mA |
| IddSL | Supply current in sleep mode(4) | Selectable by digital interface | | 1.5 | | mA |
| IddPdn | Supply current in power-down mode | Selectable by digital interface | | 5 | | µA |
| Top | Operating temperature range | | -40 | | +85 | °C |

1. The product is factory calibrated at 3.0 V.
2. Typical specifications are not guaranteed.
3. It is possible to remove Vdd maintaining Vdd_IO without blocking the communication busses, in this condition the measurement chain is powered off.
4. Sleep mode introduces a faster turn-on time compared to power-down mode.

## 2.3 Temperature sensor characteristics

**Table 6. Temp. sensor characteristics @ Vdd =3.0 V, T=25 °C, unless otherwise noted(1)**

| Symbol | Parameter | Test condition | Min. | Typ.(2) | Max. | Unit |
|---|---|---|---|---|---|---|
| TSDr | Temperature sensor output change vs. temperature | | | -1 | | °C/digit |
| TODR | Temperature refresh rate | | | 1 | | Hz |
| Top | Operating temperature range | | -40 | | +85 | °C |

1. The product is factory calibrated at 3.0 V.
2. Typical specifications are not guaranteed.

## 2.4 Communication interface characteristics

### 2.4.1 SPI - serial peripheral interface

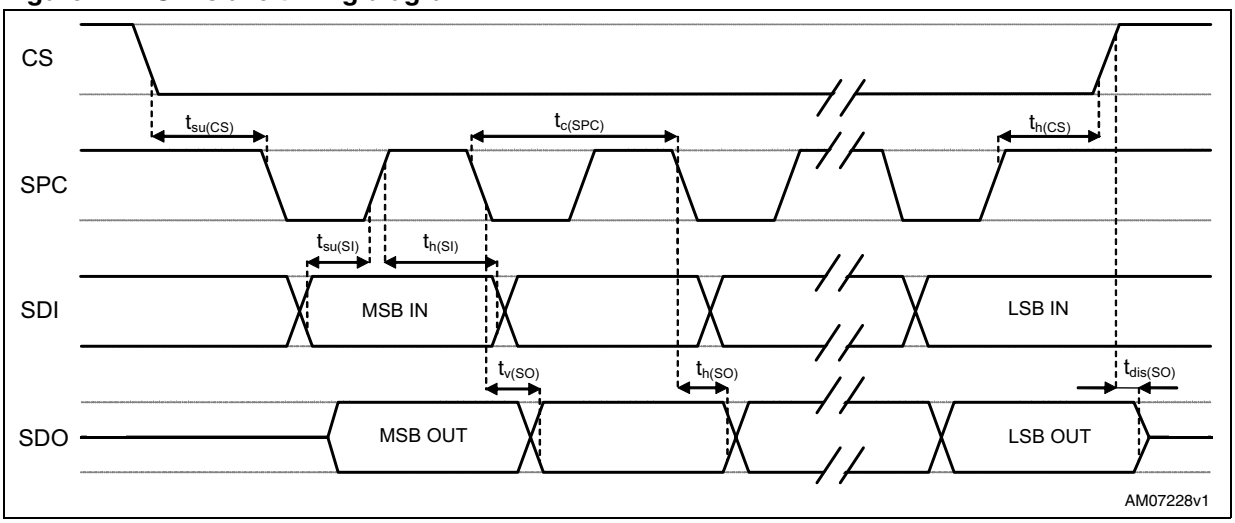
Subject to general operating conditions for Vdd and Top.

**Table 7. SPI slave timing values**

| Symbol | Parameter | Value(1) | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| tc(SPC) | SPI clock cycle | 100 | | ns |
| fc(SPC) | SPI clock frequency | | 10 | MHz |
| tsu(CS) | CS setup time | 5 | | ns |
| th(CS) | CS hold time | 8 | | |
| tsu(SI) | SDI input setup time | 5 | | |
| th(SI) | SDI input hold time | 15 | | |
| tv(SO) | SDO valid output time | | 50 | |
| th(SO) | SDO output hold time | 6 | | |
| tdis(SO) | SDO output disable time | | 50 | |

1. Values are guaranteed at 10 MHz clock frequency for SPI with both 4 and 3 wires, based on characterization results; not tested in production.

**Figure 4. SPI slave timing diagram(b)**




b. Measurement points are done at 0.2·Vdd_IO and 0.8·Vdd_IO, for both input and output ports.

### 2.4.2 I²C - inter IC control interface

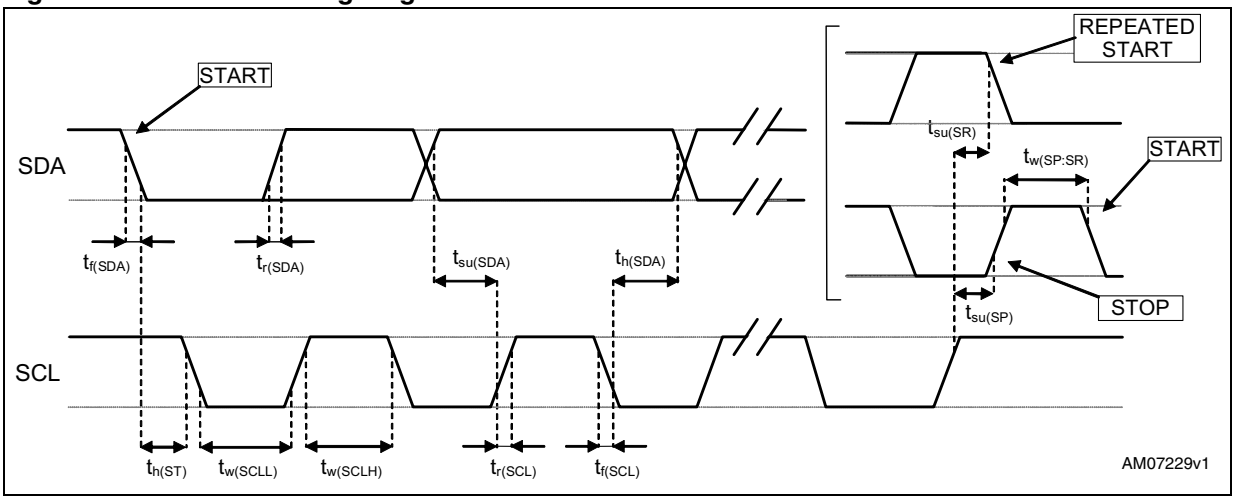
Subject to general operating conditions for Vdd and Top.

**Table 8. I²C slave timing values (TBC)**

| Symbol | Parameter | I²C standard mode(1) | | I²C fast mode (1) | | Unit |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| $f_{(SCL)}$ | SCL clock frequency | 0 | 100 | 0 | 400 | kHz |
| $t_{w(SCLL)}$ | SCL clock low time | 4.7 | | 1.3 | | µs |
| $t_{w(SCLH)}$ | SCL clock high time | 4.0 | | 0.6 | | |
| $t_{su(SDA)}$ | SDA setup time | 250 | | 100 | | ns |
| $t_{h(SDA)}$ | SDA data hold time | 0 | 3.45 | 0 | 0.9 | µs |
| $t_{r(SDA)}$ $t_{r(SCL)}$ | SDA and SCL rise time | | 1000 | $20 + 0.1C_b$ (2) | 300 | ns |
| $t_{f(SDA)}$ $t_{f(SCL)}$ | SDA and SCL fall time | | 300 | $20 + 0.1C_b$ (2) | 300 | |
| $t_{h(ST)}$ | START condition hold time | 4 | | 0.6 | | µs |
| $t_{su(SR)}$ | Repeated START condition setup time | 4.7 | | 0.6 | | |
| $t_{su(SP)}$ | STOP condition setup time | 4 | | 0.6 | | |
| $t_{w(SP:SR)}$ | Bus free time between STOP and START condition | 4.7 | | 1.3 | | |

1. Data based on standard I²C protocol requirement; not tested in production.
2. Cb = total capacitance of one bus line, in pF.

**Figure 5. I²C slave timing diagram (c)**




c. Measurement points are done at 0.2·Vdd_IO and 0.8·Vdd_IO, for both ports.

## 2.5 Absolute maximum ratings

Any stress above that listed as “Absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

**Table 9. Absolute maximum ratings**

| Symbol | Ratings | Maximum value | Unit |
|---|---|---|---|
| Vdd | Supply voltage | -0.3 to 4.8 | V |
| $T_{STG}$ | Storage temperature range | -40 to +125 | °C |
| Sg | Acceleration *g* for 0.1 ms | 10,000 | *g* |
| ESD | Electrostatic discharge protection | 2 (HBM) | kV |

This is a mechanical shock sensitive device, improper handling can cause permanent damage to the part

This is an ESD sensitive device, improper handling can cause permanent damage to the part

## 2.6 Terminology

### 2.6.1 Sensitivity

An angular rate gyroscope is a device that produces a positive-going digital output for counterclockwise rotation around the sensitive axis considered. Sensitivity describes the gain of the sensor and can be determined by applying a defined angular velocity to it. This value changes very little over temperature and time.

### 2.6.2 Zero-rate level

Zero-rate level describes the actual output signal if there is no angular rate present. The zero-rate level of precise MEMS sensors is, to some extent, a result of stress to the sensor and, therefore, the zero-rate level can slightly change after mounting the sensor onto a printed circuit board or after exposing it to extensive mechanical stress. This value changes very little over temperature and time.

### 2.6.3 Self-test

Self-test allows testing of the mechanical and electric part of the sensor, allowing the seismic mass to be moved by means of an electrostatic test-force. When self-test is activated by the IC, an actuation force is applied to the sensor, emulating a definite Coriolis force. In this case the sensor output exhibits an output change.

When ST (self-test) is active, the device output level is given by the algebraic sum of the signals produced by the velocity acting on the sensor and by the electrostatic test-force.

## 2.7 Soldering information

The LGA package is compliant with the ECOPACK®, RoHS and “Green” standard.
It is qualified for soldering heat resistance according to JEDEC J-STD-020.

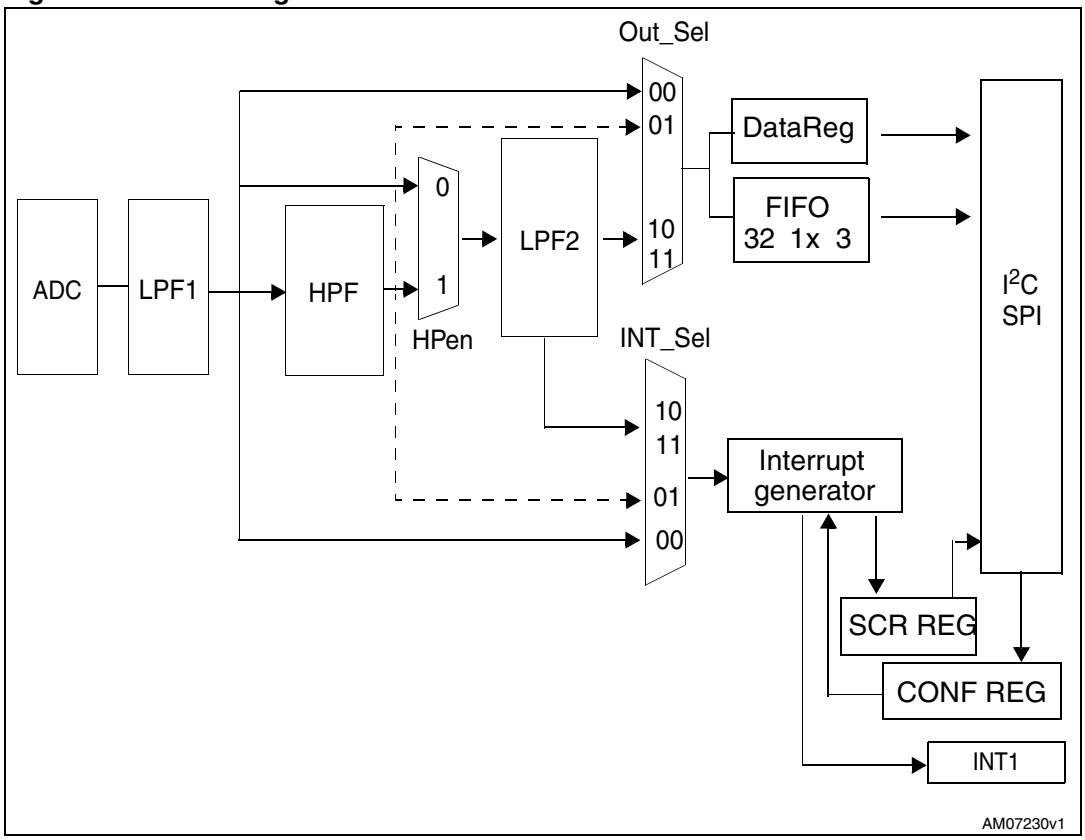
Leave “pin 1 Indicator” unconnected during soldering.

Land pattern and soldering recommendations are available at www.st.com/.

# 3 Main digital blocks

## 3.1 Block diagram

**Figure 6. Block diagram**



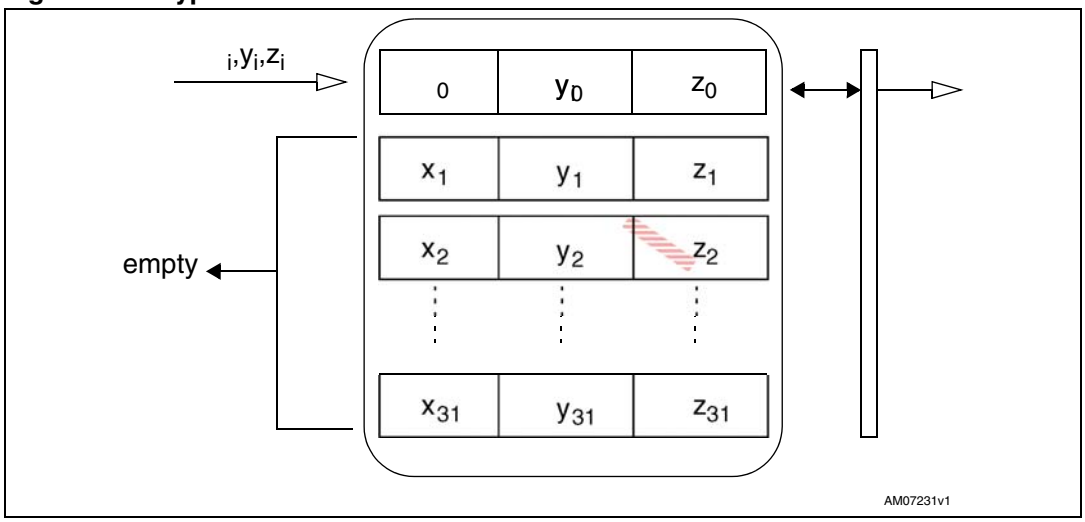

## 3.2 FIFO

The L3G4200D embeds a 32-slot, 16-bit data FIFO for each of the three output channels: yaw, pitch, and roll. This allows consistent power saving for the system, as the host processor does not need to continuously poll data from the sensor. Instead, it can wake up only when needed and burst the significant data out from the FIFO. This buffer can work in five different modes. Each mode is selected by the FIFO_MODE bits in the FIFO_CTRL_REG. Programmable watermark level, FIFO_empty or FIFO_Full events can be enabled to generate dedicated interrupts on the DRDY/INT2 pin (configured through CTRL_REG3), and event detection information is available in FIFO_SRC_REG. The watermark level can be configured to WTM4:0 in FIFO_CTRL_REG.

### 3.2.1 Bypass mode

In bypass mode, the FIFO is not operational and for this reason it remains empty. As illustrated in *Figure 7*, only the first address is used for each channel. The remaining FIFO slots are empty. When new data is available, the old data is overwritten.

**Figure 7. Bypass mode**

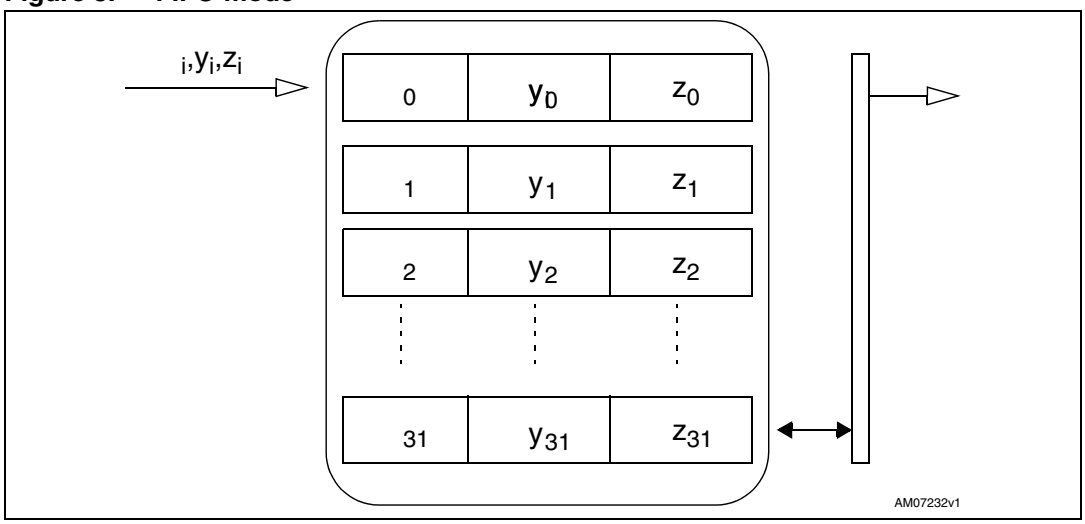



### 3.2.2 FIFO mode

In FIFO mode, data from the yaw, pitch, and roll channels are stored in the FIFO. A watermark interrupt can be enabled (I2_WMK bit in CTRL_REG3), which is triggered when the FIFO is filled to the level specified in the WTM 4:0 bits of FIFO_CTRL_REG. The FIFO continues filling until it is full (32 slots of 16-bit data for yaw, pitch, and roll). When full, the FIFO stops collecting data from the input channels. To restart data collection, it is necessary to write FIFO_CTRL_REG back to bypass mode.

FIFO mode is represented in *Figure 8*.

**Figure 8. FIFO mode**



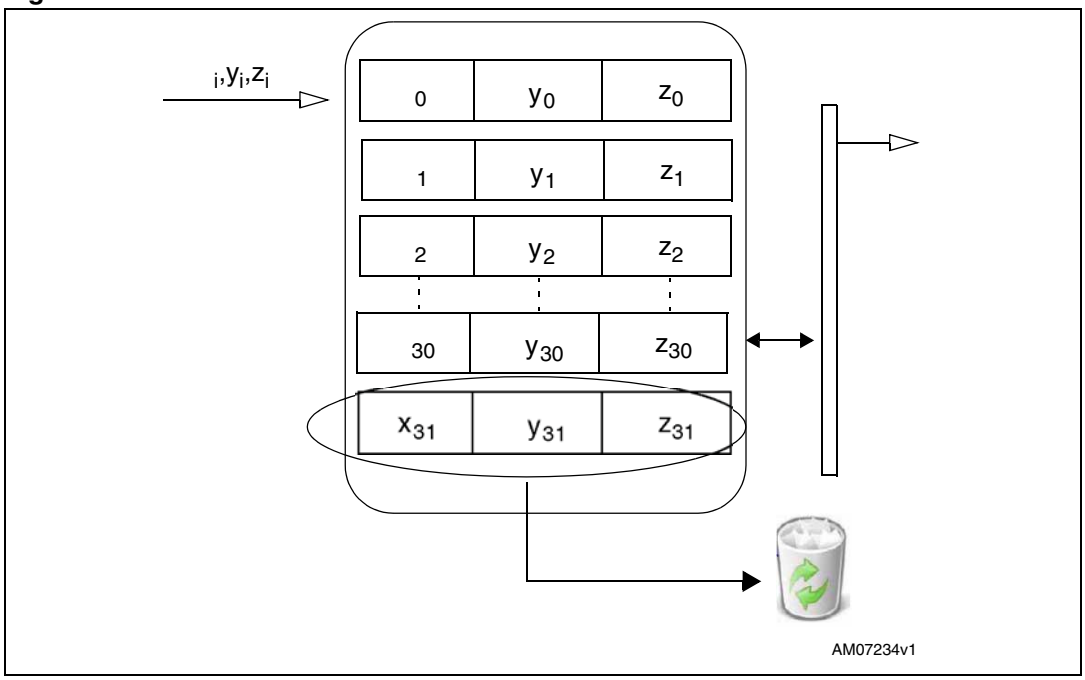

### 3.2.3 Stream mode

In stream mode, data from yaw, pitch, and roll measurements are stored in the FIFO. A watermark interrupt can be enabled and set as in FIFO mode. The FIFO continues filling until full (32 slots of 16-bit data for yaw, pitch, and roll). When full, the FIFO discards the

older data as the new data arrives. Programmable watermark level events can be enabled to generate dedicated interrupts on the DRDY/INT2 pin (configured through CTRL_REG3).

Stream mode is represented in *Figure 9*.

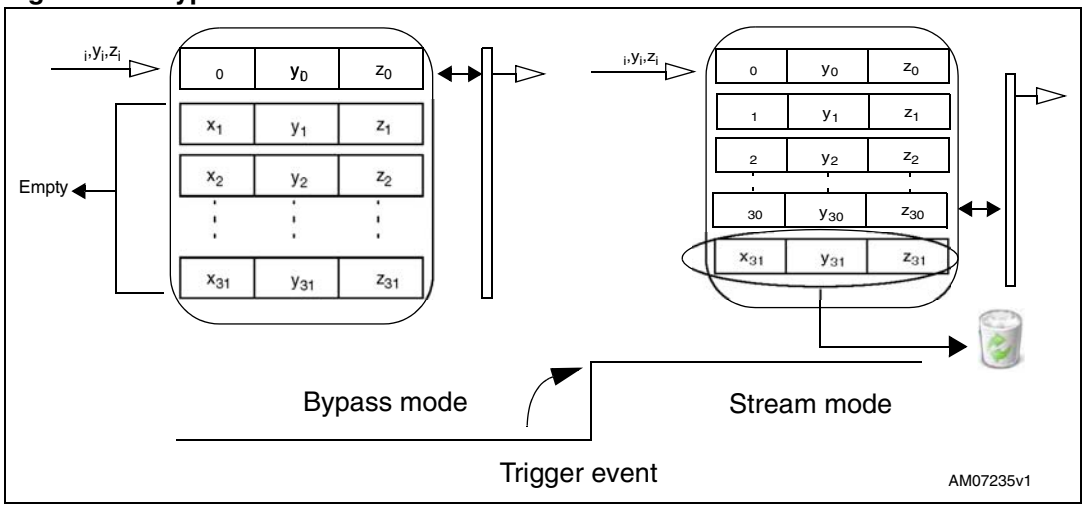
**Figure 9. Stream mode**




## 3.2.4 Bypass-to-stream mode

In bypass-to-stream mode, the FIFO starts operating in bypass mode, and once a trigger event occurs (related to INT1_CFG register events), the FIFO starts operating in stream mode (see *Figure 10*).

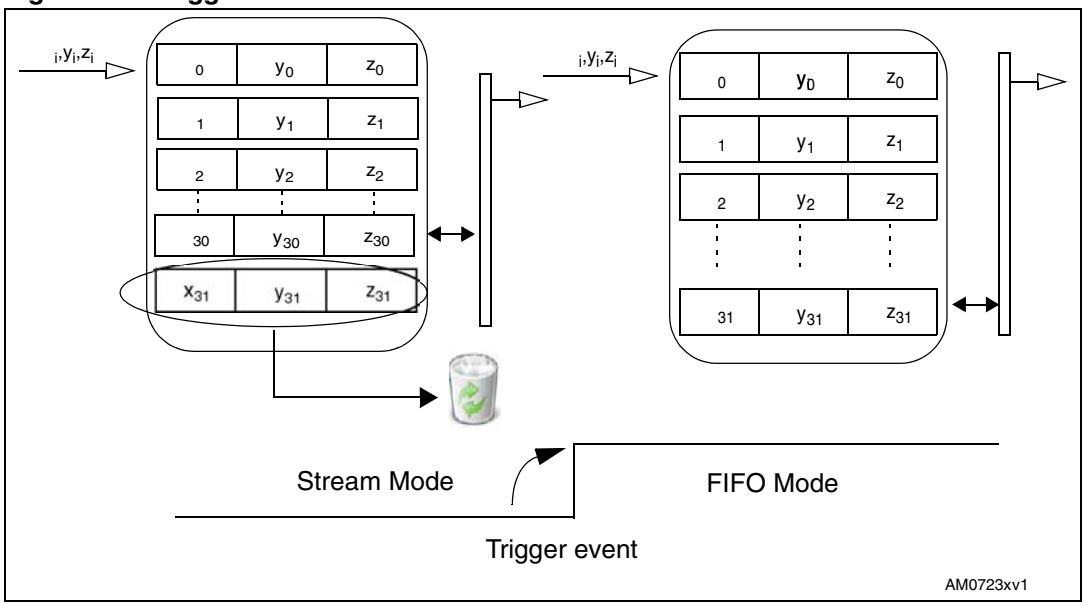
**Figure 10. Bypass-to-stream mode**



### 3.2.5 Stream-to-FIFO mode

In stream-to-FIFO mode, data from yaw, pitch, and roll measurements are stored in the FIFO. A watermark interrupt can be enabled on pin DRDY/INT2, setting the I2_WTM bit in CTRL_REG3, which is triggered when the FIFO is filled to the level specified in the WTM4:0 bits of FIFO_CTRL_REG. The FIFO continues filling until full (32 slots of 16-bit data for yaw, pitch, and roll). When full, the FIFO discards the older data as the new data arrives. Once a trigger event occurs (related to INT1_CFG register events), the FIFO starts operating in FIFO mode (see *Figure 11*).

**Figure 11. Trigger stream mode**

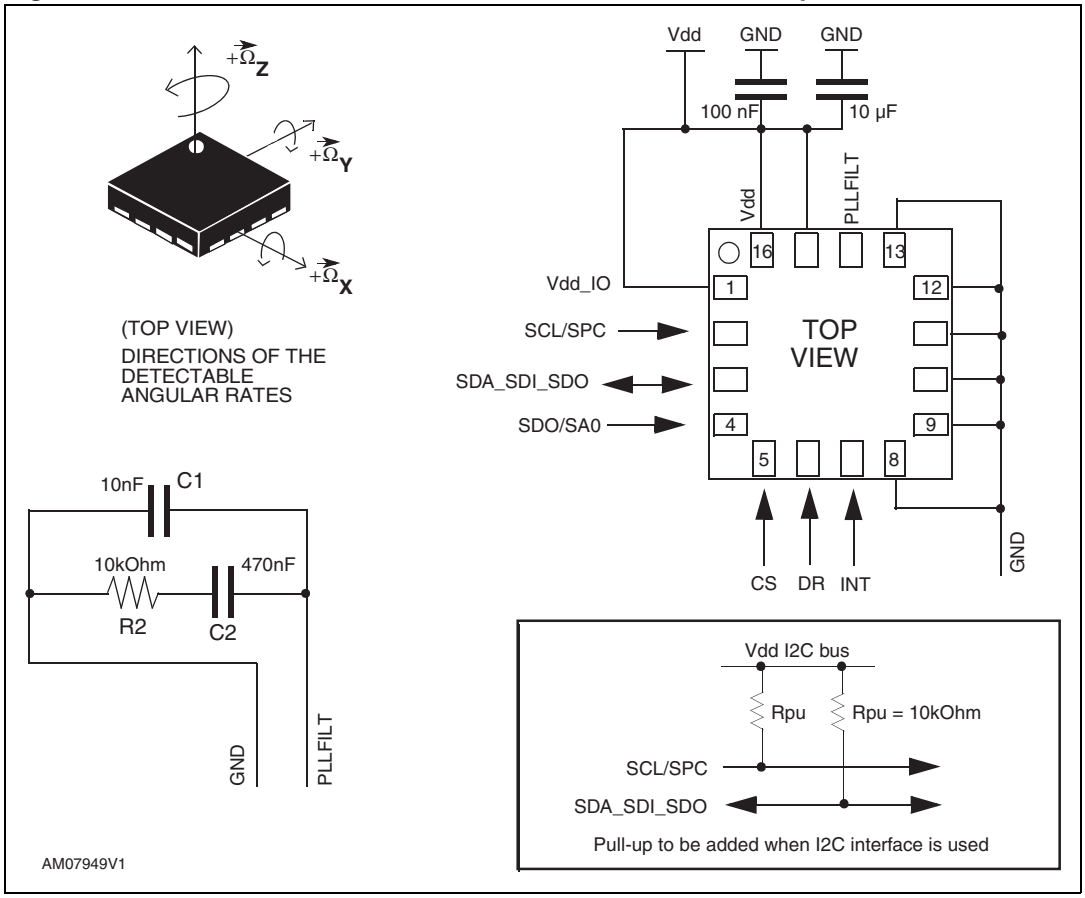



### 3.2.6 Retrieve data from FIFO

FIFO data is read through the OUT_X, OUT_Y and OUT_Z registers. When the FIFO is in stream, trigger or FIFO mode, a read operation to the OUT_X, OUT_Y or OUT_Z registers provides the data stored in the FIFO. Each time data is read from the FIFO, the oldest pitch, roll, and yaw data are placed in the OUT_X, OUT_Y and OUT_Z registers and both single read and read_burst (X,Y & Z with auto-incremental address) operations can be used. In read_burst mode, when data included in OUT_Z_H is read, the system again starts to read information from addr OUT_X_L.

# 4 Application hints

**Figure 12. L3G4200D electrical connections and external component values**




Power supply decoupling capacitors (100 nF ceramic or polyester +10 µF) should be placed as near as possible to the device (common design practice).

If Vdd and Vdd_IO are not connected together, power supply decoupling capacitors (100 nF and 10 µF between Vdd and common ground, 100 nF between Vdd_IO and common ground) should be placed as near as possible to the device (common design practice).

The L3G4200D IC includes a PLL (phase locked loop) circuit to synchronize driving and sensing interfaces. Capacitors and resistors must be added at the **PLLFILT** pin (as shown in *Figure 12*) to implement a second-order low-pass filter. *Table 10* summarizes the PLL low-pass filter component values.

**Table 10. PLL low-pass filter component values**

| Component | Value |
|---|---|
| C1 | 10 nF ± 10 % |
| C2 | 470 nF ± 10 % |
| R2 | 10 kΩ ± 10 % |

# 5 Digital interfaces

The registers embedded in the L3G4200DH may be accessed through both the $I^2C$ and SPI serial interfaces. The latter may be software-configured to operate either in 3-wire or 4-wire interface mode.

The serial interfaces are mapped onto the same pins. To select/exploit the $I^2C$ interface, the CS line must be tied high (i.e., connected to Vdd_IO).

**Table 11. Serial interface pin description**

| Pin name | Pin description |
|---|---|
| CS | SPI enable<br>$I^2C$/SPI mode selection (1: $I^2C$ mode; 0: SPI enabled) |
| SCL/SPC | $I^2C$ serial clock (SCL)<br>SPI serial port clock (SPC) |
| SDA/SDI/SDO | $I^2C$ serial data (SDA)<br>SPI serial data input (SDI)<br>3-wire interface serial data output (SDO) |
| SDO | SPI serial data output (SDO)<br>$I^2C$ least significant bit of the device address |

## 5.1 $I^2C$ serial interface

The L3G4200DH $I^2C$ is a bus slave. The $I^2C$ is employed to write data to registers whose content can also be read back.

The relevant $I^2C$ terminology is given in the table below.

**Table 12. $I^2C$ terminology**

| Term | Description |
|---|---|
| Transmitter | The device which sends data to the bus |
| Receiver | The device which receives data from the bus |
| Master | The device which initiates a transfer, generates clock signals and terminates a transfer |
| Slave | The device addressed by the master |

There are two signals associated with the $I^2C$ bus: the serial clock line (SCL) and the serial data line (SDA). The latter is a bidirectional line used for sending and receiving the data to/from the interface. Both lines must be connected to Vdd_IO through an external pull-up resistor. When the bus is free both the lines are high.

The $I^2C$ interface is compliant with fast mode (400 kHz) $I^2C$ standards as well as with normal mode.

### 5.1.1 I²C operation

The transaction on the bus is started through a START (ST) signal. A START condition is defined as a HIGH to LOW transition on the data line while the SCL line is held HIGH. After this has been transmitted by the master, the bus is considered busy. The next byte of data transmitted after the start condition contains the address of the slave in the first 7 bits and the eighth bit tells whether the master is receiving data from the slave or transmitting data to the slave. When an address is sent, each device in the system compares the first 7 bits after a start condition with its address. If they match, the device considers itself addressed by the master.

The slave address (SAD) associated with the L3G4200DH is 110100xb. The SDO pin can be used to modify the least significant bit (LSb) of the device address. If the SDO pin is connected to the voltage supply, LSb is '1' (address 1101001b). Otherwise, if the SDO pin is connected to ground, the LSb value is '0' (address 1101000b). This solution permits the connection and addressing of two different gyroscopes to the same I²C bus.

Data transfer with acknowledge is mandatory. The transmitter must release the SDA line during the acknowledge pulse. The receiver must then pull the data line LOW so that it remains stable low during the HIGH period of the acknowledge clock pulse. A receiver which has been addressed is obliged to generate an acknowledge after each byte of data received.

The I²C embedded in the L3G4200DH behaves like a slave device, and the following protocol must be adhered to. After the START (ST) condition, a slave address is sent. Once a slave acknowledge (SAK) has been returned, an 8-bit sub-address is transmitted. The 7 LSb represent the actual register address while the MSB enables address auto-increment. If the MSb of the SUB field is 1, the SUB (register address) is automatically incremented to allow multiple data read/write.

The slave address is completed with a read/write bit. If the bit is '1' (read), a REPEATED START (SR) condition must be issued after the two sub-address bytes; if the bit is '0' (write) the master transmits to the slave with the direction unchanged. *Table 13* describes how the SAD+read/write bit pattern is composed, listing all the possible configurations.

**Table 13. SAD+read/write patterns**

| Command | SAD[6:1] | SAD[0] = SDO | R/W | SAD+R/W |
|---|---|---|---|---|
| Read | 110100 | 0 | 1 | 11010001 (D1h) |
| Write | 110100 | 0 | 0 | 11010000 (D0h) |
| Read | 110100 | 1 | 1 | 11010011 (D3h) |
| Write | 110100 | 1 | 0 | 11010010 (D2h) |

**Table 14. Transfer when master is writing one byte to slave**

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Master | ST | SAD + W | | SUB | | DATA | | SP |
| Slave | | | SAK | | SAK | | SAK | |

**Table 15. Transfer when master is writing multiple bytes to slave**

| | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Master | ST | SAD + W | | SUB | | DATA | | DATA | | SP |
| Slave | | | SAK | | SAK | | SAK | | SAK | |

**Table 16. Transfer when master is receiving (reading) one byte of data from slave**

| | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Master | ST | SAD + W | | SUB | | SR | SAD + R | | | NMAK | SP |
| Slave | | | SAK | | SAK | | | SAK | DATA | | |

**Table 17. Transfer when master is receiving (reading) multiple bytes of data from slave**

| | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Master | ST | SAD+W | | SUB | | SR | SAD+R | | | MAK | | MAK | | NMAK | SP |
| Slave | | | SAK | | SAK | | | SAK | DATA | | DATA | | DATA | | |

Data are transmitted in byte format (DATA). Each data transfer contains 8 bits. The number of bytes transferred per transfer is unlimited. Data is transferred with the most significant bit (MSb) first. If a receiver cannot receive another complete byte of data until it has performed some other function, it can hold the clock line SCL LOW to force the transmitter into a wait state. Data transfer only continues when the receiver is ready for another byte and releases the data line. If a slave receiver does not acknowledge the slave address (i.e., it is not able to receive because it is performing some real-time function) the data line must be left HIGH by the slave. The master can then abort the transfer. A LOW to HIGH transition on the SDA line while the SCL line is HIGH is defined as a STOP condition. Each data transfer must be terminated by the generation of a STOP (SP) condition.

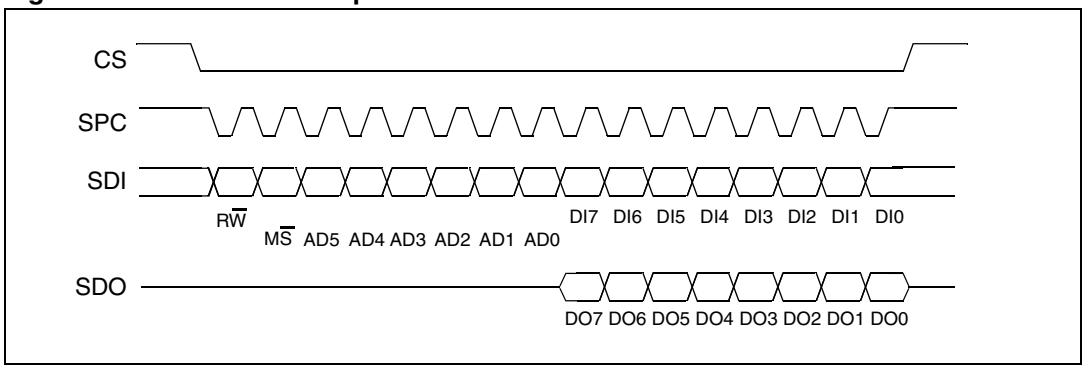
In order to read multiple bytes, it is necessary to assert the most significant bit of the sub-address field. In other words, SUB(7) must be equal to 1, while SUB(6-0) represents the address of the first register to be read.

In the presented communication format, MAK is “master acknowledge” and NMAK is “no master acknowledge”.

## 5.2 SPI bus interface

The SPI is a bus slave. The SPI allows writing and reading of the device registers. The serial interface interacts with the external world through 4 wires: **CS, SPC, SDI, and SDO**.

**Figure 13. Read and write protocol**




**CS** is the serial port enable and is controlled by the SPI master. It goes low at the start of the transmission and returns to high at the end. **SPC** is the serial port clock and is controlled by the SPI master. It is stopped high when **CS** is high (no transmission). **SDI** and **SDO** are, respectively, the serial port data input and output. These lines are driven at the falling edge of **SPC** and should be captured at the rising edge of **SPC**.

Both the read register and write register commands are completed in 16 clock pulses, or in multiples of 8 in case of multiple read/write bytes. Bit duration is the time between two falling edges of **SPC**. The first bit (bit 0) starts at the first falling edge of **SPC** after the falling edge of **CS** while the last bit (bit 15, bit 23, etc.) starts at the last falling edge of **SPC** just before the rising edge of **CS**.

***Bit 0***: R$\overline{W}$ bit. When 0, the data DI(7:0) is written to the device. When 1, the data DO(7:0) from the device is read. In the latter case, the chip drives **SDO** at the start of bit 8.

***Bit 1***: M$\overline{S}$ bit. When 0, the address remains unchanged in multiple read/write commands. When 1, the address is auto-incremented in multiple read/write commands.

***Bit 2-7***: address AD(5:0). This is the address field of the indexed register.

***Bit 8-15***: data DI(7:0) (write mode). This is the data that is written to the device (MSb first).

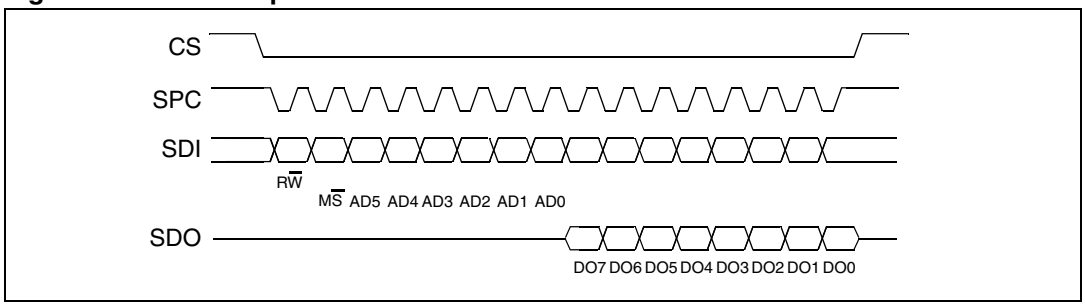
***Bit 8-15***: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

In multiple read/write commands, further blocks of 8 clock periods are added. When the M$\overline{S}$ bit is 0, the address used to read/write data remains the same for every block. When the M$\overline{S}$ bit is 1, the address used to read/write data is incremented at every block.

The function and the behavior of **SDI** and **SDO** remain unchanged.

### 5.2.1 SPI read

**Figure 14. SPI read protocol**



The SPI read command is performed with 16 clock pulses. A multiple byte read command is performed by adding blocks of 8 clock pulses to the previous one.

***Bit 0***: READ bit. The value is 1.

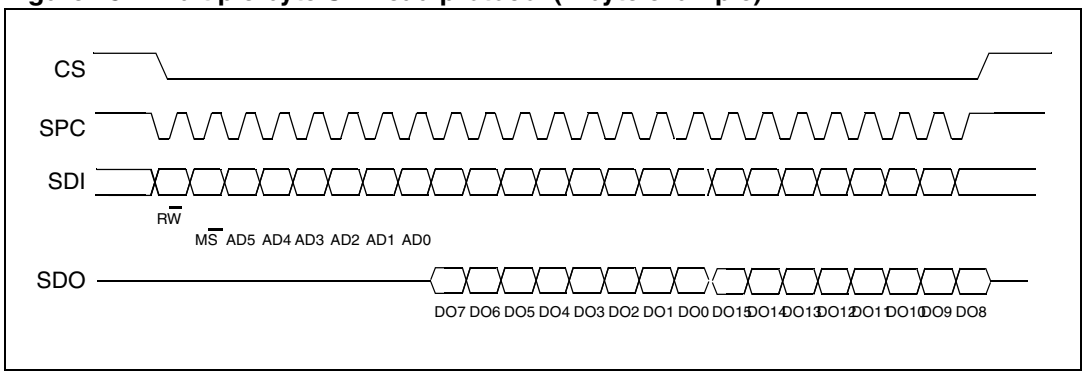
***Bit 1***: MS bit. When 0, do not increment address; when 1, increment address in multiple reading.

***Bit 2-7***: address AD(5:0). This is the address field of the indexed register.

***Bit 8-15***: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

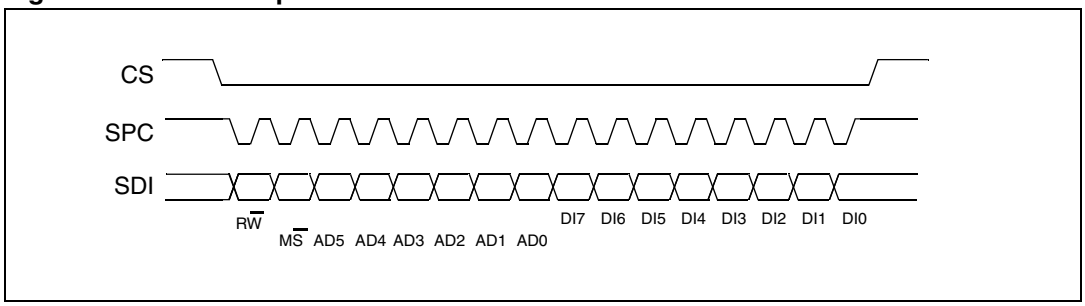
***Bit 16-...*** : data DO(...-8). Further data in multiple byte reading.

**Figure 15. Multiple byte SPI read protocol (2-byte example)**




## 5.2.2 SPI write

**Figure 16. SPI write protocol**




The SPI write command is performed with 16 clock pulses. A multiple byte write command is performed by adding blocks of 8 clock pulses to the previous one.

***Bit 0***: WRITE bit. The value is 0.

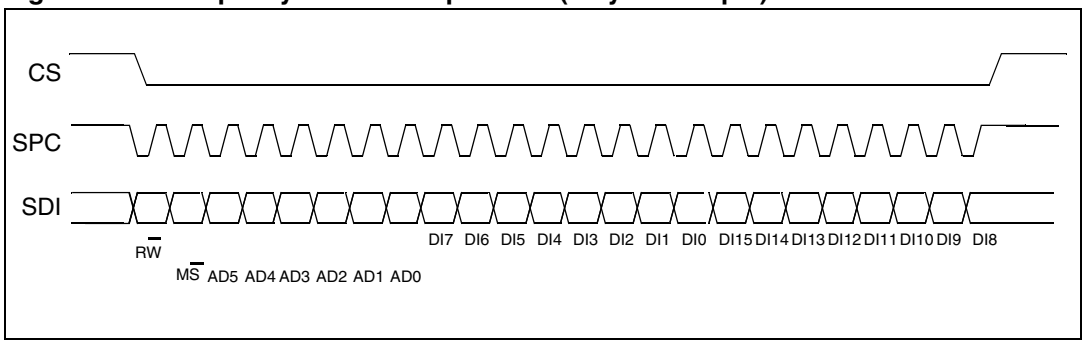
***Bit 1***: MS bit. When 0, do not increment address; when 1, increment address in multiple writing.

***Bit 2 -7***: address AD(5:0). This is the address field of the indexed register.

***Bit 8-15***: data DI(7:0) (write mode). This is the data that is written to the device (MSb first).

***Bit 16-...*** : data DI(...-8). Further data in multiple byte writing.

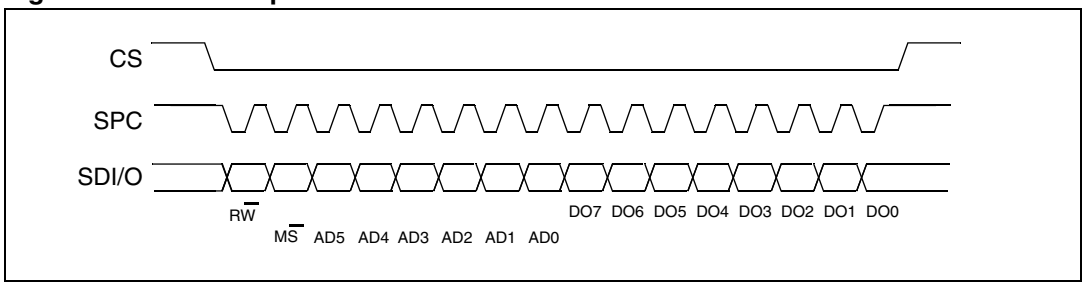
**Figure 17. Multiple byte SPI write protocol (2-byte example)**




### 5.2.3 SPI read in 3-wire mode

3-wire mode is entered by setting the SIM (SPI serial interface mode selection) bit to 1 in CTRL_REG2.

**Figure 18. SPI read protocol in 3-wire mode**




The SPI read command is performed with 16 clock pulses:

***Bit 0***: READ bit. The value is 1.

***Bit 1***: MS bit. When 0, do not increment address; when 1, increment address in multiple reading.

***Bit 2-7***: address AD(5:0). This is the address field of the indexed register.

***Bit 8-15***: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

The multiple read command is also available in 3-wire mode.

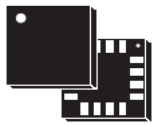
# 6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at www.st.com. ECOPACK is an ST trademark.

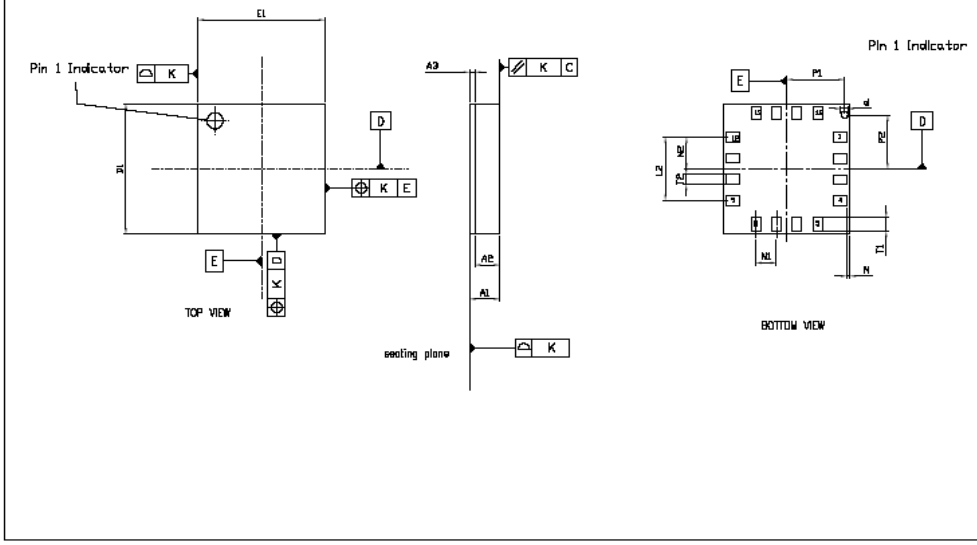
**Figure 19. LGA-16: mechanical data and package dimensions**

| Dimensions | | | |
|---|---|---|---|
| Ref. | mm | | |
| | Min. | Typ. | Max. |
| A1 | | | 1.100 |
| A2 | | 0.855 | |
| A3 | | 0.200 | |
| d | | 0.300 | |
| D1 | 3.850 | 4.000 | 4.150 |
| E1 | 3.850 | 4.000 | 4.150 |
| L2 | | 1.950 | |
| M | | 0.100 | |
| N1 | | 0.650 | |
| N2 | | 0.975 | |
| P1 | | 1.750 | |
| P2 | | 1.525 | |
| T1 | | 0.400 | |
| T2 | | 0.300 | |
| k | | 0.050 | |

Outline and mechanical data



LGA 16L (4x4x1.1mm)
Land Grid Array Package



# 7 Revision history

Table 18. Document revision history

| Date | Revision | Changes |
|---|---|---|
| 01-Apr-2010 | 1 | Initial release. |
| 03-Sep-2010 | 2 | Complete datasheet review. |

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