PROJECT PROPOSAL

Title: Design of a Formally Verified Block MiniFloat Multiply-Accumulate Unit.

Proposer: William Nicholas Marais.

Supervisor: Professor Phillip Heng Wai Leong.

Background:
This thesis builds upon the concept of a MiniFloat Block representation to train Deep Neural Networks. The paper which was previously published under the University of Sydney banner, achieved floating-point accuracy while increasing computational density and faster training times using this new spectrum of MiniFloat representation.

Problem Statement:
Currently hardware is limited by the difficulty of computing floating-point numbers efficiently and using them in further arithmetic. This leads to further trouble when approximations are made, and accuracy is lost. Therefore, the efficient use and simplification of floating-point numbers in computers are important to the ongoing progress of miniaturisation of hardware, as currently such devices as GPU's are getting larger and consuming more power.

The purpose of this thesis is to bolster the recent development of the MiniFloat Block representation with the design of a formally verified multiply-accumulate unit which uses this representation.

Methodologies:

1. Research: The need to become familiar with these areas is critical.
    - Verilog.
    - MiniFloat Blocks.
    - Verification.

2. Coding: We will then move onto the implementation.
    - Design a Multiply-Accumulate Unit with MiniFloat Block representation.
    - Formally Verify the design.

3. Testing: Ensure that the design functions as intended.
    - Formulate test cases to ensure validity.
    - Analyse output and performance.

4. Documentation: Collate findings and present them.
    - Write up a thesis report.
    - Present findings.

Schedule:
Table 1 contains the planned dates for stages of the thesis.

Name	Start	Finish	Duration
Thesis Start	18/02/2024	15/03/2024	20 days
Topic Proposal	18/02/2024	1/03/2024	10 days
Project Proposal	29/02/2024	15/03/2024	11 days
Literature Review	29/02/2024	1/04/2024	22 days
Formal Verification	29/02/2024	8/03/2024	6 days
MiniFloat Blocks	7/03/2024	19/03/2024	8 days
Verilog	19/03/2024	1/04/2024	9 days
Preliminary Design	24/03/2024	31/05/2024	50 days
Research	24/03/2024	31/05/2024	50 days
Verilog	24/03/2024	26/04/2024	25 days
Verification	25/04/2024	31/05/2024	26 days
Detailed Design	30/05/2024	30/09/2024	87 days
Revision	30/05/2024	1/07/2024	22 days
Implementation	30/06/2024	29/07/2024	21 days
Verification	28/07/2024	26/08/2024	21 days
Verification	25/08/2024	30/09/2024	26 days
Analysis	29/09/2024	21/10/2024	16 days
Report	20/10/2024	15/11/2024	20 days

Table 1: Planned Thesis Stages

Thesis meetings and check-ins will be conducted every Tuesday at 9am. And further solo work will be performed primarily on Fridays and at any other points where necessary to stay on track. See Appendix for Gantt Chart breakdown.

Approvals:

14/03/2024	*Professor Phillip Heng Wai Leong*	
Date	*Supervisor name*	*Supervisor Signature*

Appendix:

Thesis Schedule Gantt chart