Design and Performance Analysis of Multiply-Accumulate (MAC) Unit

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***Abstract*—In recent years, Multiply-Accumulate (MAC) unit is developing for various high performance applications. MAC unit is a fundamental block in the computing devices, especially Digital Signal Processor (DSP). MAC unit performs multiplication and accumulation process. Basic MAC unit consists of multiplier, adder, and accumulator. In the existing MAC unit model, multiplier is designed using modified Radix-2 booth multiplier. In this paper, MAC unit model is designed by incorporating the various multipliers such as Array Multiplier, Ripple Carry Array Multiplier with Row Bypassing Technique, Wallace Tree Multiplier and DADDA Multiplier in the multiplier module and the performance of MAC unit models is analyzed in terms of area, delay and power. The performance analysis of MAC unit models is done by designing the models in Verilog HDL. Then, MAC unit models are simulated and synthesized in Xilinx ISE 13.2 for Virtex-6 family 40nm technology.**

***Index Terms*- Carry Save Adder (CSA), Booth Multiplier, Array Multiplier, Ripple Carry Array Multiplier with Row Bypass, Wallace Tree Multipiler, DADDA Mulitplier and Multiply-Accumulate (MAC) unit.**

I. INTRODUCTION

In Digital Communication, Digital Signal Processor (DSP) is an important block which performs several digital signal processing applications such as Convolution, Discrete Cosine Transform (DCT), Fourier Transform, and so on [1]. Every digital signal processor contains MAC unit. The MAC unit performs multiplication and accumulation processes repeatedly in order to perform continuous and complex operations in digital signal processing. MAC unit also contains clock and reset in order to control its operation. Many researchers have been focusing on the design of advance MAC unit architectures. Young-Ho Seo et.al [2] discussed about the parallel multiplier-accumulator unit based on radix-2 modified booth algorithm along with the modified carry save adder scheme. Yuyun Liao et.al [3] explained about a high performance low power 32 bit multiply accumulate unit with Wallace tree multiplier and compared with MAC unit using radix booth multiplier. Devika Jaina et.al [4] discussed about design of multiply accumulate unit using Vedic multiplication techniques. In this paper, the performance analysis of MAC unit is done by incorporating various multipliers such as Array Multiplier (AM), Modified Radix2 Booth Multiplier (MRBM), Ripple Carry Array Multiplier with Row Bypass Technique (RCAM RB), Wallace Tree Multiplier (WTM) and DADDA Multiplier (DM).

The rest of the paper is organized as follows: Section I deals with the introduction about MAC unit and its operation. In section II, the designs of various multipliers are discussed. The existing MAC unit model is discussed in Section III. Various proposed MAC unit models are discussed in Section IV. And section V deals with the simulation and synthesis results of MAC unit models. Conclusion and future work are drawn in Section VI.

II. MULTIPLIERS

A variety of multipliers are used to design MAC unit, which are described below.

A. Modified Radix-2 Booth Multiplier (MRBM)

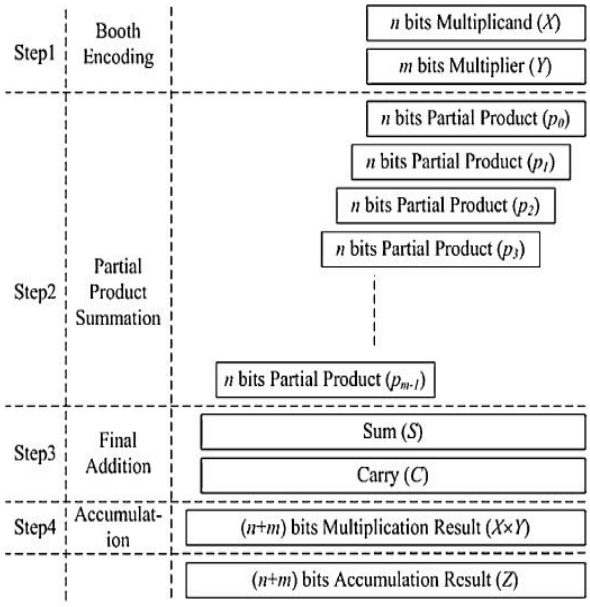

Fig.1. Modified Radix-2 Booth Multiplier (MRBM)

As shown in Fig 1, the modified Radix-2 booth multiplier consists of multiplicand and multiplier along with partial product generator and booth encoder. The partial products are generated by booth encoding technique. Hence, the number of partial products is reduced compared to that of conventional multiplier techniques. Finally, all partial products are added using Carry Save Adder [5, 6] and the result is accumulated in the Accumulator. Because of reduced number of partial products and additions, number of logic levels of the design decreases hence delay is reduced. However, the structure is increased due to complexity of the booth encoder.

B. Array Multiplier(AM)

Array Multiplier (AM) is one of the best conventional multiplier which consists of partial products generated by AND Logic [7]. All partial products are added by the Half Adder (HA) and Full Adder (FA) [8] depending on the number of input bits. Architecture of array multiplier is shown in Fig 2.

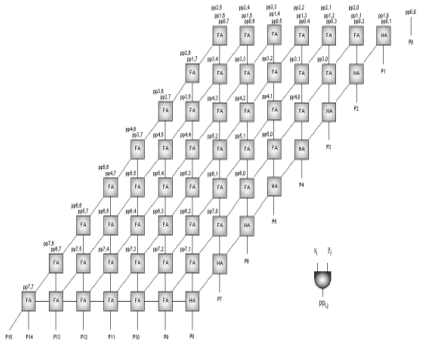

Fig.2. Array Multiplier (AM)

C. Ripple Carry Array Multiplier with Row Bypassing Technique (RCAM RB)

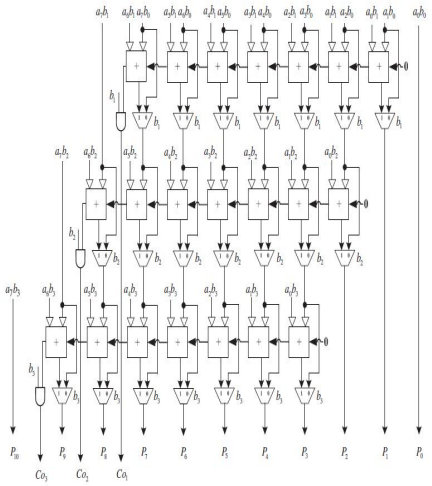

Fig.3.1. Structure of 8x4 Ripple Carry Array Multiplier with Row Bypass (RCAM RB)

In ripple carry array multiplier with row bypassing technique [9], the multiplication method is similar to the array multiplier. But the partial product stages are bypassed from previous state to next state depending upon the carry value obtained in adder stage. An 8x8 Multiplier requires two 8x4 RCM multipliers and the architecture [10] is shown in Fig 3.1 and Fig 3.2.

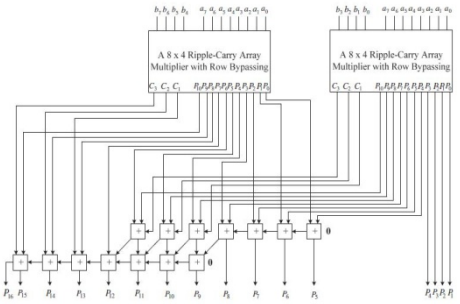

Fig 3.2.Structure of 8x8 Ripple Carry Array Multiplier with Row Bypass Technique (RCAM RB)

D. Wallace Tree Multiplier(WTM)

In Wallace tree multiplier, the Carry Save Addition (CSA) scheme is used to add partial products generated in each stage [11]. Hence, carry generated in present state saved and added in the next state. Hence the delay due to carry will be reduced in a greater extent. The design of Wallace tree multiplier is shown in Fig 4.

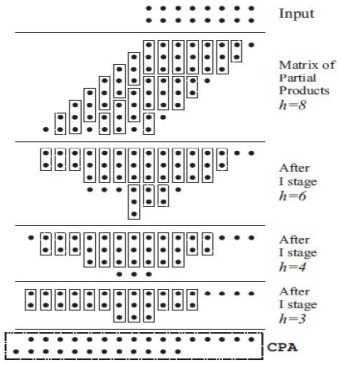

Fig.4. Wallace Tree Multiplier (WT)

E. DADDA Multiplier (DM)

DADDA multipliers are the refinement of parallel multipliers first presented by Wallace in 1964. In contrast to the Wallace reduction, DADDA multiplier performs the least reduction at each stage [11]. The maximum height of each stage is determined by working back from final stage which consists of two rows of partial products. The height of each stage should be in the order 2, 3, 4, 6, 9, 13, 19, 28, 42, 63 etc. An 8 bit DADDA multiplier reduction is shown in Fig 5.

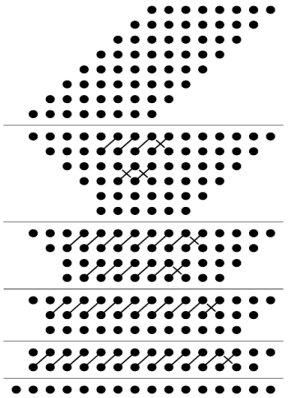

Fig.5. DADDA Multiplier

III. EXISTING MAC UNIT MODEL

The basic MAC unit contains multiplier, adder and accumulator [1]. The block diagram of basic MAC unit is given in Fig 6.

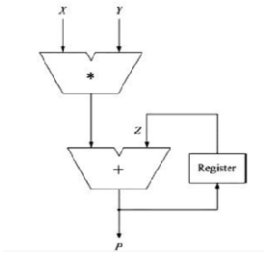

Fig.6. MAC unit Block Diagram

A typical n-bit MAC unit contains an n-bit multiplier, 2n-bit adder, and 2n-bit accumulator. Various MAC unit models can be developed by replacing the multiplier unit with various architectures.

In the existing MAC unit model, multiplier unit is replaced by modified Radix2 booth multiplier and adder by carry save adder. The internal hardware architecture of existing MAC unit model is given in Fig 7.

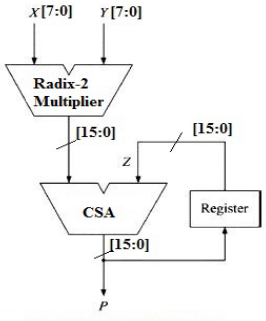

Fig.7. Existing MAC unit model (MRBM + CSA + Accumulator)

IV. PROPOSED MAC UNIT MODELS

A. *Proposed MAC Unit Model (1) (Array Multiplier + Carry Save Adder (CSA) + Accumulator)*

Proposed MAC unit model (1) contains Array Multiplier, and Carry Save Adder (CSA). The internal hardware of MAC unit model (2) is shown in Fig 8.1.

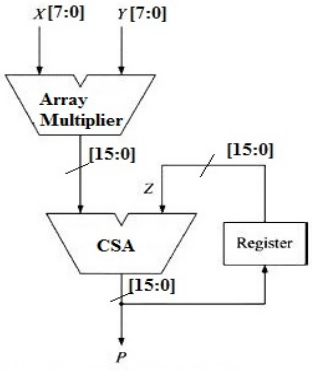

Fig.8.1. Proposed MAC unit model (1) (AM + CSA + Accumulator)

B. *Proposed MAC Unit Model (2)(Ripple Carry Multiplier + Carry Save Adder (CSA) + Accumulator)*

In the proposed MAC unit model (2), the multiplier is replaced with Ripple Carry Multiplier with Row Bypass technique and adder is replaced with Carry Save Adder Scheme (CSA) in order to reduce the delay in each stage of partial product addition.

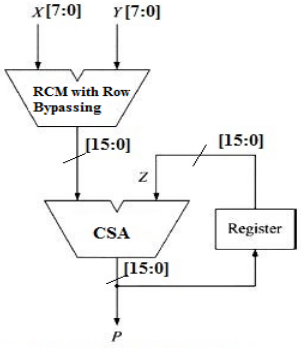

Fig.8.2. Proposed MAC unit model (2) (Ripple Carry Multiplier + Carry Save Adder (CSA) + Accumulator)

C. *Proposed MAC Unit Model (3) (Wallace Tree Multiplier + Carry Save Adder (CSA) + Accumulator)*

In the Proposed MAC unit model (3), the multiplier used is Wallace Tree Multiplier (WTM) and adder as Carry Save Adder (CSA).

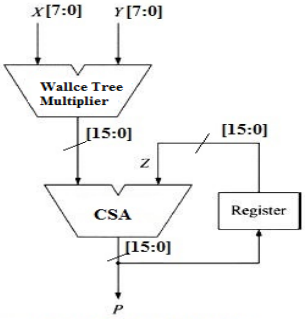

Fig.8.3. Proposed MAC unit model (3) (WT + CSA + Accumulator)

D. *Proposed MAC Unit Model (4) (DADDA Multiplier + Carry Save Adder + Accumulator)*

In the proposed MAC unit model (4), the multiplier used is DADDA Multiplier (DM) and adder is Carry Save Adder (CSA) scheme which is illustrated in Fig.8.4.

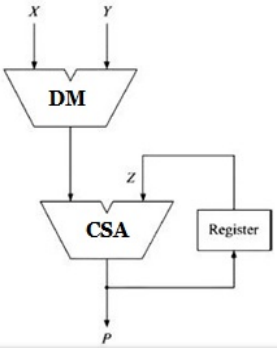

Fig.8.4. Proposed MAC unit model (4) (DM+CSA+Acc)

V. SIMULATION RESULTS

The existing and proposed MAC unit models are designed using Verilog HDL. Simulation and synthesis [12] are done using Xilinx ISE 13.2 for Virtex-6 family device with 40nm CMOS technology. In simulation results, Technology view [13] is a schematic representation of the design in terms of logic elements optimized to the target Xilinx device or technology in terms of Look Up Tables (LUTs) [14], carry logic, I/O buffers, and other technology-specific components.. RTL view is a schematic representation of the pre-optimized design in terms of generic symbols that are independent of the targeted Xilinx device in terms of adders, multipliers, counters, AND gates, and OR gates. Timing waveform [15] is generated by writing test bench program which contains the set of input test vectors applied to design.

A LUT (or Look Up-Table) is basically just a small memory. A 4-input, 1-output LUT, can generate any 4-input Boolean function (AND / OR / XOR / NOT / combinations of these / etc.). When FPGA has to be configured, it is required to configure the contents of the LUT, and thus the function that has to be implemented.

A. Simulation Results of Existing MAC Unit Model (Modified Radix2 Booth Multiplier (MRBM) + Carry Save Adder(CSA) + Accumulator)

The Technology view and RTL view of existing MAC unit model are given in Fig 9.1 and Fig 9.2.

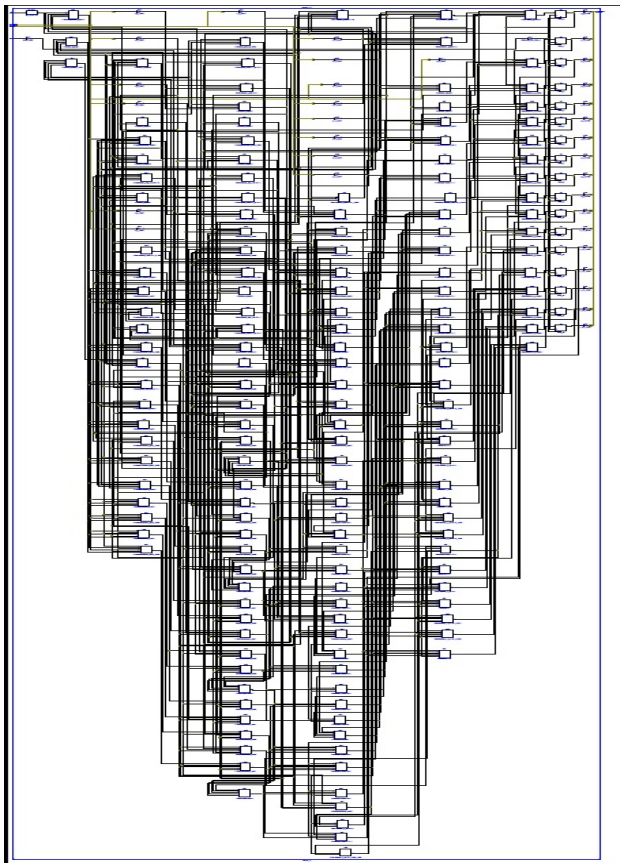

Fig.9.1. Technology View of Existing MAC Unit Model (MRBM+CSA+Accumulator)

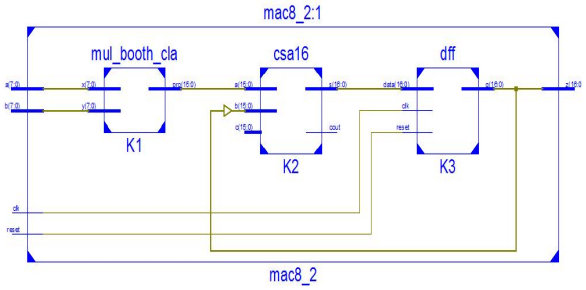

Fig 9.2.RTL View of Existing MAC Unit Model (MRBM+CSA+Accumulator)

B. Simulation Results of Proposed MAC Unit Model(1) (Array Multiplier (AM) +Carry Save Adder(CSA) + Accumulator)

Technology view and RTL view of proposed MAC unit model (1) are given in Fig 10.1 and Fig 10.2.

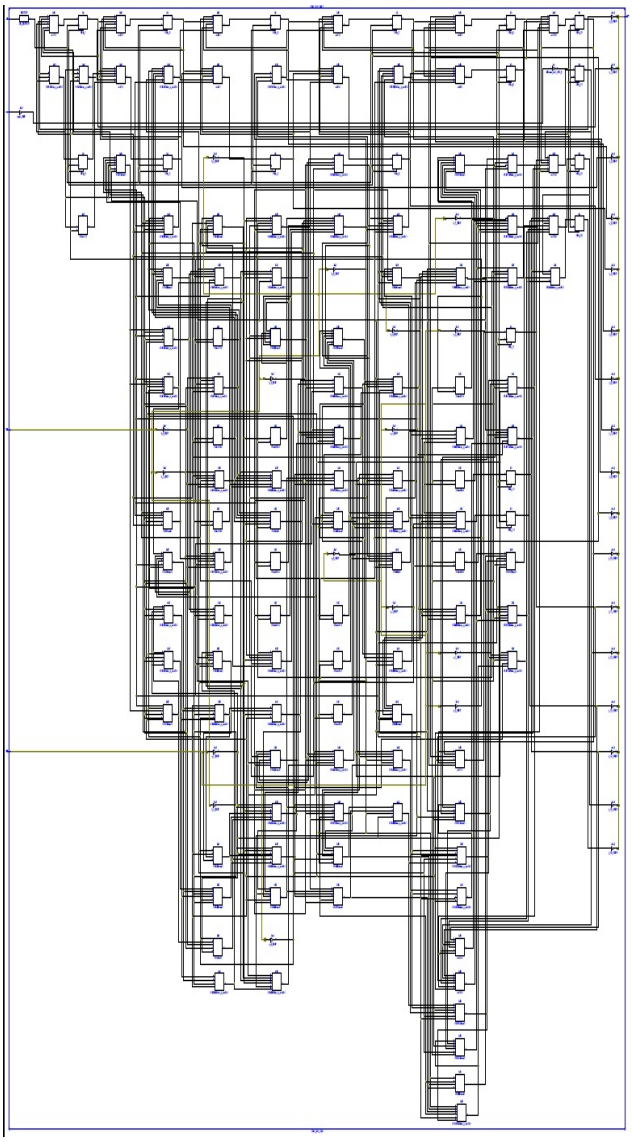

Fig.10.1. Technology View of MAC Proposed Model (1) (AM+CSA+Accumulator)

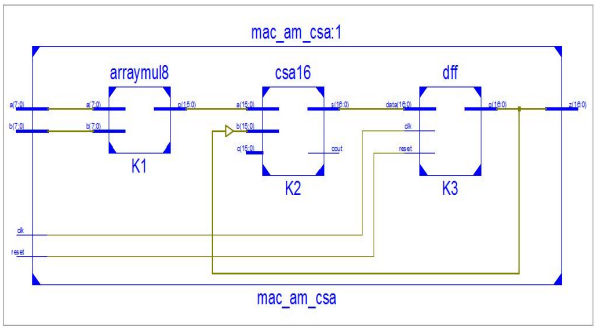

Fig.10.2. RTL View of MAC Proposed Model (1)
(AM+CSA+Accumulator)

C. Simulation Results of Proposed MAC Unit Model (2) (Ripple Carry Multiplier (RCAM RB) with Row bypass Technique + Carry Save Adder (CSA) + Accumulator)

Technology view of proposed MAC unit model (2) is given in Fig 11.1.

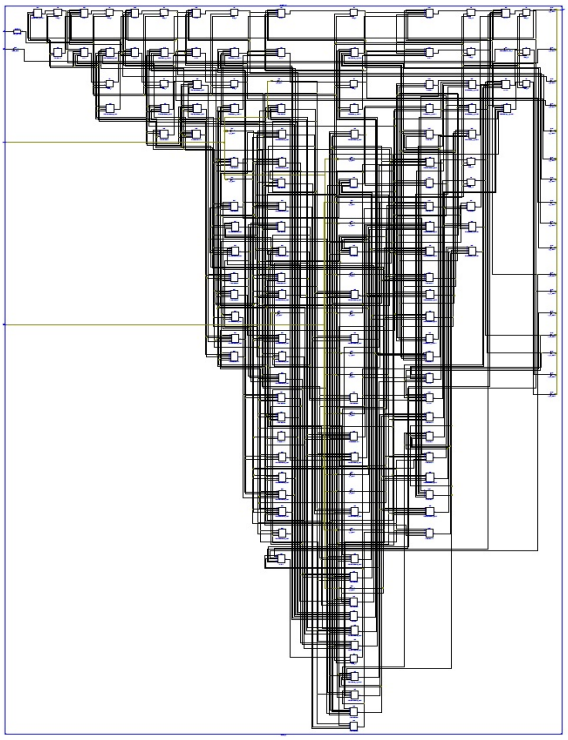

Fig.11.1. Technology View of Proposed MAC Unit Model (2)

(RCAM RB+CSA+Accumulator)

RTL view of proposed MAC unit model (2) shown in Fig 11.2.

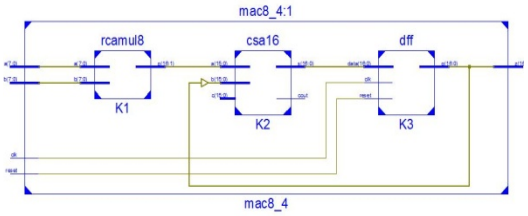

Fig.11.2. RTL View of Proposed MAC Unit Model (2) (RCAM RB+CSA+Accumulator)

D. Simulation Results of Proposed MAC Unit Model(3) (Wallace Tree Multiplier (WTM), Carry Save Adder (CSA) + Accumulator)

Technology view of proposed MAC unit model (3) is given in Fig 12.1.

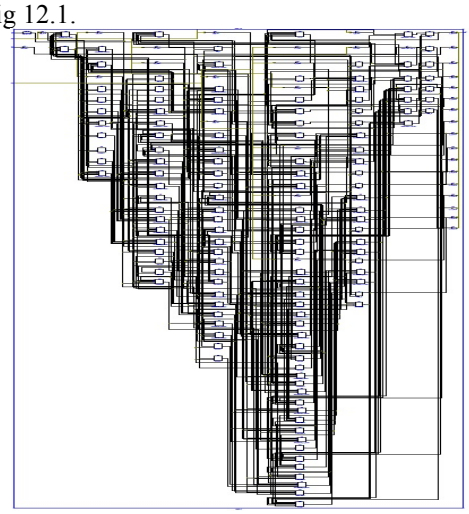

Fig.12.1. Technology View of Proposed MAC Unit Model (3)
(WTM+CSA+Accumulator)

RTL view of proposed MAC unit model (3) is shown in Fig 12.2.

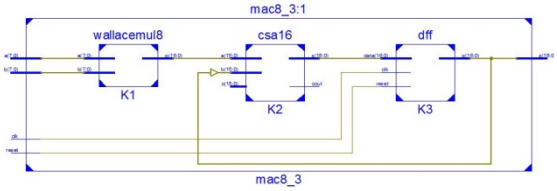

Fig.12.2. RTL view of proposed MAC unit model (3)
(WTM+CSA+Accumulator)

E. Simulation Results of Proposed MAC Unit Model(4) (Dadda Multiplier (DM), Carry Save Adder (CSA) + Accumulator)

Technology view of proposed MAC unit model (3) is given in Fig 13.1.

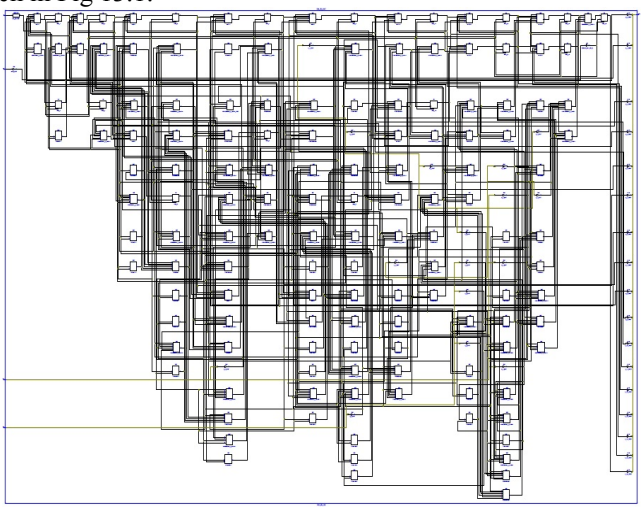

Fig.13.1. Technology View of Proposed MAC unit model (3)
(DM+ CSA + Acc)

RTL view of proposed MAC unit model (3) is shown in Fig 13.2.

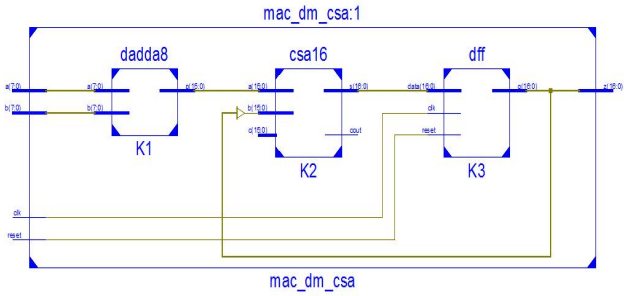

Fig.13.2. RTL View of Proposed MAC unit model (4) (DM+CSA+Acc)

F. Timing Waveform of MAC Unit Models

For various set of input vectors, the timing waveform generated with the accumulated outputs controlled by the clock and reset is shown in Fig 14.

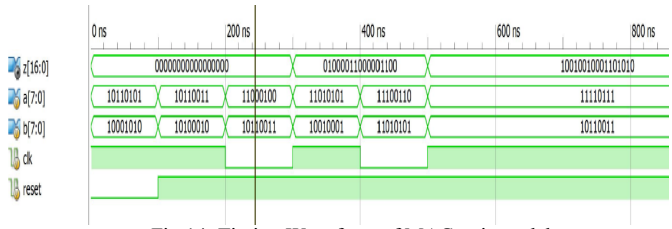

Fig.14. Timing Waveform of MAC unit models

G. Performance comparison of various MAC unit models

Performance comparison of various MAC unit models is given in Table 2.

TABLE I. COMPARISON OF PERFORMANCE METRICS OF MAC UNIT MODELS

S.No.	Design	Area (LUT's)	Delay (ns)	Power (W)
1.	Existing MAC Unit Model (MRBM+ CSA+Acc)	137	6.712	1.010
2.	Proposed MAC Unit Model (1) (AM+CSA+Acc)	97	8.175	1.067
3.	Proposed MAC Unit Model (2) (RCAM RB+CSA+Acc)	92	6.712	1.261
4.	Proposed MAC Model (3) (WTM+CSA +Acc)	96	6.102	1.061
5.	Proposed MAC Unit Model (4) (DM+CSA+Acc)	103	3.6592	2.142

It is observed that, the proposed MAC unit model (4) has optimized performance in terms of area, delay and power compared to that of existing MAC unit model and proposed MAC unit models (1), (2) and (3). However, in the proposed MAC model (4), power is increased to a small extent compared to that of existing MAC unit model.

VI. CONCLUSION AND FUTURE WORK

Various MAC unit models are designed using Verilog HDL, simulated and synthesized using Xilinx ISE 13.2 for Virtex-6 40nm technology. It is observed that, the existing MAC unit model dissipates less power. However, it occupies more area and delay. Proposed MAC unit model (4) achieves better performance in terms of area and delay compared to that of existing model. However, there is a slight increase in the power. In future work, it is required to design MAC unit architecture with low area, delay and power in order to meet the needs of current VLSI Industry. Further, this work can be extended by designing of MAC unit with higher number of bit sizes such as 16, 32 and 64 and also for designing applications like ALU, filters etc.

REFERENCES

[1] Tung Thanh Hoang, Magnus Själander, and Per Larsson-Edefors, "A High-Speed, Energy-Efficient Two-Cycle Multiply-Accumulate (MAC) Architecture and Its Application to a Double-Throughput MAC Unit", IEEE Transactions on Circuits and Systems-I: Regular Papers, vol. 57, no. 12, pp.3073-3081, Dec 2010.

[2] Young-Ho Seo, Dong-Wook Kim, "A New VLSI Architecture of Parallel Multiplier-Accumulate Based on Radix-2 Modified Booth Alogirithm", IEEE Transactions on VLSI Systems, vol.18, no.2, pp.201-207, Feb 2010.

[3] Yuyun Liao and David B. Roberts, "A High-Performance and Low-Power 32-bit Multiply-Accumulate Unit with Single-Instruction-Multiple-Data (SIMD) Feature", IEEE Journal of Solid State Circuits, vol.37, no.7, pp.926-931, July 2002.

[4] Devika Jaina, Kabiraj Sethi and Rutuparna Panda, "Vedic Mathematics based Multiply Accumulate Unit", Proceedings of International Conference on Computational Intelligence and Communication Systems, Gwalior, DOI 10.1109/CICN.2011.167, pp.754-757, July 2011.

[5] P.Jagadeesh, S.Ravi, Dr.Kittur Harish Mallikarjun, "Design of High Performance 64-Bit MAC Unit", Proceedings of IEEE International Conference on Circuits, Power and Computing Technologies, Tamilnadu, pp.782-786, 2013.

[6] Dhiraj K.Pradhan, "Fault-Tolerant Carry-Save Adders", IEEE Transactions on Computers, vol.C-23., pp.1320-1322, December 1974.

[7] Kripa Mathew, S.Asha Latha, T.Ravi, E.Logashanmugam, "Design and Analysis of Array Multiplier using an Area Efficient Full Adder Cell in 32nm CMOS Technology", International Journal of Engineering and Science, vol.2, no.3, pp.8-16, Mar 2013.

[8] Ron S. Waters and Earl E. Swartzlander, Jr., "A Reduced Complexity Wall ace Multiplier Reduction, " IEEE Transactions On Computers, vol. 59, no. 8, pp.1134-1137, Aug 2010.

[9] Ko-Chi Kuo , Chi-Wen Chou, "Low Power and High Speed Multiplier Design with Row Bypassing and Parallel Architecture", Elsevier Journal of Microelectronics, no.41, pp.639-650, July 2010.

[10] Yogesh M. Motey, Tejaswini G. Panse, "Traditional and Truncation Schemes for Different Multipliers", International Journal of Electronics and Computer Science Engineering, vol.2, no.2, pp.627-633, May 2013.

[11] Maroju SaiKumar, P.Samundiswary, "Design and Performance Analysis of Various Multipliers using Verilog HDL", CiiT International Journal of Programmable Device Circuits and Systems, vol.5, no.9, pp.391-398, Sep 2013.

[12] Xilinx13.4, "Synthesis and Simulation Design Guide", UG626 (v13.4) January 19, 2012.

[13] Xilinx 13.1, "RTL and Technology Schematic Viewers Tutorial", UG685 (v13.1), March 1, 2011.

[14] Xilinx, "7 Series FPGAs Configurable Logic Block", UG 474 (v 1.5), August 6, 2013.

[15] Xilinx 12.4, "ISim User Guide", UG660 (v 12.4), December 14, 2010.