

## CMPE 413/CMPE 640

### UMBC

## Sharing library for the project

To share a directory with cadence library files with your partner, you need to do the following (It might be best to do this during a lab session)

1. Launch virtuoso and create a new library named **finalproj** and attach it with the **gpdk045** library from the CIW window.

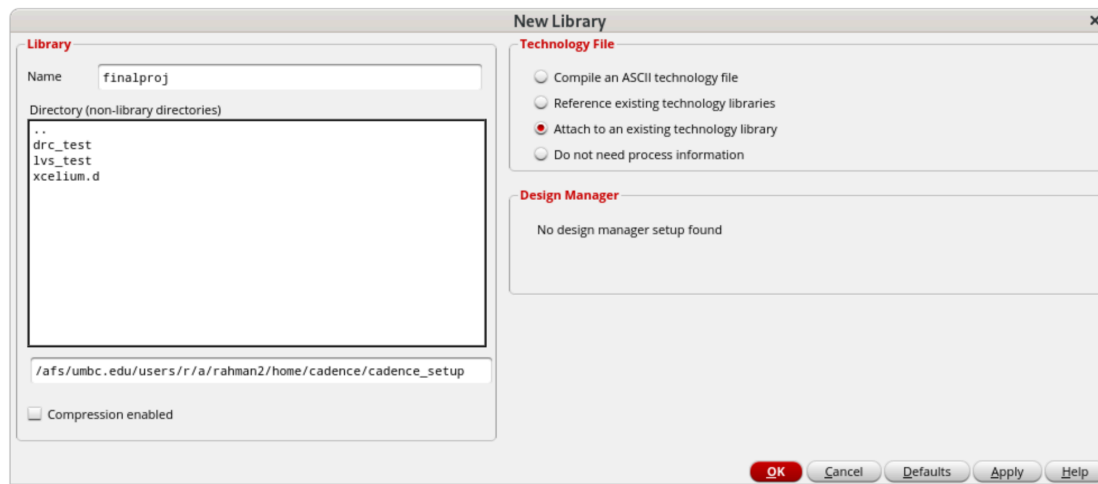


Figure 1: Creating a new library for the final project.

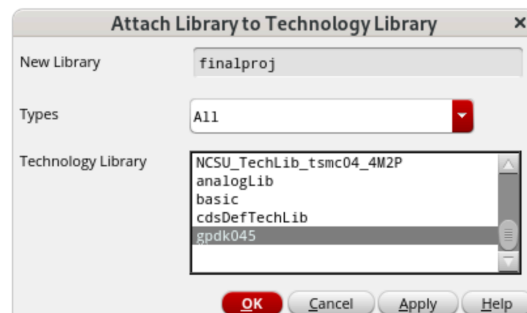


Figure 2: Attaching the new library with the 45 nm PDK.

2. Navigate to the newly created library using the following command.

```
cd ~/cadence/finalproj
```

**N.B:** Your cadence directory may vary from the example, so make sure to provide the correct path for your library. It should be in the same directory where you've launched virtuoso from.

## CMPE 413/CMPE 640

### UMBC

The first member is referred as the admin (A) and the other as (B). Let (A)'s username = aaaa1@umbc.edu. Let (B)'s username = bbbb1@umbc.edu.

The following commands need to be executed in gl.umbc.edu by (A):

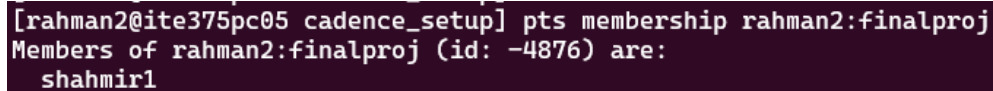
```
cd ~/cadence/finalproj

pts creategroup aaaa1:finalproj

pts adduser -user bbbb1 -group aaaa1:finalproj

pts membership aaaa1:finalproj
```

The members should be listed as the following figure.



```
[rahman2@ite375pc05 cadence_setup] pts membership rahman2:finalproj
Members of rahman2:finalproj (id: -4876) are:
shahmir1
```

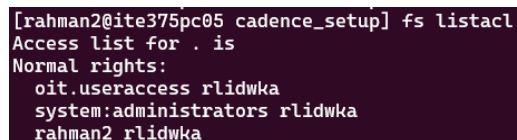
Figure 3: Members of your shared directory.

```
fs setacl ~/ aaaa1:finalproj l

fs setacl ~/cadence aaaa1:finalproj l

fs setacl ~/cadence/finalproj aaaa1:finalproj rldwkw

fs listacl
```



```
[rahman2@ite375pc05 cadence_setup] fs listacl
Access list for . is
Normal rights:
oit.useraccess rldwkw
system:administrators rldwkw
rahman2 rldwkw
```

Figure 4: Access rights of your shared directory.

3. At this point, (B) should be able to access the ~/cadence/finalproj directory fully. (B) can also list (ls) any files in (A)'s home directory and cadence directory. This should not be a security concern but (A) needs to keep in mind that (B) can see his/her directory structure. Then (B) will have to perform the following steps to see the finalproj library in his/her Library Manager:
  - Launch virtuoso
  - From the CIW window , navigate to **Tools > Library Path Editor**
  - Add a new library by entering a new row with Library as **finalproj**
  - Set the path as **/afs/umbc.edu/users/a/a/aaaa1/home/cadence/finalproj** according to figure 5.

# CMPE 413/CMPE 640

## UMBC

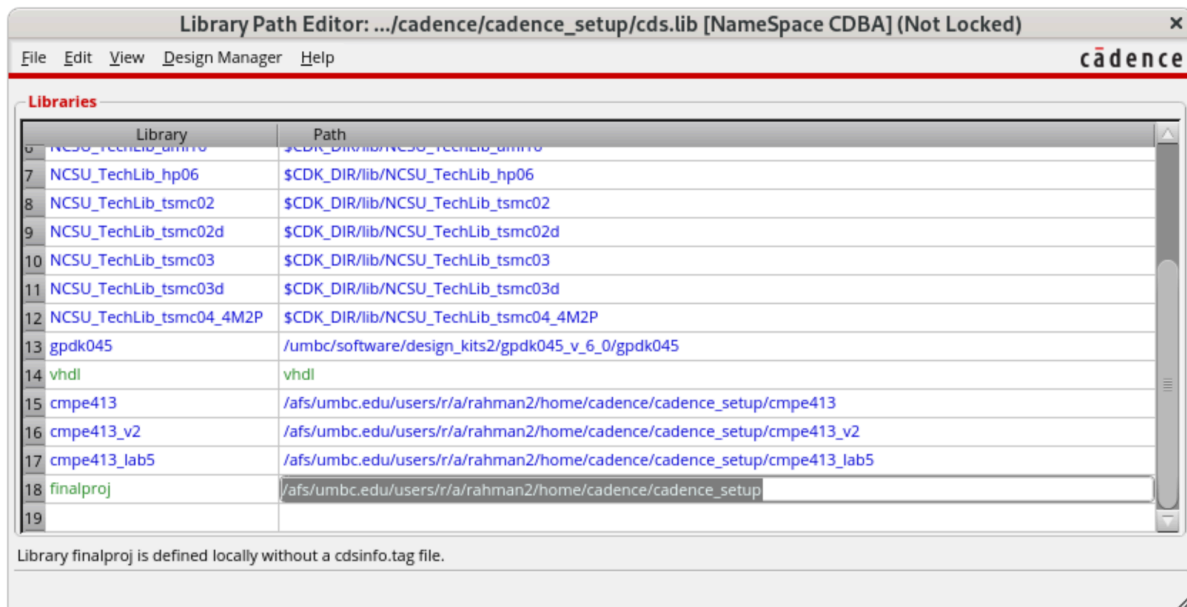


Figure 5: Changing the path for the new library (Should be performed by B).

- After providing the correct library path, another window resembling figure 4 will appear. Click **No**, since this library is already linked to the desired PDK by your group member (A). You don't need to create a new library, only update the library's directory.

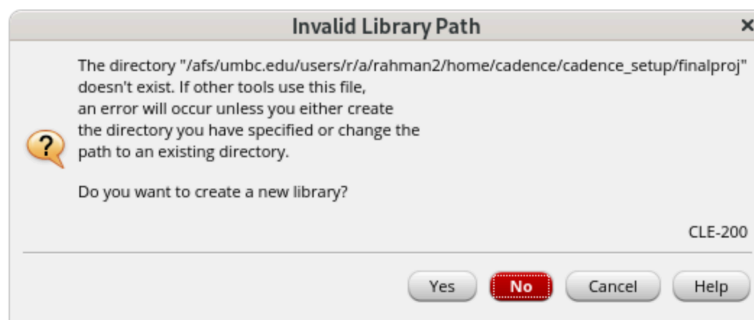


Figure 6: Skipping creation of a new library (Should be performed by B).

- Save and close the Path Editor using **File > Save**.
- Then goto the Library Manager Window and hit **View > Refresh**. This should allow both partners to work on the library.

## CMPE 413/CMPE 640 UMBC

### Removing access from the library

In order to remove access from the group use **(only use after the project is complete)**

```
fs setacl ~/aaaa1:finalproj none
```

```
fs setacl ~/cadence aaaa1:finalproj none
```

```
fs setacl ~/cadence/finalproj aaaa1:finalproj none
```

To delete the shared library, use

```
pts delete -nameorid aaaa1:finalproj
```

If you are interested in learning more then you can read the following:

- <https://itservices.stanford.edu/service/afs/learningmore/faq#5>
- <https://computing.cs.cmu.edu/help-support/afs-acls>

**PS: It is recommended to create a new library for the final project, and copy existing schematics and layouts into the new library.**

**Please do not copy config views, it will generate a lot of errors.**

Also note that, if you see any lock files on some of the schematics/layout, consult with the other partner if they are using the said schematics/layout. Both of you working on the same schematic/layout at the same time will cause a lot of confusion and lead to errors.