Regulating Pulse Width Modulators

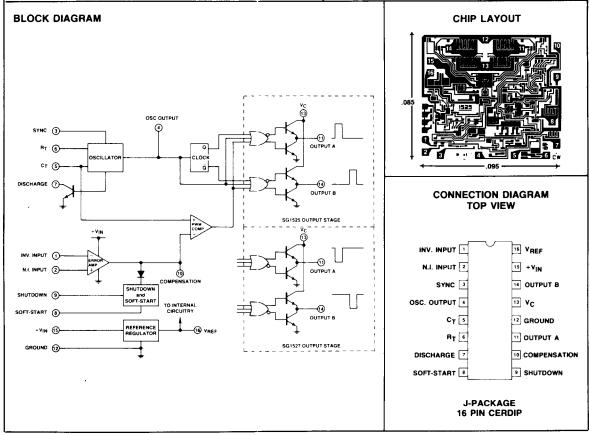
SG1525/SG2525/SG3525 SG1527/SG2527/SG3527

DESCRIPTION

The SG1525/1527 series of pulse width modulator integrated circuits are designed to offer improved performance and lowered external parts count when used to implement switching power supplies. The on-chip +5.1 volt reference is trimmed to $\pm 1\%$ initial accuracy and the common mode range of the error amplifier includes the reference voltage, eliminating external potentiometers and divider resistors. A Sync input to the oscillator allows multiple units to be slaved together, or a single unit to be synchronized to an external system clock. A single resistor between the CT pin and the Discharge pin provides a wide range of deadtime adjustment. These devices also feature internal clamp diodes and current sources for soft-start. A timing capacitor is the only external component required. A Shutdown pin controls the soft-start circuitry, allowing external monitoring devices to initiate soft-start cycles. The output stages are totem-pole designs capable of sourcing or sinking 100 mA. The SG1525 output stage features NOR logic, giving a normally LOW output level. The SG1527 utilizes OR logic, which results in a normally HIGH output level.

FEATURES

- 8 to 35 volt operation
- 5.1 volt reference trimmed to ± 1%
- 100 Hz to 400 kHz oscillator range
- Oscillator Sync terminal
- Adjustable deadtime
- · internal soft-start
- Error amp input common mode includes reference
- Dual 100 mA source/sink output drivers
- Power FET drive capability



SG1525/SG2525/SG3525 SG1527/SG2527/SG3527

ABSOLUTE MAXIMUM RATINGS (Note 1)

Power Dissipation at $T_A = +25^{\circ}C$ (Note 2) Supply Voltage (+VIN) - 40V · 40V Thermal Resistance: junction to ambient Collector Supply Voltage (V_C) -0.3 / to +5.5 V Power Dissipation at $T_C = +25 ^{\circ}\text{C}$ (Note 3) Logic Inputs Thermal Resistance: junction to case -0. iV to +VIN Analog Inputs 200 mA Operating Junction Temperature Output Current, Source or Sink Storage Temperature Range 50 mA Reference Output Current 5 mA Lead Temperature (Soldering, 10 seconds) Oscillator Charging Current

Note 1. Values beyond which damage may occur.

Note 2. Derate at 10 mW/°C for ambient temperatures above +50 °C.

Note 3. Derate at 16 mW/°C for case temperatures above +25°C.

RECOMMENDED OPERATING CONDITIONS (Note 4)

Input Voltage (+VIN) Collector Supply Voltage (VC)

Sink/Source Load Current (each output) Reference Load Current 100 Hz to 400 kHz Oscillator Frequency Range Oscillator Timing Resistor

+1.V to +35V +4.5V to +35V C to 100 mA) to 20 mA

2k \S to 150k Ω

Deadtime Resistor Range Operating Ambient Temperature Range SG1525, SG1527

Oscillator Timing Capacitor

SG2525, SG2527 SG3525, SG3527 .001 μF to 0.1 μF 0 to 500 Ω

-55°C to +125°C -25°C to +85°C 0°C to +70°C

1000 mW

100°C/W

2000 mW

60°C/W

+150°C

+300°C

-65°C to +150°C

Note 4. Range over which the device is functional and parameter limits are guaranteed.

ELECTRICAL CHARACTERISTICS (+V_{IN} = 20V, and over operating temperature, unless otherwise specified)

PARAMETER	CONDITIONS	SG152	SG1525/2525/1527/2527			SG3525/3527		
		MIN	TYP	MAX	MIN	TYP	MAX	UNITS
REFERENCE SECTION (I	L = 1 mA)		4			•		
Output Voltage	T _j = 25°C	5.05	5.10	5.15	5.00	5.10	5.20	٧
Line Regulation	V _{IN} = 8 to 35V		10	20		10	20	mV
Load Regulation	I _L = 0 to 20 mA		20	50	,	20	50	mV
Temperature Stability ⁵	Over Operating Range		20	50		20	50	mV
Total Output Variation	Line, Load, and Temp	5.00		5.20	4.95		5.25	٧
Short Circuit Current	VREF = 0, T _j = 25°C		80	100		80	100	mA
Output Noise Voltage ⁵	10 Hz \leq f \leq 10 kHz, T _j = 25°C		40	200		40	200	μVrms
Long Term Stability ⁵	T _j = 125°C		20	50		20	50	mV/khr
OSCILLATOR SECTION (Note 6)							
Initial Accuracy ⁵	T _j = 25°C		±2	± 6		± 2	± 6	%
Voltage Stability ⁵	V _{IN} = 8 to 35V		± 0.3	± 1	-	± 1	± 2	%
Temperature Stability ⁵	Over Operating Range		± 3	± 6		± 3	± 5	%
Minimum Frequency	R_T = 150 k Ω , C_T = 0.1 μ F			100			100	Hz
Maximum Frequency	$R_T = 2 k\Omega$, $C_T = 1 nF$	400			400			kHz
Current Mirror	I _{RT} = 2 mA	1.8	2.0	2.2	1.8	2.0	2.2	mA
Clock Amplitude		3.0	3.5		3.0	3.5		٧
Clock Width ⁵	T _j = 25°C	0.3	0.5	2.0	0.3	0.5	2.0	μ sec
Sync Threshold			1.0	2.0		1.0	2.0	٧
Sync Input Current	Sync Voltage = 3.5V		0.2	0.4		0.2	0.4	mA

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PARAMETER	CONDITIONS	SG1525/2525/1527/2527			SG3525/3527			
		MIN	TYP	MAX	MIN	TYP	MAX	UNITS
ERROR AMPLIFIER SECTI	ION (V _{CM} = 5.2 Volts)	1	-					•
Input Offset Voltage			0.5	5		2	10	mV
Input Bias Current			1	10		1	10	μА
Input Offset Current				1			1	μА
DC Open Loop Gain	R _L ≥ 10 Meg Ω	60	75		60	75		dB
Gain-Bandwidth Product ⁵	$A_V = 0 \text{ dB}, T_j = 25^{\circ}\text{C}$	1	2		1	2		MHz
Output Low Level			0.2	0.5		0.2	0.5	v
Output High Level		3.8	5.6		3.8	5.6		V
Common Mode Rejection	V _{CM} = 1.5 to 5.2V	60	75		60	75		dB
Supply Voltage Rejection	V _{IN} = 8 to 35V	50	60		50	60		dB
P.W.M. COMPARATOR				<u> </u>				•
Minimum Duty Cycle				0			0	%
Maximum Duty Cycle		45	49		45	49		%
Input Threshold ⁶	Zero Duty Cycle	0.6	0.9		0.6	0.9		V
Input Threshold ⁶	Max Duty Cycle		3.3	3.5		3.3	3.5	V
Input Bias Current ⁵			.05	1.0		.05	1.0	μА
SOFT—START SECTION								
Soft Start Current	VSHUTDOWN = 0V	50	100	175	50	100	175	μА
Soft Start Voltage	VSHUTDOWN = 2V		0.2	0.4		0.2	0.4	V
Error Clamp Voltage	VSHUTDOWN = 2V		0.2	0.4		0.2	0.4	V
Input Current	VSHUTDOWN = 2V		1.6	3		1.6	3	mA
OUTPUT DRIVERS (Each C	Output) (V _C = 20 Volts)							
Output Low Level	I _{SINK} = 20 mA		0.2	0.4		0.2	0.4	V
	I _{SINK} = 100 mA		1.0	2.0		1.0	2.0	V
Output High Level	ISOURCE = 20 mA	18	19		18	19		V
	ISOURCE = 100 mA	17	18		17	18		V
Collector Leakage ⁷	V _C = 35V			100			100	μА
Rise Time ⁵	$C_L = 1 \text{ nF, } T_j = 25^{\circ}\text{C}$		100	600		100	600	nsec
Fall Time ⁵	C _L = 1 nF, T _j = 25°C		50	300		50	300	nsec
Shutdown Delay ⁵	$V_{SH} = 2V, C_S = 0, T_j = 25^{\circ}C$		0.5	1.5		0.5	1.5	μsec
TOTAL STANDBY CURREN								
Supply Current	VIN = 35V, VSHUTDOWN = 2V		14	20		14	20	mA

Note 5. These parameters, although guaranteed over the recommended operating conditions, are not 100% tested in production.

Note 6. Tested at fOSC = 40 kHz (RT = 3.6 k Ω , CT = .01 uF, RD = 0 Ω).

Note 7. Applies to SG1525/2525/3525 only, due to polarity of output pulses.

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CHARACTERISTIC CURVES

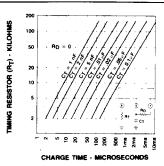


Figure 1. SG1525/1527 Oscillator Charge Time as a Function of R_{T} and C_{T} .

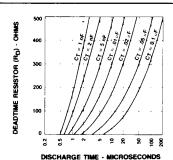


Figure 2. SG1525/1527 Oscillator Discharge Time as a Function of $R_{\mbox{\scriptsize D}}$ and $C_{\mbox{\scriptsize T}}$.

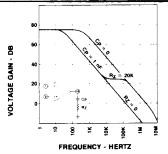


Figure 3. The error amplifier open-loop frequency response may be easily modified by shunt reactance to ground.

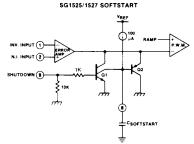


Figure 4. A soft-start cycle begins when the SHUTDOWN pin is low. Turn-on delay to 100% duty cycle is determined by the time required to charge Cg to +2.7 volts with 100 μ A.

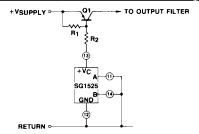


Figure 5. For single-ended supplies, the driver outputs are grounded. The V_C terminal is switched to ground by the totem-pole source transistors on alternate oscillator cycles.

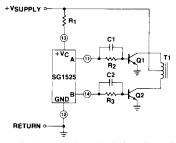


Figure 6. In conventional push-pull bipolar designs, forward base drive is controlled by R_1 - R_3 . Rapid turn-off times for the power devices are achieved with speed-up capacitors C_1 and C_2 .

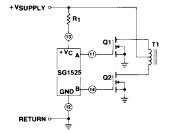


Figure 7. The low source impedance of the output drivers provides rapid charging of power FET input capacitance while minizing external components.

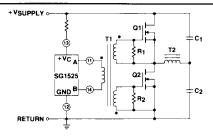


Figure 8. Low power transformers can be driven directly by the SG1525. Automatic flux reset to zero occurs during deadtime, when both ends of the primary winding are switched to ground.