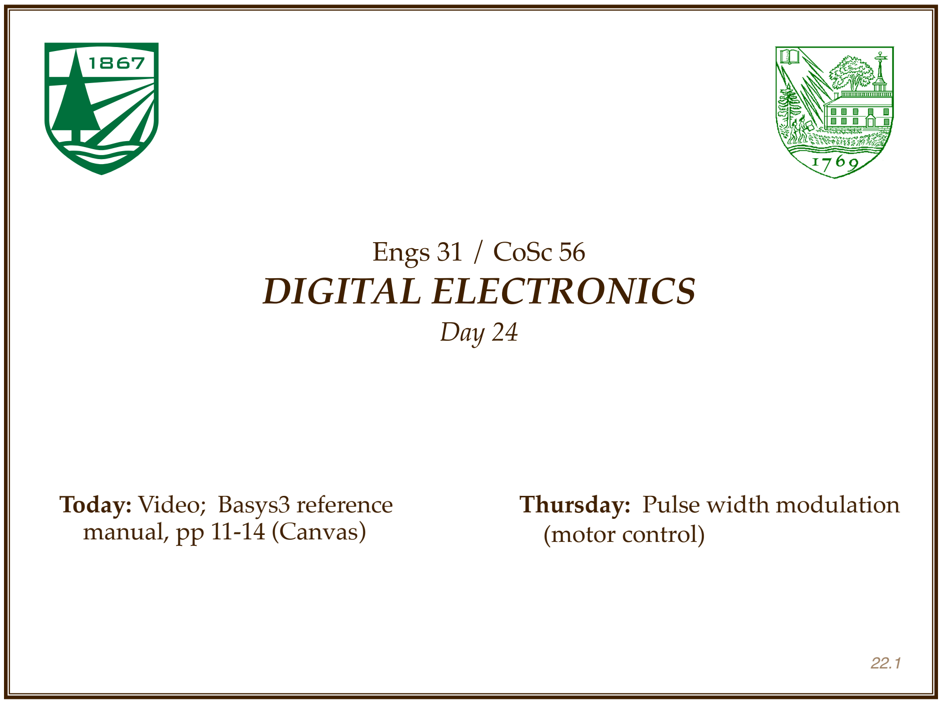


Engs 31 / CoSc 56

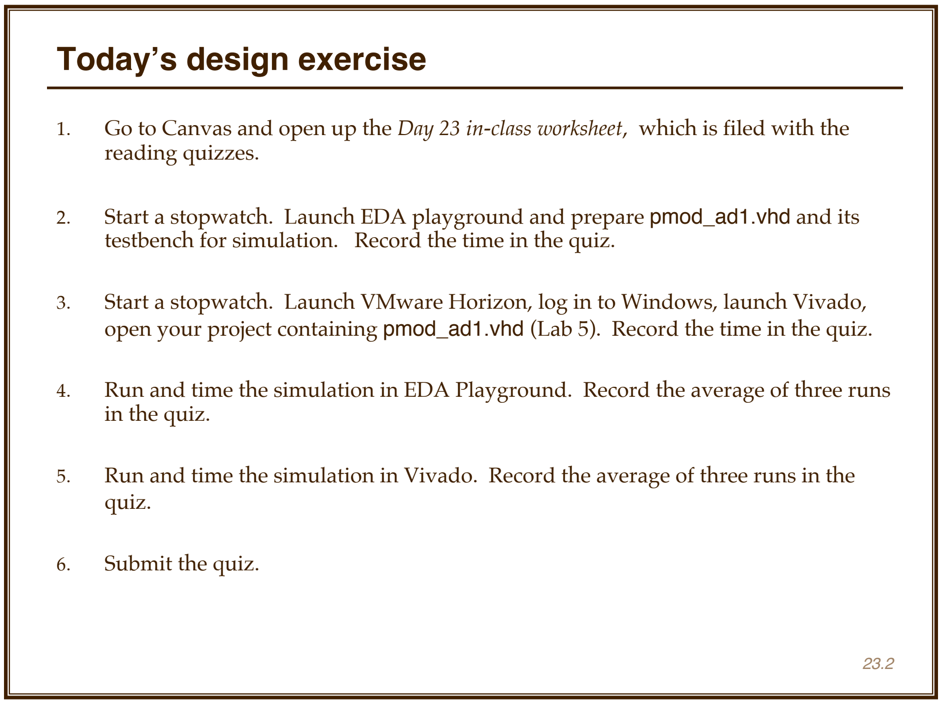
DIGITAL ELECTRONICS

Day 24

Today: Video; Basys3 reference manual, pp 11-14 (Canvas)

Thursday: Pulse width modulation (motor control)

22.1



Today's design exercise

1. Go to Canvas and open up the *Day 23 in-class worksheet*, which is filed with the reading quizzes.
2. Start a stopwatch. Launch EDA playground and prepare `pmod_ad1.vhd` and its testbench for simulation. Record the time in the quiz.
3. Start a stopwatch. Launch VMware Horizon, log in to Windows, launch Vivado, open your project containing `pmod_ad1.vhd` (Lab 5). Record the time in the quiz.
4. Run and time the simulation in EDA Playground. Record the average of three runs in the quiz.
5. Run and time the simulation in Vivado. Record the average of three runs in the quiz.
6. Submit the quiz.

23.2

Today's topic

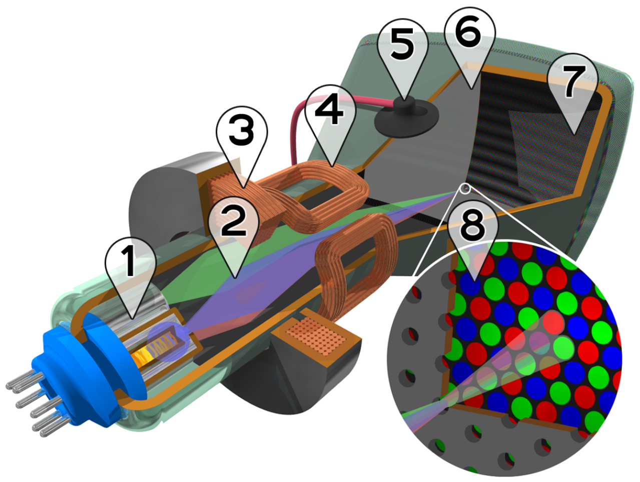
How to display graphical output on a VGA monitor.

23.3

"Ancient history": the CRT display

Ref: Wikipedia, "Cathode Ray Tube"

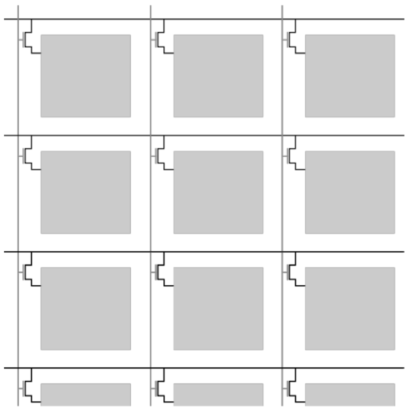
Electron beams activate a dot matrix of phosphors that glow red, green, or blue. Beams are swept across the screen by magnetic fields produced by deflection coils.



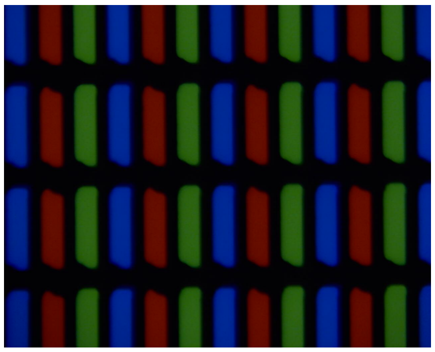
22.4

Current technology: Liquid crystal / LED display

Each pixel of the display is an individually addressed shutter or source.



Ref: Wikipedia, "TFT LCD"



Ref: Wikipedia, "LCD television"

22.5

Image formats

These are only a few of the many standards.

Format	Resolution (column × row)
VGA	640 × 480
SVGA	800 × 600
XGA	1024 × 768
UXGA	1600 × 1200
WUXGA	1920 × 1200
720p	1280 × 720
1080p / 1080i	1920 × 1080

In addition to resolution, formats differ in frame rate and whether lines are drawn **p**rogressively (consecutively) or **i**nterlaced (odd first, then even).

22.6

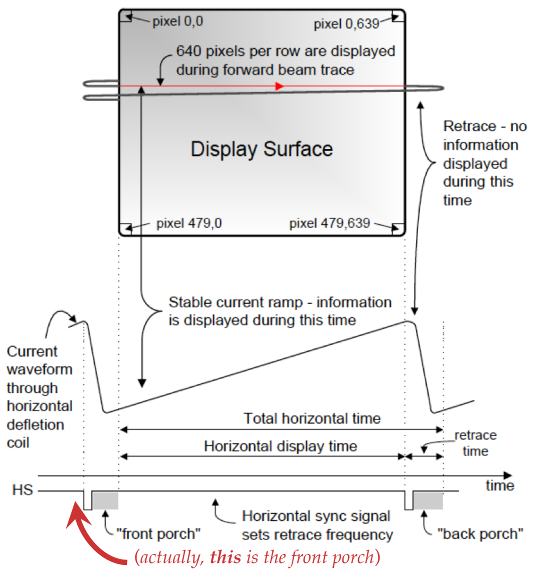
Video sweep & synchronization

Ref: Digilent

In a CRT, sync signals synchronize horizontal and vertical ramp waveforms that drive the deflection coils.

In a LCD;/LED display, sync signals synchronize counters that address pixels row-column.

Either way, RGB signals must be sent to the display in sync with the horizontal and vertical sync signals.


pixel 0,0
pixel 0,639
640 pixels per row are displayed during forward beam trace
Display Surface
Retrace - no information displayed during this time
pixel 479,0
pixel 479,639
Stable current ramp - information is displayed during this time
Current waveform through horizontal deflection coil
Total horizontal time
retrace time
Horizontal display time
HS
time
"front porch"
Horizontal sync signal sets retrace frequency
"back porch"
(actually, this is the front porch)

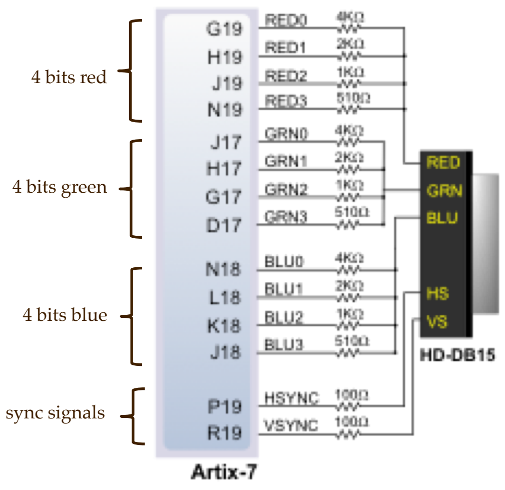
Example: VGA port on Basys3 board

Ref: Digilent, *Basys3 Reference Manual, p.11*

Logical voltage outputs from FPGA are weighted by resistors in ≈ 1:2:4:8 ratio (simple D/A conversion).

75 ohm resistors inside the VGA monitor create voltage dividers with the weight resistors, so that RGB signals range from 0 to 0.7 volts.

12 bits produce 4096 colors.

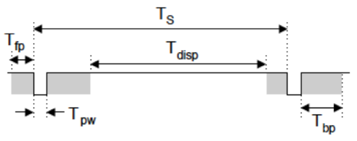


22.12

VGA sync pulse timing

Ref: Digilent, *Basys3 Board Reference Manual*

Times in “clocks” are relative to a 25 MHz clock (40 ns).



Symbol	Parameter	Vertical Sync			Horiz. Sync	
		Time	Clocks	Lines	Time	Clks
T_S	Sync pulse	16.7ms	416,800	521	32 us	800
T_{disp}	Display time	15.36ms	384,000	480	25.6 us	640
T_{pw}	Pulse width	64 us	1,600	2	3.84 us	96
T_{fp}	Front porch	320 us	8,000	10	640 ns	16
T_{bp}	Back porch	928 us	23,200	29	1.92 us	48

800 clks × 40 ns = 32 us

Figure 19: VGA system timings for 640x480 display

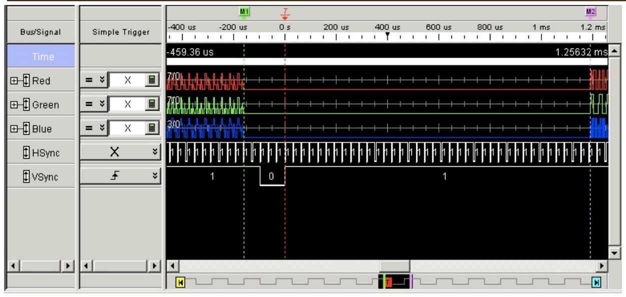
T_s isn’t really a sync pulse width, but a sync period (sync pulse to sync pulse).

The sync pulse and porch widths can vary a little, as long as T_s and T_{disp} are steady.

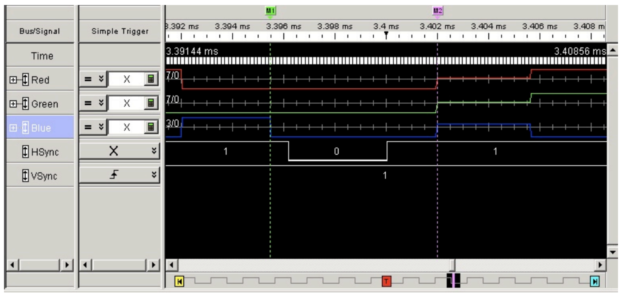
22.13

VGA sync pulse timing

Ref: Graham Keggi & Adam Marano



Vertical sync with blanking



Horizontal sync with blanking

22.14

VGA controller

Ref: P.P. Chu, *FPGA Prototyping by VHDL Examples*

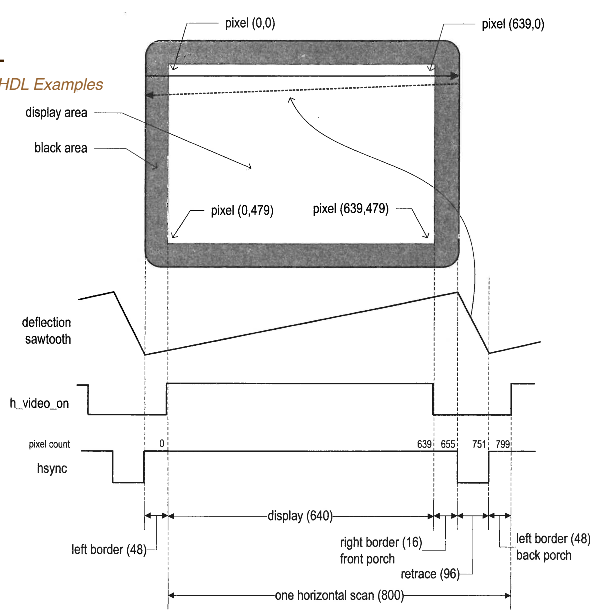


Figure 12.4 Timing diagram of a horizontal scan.

VGA controller

Ref: P.P. Chu, *FPGA Prototyping by VHDL Examples*

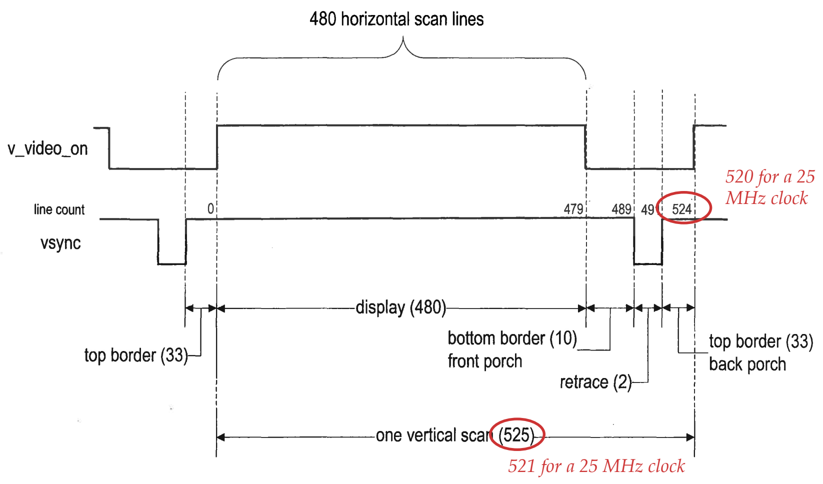
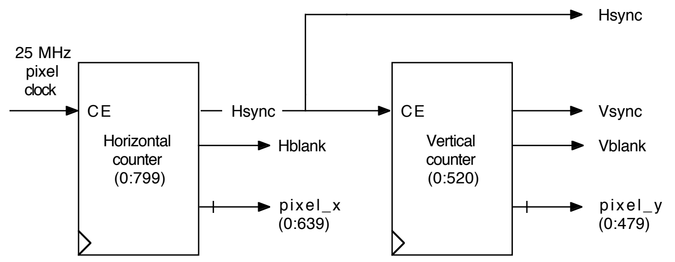


Figure 12.5 Timing diagram of a vertical scan.

22.16

VGA controller



Pixel rate for 640 × 480 is 25.175 MHz (close to 25 MHz) — small tweaks to the horizontal and vertical counters correct for the difference.

pixel_x and pixel_y are used to address frame buffer memory or to compute pixel values on the fly.

Hblank and Vblank are true when pixel_x and pixel_y are outside the active image area. Must use these to set pixels to zero on borders and during H and V syncs.

VGA controller

Ref: P.P. Chu, *FPGA Prototyping by VHDL Examples*

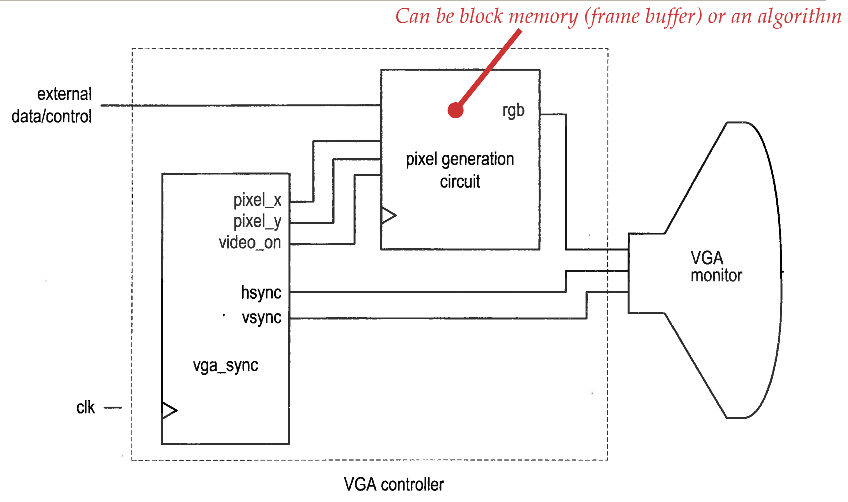


Figure 12.3 Simplified block diagram of a VGA controller.

Pixel generation

A 640 × 480 image has 307,200 pixels.
At 12 bits / pixel, this is 3,686,400 bits.
Our FPGA chip has 150 × 36K = 5,529,600 bits of BRAM.

In principle, you can hold an entire image in BRAM, if you address it efficiently.

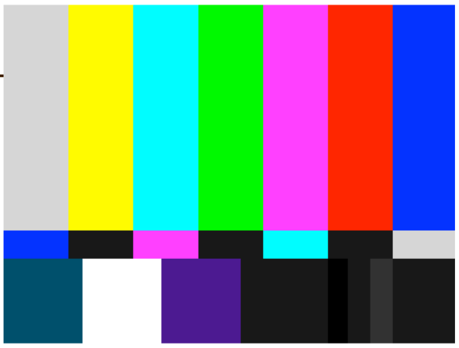
Easier with 4 bits / pixel (16 colors), fine for games.

Use even less memory with "fat pixels" (2 × 2 or 4 × 4).

23.19

Test pattern generator

Ref: Graham Keggi



Rather than look up each pixel value in a frame buffer, generate pixel color by comparing pixel coordinates with region boundaries:

```
process(row,column)
    begin
        -- large vertical color bands, evenly spaced horizontally, 320px vertically
        -- Gray, yellow, cyan, green, purple, red, blue
        if (column >= 0) and (column < 92) and (row >= 0) and (row < 320) then
            color <= GRAY1;
        elsif (column >= 92) and (column < 184) and (row >= 0) and (row < 320) then
            color <= YELLOW;
        elsif (column >= 184) and (column < 276) and (row >= 0) and (row < 320) then
            color <= CYAN;
        . . .
```

Same method used in simple video games (*e.g.*, Pong), where most of the screen is blank.

22.20

Before you go

Be sure to submit your quiz! Thank you.

23.21