Westly M. **Nolting** Ph.D.

FAILURE ANALYSIS R&D ENGINEER

Hillsboro, OR, USA

Phone # upon request | ■ w.nolting@gmail.com | • wnolting | • wnolting

Experience

Intel Corporation Hillsboro, OR, USA

FAILURE ANALYSIS R&D ENGINEER

• Failure analysis of Intel's latest process nodes as well as Intel 3, Intel 4, Intel 7, 10nm, and 14nm process nodes

- Utilizing SEM, FIB, TEM, and STEM to analyze defects in Intel's latest process nodes
- Utilizing electrical characterization tools to isolate defects in complex microarchitectures on Intel products
- Expert proficiency with use of Infrared, Laser, X-ray, and various optical probing tools for defect localization
- Marginal circuit analysis and defect isolation for test chips
- · Lead engineer for test program development for Early Life Failure (ELF) and Early Life Reliability (ELR) testing
- Lead failure analysis engineer for reliability learning in early life failures
- Low Yield Analysis for all of Intel's process nodes
- Responsible for accurate presentation and analysis of data to all customers, preparation of models and reports for yield improvement, and
 presenting findings to all levels of management
- Responsible for training and mentoring new engineers in the failure analysis group on all tools and techniques and product architectures
- Application and software development for failure analysis tools
- Database management for defect analysis and yield improvement
- Responsible for the development of new techniques for defect analysis and yield improvement

SUNY Polytechnic Institute

Albany, NY, USA

Dec. 2018 - Present

GRADUATE RESEARCH SCIENTIST

Aug. 2012 - May 2018

- Monte Carlo modelling of electron transport in metal-semiconductor junctions
- Scanning Tunneling Microscopy (STM) utilizing ballistic electron emission microscopy (BEEM) in ultra high vacuum (UHV) environment
- · SEM, STM, FIB, STEM experience imaging materials for FinFETs, Schottky barriers, Silicides, and Tunnel Barriers
- · Fabrication of novel Schottky barrier devices utilizing Molecular Beam Epitaxy (MBE), electron-beam PVD, and magnetron sputtering
- Maintenance of UHV and metrology tools
- Responsible for accurate presentation and analysis of data, preparation of manuscripts for scientific publication, and presenting the research results at scientific conferences

SUNY Albany - SUNY Research Foundation

Albany, NY, USA

GRADUATE RESEARCH SCIENTIST

May 2012 - Aug. 2017

- Academic fab environment utilizing state-of-the-art industrial fab to develop device structures
- Metrology for device structures on novel Schottky barrier diode devices
- · Design and testing of novel spintronic device structures, utilizing non-local Hanle voltage, spin valve, and DC spin current measurements
- $\bullet \quad \text{Magnetic Tunnel Junction (MTJ) characterization and STT-MRAM modeling with stacks deposited using SINGULUS Timaris tool \\$
- Responsible for accurate presentation and analysis of data, preparation of manuscripts for scientific publication, and presenting the research results at scientific conferences

University of New Orleans - Advanced Materials Research Institute

New Orleans, LA, USA

GRADUATE RESEARCH ASSISTANT

May 2010 - May 2012

- Designing, building, and testing of a high-temperature Hall effect and Nernst effect experiment
- · Maintaining spark plasma sintering (SPS), 10-ton hot press furnace, and electrical/magnetic characterization tools
- Fabrication of ceramic thermoelectric materials
- · Performing thermal and electrical measurements such as Hall effect, thermal conductivity, Seebeck coefficient, and electrical conductivity
- Responsible for accurate presentation and analysis of data, preparation of manuscripts for scientific publication, and presenting the research results at scientific conferences

Skills

Metrology & Instrumentation: SEM, TEM, Auger, XRD, BEEM, AFM, XPS, STM, VSM, MBE, PPMS

Fault Isolation: LVI, LVP, LVT, LADA, SDL, TIVA, OBIRCH, SMI, IREM, TDR, TFS Meridian, X-ray, XADA

Programming Python, C/C++, C#, LaTeX, Perl, CS, tcl, SQL

Languages English

Software Cadence, Allegro, Avalon, Mentor Graphics, Microsoft Office, ImageJ, Origin, Matlab, Mathematica, Labview

AUGUST 5, 2024

Education

State University of New York at Albany / Polytechnic Institute

Ph.D. IN NANOSCALE SCIENCE AND ENGINEERING

Albany, NY, USA

Aug. 2012 - May 2018

State University of New York at Albany - College of Nanoscale Science and Engineering

M.S. IN NANOSCALE SCIENCE AND ENGINEERING

Albany, NY, USA

Aug. 2012 - Aug. 2017

University of New Orleans

M.S. IN APPLIED PHYSICS

New Orleans, LA, USA May 2010 - May 2012

University of New Orleans

B.S. IN PHYSICS

New Orleans, LA, USA

Aug. 2006 - May 2010

Writing

Laboratory X-Ray-Assisted Device Alteration for Fault Isolation and Post-Silicon Debug

2024 IEEE International Reliability Physics Symposium (IRPS)

CELIO, K. C., SEN, S., NISENBOIM, E., PARDY, P. M., NGUYEN, B., LE, V., NOLTING, W., KUMAR, S., PETERSON, C. A., RAVEH, A., JOHNSON, K., STRIPE, B., Su, F., LUN, M., LEWIS, S., SPINK, R. I. AND YUN, W.

2024

• To explore the utility of x-rays for LADA-like work, we have developed a first-of-a-kind x-ray-assisted device alteration (XADA) tool, with an industry-leading spot size and flux density, capable of interfacing with modern integrated circuit test equipment. We demonstrate for the first time the use of XADA for real fault isolation and post-silicon debug cases.

Nansocale Schottky Barrier Visualization Utilizing Computational Modeling and Ballistic **Electron Emission Microscopy**

J. Appl. Phys

W. Nolting, C. Durcan, S. Gassner, J. Goldberg, R. Balsano, Vincent P. Labella

2018

· The findings demonstrate the ability to detect the effects of partial silicide formation in the W and Cr samples and the presence of two barrier heights in intermixed Au/Ag films upon the electrostatic barrier of a buried interface with nanoscale resolution.

Fermi Level Manipulation through Native Doping in the Topological Insulator Bi₂Se₃

ACS Nano

L. Walsh, A. Green, A. Dou, W. Nolting, et. al.

• We report the growth of near-intrinsic Bi2Se3 with a minimal Se vacancy concentration providing a Fermi level near midgap with no extrinsic counter-doping required. We also demonstrate the crucial ability to tuneEF from below midgap into the upper half of the gap near the conduction band edge by controlling the Se vacancy concentration using post-growth anneals.

Detection of Silicide Formation in Nanoscale Visualization of Interface Electrostatics

APL

W. NOLTING, C. DURCAN, V. P. LABELLA

2017

 The ability to detect localized silicide formation at a buried metal semiconductor Schottky interface is demonstrated via nanoscale measurements of the electrostatic barrier.

Nanoscale Schottky Barrier Mapping of Thermally Evaporated and Sputter Deposited W/Si(001) Diodes Using Ballistic Electron Emission Microscopy

JVST B

W. Nolting, C. Durcan, A. J. Narasimham, V. P. Labella

 Ballistic electron emission microscopy has been utilized to demonstrate differences in the interface electrostatics of tungsten-Si(001) Schottky diodes fabricated using two different deposition techniques: thermal evaporation using electron-beam heating and magnetron sputtering

Effects of Electrical Bias and Temperature Stress on the Negative Magnetoresistance of a **Low-k Dielectric**

J. Appl. Phys

B.T. McGowan, W. M. Nolting, J.R. Lloyd

· A study of the effect of electrical bias and temperature stress (BTS) on the negative magnetoresistance (MR) of a low-k dielectric composed of SiCOH is presented.

Correlation Between Microstructure and Drastically Reduced Lattice Thermal Conductivity in Bi₂Te₃/Bi Nanocomposites for High Thermoelectric Figure of Merit

Mater. Sci. in Semiconductor

D.K. MISRA, S. SUMITHRA, N.S. CHAUHAN. W. M. NOLTING, P.F.P. POUDEU, KEVIN L. STOKES

2015

• D.K. Misra, S. Sumithra, N.S. Chauhan. W. M. Nolting, P.F.P. Poudeu, Kevin L. Stokes

Effect of NiTe Nanoinclusions on Thermoelectric Properties of Bi₂Te₃

Journal of Electronic Materials

S. Sumithra, N. J. Takas, <u>W. M. Nolting</u>, S. Sapkota, P.F.P. Poudeu, and K.L. Stokes

2012

S. Sumithra, N. J. Takas, W. M. Nolting, S. Sapkota, P.F.P. Poudeu, and K.L. Stokes

Enhancement in Thermoelectric Figure of Merit in Nanostructured ${\rm Bi}_2{\rm Te}_3$ with Semimetal Nanoinclusions

S. Sumithra, N. J. Takas, D. K. Misra, W. M. Nolting, P. F. P. Poudeu, and K. L. Stokes

Adv. Energy Materials

2011

• S. Sumithra, N. J. Takas, D. K. Misra, W. M. Nolting, P. F. P. Poudeu, and K. L. Stokes

Electronic Transport in Thermoelectric Bismuth Telluride

W. Nolting, K. L. Stokes

• W. Nolting, K. L. Stokes

University of New Orleans
Scholar Works UNO Thesis Publication