Khulna University of Engineering & Technology (KUET), Khulna

Department of Computer Science and Engineering (CSE)

CSE 4224: Digital System Design Laboratory

Title: Design of an Arithmetic Logic Unit (ALU).

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Date : 27/04/2021

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Objectives: The objectives of this experiment are noted below:

i) gathering knowledge about adders (half and full) and true/complement or one/zero arithmetic logic and circuit.

ii) gathering knowledge about arithmetic and logical circuit.

iii) implementation of arithmetic and logical operations.

iv) ~~to~~ gathering knowledge for design of digital system and finally implementation of digital system.

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Introduction: Arithmetic and Logic Unit (ALU) has eight arithmetic operations and four logical operations. It has three selector variables S_2, S_1 and S_0 which select eight operations with another input C_{in} (input carry bit).

When the selector bit $S_2=0$, the three bits S_1, S_0 and C_{in} are used to select eight arithmetic operations. And when $S_2=1$, the next S_1, S_0 ~~and C_{in}~~ bits are used to select logical operations such as OR, XOR, AND and NOT operations.

OR operation: $S_2=1$, input carry C_i is zero in each stage and $S_1S_0=00$, it should generate the function $F_i=A$. To change the OR operation we must change the input of each full adder circuit from A_i to A_i+B_i.

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AND Operation: when $S_2=1$, $S_1S_0=10$ it works as AND operation, $F = A_i \oplus B_i$. We generate AND operation $F_i = A_iB_i$, some boolean function obtain when $S_2S_1S_0 = 110$ then,

$$F_i = X_i \oplus Y_i = (A_i \oplus K_i) \oplus B_i = A_iB_i + K_iB_i + A_i\acute{K}_i\acute{B}_i$$

result reveals if variable $K_i = B_i$, then

$$F_i = A_iB_i + B_i\acute{B}_i + A_iB_i\acute{B}_i = A_iB_i$$

The conclusion is that, if A_i ORed with B_i when $S_2S_1S_0 = 110$, then the output is AND generated.

The input of each full adder circuit we specified by the Boolean function.

$$X_i = A + S_2S_1\acute{S}_0B_i + S_2S_1S_0\acute{B}_i$$

$$Y_1 = S_0B_1 + S_1\acute{B}_i$$

$$z = S_2\acute{C}_i$$

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when $S_2=0$ then,

$$X_i = A_i$$

$$Y_i = S_0 B_i + S_1 B_i'$$

$$Z_i = C_i'$$

arithmetic operations are performed.

when $S_1=01$ then,

$$X_i = A_0$$

$$Y_i = S_0 B_i + S_1 B_i'$$

$$Z_i = 0$$

logical operations are performed.

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Circuit Diagram: 2-bit ALU circuit diagram for logical operations are drawn below:

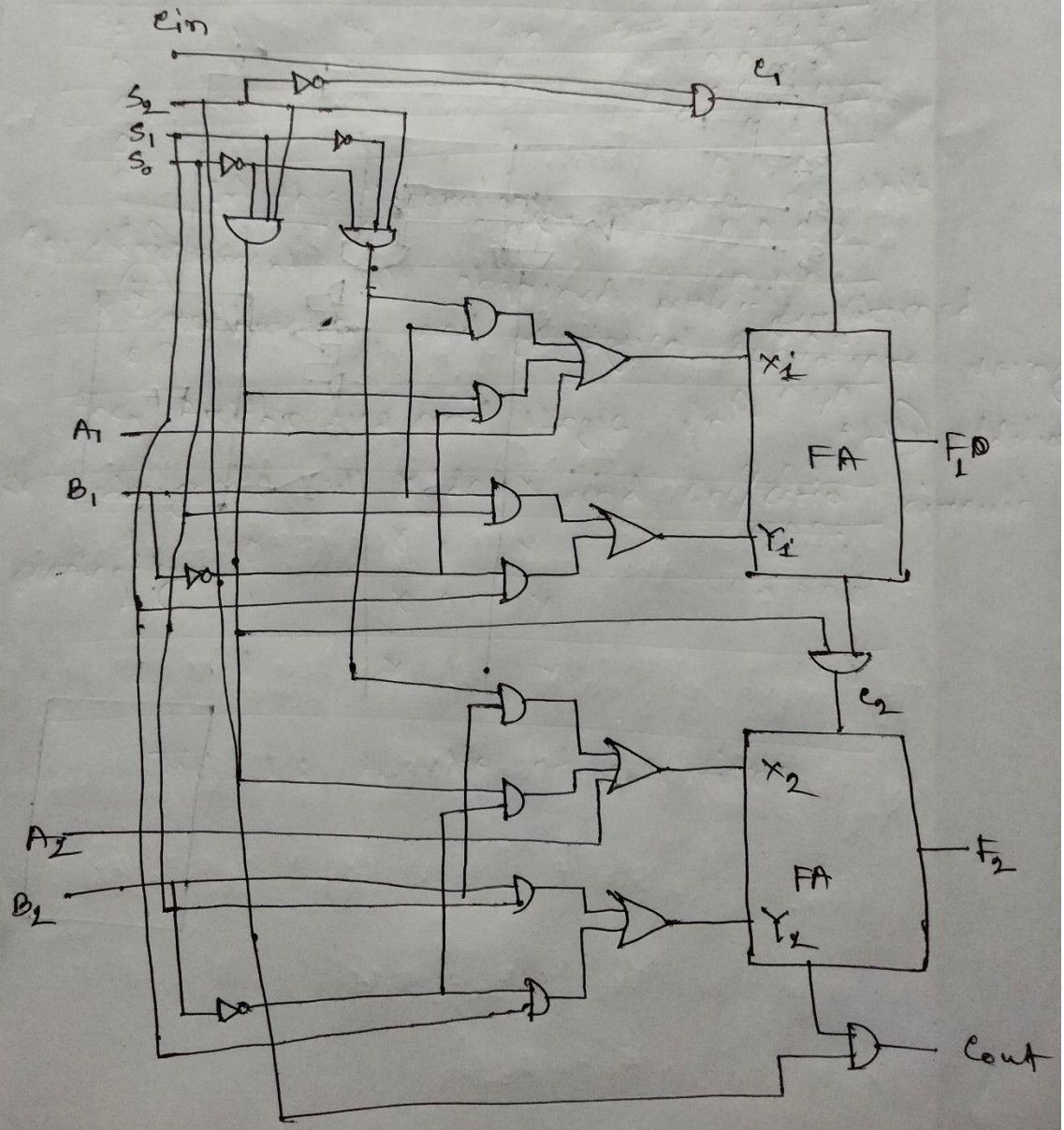

Figure 1: Circuit Diagram for 2-bit ALU

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Experimental Result: My roll is 1607021; So, A = B_2 and B = 1. So the results ~~are~~ are –

Selection				Output				
S_2	S_1	S_0	C_{in}	~~C_{out}~~	F_3	F_2	F_1	F_0
0	0	0	0		0	0	1	0
0	0	0	1		0	0	1	0
0	0	1	0		0	0	1	0
0	0	1	1		0	1	0	0
0	1	0	0		0	0	0	0
0	1	0	1		0	0	0	1
0	1	1	0		0	0	0	1
0	1	1	1		0	0	1	0
1	0	0	X		0	0	1	1
1	0	1	X		0	0	1	1
1	1	0	X		0	0	0	0
1	1	1	X		1	1	0	1

Table 1: Results of operations

Conclusion: In this laboratory, the purpose of this experiment was obtained perfectly. We performed 8 arithmetic and 4 logical operations using the Arithmetic and Logic Unit (ALU). In addition, we designed Full Adder and One/zero circuit perfectly.