

Khulna University of Engineering & Technology (KUET), Khulna Department of Computer Science and Engineering (CSE)

CSE 4224: Digital System Design Laboratory

Title: Data transferring from one tri-state buffer register to another through bus.

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西Objectives: The objectives of this experiencent are noted below:

- (i) to know about tri-state butter register.
- (ii) to know about bus connection.
- (iii) to experiment the passing of data from register to register through bus.
- (in) implementation of the circuit with bus connection and tri-state buffer register.

由 Introduction:

tri-state Butten Pegisten: A butter register is the simplest kind of register, all it does is stone a digital world. It is similar to a butter but it alls an additional enable imput that controlls whether the primary imput is passed to its output or not. Basically a tri-state butter register is a controlled

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buffer register combining with the state buffer. D-Hip flop are used here. A q-bit toci-state buffer ein. cuit is implemented below:

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(iv) implementation of the cincuit with two or

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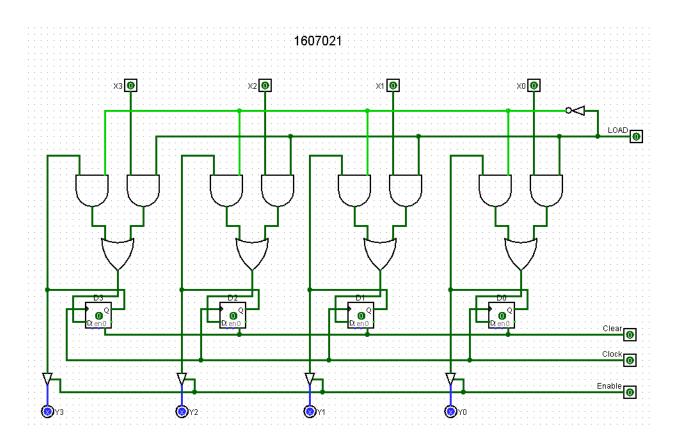


Figure 1: A 4 bits tri-state buffer register.

be almosters a word from one negister to as

Bus: A bus is a group of wines that transmit a binary word. It is a high speed internal connection.

Expus-organised Computers: A bus of 4 wines is a common transmission path between the trustate registers. The imput data bits for register come from the bus, at the same time, the truistate output of registers connects back to the bus, simply, the other negisters have their imputs and output eastnected to the bus. The beauty of bus organization is the ease of transferring a world from one negister to another. To begin with, the same clock signal drives all registers, but nothing happens until applying high controls imputs. In other words

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as long as all to LOAD and ENABLE inputs are low, the registeris are isolated from the bus.

a representation of the constitute

To transfer a world from one register to another making the appropriate control inputs high. The whole circuit through bus is irreplemented below:

quadrete. The ireput disto bute in neglectus corner the two, at the law distribe only at the two, at the law distribe only at negligible connects back to the bus, simply other, negligibles bear their impuls oned output and the law impulsion of the bus, the beauty of two impurious is the constraint of the marketining is should the energy of the law in the begins with the energy of the contraint of the contraint

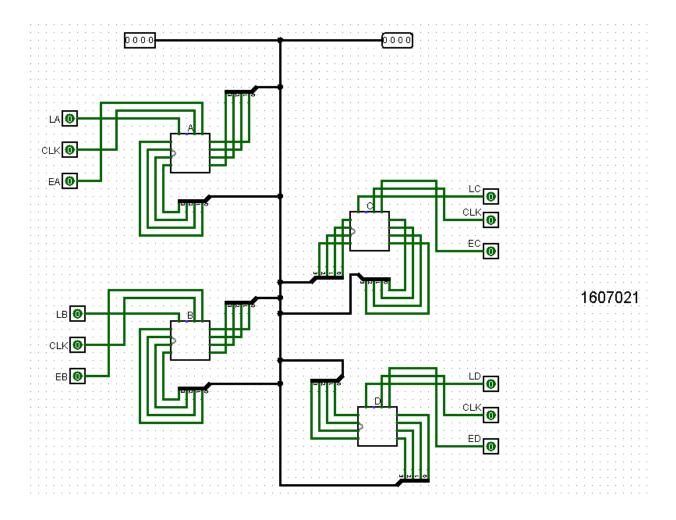


Figure 2: Data transferring from one register to another through bus.

En Discussion: In this bebonatory, the expercionent of cornecting this state button registers through bus was implemented. In addition, a world of 4 bits obtained included from the addition of best 2 digits of my roll number was transferenced from one register to another register using bus without any errors o successfully.