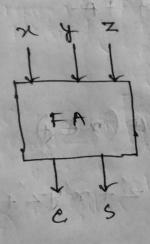
The Objectives of this laboratory are noted below.

- i) to know about digital system degism design mechanism.
- ii) to know about adder (half and full), zero/one circuit and anithmetic circuit.
 - iii) to know how to impliment digital circuits using logisim.
 - "in) to impliment areithmetic circuit using logistion or and verify outputs.
 - v) to impliment a cineuit using top-down modular fashion.

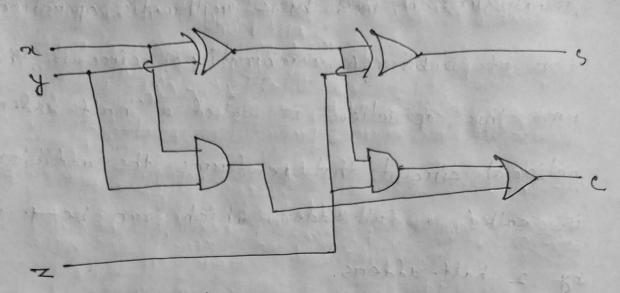
Harmoduction: The most basic arithmetic operation the addition of 2 bits. A combinational circuit that pertonents this operation is called a half-adden. A combinational circuit that performs the addition of 3 bits national circuit that performs the addition of 3 bits is called a full-adden, which can be primplimented by 2 half-addens.



	vi	-1	5	2
7	8			-
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	L
L	0	0	1	0
1	0	1	0	1
L	L	0	10	11
THE	4	L	1	

Full Adder





Implementation of FA

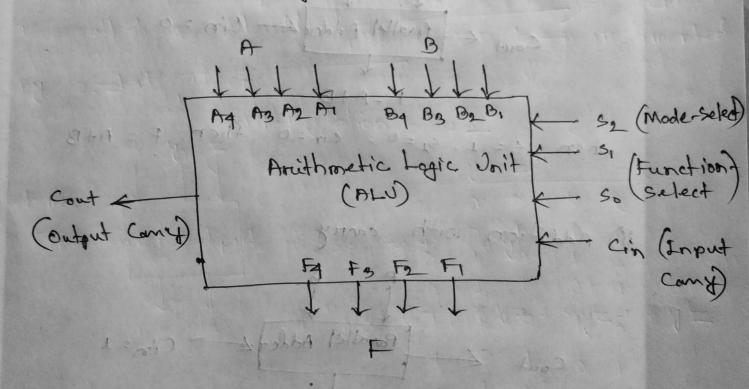
here,

The sum output is, s= = = (x 0)

= 24/2/+ 2/42/+ 242 + 2/4/2

The carry output is, c = z(x'y + xy') + xy = xy'z + x'yz + xy

Ancithmetic togic Unit (ALU): An anithmetic are logic unit is a digital circuit used to perform anithermetic and logical operations. It represents the fundamental building block of a computer.



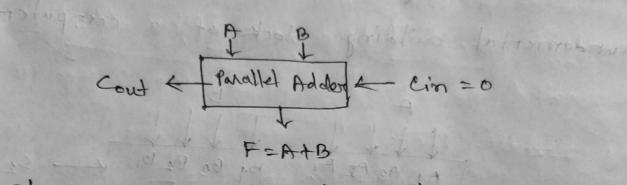
Block Diagram of a 4-bit ALV

The half said to a solution to adapt

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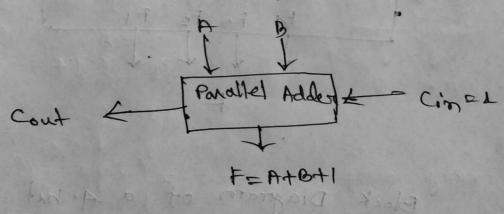
There are 8 operations of ALU. They one given below:

1) Addition



when s=1, s1=0, cin=0 then F=A+B

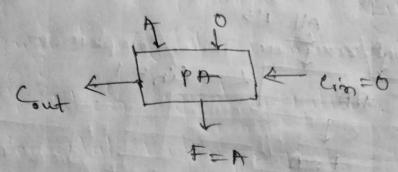
ii) Addition with carry



when So=1, S1=0, Cin=01 then F= A+B+1

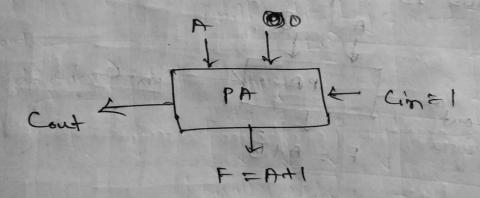


iii) Transfer A



when sico, sico, cinto then FEA

is) Increment A



when 5,=0, 5,=0, cin=1 then F=A+1

Decrement A

PA

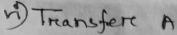
Cout

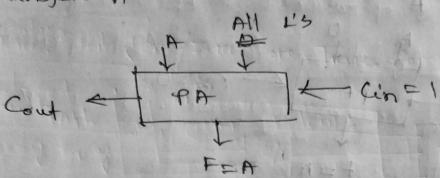
Cout

F=A-1

when 5=1, 5=1, ein=0 then F=A-1

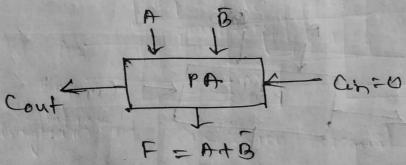






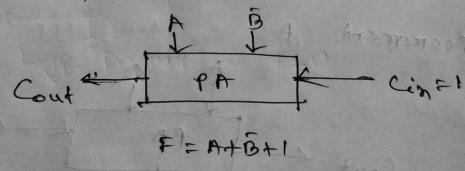
when s=1, s=1, ein=1 then F=A

vii) A plus is complement



when so=0, si=1, cin=0 then F=A+B

viii) Subtraction



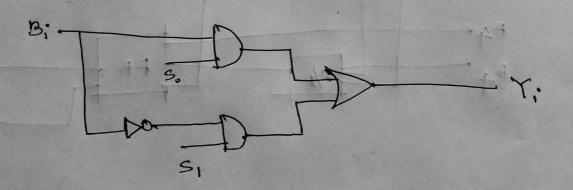
when so=0, s=1, lin=1 then f=A+18+1

Herce, fore onefzero ore True/Complement circuit, the

truth table is given below:

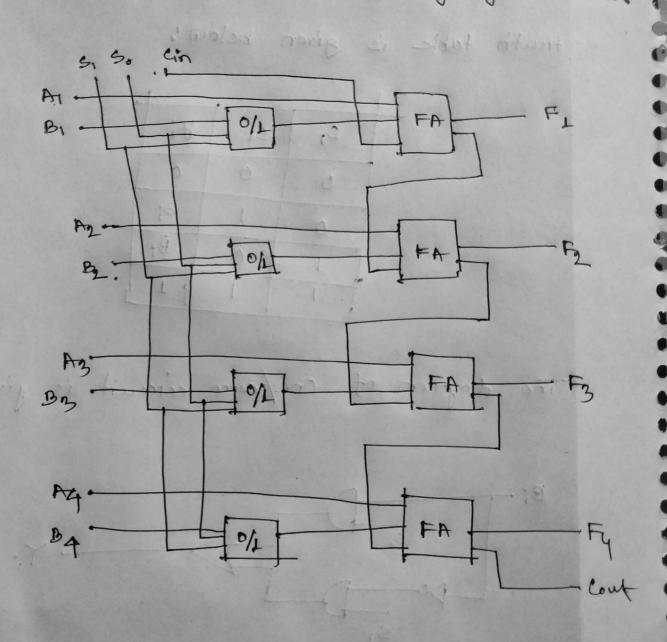
5,	S	y: T
0	0	0
0	1	B;
	10	Bi
41	1	41

The diagram of one/zereo cerecuit is given below:



water biogram of ALU

The ALV diagram fore 4 bits is gen given below:



Logic Diagram of ALU

The Condusion: In this laboratory, arithmetic circuit has been impliment using logisim. Full adder and zero one-zero modular circuit is included into main arithmetic circuit successfully, 8 bits arithmetic circuit is implemented and designed outputs are checked properly.

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