Noritake itron

RoHS 2011/65/EU

Vacuum Fluorescent Display
Module
Specification

Model: GU128X64E-U100

Specification No.	: DS-1702-0000-01	
Date of issue	: February 08, 2012	(00)
Revision	: March 07, 2012	(01)
	:	
	:	
	:	

Published by
NORITAKE ITRON Corp. / Japan
http://www.noritake-itron.jp

This product complies with RoHS Directive 2011/65/EU

Contents

1 General Description

1.1 Application

Readout of computer, micro-computer, communication terminal and automatic instruments.

1.2 Construction

The module consists of a 128 × 64 dot graphic BD-VFD, DC/DC converter, display controller, and all necessary control logic.

1.3 Scope

Power supply: Single $5V_{DC}$ power supply
Interface *: Parallel interface (CMOS-level)
Serial interface (CMOS-level) [Synchronous, SPI and Signal separate]
Function: Graphic display, Control command

*: Select by Jumper setting. (Refer to “10 Interface Description”.)

2 Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Power Supply Voltage	V_{CC}	-0.3	-	+6.5	V_{DC}	-
Logic Input Voltage	V_I	-0.5	-	+7.0	V_{DC}	-

3 Electrical Ratings

Measuring Conditions: Ambient temperature = 25 ºC

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Power supply Voltage	V_{CC} - V_{SS}	4.75	5.00	5.25	V_{DC}	-

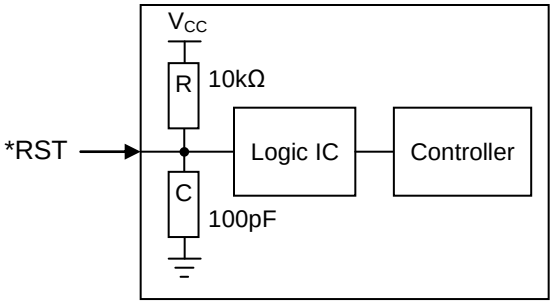
4 Electrical Characteristics

Measuring Conditions: Ambient temperature = 25 ºC, V_{CC} = 5.0V_{DC}

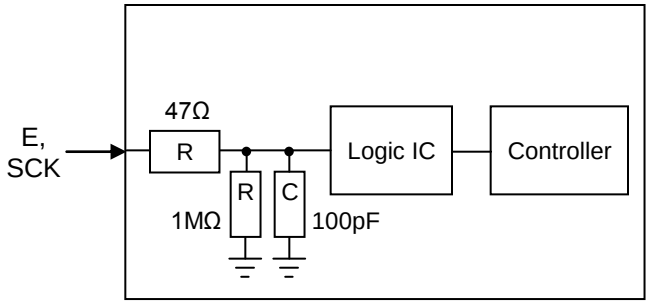
Parameter		Symbol	Min.	Typ.	Max.	Unit	Condition
Logic Input Voltage	‘H’	V_{IH}	0.7V_{CC}	-	V_{CC}	-	-
	‘L’	V_{IL}	V_{SS}	-	0.9	V_{DC}	-
Logic Output Voltage	‘H’	V_{OH}	3.5	-	-	V_{DC}	I_{OH} = -0.2mA
	‘L’	V_{OL}	-	-	0.6	V_{DC}	I_{OL} = 1.6mA
Power Supply Current 1		I_{CC1}	-	550	720	mA	Display ON, All dots ON
Power Supply Current 2		I_{CC2}	-	400	520	mA	Display ON, All dots OFF
Power Supply Current 3		I_{CC3}	-	35	70	mA	Power-save-mode
Power Consumption			-	2.75	3.60	W	Display ON

Note: I_{CC} might be anticipated twice as usual at power on rush.

*RST Internal Diagram



E, SCK Internal Diagram



5 Environmental Specifications

Operating temperature	: -40 to +85 ºC
Storage temperature	: -40 to +85 ºC
Operating humidity	: 20 to 80 % RH (non-condensing)
Vibration (non-operating)	: 10-55-10Hz, all amplitude 1.0mm, 30minutes, X-Y-Z
Shock (non-operating)	: 539 m/s^2 (55G), 10ms, X-Y-Z, 3 times each direction

6 Optical Specifications

Luminance	: Min.350 cd/m^2 (Typ.1,000 cd/m^2)
Color of illumination	: Green (Blue-green)

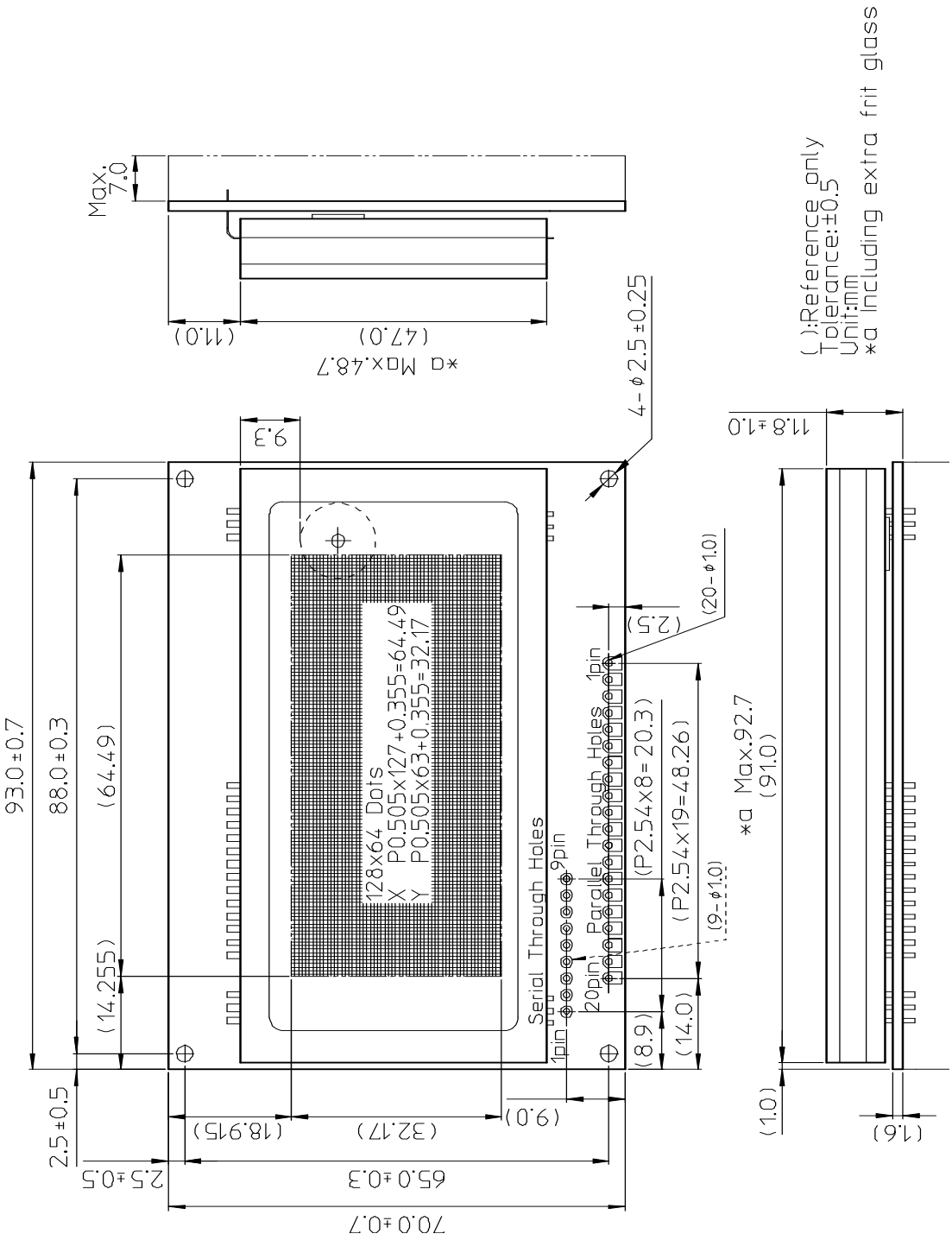
7 Physical Specifications

Number of dots	: 8,192 (128 × 64)
Display area	: 64.49 × 32.17 mm (X × Y)
Dot size	: 0.355 × 0.355 mm (X × Y)
Dot pitch	: 0.505 × 0.505 mm (X × Y)
Weight	: Approximately 99g

8 Applicable Specifications

Applicable VFD module reliability specification:	TT-99-3102
Applicable VFD module quality specification:	TT-98-3413
Applicable VFD quality specification:	TT-93-3336D

9 Outline dimension



DS-1702-0100-00

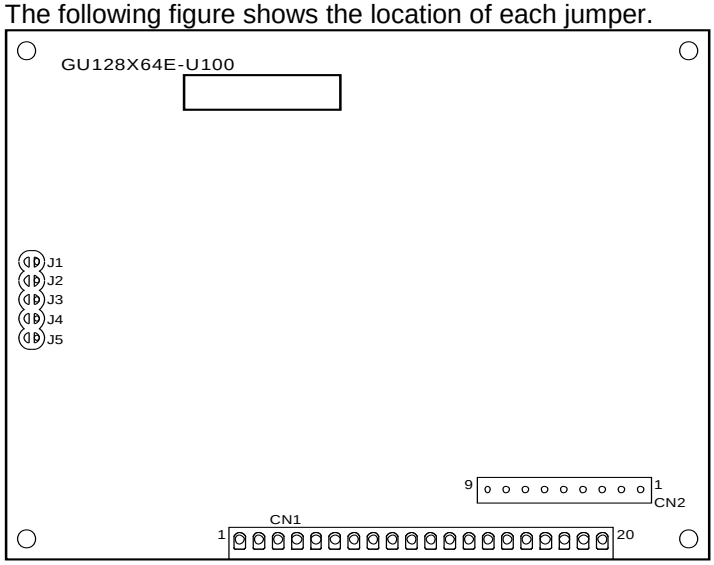
10 Interface Description

This module supports 4 kinds of interfaces. These interfaces can be changed by the jumpers.
The following table shows the function of Jumpers. Default setting is parallel interface.

J2	J1	Interface type
Open	Open	Parallel (default)
Open	Short	Serial: type1
Short	Open	Serial: type2
Short	Short	Serial: type3

Note: J3 ~ J5 are factory use only.

The following figure shows the location of each jumper.



10.1 Signal Description

The display area is selected from Left area or Right area by the CS1 and CS2.
Refer to “14 Display Data RAM map”.
*Display Data RAM: hereinafter referred to as the "DDRAM"

CS1	CS2	Description
L	L	non-operation
L	H	Write to Right area or Read from Right area
H	L	Write to Left area or Read from Left area
H	H	Write to Left and Right area or Read from Left area

Note: In the following pages, *CS1 and *CS2 are logical inversion of CS1 and CS2, respectively.

The data write or read is selected by RW.
When RW is “0”, the data is written.
When RW is “1”, the data is read.

The register is selected from Instruction Register or Data Register by RS.
When RS is “0”, the register is Instruction-Register.
When RS is “1”, the register is Data-Register.

	L	H
RW	Data Write	Data Read
RS	Instruction Register	Data Register

10.2 Parallel interface through-holes (CN1)

Pin No.	Signal name	Function
1	V_{SS}	Ground
2	V_{CC}	Power supply
3	NC	Non connection
4	RS	Register Select
5	RW	Data transfer select
6	E	Enable
7	DB0	Data input/output
8	DB1	Data input/output
9	DB2	Data input/output
10	DB3	Data input/output
11	DB4	Data input/output
12	DB5	Data input/output
13	DB6	Data input/output
14	DB7	Data input/output
15	CS1	Selection for Left area, active High
16	CS2	Selection for Right area, active High
17	*RST	Reset signal, active Low
18	NC	Non connection
19	NC	Non connection
20	NC	Non connection

10.3 Serial interface through-holes (CN2)

*** IC: Don't connect.**

10.3.1 At the Type1 is selected

Pin No.	Signal name	Function
1	V_{CC}	Power supply
2	SI/SO	Data input/output
3	V_{SS}	Ground
4	*CS	Chip select, active Low
5	SCK	Display clock
6	*RST	Reset signal, active Low
7	IC	Internal connection
8	IC	Internal connection
9	IC	Internal connection

10.3.2 At the Type2 is selected

Pin No.	Signal name	Function
1	V_{CC}	Power supply
2	SO	Data output
3	V_{SS}	Ground
4	IC	Internal connection
5	SCK	Display clock
6	*RST	Reset signal, active Low
7	*CS2	Selection for Right area, active Low
8	*CS1	Selection for Left area, active Low
9	SI	Data input

10.3.3 At the Type3 is selected

Pin No.	Signal name	Function
1	V_{CC}	Power supply
2	IC	Internal connection
3	V_{SS}	Ground
4	RS	Register Select
5	SCK	Display clock
6	*RST	Reset signal, active Low
7	CS2	Selection for Right area, active High
8	CS1	Selection for Left area, active High
9	SI	Data input

10.4 Serial Data Transfer

10.4.1 Type1: CU-UW series [Noritake-itron module] like format

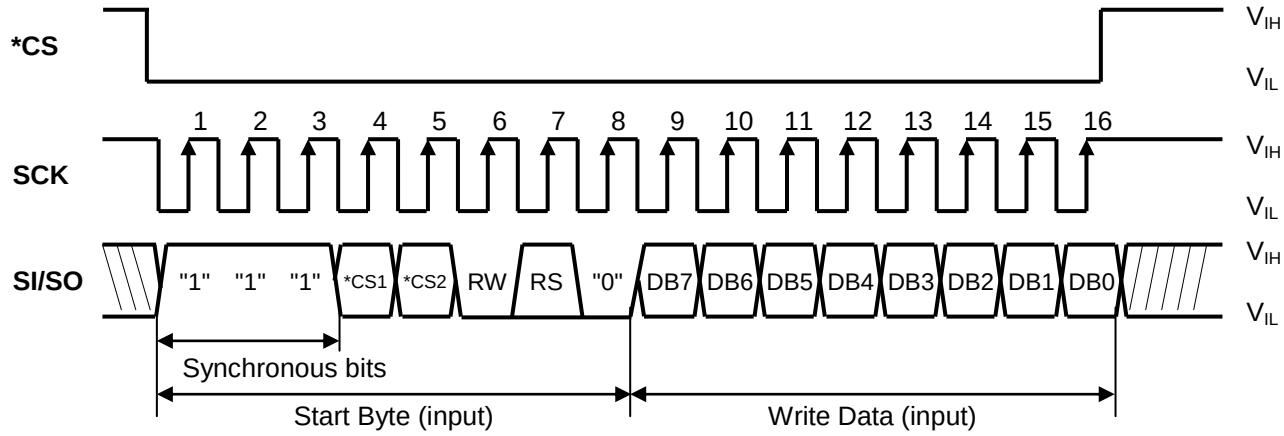
In this communication method, serial data can be inputted when the *CS goes to Low level.

Serial data consists of 2 bytes.
The 1st byte (Start Byte) consists of a total of 8 bits: the Synchronous bits (bit1~bit3), *CS1 (bit4), *CS2 (bit5), RW (bit6), RS (bit7) and bit8.

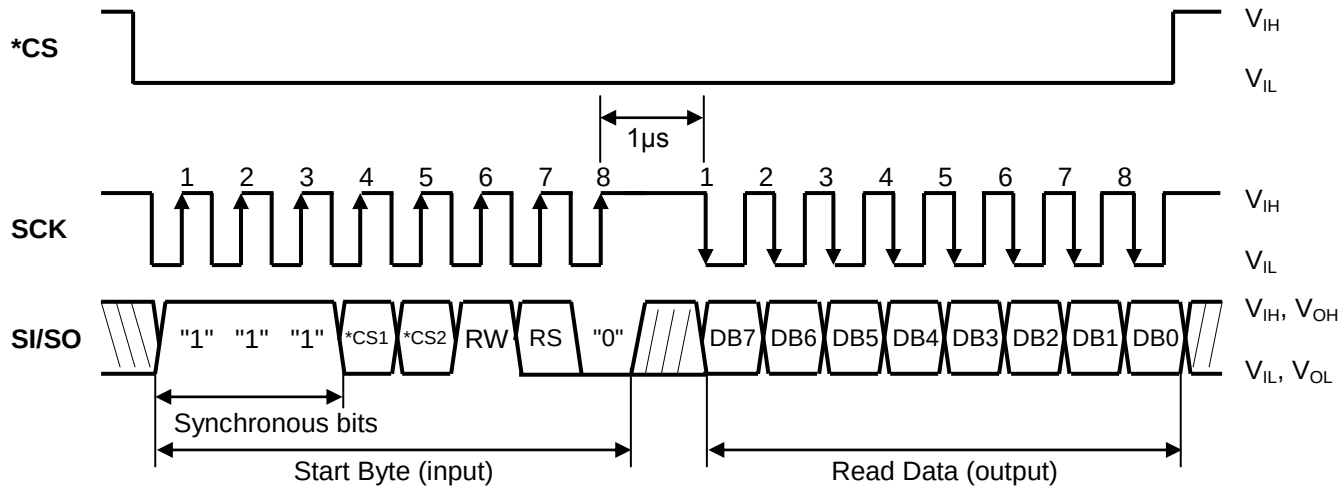
When "Write Display Data" or "Read Display Data" is operating, the 1st byte is required only once. The data since the 2nd byte can be written or read continuously without switching *CS. Then you can stop the continuous writing when *CS goes to High level.

*The read data is outputted at the falling edge of SCK.

<Data Write>



<Data Read>



10.4.2 Type2: SPI [Serial Peripheral Interface] format

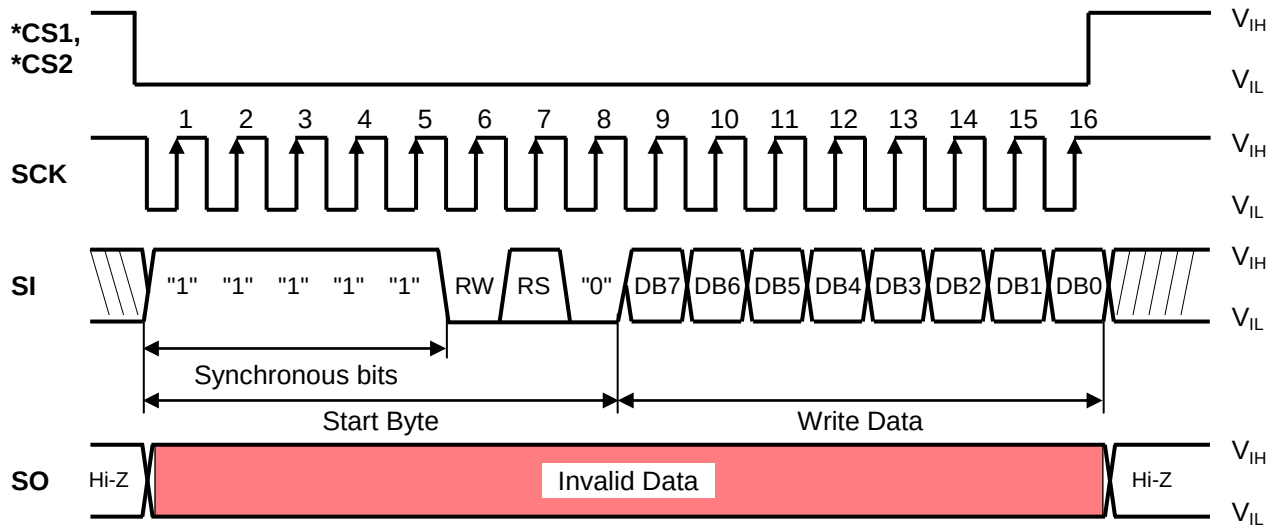
In this communication method, serial data can be inputted when the *CS1 (or *CS2) goes to Low level. Because SI and SO are separate signals, SI is write-only, SO is read-only.

Serial data consists of 2 bytes.
The 1st byte (Start Byte) consists of a total of 8 bits: the Synchronous bits (bit1~bit5), RW (bit6), RS (bit7) and bit8.

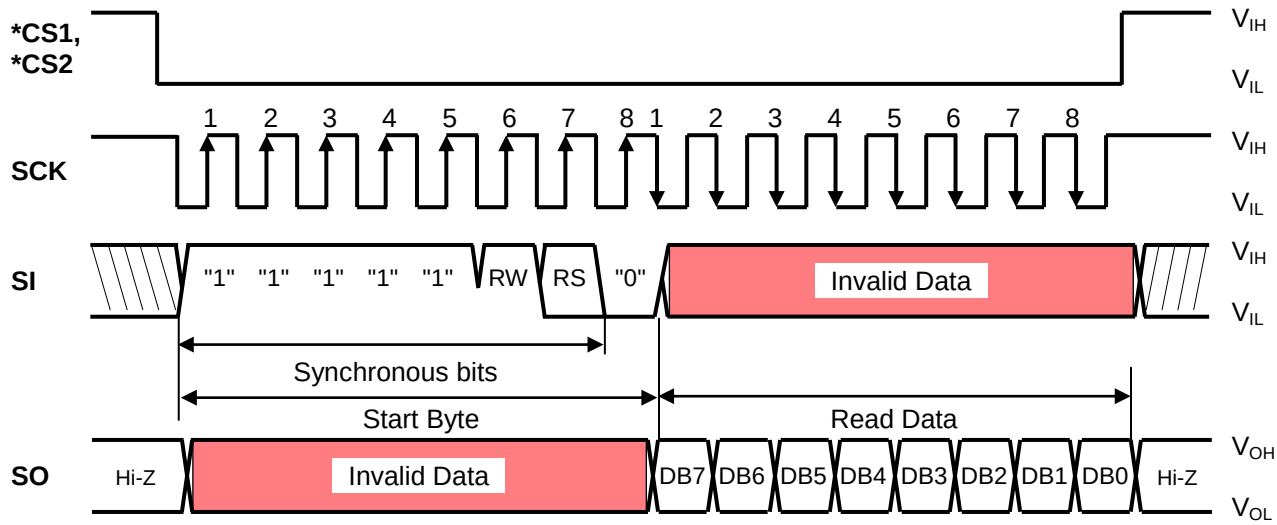
When "Write Display Data" or "Read Display Data" is operating, the 1st byte is required only once. The data since the 2nd byte can be written or read continuously without switching *CS1 (or *CS2). Then you can stop the continuous writing when *CS1 (or *CS2) goes to High level.

*The read data is outputted at the falling edge of SCK.

<Data Write>



<Data Read>



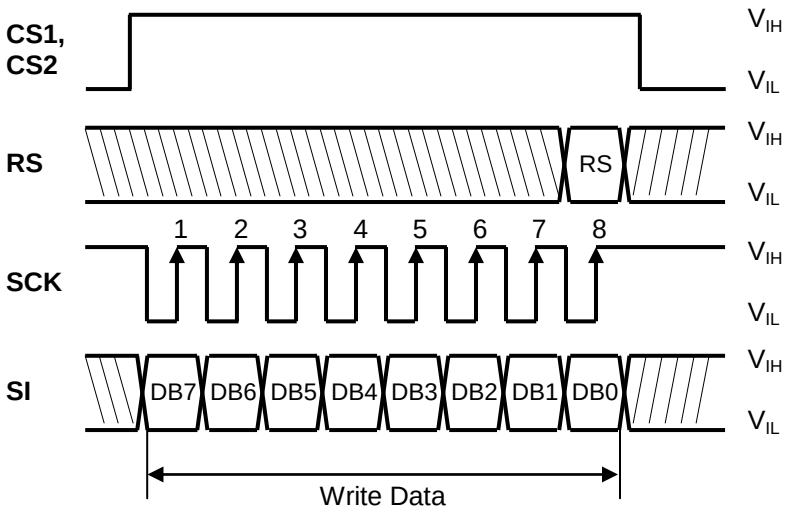
10.4.3 Type3: Signal separate format

In this communication method, serial data can be inputted when the CS1 (or CS2) goes to High level.

SI is shifted into the CPU on rising edge of SCK in the order of DB7 ~ DB0.
RS is sampled on 8th clock of SCK and the Write Data is written to the DDRAM or command register in the same clock.

When "Write Display Data" is operating, the data since 2nd byte can be written continuously without switching RS and CS1 (or CS2).
Then you can stop the continuous writing when CS1 (or CS2) goes to Low level.

<Data Write>

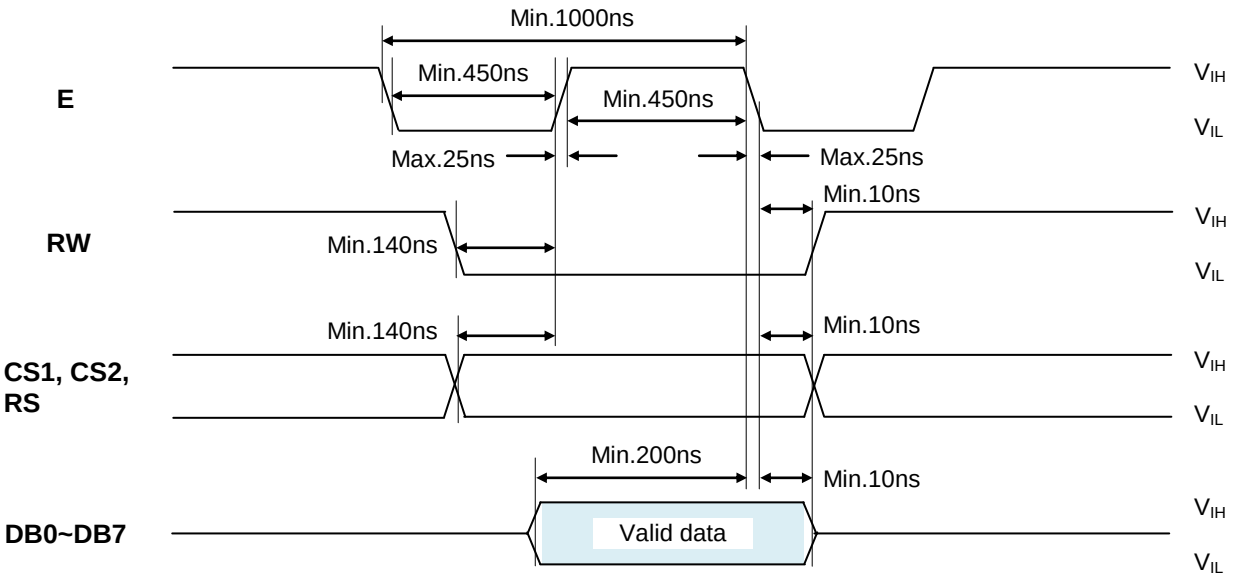


* <Data Read> is not available because this communication method doesn't have RW.

11 Timing Characteristics

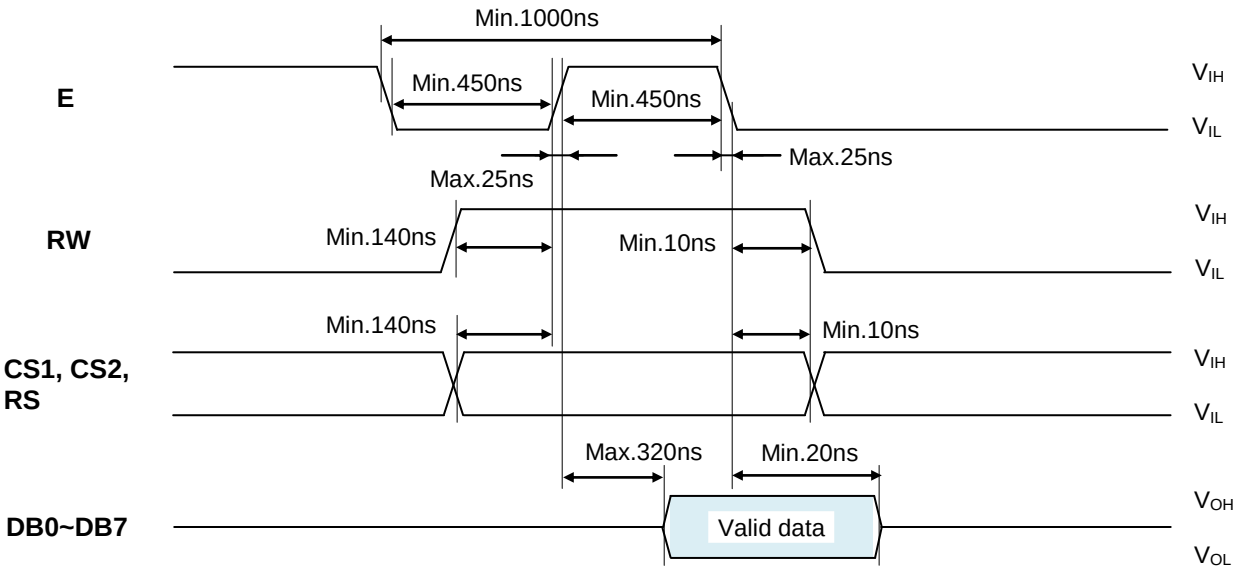
Input signal rise time and fall time < 15 ns.

11.1 Write timing (Parallel interface)



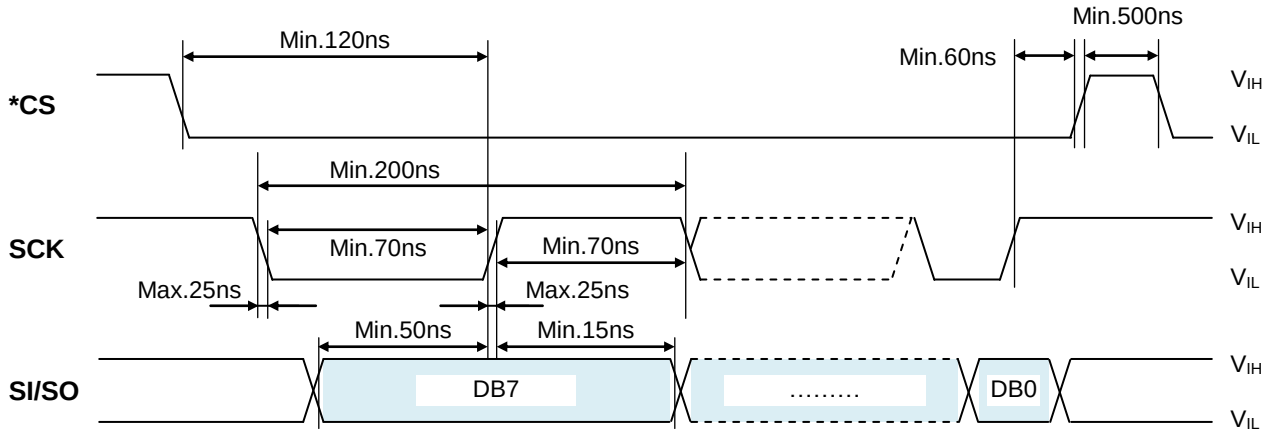
When "Write Display Data" is operating, the data since the 2nd byte can be written continuously without switching CS1 (or CS2), RW and RS.
Then you can stop the continuous writing when CS1 (or CS2) goes to Low level.

11.2 Read timing (Parallel interface)

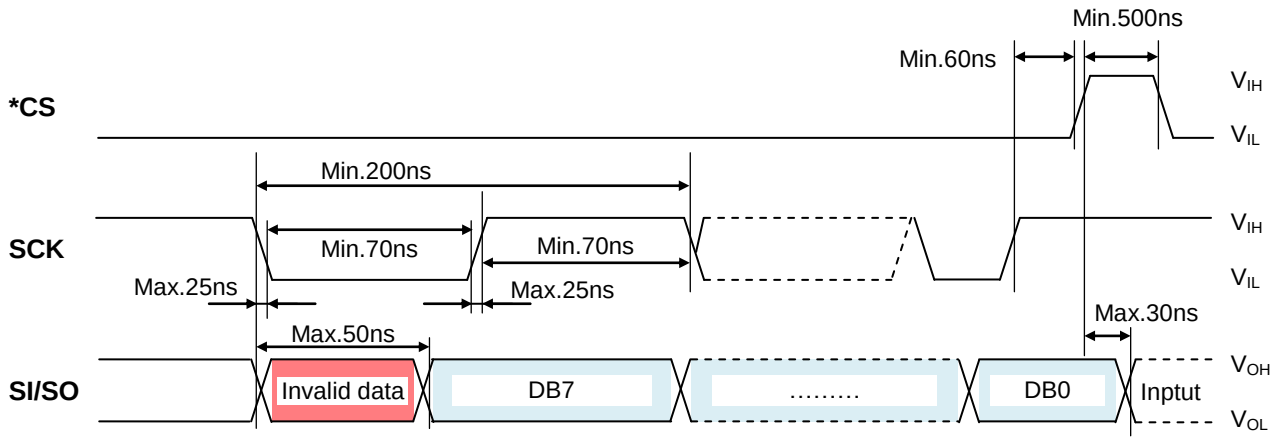


When "Read Display Data" is operating, the data since the 2nd byte can be read continuously without switching CS1 (or CS2), RW and RS.
Then you can stop the continuous writing when CS1 (or CS2) goes to Low level.

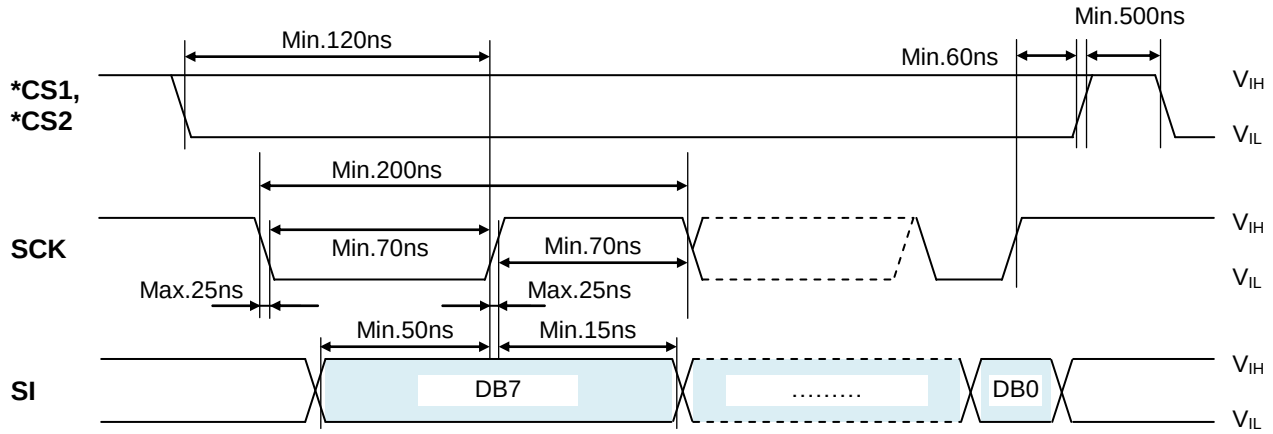
11.3 Write timing (Serial interface: Type1)



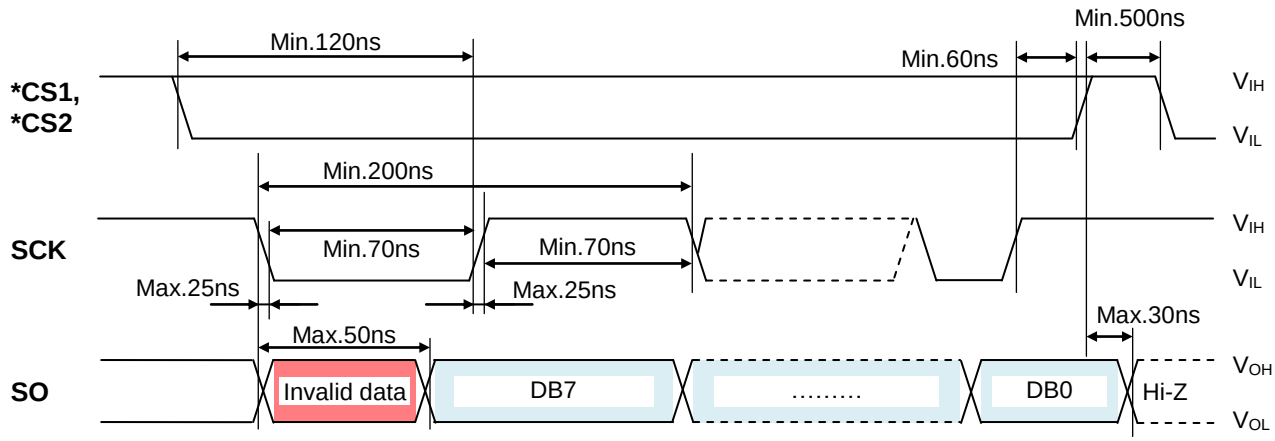
11.4 Read timing (Serial interface: Type1)



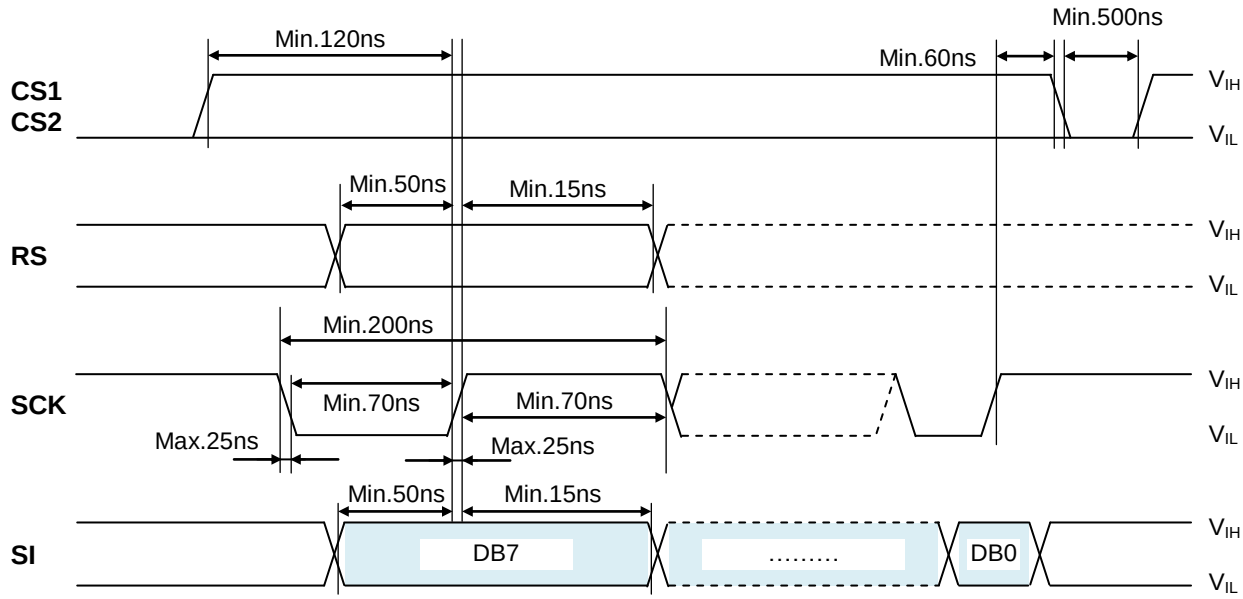
11.5 Write timing (Serial interface: Type2)



11.6 Read timing (Serial interface: Type2)



11.7 Write timing (Serial interface: Type3)



12 Display Control Instruction

The display control instructions control the internal state of the module.
Instruction is received from CPU to module for the display control.
The following table shows various instructions.

12.1 Instruction table

Instruction	CODE										Description
	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
Display ON/OFF	0	0	0	0	1	1	1	1	1	D	Controls the display ON or OFF. The internal status and the DDRAM data are not affected. **D:** 0: OFF, 1: ON **Default: Display OFF**
Set Address (Y Address)	0	0	0	1	Y address (0 ~ 63)						Sets the Y address at the column address counter. **Default: Y address = 00h**
Set Page (X Address)	0	0	1	0	1	1	1	Page (0~7)			Sets the X address at the X address register. **Default: X address = 00h**
Display Start Line (Z Address)	0	0	1	1	Display start line (0~63)						Indicates the DDRAM displayed at the top of the screen. **Default: Z address = 00h**
Status Read	0	1	Busy	0	ON / OFF	Reset	0	0	0	0	Reads the internal status. **Busy:** 0: Ready, 1: In operation **ON/OFF:** 0: Display ON, 1: Display OFF **Reset:** 0: Normal, 1: Reset
Write Display Data	1	0	Data writing								Writes data D0 ~ D7 into the DDRAM. After writing instruction, Y address is incriminated by 1 automatically.
Read Display Data	1	1	Data reading								Reads data D0 ~ D7 from DDRAM to the data bus.

<Extended instruction >

Function set	0	0	0	0	1	0	*	*	*	*	This instruction sets converter-power and screen brightness by next one byte data.
Power and Brightness Control	0	0	0	0	1	0	MD	BR2	BR1	BR0	Controls the screen brightness and Power-save-mode is on or off. **MD:** 0: Power-save-mode is on. 1: Power-save-mode is off. **BR2~BR0:** 00h: 100% ~ 07h: 12.5% **Default: Power-save-mode is off, Brightness = 100%**

*: Don't care.

12.2 Instruction Description

12.2.1 Display ON/OFF

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	1	1	1	1	1	D

The display data appears when D is 1 and disappears when D is 0.
Though the data is not on the screen with D=0, it remains in the DDRAM.
Therefore, you can make it appear by changing D=0 into D=1.

12.2.2 Set Address (Y Address)

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0

Y address (AC0~AC5) of the DDRAM is set in the Y address counter.
An address is set by instruction and increased by 1 automatically by read or write operations of display data.

12.2.3 Set Page (X Address)

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	1	0	1	1	1	AC2	AC1	AC0

X address (AC0~AC2) of the DDRAM is set in the X address register.
Writing or reading to or from MPU is executed in this specified page until the next page is set.

12.2.4 Display Start Line (Z Address)

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	1	1	AC5	AC4	AC3	AC2	AC1	AC0

Z address (AC0~AC5) of the DDRAM is set in the display start line register and displayed at the top of the screen.
The data of total line number of display screen from the line specified by this instruction is displayed.
This instruction is used for scrolling of the display screen.

12.2.5 Status Read

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	1	Busy	0	ON / OFF	Reset	0	0	0	0

Busy:
When Busy is 1, the module is executing internal operation and no instructions are accepted.
When Busy is 0, the module is ready to accept any instructions.

ON / OFF:
When ON/OFF is 1, the display is off.
When ON/OFF is 0, the display is on.

Reset:
When Reset is 1, the system is being initialized. In this condition, no instructions except status read can be accepted.
When Reset is 0, initializing has finished and the system is in the usual operation condition.

12.2.6 Write Display Data

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	1	0	D7	D6	D5	D4	D3	D2	D1	D0

Writes data D0 ~ D7 into the DDRAM.
After writing instruction, Y address is increased by 1 automatically.

12.2.7 Read Display Data

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	1	1	D7	D6	D5	D4	D3	D2	D1	D0

Reads data D0 ~ D7 from the DDRAM.
After reading instruction, Y address is increased by 1 automatically.

Note:
When using the parallel interface, the first read data is dummy data.

12.2.8 Function set

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	1	0	*	*	*	*

*: Don't care.

This instruction sets converter-power and screen brightness by next one byte data.
However, if the next data is not given the following data, this instruction is ignored and handled as normal data.

12.2.9 Power and Brightness Control

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	1	0	MD	BR2	BR1	BR0

MD:
When MD is 1, the Power-save-mode is off. [Converter-power is on, default setting]
When MD is 0, the Power-save-mode is on. [All dots is off, Converter-power is off]

Control Converter-power is on or off. This is applied until this instruction is re-specified.

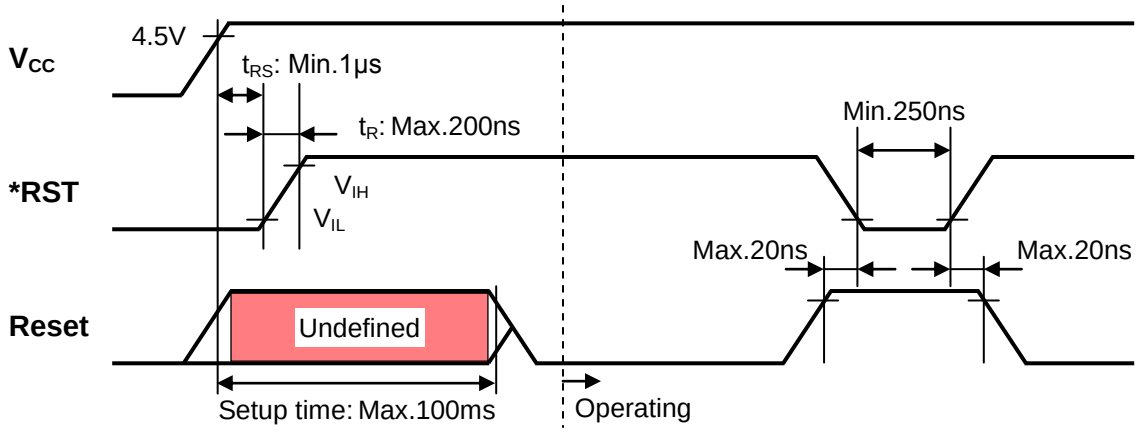
BR2 ~ BR0:
Screen brightness level is as follows.

BR2	BR1	BR0	Brightness
L	L	L	100.00 %
L	L	H	87.50 %
L	H	L	75.00 %
L	H	H	62.50 %
H	L	L	50.00 %
H	L	H	37.50 %
H	H	L	25.00 %
H	H	H	12.50 %

13 Reset and Initializing flow chart

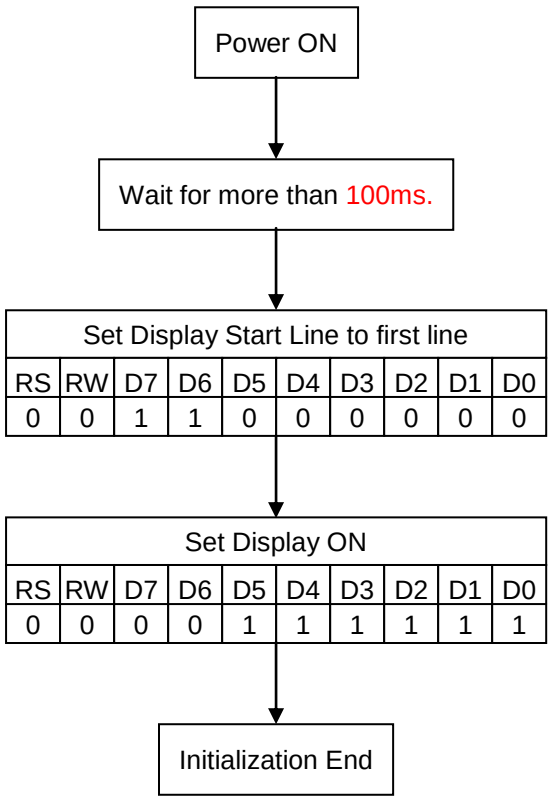
13.1 Reset

The system can be initialized by setting *RST terminal at low level when turning power on, receiving instruction from CPU.
When *RST becomes low, following procedure is occurred.
— Display off
— Display start line register become set by 0. (Z-address 0)
While *RST is low, No instruction except status read can be accepted. Therefore, execute other instructions after making sure that DB4 = 0 (clear *RST) and DB7 = 0 (ready) by status read instruction.
The Conditions of power supply at initial power up are shown as follow.



Reset: Refer to "12.2.5 Status Read".

13.2 Initializing flow chart



14 Display Data RAM map

Pages (X Address)	Lines (Z Address)	Column Address (Y Address) (0~63)													Data
1st page (X=0)	Line 0→	0	1	1	1	0	0	…..	0	0	1	0	0	0	←DB0 (LSB)
	Line 1→	1	0	0	0	1	0	…..	0	0	1	1	0	0	←DB1
	Line 2→	1	0	0	0	1	0	…..	0	0	1	0	1	0	←DB2
	Line 3→	1	0	0	0	1	0	…..	0	0	1	0	1	0	←DB3
	Line 4→	1	1	1	1	1	0	…..	0	0	1	0	0	0	←DB4
	Line 5→	1	0	0	0	1	0	…..	1	1	1	0	0	0	←DB5
	Line 6→	1	0	0	0	1	0	…..	1	1	1	0	0	0	←DB6
	Line 7→	0	0	0	0	0	0	…..	0	0	0	0	0	0	←DB7 (MSB)
2nd page (X=1)	Line 8→	1	1	1	1	0	0	…..	0	1	1	1	0	0	←DB0 (LSB)
	Line 9→	1	0	0	0	1	0	…..	0	1	0	0	1	0	←DB1
	Line 10→	1	0	0	0	1	0	…..	0	1	0	0	1	0	←DB2
	⋮	1	1	1	1	0	0	…..	1	1	1	0	1	0	←DB3
		1	0	0	0	1	0	…..	0	1	0	0	1	0	←DB4
		1	0	0	0	1	0	…..	0	1	0	0	1	0	←DB5
		1	1	1	1	0	0	…..	0	1	1	1	0	0	←DB6
	Line 15→	0	0	0	0	0	0	…..	0	0	0	0	0	0	←DB7 (MSB)
…..	⋮							⋮							
8th page (X=7)	Line 56→	1	0	0	0	1	0	…..	0	0	0	0	0	0	←DB0 (LSB)
	⋮	1	0	0	0	1	0	…..	0	0	0	0	0	0	←DB1
		1	0	0	0	1	0	…..	0	1	0	0	1	0	←DB2
		1	1	1	1	1	0	…..	1	0	1	0	1	0	←DB3
		1	0	0	0	1	0	…..	1	0	0	1	0	0	←DB4
		1	0	0	0	1	0	…..	1	0	0	1	0	0	←DB5
	Line 62→	1	0	0	0	1	0	…..	0	1	1	0	1	0	←DB6
	Line 63→	0	0	0	0	0	0	…..	0	0	0	0	0	0	←DB7 (MSB)

		Left area (CS1=1)							Right area (CS2=1)						
Pages	Lines	0	1	2	3	…..	62	63	0	1	2	3	…..	62	63
X=0	Line 0 : Line 7	DB0 : DB7						DB0 : DB7	DB0 : DB7						DB0 : DB7
⋮	Line 8 : Line 55	⋮						⋮	⋮						⋮
X=7	Line 56 : Line 63	DB0 : DB7						DB0 : DB7	DB0 : DB7						DB0 : DB7

Notice for the Cautious Handling of VFD Modules

Handling and Usage Precautions:
Please carefully follow the appropriate product application notes and operation standards for proper usage, safe handling, and maximum performance.

[VFD tubes are made of glass]

- The edges of the VFD glass envelope are not smooth, so it is necessary to handle carefully to avoid injuries to hands.
- Use caution to avoid breaking the VFD glass envelope, to prevent injury from sharp glass particles.
- The tip of the exhaust pipe is fragile so avoid shock from impact.
- It is recommended to allow sufficient open space surrounding the exhaust pipe to avoid possible damage.
- Please design the PCB for the VFD module within 0.3 mm warping tolerance to avoid any forces that may damage the display due to PCB distortion causing a breakdown of the electrical circuit leading to VFD failure.

[High voltage]

- Avoid touching conductive electrical parts, because the VFD module uses high voltage exceeding 30 – 100 volts.
- Even when electric power is turned off, it may take more than one minute for the electrical current to discharge.

[Cable connection]

- Do not unplug the power and/or data cables of VFD modules during operation, because unrecoverable damage may result.
- Sending input signals to the VFD module when not powered can cause I/O port damage.
- It is recommended to use a 30cm or shorter signal cable to prevent functional failures.

[Electrostatic charge]

- VFD modules need electrostatic-free packaging and protection from electrostatic charges during handling and usage.

[Structure]

- During operation, VFD and VFD modules generate heat. Please consider sufficient heat radiation dissipation using heat sink solutions.
- Preferably, use UL-grade materials or components in conjunction with VFD modules.
- Warp and twist movement causes stress and may break VFDs and VFD modules. Please adhere to allowances within 0.3mm at the point of attachment.

[Power]

- Apply regulated power to the VFD module within specified voltages to protect from failures.
- VFD modules may draw in-rush current exceeding twice the typical current at power-on, so a power supply with sufficient capacity and quick starting of the power regulator is recommended.
- VFD module needs a specified voltage at the point of connection. Please use an adequate power cable to avoid a decrease in voltage. As a safety measure, a fuse or other over-current protection is recommended.

[Operating consideration]

- Illuminating phosphor will decrease in brightness during extended operation. If a fixed pattern illuminates for an extended period (several hours), the phosphor efficiency will decrease compared to the non-operating phosphor, causing non-uniform brightness. Please consider programming the display patterns to use all phosphor segments evenly. Scrolling may be a consideration for a period of time to refresh the phosphor condition and improve even illumination of the pixels.
- A signal cable 30cm or less is recommended to avoid possible disturbances to the signal.

[Storage and operating environment]

- Please use VFD modules under the recommended specified environmental conditions. Salty, sulfuric and dusty environments may damage the VFD module even during storage.

[Disposal]

- VFD uses lead-containing materials (RoHS directive exempts these lead compounds in the glass for electronic devices). When discarding VFDs or VFD modules, please adhere to applicable laws and regulations.

[Other cautions]

- Although the VFD module is designed to be protected from electrical noise, please plan your circuitry to exclude as much noise as possible.
- Do not reconstruct or repair the VFD module without our authorization. We cannot assure the quality or reliability of unauthorized reconstructed VFD modules.

Notice:

- We do not authorize the use of any patents that may be inherent in these specifications.
- Neither whole nor partial copying of these specifications is permitted without our approval. If necessary, please ask for assistance from our sales consultant.
- This product is not designed for military, aerospace, medical or other life-critical applications. If you choose to use this product for these applications, please ask us for prior consultation or we cannot accept responsibility for problems that may occur.

MBBZ-009-S18A

Revision Note

Specification No.	Date	Revision
DS-1702-0000-00	Feb. 08, 2012	Initial issue.
DS-1702-0000-01	Mar. 07, 2012	·11 Timing Characteristics All timing diagrams have been revised. ·12.2.4 Display Start Line (Z Address) "When the display duty cycle is 1/64 or others (1/32~1/64), the data of total line number of LCD screen, from the line specified by display start line instruction, is displayed." ↓ "The data of total line number of display screen from the line specified by this instruction is displayed. This instruction is used for scrolling of the display screen." ·12.2.5 Status Read ON / OFF: When ON/OFF is 1, the ~~display is on~~. → display is off When ON/OFF is 0, the ~~display is off~~. → display is on In addition, the correction of errors etc. at all pages.