FH | JOANNEUM
Electronics and
Computer Engineering

Development of a Permittivity-Meter

Characterization of Snow by the Determination of Permittivity

Master's Thesis

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Abstract

This thesis focuses on the design and implementation of a Permittivity-Meter dedicated to characterizing snow samples by determining their relative permittivity. The measurement of complex relative permittivity is achieved using a specifically devised Notch filter circuit incorporating a resonant frequency characteristic initially proposed by A. Denoth in 1994. A prior master's thesis has substantiated the validity of the original Denoth Meter concept. Building upon this foundation, the present work aims to leverage acquired knowledge to develop a handheld prototype. This prototype integrates a single board encompassing a sensor unit, measurement circuits, and a microcontroller serving as the processing unit. The proposed methodology employs undersampling for a high-frequency signal processing approach. Multiple electrical circuits are imperative for the implementation, with particular emphasis on integrating a switchable gain amplifier essential for measuring the extensive magnitude range of the signal. In addition to circuit board design, the creation of firmware for the microcontroller is a crucial aspect. The firmware is designed to execute measurements automatically and furnish results through a user-accessible interface, accessible via USB or Bluetooth.

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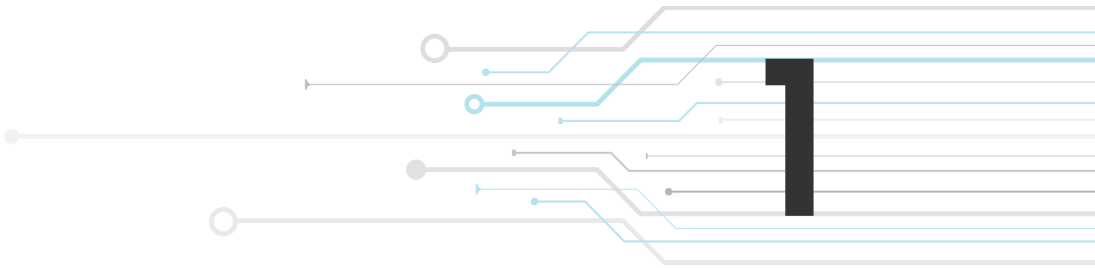

1 Introduction

1.1 Motivation

The following thesis is built upon the thesis from Stefan Dierer [4], with a focus on proving the concept of the Permittivity Meter initially published by A. Denoth in 1989 [5]. The Permittivity Meter allows the determination of the relative permittivity of snow, seen as a complex quantity. The resonant circuit concept from Denoth is designed to expose the sensor unit to snow, which leads to a detuning of the circuit. Detunign means changes in the quality factor and resonant frequency in this case. The thesis of S. Dierer concluded that Denoth's concept works and that the real and the imaginary part of the relative permittivity can be determined. The implementation of Dierer was limited to a small test board containing a lowpass filter, an amplifier circuit and the actual notch filter, which allows hardware measurements under laboratory conditions with external equipment. The following thesis should go further to develop an easy-to-use handheld device.

1.2 Properties of Snow and the measurable Physical Quantities

According to [6], snow can be seen as a heterogeneous dielectric material consisting of three main components: ice, air and water, whereby the individual component's contribution to snow's properties depends heavily on the type of snow. Dry snow has no significant water content part. Therefore, the water does not contribute to the physical properties, whereas the properties of wet snow are highly dependent on the water content. As snow is a dielectric quantity, the permittivity measurement can be used to determine different types of snow. In [5], the dependence of relative permittivity ϵ_r by frequency has been proven through practical experiments. At frequencies higher than a few MHz, ϵ_r becomes independent from frequency and remains constant up to the GHz range.

The permittivity of snow must be interpreted as a complex quantity. The real part describes

the relative permittivity and the imaginary part $Im\{\epsilon_r\} = \epsilon_r^{''}$ the losses. The losses are encountered by dielectric losses and by losses due to ionic conductivity [7].

$$\epsilon_r = \epsilon_r^{'} - j\epsilon_r^{''} \tag{1.1}$$

In the frequency range of 10MHz, only a small influence of snow wetness regarding $\epsilon_r^{''}$ can be seen. The major effect on $\epsilon_r^{''}$ is mainly coming from snow texture and the effect of ionic conductivity. Snow porosity Φ can be explained by equation 1.2 in case of dry snow and $\Phi \geq 0.3$ [5].

$$\epsilon_d^{'} = 1 + 1.76(1 - \Phi) + 0.37(1 - \Phi)^2 \qquad [5] \tag{1.2}$$

In case of wet snow, the incremental permittivity $\triangle\epsilon^{'}$ is defined by Eq. 1.3 and $\epsilon^{'}(wet)$ can be rewritten by Eq. 1.4, with ρ as density of wet snow. The incremental permittivity indicates the variation in relative permittivity based on varying water content levels. It can be seen that the relative and especially the incremental permittivity depends on the volumetric water content W in percentage, the density p and the porosity Φ. These equations are valid for a frequency from MHz to sub-GHz range. [5]

$$\triangle\,\epsilon^{'} = \epsilon^{'}(wet) - \epsilon_d^{'} \qquad [5] \tag{1.3}$$

$$\epsilon^{'}(wet) = 1 + 1.92p + 0.44p^2 + 0.187W + 0.0045W^2 \qquad [5] \tag{1.4}$$

Snow porosity can be calculated by 1.5, where ρ is related to snow, ρ_W to water at 0°C and ρ_i to ice density.

$$\Phi = 1 - (\rho - \rho_W.W)/\rho_i \qquad [5] \tag{1.5}$$

Austin Kovacs mentions an alternative approach for the relation between relative permittivity and snow density [7]. Through empirical determination, they could form Eq. 1.6, with measurements in the radio-frequency range. Hence, the relative permittivity ϵ_r' for frequencies beyond the sub-MHz range is independent of frequency, Eq. 1.6 is valid for 20 MHz too and can therefore also be used for computing the density of the snow samples out of the determined ϵ_r' from the Permittivity Meter.

$$\epsilon_r^{'} = (1 + 0.851\rho)^2 \qquad [7] \tag{1.6}$$

Dedicated equations for the imaginary part of the relative permittivity are not available in these amounts. However, it is evident that in the case of a high water content, the polarization losses are high too, corresponding to a higher ϵ_r''. The relative permittivity of liquid water at 0 °C is given by $\epsilon_r = 88 - j9.8$, measured at 1 GHz [8]. In contrast, the relative permittivity of ice is $\epsilon_r = 3.15 - j0.0001$ [9]. Ari Siholva and Martti Tiuri [8] summarized results from previous measurements [10]. According to [10], the imaginary part is directly related to the wetness (but only in the GHz range, where the ionic conductivity is not present). However, the real part depends on the density and wetness. The measured ϵ_r'' can be used to determine the water content of snow by Eq. 1.7 in the GHz frequency range.

$$\epsilon''_{r,snow} = (0.10W + 0.80W^2)\epsilon''_{r,water} \qquad [10] \tag{1.7}$$

In conclusion, one can say that the imaginary part can be neglected in case of dry snow.[5] Therefore, the ϵ_r' can be used to determine the snow density. On the other hand, the water content influences both the real and the imaginary part or relative permittivity.[9].

1.3 Project Target

As explained, a handheld prototype is the primary goal of the following project. The realization of such a device covers multiple details that need to be solved first. The notch filter circuit is designed for an input frequency of 20 MHz, leading to problems regarding signal digitalization. In contrast to the original concept from Denoth, which uses a frequency mixer to lower the high-frequency signal, the following thesis will use the undersampling approach for digitalization. A two-stage amplifier circuit is designed to accomplish a wide range of signal amplitudes, with the possibility of individually turning the gain stages on or off. A state-of-the-art user interface, consisting of a Universal Serial Bus (USB) and Bluetooth interface for sending commands to the device or receiving measurement results, is also part of the work. A central microcontroller unit performs the processing tasks, and to ensure rapid development and easy firmware debugging, a microcontroller development board is used.

1.4 Requirements for the Permittivity Meter as Handheld Device

The handheld device's requirements should describe the device's product features and the kind of implementation, which leads to a separation into functional and non-functional requirements.

The functional requirements describe the product features and the non-functional implementation-related requirements.

Functional Requirements

- User interaction via USB and Bluetooth connection, status LED, optionally visualization via LCD
- Low power consumption, µA region for sleep state, shutdown of all peripheral devices (radio module, Operational Amplifier (OpAmp)s)
- Measurement with 20 MHz sinusoidal input signal
- Measurement of the real and imaginary parts of the relative permittivity
- Providing a calibration procedure

Non-functional Requirements

- Use of undersampling for signal acquisition
- Main clock signal must be greater than 20 MHz otherwise undersampling is impossible
- Use of a 16 or 32-bit microcontroller (either MSP430 or STM32)
- Minimal Analog-to-Digital Converter (ADC) resolution of 12-bit
- Usage of a microcontroller development board
- 5V supply voltage
- Two Digital-to-Analog Converter (DAC)s for varactor-diodes controlling
- Multiple switchable gain stages for using the full range of ADC reference voltage

2 Concept

2.1 Measurement Principle to Determine the Permittivity

Different measurement principles are possible for the determination of the relative permittivity of snow. In [11], different dielectric sensors for measuring the liquid water content of snow are compared and described in their functionality. The measurement principle for this project is based on the Permittivity Meter developed by A. Denoth [1].

The measurement setup consists of a flat capacitive sensor that allows near-surface and volume measurements. FR4 material is used as a carrier, and a copper layer is placed on both the top and bottom sides of the capacitive sensor. Figure 2.1 shows is the original sensor unit from A. Denoth [1] and illustrates that the electric field propagates between the inner and outer electrodes. The inner electrode is directly connected to a twin-measurement T-bridge, whereas the outer electrode is connected to ground potential. The backplane can be connected to ground potential or otherwise free-floating. The numerical values of the measurement bridge components, especially the capacitor, inductor and resistor values, are chosen for a specific frequency. Hence, the T-bridge, classified as a band-stop or notch filter, has its strongest attenuation at around $f = 20\,\mathrm{MHz}$. Therefore, a sinusoidal signal with a frequency of $f = 20\,\mathrm{MHz}$ is used as input. Changes in the relative permittivity of the exposed measurement medium lead to a difference in the notch filter's frequency response. The actual designed schematic from A. Denoth is visible in Fig. 2.2.

2.1.1 Notch Filter as Measurement Bridge

The central pillar of the measurement concept is tuning the notch filter so that the identical frequency response of the filter is achieved as in the calibration process. Calibration is done with a specific medium, preferably by air with $\epsilon_r = 1$ and at a particular temperature, ideally at the ambient temperature where the subsequent measurement will take place. Tuning of the filter is

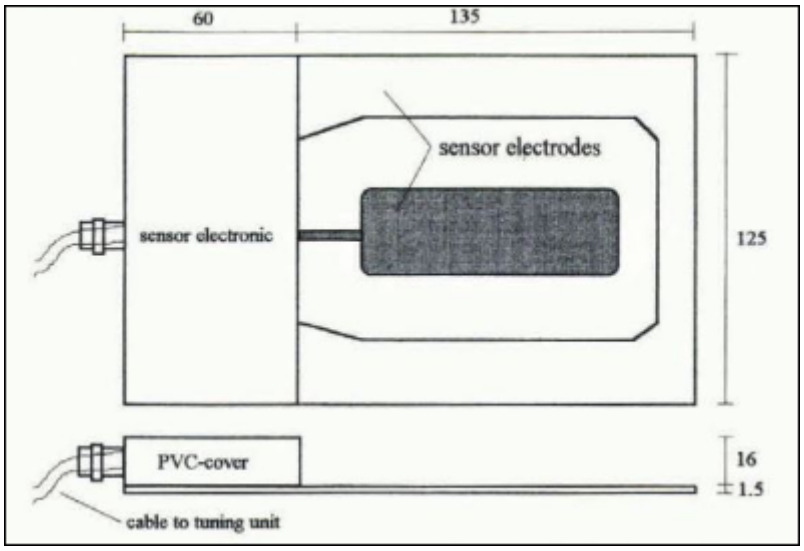

Figure 2.1: Original sensor unit from A. Denoth published in [1]

capable via two varactor diodes, which allows a voltage-controlled variation of the diode capacitance in the range of approximately $2pF < C_d < 30pF$. The actual diode capacitance depends on the manufacturer and the varactor diode used.

The concept of the notch filter itself is discussed in great detail by the master thesis of Stefan Dierer [4], where the focus was set on proofing the measurement concept of A. Denoth [1]. This concept proof includes a detailed investigation of the measurement bridge schematic and its operation, starting with Spice simulations and ending with a real laboratory test setup. The thesis shows that the measurement principle by A. Denoth can detect changes in the material properties exposed by the sensor through changes in the propagation of the electric field, especially by changes in the relative permittivity ϵ_r. The differentiation between real and imaginary parts of ϵ_r is possible because of distinguishable effects on the notch filter frequency response.

Under normal circumstances, when calculating the capacitance of a plate capacitor as shown in Eq. 2.1, the absolute permittivity consists of the relative ϵ_r and the vacuum permittivity ϵ_0.

$$C = \epsilon \frac{A}{d} = \epsilon_0 \cdot \epsilon_r \frac{A}{d} \tag{2.1}$$

In the case of dielectric losses in the material, like given for snow, the relative permittivity must be extended to a complex quantity, where the imaginary part correlates to the dielectric losses in the material. Dielectric losses can be interpreted as additional resistance, which is placed in parallel to the capacitance of the sensor. Ideally, when dry snow is used as a probe, the imaginary part of ϵ_r is zero, which means an infinite high electrical resistance. With higher dielectric losses,

the resistance will decrease. According to the literature, polarization losses of snow are in the range of $0.01 < \epsilon_r'' < 0.4$. The impedance of the sensor unit during measurement can be described with Eq. 2.2, the corresponding admittance by Eq. 2.3. In this case, the capacitance of the sensor can be calculated by Eq. 2.4 and its related reactance is given by Eq. 2.5. The introduced factor $k_1 = \frac{A}{d} = \frac{C_{s,calib}}{\epsilon_0}$ describes the characteristic of the sensor during calibration time with $\epsilon_r = 1 + j0 = 1$, which corresponds to the permittivity of air.

$$Z_m = \frac{1}{sC_m + \frac{1}{R_m}} = \frac{R_m}{sC_m R_m + 1} \tag{2.2}$$

$$Y_m = \frac{1}{Z_m} = \frac{1 + sC_m R_m}{R_m} = \frac{1}{R_m} + sC_m \overset{s \to j\omega}{=} \frac{1}{R_m} + j\omega C_m \tag{2.3}$$

$$C_m = \epsilon \frac{A}{d} = \epsilon_0(\epsilon_r' - j\epsilon_r'')\frac{A}{d} = \epsilon_0(\epsilon_r' - j\epsilon_r'')k_1 = (\epsilon_r' - j\epsilon_r'')C_{s,calib} \tag{2.4}$$

$$X = \frac{1}{j\omega C_m} = \frac{1}{j\omega\epsilon_0(\epsilon_r' - j\epsilon_r'')k_1} = \frac{1}{j\omega\epsilon_0\epsilon_r' k_1 + \omega\epsilon_0\epsilon_r'' k_1} \tag{2.5}$$

$$Y = \frac{1}{X} = j\omega\epsilon_0\epsilon_r' k_1 + \omega\epsilon_0\epsilon_r'' k_1 \tag{2.6}$$

Now, equation 2.3 and 2.6 can be equated and a comparison of coefficients results in 2.7 and 2.8, where the first describes the relation between the imaginary part of ϵ_r and the electrical resistance, and the second one between the real part and the capacitance. As these two equations show, determining ϵ_r' and ϵ_r'' is possible in case R_m and C_m are somehow measured. It is also worth noting that the $C_{s,calib}$ only consists of the differential sensor capacitance, not the whole capacitance generated between the copper layers.

$$Re\{Y_m\} = Re\{Y\} = R_m = \frac{1}{\omega\epsilon_0\epsilon_r'' k_1} = \frac{1}{\omega\epsilon_r'' C_{s,calib}} \tag{2.7}$$

$$Im\{Y_m\} = Im\{Y\} = C_m = \epsilon_0\epsilon_r' k_1 = \epsilon_r' C_{s,calib} \tag{2.8}$$

Interpreting Eq. 2.8 concerning measurement ranges leads to the conclusion that the numerical value of the sensor capacitance $C_{s,calib}$ is significant. The sensor capacitance C_s is synonymous with C_{diff} from section 2.1.2. Snow samples with various values for ϵ_r will be multiplied with the initial sensor capacitance suspended to air. Therefore, a high initial value for C_s will result in a

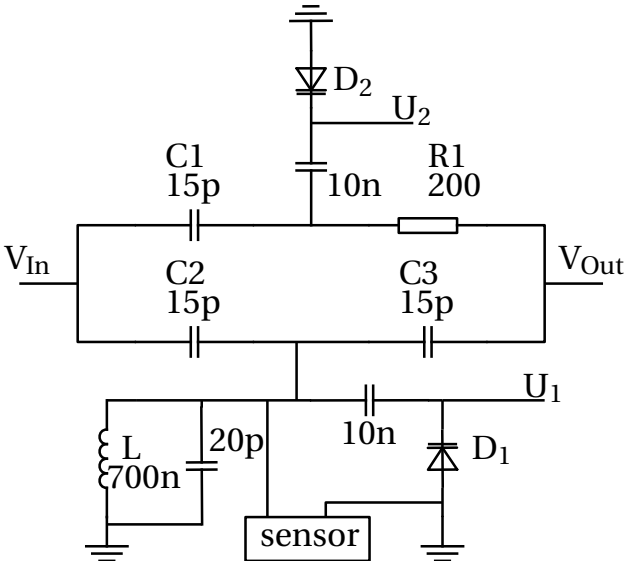

Figure 2.2: Notch filter schematic according to A. Denoth [1]

high measured capacitance C_m. Hence, the circuit must be tuned back to the initial characteristic to determine capacitance change, the diode must allow its capacitance to be reduced by the same value as C_s has increased. Consequently, the variation in C_s must fall within the range according to the possible capacitance fluctuations of the diode. Furthermore, the variation of diode capacitance will directly define the maximal measurable ϵ_r.

Equation 2.8 can be used later in section 2.3.2 to determine ϵ'_r. However, the derived equation 2.7 will not fully describe the determination of ϵ''_r. Hence, ϵ''_r will mainly influence the quality factor; a better way to determine ϵ''_r will be by using a mapping between quality factor change and ϵ''_r. The mathematical determination of the notch filter's quality factor with nominal component values is impractical because minimal changes in the ohmic resistance of the inductor will influence the quality factor heavily, as seen later on during simulations (section 3.1). Therefore, further investigations are necessary to provide a possibility to calculate ϵ''_r out of the available measurement quantities.

2.1.2 Composition of the Sensor Capacitance

Due to the structure of the sensor unit, consisting of FR4 core material with a thickness of $d = 1.55\,\text{mm}$ and copper polygons, which are not connected electrically but coupled capacitively, plate capacitors are introduced, with a relative permittivity of $\epsilon_r \approx 4$. The following capacitances visible in Fig. 2.3 represent the sensor unit Printed Circuit Board (PCB). Note, a major difference between C_{diff} and C_A and C_B is their relative permittivity ϵ_r. C_A is located between the inner

front electrode and the backplane, whereas C_B is between the rear copper polygon and the outer electrode on the top layer, but both capacitances are between layers; thus, the relative permittivity is the one of FR4 material.

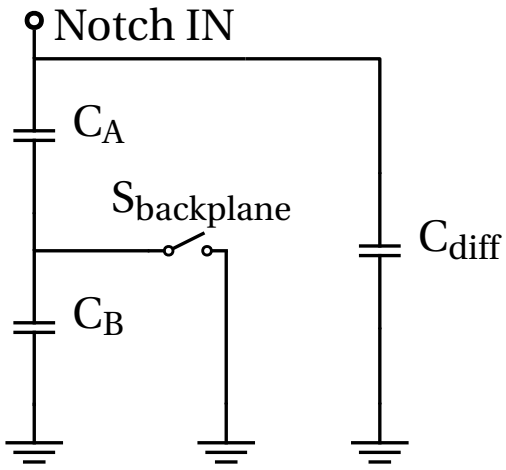

Figure 2.3: Composition of sensor capacitances; C_A and C_B are located between the top and bottom layer, C_{diff} can be seen as the differential capacitance between the inner and outer electrode, will be affected by changes of ϵ_r.

In contrast, C_{diff}, the measurement or calibration capacitance, is between the inner and outer top layer electrode. Therefore, this capacitance will be affected by ϵ_r changes due to the exposed medium to the sensor unit. In other words, the capacitances C_A and C_B will not directly influence the measurement (can be seen as offset capacity) but will affect the resonant frequency of the notch circuit. In the case of a floating backplane connection, C_A and C_B are in series, leading to a capacitance reduction and further increasing the resonant frequency. Connecting the rear polygon to the ground will short C_B.

2.2 Notch Filter Simulations

The notch filter basics were already discussed in chapter 2.1. However, the complex operational principle should now be analyzed in greater detail. In particular, the properties that will later have a major influence on the implemented notch filter are to be investigated. Critical component values that need to be considered during implementation should be determined. The parasitic effects should be kept in mind primarily. To concentrate on the basic operational principle, the circuit used for simulation shown in Fig. 2.4 was reduced to the essential components, meaning to replace the varactor diodes with equivalent capacitors C_{D1} and C_{D2} and to combine the parasitic capacitance of the PCB and the exposed capacitance on the sensor unit into C_{sens}.

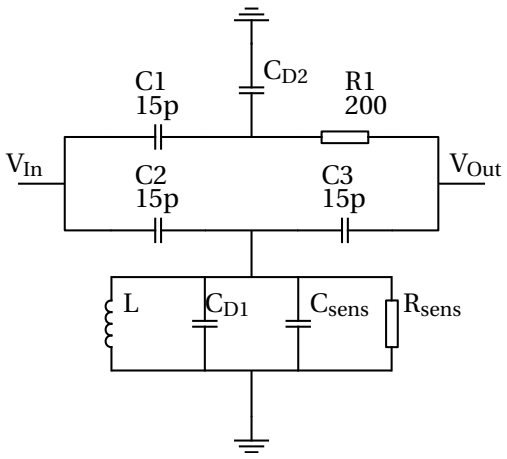

Figure 2.4: Used notch circuit schematic for simulation; circuit structure was reduced to the essential components

2.2.1 Notch Filter's Transfer Function

In order to allow simulations in Matlab too, a Laplace transfer function can be derived from the given circuit in Fig. 2.4. Hence, the master thesis of S. Dierer [4] discusses the derivation process in detail; the final result of the notch filter's transfer function derivation is used here and is visible in Eq. 2.9, where Z_1 (Eq. 2.10) is the equivalent circuit for the lower and Z_2 (Eq. 2.11) the one for the upper T branch. The inductor L is extended by its series ohmic resistance $R_{L,s}$.

$$H(s) = \frac{\frac{sC_1}{sRC_1+1+\frac{R}{Z_2}} + \frac{s^2C_2C_3}{s(C_3+C_2)+\frac{1}{Z_1}}}{-\frac{\frac{1}{R}}{sRC_1+1+\frac{R}{Z_2}} + \frac{1}{R} - \frac{s^2C_3^2}{s(C_3+C_2)+\frac{1}{Z_1}} + sC_3} \tag{2.9}$$

$$Z_1(s) = \frac{1}{\frac{1}{R_{sens}} + s(C_{sens}+C_{D1}) + \frac{1}{R_{L,s}+sL}} \tag{2.10}$$

$$Z_2(s) = \frac{1}{sC_{D2}} \tag{2.11}$$

The behavior of the notch filter can be described by the bode diagram shown in Fig. 2.5, which is generated with the help of the Laplace transfer function from Eq. 2.9. A characteristic of a notch filter is its narrow stop band in the frequency domain, which means only a thin frequency band is attenuated. A closer look at the bode diagram shows something like a resonance frequency, where the capacitance is dominant for lower frequencies and the inductance is dominant for frequencies higher than the resonant frequency, as seen in the phase diagram from Fig. 2.5. The observed behavior and their interpretation leads to further investigations in the following section.

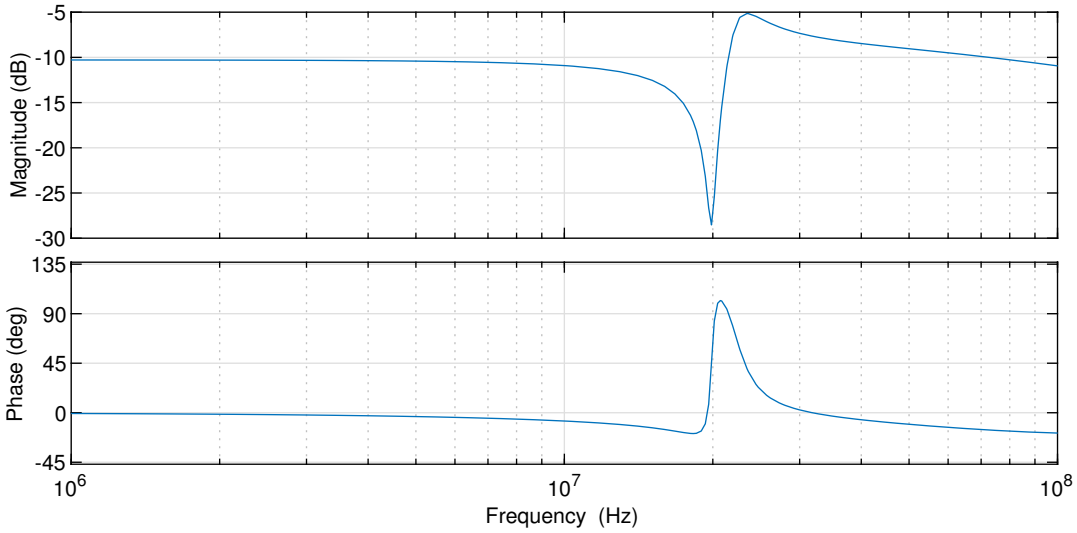

Figure 2.5: Bode diagram of notch filter, generated via Laplace transfer function in Matlab according to Eq. 2.9

2.2.2 Interpretation of Notch Filter Behavior

Due to the rather complex transfer function in Eq. 2.9, a simplified description of the filter behavior is an expedient solution. Interpreting the bode plot from Fig. 2.4 leads to the conclusion that the filter behaves partly like an inverted frequency response of a parallel resonant circuit, with a maximal attenuation at a frequency of $f = 20\,\mathrm{MHz}$.

Interpretation as Parallel Resonant Circuit

To be more precise, the lower T branch is basically a parallel resonant circuit with L, C_{sens} and R_{sens}. Their frequency behavior is visible in Fig. 2.6.

Changing the size of the inductance (L) or the capacitance values (C_{sens}, C_{D1}) causes a drift in the resonant frequency, described by the resonant frequency of a parallel resonant circuit in Eq. 2.12. On the one hand, a lower inductance or capacitance will increase the resonant frequency; on the other hand, a higher capacitance or inductance value will decrease it.

$$f_r = \frac{1}{2\pi\sqrt{LC}} \tag{2.12}$$

The circuit's ohmic resistance (here R_{sens} and $R_{L,s}$) will not move the band stop in the frequency domain but will influence the depth of the magnitude in the band stop. The quality factor of a parallel resonant circuit describes this influence and can be determined by Eq. 2.13. A high ohmic

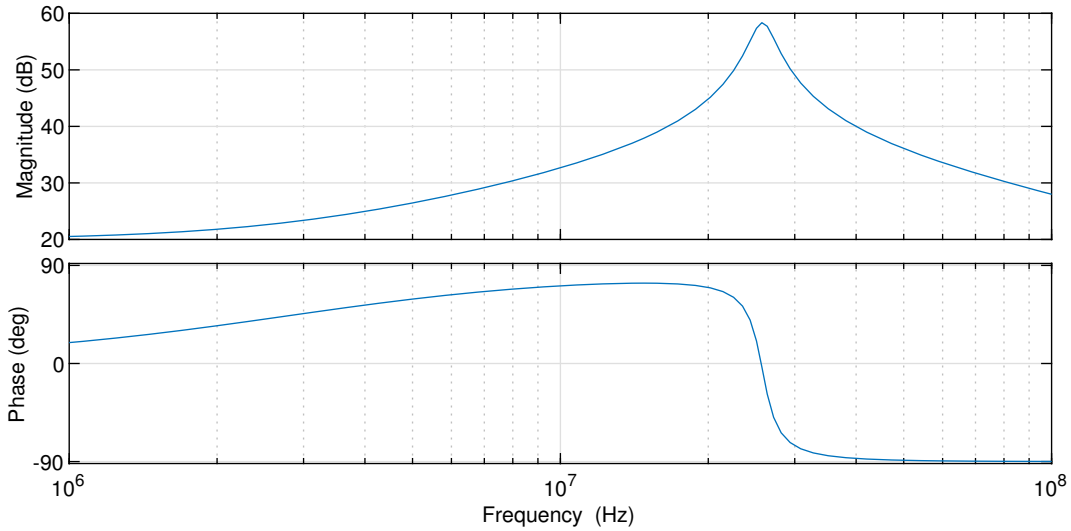

Figure 2.6: Bode diagram of the parallel resonant circuit Z_2 in the lower T branch, generated via Laplace transfer function in Matlab according to Eq. 2.10

resistance of R_{sens} will not influence the circuit, whereas a lower ohmic resistance will influence the parallel circuit of L, C_{sens} and C_{D1} heavily.

If the notch only consists of a simple parallel resonant circuit, a lowered ohmic resistance will consequently lower the quality factor according to Eq. 2.13. Nevertheless, this statement is only valid for a pure parallel resonant circuit! Hence, the given notch circuit is more than just the parallel resonant circuit formed by L, C_{sens} and C_{D1}, Eq. 2.13 is not suitable to describe the quality factor of the notch.

An alternativ approach for the quality factor Q can be defined via Eq. 2.15, where the -3 dB bandwidth of the resonant curve is used from Eq. 2.3. Combining both approaches, it is seeable that a lower quality factor increases the bandwidth and lowers the depth of the curve. In contrast, a high-quality factor creates a sharp band stop behavior, implying a small bandwidth and a deep curve.

$$Q = R\sqrt{\frac{C}{L}} \tag{2.13}$$

$$B = f_u - f_l \tag{2.14}$$

$$Q = \frac{f_0}{B} \tag{2.15}$$

Interpretation regarding Measurement of the relative Permittivity

The described behavior of the notch filter suggests how the filter can be used for measuring the relative permittivity of different materials, including a measurement of both, the real and imaginary parts of the relative permittivity interpreted as complex quantity. A calibration process for a relative permittivity of $\epsilon_r = \epsilon_r' + j\epsilon_r'' = 1 + 0j$ describes the initial situation. A later measurement will change the frequency behavior of the resonant circuit. The measurement is then performed by tuning the varactor diodes to return the circuit's behavior to the initial state. More precisely, the relative change in the quantity of the adjusting variables can then be used to determine the changes in the relative permittivity through calculations.

Changes in the real part of the relative permittivity ϵ_r' imply a change in the capacitance of the electrode sensor unit and furthermore a drift in the resonant frequency. Tuning the resonant circuit to return to the original frequency response can be done by inductance or capacitance change. Hence, the value of the inductor cannot be changed, the capacitance must be tuned, which is possible using varactor diodes.

In contrast, the imaginary part of the relative permittivity ϵ_r'' is linked to the ohmic resistance of the circuit and further to the quality factor. A ϵ_r'' unequal to zero will add a significant ohmic component, where significant in this case means a low ohmic resistance value. A lower ohmic resistance will influence the quality factor for sure. However, it is wrong to say that a lower ohmic resistance reduces the quality factor, as can be seen in Eq. 2.13. Upcoming simulations and measurements will show that a lower ohmic resistance can lead to different changes in the quality factor, including an increase and decrease (Fig. 2.9, Fig. 2.10). The sign of the change depends strongly on the varactor diode capacitance C_{D2} in the upper T-branch.

2.2.3 Notch Filter in Detail

Influence of the Indcutor's Ohmic Resistance on the Notch

A first simulation investigates the influence of the ohmic resistance of the inductor, which is generally given by the manufacturer and is noted at DC level. Measurements by the thesis of [4] showed dramatically deviating values for this ohmic resistance. The skin effect contributes to increased ohmic resistance for higher frequencies. Due to a specific penetration depth at 20 MHz, the current flow is not able in the entire cross-section of the coil wires. According to [4], the ohmic resistance at 20 MHz will be increased by a factor of 6.7 compared to DC level for a wire diameter $d = 0.2\,\text{mm}$ and copper as material.

The simulation results of Fig. 2.7 show an interesting behavior, especially in the phase plot. The simulation sweeps over various values for the ohmic resistance of the inductor with an interval of [1...14.5]Ω. The consequences of the sweep are different depths of the band stop in the frequency domain, which is equal to different quality factors. Starting with a lower quality factor, the quality factor is increased until reaching a maximum at $R_{Ls} = 4\Omega$. A further increase in ohmic resistance will decrease the quality factor again and lead to the worst quality factor during the sweep.

A detailed look at the phase plot helps to understand this behavior. The capacitive part of the resonant circuit is present before reaching the resonant point, whereas the inductivity takes over for frequencies beyond. Sweeping through the resonant frequency is synonymous with rotating on the unit circle, starting in the lower capacitance half and reaching the upper half for frequencies greater than the resonant point. The way of reaching the other half is either through clockwise or counterclockwise rotation. This process of rotation is precisely seen in the phase plot in Fig. 2.7, where the ohmic resistance of the inductor influences the rotation direction. This knowledge will be needed later during measurement because tuning the circuit will affect the rotation direction.

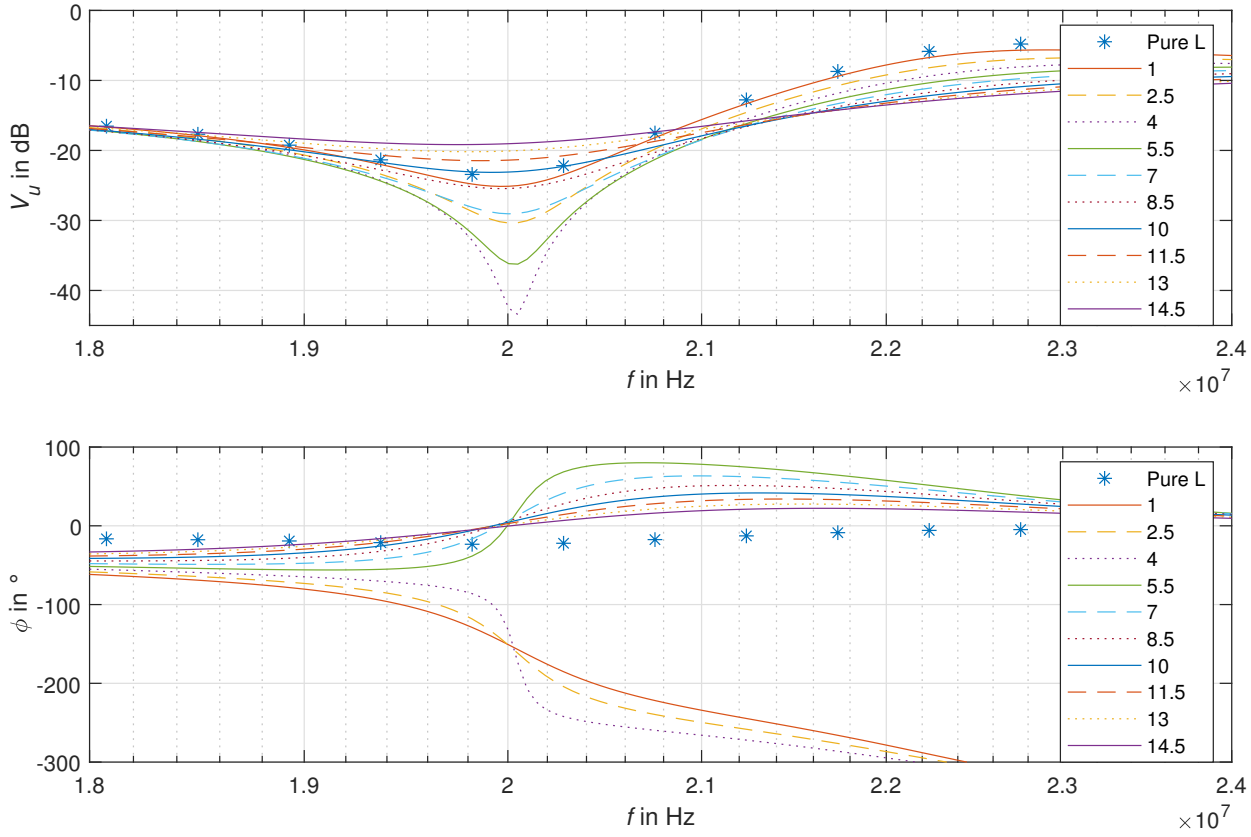

Figure 2.7: Simulation with different ohmic resistances of inductor L; $C_{D1} = C_{D2} = 20pF$, $C_{sens} = 48pF$, $R_{meas} = 100k$, Spice model 1008Hs-561 from Coilcraft with nominal L of $L_{nom} = 550n$ used, "Pure L" uses a $L_{nom} = 550n$ without parasitics

Influence of parallel Sensor Resistances

The following simulation investigates the notch filter behavior when the relative permittivity also consists of an imaginary part. Such an imaginary part can be imitated by adding parallel resistances to the sensor unit, which means that the resistance in the parallel resonant circuit is lowered. Usually, one would expect the quality to drop with smaller resistance values. However, the opposite is seen in Fig. 2.8. First, by reducing the resistance value, the amplitude gets lowered (higher quality factor), but after a specific resistance value, the amplitude rises.

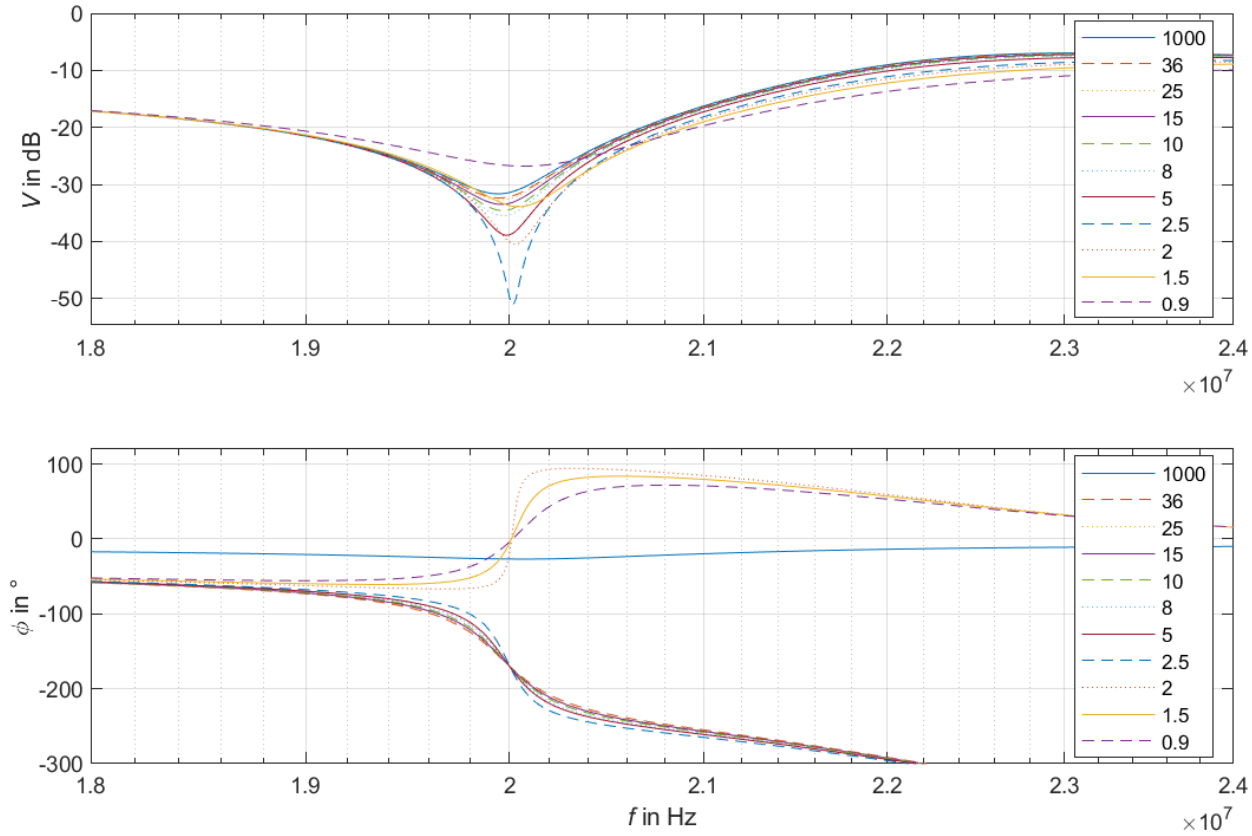

Figure 2.8: Simulation with different parallel resistances to the sensor unit, resistance values in kΩ; L; $C_{D1} = C_{D2} = 21pF$, $C_{sens} = 48pF$,$L = 550n$

Figure 2.9 was created to illustrate the effect in a better way. Therefore, the simulated amplitude values at 20 MHz were plotted with actual measurement data of the later-developed notch circuit. The interpretation of the Figure starts on the right side, where the parallel resistance is high. The resistance is decreased by going to the left side, which should lower the quality factor. Indeed, the quality is first rising, but with a change in the quality factor's growth sign around 2.7 kΩ, the quality is decreasing as expected. Note that an offset of 25dB moved the measurement values to

enable a more accurate comparison between the two curves.

In contrast to Fig. 2.9, the diode capacitance D2 is reduced to $C_{D2} = 9\,\text{pF}$ (equal to apply 5V to the varactor diode) in Fig. 2.10. Consequently, the quality factor is continuously decreasing when the resistance is lowered. This observation is also identical for simulation and measured resistances. Additionally, the simulation showed how the inductor's series resistance influences the curve's gradient. By reducing the series resistance to $R_L = 5\,\Omega$, the measurement results and those of the simulation coincide better. Figure A.6 shows how a low ohmic parallel resistance could be compensated by tuning the D2 diode (increasing the diode capacitance) in order to get the same amplitude value as at calibration time.

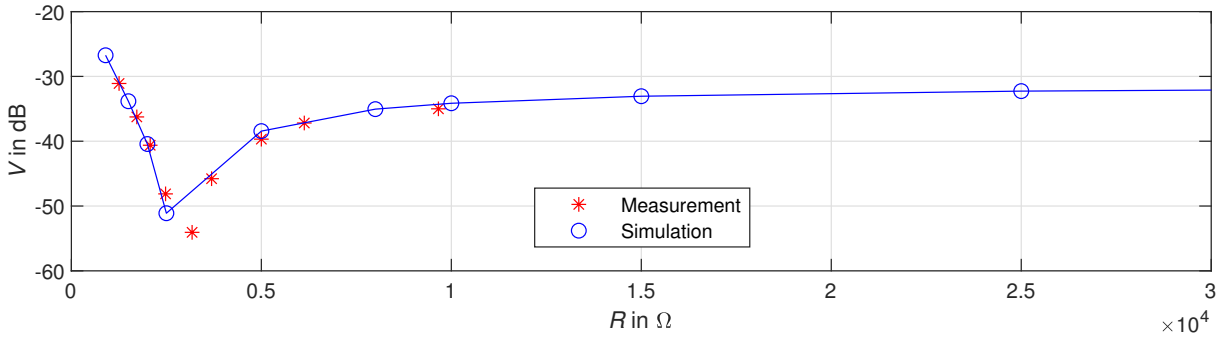

Figure 2.9: Influence on signal amplitude through different sensor resistances. Comparison between signal amplitudes for simulation and measurement; Simulation with: L; $C_{D1} = C_{D2} = 21\,\text{pF}$, $C_{sens} = 48\,\text{pF}$, $L = 550\,\text{nH}$, $R_L = 6.5\Omega$ (R_L is a synonym for $R_{L,s}$)

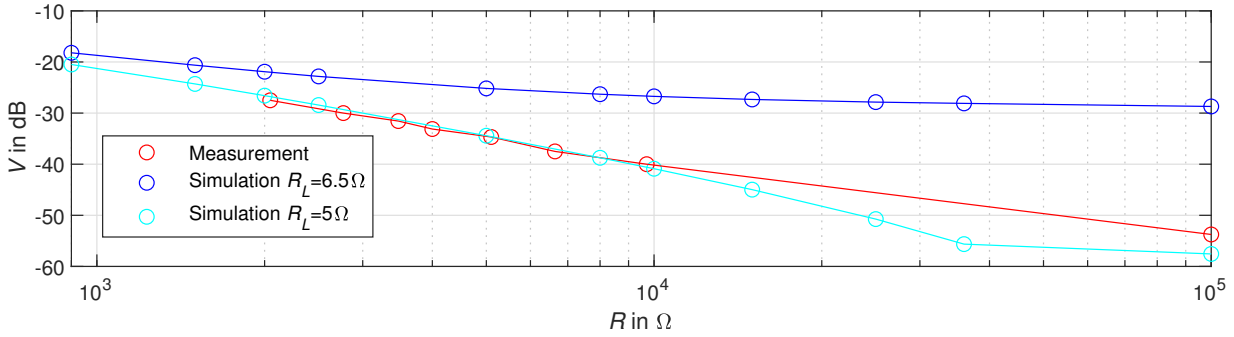

Figure 2.10: Influence on signal amplitude through different sensor resistances. Comparison between signal amplitudes for simulation and measurement with later designed notch circuit; Simulation with: L; $C_{D1} = 21\,\text{pF}$, $C_{D2} = 9\,\text{pF}$, $C_{sens} = 48\,\text{pF}$, $L = 550\,\text{nH}$

2.3 Determination of relative Permittivity through Tuning Process

2.3.1 Variable Capacitance through Varactor Diodes

The usage of varactor diodes can be observed, especially in applications where frequency tuning is necessary and can be described as voltage-controlled capacitors. The operational principle of diodes is based on the inner pn junction, which can operate in a forward or reverse direction, depending on the sign of the applied voltage. Varactor diodes operate in a reversed-biased state, leading to a depletion zone, which is not passable for DC. The dimensions of the depletion zone are modifiable through variations in the applied voltage. Elevating the applied reverse voltage results in an expanded depletion zone. The depletion zone can be analogously envisioned as a plate capacitor. Consequently, increasing the applied reverse voltage across a varactor diode leads to an increased separation between the two plates, resulting in a concomitant reduction in the overall capacitance.

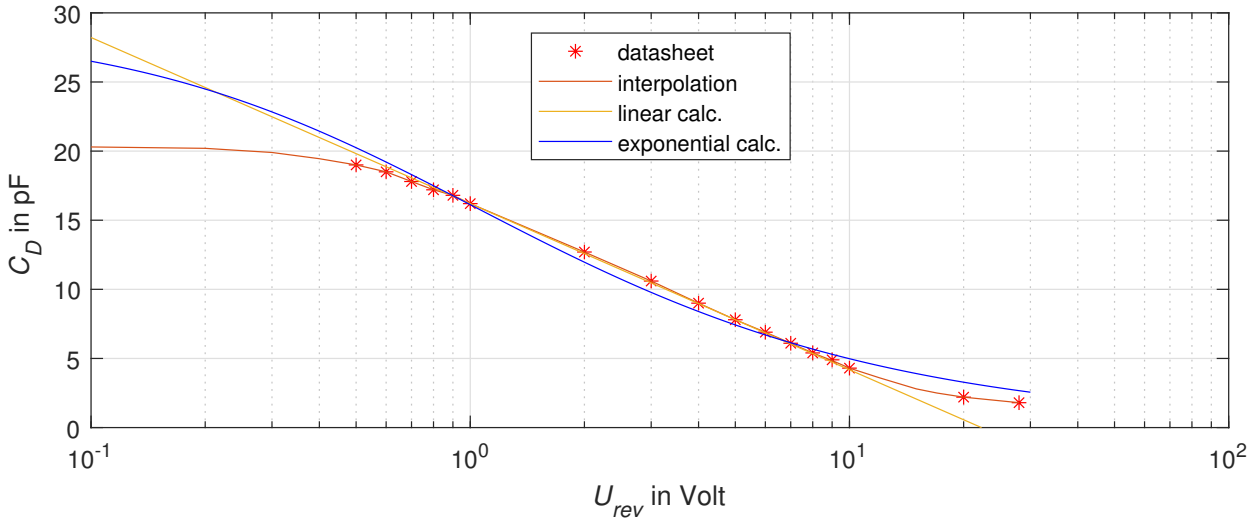

Figure 2.11: Capacitance curve of the varactor diode BB135 from NXP over a voltage range from 0.1V to 28V; capacitance values from the datasheet for voltages lower than 0.5V are interpolated; exponential calculation is done with $\gamma = 0.63$, $V_d = 0.65\,\mathrm{V}$, and $C_0 = 29\,\mathrm{pF}$ according to Eq. 2.17; linear calculation with Eq. 2.16 is valid for rage of 1V to 5V, with $k_d = -12pF$ and $d = 16.2pF$

The relation between applied reverse voltage and capacitance for varactor diodes cannot be seen as linear, as shown in Fig. 2.11. The plot uses the varactor diode BB135 from NXP, where the datasheet provides values ranging from 0.5V to 28V. The area of interest is up to a voltage of 5V, which is the maximum available voltage in the developed Permittivity Meter. The available capacitance range for voltages between 0.5V to 5V leads is $\Delta C = 8.4pF$, calculated by the minimal

and maximal capacitance of $C_{min} = 7.8pF$ and $C_{max} = 16.2pF$.

In the later Firmware (FW) application, the relation between varactor diode voltage and their corresponding capacitance is essential to determine the relative permittivity of snow. A lookup table will be used to determine the diode's capacitance from the known applied voltage to the diode in the FW application. To generate the content of the table, a mathematical representation of capacitance related to voltage is needed.

Fig. 2.11 shows two different approaches for describing the characteristics of the varactor diode, first by using Eq. 2.17, which is a standard formula for varactor diodes capacitance determination. C_0 is the initial capacitance given for zero volts and is usually available in the varactor diode datasheet (in some cases, the initial capacitance is given for a specific voltage like 0.5 V). To calculate the actual diode capacitance C_D, the applied reverse voltage U_{rev} must inserted, the diffusion voltage of the and the numerical value for γ, which influences the shape of the exponential function. However, as shown in Fig. 2.11, the exponential calculation does not entirely reflect the diode characteristic from the datasheet. The exponential interpolation is adequate for the voltage range between 1 V and 10 V, whereas the interpolation for values below 1 V does not supply a satisfying result.

As a second approach, linear interpolation can be used. The linear computation depicted in Fig. 2.11, mathematically expressed by Eq. 2.16, can serve as a highly accurate approximation within a voltage range spanning from 1V to 5V.

$$C_d = k_d \cdot \log\left(\frac{V_{rev}}{1V}\right) + d \tag{2.16}$$

$$C_d = \frac{C_0}{\left(1 + \frac{V_{rev}}{V_d}\right)^{\gamma}} \tag{2.17}$$

2.3.2 Calibration and Tuning Process

The operational principle of the Permittvity Meter is based on detuning the resonant circuit, which includes a modified resonant frequency and quality factor. These two parameters are caused by changes in the properties of the exposed material to the sensor unit. The changes are always relative to the calibration point. Thus, before performing any measurement, a calibration must be initiated, preferred with a relative permittivity $\epsilon_r = 1$, corresponding to that of vacuum and approximately to air. Ideally, the circuit's resonant frequency is precisely located at the input signal frequency, favored at 20 MHz. Instead of using the simplest way of quantifying the notch

filter characteristic by a bode diagram, the only possible parameter to characterize the resonant circuit within the portable Permittvity Meter device is by voltage amplitude of the Fast Fourier Transformation (FFT) analysis.

The change of the relative permittivity is only possible in the positive direction, which means a growth of the corresponding capacitance. According to section 2.2.2, growth results in a lower resonant frequency. A shifted resonance frequency is identifiable by an increased amplitude of the measurement signal. This is evident as the frequency domain's low point shifts towards the spectrum's left side.

Determination of Relative Permittivity without Imaginary Part

The initial position is a 5 pF added capacitance to the sensor unit, imitating a specific relative permittivity. The actual measurement is now performed by successive increasing the voltage over the varactor diodes, which results in a lower capacitance due to their negative exponential correlation between voltage and capacitance. The reduction in capacitance initiates a shift in the resonant frequency, this time in the opposite direction—towards the right. The exemplary tuning process in Fig 2.12 shows the resonant frequency movement. As the capacitance changes, the amplitude experiences an initial decrease until it reaches a minimum, then rises again because the low point in the frequency domain is now further shifted rightwards. The frequency shift cannot be measured, but the altered amplitude at 20 MHz input signal. The right image of Fig. 2.12 shows the amplitude variation produced by the intersection of the vertical line at 20 MHz and the corresponding bode diagram, considering the capacitance as the swept parameter. This minimum's occurrence signifies that the notch filter's resonant frequency is now trimmed to equal the input signal frequency.

In the non-ideal case, the resonant frequency is unequal to the input signal frequency at the calibration time. The measurement process cannot aim to reach an absolute minimum in this situation. However, this problem can be defused by tuning the circuit's resonant frequency already at calibration time to match the input signal frequency, with the drawback of reduced measurement range, because the remaining capacitance range of the varactor diode is lowered. This process is only feasible when the resonant frequency is initially too low. This limitation arises from the fact that the capacitance of the varactor diodes cannot be increased related to their capacitance level at zero volts.

Returning to the simulation, the attainment of the minimum amplitude by tuning the varactor diode marks the completion of the measurement process. The relative permittivity of the material interacting with the sensor unit, causing the initial resonant frequency shift, can now be calculated

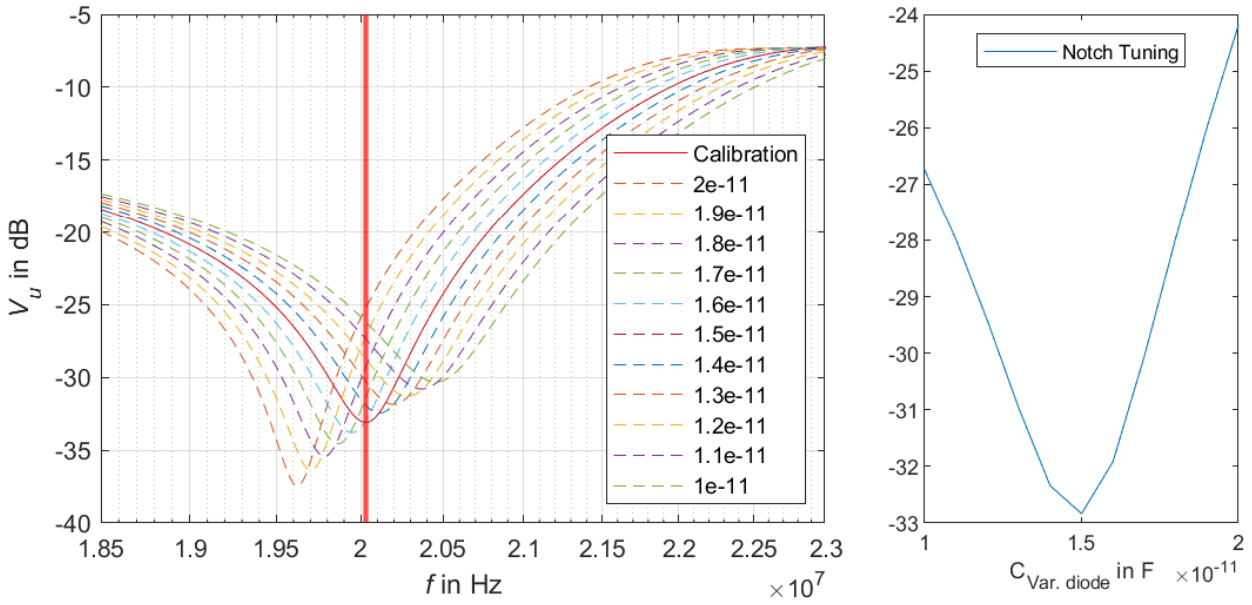

Figure 2.12: Exemplary tuning process for a 5 pF change on the sensor unit; left image shows notch characteristic for different varactor capacitance (vertical line represents the target frequency) and right image the signal amplitude (at 20 MHz) for different tuning steps (note, tuning goes from right to left with 20 pF initial value); Initial values of simulation: [20 pF for var. diodes, $R_L = 100\,\mathrm{k\Omega}$, PCB parasitic of 48 pF, nominal inductance 550 nH with $R_{L,s} = 6.5\,\Omega$, resonant frequency $f_r \approx 20\,\mathrm{MHz}$]

by comparing the actual diode voltage to the voltage at calibration time. This calculation relies on knowledge of the varactor diodes' characteristics, enabling the conversion of the diode voltage change to a capacitance change. The sensor capacitance at calibration time and the measured capacitance change are then utilized to determine the relative permittivity ϵ_r.

Determination of Relative Permittivity with Imaginary Part

The previous simulation is only valid for materials with pure real relative permittivity $\epsilon_r = \epsilon_r'$. Materials such as snow exhibit a complex permittivity $\epsilon_r = \epsilon_r' + j\epsilon_r''$. Thus, the tuning process is expanded by an additional step. Choosing the same exemplary example as before, but now with an additional imaginary part of ϵ_r, which is characterized in the simulation by a parallel ohmic resistance to the sensor. Fig. 2.13 shows the first tuning step again, with a variation of the varactor capacitance through the applied voltage. Now a minimum for a reduced diode capacity of approximately $15 - 16\,\mathrm{pF}$ is reached. Closer looking at 2.13 shows, that the initial calibration point is never reached, because the additional parallel resistance moved the whole array of curves downwards.

A second tuning step is required to return the curve to the initial point. To avoid any confusion,

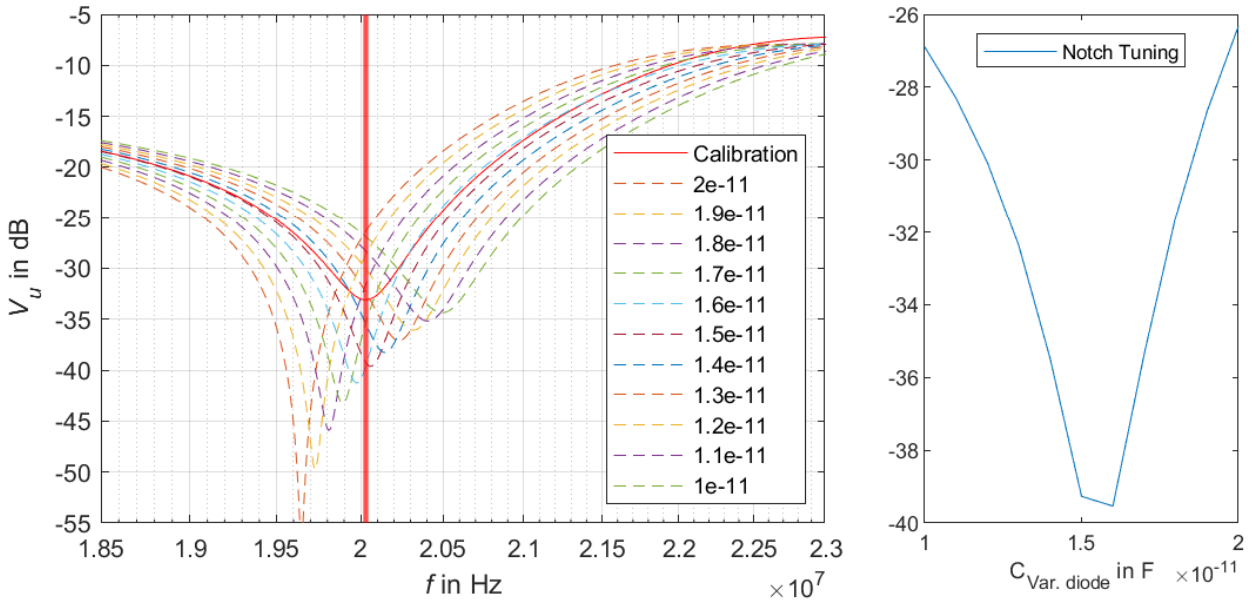

Figure 2.13: In addition to Fig. 2.12, a resistance of $R_L = 6\,\text{k}\Omega$ is added; simulation configuration is identical as for Fig. 2.12; left image shows that the initial calibration amplitude cannot be reached, but right image visualize reaching a local minimum between $\Delta C_d = 4 - 5\,\text{pF}$.

the varactor diode used in the previous explanation is now named with diode one. In contrast, the varactor diode used for tuning the imaginary part ϵ_r'' is called diode two. Tuning the varactor diode two can be seen in Fig. 2.14, where the voltage curve is moved back upwards when increasing the diode's capacitance. The third final curve reaches exactly the initial voltage at 20 MHz. The capacitance of varactor diode two can now be used to determine the imaginary part ϵ_r''.

As shown in Fig. 2.12, the simulation was initially performed with an additional 5 pF capacitance, but the minimum was already detected at 4 pF capacitance change of the varactor diode one. This phenomenon can be explained by 2.14, showing a slight resonant frequency deviation to the left side due to the additional parallel resistance. It is also visible that the minimum of the notch curve is not exactly reached; therefore, the tuning goes into a second iteration, meaning going back and rerunning step one by reducing the diode capacitance one minimally to reach the minimum again. This leads to a resonant frequency shift to the right side, moving the curve share of tuning step two rightwards. Furthermore, tuning step two will also result in a slightly different diode capacitance to reach the initial curve exactly.

Conversion of Capacitance Difference ΔC_d to relative permittivity ϵ_r'

Determination of the relative permittivity ϵ_r' is now possible by knowing the capacitance difference ΔC_d of the varactor diode during the tuning procedure. With Eq. 2.18 and the case of staying

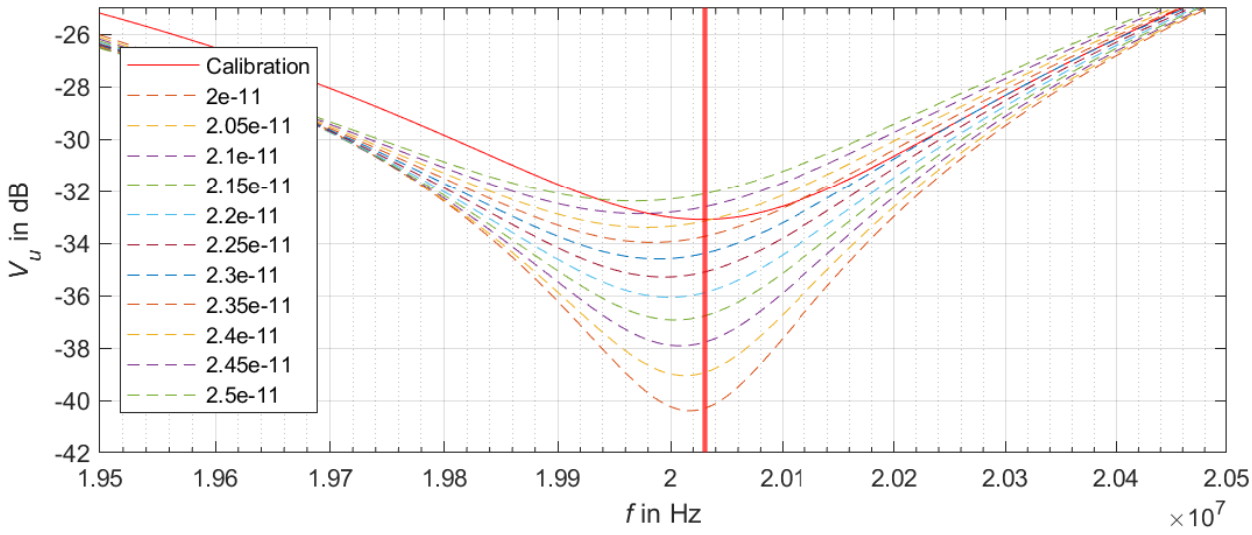

Figure 2.14: Exemplary tuning process for varactor diode 2; simulation configuration is identical as for left 2.12; capacitance change influences the signal amplitude with minimal resonant frequency variation;

within the linear range of the diode, the capacitance difference between the reference point, or calibration point, and the actual measurement point results in 2.19.

$$\Delta C_d = C_{d,m} - C_{d,ref} = k_d \cdot \log(V_m) + d - (k_d \cdot \log(V_{ref}) + d) \tag{2.18}$$

$$\Delta C_d = k_d \cdot \log\left(\frac{V_m}{V_{ref}}\right) \tag{2.19}$$

Furthermore, ΔC_d can be equated with 2.20, describing the actual capacitance change on the sensor unit. Rearranging Eq. 2.22 allows the determination of the actual ϵ'_r of the exposed snow sample to the sensor unit. V_{ref} is the applied diode voltage during calibration whereas V_m represents the used voltage to tune the Notch circuit's resonant frequency back to the one of calibration. The diode-specific factor k_d is the actual relation between diode voltage and capacitance, and C_s characterizes the initial differential sensor capacitance. Eq. 2.23 is only valid in case of sensor calibration in air with $\epsilon'_r = 0$.

$$\Delta C_m = C_m - C_{ref} = \epsilon'_r \cdot \epsilon_0 \frac{A}{d} - \epsilon_0 \frac{A}{d} = C_s(\epsilon'_r - 1) \tag{2.20}$$

$$\Delta C_m = \Delta C_d \tag{2.21}$$

$$C_s(\epsilon'_r - 1) = k_d \cdot \log\left(\frac{V_m}{V_{ref}}\right) \tag{2.22}$$

$$\epsilon'_r = 1 + \frac{k_d}{C_s} \cdot \log\left(\frac{V_m}{V_{ref}}\right) \tag{2.23}$$

Equation 2.23 can originally be found in a publication from A. Denoth [1], where k_d and C_s are merged into a common sensor constant $k = k_d/C_s$. With 2.23, it is now possible to compute the actual relative permittivity ϵ'_r of snow, by using the parameters of the sensor unit and the diode voltage from the tuning procedure.

Suppose the linear relation between diode voltage and capacitance is left. In that case, Eq. 2.24 can be used, where the ΔC_{meas} must be determined first using a lookup table with relation between diode voltage and capacitance.

$$\epsilon'_r = 1 + \frac{\Delta C_{meas}}{C_s} \tag{2.24}$$

Calculating the Losses of the relative Permittivity

For calculating the real part of ϵ_r, the difference of the diode capacitance can be directly converted into a relative permittivity of the exposed snow sample. Determining the imaginary part ϵ''_r out of the measurement results is difficult because there is no simple mathematical equation to describe the relationship between the capacitance difference and ϵ''_r. Therefore, a practical approach could be the generation of a look-up table, where the actual capacitance difference is mapped with a specific ϵ''_r.

2.4 Signal Processing Approaches

Since the notch filter only influences the signal amplitude and phase but not the frequency itself, the measurement signal has a frequency of $f = 20\,\text{MHz}$. The only way to process the signal quantities further is through analog to digital conversion. The analog to digital conversion itself can be done in different ways.

2.4.1 Oversampling

Oversampling describes the default way of quantizing an analog signal. The term oversampling can be defined by having a sampling frequency greater than two times the highest available signal

frequency to prevent aliasing. In other words, the Nyquist-Shannon sampling theorem must be fulfilled.

$$f_s > 2f_{max}, \tag{2.25}$$

This theorem leads to a minimum required sampling frequency of $fs = 40\,\text{MHz}$. An internal ADC of a standard microcontroller cannot provide such a high sampling frequency. Therefore, an external ADC with a specific data interface is required. SPI is a common way to transfer data between external ADCs and the Microcontroller Unit (MCU). For a digital quantization of 12-bit, a minimal SPI frequency of $f_{clock,SPI} = 12f_s = 480MHz$ is required to push the sampled data to the MCU. In reality, the clock frequency of the SPI must be higher due to the internal sampling and conversion time of the ADC. Such a high frequency is not typical for low-power microcontrollers. Hence, the oversampling approach is not practicable for this application.

2.4.2 Mixer for Frequency Conversion

An analog mixer allows shifting down the high-frequency signal to a frequency range where analog-to-digital conversion is much easier. This technique requires an analog mixer circuit (different analog circuits can be used) and a second frequency with a dedicated frequency offset compared to the original signal. The mixer technique can be described in the mathematical domain by theorems of the products of trigonometric functions.

$$y = \sin(\alpha) \cdot \sin(\beta) = \frac{1}{2} \cdot [\cos(\alpha - \beta) - \cos(\alpha + \beta)] \tag{2.26}$$

$$y = \sin(\omega_1 t) \cdot \sin(\omega_2 t) = \frac{1}{2} \cdot [\cos((\omega_1 - \omega_2)t) - \cos((\omega_1 + \omega_2)t)] \tag{2.27}$$

The result consists of a signal with two frequency components, one with a frequency component regarding their difference and a second one according to the summation of both signals. The summation is then suppressed by a low-pass filter and the remaining signal of interest with a frequency of $\omega' = (\omega_1 - \omega_2)$ can be sampled. The technical effort for this approach is to provide a second sinusoidal signal with minimal frequency shift compared to the signal of interest.

2.4.3 Undersampling

Undersampling is a technique where the Nyquist-Shannon sampling theorem is intentionally violated and uses aliasing as an advantage effect. Aliasing as an advantage can only be used if specific prerequisites are fulfilled. The Nyquist-Shannon sampling theorem for signals that range from DC

to an upper-frequency component is defined by $f_s \geq 2f_{max}$. For signals that do not range to the DC level, the sampling theorem is defined in more detail by $f_s \geq 2(f_{max} - f_{min})$ or $f_s \geq 2B$, where B describes the signal bandwidth. Therefore, the signal's bandwidth to be measured must first be known. Secondly, the exact position of the measurement signal in the frequency spectrum is essential. In more detail, one has to ensure that the bandwidth of the measurement signal lies within a multiple of the Nyquist bandwidth, also known as the Nyquist zone [12]. Equation 2.28 can define a Nyquist zone with $0 \leq n \leq \infty$.

$$n^{th} Nyquistzone = [\frac{n}{2} f_s, \frac{n+1}{2} f_s] \tag{2.28}$$

In other words, two properties of the measurement signal must be known to locate the signal in the frequency spectrum: the bandwidth itself and the lower bandwidth frequency. Undersampling aims to shift a specific frequency bandwidth to fall back into the Nyquist bandwidth between DC and $f_s/2$, corresponding to the first Nyquist zone. Therefore, any signal that falls outside the bandwidth of interest must be filtered out. Otherwise, it will be aliased into the Nyquist bandwidth and corrupt the signal of interest.[12]

This project aims to measure a target frequency of around $f_{targ} = 20\,\text{MHz}$, with an ideal bandwidth of $B_{ideal} = 0$. In reality, the 20 MHz signal will be produced by a crystal oscillator with a specific tolerance in the ppm range. Therefore, a theoretical bandwidth of $B = 100Hz$ will be sufficient. According to [12] a minimal required sampling frequency can be seen as a function of the ratio of the highest frequency component f_{max} to the total signal bandwidth B. For a large ratio of f_{max} to the signal bandwidth B, a minimal sampling rate of $2B$ is sufficient.

In general, any sampling frequency could be used, which ensures that the signal bandwidth does not cross an integer multiple of fs/2. Since the sample rate, in reality, cannot be chosen arbitrarily, a suitable rate must be selected out of a limited set of available sample rates for a specific ADC. The sample rate of the onboard ADC built in the STML476RG MCU can be calculated with the help of the corresponding datasheet [13, p. 525] and can be described by Eq. 2.29. The T_{sar} describes the conversion time for the Successive-approximation-ADC (SAR-ADC), which depends on the selected resolution and can be quantified by 12.5 clock cycles for 12-bit resolution. Sample cycles can be chosen according to 2.1, where the corresponding calculated sample frequencies are included too. The used ADC clock is quantified with $f_{adc_clk} = 80\,\text{MHz}$.

$$T_{conv} = T_{smpl} + T_{sar} = (n_{cylces} + 12.5)T_{adc,clk} \tag{2.29}$$

Table 2.1: Sample Frequency calculated by to sample cycles based on Eq. 2.29

Sample cycles	Sample period	Sample frequency (Hz)
2.5	1.88E-07	5.333E+06
6.5	2.38E-07	4.211E+06
12.5	3.13E-07	3.200E+06
24.5	4.63E-07	2.162E+06
47.5	7.50E-07	1.333E+06
92.5	1.31E-06	7.619E+05
640.5	8.16E-06	1.225E+05

The lowest possible sample frequency is $f_s = 122.511\,\text{kHz}$. For a target frequency of $f_{targ} = 20\,\text{MHz}$, a so-called undersampling factor of $k = 163.250$ can be determined. This factor k is not an integer multiple; thus, the target frequency f_{targ} lies within exactly one Nyquist zone, especially in the one with $n = 163$, ranges from 19.969 MHz to 20.092 MHz. The conclusion of $k = 163$ is a frequency shift by a factor of $163 f_s$, which leads to a correlated baseband frequency of $f_{baseband} \approx 30.628\,\text{kHz}$ according to Eq. 2.30. The factor n is the integer value of k.

$$f_{baseband} = |f_{targ} - n \cdot f_s| = |20 \cdot 10^6 - 163 \cdot 122.511\,\text{kHz}| = 30.628\,\text{kHz} \tag{2.30}$$

Essential Properties for Undersampling Applications

Analog Bandwidth of the ADC

The undersampling approach comes with some limitations regarding the measurable quantity. To quantify an analog signal, ADCs use a sample and hold circuit consisting of an input resistance and a capacitance in the simplest version. This circuit can be seen as a lowpass filter, with a specific cutoff frequency $f_c = 1/2\pi RC$ at -3dB, and forms the analog bandwidth of an ADC. Higher signal frequencies than the cutoff will be damped according to the filter's frequency response. The measurement frequency must be within the analog bandwidth or at least minimal above the cutoff frequency to avoid unwanted attenuation. The sample time $T_s = 1/f_s$ can be split into an actual sample and conversion time $T_s = t_{smpl} + t_{conv}$. During sample time, a switch is closed and the applied voltage will charge the capacitance through a resistor. In contrast, while conversion, the subsequent logic, which depends on the type of the ADC; for the STM32L476RG, it is a SAR, measures the voltage of the capacitor.

High Undersampling Factors

For high undersampling factors, the ADC must be able to accurately digitize signals well outside of the Nyquist bandwidth that most ADCs are designed to handle. Therefore, ADC's for the undersampling approach must have a low disturbance at the high input frequency f_{targ}. Thus, a

decisive characteristic for selecting the proper ADC is the SFDR curve, especially for the target frequency f_{targ}. Low distortion at f_{targ} will increase system performance.[12].

Clock Jitter

According to [2], the total Signal-to-Noise Ratio (SNR) of an ADC can be calculated by Eq. 2.31 and consists of three main parts, the quantization noise dependent on the reverence voltage and bit-resolution, the frequency-independent thermal noise of the ADC and the uncertainty regarding clock jitter. Equation 2.31 from [2] is initially composed for voltage ratios but was rewritten for the power ratio between signal and noise.

$$SNR_{ADC}[dB] = 10 \cdot \log\left(10^{\frac{-SNR_{QuantNoise}}{10}} + 10^{\frac{-SNR_{ThermalNoise}}{10}} + 10^{\frac{-SNR_{Jitter}}{10}}\right) \tag{2.31}$$

ADCs are typically connected to a clock system, which provides a high clock frequency for the ADC core. In contrast to the sample and hold frequency, which triggers the ADC and is equal to the sampling frequency f_s, the frequency for the ADC core is much higher. For the STM32L476RG, the ADC core frequency is selectable up to 80 MHz, whereas the used sampling frequency can be a fraction and is chosen for the given application with $f_s \approx 122.5\,\text{kHz}$. According to [2], for undersampling applications, special attention must be paid to the used clocks because the clock's jitter becomes a dominant part for high input frequencies and will degrade the SNR of the ADC.

Figure 2.15 looks at one sampling point and shows how timing uncertainties create amplitude variations. A particular clock jitter, called phase noise, will produce higher amplitude variations when the input frequency increases and degrade the SNR according to Eq. 2.31. The thermal noise of an ADC is independent of the frequency and is the dominant part for lower frequencies, whereas the clock jitter dominates the high-frequency range. Furthermore, the slew rate of the clock signal directly influences the sampling instant. In case of thermal noise in the clock distribution, the slew rate will also be converted into a timing uncertainty (aperture jitter). Aperture and clock jitter are separate effects but will be combined at sample instant and the absolute value can be determined by 2.32. For a specific measurement frequency, the SNR_{Jitter} can be determined by 2.33. [2]

$$t_{jitter} = \sqrt{(t_{jitter,clockinput})^2 + (t_{aperture,ADC})^2} \tag{2.32}$$

$$SNR_{jitter}[dB] = -10\log(2\pi f_{in} t_{jitter}) \tag{2.33}$$

The input signal undergoes convolution with the sampling clock signal in the sampling process,

incorporating its associated phase noise. When conducting FFT analysis on the input signal, the central focus is on the primary FFT bin, aligning it with the input signal. The amplitude of the bins surrounding the primary bin is influenced by the phase noise around the sampled signal, originating from either the clock or the input signal. If the phase noise falls within one bin of the FFT, where the bin width (f_s/N) is defined by the sampling rate and the number of sampling points, it does not significantly impact the FFT spectrum. However, when the phase noise extends beyond one FFT bin, the primary FFT bin undergoes division into multiple bins. This effect is further amplified in applications involving substantial undersampling factors, resulting in a broad signal distribution across multiple FFT bins. Consequently, determining the actual signal frequency becomes challenging within the FFT spectrum.

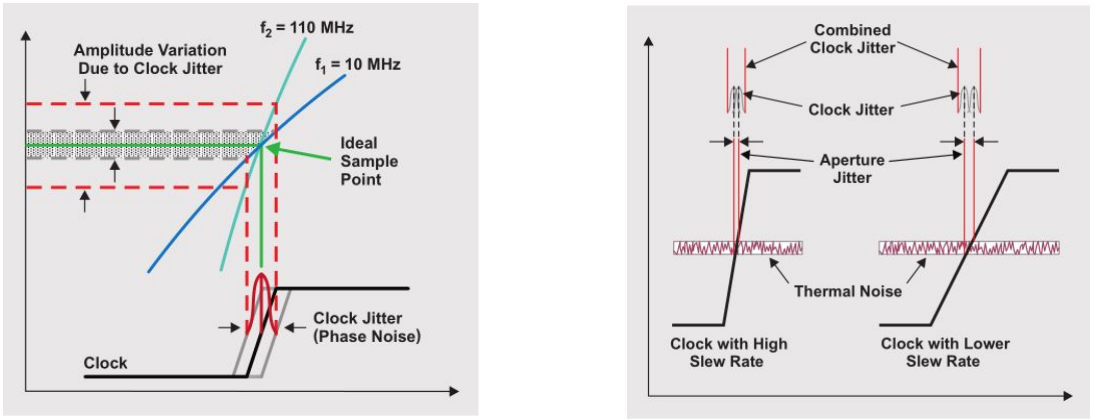

Figure 2.15: Clock jitter effects on sample data; left figure shows how clock jitter creates more amplitude error with faster input signals; right picture shows jitter produced by the ADC aperture jitter combined at sampling instant [2]

Signal Measurement with shared Clock Source

On a MCU, a primary clock source, typically derived from an external crystal or an internal RC oscillator, is commonly employed to generate various other required clock sources with distinct frequencies. As elucidated in section 2.4.3, it is imperative that the measurement signal falls within an integer multiple of the sampling frequency f_s. To achieve the measurement of a target frequency of 20 MHz, complying with this condition, the master clock of the MCU must exceed 20 MHz. The limitation is introduced because the onboard ADC is connected to the master clock or at least to an integer-divided subfrequency.

An exception arises when the master clock can be divided in a manner that results in the ADC main clock not being a frequency derived from integer division. In such a case, the following lines can be skipped.

The assertion can be exemplified with a scenario featuring a measurement signal $f_{meas} = 20\,\mathrm{MHz}$ and a master clock $f_{master} = 20\,\mathrm{MHz}$. By examining the periods instead of the frequencies and employing 653 ADC clock cycles for sampling, the master clock corresponds to a period $T_{master} = 50\,\mathrm{ns}$, while the sample period $T_s = 32.65\,\mu\mathrm{s}$ is observed. It becomes evident that the measurement signal's period is now an integer multiple of the actual sample period. Consequently, both frequencies are also related by an integer multiple, situating the measurement signal at the edge of a Nyquist zone.

If the MCU allows higher frequencies through an internal Phase Locked Loop (PLL), the ADC clock can be elevated to 40 or 80 MHz resulting in associated periods of $T_{Adc,40\,\mathrm{M}} = 16.325\,\mu\mathrm{s}$ and $T_{Adc,80\,\mathrm{M}} = 8.1625\,\mu\mathrm{s}$, while maintaining the same number of ADC clock cycles for sampling. In this scenario, the relationship between the measurement signal period and the sampling period is $k_{40\,\mathrm{M}} = 326.5$ and $k_{80\,\mathrm{M}} = 163.25$ respectively. This non-integer multiple ensures the measurement signal is positioned within a Nyquist zone rather than at the zone's edge.

2.5 Discrete Fourier Transformation for Signal Evaluation

In order to get information about absolute signal amplitude, an analysis tool such as the Discrete Fourier Transform (DFT) is a good choice. Hence, the DFT is an integrating procedure that increases the SNR between the actual signal and distortions. Furthermore, the DFT provides a form of averaging by processing many sample points. With the resultant frequency spectrum from the DFT algorithm, distortions introduced by amplifiers can be distinctly isolated from the intended measurement signal. As a result, these distortions have no bearing on determining amplitude.

The computational complexity of the DFT is characterized by $\mathrm{O}(N^2)$, implying that for a 512-sample signal, the analysis would necessitate 262144 computational steps. The decimation-in-time FFT aims to reduce the computation effort compared to the DFT, without losing accuracy simultaneously. This is possible by decomposing the DFT into smaller and smaller DFTs, and using the symmetry of the twiddle factors. Each decomposing is called a stage. The used algorithm is called radix 2, initially developed by Tukey and Cooley in 1965 [14], where the number of stages can be calculated with $\mathrm{ld}(N)$. In total, the number of complex multiplications can be reduced to Eq. 2.34, compared to an order $\mathrm{O}(N^2)$ for a normal DFT computation. The complex multiplications are reduced by using the symmetries of the twiddle factors. Using the mentioned example again, the computational effort would be reduced to 2304 steps.

$$\mathrm{O}(N/2 \cdot \mathrm{ld}(N)) \tag{2.34}$$

In a subsequent FFT implementation within the firmware, these complex twiddle factors can be calculated and scaled beforehand and stored in a non-volatile memory.

3 Realization

3.1 Schematic and Component Groups

The realization starts with grouping the required circuits into seven parts. The centerpiece is formed by the microcontroller, affording flexibility with the option of employing either the NUCLEO STM32L476RG from STMicroelectronics N.V. (STM) or the MSP430FR2355 from TI for the Permittivity Meter. The design incorporates two distinct pin header dimensions, facilitating the fast interchangeability of the development kit with the main board. User interaction is assured through two interfaces: USB and Bluetooth, where Bluetooth is an optional feature. Additionally, provision has been made for a reset button and an individual-use button, providing functionality such as waking up the system from a sleep state. Furthermore, an onboard RGB status LED enhances user experience by visually indicating the current state of the handheld device. The primary design circuit components are summarized as follows:

- Sinewave filter
- Pre-amplifier
- Notch filter
- Two-stage amplifier
- Post-amplifier
- Varactor diodes amplifier
- Microcontroller and user interaction

The subsequent explained circuits are visible in the schematic plots in Fig. A.11 and A.12. The corresponding component values are also listed in the bill of materials plotted in Fig. A.10.

3.1.1 Sinewave-Filter

The measurement bridge incorporates a notch filter and requires a sinusoidal input signal with a frequency of 20 MHz. Although the MCU can produce the signal, it is initially rectangular. Therefore, a filter is necessary to convert it into a sine wave. Rectangular signals can be characterized by a Fourier series with harmonic frequency components at $3, 5, 7, 9, 11..$ times the fundamental oscillation. Thus, the filter steepness must be high to suppress the most shaping harmonic components at 60 and 100 MHz, which can be sufficiently achieved by a 7^{th} order filter.

The filter design is based on the considerations outlined in [4], whereas the individual component values are calculated following the instructions provided in [3]. A 7^{th} order filter is chosen to manage the demand having a -3 dB cutoff at 20 MHz and suppression of -60 dB at 60 MHz. The required order to satisfy the requirement can be obtained from the attenuation characteristics for Chebyshev filters with -1 dB ripple [3, p. 57], plotted for normalized frequencies where the normalization refers to the cutoff frequency (60 MHz related to $\Omega = 60\,\text{MHz}/20\,\text{MHz} = 3$). The normalized component values can be determined for -1 dB Chebyshev [3, p. 459].

The input impedance of the filter must be chosen according to the output pin characteristic of the MCU. According to the thesis of [4], the output resistance of the MSP430 is defined by $40\,\Omega$. On the other hand, for the STM controller, the output resistance can be computed by the maximal possible output current specified in [15, p. 172] with $I_{IO} = 20\,\text{mA}$, together with the output voltage of $V_{IO} = 3.3\,\text{V}$, the output resistance leads to $R_{IO} = 165\,\Omega$.

Denormalization with the frequency scaling factor $FSF = 2\pi f_c/\omega'$ and the input and load impedance, which is selected by either $R_s = R_l = 200\,\Omega$ or $R_s = R_l = 40\,\Omega$ leads to the needed nominal component values by Eq. 3.1 and 3.2. The denormalized component values are in Tab. 3.1.

$$L = \frac{L' \cdot R_s}{FSF} \tag{3.1}$$

$$C = \frac{C'}{FSF \cdot R_s} \tag{3.2}$$

Table 3.1: Denormalized nominal coefficient values for the sinewave filter, depending on the required input resistance; * normalized coefficients according to 1-dB Chebyshev characteristic [3, p. 459].

Type	**fc**	**FSF**	$R_s = R_l$	$C_1 = C_7$	$L_2 = L_6$	$C_3 = C_5$	L_4
Normalized*	$1.00 \cdot 10^0$	1	1	2.2043	1.1311	3.1472	1.1942
$R = 40$	$20.0 \cdot 10^6$	$1.26 \cdot 10^8$	$4.00 \cdot 10^1$	$4.38 \cdot 10^{-10}$	$3.60 \cdot 10^{-7}$	$6.26 \cdot 10^{-10}$	$3.80 \cdot 10^{-7}$
$R = 200$	$20.0 \cdot 10^6$	$1.26 \cdot 10^8$	$2.00 \cdot 10^2$	$8.77 \cdot 10^{-11}$	$1.80 \cdot 10^{-6}$	$1.25 \cdot 10^{-10}$	$1.90 \cdot 10^{-6}$
Nominal ($R = 40$)	$20.0 \cdot 10^6$	–	$39\,\Omega$	$470 \cdot 10^{-12}$	$330 \cdot 10^{-9}$	$680 \cdot 10^{-12}$	$390 \cdot 10^{-9}$

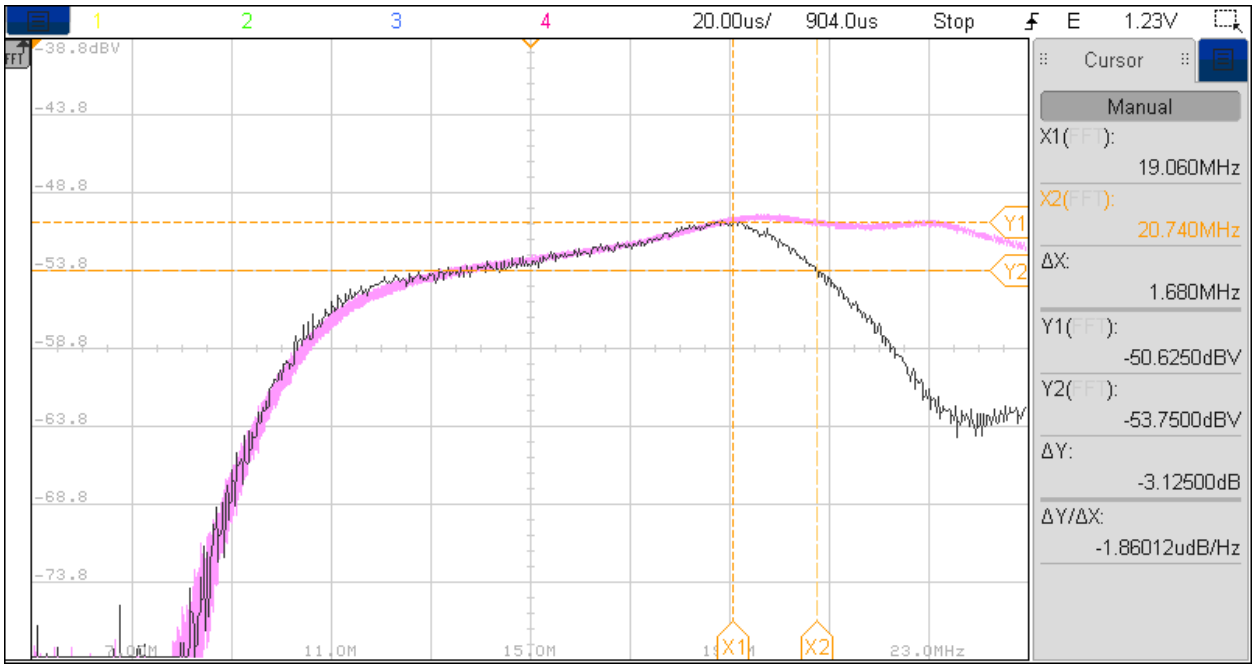

Figure 3.1: Measured bode diagram of the sinewave-filter; the pink curve is the input whereby the black curve is the output signal; Cuttoff frequency of $f_c = 20.74\,\text{MHz}$ detected

3.1.2 Operational Amplifiers

To accomplish various tasks, the Permittivity Meter circuit uses multiple OpAmps, two different OpAmp models to be more precise. The selection process of finding the correct OpAmps to satisfy the different requirements is a challenging task. Challenging parameters are a high Gain-Bandwidth-Product (GBW) to operate with 20 MHz input signals in combination with high gain factors, because the gain factor will determine and limit the actual cutoff frequency of the first-order low-pass filter, which most OpAmps are trimmed to. The possibility of operating with adjustable gains down to unity gain does not apply to every model, and some will require a minimal gain for stable operation. Only OpAmps marked with unity gain stability can provide such a stability pledge.

The intrinsic circuitry of OpAmps imposes constraints on the output control range, limiting it in both the lower and upper directions. This limitation parameter is primarily given by the relative positioning concerning the positive and negative power supply levels. An essential metric in this context is the rail-to-rail voltage output, with less focus on rail-to-rail input. The deviation from the ideals of the OpAmp leads to non-ideal properties and thus generates harmonic distortions. Various factors contribute to these distortions, and their manifestation is quantified by using their relation to the fundamental frequency component and is known as Spurious Free Dynamic Range

(SFDR), describing the relation between the RMS amplitude of the carrier frequency and the highest harmonic distortion. These distortions are graphically represented in a bode diagram, showcasing their frequency dependence. The most significant harmonic distortions occur at double and triple the fundamental frequency. The extent of harmonic distortions is significantly influenced by parameters such as supply voltage, applied load, selected gain, and other operational conditions.

In the context of high-frequency measurements, an indispensable parameter is the maximal slew rate (Slew Rate (SR)) of an OpAmp, conventionally denoted in V/µs. This metric signifies the upper limit of the voltage gradient achievable at the output. Checking the appropriateness of a specified slew rate is essential and can be performed by calculating the maximum gradient of the input signal. This maximal gradient manifests at the zero crossing for sinusoidal signals and can be calculated employing Eq. 3.3. Considering a sinusoidal signal with a frequency $f = 20\,\mathrm{MHz}$ and an amplitude $A = 1\,\mathrm{V}$, the slew rate corresponds to $SR \approx 125\,\mathrm{V/\mu s}$.

$$SR = \max\left(\frac{d}{dt}A \cdot sin(2\pi ft)\right) = \max\left(2\pi fA \cdot \cos(2\pi ft)\right) = 2\pi fA \tag{3.3}$$

All OpAmps are used in the single-ended configuration, which demands lifting the non-inverting input to a specific voltage level. A DC offset of $V_{cc}/2$ was set, using two equal resistances as a voltage divider with $R = 20\,\mathrm{k\Omega}$. Additionally, two capacitances are needed. One is placed in front of the voltage divider, and the second is the amplifier circuit's ground path, avoiding amplification of the DC part. The used component values for all OpAmps can be found in Tab. 3.2. The cutoff frequency is deliberately set low to facilitate testing measurements at lower frequencies.

Table 3.2: Nominal component values for input highpass DC blocker(marked with in) and high pass(marked with g) in ground path to avoid DC amplification; *Post amplifier requires only 1.25VDC offset to reach half of the ADC reference voltage $V_{ref,ADC} = 2.5\,\mathrm{V}$.

Amplifier Type	R_{in}	C_{in}	$f_{c,in}$	R_g	C_g	$f_{c,g}$
Pre	$2.00 \cdot 10^4$	10	$7.96 \cdot 10^2$	100	10	$1.59 \cdot 10^5$
Gain 1	$2.00 \cdot 10^4$	10	$7.96 \cdot 10^2$	56	10	$2.84 \cdot 10^5$
Gain 2	$2.00 \cdot 10^4$	10	$7.96 \cdot 10^2$	56	10	$2.84 \cdot 10^5$
Post*	$6.80 \cdot 10^3$	10	$2.34 \cdot 10^3$	–	–	–

Pre- and Post-amplifier

Pre- and Post-amplifiers are built with the same OpAmp model but have different responsibilities. The output of the sinewave filter sources the pre-amplifier and should amplify the damped signal to a desired voltage level. The circuity of the OpAmp, especially the gain, can be adapted to the voltage level of the rectangular input signal of the sinewave filter (the voltage level depends on the

used MCU). The amplifier also separates the sine filter from the notch circuit and ensures that they do not influence each other.

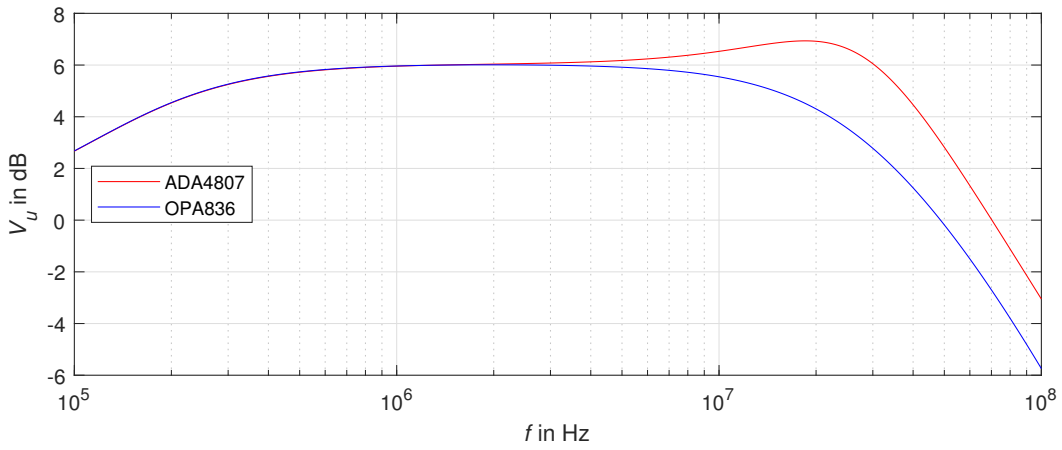

Figure 3.2: Bode plots comparison between OPA836 and ADA4807; non-inverting mode with $G = +2$, 1Vp input voltage, $R_g = R_f = 100\Omega$ and single-ended with 10nF leads to $f_c \approx 160kHz$

Conversely, the post-amplifier is assigned a distinct role. Hence, the two-stage amplifier in front of the post-amplifier must provide a very high GBW to accomplish gains up to a factor of ten, the output voltage range is limited for such models. Given that the single-ended ADC operates with a reference voltage of $V_{ref} = 2.5\,\mathrm{V}$ and mandates a DC offset of $V_{off} = 1.25\,\mathrm{V}$, a direct linkage of the two-stage amplifier to the ADC input would severely limit the achievable output voltage swing. A strategic compromise is made to overcome this limitation and enable the two-stage amplifier to utilize its full voltage swing without output limitations. This entails the integration of an additional rail-to-rail post-amplifier. Although this intervention effectively prevents voltage limitation, it also has a disadvantage: increased power consumption.

In the thesis of [4], the OPA836 OpAmp with a nominal GBW of 205 MHz according to the datasheet is used, where figure 3.3 shows the GBW for different gain settings and output amplitudes. Regarding 3.3, at least a gain of $G = +2$ for an output voltage swing of 2 Vpp should be no problem for the OpAmp.

In contrast to the datasheet, the Orcad Pspcie (Spice) simulation for the OPA836 results in a different behavior with an attenuation of -1dB at 20 MHz for the same output voltage swing. The cutoff frequency will be further lowered for higher gain settings; therefore, another OpAmp model, the ADA4807 from Analog Devices (AnalogD), is analyzed. According to the datasheet, this OpAmp has a lower nominal cutoff frequency, but Orcad Pspcie simulations show a much higher GBW compared to the OPA836.

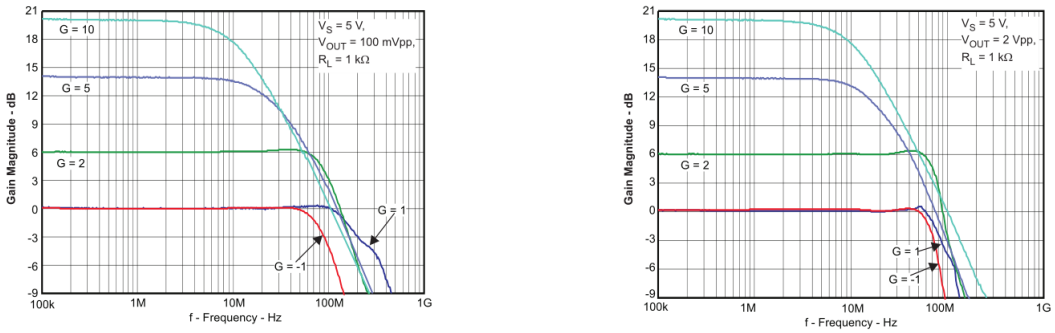

Figure 3.3: Frequency behavior of OPA836 from TI for different output amplitudes

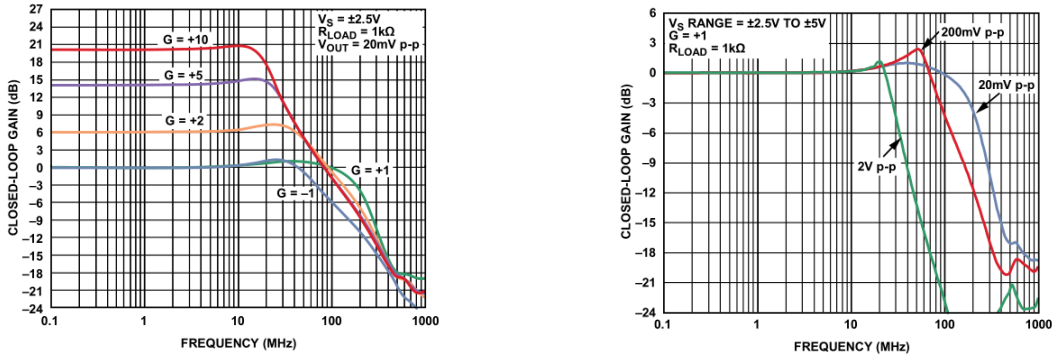

Figure 3.4: Frequency behavior of ADA4807 from AnalogDevices; left describes the dependence on the selected gain, right the dependence on different output amplitudes

The ADA4807's higher cutoff frequency compared to the OPA836 could be confirmed through measurements. The elevated harmonic distortions exhibited by the ADA4807 necessitated the utilization of the OPA836. Significantly, the third harmonic was relatively high for the ADA4807, which can be seen in Fig. A.5. Contrastingly, the distortion characteristics of the OPA836, as illustrated in Fig. A.4, exhibit a 13 dB greater separation between the carrier and the third-order distortion. Both measurements were performed under equal terms; the reduced amplitude due to the OPA836 (lower gain due to GBW) was also considered.

Figure A.3 shows the measurement of the achieved practical gain, where the limitation of the OPA836's GBW is visible. The practical gain with $G_{meas} = 3.12\,\text{dB}$ is in lower than in the simulation with $G_{sim} = 4.2\,\text{dB}$.

Two-stage Amplifier

The two-stage amplifier aims to provide a live adjustable gain stage, enabling the output signal to closely approach the ADC input limits, thereby maximizing ADC resolution. The ideal amplification steps should be +1, +10 and +100, where the maximal gain per stage is +10. Consequently,

the amplifier is set up in a non-inverting configuration with a fundamental gain of +10, whereby the resistor connected to the ground is switchable, implying an open ground connection and thus leading to a gain of +1. The easiest way to switch the resistor is through a Metal-oxide semiconductor field-effect transistor (MOSFET). A drawback of MOSFETs is the higher drain and source capacitance, which is the present impedance in the open state. Especially at high frequencies, using the MOSFET as a switch becomes challenging and distinguishing between open and closed states is impossible. Frequency sweeps in Orcad Pspcie simulations show exactly this behavior. The drain-source impedance of the MOSFET will be lowered for higher frequencies. Thus, the result is a lowpass behavior with a significant cutoff frequency. Therefore, the BS170 MOSFET is unsuitable for applications around 20 MHz. Hence, no other MOSFETs with much lower drain-source capacitance could be found, resulting in an increased cutoff frequency; another component technology, a Bipolar Junction Transistor (BJT), was used. Orcad Pspcie simulations with the BC547B transistor show a satisfying simulation result (Fig. 3.5), whereby the transistor can provide a much higher collector-emitter impedance in the off state than the MOSFET The BJT is also not able to separate the connection, therefore, a practical minimal gain of $G_{min} \approx 1.4$ must be taken into account.

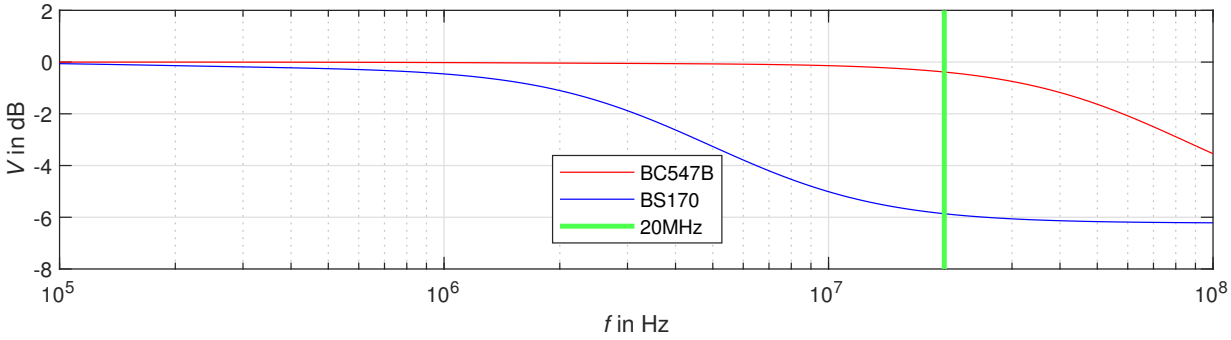

Figure 3.5: Bode diagram comparison between BS170 and BC457C; recorded by using two equal resistances as a voltage divider, where the MOSFET / BJT will switch the ground resistance

The selection of an OpAmp represents a significant challenge, particularly in achieving variable gains within the range of 1 to 10. The upper gain is heavily limited by the GBW of the OpAmp. In contrast, the lower gain is determined by the stability criterion and the fact of providing unity gain stability. The OPA2690 can fulfill both requirements from TI. Figure 3.6 visualizes the relevant simulation results.

The values for the feedback and ground resistors are chosen according to a rule of thumb in the datasheet [16, p. 21]. Regarding the recommendation, the parallel combination of R_f and

R_g should be less than 300 Ω. This can be achieved by a feedback resistor of $R_f = 500\,\Omega$ and $R_g = 56\,\Omega$ which then results in a overall gain of $G = 1 + \frac{R_f}{R_g} = 9.93$. When deactivating the gain stage, a stable behavior in practice could only be reached by a minimal gain of two. Therefore, a resistor parallel to the BJT was added. The nominal value of the parallel resistor corresponds to R_f, aligning precisely with the desired parallel resistance criterion of 300 Ω.

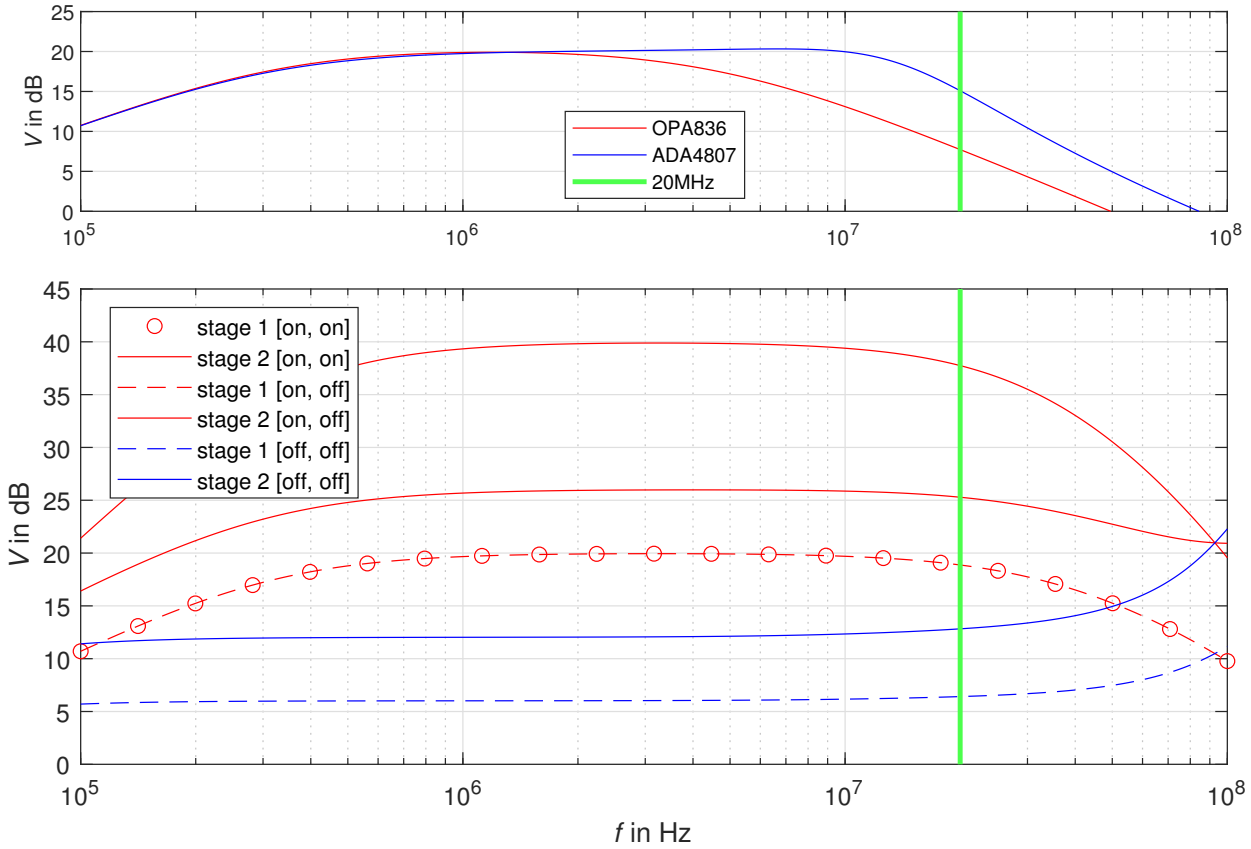

Figure 3.6: Detailed analysis of two-stage amplifier; (upper) alternative OpAmp models used, not able to reach desired 20 dB gain; (lower) two-stage amplifier with OPA2690, different achieved gains by switching gain stages individually, [off, off] $G = 12.826\,\text{dB} = 4.37$, [on, off] $G = 25.289\,\text{dB} = 18.4$, [on, on] $G = 37.7473\,\text{dB} = 77.1$

3.1.3 Varactor Diode Circuit

In the master thesis of Dierer [4], a varactor diode from Infineon with model code BB535 is used. According to electronic distributors, the product is marked with End-of-Life; thus, an equivalent model from NXP (NXP) with label BB135 is used.

To achieve an extensive dynamic capacitance range for the varactor diodes, it is necessary to have a minimal voltage range from zero to five volts. The analog outputs of the MCU, operating

with a reference voltage of $V_{ref} = 2.5\,\mathrm{V}$, are employed to supply the voltage to the varactor diodes. To reach the required five volts, the integration of an additional amplifier becomes essential. Given that the applied signal comprises only a DC component, the demands placed on the OpAmp are relatively moderate compared to the other instances and include only a rail-to-rail output voltage swing, aiming to attain the targeted DC voltage level up to $U_{DC} = 5V$. OPA341's features accomplish these requirements. The amplifier is used in non-inverting mode with a gain factor of $G = +2$, which is achieved by two identical resistor values for the forward and ground resistor $R_f = R_g = 9k1$.

3.2 Signal Processing

The signal processing pipeline initiates with analog sampling using the ADC, involving frequency manipulation through undersampling. Subsequently, the signal is analyzed in the frequency domain through FFT calculations, and amplitude determination is achieved via peak finding.

3.2.1 Limitation by Analog Bandwidth

Within the datasheet of the STM32L476RG controller [15, p. 177], a maximal internal sample and hold capacitor of $C_{ADC} = 5\,\mathrm{pF}$ is mentioned, whereas the specification of a resistance is missing. As a reference, the internal resistance of the MSP430FR2355 controller can be found in the datasheet [17, p. 51], specified as $R_{in_max} = 2\,\mathrm{k\Omega}$, together with the associated capacitance $C_{ADC} = 4.5\,\mathrm{pF}$. Facing the difference in the maximal sample frequency, where the TI model operates at 200 ksps and the STM model at 5 Msps, it can be deduced that STM's input resistance will be smaller than the TI. The measurement results show a minimal reduced bandwidth for the TI controller, but both controller ADCs provide a sufficient bandwidth for the target application.

The most straightforward method for ascertaining the analog bandwidth of the ADC involves empirical measurements. The results are shown in Fig. 3.7. The experimental setup employs a frequency generator as the source, and signal processing is done by undersampling and the implemented FFT. Various factors, such as the non-uniform amplitude of the input signal across the frequency spectrum and the influence of spectral leakage, are considered. Consequently, adjustments are made to maintain a consistent 1V peak-to-peak amplitude for the input, and the input frequency is trimmed to be precisely on one frequency bin.

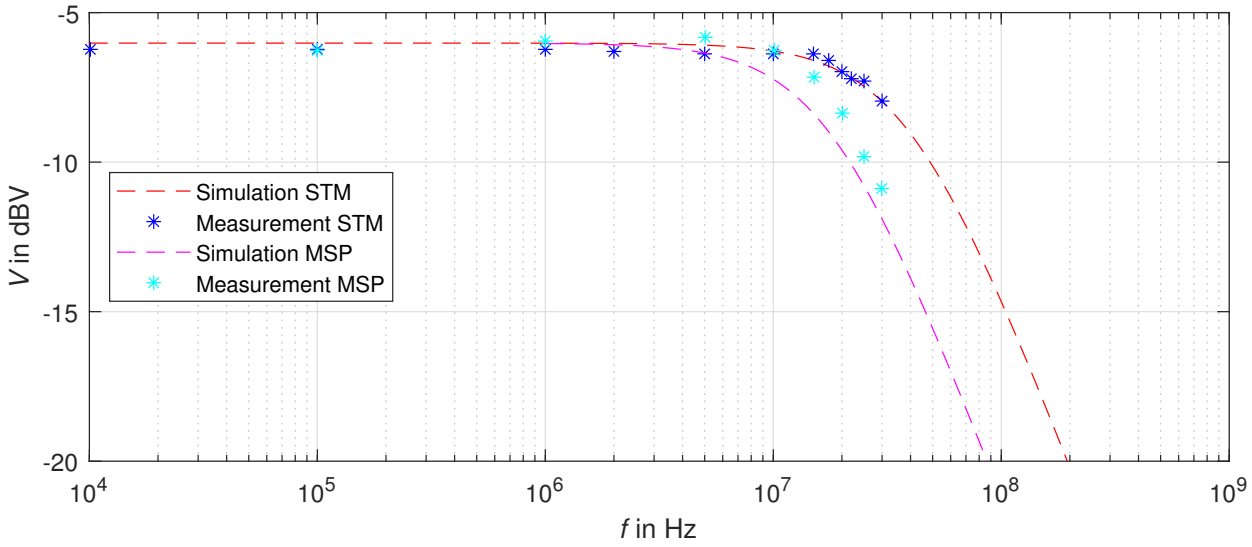

Figure 3.7: Measured analog bandwidth of the STM32L476RG and MSP430FR2355 onboard-ADC together with simulated bandwidth; STM32 consisting of $R_{in} = 800\,\Omega$, $C_{ADC} = 5\,\text{pF}$, MSP consisting of $R_{in} = 2000\,\Omega$, $C_{ADC} = 4.5\,\text{pF}$

3.2.2 Effects on Sampling due to Clock Jitter

A fundamental prerequisite for sampling is the presence of a stable ADC core and sampling clock. The nomenclature characterizes the ADC core clock as the one used for sampling the analog signal and its conversion into a digital representation. In contrast, the sampling clock is synonymous with the sampling period. For a meaningful frequency analysis of sampled data using the FFT, it is crucial to have a uniform sampling period for the data points. Minimal jitter in the sampling frequency will not affect the frequency representation, because, due to discrete frequency bins, minimal shifts will be merged into the same frequency bin.

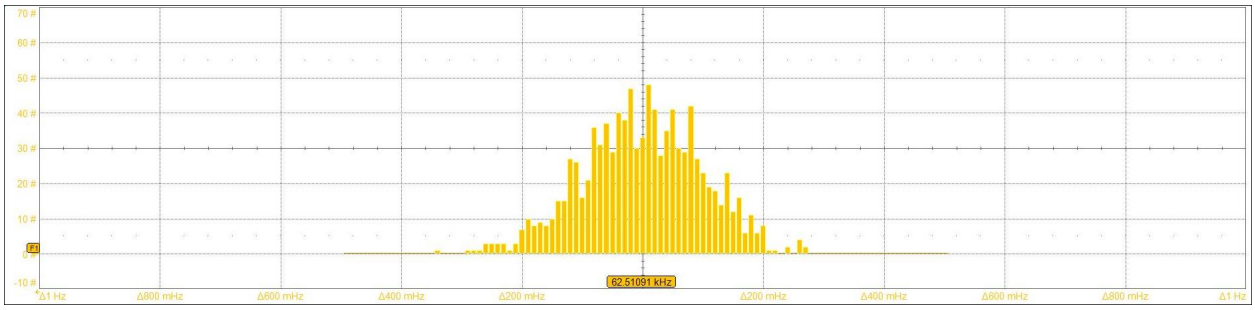

Figure 3.8: Histogram of sampling frequency jitter with external crystal as main clock source, TI controller; Distribution in the mHz range; main horizontal frequency division in 200 mHz

However, in undersampling applications, especially with high undersampling rates, a minimal

jitter will significantly affect the frequency analysis because the frequency jitter will be multiplied by the undersampling factor. The product of this multiplication manifests as observable frequency fluctuations across multiple bins within the Nyquist bandwidth, mainly when the jitter induces a frequency variation that exceeds the resolution of the FFT. This effect is illustrated in the subsequent section 3.2.3, especially in Fig. 3.10 and Fig. 3.11, where two measurements are conducted—one employing oversampling and the other involving significant undersampling. Both measurements are carried out through a practical investigation using the STM32 controller. Each figure shows how a stable clock from an external crystal and a jittered clock from the internal oscillator influence the FFT analysis.

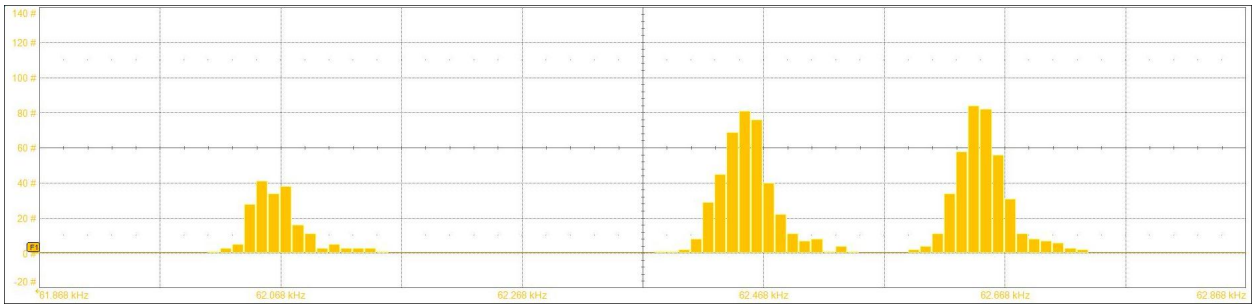

Figure 3.9: Histogram of sampling frequency jitter with internal oscillator as main clock source, TI controller, Distribution in the Hz range; main horizontal frequency division in 100 Hz

In order to manifest the jitter of the ADC sampling frequency, a General Purpose Input Output (GPIO) pin in the ADC's Interrupt Service Routine (ISR) will be toggled. The measurement procedure was done with two different configurations, once using the internal MCU oscillator and a PLL to reach 20 MHZ and once with an external 20 MHz crystal oscillator. The sampling frequency is set to $f_s = 125\,\text{kHz}$, toggling a GPIO after each conversion will result in halved frequency. Figure 3.8 and 3.9 demonstrate how the usage of a crystal will influence the normal distribution of the measured frequency, plotted in a histogram. With crystal, the standard deviation is in the mHz range, whereas the distribution of using an internal oscillator leads to a deviation in the two-digit herz range. The behavior observed in Figure 3.9, in which three curves appear shifted by around 200 Hz and -400 Hz, can be explained by the offset of one or two master clock cycles.

3.2.3 Real-Time Data Visualization Tool for Sampled Data

The strategy of digitizing analog data through undersampling necessitated the development of a tool for the early-stage assessment and in-depth data analysis. This step was crucial to verify the practical feasibility of the approach within the initial phases of the thesis. Therefore, the following

setup was created: The microcontroller performs undersampling of the analog signal, transmitting continuous data to a PC through a USB connection. On the PC side, a Python script listens to the specific COM port, reads the data from the controller, computes the voltage values based on known resolution and reference voltage, and stores the data in a file. This script can read data simultaneously for multiple controllers, such as for the STM and TI development board.

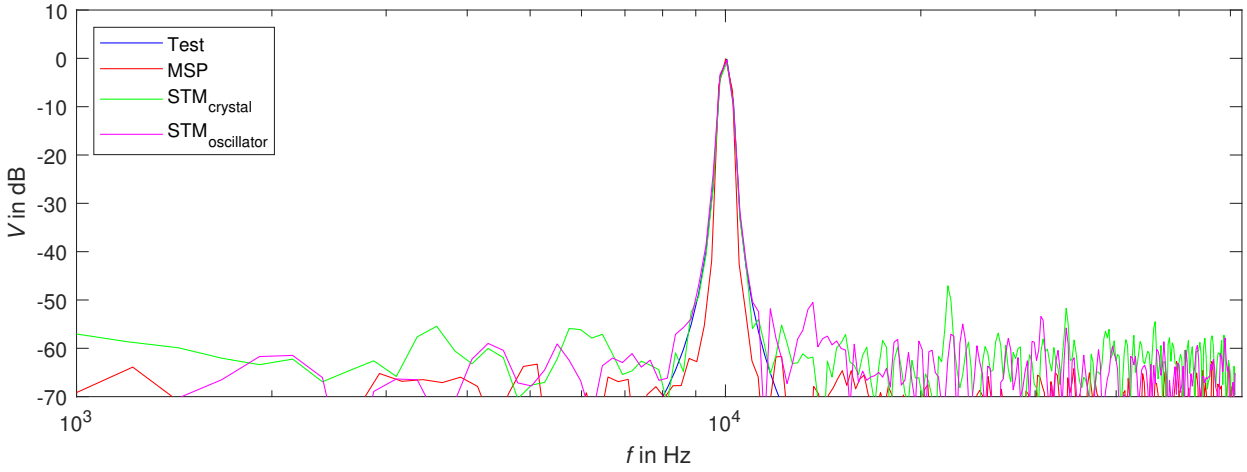

Figure 3.10: Snapshot of real-time visualization tool, plotted FFT result, oversampling applied with $f = 10\,\text{kHz}$ input frequency, sample frequency is greater than 120 kHz; $V_p = 1V$.

The temporarily stored data is further analyzed in Matlab, providing better evaluation and visual presentation possibilities. The primary analyses are performed by the FFT, where multiple optional features like zero padding, applying different window functions, adding different noise distributions, or simulating the sampling frequency's clock jitter is possible. Subsequently, the outcomes from both controllers are visualized in real-time, complemented by a synthesized test signal for comparative analysis. The live plot allows frequency exploration, beginning from the oversampling spectrum and progressively transitioning to undersampling through incremental frequency adjustments.

The most exciting findings emerge when using three microcontrollers, one STM derivate with external crystal and one with internal oscillation configuration, and a TI development board (with external crystal). As seen in Fig. 3.10 operating in the oversampling range, all controllers deliver the same output. However, by increasing the frequency, it is seeable how the ADC clock jitter is influencing the FFT results. The original one-bin result is spread over multiple frequency bins and can no longer reconstruct the input frequency. Such behavior is shown in Fig. 3.11, where the analog bandwidth of the ADC is already a limitation factor regarding amplitude. Due to the measurement results, it is evident that the TIs ADC provides a lower analog bandwidth than the

STM controller.

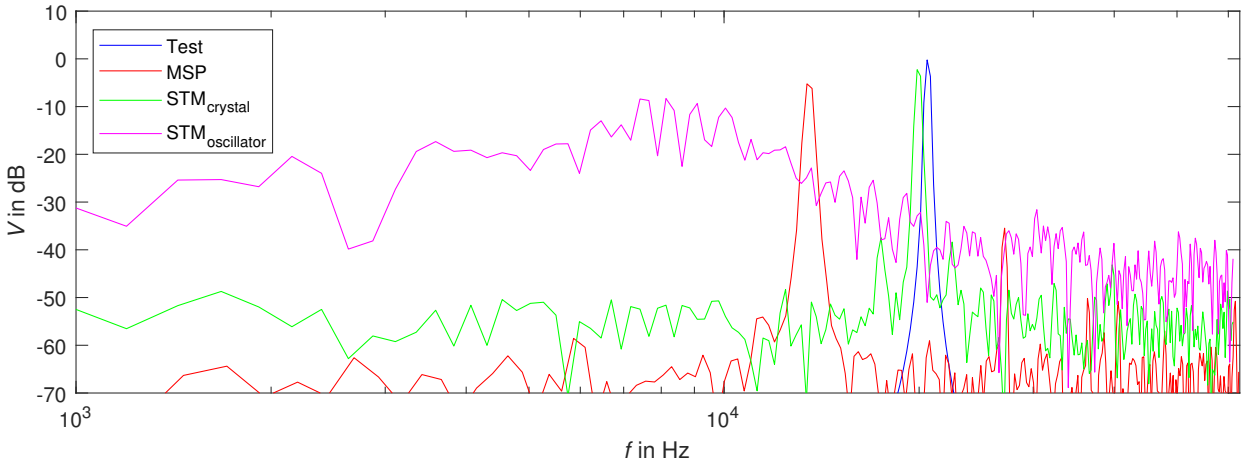

Figure 3.11: Snapshot of applied undersampling with $f = 19.99\,\text{MHz}$ input frequency; STM and TI results in different Nyquist frequencies due to minimal different sampling frequencies ($f_{s,STM} = 122.51\,\text{kHz}$, $f_{s,TI} = 125.0\,\text{kHz}$); $V_p = 1V$

3.2.4 Evalution of the Measurement Signal

The noise and the contributed harmonic distortions through the amplifiers in the measurement signal will generally influence the signal evaluation. By undersampling, the complete bandwidth of the signal will be shifted into the Nyquist bandwidth. Compared to noise, which will lower the SNR heavily, the harmonic distortions are not that disadvantageous. This is because the second or third harmonic distortions do not exhibit a periodicity aligned with multiples of the sampling frequency, which implies that the carrier frequency cannot be merged into a single frequency bin together with second or third harmonics.

Amplitude Relation of FFT Result

The absolute signal amplitude can only be ascertained by appropriately scaling the output of the FFT, while considering the application of zero padding and/or a window function. In the mathematical formulation of the FFT, the magnitude of frequency bins is not equal to the input signal amplitude. When the input frequency precisely aligns with a single bin, the bin level is scaled according to Eq. 3.4; otherwise, the bin level is reduced further. Thus, it is possible to compute the original input signal amplitude by using the factor $2\frac{1}{A}$ through back-calculation. When applying a Hanning window function (Eq. 3.5) to the sampled data, the function will additionally scale the frequency bin by 1/2. Thus, the bin level must be further multiplied by a factor of 2 for

back-calculation.

$$|X(k)| = \frac{1}{2} A \cdot N \tag{3.4}$$

$$w(n) = \frac{1}{2}\left[1 - cos\left(\frac{2\pi n}{N-1}\right)\right] \tag{3.5}$$

3.3 Board Layout

The discussion was to design a single board containing the sensor unit, all other required electrical circuits and a development board with the microcontroller, which can be plugged onto the main board. The designed board is visible in Fig. 3.12, with a relatively simple layer stack consisting of only two layers and a 1.55mm thick FR4 core material. Generally, a large polygon with ground potential was placed over the top and bottom layers. To avoid ground islands and to reach minimal potential differences on the ground planes, generous ground vias are placed. Furthermore, the specified technology class 6C from Eurocircuits is used as a reference, including the pattern and drill class definition.

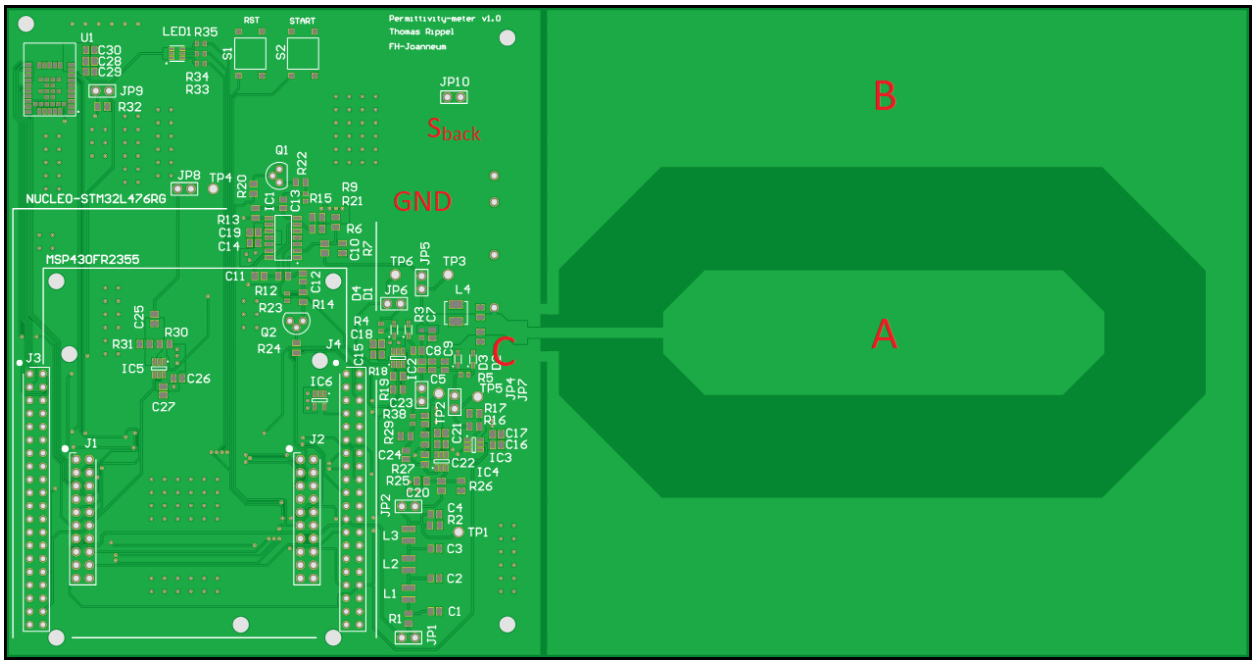

Figure 3.12: Designed board with all required component circuits and directly connected sensor unit; Overall dimension 240x125 mm, sensor unit 135x125 mm; labels define the explained capacitances (section 3.3.2) between top and bottom layer, S_{back} is used to connect or disconnect the backplane polygon to ground

3.3.1 Component Arrangement

The challenging task regarding component placement of this board design is finding an appropriate place for the relatively large development boards. Firstly, the microcontroller should not interfere with the highly sensitive notch circuit. Secondly, the signal path of the 20 MHz signal, starting from a microcontroller output, going through the sinewave filter and the pre-amplifier, passing the notch filter and the two-stage gain amplifier and finally reaching again the microcontroller should be short. Last but not least, the individual component groups, especially the placed test points, should be accessible for measurements through oscilloscope probes, which excludes placing the circuits under the development board. Therefore, the placement of the individual groups is performed as visible in Fig. 3.13.

In addition to the placed test points, Fig. 3.13 shows several Jumper connections between each component group. These easy removable connections allow the isolated operation of each component group. This approach effectively allows the exclusion of a group, meaning skipping a specific group in the previously explained signal pipeline. The primarily used microcontroller board is the NUCLEO STM32L476RG from STM. However, the board design allows the usage of the MSP4302355 development kit from TI, including a dual routing of all microcontroller pins connections to both microcontroller boards. Boundary lines on the top overlay indicate the individual form factor of the two development boards. The highlighted area in Fig. 3.13 shows the power supply polygon with 5 V operational voltage.

3.3.2 Sensor Capacitance

Calculated Capacitance

The principle structure of the sensor capacity is already defined in section 2.1.2. However, now the sensor-specific values are inserted and an additional capacity C_C is added, but with minimal influence. With a relative permittivity of the core material of $\epsilon_r \approx 4$ according to the manufacturer, the following capacitances shown in Tab. 3.3 are available. The connection of these four capacitances depends on whether the rear backplane is electrically connected to the common ground or floating. In the case of backplane connection, capacitance A and C are connected in parallel, which results in $C_{calc,con} = 47.0\,\text{pF}$. In contrast, the sensor capacitance is lowered to $C_{calc,float} = 39.3\,\text{pF}$ when the backplane is floating because now A and B are in series, which leads to capacitance reduction. The capacitance difference of $\Delta C_{calc} = 7.66\,\text{pF}$ will influence the notch filter by shifting the resonant frequency.

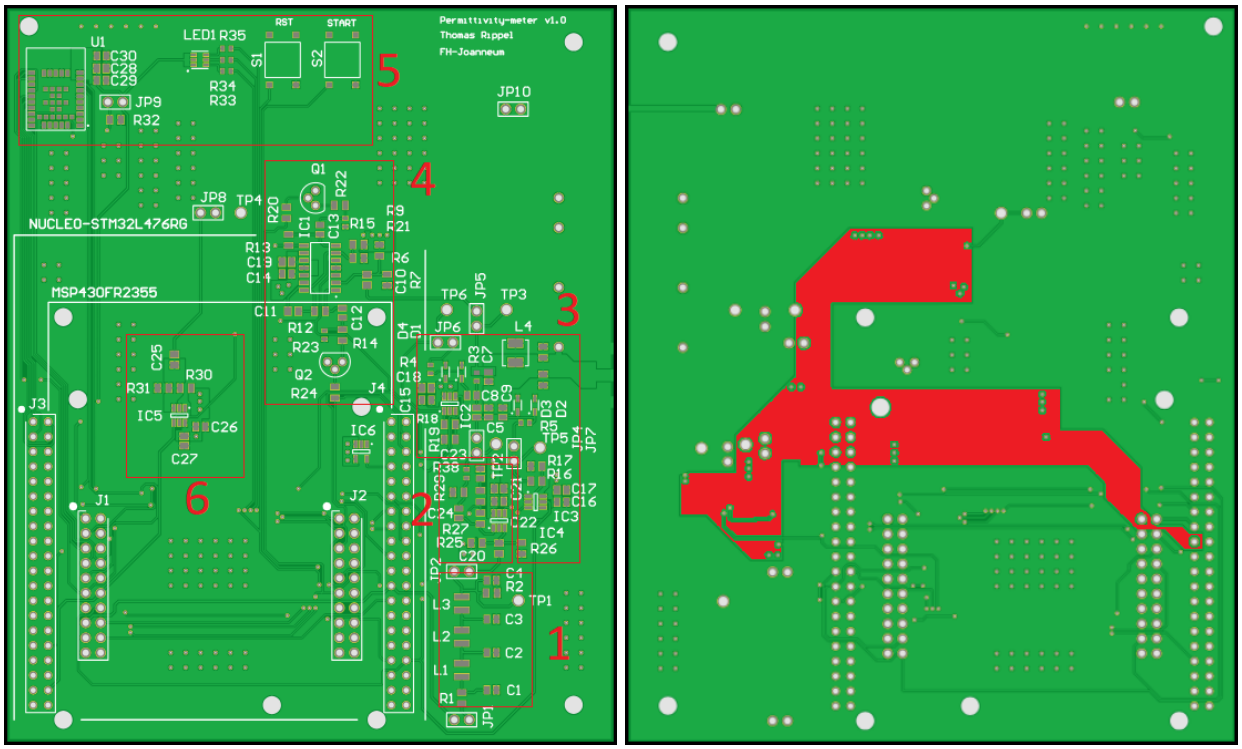

Figure 3.13: Detailed view on the top (left) and bottom (right) layer of the circuit area; Left shows the individual component groups [1, sinewave filter; 2, preamplifier stage; 3, Notch filter together with the two varactor amplifiers; 4, two-stage amplifier with switchable gain; 5, user interaction; 6: DC level adjustment for ADC input]; red colored 5 V polygon on bottom layer

Measured Capacitance

The calculated capacitance can be verified by the measurement results from 3.14, where the capacitances for connected and floating backplane is $C_{meas,float} \approx 55\,\text{pF}$ and $C_{meas,con} = 45\,\text{pF}$. The difference between connected and floating backplanes leads to $\Delta C_{meas} = 10\,\text{pF}$. The comparison between calculated and measured absolute capacitance values shows a significant offset, whereas the values for the capacitance difference ΔC are in the same area of magnitude.

To determine the concrete frequency shift, the capacities of the notch filter must be taken into account too. Therefore, a practical measurement will be consulted. Figure 3.15 shows the concrete influence of the backplane connection to the resonant frequency. The resonant frequency is again defined by Eq. 3.6 and the capacitance can be computed with Eq. 3.7 through conversion. With a numerical inductor value $L = 680\,\text{nH}$, the two capacitances resulting in $C_{max}(f_r = 17.56\,\text{M}) = 120.80\,\text{pF}$ and $C_{min}(f_r = 18.29\,\text{M}) = 111.35\,\text{pF}$. The capacitance difference between the floating backplane and the connected to ground determined based on the resonant frequency shift is $\Delta C_{shift} = 9.45\,\text{pF}$.

Table 3.3: Calculated capacitances of PCB polygons; labels are according to Fig. 3.12; * value for C_{diff} (between the inner and outer electrode of the top layer) is taken from the master thesis of Stefan Dierer [4];

Label	Area in mm^2	Capacity in pF	Comment
A (C_A)	1.97E-03	44.9	sensor front inner
B (C_B)	9.56E-03	218.5	sensor front outer
C (C_C)	9.00E-05	2.06	notch filter polygon
diff (C_{diff})	-	1.0 *	differential capacitance

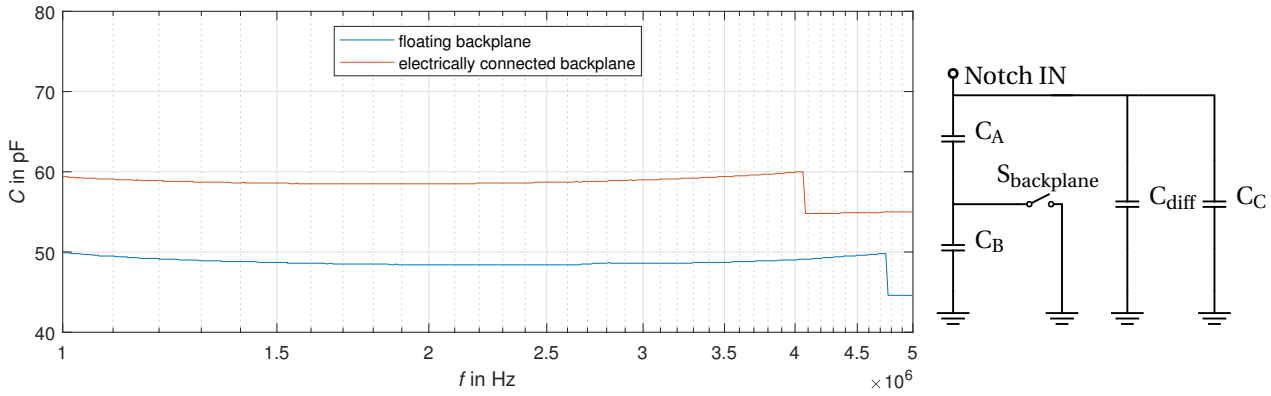

Figure 3.14: Left: measured PCB capacitance with Impedance Analyzer for connected and floating backplane; non-assembled CB used; Right: PCB capacitances circuit; If backplane is connected to ground, C_B is shorten and therefore overall C increases; C_A between sensor front inner and backplane, C_B between backplane, sensor front outer and C_C between notch filter polygon and ground plane and C_{diff} between the inner and outer electrode of the top layer.

$$f_r = \frac{1}{2\pi\sqrt{LC}} \tag{3.6}$$

$$C = \left(\frac{1}{2\pi f_r \sqrt{L}}\right)^2 \tag{3.7}$$

$$C_{max,shift}(f_r = 17.56\,\mathrm{M}) = 120.80\,\mathrm{pF} \tag{3.8}$$

$$C_{min,shift}(f_r = 18.29\,\mathrm{M}) = 111.35\,\mathrm{pF} \tag{3.9}$$

$$\Delta C_{shift} = 9.45\,\mathrm{pF} \tag{3.10}$$

Intepretiaon of the Sensor Capacitance

The conclusion of the obtained capacitance investigations can be summarized in the following words. The difference between connected and floating backplanes is in the range between 7.66 pF and 10 pF (Eg. 3.11). The absolute values for the capacitance differ. Hence, the first measurement by the impedance analyzer and the calculation is done with a non-assembled board, considering purely the PCB structure. In contrast, the measurement regarding resonant frequency shift involves the capacitacnes from the notch circuit too.

This measurement can also provide absolute values for the sensor capacitance but with the following note: The capacitances generated by the layer structure and specific components of the notch circuit exhibit a constant ϵ_r, which is independent of the exposed snow sample! A completely different behavior shows the capacitance $C_{diff,m}$. Its capacitance is mainly defined by the specific ϵ_r of the snow sample!

$$\Delta C_{calc} \approx \Delta C_{meas} =\approx \Delta C_{shift} \approx 7.66\,\text{pF to}\,10\,\text{pF} \tag{3.11}$$

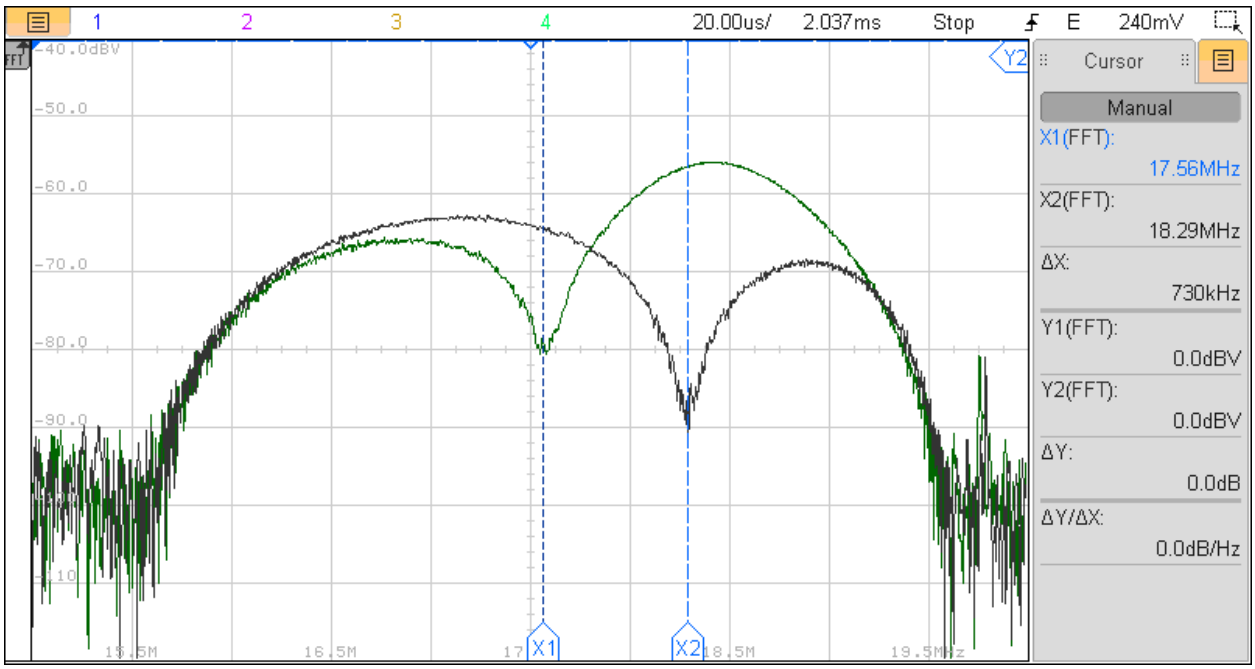

Figure 3.15: Resonant frequency of the notch circuit depending on whether backplane is connected or not; $f_{r,con} = 17.56\,\text{MHz}$, $f_{r,float} = 18.29\,\text{MHz}$, difference of $\Delta f_r = 730\,\text{kHz}$.

3.4 Microcontroller and Firmware-Implementation

3.4.1 Microcontroller Development Board

The decision to use a development board was made because the development focus can be placed on the Permittivity Meter, and the firmware implementation is easy to debug. Two development boards, the NUCLEO STM32L476RG [18] and the MSP4302355FR were initially considered, whereby the focus is set on the STM derivate. This controller board provides all required modules and satisfies low power considerations. Different sleep modes are available, whereby the STOP2 mode decreases the current consumption into the single-digit µA range, with concurrent Random Access Memory (RAM) memory retention. The onboard Real Time Clock (RTC) allows waking up the board regularly to execute measurements, followed by going to sleep again. Minor modifications are needed to use the board for the following project. First, a 20 MHz crystal is added, with suitable external capacitances to the prepared X3 component pads. Second, the default configuration connects the analog reference voltage to V_{DD}, corresponding to 3.3 V. Removing the solder bridge SB57 allows an external component to supply the analog reference [18]. The whole Permittivity Meter board will be sourced by USB power.

3.4.2 Layer Overview

Descending on the designed board, the microcontroller and the firmware running on it are the centerpieces of the Permittivity Meter. As the board supports a STM and a TI controller, the firmware development must strictly follow the aim of abstracted software layers. This abstraction defines three layers, starting with the hardware layer (HL) as the lowest. The hardware layer holds all source files with controller-specific content, mostly to initialize the hardware-related modules, such as the clock system, the ADC, the DAC, the Direct Memory Access (DMA) controller, the Universal Asynchronous Receiver/Transmitter (UART) interface and the GPIO configuration. The heading of the hardware layer is the source code bundle "hl_general", which includes all hardware initialization steps and provides a function to initial them in the correct order. The manufacturer-supplied controller-specific driver layer provides a comprehensive suite of functions facilitating hardware initialization. This approach eliminates the need for direct manipulation of special configuration registers and enables a more abstract and user-friendly interface.

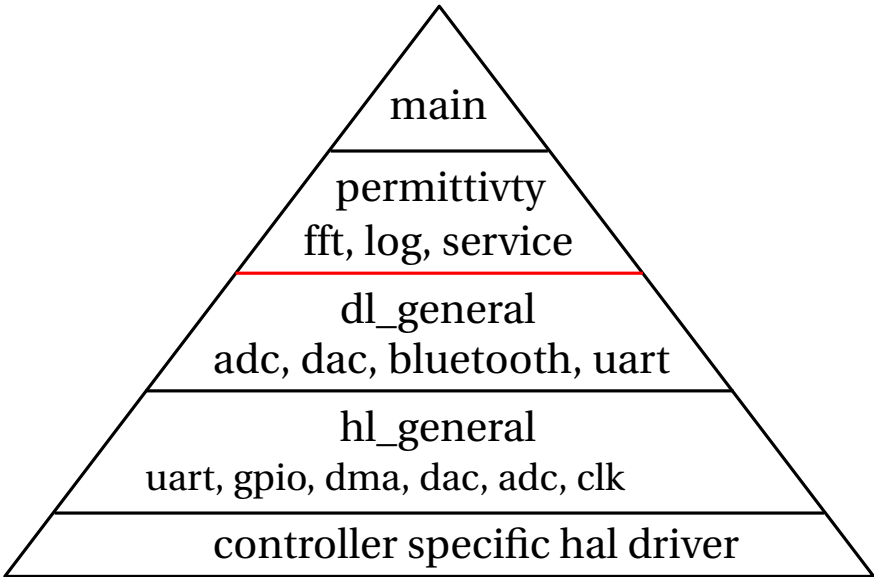

Figure 3.16: Firmware layer overview, clear separation between hardware and application-related implementation

3.4.3 Utilized Hardware Modules

Implementing the initialization of hardware modules includes the correct configuration via memory registers, which is quite time-consuming because the individual register usage must be checked via browsing the user guide. This process can be massively accelerated by the provision of configuration software by the manufacturer. STM provides a graphical user interface solution where the user can configure any controller with the desired configuration. Based on the setup, the software will produce corresponding source and header bundles for each module. This approach allows a focus on the user application implementation and enables the hardware configuration to be changed later with just a few clicks. It necessitates a clear division between automatically generated and manually written code. Special designated sections within the generated source files allow the insertion of user-specific code, ensuring its preservation during the regeneration of the hardware layer modules.

The requisite hardware modules are nearly identical for both the STM and TI devices, with the notable exception of the DMA module, because the MSP430 derivate does not provide such a feature. Therefore, the following hardware module descriptions only refer to the STM controller. The general voltage of the analog input and outputs is defined either via the power supply voltage of 3.3V or by using an external reference voltage. The latter is the case here, with a reference voltage $U_{ref} = 2.5\text{V}$, limiting the ADC input and the DAC output to this voltage level.

Clock System

The clock module mainly defines the clock source for the master clock system. The controller allows the usage of internal RC oscillators, but the undersampling application requires a highly stable clock. Therefore, the external high-speed input is used, with an external crystal running at 20 MHz. The crystal frequency can internally be increased by PLL to reach master clock frequencies up to 80 MHz. The concrete master clock frequency depends on the required notch filter signal frequency, which the controller provides. The configuration of a dedicated clock multiplexer enables the output of the master clock to a controller pin. An available frequency scaler allows scaling the high frequency to the desired range. The notch filter was initially designed for a resonant frequency of 20 MHz. Due to the visible resonant frequency shift of the designed board, the output frequency can be decreased to 17.5 MHz by using a reduced master clock of 70 MHz and an output scaler of four. Figure A.2 shows the clock output signal, once without load and once with a connected sinewave filter input. By loading the system with $R_l = 200\,\Omega$, the signal level is minimally reduced to approximately 3V.

ADC and DMA

Apart from the ADC module, the sampling process includes an DMA, which allows transferring the sampled data without any Central Processing Unit (CPU) consumption to a desired memory section. An additional timer module will trigger the recording of a configurable bundle of sampling points in a regular interval. The ADC is configured in single-ended mode, with 12-bit resolution. Activating the continuous conversion mode makes an external trigger superfluous, as the ADC triggers itself after an adjustable sampling plus constant conversion time. The conversion time is fixed to 12.5 cycles, whereas the choosable sample cycles are mentioned in Tab. 2.1 in section 2.4.3. The sample period is computable with the selected ADC core clock.

The sampling process starts via a provided hardware layer function, including the activation of the DMA and overhanding two parameters. First, a pointer to the desired memory address and second the number of sample points is required. On reaching the desired amount of points, the "Conversion-Complete" callback function will be executed, where the DMA is stopped and a ready flag is set. This flag signals the existence of recently sampled data to a higher software layer.

UART Interface

Two UART UART interfaces are used simultaneously; one is used for user interaction and is connected to the USB port of the development kit, and the other is for data exchange with the Bluetooth

module. Through the code in List. 3.1, the standard output is redirected the corresponding UART interface. Changing line 6 to huart1 will redirect the data to the Bluetooth module.

Listing 3.1: Redirecting stdout to UART interface

```
1
2       #include <stdio.h>
3       #define PUTCHAR_PROTOTYPE int __io_putchar(int ch)
4
5       PUTCHAR_PROTOTYPE {
6         HAL_UART_Transmit(&huart2, (uint8_t*) &ch, 1, HAL_MAX_DELAY);
7         return ch;
8       }
```

3.4.4 Introducing the Driver Layer

As the name already suggests, this layer provides drivers to the above layers, aiming the same goal as device drivers in operating systems: the driver user does not carry which actual hardware is executing or how the hardware is implementing things. All interactions with hardware must be encapsulated in the drivers. Therefore, these drivers must be written for both, the STM and the TI controllers but with one thing in common: the provided functions to the higher layers are the same. The driver layer header files will be identical for different controller implementations; therefore, individually included header files are not allowed.

Device drivers are written for the ADC, the DAC, the UART and the Bluetooth module. Additionally, a general device driver is offered for switching GPIO pins according to their feature, including turning the gain stage one and two either on or off, generally powering all OpAmps on or off, activating or deactivating the master clock output, lighting the status LED in a desired color and initiating a system reboot in case of issues.

For example, the DAC driver facilitates the input of a millivolt value, along with the specified channel name, and manages the conversion process, encompassing considerations such as resolution and reference voltage. Another illustrative example is the UART driver, designed not only to facilitate the transmission of data but also to oversee the data reception process. The driver systematically gathers all incoming packets and sends a notification to the user upon detecting an end-of-line character. Subsequently, the user can process the received data, conveniently treating it as an array or string.

3.4.5 Application Layer

Due to the strict separation between hardware and application software, the following explained code bundles can be used independently from the controller. The application layer includes the following bundles:

- A logger with different log levels
- The FFT algorithm
- A service command module for parsing user commands
- A Permittivity-Meter specific module

Fast Fourier Implementation

The FFT module includes several functions, which can be explained by looking at the data processing pipeline. Raw data are preprocessed from the ADC or an available dummy data array. Preprocessing includes the optional usage of a window function, especially a Hanning window, and moves on to scramble the data. Scrambling the raw data facilitates handling the frequency domain result of the FFT so that the individual frequency components are sorted in the correct order. The next step involves the transformation from time to frequency domain, using the radix-2 decimation in time FFT [14]. As seen in List. 3.2, the used algorithm is an in-place process. The complex twiddle factors have been computed beforehand with a Matlab script, scaled by 2^{12} and stored in a dedicated flash memory page (explicitly defined in the linker script). This scaling is responsible for the shift of the computed result in line 18. The FFT algorithm output consists of complex values. The power spectrum is reached by adding up their squares, and an additional square root achieves the voltage conversion. Using a peak finder algorithm, the major frequency component and the related amplitude can be found, shown in millivolt or dBV. Verifying the computed result can be easily done by using the already mentioned dummy data array, generated by a Matlab script with $f = 10.049\,\text{kHz}$, $U_{peak} = 1\,\text{V}$ and a DC offset of $U_{DC} = 1.25\,\text{V}$.

Listing 3.2: Implementation of the radix-2 FFT algorithm

```
1
2       void AL_FFT_fft(complex32_t* data, uint16_t len)
3   {
4     uint16_t stage = len;
5     uint16_t half = 1;
```

```
6     uint16_t pos =0;
7     uint16_t k =0;
8     complex32_t temp = {0,0};
9
10    while(stage > 1)
11    {
12      for(short index=0; index < len; index += half<<1)
13      {
14        for(short n=0; n < half; n++)
15        {
16          pos=index +n;
17          k = n*(stage/2);
18          temp.re = (data[pos+half].re * twiddle_arr[k*TWIDDLE_FACTORS_FRACT].re
                - data[pos+half].im * twiddle_arr[k*TWIDDLE_FACTORS_FRACT].im)
                >>12;
19          temp.im = (data[pos+half].im * twiddle_arr[k*TWIDDLE_FACTORS_FRACT].re
                + data[pos+half].re * twiddle_arr[k*TWIDDLE_FACTORS_FRACT].im)
                >>12;
20
21          data[pos+half].re = (data[pos].re - temp.re)>>1;
22          data[pos+half].im = (data[pos].im - temp.im)>>1;
23
24          data[pos].re = (data[pos].re + temp.re)>>1;
25          data[pos].im = (data[pos].im + temp.im)>>1;
26        }
27      }
28      half= half<<1;
29      stage = stage >> 1;
30    }
31  }
```

Service Command Interface

The primary function of the service command interface is to receive user commands, currently utilizing the UART driver module exclusively. User commands are transmitted in string format and may include up to three additional arguments besides the primary command. Due to variations in command and argument lengths, the received character stream undergoes initial segmentation based on whitespaces. The individual character sequences are then copied to dynamically allocated memory, whereby the pointer to the first character of each character sequence is included in an array. A query logic then determines the appropriate command-related function to execute. The allocated memory is released after each command execution. Table 3.4 provides an overview of available commands. With the integration of an additional Bluetooth module bundle, the service commands can be accessed through both interfaces: UART and Bluetooth.

Table 3.4: Overview of available commands used to interact with the Permittivity-Meter

Command	Arg1	Arg2	Description
exit			Exit the command mode
nina	<x>		Forware command to the Bluetooth module
fft			Execute the FFT based on the sample points
loop			Continuously sampling and FFT computation
pc			Continuously sampling and sending datapoint to the PC
dummy			Perform FFT analysis based on dummy data
dummy	loop		Continuously send data dummy data to the PC
op<x>	on		Switch gain of OpAmp 1/2 to high
op<x>	off		Switch gain of OpAmp 1/2 to low
ch<x>	sweep	up	Sweep diode voltage from current level to 0, 250mV interval
ch<x>	sweep	down	Sweep diode voltage from current level to 5V, 250mV interval
ch<x>	<value>		Individually increment or decrement diode voltage 1/2
reboot			Reboot the system (MCU)
minima			Tune circuit back to calibration point (ϵ_r')
diff			Tune circuit back to calibration point (ϵ_r'')
epsilon			Tune circuit back to calibration point for ϵ_r' and ϵ_r''
calib			Calibration
clkon			Activate clock output

Permitiivity Application

The Permittivity-Meter application-specific part forms the head of the FW implementation. The primary objective of this implementation is to furnish the user with an outcome delineating both the real and imaginary components of the relative permittivity of the analyzed medium. The current firmware implementation cannot fulfill this goal as a whole. The foundational methodology for ascertaining ϵ_r' and ϵ_r'' is anchored in the tuning procedure, yielding paired outcomes: the voltages of D1 and D2. The voltage difference between the obtained diode voltages and those from calibration can be converted into a capacitance difference through the relation between diode voltage and capacitance (section 2.3.1). The real part of ϵ_r can be easily determined, whereas the ϵ_r'' is much more challenging to determine. Therefore, the computation of ϵ_r'' could not be implemented yet.

Normalized Amplitude and automatically switched Gain

The designed switchable amplifier allows four different configuration states: both on, both off, first off & second on, first on & second off. The firmware implementation defines a valid signal amplitude's upper and lower limits. A function called AL_PERMITIVITY_OptimalAmplitude() provides logic to automatically get an amplitude within the range of interest by switching the amplifier state. The current amplifier status is saved in addition to the amplitude value to enable a later comparison. Storing all relevant data is accomplished by the data structure listed in List. 3.4, an extension of the basic FFT result struct shown in List. 3.3. The amplitude conversion is only

carried out when the amplitude value is read. The function AL_PERMITTIVITY_GetNormalizedAmplitude() converts the raw measurement amplitude to a normalized one using the pre-saved individual gain values.

Listing 3.3: Typdef struct to quantify the FFT frequency components

```
1  typedef struct{
2    uint16_t amplitude;
3    uint16_t pos;
4  }peak_t;
```

Listing 3.4: Typdef struct to quantify the current notch filter behavior

```
1  typedef struct {
2  peak_t peak;
3  gainState_t gainState;
4  uint16_t ch1;
5  uint16_t ch2;
6  } notch_t;
```

Calibration

Before measuring any snow samples, a calibration step is required by exposing the sensor unit to air. The calibration procedure will store the initial amplitude, which can be later used as a reference. In order to get accurate measurement results, the AL_PERMITTIVITY_FindRealMinimum() function is executed before saving the initial state of the notch circuit (List. 3.5). After trimming the circuit to the minimal possible signal amplitude, the AL_PERMITTIVITY_CalibrationIntern() function will set the diode voltage D2 to 5 V and store the actual measurable amplitude value together with the gain state into a global variable.

Listing 3.5: Calibration function of the permittivity application

```
1  void AL_PERMITTIVITY_Calibration(void)
2  {
3    AL_PERMITTIVITY_FindRealMinimum();
4    AL_PERMITTIVITY_CalibrationIntern();
5  }
```

Notch Filter Compensation

After the calibration, the sensor can be exposed to the measurement sample, which leads to a modified notch filter frequency response. Tuning the circuit back to the calibration point starts with the execution of AL_PERMITTIVITY_FindRealMinimum() and AL_PERMITTIVITY_-FindImaginaryPart().

Finding the real minimum is done in an interactive process, sweeping over the whole D1 voltage range with a rough voltage increment of 400 mV. A logic within the performed loop will temporarily save the minimum achievable voltage amplitude. In the subsequent interactions, the incremental voltage value is decreased to 20%, simultaneously downsizing the sweep interval. This procedure combines the rough search and the exact determination.

In a second procedure, instead of finding a global minimum, the minimal difference between the actual signal amplitude and the calibration point is of interest, where the code implementation structure is the same as for finding the real minimum. Both tuning functions are executed twice because the imaginary part will also magically influence the resonant frequency (List. 3.6).

Listing 3.6: Tuning the notch curcuit back to the calibration point

```
1  void AL_PERMITTIVITY_Epsilon(void)
2  {
3     AL_PERMITTIVITY_FindRealMinimum();
4     AL_PERMITTIVITY_FindImaginaryPart();
5     AL_PERMITTIVITY_FindRealMinimum();
6     AL_PERMITTIVITY_FindImaginaryPart();
7
8     logging(INFO, "Measurement result: imag ch1: %4d, real Ch2: %4d",
          AL_PERMITTIVITY_ch1_global, AL_PERMITTIVITY_ch2_global);
9     logging(INFO, "Calibration with: Ch1: %4d, Ch2: %4d", peak_calibration.ch1,
          peak_calibration.ch2);
10 }
```

4

Measurements and System Verification

The last section is dedicated to the verification of the developed Permittivity-Meter. Instead of checking the individual components, the system's overall behavior should be checked from the perspective that a later user will have.

4.1 Lowered Resonant Frequency due to higher Capacitance

The desired sensor unit could not accomplish the nominal target resonant frequency of $f_{tar} = 20\,\text{MHz}$, due to the high interlayer capacitances of the sensor unit. As computed in 3.3.2, the overall capacitance for the resonant circuit results in $C_{max}(f_r = 17.56M) = 120.80pF$ and $C_{min}(f_r = 18.29M) = 111.35pF$, depending whether the backplane is floating or grounded. Therefore, as seen in Fig. 3.15, the configuration with a connected backplane is used for the upcoming measurements. The shifted resonant frequency does not influence the general measurement possibilities of the Permittivity-Meter. By changing the MCU output clock to $f = 17.5\,\text{MHz}$, the system can be used as with 20 MHz input frequency. Alternatively, the inductor size can be further decreased to $L = 560nH$ to tune the circuit back to the original 20 MHz signal.

4.2 Two stage Amplifier Verfication

An essential point is the verification of the two-stage amplifier circuit. The FW application will switch the individual stages on and off, depending on the current signal amplitude. To accurately determine the amplitude, it is essential to ascertain the respective gain values. Initially, the following methodological approach was established: A frequency generator serves as the source for the sinewave filter to ensure a consistent signal amplitude. Subsequently, the actual signal amplitude is measured before the gain stage (notch output) and after the amplifier. Empirical observations revealed that simultaneous utilization of dual probes induced oscillations within the amplifier.

Therefore, both amplitudes are measured with one probe staggered in time.

In order to accurately assess the maximum gain setting, the input signal must possess a comparatively low magnitude to avoid voltage clipping on the amplifier. Direct measurement of this setting in the time domain presents a challenge. Consequently, amplitude determination is conducted utilizing FFT analysis. The recorded amplitudes and associated gain calculations are delineated in Tab. 4.1.

Table 4.1: Measured gains depending on the two-stage amplifier configuration; notch filter included; measured with $f = 20\,\text{MHz}$

Type	V_p **in dBV**	V_p **in mVp**	**Gain**	**Gain in dB**	**relative gain**
Input	-38.56	11.80	-	-	-
Op1 & op2 off	-22.4	75	6.35	16.06	1
Op1 on, op2 off	-10.4	297	25.16	28.02	3.96
Op1 off, op2 on	-11.2	274	23.21	27.32	3.65
Op1 & op2 on	-0.4	1051	89.04	38.99	14.01

Later measurements showed that the probe at the output of the notch filter strongly influenced the measurement. A test measurement demonstrated, without adding the oscilloscope probe to the notch output, the measured voltage at the ADC input was $U = 313\,\text{mV}$. In contrast, by adding the probe, the voltage decreased to $U = 249\,\text{mV}$, resulting in a measurement failure of 20%. The influence of the oscilloscope probe can probably be explained by introducing the 15 pF probe capacity. The calculated absolute gain values are incorrect if this knowledge is applied to the measurements in Tab. 4.1.

An alternative measurement configuration should prevent the occurrence of the effect by bypassing the notch filter. Table 4.2 shows the corrected absolute gains. While the absolute gain values differ between Tab. 4.2 and Tab. 4.1, their relative magnitudes remain approximately consistent, which confirms the measurement's results. Comparing the results from 20 MHz and 17.5 MHz; lower gain for 20 MHz due to GBW limitations when both stages are on; higher gain for 20 MHz when both stages are off(explainable by the frequency behavior of the used BJT, Fig. 3.5).

Table 4.2: Measured gains depending on the two-stage amplifier configuration; notch filter is bypassed through a jumper cable

Type	**Gain in dB (17.5MHz)**	**Gain**	**relative gain**	**Gain in dB (20MHz)**	**Gain**	**relative gain**
Op1 & op2 off	13.75	4.87	1	14.37	5.23	1
Op1 on, op2 off	25	17.78	3.65	25	17.78	3.40
Op1 off, op2 on	24.37	16.54	3.40	24.37	16.54	3.16
Op1 & op2 on	36.25	64.93	13.34	35.9	62.37	11.93

4.3 Influence of the Varactor Diodes on the Notch Filter Behavior

4.3.1 Bodediagram of Notch Filter with Frequency Sweep

The following section will show how changes in the varactor diode voltages influence the notch filter behavior. For clarification, the two varactor diodes are named diode one (D1) and diode two (D2), where D1 will influence the resonant frequency of the notch circuit and is needed for the determination of the real part of ϵ_r. In contrast, D2 will marginally influence the resonant frequency but heavily affect the quality factor and the related amplitude and is needed for tuning the circuit when an imaginary part of ϵ_r is present.

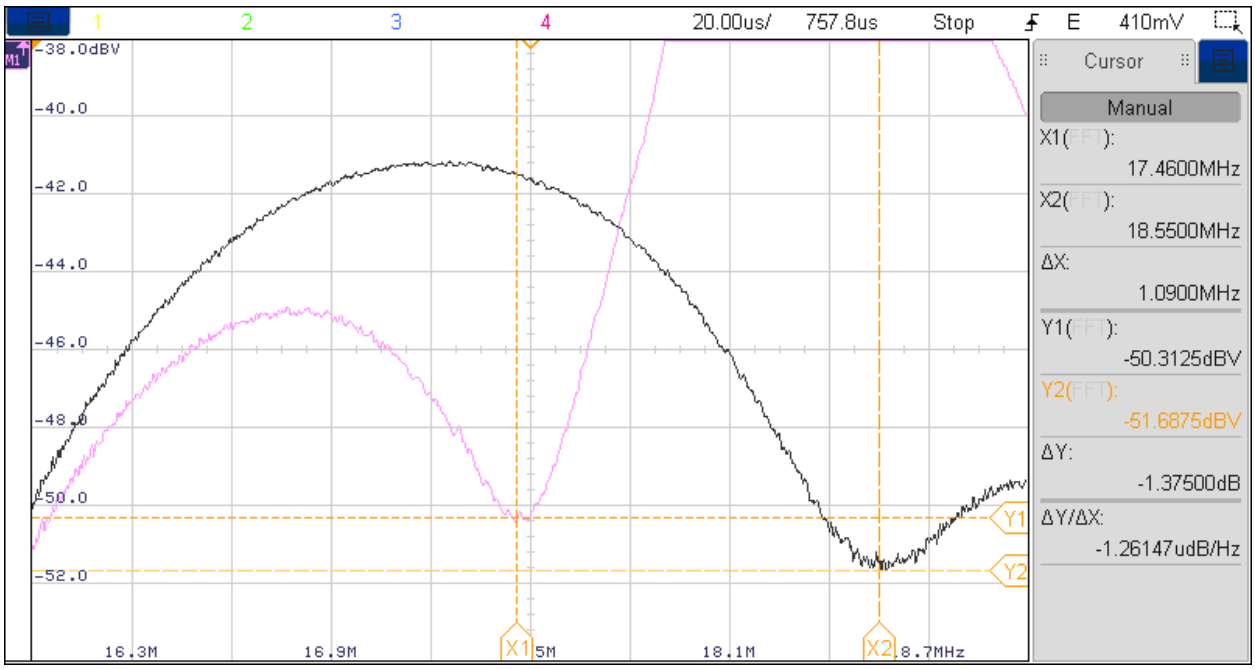

Figure 4.1: Sweep D1 voltage in interval [0 5] V, D2 voltage is set to 0 V; Pink curve represents D1 0 V, black curve D1 5 V;resonant frequency drift by $\Delta f = 1.09\,\text{MHz}$

The measured amplitude values and the illustrated waveform of the recorded frequency responses are not representative. Hence, the measured frequencies are not present over the whole recording, but the FFT is scaling the amplitudes by the number of samples N, and the resulting amplitude is lowered. Secondly, to perform a recording with a high-resolution oscilloscope setting, only a limited interval of frequencies is within the available time frame. This effect is reflected in the following images by lowered amplitude values for frequency components located at the edge. The measurement was performed after the two-stage gain amplifier to avoid the probe influences as explained in section 4.2 by constantly keeping minimal gain to allow comparisons between mea-

surements.

The first sweep by D1 caused a resonant frequency change by $\Delta f = 1.09\,\text{kHz}$, as shown in Fig. 4.1. The D2 voltage is set to 5V before creating the distinctive notch minimum. By changing the voltage level of D2 to 0V, the quality factor gets lowered heavily, and for the shifted resonant frequency, no sharp notch is visible anymore (Fig. A.7).

The subsequent image was created by changing the diode voltage D2, initially starting at 0 V and moving to 5 V. Increasing the voltage of D2 means reducing the diode capacitance, and therefore, the quality factor will rise, which is detectable by the sharp notch curve in Fig. 4.2. The increase in the quality factor is explainable: The D2 diode is not located in the inductor's parallel resonant circuit but on the other side of the twin T-bridge. Hence, when the capacitance of this diode is lowered, the quality improves. This behavior is challenging to quantify using simple equations, primarily due to the complex notch filter's transfer function.

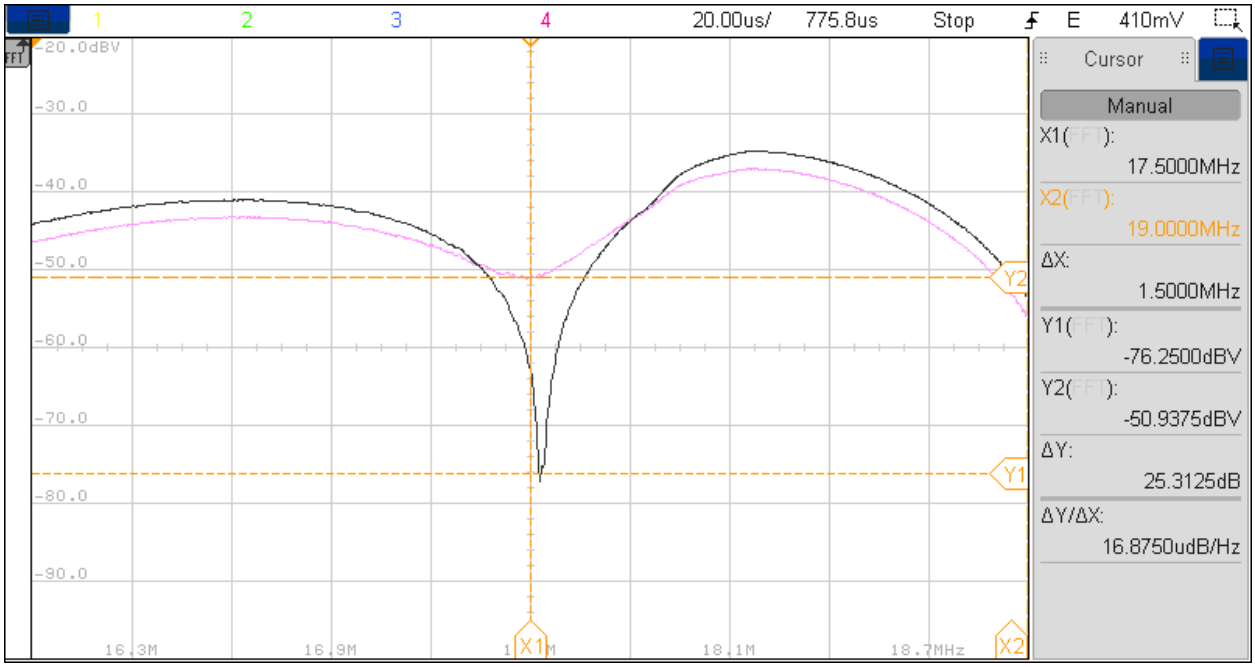

Figure 4.2: Sweep D2 voltage interval [0 5] V; D1 is set to 0 V; Measured amplitude difference is $\Delta V_p = 25,31\,\text{dB}$; pink curve is for 0 V, black for 5V

4.3.2 Measurements with Microcontroller Clock Output

Instead of recording the bode diagram of the notch filter, the input signal is provided by the MCU clock output, and the signal is measured after the two-stage gain amplifier. The gain is permanently reduced to the minimal to allow interplot comparisons (both stages are off). In order to better

recognize the signals on the oscilloscope images, the frequency axis was scaled differently, and the signals appeared next to each other, although in reality, they had the same frequency.

Changing Diode voltage D1 (Resonant Frequency Influence)

Reducing the capacitance of D2 before calibration will form a more distinctive notch in the frequency response. Therefore, when shifting the resonant frequency by diode voltage D1, the difference in the amplitude is much higher. This influence by D1 voltage is presented in Fig. 4.3, with an overall amplitude difference of 19.53 dBV. The amplitude change for voltage variation of D1 (and by setting D2 voltage to 0 V) is much lower, as visible in Fig. A.8.

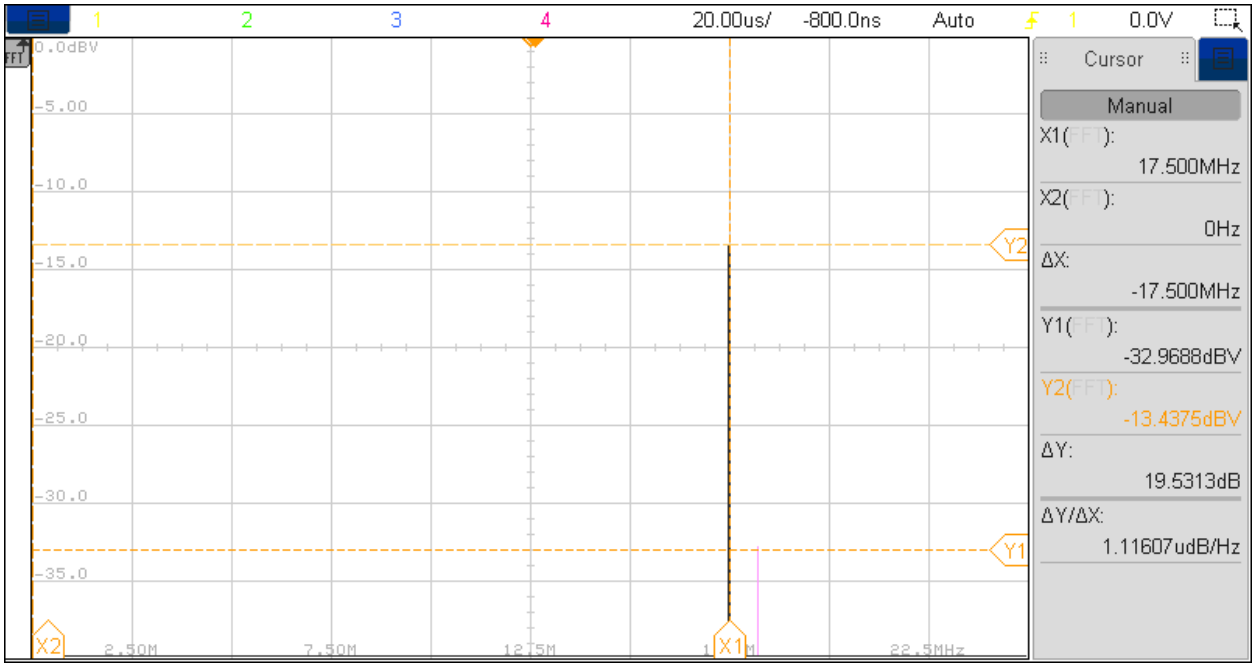

Figure 4.3: Changing D1 voltage from 0 to 5 V, but with D2 is set to 5 V before calibration; Pink curve is calibration of D1 (with D2 set to 5 V), black curve is with D1 set to 5 V; D1 calibration with 90 mV

Changing Diode voltage D2 (Quality Factor Influence)

Figure 4.4 visualizes how the quality factor is increased when decreasing the capacitance of the D2 diode. This diode is not in the parallel resonant circuit of the inductor; it is located on the other side of the twin T-bridge. The shown measurement in Fig. 4.4 provides an amplitude difference of -11.4 dB. The high amplitude difference is only achieved when D1 is tuned to find the minimum again after tuning D2 voltage. When skipping the minimum tuning after setting D2 voltage, the

measured amplitude difference is much smaller (Fig. A.9). With this figure, it can be shown that the D2 also has a marginal influence on the resonant frequency.

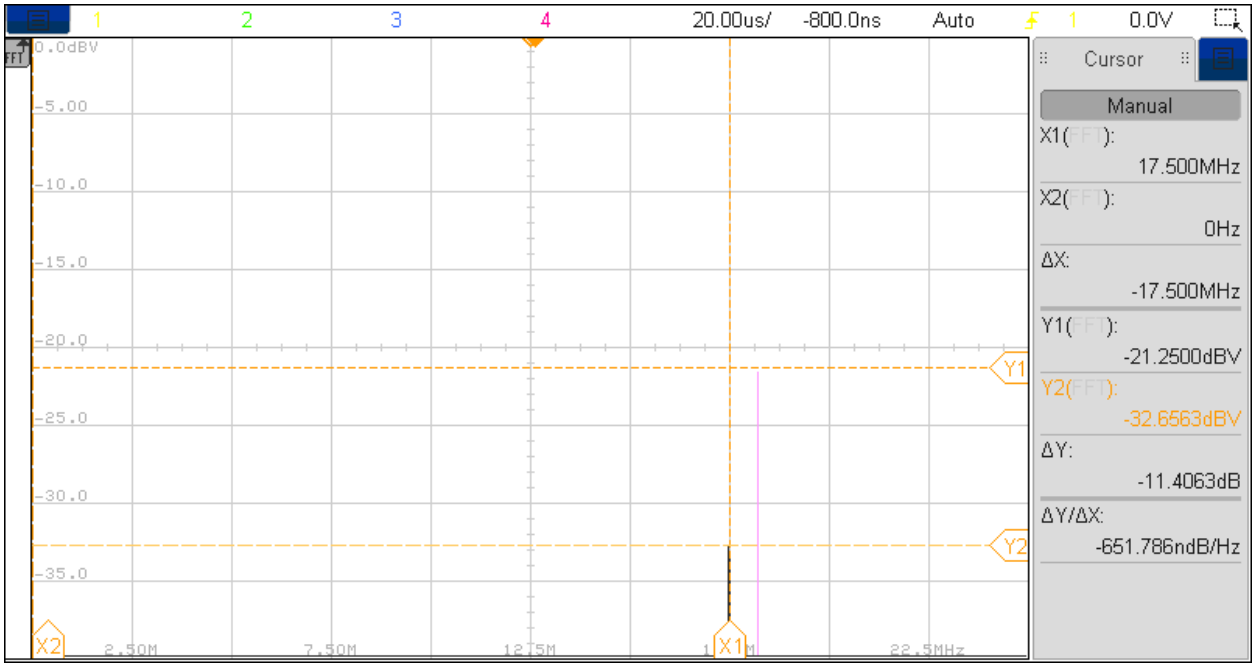

Figure 4.4: Change D2 voltage from 0 to 5 V; D1 was calibrated and set to 239 mV; measured amplitude difference is $\Delta V_p = -11.4\,\text{dB}$ (recalibration after set D2 to 5 V in order to find minima again, D1 is set to 99 mV); pink curve is for D2 0 V, black for D2 5 V; higher quality factor due to less capacitance

4.4 Imitate relative Permittivity Changes using soldered Capacitors and Resistors

The designed board provides solder pads to add resistors and capacitors to imitate changes in relative permittivity. In the first step, a capacitance with $C = 10.29\,\text{pF}$ is soldered to the sensor unit, resulting in a corresponding frequency drift of $\Delta f_r = -645\,\text{kHz}$ as seen in Fig. 4.5. The interpretation of the frequency shift can be made as follows: Taking the initial circuit at calibration time, with $C = 120.08\,\text{pF}$ and a nominal inductor value of $L = 680\,\text{nH}$, the resonant frequency can be computed to $f_{r,calib} = 17.56\,\text{MHz}$. Consequently, adding a capacitance will shift the resonant frequency downwards. Due to calculation (Eq. 4.1), the 10.29 pF capacitor should shift the frequency by $\Delta C = -703.29\,\text{kHz}$. Calculated and measured frequency drift are not identical and show a significant difference. A possible explanation is that the used capacitor will have a lower capacitance at high frequencies than the capacitance measurement evaluated by an RLC-Meter in

the low-frequency range.

$$f_r = \frac{1}{2\pi\sqrt{LC}} \tag{4.1}$$

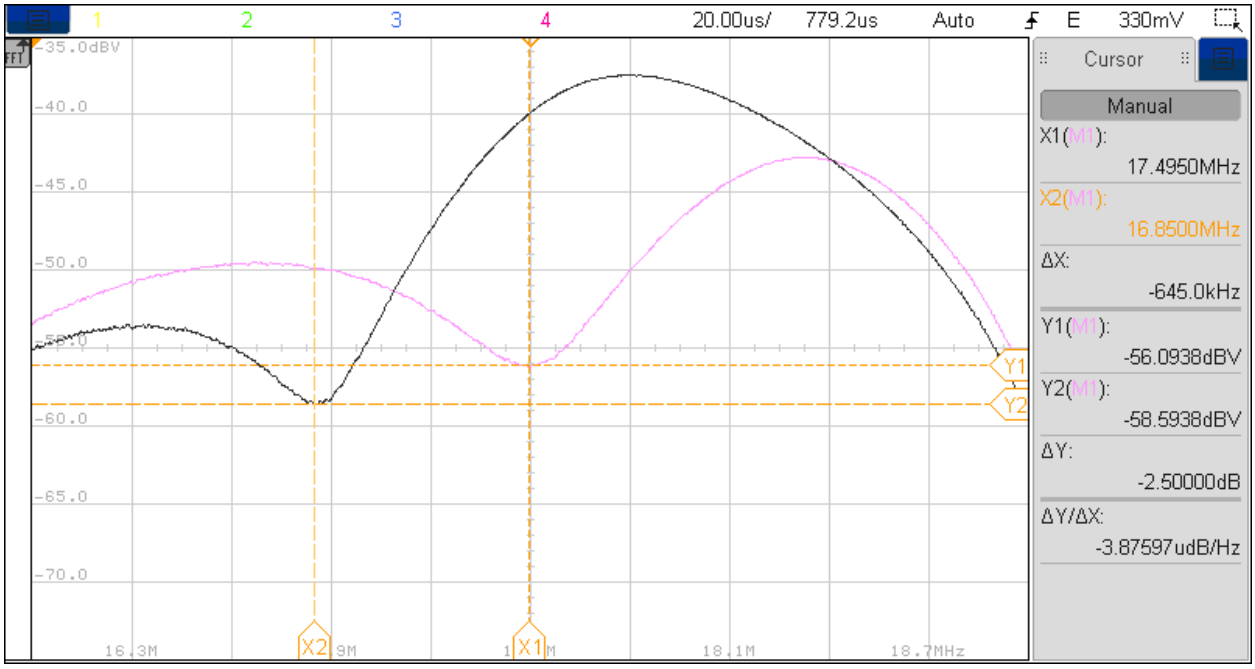

Figure 4.5: Adding a capacitor of $C = 10.29\,\text{pF}$ to the sensor; the Pink curve is the calibration curve for D1 voltage of 0V; the black curve shows resonant frequency drift of $\Delta f_r = -645\,\text{kHz}$ due to the added capacitor.

Secondly, a potentiometer is soldered to the sensor to imitate the presence of an additional imaginary part. The used potentiometer allows resistor changes in continuous steps between around $10\,\Omega$ and $10\,\text{k}$. Figure 4.6 shows the measured amplitude marked as points (D2 voltage is set to $5\,\text{V}$) and the corresponding interpolation curve formed by Eq. 4.2. By decreasing the resistance, the amplitude rises, whereas the quality factor gets lowered. The minimal resistance that can be compensated by applying $0\,\text{V}$ to D2 is measured with $R_{min} = 2.723\,\text{k}\Omega$. Lower resistances cannot be measured anymore.

An interesting fact is the behavior of the quality factor by changing the voltage on D2. On the one hand, in the previous measurement presented in Fig. 4.2 the amplitude is lowered (higher quality factor) by increasing the voltage on D2. This measurement is taken without any additional resistance in the parallel resonant circuit. On the other hand, when a parallel resistance is present (like for Fig. 4.2), the quality factor rises by decreasing the D2 voltage. This finding proves the concept from section 2.2.2. As explained, the quality factor is not describable by $Q = R\sqrt{\frac{C}{L}}$,

because the notch filter is much more than a simple parallel resonant circuit.

$$V_p = 3.0593 \cdot R^{-0.939} \tag{4.2}$$

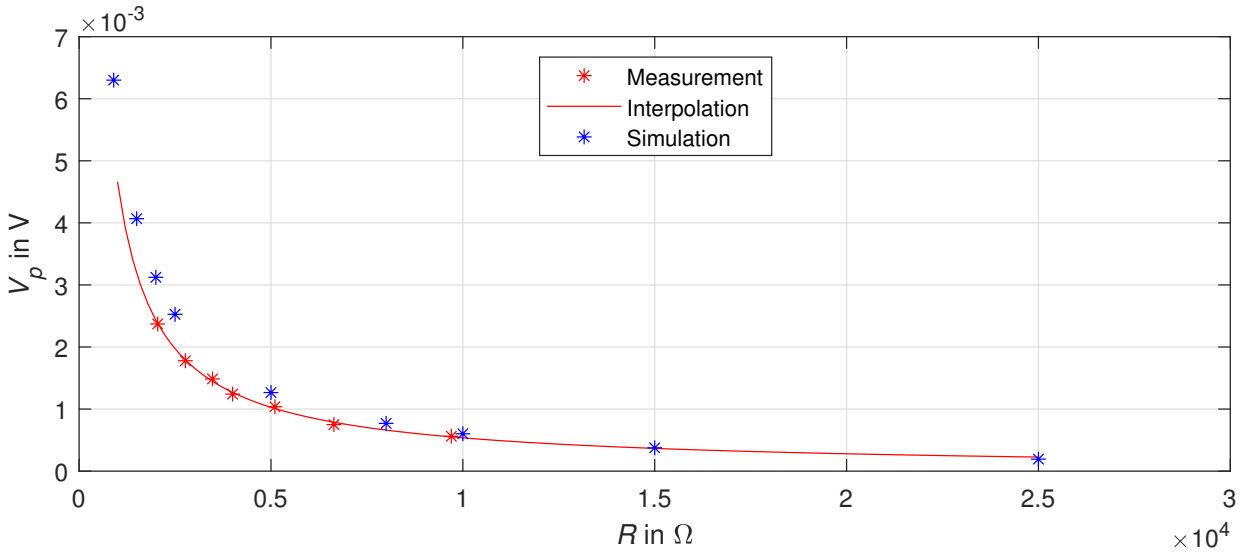

Figure 4.6: Notch filter output amplitude depending on soldered resistances in the range of [2.047 9.7] kΩ; diode voltage D2 set to 5 V

4.5 Automatic Circuit Tuning for relative Permittivity Determination

The tuning procedure in Fig 4.7 demonstrates how the calibration point can be reached in case of imitating real and imaginary parts of ϵ_r. By adding the components, the amplitude is heavily increased (resonant frequency shift).

Therefore, before any local minimum can be determined, the ϵ_r'' must be compensated by tuning D2. Afterward, the minima algorithm can find again the overall minimum (snapshot in Fig.4.7 shows exactly that step in the procedure). Subsequently, the D2 tuning can be executed again and the frequency bin reaches the calibration level again.

A detailed view of the tuning process is visible in Fig. 4.8 and 4.9. The implemented FW application automatically does the tuning, which also provides the raw data for the two plots. Figure 4.8 shows the result of finding the local minima by applying a diode voltage of $U_{D1} = 2.185\,\text{V}$.

The second tuning step, including the D2 tuning, is plotted in Fig. 4.9. In contrast to determining the absolute minimum, the desired minimum is the difference between the actual amplitude and the one at the calibration.

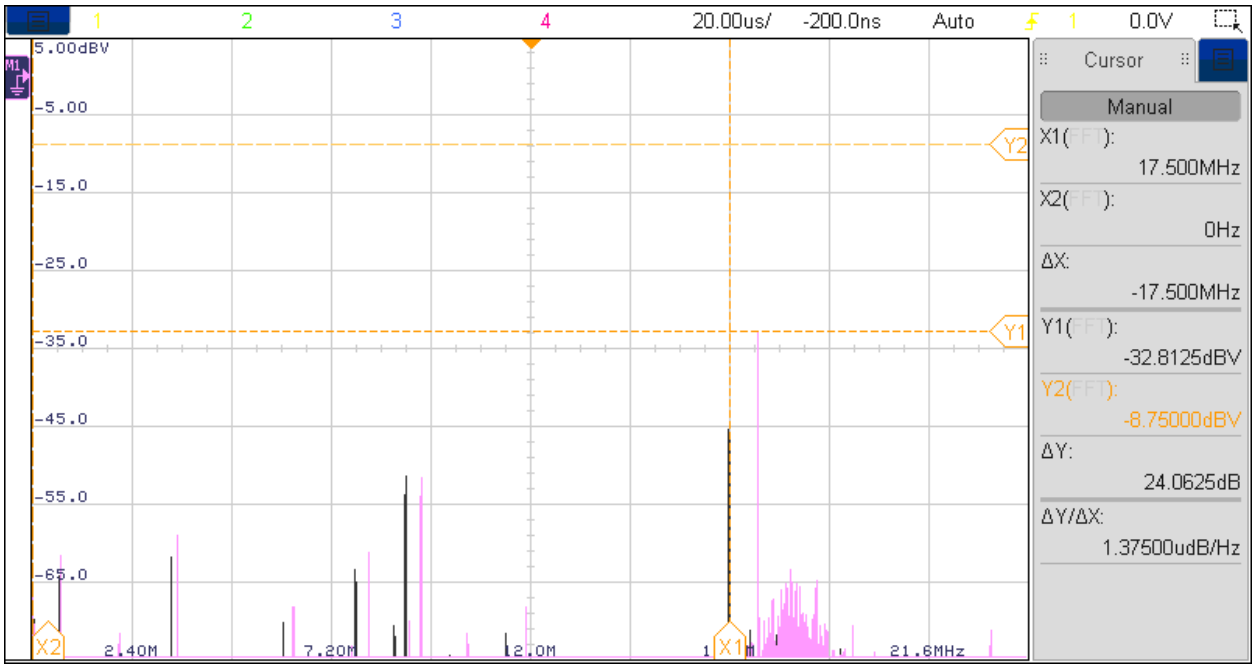

Figure 4.7: Adding an resistor of 1.998 kΩ and capacitance 10.29 pF to the sensor. The pink curve represents the calibration point; cursor Y2 shows the achieved amplitude height due to the added capacitor and resistor. Black FFT bin shows the found local minimum in the first step (D1 is set to 2218 mV). With variation of D2, the calibration point can be reached again with $U_{D2} = 670\,\text{mV}$

4.6 Measurments with two different Media

The last step in the verification process should demonstrate the system's behavior for real measurement samples. Therefore, the sensor was calibrated in air at around 0°C and afterward, two different media were measured.

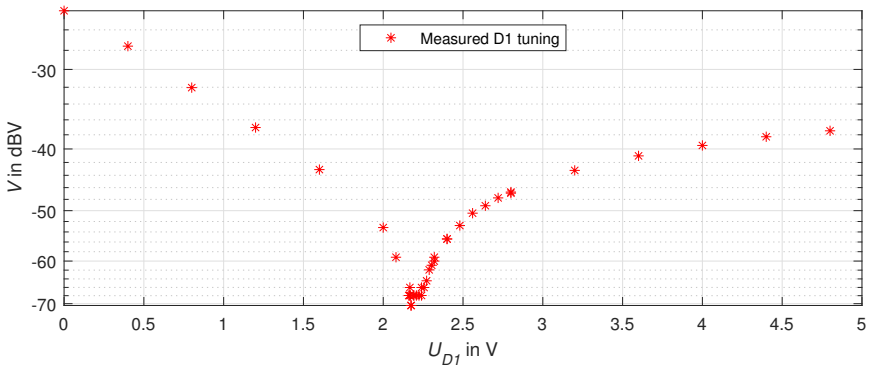

Figure 4.8: Measured D1 tuning regarding measurement shown in 4.7; Minimum found for $U_{D1} = 2.185\,\text{V}$

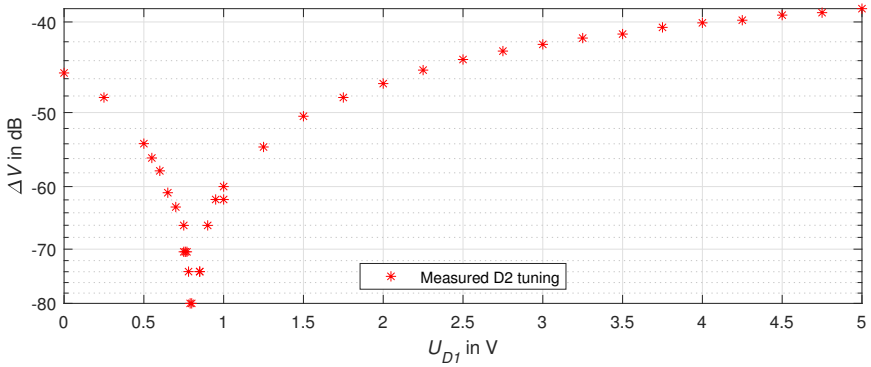

Figure 4.9: Measured D2 tuning regarding measurement shown in 4.7; Minimal difference found for $U_{D2} = 0.8\,\mathrm{V}$

Calibration Step

The calibration step is here performed twice, once for a diode voltage D2 of 5 V and once for 0 V. Typically, the diode voltage D2 will be set to 5 V in order to enable a later tuning to the calibration point in case of an available imaginary part of ϵ_r. Listing 4.1 shows the calibration with D2 voltage set to 0 V, whereas List. 4.2 shows the calibration with D2 set to 5 V.

Listing 4.1: FW log of calibration process with D2 voltage set to 0 V

```
1
2 [INFO] Calibration() -> Amp: 5.5 mVp (-45.1 dBV), Freq: 19142 Hz, Position: 80:
      Gain: 1, RawAmp: 91 mVp
3 [INFO] Calibration with: Ch1: 0, Ch2: 73
4 [INFO] RunServiceCommand() Peak -> Amp: 24.2 mVp (-32.3 dBV), Freq: 19142 Hz,
      Position: 80: Gain: 0, RawAmp: 118 mVp
```

Listing 4.2: FW log of calibration process with D2 voltage set to 5 V

```
1
2 [INFO] Calibration() -> Amp: 9.6 mVp (-40.3 dBV), Freq: 19142 Hz, Position: 80:
      Gain: 1, RawAmp: 159 mVp
3 [INFO] Calibration with: Ch1: 5000, Ch2: 64
4 [INFO] RunServiceCommand() Peak -> Amp: 8.4 mVp (-41.5 dBV), Freq: 19142 Hz,
      Position: 80: Gain: 0, RawAmp: 41 mVp
```

Measurement with wet Snow

Now, the sensor unit is exposed to a wet snow sample by sticking the sensor unit vertically into the snow. Listing 4.3 shows the influence of the wet snow sample. Due to high polarization losses in the wet sample, an imaginary part of ϵ_r is present, whereas the real part is minimally influenced.

Listing 4.3: FW log of measurement process, $\Delta V_{D1} = 211\,\text{mV}$, $\Delta V_{D2} = 600\,\text{mV}$

```
1 [INFO] Starting "AL_PERMITTIVITY_Epsilon()"...
2 [INFO] Measurement result: imag ch1: 4400, real Ch2: 275
3 [INFO] Calibration with: Ch1: 5000, Ch2: 64
4 [INFO] Starting FFT measurement...
5 [INFO] RunServiceCommand() Peak -> Amp: 8.2 mVp (-41.7 dBV), Freq: 19142 Hz,
      Position: 80: Gain: 0, RawAmp: 40 mVp
```

Measurement in Water

In the following measurement, the sensor unit is put into liquid water. As described in section 1.2, liquid water exhibits a high real and imaginary part of the relative permittivity. Consequently, the quality factor of the notch filter will degrade and the resonant frequency will be shifted highly. Therefore, the signal amplitude should rise, as in List. 4.4.

Listing 4.4: FW log of executed FFT measurement, amplitude rises dramatically after exposing the sensor to liquid water, $V_p = 656\,\text{mV}$

```
1 [INFO] Starting FFT measurement...<\r><\n>
2 [INFO] RunServiceCommand() Peak -> Amp: 134.7 mVp (-17.4 dBV), Freq: 19142 Hz,
      Position: 80: Gain: 0, RawAmp: 656 mVp,<\r><\n>
```

5 Conclusion

The result of this master thesis is a developed prototype of a Permittivity Meter. The prototype consists of a single board where the actual sensor unit and all additional required circuits are mounted. The processing part is performed by an onboard microcontroller from STM, using the supplied USB or the Bluetooth interface to control the Permittivity Meter with simple text commands. The board design and the deviation of the implemented firmware into dedicated layers allow the usage of an additional TI controller.

The undersampling approach was a crucial point of this thesis and proved to be suitable for digitizing the MHz signal. It turned out that not the analog bandwidth of the ADC was a limiting factor but the clock jitter introduced by internal oscillators, which could be visualized with the developed real-time visualization tool. The measurement of the low signal amplitude down to the low millivolt range is possible through the designed two-stage amplifier stage. Turning the individual gain stages on or off allows a wide range of signal amplitudes to be covered optimally.

Deep simulations showed the complex behavior of the notch circuit designed by A. Denoth. However, it was possible to show that a substitute circuit using a parallel resonant circuit is suitable, where the main components are the inductor and the related ohmic resistance, the sensor capacitance and the parallel ohmic resistor, which imitates the imaginary part of the relative permittivity. Laboratory measurements demonstrated how the notch circuit's behavior changed for different values of the real and imaginary part of the relative permittivity, where additional parallel capacitors and resistors imitated the real and imaginary part.

The developed handheld device generally allows measurements of the relative permittivity's real and imaginary parts. Before measurements are performed, the device starts a calibration procedure. In the later measurement, where the sensor unit is exposed to a snow sample, the device can automatically tune the resonant circuit back to the calibration point. Tuning the circuit to the calibration point is also possible when imaginary parts of the relative permittivity are unequal

to zero.

The handheld device can calculate the real part of the complex relative permittivity, whereas the computation of the imaginary part needs some further investigations. The quality factor of the notch circuit is mainly related to the imaginary part of the relative permittivity. However, providing a simple equation to convert the measurement result into a dedicated imaginary part of the relative permittivity was impossible. Further investigations are also needed in field measurements, including measuring different kinds of snow samples.

To conclude, the developed handheld device is equipped with all required modules to perform automatic measurements, but converting the actual measurement results into numerical values for the real and imaginary part of the relative permittivity needs further development.

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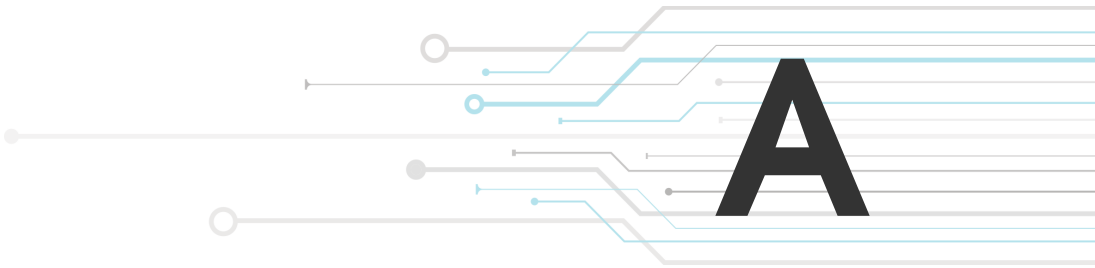

A Appendix

Table A.1: MCU, pin assignment overview for both controllers with additional net name of the schematic

Usage/Description	**STM**	**MSP**	**NetName**	**Type**
Notch Filter ADC In	PC0	P1.3 / P5.0	ADC_IN	In/AF
Varicap 1 DAC	PA4	P1.5	DAC_D1	Out
Varicap 2 DAC	PA5	P1.1	DAC_D2	Out
20 MHz notch input	PA8	P3.4	20M_CLK	Out/AF
Uart TX Nina	PA9	P1.7	NINA_RX	Out/AF
Uart Rx Nina	PA10	P1.6	NINA_TX	In/AF
Uart Usb Tx	PA2	P4.3	-	Out/AF
Uart Usb Rx	PA3	P4.2	-	In/AF
Nina Reset	PA6	P5.2	NINA_RST	Out
Nina Stop	PA7	P5.3	NINA_STOP	Out
OpAmp Disable	PC4	P5.4	OP_DIS	Out
Switch Gain 1	PC5	P6.3	SW_G1	Out
Switch Gain 2	PB0	P6.4	SW_G2	Out
Status LD RED	PC7	P2.1	LED_RED	Out
Status LD Green	PC6	P6.1	LED_GREEN	Out
Status LD Blue	PB15	P6.0	LED_BLUE	Out
User Button	PB1	P3.3	USER_BUT	In
Nina Red	PB2	P3.2	NINA_LD_RED	In
Nina Blue	PB10	P3.5	NINA_LD_BLUE	In
Nina Green	PB11	P3.6	NINA_LD_GREEN	In
Vcc 5V	+5V	5V	+5V	-
Vcc 3.3V	+3V3	3V	+3V3	-
Reset	NRST	RST	B_RST	-
Vref 2.5V	AVDD	-	VREF	-
Uart CTS Nina	PC12	-	NINA_CTS	Out
Uart RTS Nina	PC10	-	NINA_RTS	In
Uart DTR Nina	PC11	-	NINA_DTR	Out
Uart DSR Nina	PD2	-	NINA_DSR	In

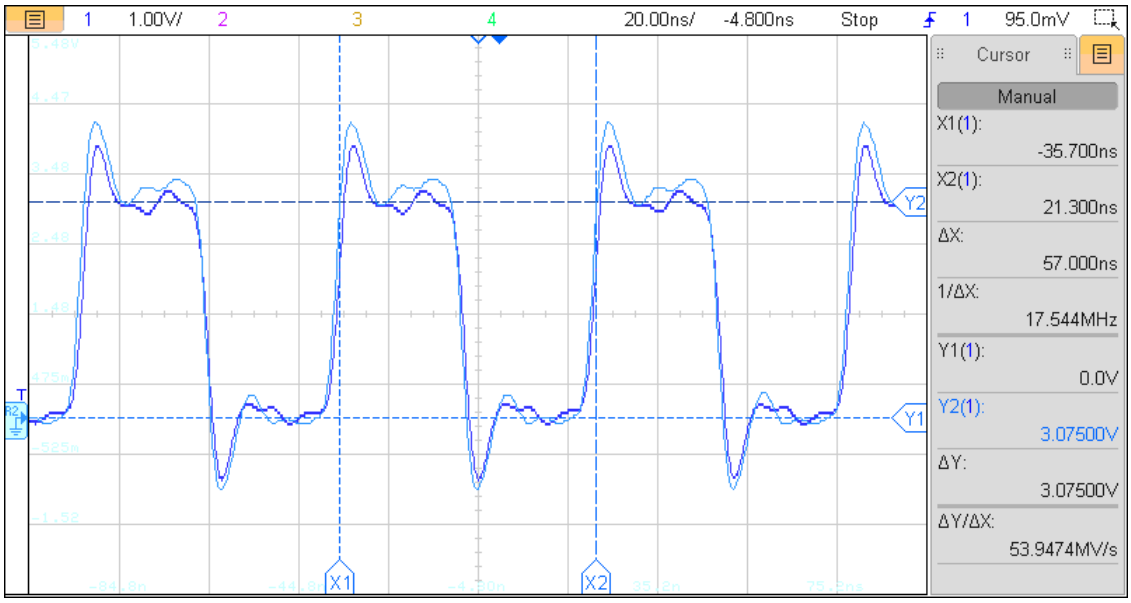

Figure A.1: MCU, 17.5 MHz MCU clock output; light blue curve is with unloaded output, dark blue curve with connected sinewave filter input ($R_{in} = 200\,\Omega$)

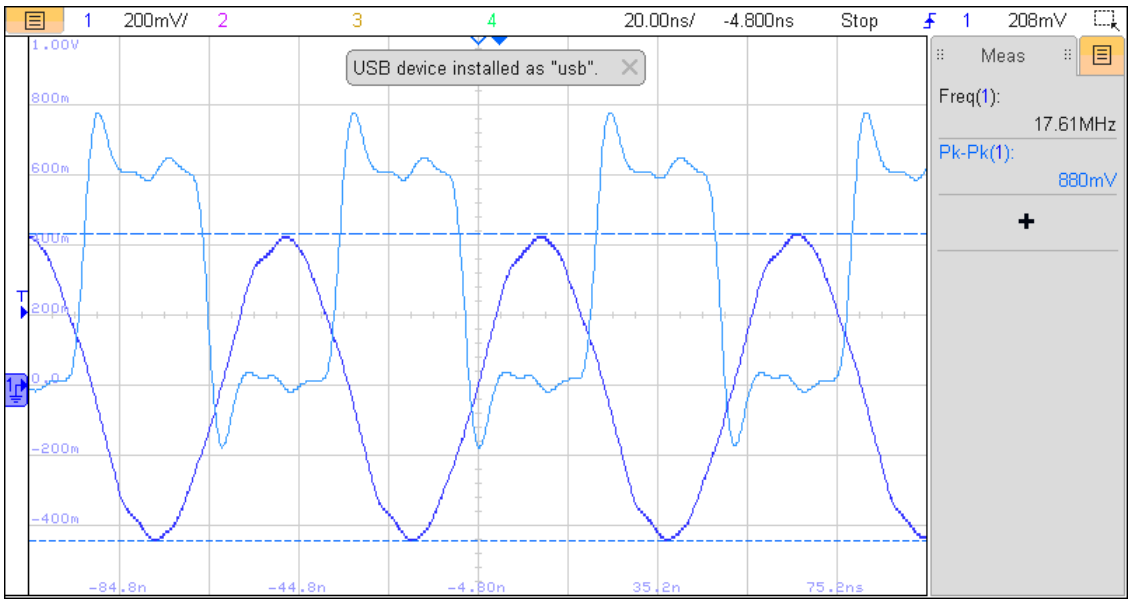

Figure A.2: MCU, 17.5 MHz MCU clock output; the light blue curve is the input signal, dark blue curve is the output of the pre-amplifier circuit; Voltage of $V_p = 440\,\text{mV}$ is applied to the Notch Circuit

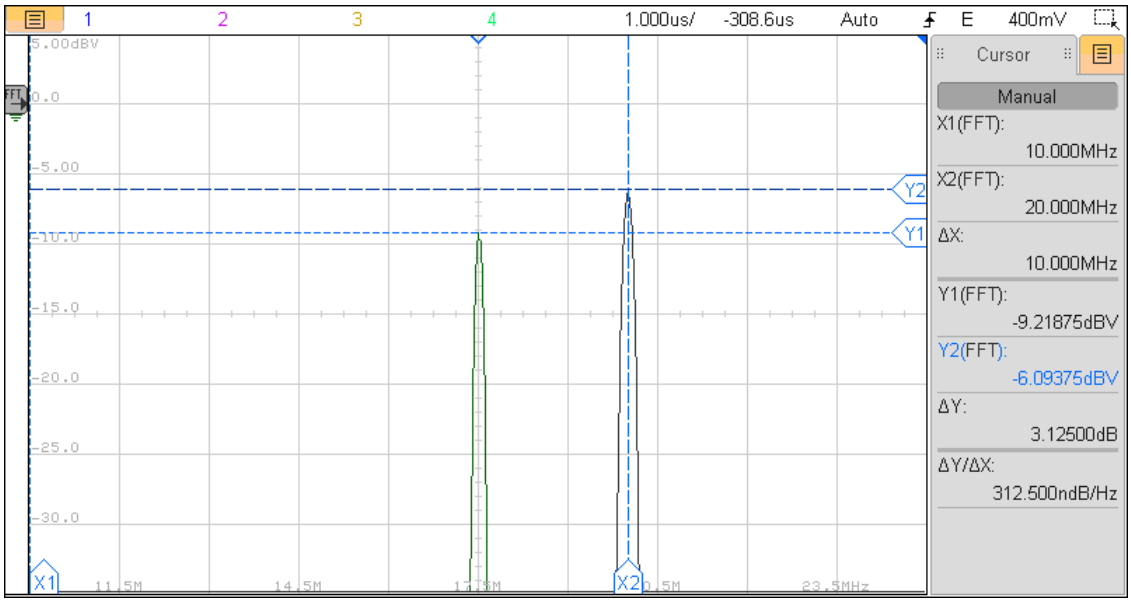

Figure A.3: Amplifiers, gain measurement through FFT with OPA836 at 20 MHz; black FFT bin represents output, green bin the input signal, measured under same conditions, green bin was horizontally moved to see both bins clearly

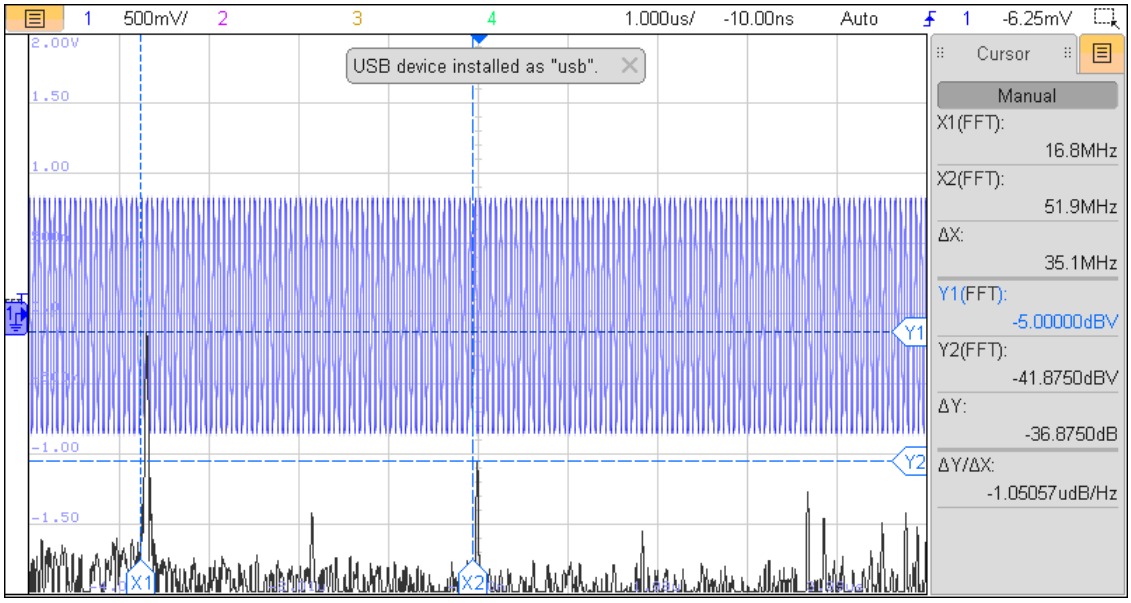

Figure A.4: Amplifiers, harmonic distortions of the OPA836; THD2 = −36.9 dB, 0.75 Vp input voltage at $f = 17.5$ MHz

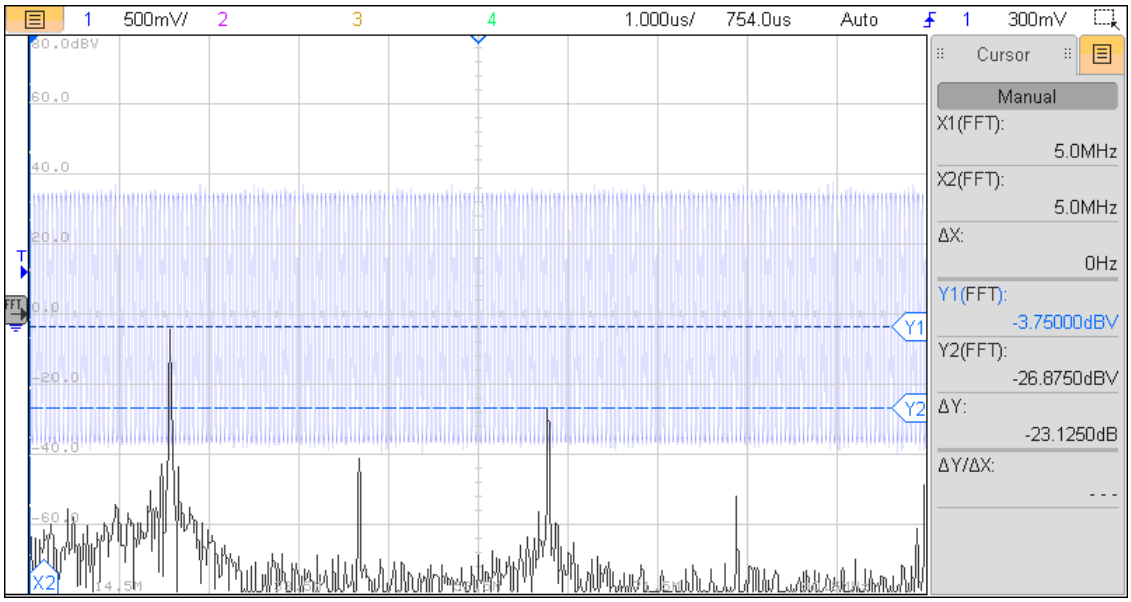

Figure A.5: Amplifiers, harmonic distortions of the ADA4807; THD2 = −23.12 dB,0.75 Vp input voltage at $f = 17.5\,\mathrm{MHz}$

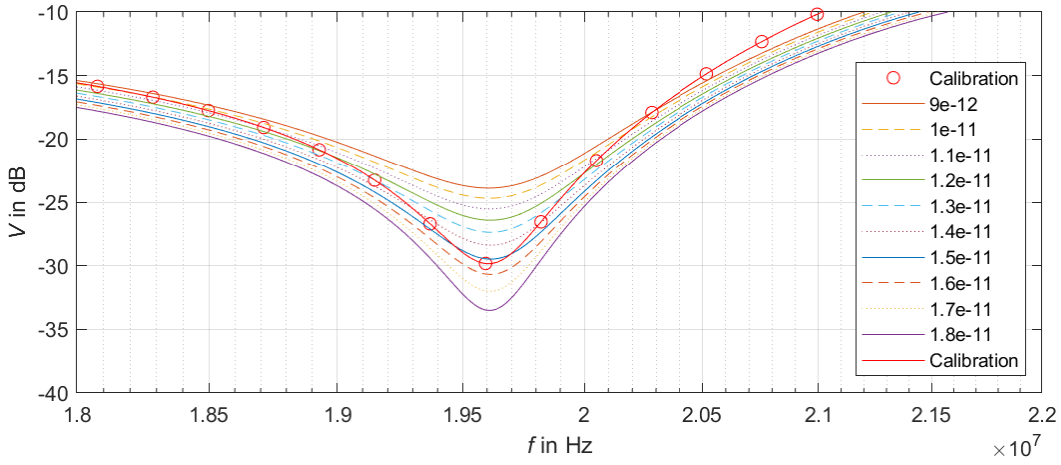

Figure A.6: Notch, simulation with parallel resistance $R_L = 2.7\,\mathrm{k\Omega}$ and D2 capacitance sweeep. Calibration is with high resistance value and $C_{ch2} = 9\,\mathrm{pF}$. Simulation with: L; $C_{ch1} = 21pF$, $C_{ch2} = 9\,\mathrm{pF}$, $C_{sens} = 48pF$,$L = 550n$

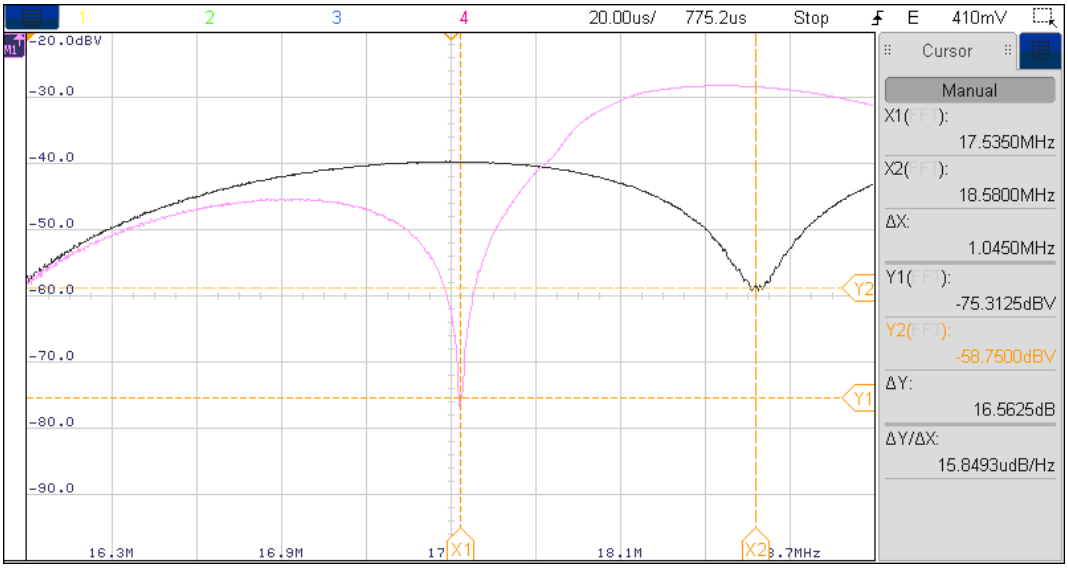

Figure A.7: Notch, sweep D1 voltage in interval [0 5]V, D2 voltage is set to 5 V; Pink curve represents D1 0 V, black curve D1 5 V;resonant frequency drift by $\Delta f = 1.045$ MHz

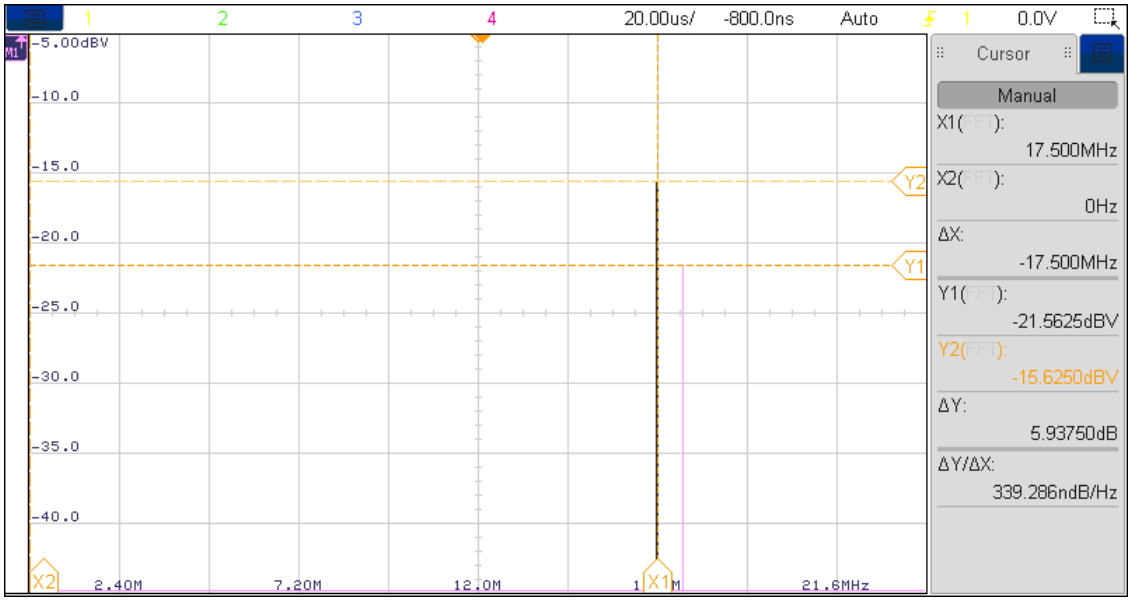

Figure A.8: Notch, changing D1 voltage from 0 to 5 V, D2 is set to 0 V; Pink curve is calibration of D1, black curve is with D1 set to 5V; D1 calibration with 156 mV

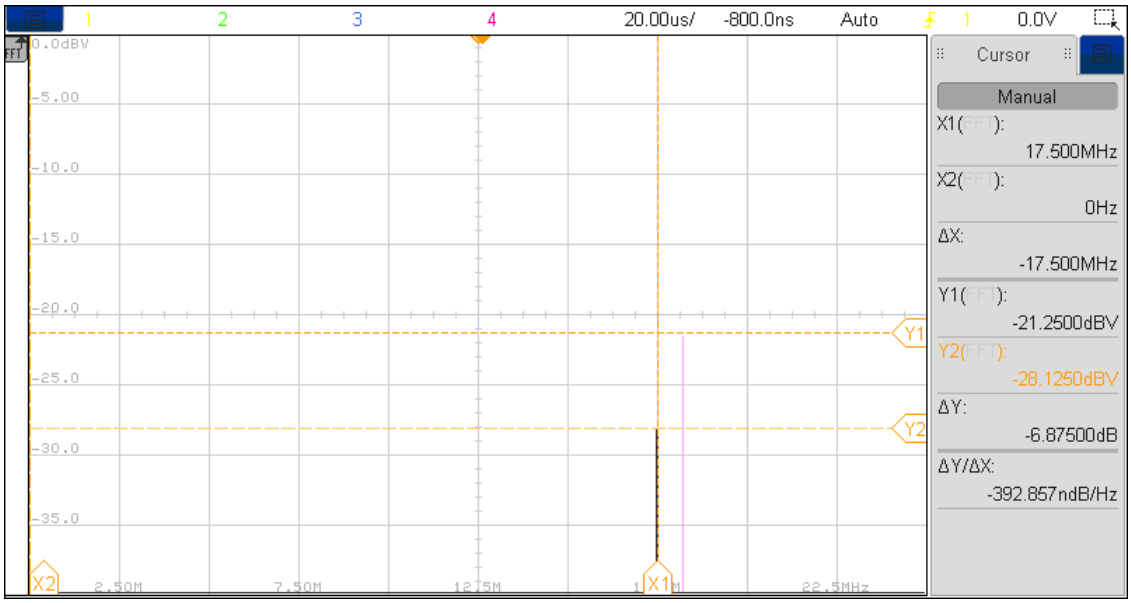

Figure A.9: Notch, microcontroller clock used as input signal, change D2 voltage from 0 to 5 V ; D1 was calibrated and set to 239 mV; Measured amplitude difference is $\Delta V_p = -6.87\,\mathrm{dB}$; pink curve is for D2 0 mV, black for D2 5 V; higher quality factor due to less capacitance

Description	Designator	Value	Tolerance	Package	Mouser Part Number	Quantity	Comment
Capacitor	C1, C4	470pF	10%	0805	710-885012207084	2	885012207084
Capacitor	C2, C3	680pF	10%	0805	710-885012207085	2	885012207085
Capacitor	C5, C6, C7	15pF	5%	0805	710-885012007052	3	885012007052
Capacitor	C8, C9, C10, C11, C12, C13, C20, C23, C25	10nF	10%	0805	710-885012207092	9	885012207092
Capacitor	C14, C15, C16, C22, C26, C29, C30	100nF	10%	0805	710-885382207007	7	885382207007
Capacitor	C17, C18, C19, C21, C27, C28	2.2uF	10%	0805	80-C0805C225K5RAUTO	6	C0805C225K5RACAUTO
Capacitor Dummy	C24			0805		1	Capacitor Dummy
Diode, varicap BB135	D1, D2, D3, D4				771-BB135-T/R	4	BB135,115
IC, OpAmp OPA2690	IC1				595-OPA2690I-14D	1	OPA2690I-14D
IC, OpAmp OPA341	IC2, IC3				595-OPA341NA/3K	2	OPA341NA_3K
IC, OpAmp ADA4807	IC4, IC5				584-ADA4807-1ARJZ-R7	2	ADA4807-1ARJZ-R7
IC, OpAmp OPA836*	IC4, IC5				595-OPA836IDBVT	2	OPA836IDBVT
IC, RefVoltage 2V5	IC6				595-REF4132B25DBVRQ1	1	REF4132B25DBVRQ1
Connector 2x10	J1, J2				200-MTSW11008GD340	2	MTSW-110-08-G-D-340
Connector, 2x20	J3, J4				571-7-534206-0	2	7-534206-0
Connector 1x2	JP1, JP2, JP4, JP5, JP6, JP7, JP8, JP9, JP10				649-69190-102HLF	9	69190-102HLF
Inductor	L1, L3	330nH	2%	1008	994-1008CS-331XGLC	2	1008CS-331XGLC
Inductor	L2	390nH	2%	1008	994-1008CS-391XGLC	1	1008CS-391XGLC
Inductor	L4	680n	10%		652-SRP0415-R68K	1	SRP0415-R68K
Inductor*	L4	680n	5%		807-1025R-16J	1	1025R-16J
LED, RGB	LED1				720-KRTBLFLP713A9639	1	KRTBLFLP71.32-UVUZ-GP+VYAU-JS+SVSZ-SZ-B
BJT, npn BC547B	Q1, Q2				512-BC547B	2	BC547BG
Resistor	R1, R2	39R	1%	0805	652-CR0805FX-39R0ELF	2	CR0805-FX-39R0ELF
Resistor	R3, R33, R34, R35	200R	0.1%	0603	667-ERA-3AEB201V	4	ERA-3AEB201V
Resistor	R4, R5	100k	1%	0603	667-ERJ-UP3F1003V	2	ERJUP3F1003V
Resistor	R6, R7, R9, R21, R25, R26, R30	20k	1%	805	652-CR0805FX-2002ELF	7	CR0805-FX-2002ELF
Resistor	R12, R13, R15, R23	510	5%	0805	652-CR0805JW-511ELF	4	CR0805-JW-511ELF
Resistor	R14, R22	56	5%	0805	652-CR0805JW-560ELF	2	CR0805-JW-560ELF
Resistor	R16, R17, R18, R19, R32	9k1	1%	805	652-CR0805FX-9101ELF	5	CR0805-FX-9101ELF
Resistor	R20, R24	1k	1%	0805	652-CR0805FX-1001ELF	2	CR0805-FX-1001ELF
Resistor	R27, R28	100	1%	0805	652-CR0805FX-1000ELF	2	CR0805-FX-1000ELF
Resistor Dummy	R29, R36, R37	0R		0805		3	Resistor Dummy
Resistor	R31	6k8	1%	0805	652-CR0805FX-6801ELF	1	CR0805-FX-6801ELF
Resistor	R38	100m	1%	0603	667-ERJ-3BSFR10V	1	ERJ-3BSFR10V
Switch, SMD	S1, S2				474-COM-12992	2	COM-12992
TestPoint	TP1, TP2, TP3, TP4, TP5, TP6					6	TestPoint
Module, u-blox NINA-W152	U1				377-NINA-W152-03B	1	NINA-W152-03B

Figure A.10: Board design, Bill of materials; * marked items are for assembly option V1.1,

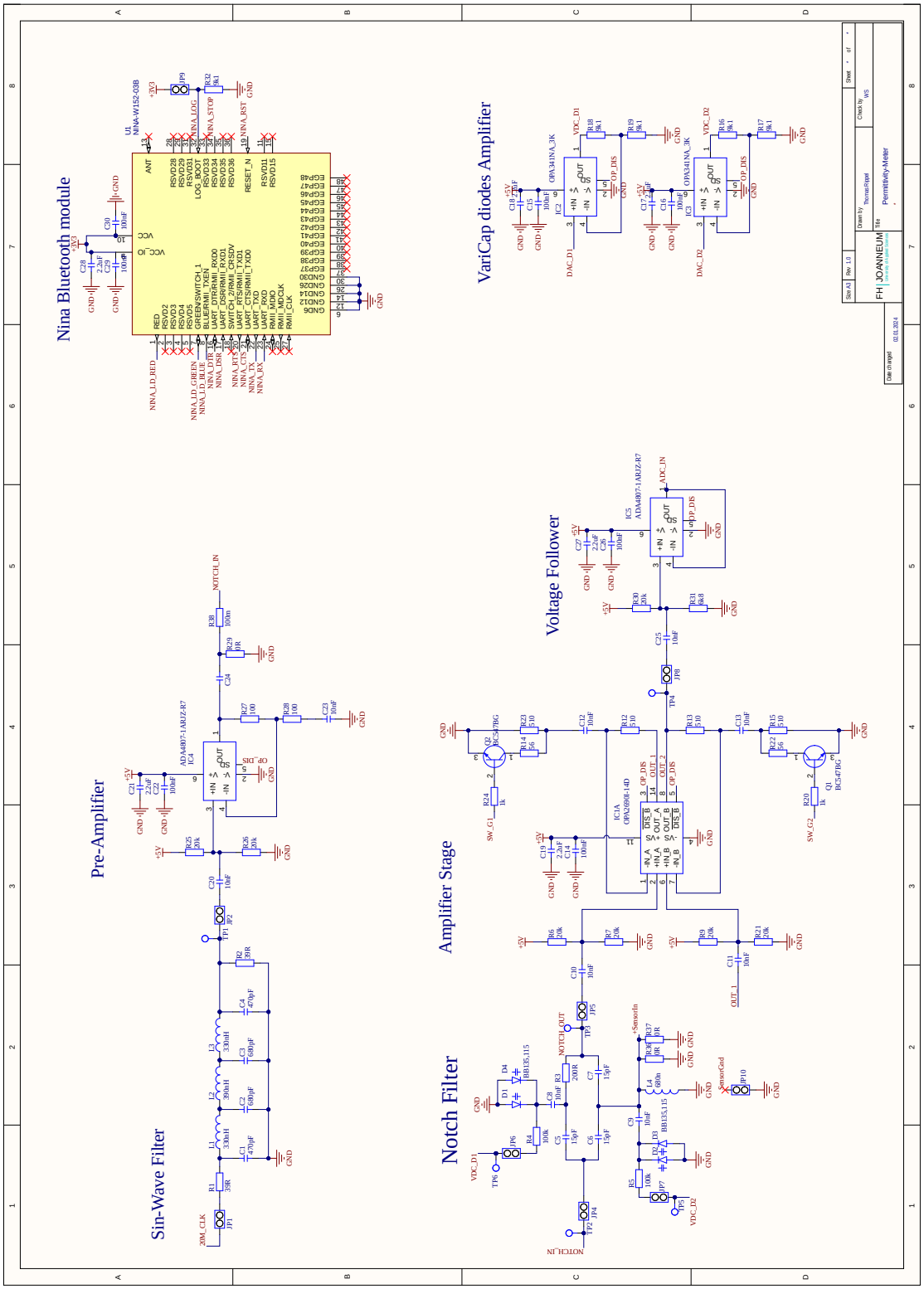

Figure A.11: Board design, schematic part 1, includes all notch-related circuits

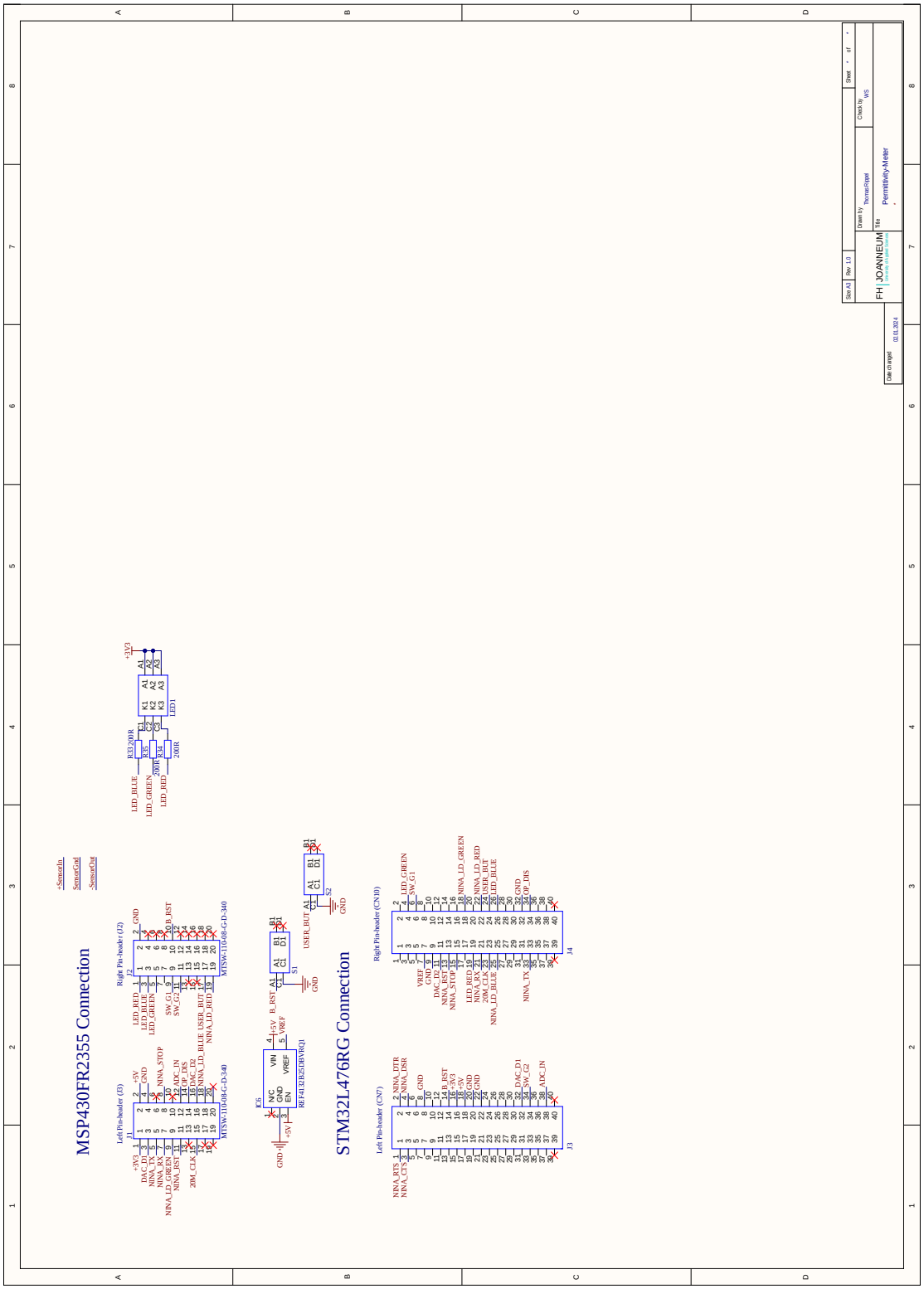

Figure A.12: Borad design, schematic part 2, includes user interaction and pin headers