


Computer Organization and Design:
The Hardware/Software Interface
by Patterson and Hennessy

Cache Simulator 과제

컴퓨터공학과
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1. 선택한 과제 수준(Challenge) - 10점

❖ Challenge (10점 만점)		
❖	Set associative data, instruction cache simulator	
	LRU를 구현하고 프로그램 내에서 선택이 가능 하도록 구현 (Instruction / Data cache의 size는 서로 다를 수 있음)	
❖	입력	
❖	Trace file	
❖	LRU mode / FIFO mode 선택	
❖	Instruction cache size, block size	
❖	Instruction associativity (1 ~ 16)	
❖	Data cache size, block size	
❖	Data cache associativity (1 ~ 16)	
❖	(cache size, block size 범위는 Advanced와 같음)	
❖	출력	
❖	Instruction cache access	
❖	Instruction cache miss, miss ratio	
❖	Data cache access	
❖	Data cache miss, miss ratio	
<div>  <div> SEJONG UNIVERSITY Department of Computer Engineering </div> <div>Computer Architecture</div> <div>23</div> </div>		
사진 1. 선택한 과제 수준		

2. DineroIV 입력 정보

입력\파일	trace_1.din	trace_2.din
입력1	./dineroIV -l1-dsize 64k -l1-dbsize 4 -l1-dassoc 2 -l1-drepl 1 -l1-isize 128k -l1-ibsize 8 -l1-iassoc 4 -l1-irepl 1 -informat d < trace_1.din	./dineroIV -l1-dsize 64k -l1-dbsize 4 -l1-dassoc 2 -l1-drepl 1 -l1-isize 128k -l1-ibsize 8 -l1-iassoc 4 -l1-irepl 1 -informat d < trace_2.din
Data Size	Data cache size : 64KB Data block size : 4B Data cache associativity : 2 Instruction cache size : 128KB Instruction block size : 8B Instruction associativity : 4	Data cache size : 64KB Data block size : 4B Data cache associativity : 2 Instruction cache size : 128KB Instruction block size : 8B Instruction associativity : 4
입력2	./dineroIV -l1-dsize 32k -l1-dbsize 4 -l1-dassoc 1 -l1-drepl 1 -l1-isize 512k -l1-ibsize 64 -l1-iassoc 16 -l1-irepl 1 -informat d < trace_1.din	./dineroIV -l1-dsize 32k -l1-dbsize 4 -l1-dassoc 1 -l1-drepl 1 -l1-isize 512k -l1-ibsize 64 -l1-iassoc 16 -l1-irepl 1 -informat d < trace_2.din
Data Size	Data cache size : 32K Data block size : 4B Data cache associativity : 1 Instruction cache size : 512K Instruction block size : 64B Instruction associativity : 16	Data cache size : 32K Data block size : 4B Data cache associativity : 1 Instruction cache size : 512K Instruction block size : 64B Instruction associativity : 16

3. 수행한 화면

<pre> File : trace_1.din Mode select (LRU : 1 / FIFO : 2) : 1 Instruction cache size (KB) : 128 Instruction cache block size (B) : 8 Instruction associativity : 4 Data cache size (KB) : 64 Data cache block size (B) : 4 Data associativity : 2 Instruction cache Access : 653574 Miss : 9183 Miss ratio : 0.0139 Data cache Access : 269200 Miss : 21303 Miss ratio : 0.0733 계속하려면 아무 키나 누르십시오 . . . </pre>	<pre> ---Simulation complete. 11-icache Metrics ----- Demand Fetches Fraction of total Demand Misses Demand miss rate Multi-block refs Bytes From Memory (/ Demand Fetches) Bytes To Memory (/ Demand Writes) Total Bytes r/w Mem (/ Demand Fetches) 11-dcache Metrics ----- Demand Fetches Fraction of total Demand Misses Demand miss rate Multi-block refs Bytes From Memory (/ Demand Fetches) Bytes To Memory (/ Demand Writes) Total Bytes r/w Mem (/ Demand Fetches) ---Execution complete. </pre> <table border="1"> <thead> <tr> <th>Metrics</th> <th>Total</th> </tr> </thead> <tbody> <tr> <td>Demand Fetches</td> <td>662757</td> </tr> <tr> <td>Fraction of total</td> <td>1.0000</td> </tr> <tr> <td>Demand Misses</td> <td>9183</td> </tr> <tr> <td>Demand miss rate</td> <td>0.0139</td> </tr> <tr> <td>Multi-block refs</td> <td>0</td> </tr> <tr> <td>Bytes From Memory</td> <td>73464</td> </tr> <tr> <td>(/ Demand Fetches)</td> <td>0.1108</td> </tr> <tr> <td>Bytes To Memory</td> <td>0</td> </tr> <tr> <td>(/ Demand Writes)</td> <td>0.0000</td> </tr> <tr> <td>Total Bytes r/w Mem</td> <td>73464</td> </tr> <tr> <td>(/ Demand Fetches)</td> <td>0.1108</td> </tr> <tr> <td>Demand Fetches</td> <td>290503</td> </tr> <tr> <td>Fraction of total</td> <td>1.0000</td> </tr> <tr> <td>Demand Misses</td> <td>21303</td> </tr> <tr> <td>Demand miss rate</td> <td>0.0733</td> </tr> <tr> <td>Multi-block refs</td> <td>0</td> </tr> <tr> <td>Bytes From Memory</td> <td>19616</td> </tr> <tr> <td>(/ Demand Fetches)</td> <td>0.0675</td> </tr> <tr> <td>Bytes To Memory</td> <td>74604</td> </tr> <tr> <td>(/ Demand Writes)</td> <td>0.4535</td> </tr> <tr> <td>Total Bytes r/w Mem</td> <td>94220</td> </tr> <tr> <td>(/ Demand Fetches)</td> <td>0.3243</td> </tr> </tbody> </table>	Metrics	Total	Demand Fetches	662757	Fraction of total	1.0000	Demand Misses	9183	Demand miss rate	0.0139	Multi-block refs	0	Bytes From Memory	73464	(/ Demand Fetches)	0.1108	Bytes To Memory	0	(/ Demand Writes)	0.0000	Total Bytes r/w Mem	73464	(/ Demand Fetches)	0.1108	Demand Fetches	290503	Fraction of total	1.0000	Demand Misses	21303	Demand miss rate	0.0733	Multi-block refs	0	Bytes From Memory	19616	(/ Demand Fetches)	0.0675	Bytes To Memory	74604	(/ Demand Writes)	0.4535	Total Bytes r/w Mem	94220	(/ Demand Fetches)	0.3243
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사진 3. trace_2.din에서 입력 1 했을 때

File : trace_1.din	---Simulation complete.
Mode select (LRU : 1 / FIFO : 2) : 1	l1-icache
Instruction cache size (KB) : 512	Metrics
Instruction cache block size (B) : 64	-----
Instruction associativity : 16	Demand Fetches
Data cache size (KB) : 32	Fraction of total
Data cache block size (B) : 4	
Data associativity : 1	
	Demand Misses
Instruction cache	Demand miss rate
Access : 661332	
Miss : 1425	
Miss ratio : 0.0022	
Data cache	
Access : 257735	
Miss : 32768	
Miss ratio : 0.1128	
계속하려면 아무 키나 누르십시오 . . .	
	Multi-block refs
	Bytes From Memory
	(/ Demand Fetches)
	Bytes To Memory
	(/ Demand Writes)
	Total Bytes r/w Mem
	(/ Demand Fetches)
	l1-dcache
	Metrics

	Demand Fetches
	Fraction of total
	Demand Misses
	Demand miss rate
	Multi-block refs
	Bytes From Memory
	(/ Demand Fetches)
	Bytes To Memory
	(/ Demand Writes)
	Total Bytes r/w Mem
	(/ Demand Fetches)
	---Execution complete.

사진 4. trace_1.din에서 입력 2 했을 때

File : trace_2.din	---Simulation complete.
Mode select (LRU : 1 / FIFO : 2) : 1	l1-icache
Instruction cache size (KB) : 512	Metrics
Instruction cache block size (B) : 64	-----
Instruction associativity : 16	Demand Fetches
Data cache size (KB) : 32	Fraction of total
Data cache block size (B) : 4	
Data associativity : 1	
	Demand Misses
Instruction cache	Demand miss rate
Access : 661332	
Miss : 1425	
Miss ratio : 0.0022	
Data cache	
Access : 257740	
Miss : 32734	
Miss ratio : 0.1127	
계속하려면 아무 키나 누르십시오 . . .	
	Multi-block refs
	Bytes From Memory
	(/ Demand Fetches)
	Bytes To Memory
	(/ Demand Writes)
	Total Bytes r/w Mem
	(/ Demand Fetches)
	l1-dcache
	Metrics

	Demand Fetches
	Fraction of total
	Demand Misses
	Demand miss rate
	Multi-block refs
	Bytes From Memory
	(/ Demand Fetches)
	Bytes To Memory
	(/ Demand Writes)
	Total Bytes r/w Mem
	(/ Demand Fetches)
	---Execution complete.

사진 5. trace_2.din에서 입력 2 했을 때

4. 느낀점

이번 과제를 받고 나서 정말 막막했다. 수업도 들었고 틈틈이 공부를 했지만 막상 Cache에 대해 잘 몰랐고 Cache Simulator를 구현하는 건 접근조차도 못했다. 구현하기 전 Cache의 Tag, Index, BlockOffset에 대한 정의를 공부하고 각각의 길이를 구하는 법을 한참 동안 인터넷 서칭도 하고 책도 보며 공부를 했다. 하루 정도 공부하고 C언어로 코드를 짜기 시작했다. 짜다 보니 LRU 방식을 하기 위해 리스트를 만들어야 하는데 귀찮아서 C++로 넘어가서 라이브러리를 사용했다.

과제를 통해 Cache의 전반적인 동작방법을 확실히 익혔으며 Cache Simulator를 구현하는 힘들었지만 재미있었던 과제였다.