AAC CLYDE SPACE

Command and data handling

KRYTEN-M3

Our flight-proven, robust OBC is developed to deliver 'always-on' operation and is flexible across multiple mission applications and customer requirements. Incorporating a Cortex-M3 processor and innovative hardware/firmware recovery mechanisms, our highly miniaturized OBC delivers high-performance computing for the most demanding nanosatellite missions. Requiring <1W during operations, it is one of the most power efficient COTS OBCs available on the market.

Main Features

- SmartFusion 2 SoC including Cortex-M3 processor @ 50 MHz delivering 62.5 DMIPS
- Integrated cache and Memory Protection Unit
- 8 MB MRAM for code storage and execution
- 4 GB flash memory for bulk data storage
- Autonomous single event latch-up protection
- EDAC protected memories and FIFOs
- JTAG with ETM support for programming and debugging
- Cryptographic Accelerator
- Reed Solomon Accelerator
- GPS available on KRYTEN-M3-PLUS

Dependable Technologies

The MRAM and Flash memories are protected via an EDAC mechanism to guard against radiation effects. This mechanism provides protection, not only against data modifications, but also against errors in the address decode logic. Non-volatile MRAM memory provides zero-boot and zero-sleep times which facilitate further energy savings. The inclusion of 4 GB of SLC flash memory provides ample space for mission data storage. Additionally, a microSD card slot is available for further memory expansion.

Software

The OBC is supplied with a BSP including bare drivers and a FreeRTOS port. The OBC is compatible with Gen1 and software support from Bright Ascension Limited (BAL) is available. The highly configurable software combines a component based OBSW framework and flight-proven software solutions to meet all the command and data handling needs of the next generation of highly-capable CubeSats. Provided with comprehensive API reference documentation, a full user manual and thoroughly documented source code.

Technical Specifications

General

Design Life	5 years in LEO
Processor	Smart Fusion 2 SoC including an ARM Cortex-M3 processor delivering 62.5 DMIPS
Processor Clock	50 MHz
SCET	Real time counter (w/40mins. Backup Power)
MRAM	8 MB
Operating Temperature Range	-40°C to +80°C
Boot Image Storage	256 kB eNVM + 8MB MRAM
Radiation (TiD)	20 kRAD
Typical Energy Usage	6.4 mJ/DM
GPS (PLUS model only)	<10m RMS position accuracy <1m/s RMS velocity accuracy

Interfaces

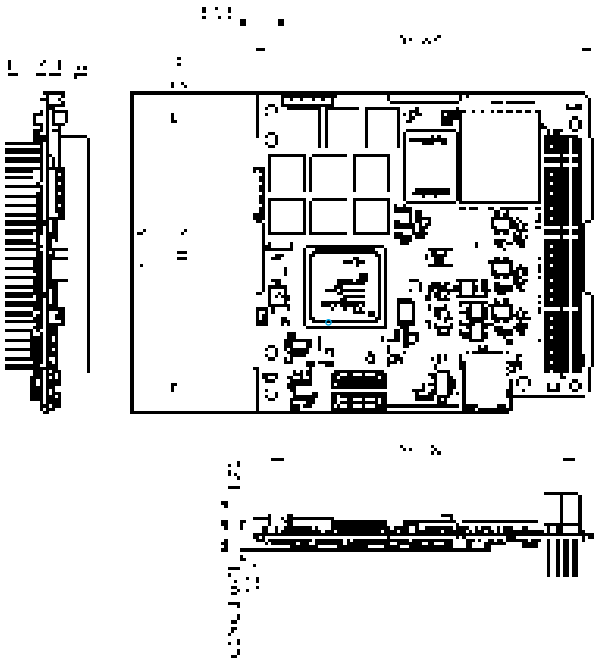
I2C		2
SPI	7 Chip Select Lines	1
UART	3.3 V Logic	8
RS422	(can be used as 2xRS485)	1
CAN		1
DTMF		1
	JTAG w/ETM Support + 1 Serial	
Debugging	Debug	1
LVDS	20x Lines, Expansion	1
QSPI	(2x LVDS, 1x 3V3 Logic)	3
GPIO	3.3 V Logic	17

** Not all interfaces available simultaneously*

Size, Weight and Power

Nominal Power Consumption	400 mW (typ), 1 W max
Mass	61.9 g
Length	95.89 mm
Width	90.17 mm
Height*	5.51 mm

** Height from top PCB to lowest component*



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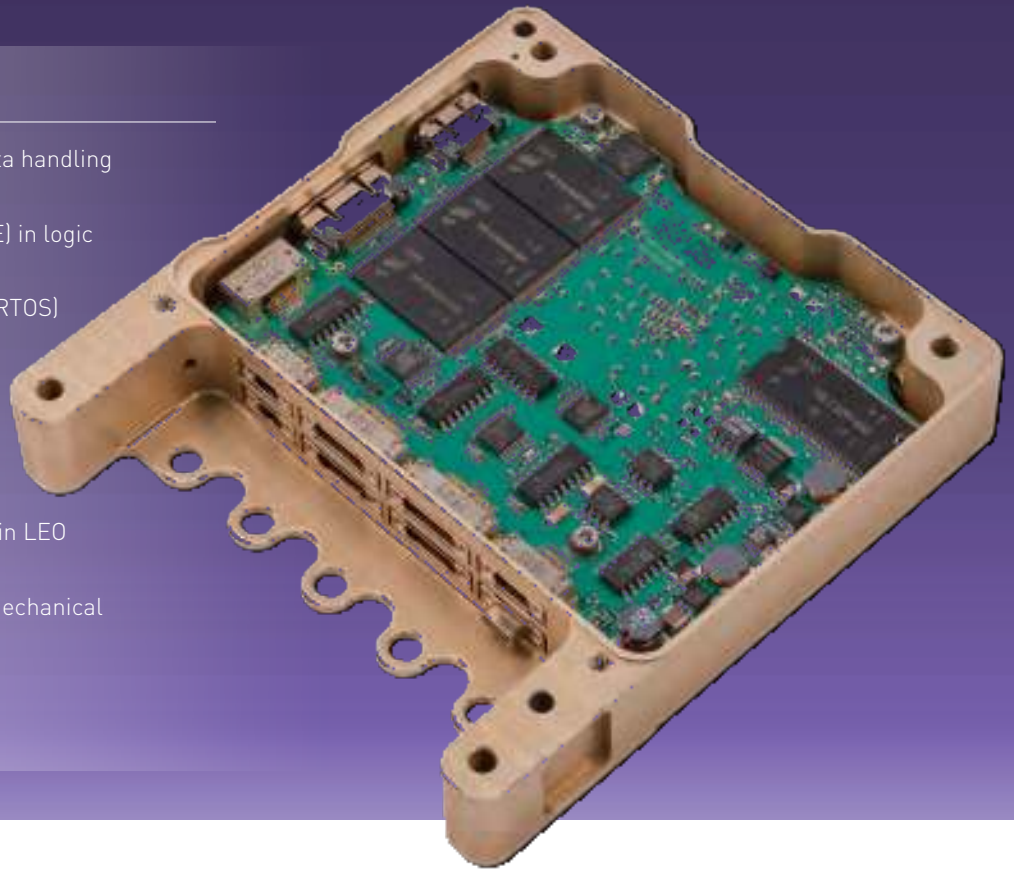
Sirius TCM LEON3FT

This is the latest addition to AAC Clyde Space's Sirius family of avionics equipment. The latest TCM offers increased reliability and high-performance for advanced small and nano-satellite missions. The real-time operating system runs on a LEON3FT fault-tolerant soft processor, is compliant to IEEE 1754 SPARC v8, and provides enhanced error detection and correction. Fault tolerance is secured by using triple-modular redundancy on FPGA and memory scrubbing.

Main Features

- Reliable high-performance space data handling avionics
- Tolerant to Single-Event-Effects (SEE) in logic and data storage
- RTEMS real-time operating system (RTOS)
- 50 MHz LEON3FT soft processor
- SpaceWire on-board data bus
- S- and X-band transceiver interface
- 32 GB mass storage capacity
- CCSDS satellite link services
- Designed and qualified for five years in LEO
- ITAR free equipment
- Modular, nanosatellite compatible, mechanical design
- Pulse commands for low level, basic commanding



Technologies

The Sirius TCM implements SpaceWire for the main on-board data bus for high bandwidth on-board data transfer. The transceiver interface of the unit implements the CCSDS encoding standards for satellite link services and provides compatibility with leading ground stations networks. The Sirius TCM is supplied with a user-friendly application software for management of on-board services which makes it ready for integration out of the box or with a board support package for custom software development. A desktop development kit is also available for rapid design and integration to new spacecraft platforms.

Modular Design

The Sirius family of spacecraft avionics products are designed for modularity. A standard single string system consists of an on-board computer (Sirius OBC) and a combined mass memory with CCSDS stack (Sirius TCM). The OBC runs mission specific software and manage the spacecraft system. The TCM receives and stores payload data and platform housekeeping data while at the same time distributing telecommands and serving mass memory data to the transceiver. The Sirius avionics modules can be combined to offer redundant configurations or to simply accommodate mission specific requirements.

Technical Specifications

General

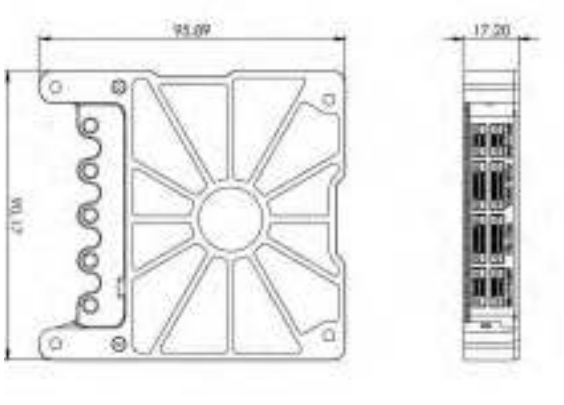
Design Life	5 years in LEO
Processor	32-bit LEON3FT (IEEE-1754 SPARC v8) fault-tolerant processor
FPU	IEEE-754 single/double precision FPU
Processor Clock	50 MHz
SCET	15.25 µs accuracy
SDRAM	64 MB (post-EDAC)
Instruction Cache	8 kB
Data Cache	8 kB
NVRAM	16 kB (post-EDAC)
Operating Temperature Range	-30°C to +60°C
Boot Image Storage	2 GB (post-EDAC)
Mass Memory	32 GB
Power Supply Input	4.5 V to 16 V
Radiation (TiD)	20 kRAD (qualified >30 kRAD, Si)

Interfaces

SpaceWire	50 Mbps, RMAP support	2
Serial Ports	RS422 / RS485 UARTs	3
Serial Ports	RS485-only UARTs	2
PSS Interface	RS485 PPS input	1
GPIO	3.3 V logic	12
CCSDS Sband	RS422 level data stream and TRX command and house-keeping	1
CCSDS Xband	LVDS level data stream and both RS422 and LVDS level TRX command and house-keeping	1
CCSDS Umbilical	RS422 level data stream	1
Pulse Command Output	RS422 level CPDU pulse output	12

Size, Weight and Power

Nominal Power Consumption	1.3 W
Mass	134 g
Length	95.89 mm
Width	90.17 mm
Height	17.20 mm



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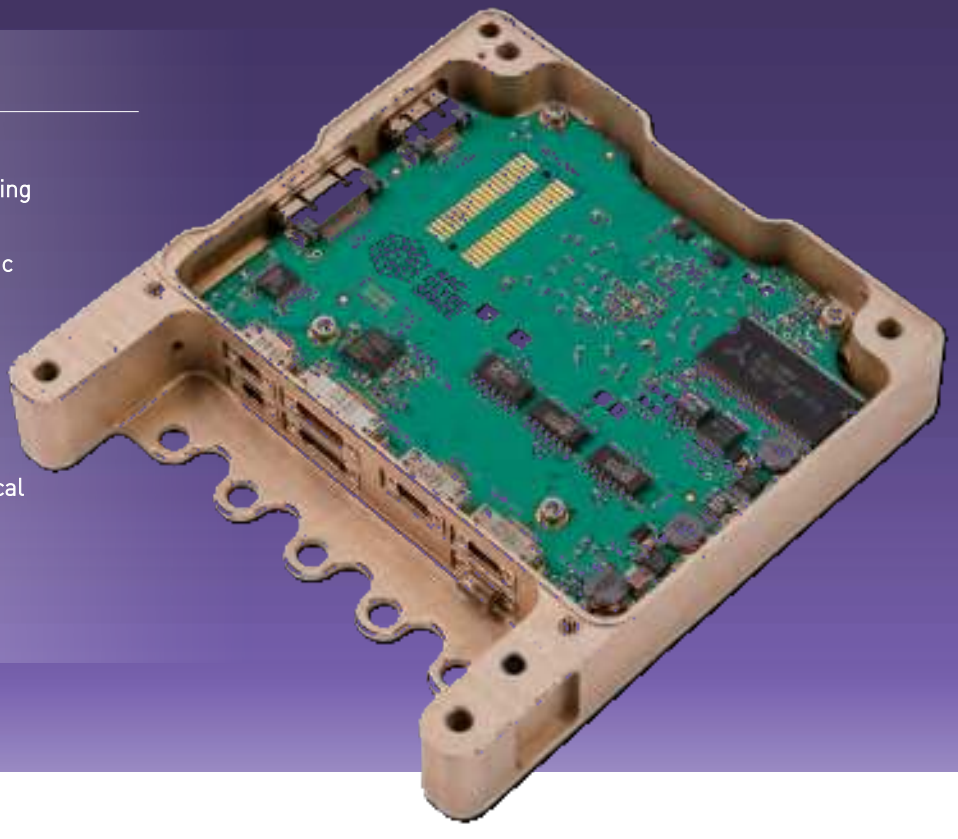
Sirius OBC LEON3FT

AAC Clyde Spcae has developed the Sirius OBC with LEON3FT enables a new reliable high-performance on-board computer specialized on advanced missions. Its real-time operating system runs on a LEON3FT fault-tolerant soft processor, is compliant to IEEE 1754 SPARC v8, and emphases on enhanced error detection and correction. The on-board computer is designed to emphasis high performance, resilience and reliability.

Main Features

- 50 MHz LEON3FT soft processor
- Reliable high-performance space data handling avionics
- Tolerant to Single-Event-Effects (SEE) in logic and data storage
- RTEMS real-time operating system (RTOS)
- SpaceWire on-board data bus
- Designed and qualified for five years in LEO
- ITAR free equipment
- Modular, nanosatellite compatible, mechanical design
- Pulse commands for low level, basic commanding



Technologies

The Sirius OBC with LEON3FT enables advanced nanosatellite constellations in LEO and deep space exploration missions due to its focus on high reliability, resilience and performance. Fault tolerance is secured through TMR (Triple-Modular Redundancy) on all FPGA flip-flops and through boot flash and EDAC (error detection and correction) on memories. Sirius OBC is tolerant to Single-Event-Effects (SEE) in logic/data storage and the equipment is ITAR free.

Modular Design

The Sirius products are designed for modularity. A standard single string system consists of an on-board computer (Sirius OBC) and a combined mass memory with CCSDS stack (Sirius TCM). The OBC runs mission specific software and manage the spacecraft system. The TCM receives and stores payload data and platform housekeeping data while at the same time distributing telecommands and serving mass memory data to the transceiver. A Sirius data handling system is easily adapted for additional capacity and redundancy by adding modules.

Technical Specifications

General

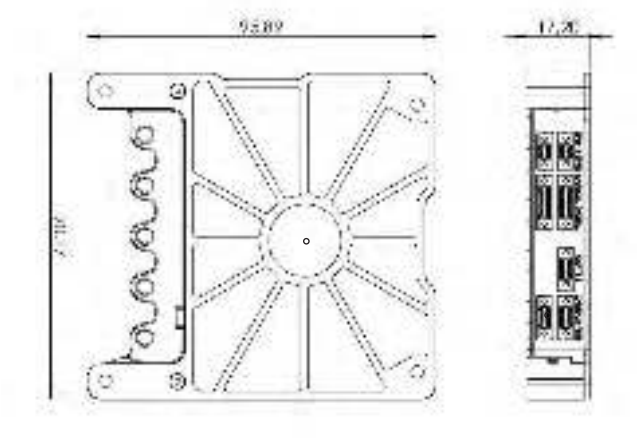
Expected Life	5 years in LEO
Processor	32-bit LEON3FT (IEEE-1754 SPARC v8) fault-tolerant processor
FPU	IEEE-754 single/double precision FPU
Processor Clock	50 MHz
SCET	15.25 µs accuracy
SDRAM	64 MB (post-EDAC)
Instruction Cache	8 kB
Data Cache	8 kB
NVRAM	16 kB (post-EDAC)
Operating Temperature Range	-30°C to +60°C
Nonvolatile System Memory Nand Flash	2 GB (post-EDAC)
Power Supply Input	4.5 V to 16 V
Radiation (TiD)	20 kRAD (qualified >30 kRAD, Si)

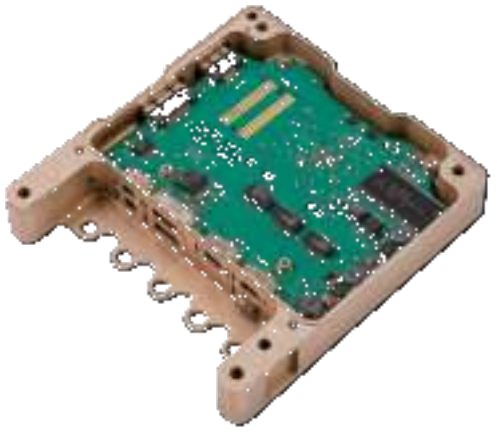
Interfaces

SpaceWire	50 Mbps	2
Serial Ports	RS422 / RS485 UARTs	6
Serial Ports	RS485-only UARTs	2
PSS Interface	RS485 PPS input / output	1/1
Analog Input Buffered	24 bit, up to 31250 SPS	8
GPIO	3.3 V logic	16
Debugging	JTAG port for CPU debugging via GRMON/GDB	1

Size, Weight and Power

Nominal Power Consumption	1.3 W
Mass	130 g
Length	95.89 mm
Width	90.17 mm
Height	17.20 mm





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