# DM3730, DM3725
# Digital Media Processors
### Check for Samples: DM3730, DM3725

## 1 DM3730, DM3725 Digital Media Processors

### 1.1 Features

- **DM3730/25 Digital Media Processors:**
  - **Compatible with OMAP™ 3 Architecture**
  - **ARM® Microprocessor (MPU) Subsystem**
    - **Up to 1-GHz ARM® Cortex™-A8 Core Also supports 300, 600, and 800-MHz operation**
    - **NEON™ SIMD Coprocessor**
  - **High Performance Image, Video, Audio (IVA2.2™) Accelerator Subsystem**
    - **Up to 800-MHz TMS320C64x+™ DSP Core Also supports 260, 520, and 660-MHz operation**
    - **Enhanced Direct Memory Access (EDMA) Controller (128 Independent Channels)**
    - **Video Hardware Accelerators**
  - **POWERVR SGX™ Graphics Accelerator (DM3730 only)**
    - **Tile Based Architecture Delivering up to 20 MPoly/sec**
    - **Universal Scalable Shader Engine: Multi-threaded Engine Incorporating Pixel and Vertex Shader Functionality**
    - **Industry Standard API Support: OpenGLES 1.1 and 2.0, OpenVG1.0**
    - **Fine Grained Task Switching, Load Balancing, and Power Management**
    - **Programmable High Quality Image Anti-Aliasing**
  - **Advanced Very-Long-Instruction-Word (VLIW) TMS320C64x+™ DSP Core**
    - **Eight Highly Independent Functional Units**
    - **Six ALUs (32-/40-Bit); Each Supports Single 32- bit, Dual 16-bit, or Quad 8-bit, Arithmetic per Clock Cycle**
    - **Two Multipliers Support Four 16 x 16-Bit Multiplies (32-Bit Results) per Clock Cycle or Eight 8 x 8-Bit Multiplies (16-Bit Results) per Clock Cycle**

- **Load-Store Architecture With Non-Aligned Support**
- **64 32-Bit General-Purpose Registers**
- **Instruction Packing Reduces Code Size**
- **All Instructions Conditional**
- **Additional C64x+™ Enhancements**
  - **Protected Mode Operation**
  - **Expectations Support for Error Detection and Program Redirection**
  - **Hardware Support for Modulo Loop Operation**
- **C64x+™ L1/L2 Memory Architecture**
  - **32K-Byte L1P Program RAM/Cache (Direct Mapped)**
  - **80K-Byte L1D Data RAM/Cache (2-Way Set- Associative)**
  - **64K-Byte L2 Unified Mapped RAM/Cache (4- Way Set-Associative)**
  - **32K-Byte L2 Shared SRAM and 16K-Byte L2 ROM**
- **C64x+™ Instruction Set Features**
  - **Byte-Addressable (8-/16-/32-/64-Bit Data)**
  - **8-Bit Overflow Protection**
  - **Bit-Field Extract, Set, Clear**
  - **Normalization, Saturation, Bit-Counting**
  - **Compact 16-Bit Instructions**
  - **Additional Instructions to Support Complex Multiplies**
- **External Memory Interfaces:**
  - **SDRAM Controller (SDRC)**
    - **16, 32-bit Memory Controller With 1G-Byte Total Address Space**
    - **Interfaces to Low-Power SDRAM**
    - **SDRAM Memory Scheduler (SMS) and Rotation Engine**
  - **General Purpose Memory Controller (GPMC)**
    - **16-bit Wide Multiplexed Address/Data**

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Bus
- – Up to 8 Chip Select Pins With 128M-Byte Address Space per Chip Select Pin
- – Glueless Interface to NOR Flash, NAND Flash (With ECC Hamming Code Calculation), SRAM and Pseudo-SRAM
- – Flexible Asynchronous Protocol Control for Interface to Custom Logic (FPGA, CPLD, ASICs, etc.)
- – Nonmultiplexed Address/Data Mode (Limited 2K-Byte Address Space)
- – 1.8-V I/O and 3.0-V (MMC1 only), 0.9-V to 1.2-V Adaptive Processor Core Voltage 0.9-V to 1.1-V Adaptive Core Logic Voltage Note: These are default Operating Performance Point (OPP) voltages and could be optimized to lower values using SmartReflex AVS.
- – Commercial, Industrial, and Extended Temperature Grades
- – Serial Communication
  - • 5 Multichannel Buffered Serial Ports (McBSPs)
    - – 512 Byte Transmit/Receive Buffer (McBSP1/3/4/5)
    - – 5K-Byte Transmit/Receive Buffer (McBSP2)
    - – SIDETONE Core Support (McBSP2 and 3 Only) For Filter, Gain, and Mix Operations
    - – Direct Interface to I2S and PCM Device and T Buses
    - – 128 Channel Transmit/Receive Mode
  - • Four Master/Slave Multichannel Serial Port Interface (McSPI) Ports
  - • High-Speed/Full-Speed/Low-Speed USB OTG Subsystem (12-/8-Pin ULPI Interface)
  - • High-Speed/Full-Speed/Low-Speed Multiport USB Host Subsystem
    - – 12-/8-Pin ULPI Interface or 6-/4-/3-Pin Serial Interface
  - • One HDQ/1-Wire Interface
  - • Four UARTs (One with Infrared Data Association [IrDA] and Consumer Infrared [CIR] Modes)
  - • Three Master/Slave High-Speed Inter-Integrated Circuit (I2C) Controllers
- – Camera Image Signal Processing (ISP)
  - • CCD and CMOS Imager Interface
  - • Memory Data Input
  - • BT.601/BT.656 Digital YCbCr 4:2:2 (8-/10-Bit) Interface
    - • Glueless Interface to Common Video Decoders
    - • Resize Engine
      - – Resize Images From 1/4x to 4x
      - – Separate Horizontal/Vertical Control
  - – System Direct Memory Access (SDMA) Controller (32 Logical Channels With Configurable Priority)
  - – Comprehensive Power, Reset, and Clock Management
    - • SmartReflex™ Technology
    - • Dynamic Voltage and Frequency Scaling (DVFS)
  - – ARM® Cortex™-A8 Core
    - • ARMv7 Architecture
      - – TrustZone®
      - – Thumb®-2
      - – MMU Enhancements
    - • In-Order, Dual-Issue, Superscalar Microprocessor Core
    - • NEON Multimedia Architecture
    - • Over 2x Performance of ARMv6 SIMD
    - • Supports Both Integer and Floating Point SIMD
    - • Jazelle® RCT Execution Environment Architecture
    - • Dynamic Branch Prediction with Branch Target Address Cache, Global History Buffer, and 8-Entry Return Stack
    - • Embedded Trace Macrocell (ETM) Support for Non-Invasive Debug
  - – ARM Cortex-A8 Memory Architecture:
    - • 32K-Byte Instruction Cache (4-Way Set-Associative)
    - • 32K-Byte Data Cache (4-Way Set-Associative)
    - • 256K-Byte L2 Cache
  - – 32K-Byte ROM
  - – 64K-Byte Shared SRAM
  - – Endianess:
    - • ARM Instructions - Little Endian
    - • ARM Data – Configurable
    - • DSP Instructions/Data - Little Endian
- • Removable Media Interfaces:
  - – Three Multimedia Card (MMC)/ Secure Digital (SD) With Secure Data I/O (SDIO)
- • Test Interfaces
  - – IEEE-1149.1 (JTAG) Boundary-Scan Compatible
  - – Embedded Trace Macro Interface (ETM)
  - – Serial Data Transport Interface (SDTI)
- • 12 32-bit General Purpose Timers
- • 2 32-bit Watchdog Timers

- **1 32-bit Secure Watchdog Timer**
- **1 32-bit 32-kHz Sync Timer**
- **Up to 188 General-Purpose I/O (GPIO) Pins (Multiplexed With Other Device Functions)**
- **45-nm CMOS Technology**
- **Package-On-Package (POP) Implementation for Memory Stacking (Not Available in CUS Package)**

- **Packages:**
  - **515-pin s-PBGA package (CBP Suffix), .5mm Ball Pitch (Top), .4mm Ball Pitch (Bottom)**
  - **515-pin s-PBGA package (CBC Suffix), .65mm Ball Pitch (Top), .5mm Ball Pitch (Bottom)**
  - **423-pin s-PBGA package (CUS Suffix), .65mm Ball Pitch**

## 1.2 Description

The DM37x generation of high-performance, digital media processors are based on the enhanced device architecture and are integrated on TI's advanced 45-nm process technology. This architecture is designed to provide best in class ARM and Graphics performance while delivering low power consumption. This balance of performance and power allow the device to support the following example applications:

- Portable Data Terminals
- Navigation
- Auto Infotainment
- Gaming
- Medical Imaging
- Home Automation
- Human Interface
- Industrial Control
- Test and Measurement
- Single board Computers

The device can support numerous HLOS and RTOS solutions including Linux and Windows Embedded CE which are available directly from TI. Additionally, the device is fully backward compatible with previous Cortex™-A8 processors and OMAP™ processors.

This DM3730/25 Digital Media Processor data manual presents the electrical and mechanical specifications for the DM3730/25 Digital Media Processor. The information contained in this data manual applies to the commercial, industrial, and extended temperature versions of the DM3730/25 Digital Media Processor unless otherwise indicated. It consists of the following sections:

- A description of the DM3730/25 terminals: assignment, electrical characteristics, multiplexing, and functional description
- A presentation of the electrical characteristics requirements: power domains, operating conditions, power consumption, and dc characteristics
- The clock specifications: input and output clocks, DPLL and DLL
- A description of thermal characteristics, device nomenclature, and mechanical data about the available packaging

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Product Folder Link(s): *DM3730  DM3725*

## 1.3 Functional Block Diagram

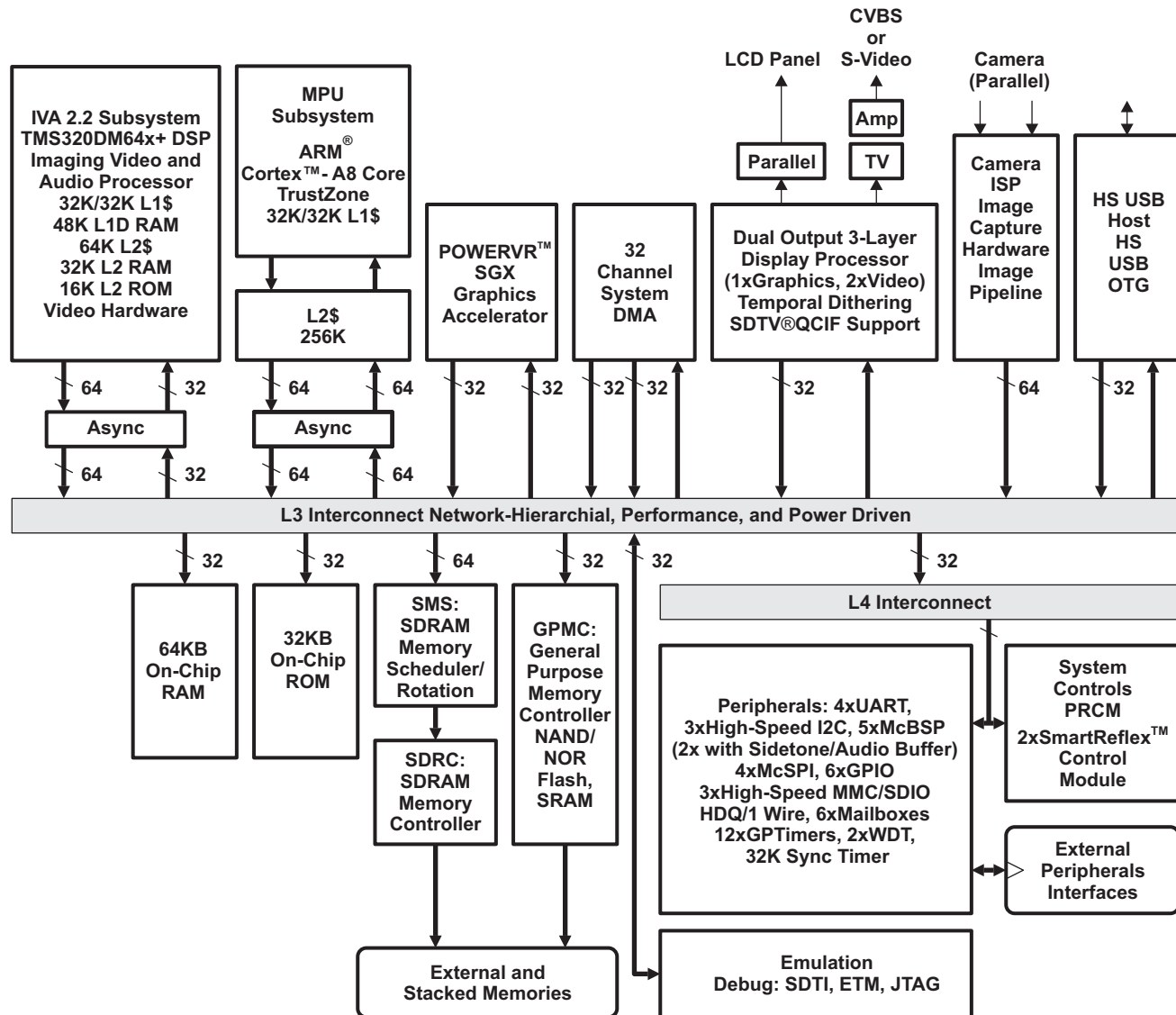The functional block diagram of the DM3730/25 Digital Media Processor is shown below.



**Figure 1-1. DM3730/25 Functional Block Diagram**

## Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

This data sheet revision history highlights the technical changes made from the previous to the current revision.

### Revision History

| SECTION | ADDITIONS/CHANGES/DELETIONS |
|---|---|
| Terminal Description | Changed:<br>• Table 2-1. Ball Characteristics (CBP Pkg.). Removed restriction note from GPIO_16.<br>• Table 2-2. Ball Characteristics (CBC Pkg.). Removed restriction note from GPIO_16.<br>• Table 2-3. Ball Characteristics (CUS Pkg.). Removed restriction note from GPIO_16. |
| Electrical Characteristics | Changed:<br>• Table 3-1. Absolute Maximum Rating over Junction Temperature Range. Added JTAG to VESD.<br>• Table 3-5. DC Electrical Characteristics. Removed USIM ball R27. |
| Clock Specifications | Added note on rise and fall times for these tables:<br>• Input Clock Requirements<br>• sys_xtalin Squarer Input Clock Timing Requirements - Bypass Mode<br>• sys_32k Input Clock Timing Requirements<br>• sys_altclk Input Clock Timing Requirements<br>• sys_clkout1 Output Clock Switching Characteristics<br>• sys_clkout2 Output Clock Switching Characteristics<br><br>Added:<br>• Table 4-2, Crystal Electrical Characteristics. Added entry for DL - Crystal drive level |

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Product Folder Link(s): *DM3730  DM3725*

# 2 TERMINAL DESCRIPTION

## 2.1 Terminal Assignment

Figure 2-1 through Figure 2-5 show the ball locations for the 515- and 423- ball plastic ball grid array (s-PBGA) packages. Table 2-1 through Table 2-25 indicate the signal names and ball grid numbers for both packages.

**Note**: There are no balls present on the top of the 423-ball s-PBGA package.



030-001
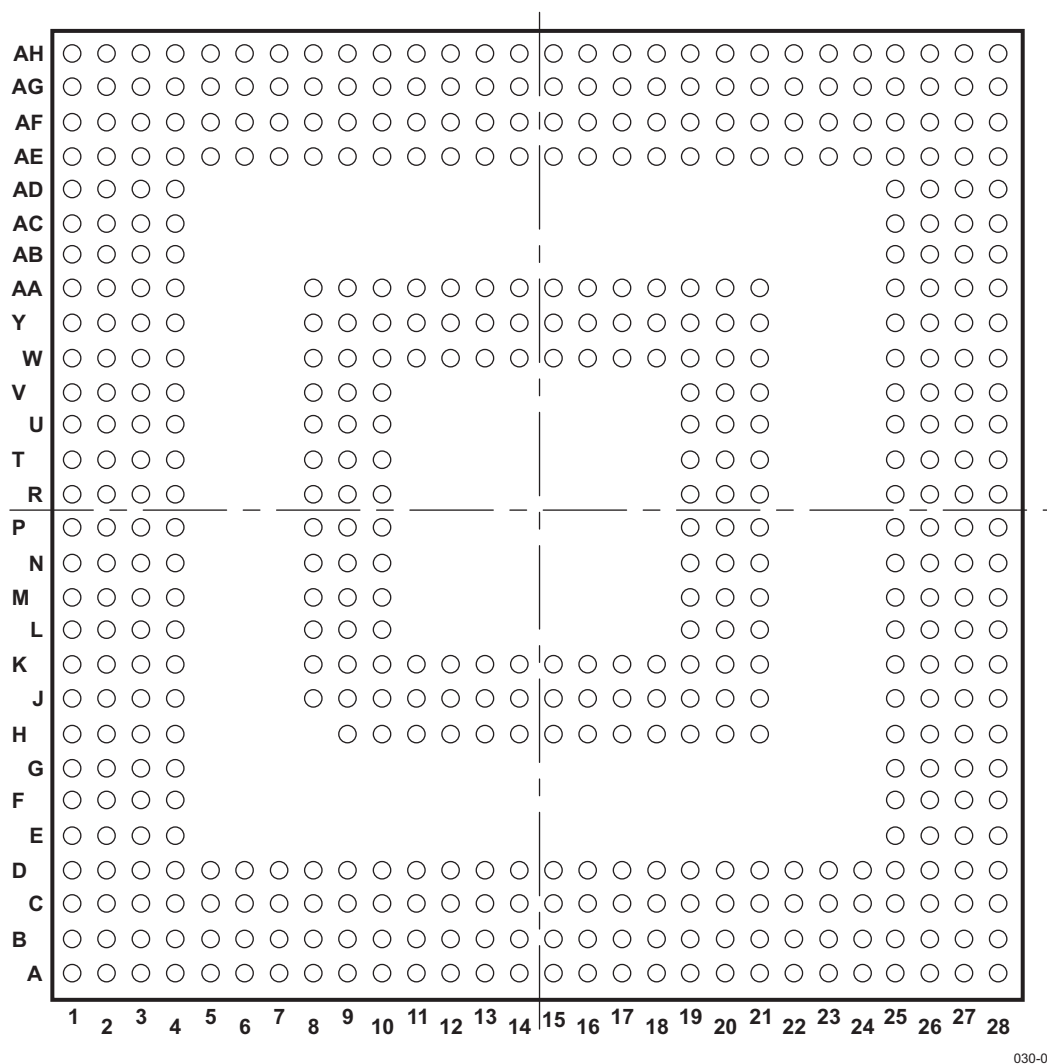
**Figure 2-1. DM3730/25 Digital Media Processor CBP s-PBGA-N515 Package (Bottom View)**
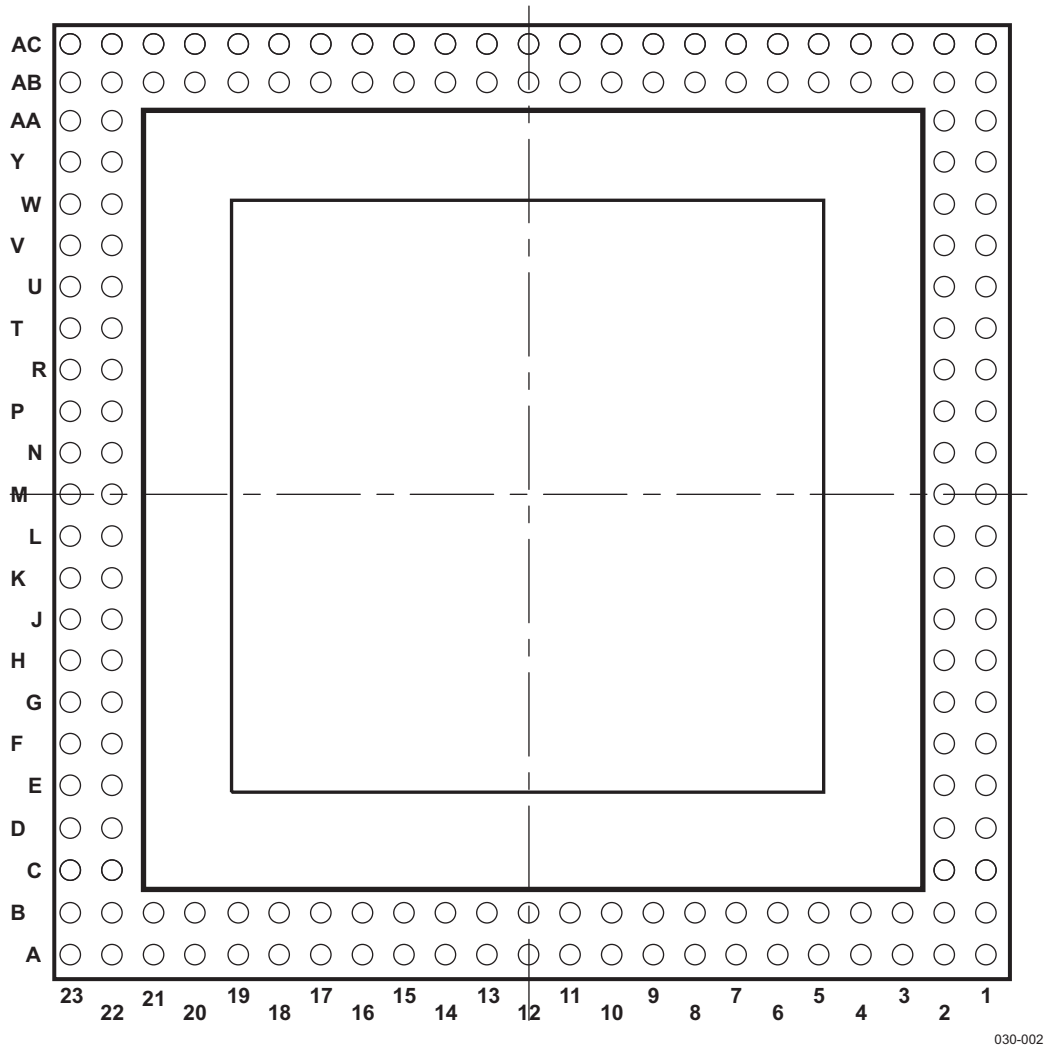
**Figure 2-2. DM3730/25 Digital Media Processor CBP s-PBGA-N515 Package (Top View)**
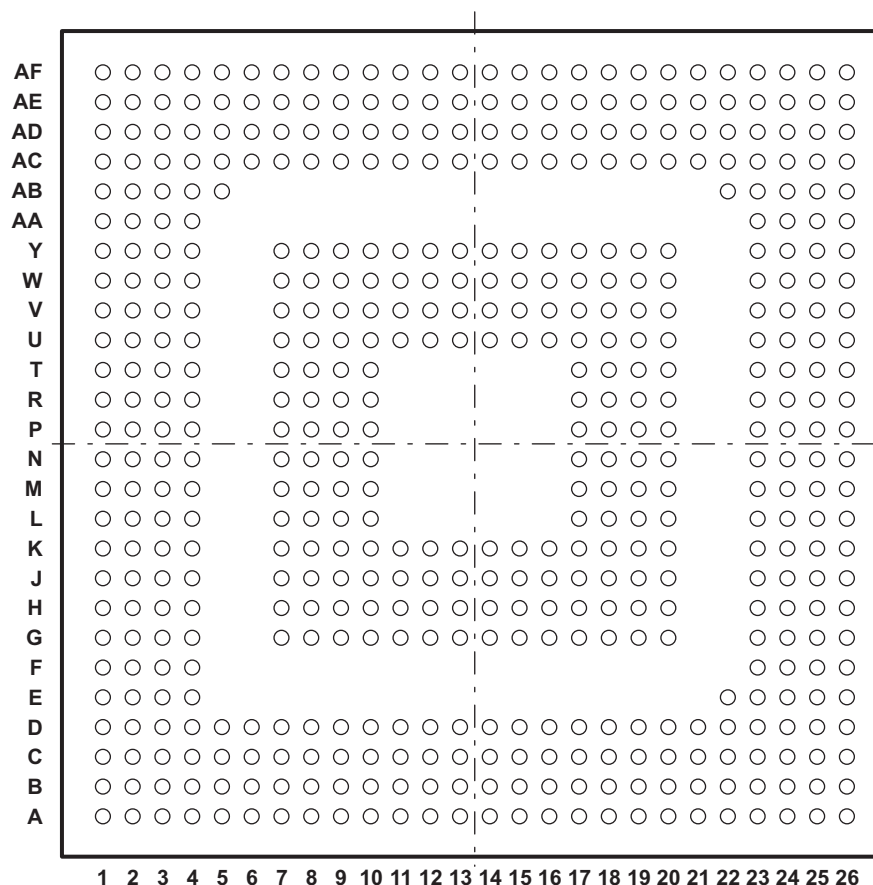
**Figure 2-3. DM3730/25 Digital Media Processor CBC s-PBGA-515 Package (Bottom View)**
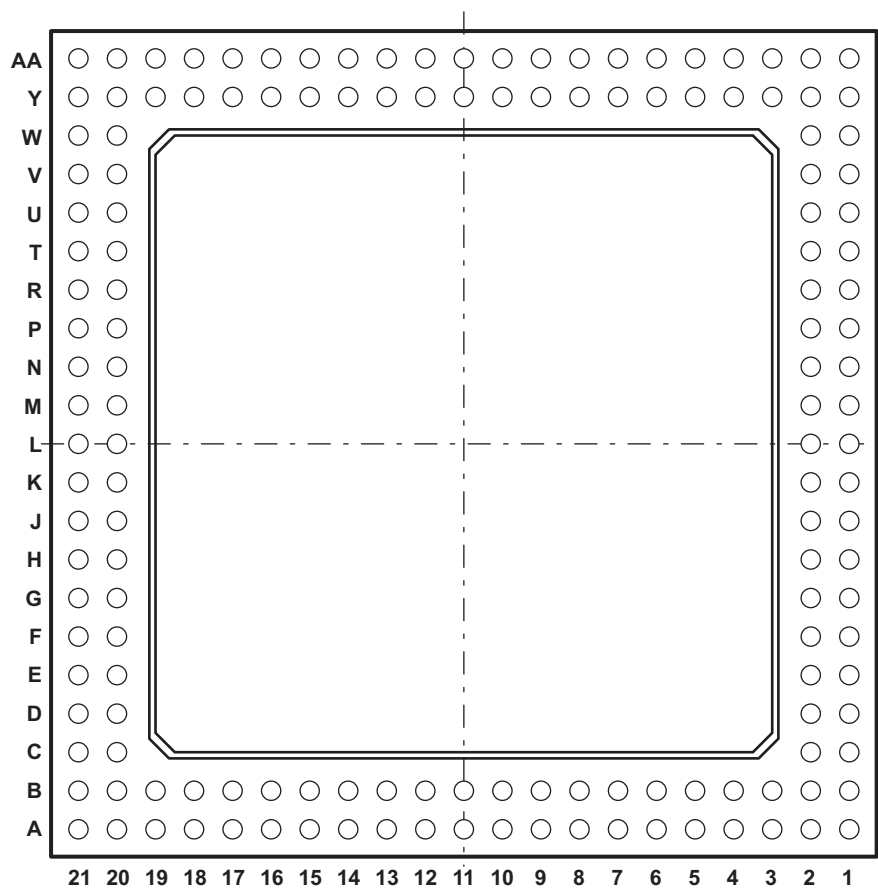
**Figure 2-4. DM3730/25 Digital Media Processor CBC s-PBGA-515 Package (Top View)**
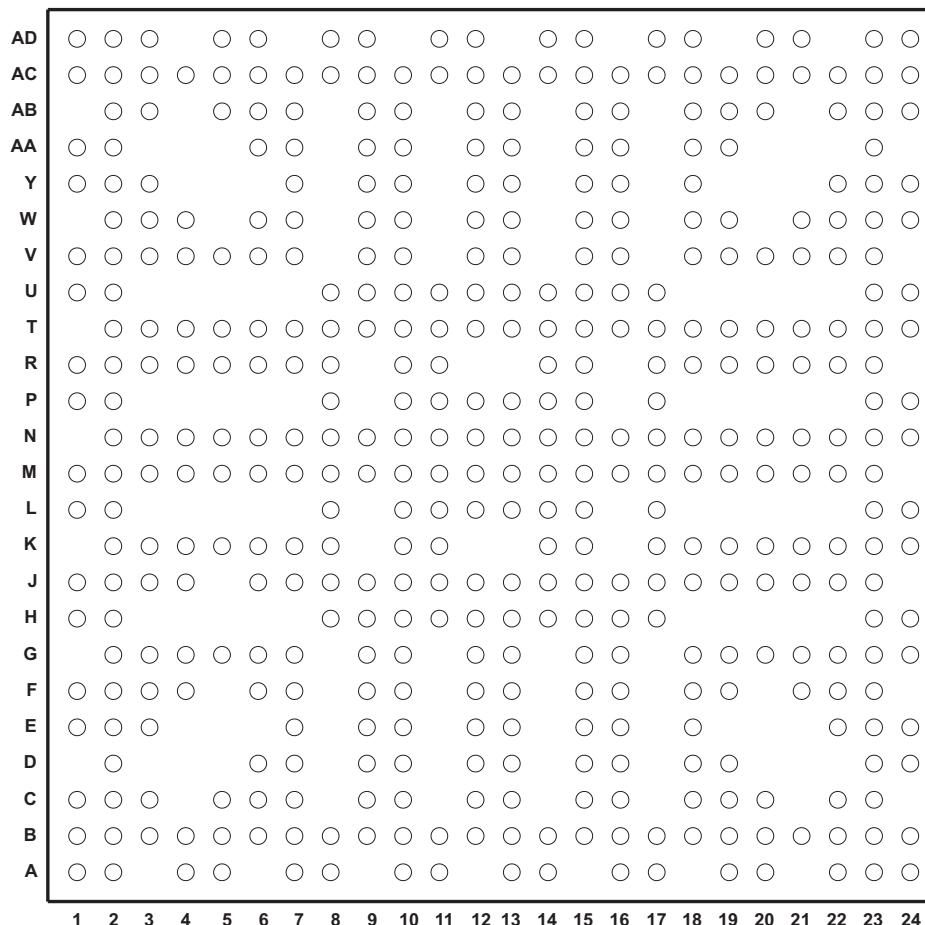
**Figure 2-5. DM3730/25 Digital Media Processor CUS s-PBGA-N423 Package (Bottom View)**

## 2.2 Pin Assignments

### 2.2.1 Pin Map (Top View)

The following pin maps show the top views of the 515-pin sPBGA package **[CBP]**, the 515-pin sPBGA package **[CBC]**, and the 423-pin sPBGA package **[CUS]** pin assignments in four quadrants (A, B, C, and D).

**Note**: A pin with an "NC" designator indicates No Connection. For proper device operation, these pins must be left unconnected.

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | NC | NC | vss | NC | vdds_mem | NC | NC | vdds_mem | NC | NC | NC | vdds_mem | NC | NC |
| B | NC | vss | NC | NC | vdds_mem | NC | NC | vdds_mem | NC | NC | NC | vdds_mem | NC | NC |
| C | NC | NC | NC | NC | NC | NC | vss | NC | NC | vss | NC | NC | vss | NC |
| D | NC | NC | NC | NC | NC | NC | vss | vdd_core | vdd_core | vss | NC | NC | vss | NC |
| E | NC | NC | vss | vss | | | | | | | | | | |
| F | vdds_mem | vdds_mem | gpmc_nadv_ale | gpmc_nwe | | | | | | | | | | |
| G | NC | gpmc_noe | gpmc_nbe0_cle | gpmc_ncs0 | | | | | | | | | | |
| H | gpmc_nwp | gpmc_d8 | gpmc_ncs1 | vdd_core | | | | | NC | NC | NC | NC | NC | NC |
| J | vdds_mem | vdds_mem | vss | vdd_core | | | | gpmc_wait3 | vdd_mpu_iva | vdd_mpu_iva | vdd_mpu_iva | vss | vss | vdd_mpu_iva |
| K | gpmc_d0 | gpmc_d9 | gpmc_a10 | gpmc_a4 | | | | gpmc_wait2 | vss | vss | vdd_mpu_iva | vss | vdd_mpu_iva | vdd_mpu_iva |
| L | gpmc_d1 | gpmc_d2 | gpmc_a9 | gpmc_a3 | | | | gpmc_wait1 | vdd_mpu_iva | vdd_mpu_iva | | | | |
| M | pop_y23_m1 | pop_k2_m2 | gpmc_a8 | gpmc_a2 | | | | gpmc_wait0 | vdd_mpu_iva | vdd_mpu_iva | | | | |
| N | pop_u1_n1 | pop_l2_n2 | gpmc_a7 | gpmc_a1 | | | | gpmc_ncs7 | vss | vdd_mpu_iva | | | | |
| P | gpmc_d10 | gpmc_d3 | vss | vss | | | | gpmc_ncs6 | vss | vss | | | | |

A.   Top Views are provided to assist in hardware debugging efforts.

**Figure 2-6. CBP Pin Map [Quadrant A - Top View]**

| | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | pop_a12_a15 | NC | NC | vdds_mem | NC | NC | NC | vdds_mem | cam_vs | cam_hs | cam_d5 | vss | pop_a22_a27 | pop_a23_a28 | A |
| | pop_b12_b15 | NC | NC | vdds_mem | NC | NC | NC | vdds_mem | cam_wen | cam_d2 | cam_d10 | cam_xclkb | vss | pop_b23_b28 | B |
| | NC | vdds_mem | NC | NC | vss | NC | NC | vss | cam_fld | cam_d3 | cam_xclka | cam_d11 | cam_pclk | vdds_mem | C |
| | vdd_core | vdds_mem | NC | NC | vss | NC | vss | vdd_core | vdd_core | cam_d4 | cam_strobe | dss_hsync | dss_vsync | dss_pclk | D |
| | | | | | | | | | | | vdd_core | dss_data6 | dss_acbias | dss_data20 | E |
| | | | | | | | | | | | vdds | vdds | dss_data8 | dss_data7 | F |
| | | | | | | | | | | | dss_data16 | dss_data9 | vss | vdds_mem | G |
| | NC | NC | NC | uart3_cts_rctx | uart3_rts_sd | uart3_rx_irrx | uart3_tx_irtx | | | | dss_data19 | dss_data18 | dss_data17 | vdds | H |
| | vdd_mpu_iva | vss | vss | vdd_core | vdd_core | vdd_core | i2c1_sda | | | | hdq_sio | dss_data21 | pop_h22_j27 | pop_k1_j28 | J |
| | vdda_dplls_dll | vss | vss | vdd_core | vss | vdd_core | i2c1_scl | | | | vdds_mmc1 | mcbsp1_fsx | cam_d8 | cam_d6 | K |
| | | | | | vss | vss | cap_vdd_sram_core | | | | vdd_core | vss | cam_d9 | cam_d7 | L |
| | | | | | vdd_core | vss | mcbsp2_dx | | | | vdd_core | pop_k22_m26 | mmc1_cmd | vss | M |
| | | | | | vdd_core | vdd_core | mcbsp2_clkx | | | | mmc1_dat2 | mmc1_dat1 | mmc1_dat0 | mmc1_clk | N |
| | | | | | vss | vdd_core | mcbsp2_fsx | | | | vdds_x | gpio_127 | gpio_126 | mmc1_dat3 | P |

**Figure 2-7. CBP Pin Map [Quadrant B - Top View]**

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| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R | gpmc_d11 | gpmc_d12 | gpmc_a6 | vdds_mem | | | | gpmc_ncs5 | vdd_mpu_iva | vdd_mpu_iva | | | | |
| T | gpmc_d4 | gpmc_d13 | gpmc_a5 | gpmc_clk | | | | gpmc_ncs4 | vdd_mpu_iva | vdd_mpu_iva | | | | |
| U | vdds_mem | vss | gpmc_nbe1 | cap_vdd_bb_mpu_iva | | | | gpmc_ncs3 | vss | vdd_mpu_iva | | | | |
| V | gpmc_d5 | gpmc_d6 | mcspi2_cs1 | cap_vdd_sram_mpu_iva | | | | gpmc_ncs2 | vss | vss | | | | |
| W | gpmc_d14 | gpmc_d7 | vss | vdds | | | | uart1_cts | vdd_mpu_iva | vss | vdd_mpu_iva | vdd_mpu_iva | vss | vss |
| Y | gpmc_d15 | mcspi2_simo | mcspi2_somi | mcspi2_cs0 | | | | uart1_rx | vdd_mpu_iva | vdd_mpu_iva | vdd_mpu_iva | vss | vss | vdd_mpu_iva |
| AA | pop_aa1_aa1 | pop_aa2_aa2 | mcspi2_clk | mcspi1_somi | | | | uart1_tx | uart1_rts | jtag_emu1 | jtag_emu0 | jtag_rtck | jtag_tck | vdda_wkup_bg_bb |
| AB | mcspi1_cs2 | mcspi1_cs3 | mcspi1_clk | mcspi1_simo | | | | | | | | | | |
| AC | mcbsp4_fsx | mcspi1_cs0 | mcspi1_cs1 | vdd_core | | | | | | | | | | |
| AD | mcbsp4_dr | mcbsp4_dx | vdds | vdds | | | | | | | | | | |
| AE | mcbsp4_clkx | mmc2_clk | mmc2_dat7 | mmc2_dat4 | mcbsp3_fsx | mcbsp3_dr | etk_d10 | vdds | vdd_core | etk_ctl | etk_d4 | vss | etk_d3 | sys_boot2 |
| AF | pop_ac8_af1 | pop_u2_af2 | mmc2_dat6 | mmc2_dat3 | mcbsp3_clkx | mcbsp3_dx | etk_d11 | vdds | etk_d8 | etk_clk | etk_d0 | vss | etk_d6 | i2c3_scl |
| AG | pop_ab1_ag1 | vss | vss | mmc2_dat2 | mmc2_cmd | vss | etk_d12 | etk_d14 | etk_d9 | pop_ab8_ag10 | pop_ab9_ag11 | etk_d1 | pop_ab11_ag13 | i2c3_sda |
| AH | pop_ac1_ah1 | pop_ac2_ah2 | mmc2_dat5 | mmc2_dat1 | mmc2_dat0 | vdds_mem | etk_d13 | etk_d15 | etk_d5 | pop_ac13_ah10 | pop_ac9_ah11 | etk_d2 | pop_ac11_ah13 | etk_d7 |

**Figure 2-8. CBP Pin Map [Quadrant C - Top View]**

| Row | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R | | | | | vss | vss | mcbsp2_dr | | | | gpio_129 | vss | gpio_128 | hsusb0_dir |
| T | | | | | vdd_core | vss | mcbsp_clks | | | | hsusb0_stp | hsusb0_nxt | hsusb0_data0 | hsusb0_clk |
| U | | | | | vdd_core | vdd_core | mcbsp1_dr | | | | hsusb0_data4 | hsusb0_data3 | hsusb0_data2 | hsusb0_data1 |
| V | | | | | vss | vdd_core | mcbsp1_dx | | | | vdda_dac | hsusb0_data7 | hsusb0_data6 | hsusb0_data5 |
| W | vdd_mpu_iva | vdds_sram | vss | vdd_core | vss | vdd_core | mcbsp1_clkx | | | | vss | cvideo1_rset | cvideo2_vfb | cvideo2_out |
| Y | vdd_mpu_iva | vdd_core | sys_xtalgnd | vdd_core | vdd_core | vdd_core | mcbsp1_clkr | | | | vss | vssa_dac | cvideo1_vfb | cvideo1_out |
| AA | cap_vddu_wkup_logic | vdda_dpll_per | jtag_ntrst | jtag_tms_tmsc | jtag_tdo | jtag_tdi | mcbsp1_fsr | | | | uart2_tx | NC | dss_data15 | dss_data14 |
| AB | | | | | | | | | | | uart2_rts | uart2_cts | dss_data13 | dss_data12 |
| AC | | | | | | | | | | | vss | vss | dss_data22 | dss_data23 |
| AD | | | | | | | | | | | uart2_rx | i2c4_scl | dss_data11 | dss_data10 |
| AE | i2c2_sda | vdds | sys_xtalin | vdd_core | vdd_core | vss | sys_boot5 | sys_clkout2 | vdds | vdd_core | sys_32k | i2c4_sda | NC | pop_aa23_ae28 |
| AF | i2c2_scl | vdds | sys_xtalout | sys_boot3 | sys_boot4 | vss | sys_boot6 | sys_off_mode | vdds | sys_nreswarm | sys_clkreq | sys_nirq | pop_aa22_af27 | pop_h23_af28 |
| AG | pop_ab13_ag15 | vss | cam_d0 | gpio_114 | gpio_112 | vdds | vdds | dss_data0 | dss_data2 | dss_data4 | sys_clkout1 | sys_boot1 | vdds | pop_ab23_ag28 |
| AH | pop_l1_ah15 | pop_ac14_ah16 | cam_d1 | gpio_115 | gpio_113 | cap_vddu_array | vss | dss_data1 | dss_data3 | dss_data5 | sys_nrespwron | sys_boot0 | pop_ac22_ah27 | pop_ac23_ah28 |

**Figure 2-9. CBP Pin Map [Quadrant D - Top View]**

TERMINAL DESCRIPTION    15

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | pop_a1_a1 | NC | gpmc_ncs2 | gpmc_a11 | NC | vss | NC | vss | NC | NC | NC | NC | vss |
| B | NC | vss | gpmc_wait2 | gpmc_ncs4 | gpmc_ncs6 | gpmc_ncs3 | NC | NC | NC | NC | NC | NC | NC |
| C | I2C2_SDA | i2c2_scl | sys_boot2 | gpmc_ncs5 | gpmc_ncs7 | gpmc_wait3 | NC | NC | NC | NC | vdds | vss | NC |
| D | gpmc_a9 | gpmc_a10 | sys_boot1 | sys_boot6 | NC | cap_vdd_bb_mpu_iva | vss | NC | vdds | vss | NC | vss | vdd_mpu_iva |
| E | gpmc_a7 | gpmc_a8 | sys_boot3 | sys_boot4 | | | | | | | | | |
| F | gpmc_a5 | gpmc_a6 | sys_boot0 | NC | | | | | | | | | |
| G | vss | gpmc_a4 | sys_boot5 | vdds | | | NC | vss | vdd_mpu_iva | vss | vdd_core | vdd_mpu_iva | NC |
| H | gpmc_a2 | gpmc_a3 | uart1_rx | vss | | | vdd_mpu_iva | NC | NC | NC | NC | NC | NC |
| J | gpmc_nbe1 | gpmc_a1 | NC | NC | | | NC | NC | NC | NC | NC | NC | NC |
| K | vss | gpmc_nbe0_cle | mmc2_dat7 | NC | | | NC | NC | NC | NC | vdd_mpu_iva | NC | vdda_dplls_dll |
| L | pop_j1_l1 | gpmc_d14 | mmc2_dat6 | uart1_tx | | | vdds | NC | vdd_mpu_iva | vss | | | |
| M | gpmc_nwe | gpmc_d15 | mmc2_dat5 | vdds | | | vdd_core | NC | vdd_mpu_iva | vdd_mpu_iva | | | |
| N | gpmc_clk | gpmc_noe | mcbsp3_dr | vss | | | vdd_mpu_iva | vdd_mpu_iva | cap_vdd_sram_mpu_iva | vss | | | |

A.    Top Views are provided to assist in hardware debugging efforts.

**Figure 2-10. CBC Pin Map [Quadrant A - Top View]**

| | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **A** | NC | NC | NC | NC | vdds | NC | pop_b16_a20 | NC | NC | cam_wen | cam_d2 | pop_a20_a25 | pop_a21_a26 | A |
| **B** | NC | NC | NC | NC | NC | NC | NC | NC | NC | cam_fld | cam_d3 | vss | pop_b21_b26 | B |
| **C** | NC | NC | NC | NC | NC | NC | NC | NC | NC | cam_hs | cam_d5 | cam_xclka | cam_pclk | C |
| **D** | vss | vdd_core | NC | NC | vss | NC | vss | NC | NC | cam_vs | cam_d4 | cam_d10 | cam_strobe | D |
| **E** | | | | | | | | | vss | NC | vdds | cam_xclkb | cam_d11 | E |
| **F** | | | | | | | | | | uart3_cts_rctx | uart3_rts_sd | dss_data20 | dss_acbias | F |
| **G** | NC | NC | NC | NC | vdd_core | NC | vss | | | vss | uart3_tx_irtx | dss_pclk | dss_data6 | G |
| **H** | NC | NC | NC | NC | NC | NC | vdd_core | | | NC | uart3_rx_irrx | dss_data7 | dss_data8 | H |
| **J** | NC | vdds | NC | NC | vdds | NC | NC | | | hdq_sio | i2c1_sda | i2c1_scl | dss_data9 | J |
| **K** | cap_vddu_wkup_logic | vss | NC | NC | mmc1_dat2 | NC | cap_vdd_sram_core | | | NC | dss_hsync | vss | pop_h21_k26 | K |
| **L** | | | | vss | mmc1_cmd | vss | vdds | | | vss | vdds | dss_data16 | dss_data17 | L |
| **M** | | | | vdd_core | mmc1_dat1 | mmc1_dat0 | gpio_126 | | | NC | dss_data18 | dss_vsync | dss_data19 | M |
| **N** | | | | vss | NC | mmc1_clk | mmc1_dat3 | | | vdds_mmc1 | dss_data21 | cam_d8 | cam_d9 | N |

**Figure 2-11. CBC Pin Map [Quadrant B - Top View]**

TERMINAL DESCRIPTION     17

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| P | gpmc_d13 | NC | mcbsp3_dx | NC | | | mcspi1_somi | mcspi1_simo | mcspi1_clk | vdd_mpu_iva | | | |
| R | vss | uart1_rts | mcbsp4_dx | vss | | | mcspi1_cs0 | mcspi1_cs1 | mcspi1_cs2 | mmc2_cmd | | | |
| T | gpmc_d10 | pop_n2_t2 | mcbsp4_fsx | vdds | | | vdd_core | mcspi1_cs3 | mmc2_dat1 | mmc2_dat0 | | | |
| U | gpmc_d12 | gpmc_d11 | mcbsp3_clkx | mcbsp4_dr | | | vdd_mpu_iva | mcspi2_somi | mmc2_dat3 | mmc2_dat2 | vdd_mpu_iva | vdds_sram | vdd_mpu_iva |
| V | gpmc_d8 | etk_d9 | mcbsp4_clkx | NC | | | vdd_mpu_iva | mcspi2_cs0 | mcspi2_cs1 | mmc2_dat4 | vdd_mpu_iva | sys_off_mode | sys_nrespwron |
| W | vss | uart1_cts | mcbsp3_fsx | vss | | | mcspi2_clk | mcspi2_simo | vdd_mpu_iva | mmc2_clk | sys_clkout2 | NC | jtag_rtck |
| Y | gpmc_d9 | pop_t2_y2 | etk_d4 | vdds | | | vss | vdd_core | vdd_mpu_iva | vss | vdd_mpu_iva | vdd_core | jtag_tdo |
| AA | gpmc_d1 | gpmc_d0 | etk_d3 | etk_d8 | | | | | | | | | |
| AB | etk_d5 | etk_clk | etk_ctl | i2c3_scl | vss | | | | | | | | |
| AC | gpmc_d3 | gpmc_d2 | etk_d0 | i2c3_sda | gpmc_d7 | gpmc_nwp | vdds | gpmc_wait1 | NC | vss | gpmc_wait0 | NC | NC |
| AD | gpmc_ncs1 | etk_d7 | etk_d2 | etk_d1 | gpmc_d6 | gpmc_d5 | sys_nreswarm | gpmc_ncs0 | NC | gpmc_nadv_ale | NC | NC | NC |
| AE | NC | pop_w2_ae2 | etk_d6 | etk_d10 | gpmc_d4 | etk_d12 | vss | NC | etk_d15 | vdds | NC | NC | NC |
| AF | NC | NC | NC | pop_y2_af4 | pop_aa6_af5 | etk_d11 | etk_d13 | pop_y7_af8 | etk_d14 | pop_y9_af10 | NC | pop_aa10_af12 | pop_aa11_af13 |

**Figure 2-12. CBC Pin Map [Quadrant C - Top View]**

| | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| P | | | | gpio_127 | gpio_128 | gpio_129 | mcbsp1_fsx | | | vdds_x | NC | cam_d6 | cam_d7 | P |
| R | | | | vss | mcbsp2_clkx | mcbsp2_dx | vdd_core | | | NC | NC | NC | NC | R |
| T | | | | mcbsp1_clkx | mcbsp2_dr | mcbsp_clks | mcbsp1_dr | | | vss | vdds | NC | NC | T |
| U | vdda_dpll_per | jtag_ntrst | jtag_tdi | mcbsp1_dx | mcbsp2_fsx | mcbsp1_clkr | hsusb0_stp | | | NC | cvideo2_vfb | vss | pop_p21_u26 | U |
| V | jtag_tck | jtag_tms_tmsc | sys_nirq | mcbsp1_fsr | hsusb0_data2 | hsusb0_dir | hsusb0_data0 | | | cvideo1_rset | vssa_dac | vdda_dac | cvideo2_out | V |
| W | vdda_wkup_bg_bb | sys_clkreq | i2c4_sda | hsusb0_data4 | hsusb0_nxt | hsusb0_clk | hsusb0_data3 | | | vss | vdds | cvideo1_vfb | cvideo1_out | W |
| Y | jtag_emu1 | jtag_emu0 | vss | hsusb0_data7 | hsusb0_data5 | hsusb0_data6 | hsusb0_data1 | | | NC | uart2_cts | dss_data13 | vss | Y |
| AA | | | | | | | | | | NC | uart2_rts | dss_data12 | dss_data14 | AA |
| AB | | | | | | | | | vss | NC | vdds | dss_data23 | dss_data15 | AB |
| AC | NC | vdds | vss | NC | vdds | vss | NC | vdd_core | NC | NC | vdds | dss_data22 | dss_data10 | AC |
| AD | vss | i2c4_scl | gpio_113 | gpio_112 | vdds | vdds | vdds | uart2_rx | uart2_tx | dss_data4 | dss_data5 | vss | dss_data11 | AD |
| AE | sys_clkout1 | cam_d1 | cam_d0 | gpio_115 | gpio_114 | cap_vddu_array | sys_32k | dss_data0 | dss_data1 | dss_data2 | dss_data3 | pop_y20_ae25 | pop_y21_ae26 | AE |
| AF | pop_aa12_af14 | pop_aa13_af15 | pop_aa14_af16 | pop_y14_af17 | pop_aa17_af18 | sys_xtalin | sys_xtalout | pop_y17_af21 | pop_aa19_af22 | sys_xtalgnd | pop_y19_af24 | pop_aa20_af25 | pop_aa21_af26 | AF |
| | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | |

**Figure 2-13. CBC Pin Map [Quadrant D - Top View]**

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Product Folder Link(s): DM3730  DM3725

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | NC | NC | | sdrc_a0 | sdrc_dqs0 | | sdrc_dm2 | sdrc_dqs2 | | sdrc_clk | sdrc_nclk | |
| B | NC | sdrc_a4 | sdrc_a3 | sdrc_a1 | sdrc_d3 | sdrc_dm0 | sdrc_d7 | sdrc_d18 | sdrc_d19 | sdrc_d21 | sdrc_d8 | sdrc_d10 |
| C | gpmc_wait0 | gpmc_wait3 | sdrc_a5 | | sdrc_d1 | sdrc_d2 | sdrc_d6 | | sdrc_d16 | sdrc_d20 | | sdrc_d9 |
| D | | gpmc_ncs3 | | | | sdrc_a2 | sdrc_d0 | | sdrc_d4 | sdrc_d5 | | sdrc_d22 |
| E | gpmc_nwp | gpmc_ncs0 | sdrc_a6 | | | | sdrc_a10 | | sdrc_a9 | sdrc_a8 | | sdrc_d17 |
| F | gpmc_nadv_ale | gpmc_noe | gpmc_ncs6 | gpmc_ncs4 | | sdrc_a7 | sdrc_a13 | | sdrc_a14 | vdd_mpu_iva | | vdd_core |
| G | | gpmc_a10 | gpmc_nwe | gpmc_ncs7 | gpmc_ncs5 | sdrc_a11 | sdrc_a12 | | vdd_mpu_iva | vdd_mpu_iva | | vdd_core |
| H | gpmc_a8 | gpmc_a9 | | | | | | vdds_x | vdd_mpu_iva | vdd_mpu_iva | vss | vdd_core |
| J | gpmc_a7 | gpmc_a6 | gpmc_a5 | gpmc_a4 | | vdds_mem | vdds_mem | vdds_mem | vdd_mpu_iva | vdd_mpu_iva | vss | vss |
| K | | gpmc_a3 | gpmc_a2 | gpmc_a1 | gpmc_nbe0_cle | vdds_mem | vdds_mem | vdds_mem | | vss | vss | |
| L | gpmc_nbe1 | gpmc_d0 | | | | | | vss | | vss | vdd_mpu_iva | vdd_mpu_iva |
| M | gpmc_d1 | gpmc_d2 | gpmc_d4 | mcspi2_cs1 | mcspi2_cs0 | vdd_mpu_iva | vdd_mpu_iva | vdd_mpu_iva | vss | vss | vss | vdd_mpu_iva |

A.  Top Views are provided to assist in hardware debugging efforts.

**Figure 2-14. CUS Pin Map [Quadrant A - Top View]**

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Product Folder Link(s): DM3730  DM3725

| | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | sdrc_dqs1 | sdrc_d14 | | sdrc_dm3 | sdrc_dqs3 | | sdrc_ncs0 | sdrc_nwe | | cam_hs | uart3_cts_rctx | hdq_si0 | A |
| B | sdrc_dm1 | sdrc_d13 | sdrc_d15 | sdrc_d27 | sdrc_d30 | sdrc_d31 | sdrc_ncs1 | sdrc_cke0 | cam_d5 | cam_xclka | uart3_rts_sd | uart3_rx_irrx | B |
| C | sdrc_d12 | | sdrc_d26 | sdrc_d28 | | sdrc_ba0 | sdrc_ncas | sdrc_cke1 | | cam_xclkb | uart3_tx_irtx | | C |
| D | sdrc_d11 | | sdrc_d25 | sdrc_d29 | | sdrc_ba1 | sdrc_nras | | | | dss_data20 | dss_data6 | D |
| E | sdrc_d23 | | sdrc_d24 | vdds_mem | | cam_vs | | | | dss_hsync | dss_data7 | dss_data8 | E |
| F | vdd_core | | vdds_mem | vdds_mem | | cam_wen | cam_d3 | | cam_d10 | dss_vsync | dss_data9 | | F |
| G | vdd_core | | vdds_mem | vdds_mem | | vdda_dplls_dll | cam_d2 | cam_d4 | cam_d11 | dss_pclk | dss_data17 | dss_data18 | G |
| H | vdd_core | vss | vdds_mem | vss | cap_vdd_sram_core | | | | | | dss_data19 | cam_fld | H |
| J | vss | vss | vss | vss | vdd_core | vdd_core | cam_pclk | cam_strobe | dss_acbias | dss_data16 | cam_d8 | | J |
| K | | vss | vss | | vdd_core | vdd_core | vdd_core | i2c1_scl | i2c1_sda | dss_data21 | cam_d9 | cam_d7 | K |
| L | vss | vdd_core | vdd_core | | vss | | | | | | mmc1_cmd | cam_d6 | L |
| M | vss | vdd_core | vdd_core | vss | vdds | vdds | vdds | mmc1_dat2 | mmc1_dat1 | mmc1_dat0 | mmc1_clk | | M |

**Figure 2-15. CUS Pin Map [Quadrant B - Top View]**

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| N | | gpmc_d3 | mcspi2_somi | mcspi2_simo | mcspi2_clk | vdd_mpu_iva | vdd_mpu_iva | vdd_mpu_iva | vss | vss | vss | vss |
| P | gpmc_d5 | gpmc_d6 | | | | | vss | | | vss | vss | vss |
| R | gpmc_d7 | gpmc_d8 | gpmc_d11 | mcspi1_simo | mcbsp1_cs3 | vdd_mpu_iva | vdd_mpu_iva | vdd_mpu_iva | | vss | vss | |
| T | | gpmc_d9 | gpmc_d12 | mcspi1_somi | mcspi1_clk | mcspi1_cs0 | vdd_mpu_iva | vdd_mpu_iva | vss | vss | vss | vss |
| U | gpmc_d10 | gpmc_d13 | | | | | | cap_vdd_sram_mpu_iva | vss | vdds | vss | vdd_mpu_iva |
| V | gpmc_d14 | gpmc_d15 | mmc2_dat3 | mcbsp3_fsx | mcbsp3_dr | mcbsp3_dx | uart1_rx | | vdds | vdds | | vdd_mpu_iva |
| W | | gpmc_clk | mmc2_dat2 | mcbsp3_clkx | | uart1_rts | uart1_tx | | vdds | vdds | | vdd_mpu_iva |
| Y | mmc2_clk | mmc2_dat6 | mmc2_dat1 | | | | sys_clkout1 | | vdds | sys_nres warm | | cap_vddu_wkup_logic |
| AA | mmc2_dat7 | mmc2_dat5 | | | | sys_clkout2 | jtag_rtck | | jtag_tms_tmsc | sys_nres pwron | | vdds_sram |
| AB | | mmc2_dat4 | mmc2_dat0 | | mmc2_cmd | jtag_tck | jtag_ntrst | | jtag_tdo | jtag_tdi | | sys_boot0 |
| AC | etk_clk | uart1_cts | etk_d10 | etk_d8 | etk_d4 | etk_d1 | etk_d2 | etk_d6 | etk_d11 | etk_d12 | etk_d14 | i2c3_sda |
| AD | NC | etk_d5 | etk_ctl | | etk_d9 | etk_d0 | | etk_d3 | etk_d7 | | etk_d13 | etk_d15 |

**Figure 2-16. CUS Pin Map [Quadrant C - Top View]**

| | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | vss | vss | vss | vss | vdds | vdds | vdds | cap_vddu_array | cap_vdd_bb_mpu_iva | gpio_126 | mmc1_dat3 | vdds_mmc1 | N |
| | vss | vss | vss | | vss | | | | | | hsusb0_dir | gpio_129 | P |
| | | vss | vss | | vdd_core | vdd_core | vdd_core | mcbsp2_dx | hsusb0_clk | hsusb0_nxt | hsusb0_stp | | R |
| | vss | vss | vss | vss | vdd_core | vdd_core | vdd_core | vdd_core | mcbsp2_clkx | hsusb0_data7 | hsusb0_data1 | hsusb0_data0 | T |
| | vdd_mpu_iva | vss | vss | vss | vdda_dpll_per | | | | | | hsusb0_data3 | hsusb0_data2 | U |
| | vdd_mpu_iva | | vss | vss | | mcbsp1_clkx | mcbsp2_dr | mcbsp2_fsx | dss_data22 | dss_data15 | hsusb0_data5 | | V |
| | vdd_mpu_iva | | sys_xtalgnd | sys_nirq | | mcbsp1_dx | mcbsp1_clkr | | dss_data23 | dss_data14 | hsusb0_data6 | hsusb0_data4 | W |
| | sys_clkreq | | i2c4_sda | i2c4_scl | | mcbsp1_dr | | | | dss_data13 | cvideo2_vfb | cvideo1_rset | Y |
| | vdda_wkup_bg_bb | | sys_boot6 | sys_32k | | mcbsp_clks | mcbsp1_fsx | | | | cvideo2_out | | AA |
| | vdda_dac | | vssa_dac | sys_boot5 | | cam_d0 | dss_data1 | mcbsp1_fsr | | dss_data12 | cvideo1_vfb | cvideo1_out | AB |
| | i2c3_scl | i2c2_sda | i2c2_scl | sys_boot1 | sys_boot4 | cam_d1 | dss_data0 | dss_data3 | dss_data5 | dss_data10 | dss_data11 | jtag_emu0 | AC |
| | | sys_xtaout | sys_xtalin | | sys_boot2 | sys_boot3 | | dss_data2 | dss_data4 | | sys_off_mode | jtag_emu1 | AD |
| | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | |

**Figure 2-17. CUS Pin Map [Quadrant D - Top View]**

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Product Folder Link(s): DM3730  DM3725

## 2.3 Ball Characteristics

Table 2-1 through Table 2-3 describe the terminal characteristics and the signals multiplexed on each pin for the CBP, CBC, and CUS packages, respectively. The following list describes the table column headers.

1. **BALL BOTTOM:** Ball number(s) on the bottom side associated with each signal(s) on the bottom.
2. **PIN NAME:** Names of signals multiplexed on each ball (also notice that the name of the pin is the signal name in mode 0).
   **Note**: Table 2-3 does not take into account subsystem pin multiplexing options. Subsystem pin multiplexing options are described in Section 2.5, *Signal Descriptions.*
3. **MODE:** Multiplexing mode number.
   (a) Mode 0 is the primary mode; this means that when mode 0 is set, the function mapped on the pin corresponds to the name of the pin. There is always a function mapped on the primary mode. Notice that primary mode is not necessarily the default mode.

      **Note**: The default mode is the mode at the release of the reset; also see the RESET REL. MODE column.
   (b) Modes 1 to 7 are possible modes for alternate functions. On each pin, some modes are effectively used for alternate functions, while some modes are not used and do not correspond to a functional configuration.
4. **TYPE:** Signal direction
   – I = Input
   – O = Output
   – I/O = Input/Output
   – D = Open drain
   – DS = Differential
   – A = Analog
   – PWR = Power
   – GND = Ground

      **Note**: In the safe_mode, the buffer is configured in high-impedance.
5. **BALL RESET STATE:** The state of the terminal at the power-on reset.
   – 0: The buffer drives $V_{OL}$ (pulldown/pullup resistor not activated)
      0(PD): The buffer drives $V_{OL}$ with an active pulldown resistor.
   – 1: The buffer drives $V_{OH}$ (pulldown/pullup resistor not activated)
      1(PU): The buffer drives $V_{OH}$ with an active pullup resistor.
   – Z: High-impedance
   – L: High-impedance with an active pulldown resistor
   – H : High-impedance with an active pullup resistor
6. **BALL RESET REL. STATE:** The state of the terminal at the release of the System Control Module reset (PRCM CORE_RSTPWRON_RET reset signal).
   – 0: The buffer drives $V_{OL}$ (pulldown/pullup resistor not activated)
      0(PD): The buffer drives $V_{OL}$ with an active pulldown resistor.
   – 1: The buffer drives $V_{OH}$ (pulldown/pullup resistor not activated)
      1(PU): The buffer drives $V_{OH}$ with an active pullup resistor.
   – Z: High-impedance
   – L: High-impedance with an active pulldown resistor
   – H : High-impedance with an active pullup resistor
7. **RESET REL. MODE:** The mode is automatically configured at the release of the System Control Module reset (PRCM CORE_RSTPWRON_RET reset signal).
8. **POWER:** The voltage supply that powers the terminal's I/O buffers.
9. **HYS:** Indicates if the input buffer is with hysteresis.
10. **BUFFER STRENGTH:** Drive strength of the associated output buffer.

11. **PULL U/D - TYPE:** Denotes the presence of an internal pullup or pulldown resistor. Pullup and pulldown resistors can be enabled or disabled via software.
    **Note**: The pullup/pulldown drive strength is equal to minimum = 50µA, typical = 100 µA, maximum = 250 µA (unless otherwise specified), except for CBP balls P27, P26, R27, and R25, and CUS balls N22 and P24, where the pulldown drive strength is equal to 1.8 kΩ.

12. **IO CELL:** IO cell information.

    **Note**: Configuring two pins to the same input signal is not supported as it can yield unexpected results. This can be easily prevented with the proper software configuration.

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**NOTE**

In the DM3730/25 device, new Far End load Settings registers are added for some IOs. This new feature configures the IO according to the transmission line and the application/peripheral load. For a full description on these registers, see the System Control Module / SCM Functional Description / Functional Register Description / Signal Integrity Parameter Control Registers with Pad Group Assignment section of the *AM/DM37x Multimedia Device Technical Reference Manual* (literature number SPRUGN4).

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### Table 2-1. Ball Characteristics (CBP Pkg.)[(3)]

| BALL BOTTOM [1] | BALL TOP [1] | PIN NAME [2] | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | POWER [8] | HYS [9] | BUFFER STRENGTH (mA) [10] | PULLUP /DOWN TYPE [11] | IO CELL [12] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| NA | J2 | sdrc_d0 | 0 | IO | L | Z | 0 | vdds_mem | Yes | 4 [(12)] | PU/ PD | LVCMOS |
| NA | J1 | sdrc_d1 | 0 | IO | L | Z | 0 | vdds_mem | Yes | 4 [(12)] | PU/ PD | LVCMOS |
| NA | G2 | sdrc_d2 | 0 | IO | L | Z | 0 | vdds_mem | Yes | 4 [(12)] | PU/ PD | LVCMOS |
| NA | G1 | sdrc_d3 | 0 | IO | L | Z | 0 | vdds_mem | Yes | 4 [(12)] | PU/ PD | LVCMOS |
| NA | F2 | sdrc_d4 | 0 | IO | L | Z | 0 | vdds_mem | Yes | 4 [(12)] | PU/ PD | LVCMOS |
| NA | F1 | sdrc_d5 | 0 | IO | L | Z | 0 | vdds_mem | Yes | 4 [(12)] | PU/ PD | LVCMOS |
| NA | D2 | sdrc_d6 | 0 | IO | L | Z | 0 | vdds_mem | Yes | 4 [(12)] | PU/ PD | LVCMOS |
| NA | D1 | sdrc_d7 | 0 | IO | L | Z | 0 | vdds_mem | Yes | 4 [(12)] | PU/ PD | LVCMOS |
| NA | B13 | sdrc_d8 | 0 | IO | L | Z | 0 | vdds_mem | Yes | 4 [(12)] | PU/ PD | LVCMOS |
| NA | A13 | sdrc_d9 | 0 | IO | L | Z | 0 | vdds_mem | Yes | 4 [(12)] | PU/ PD | LVCMOS |
| NA | B14 | sdrc_d10 | 0 | IO | L | Z | 0 | vdds_mem | Yes | 4 [(12)] | PU/ PD | LVCMOS |
| NA | A14 | sdrc_d11 | 0 | IO | L | Z | 0 | vdds_mem | Yes | 4 [(12)] | PU/ PD | LVCMOS |
| NA | B16 | sdrc_d12 | 0 | IO | L | Z | 0 | vdds_mem | Yes | 4 [(12)] | PU/ PD | LVCMOS |
| NA | A16 | sdrc_d13 | 0 | IO | L | Z | 0 | vdds_mem | Yes | 4 [(12)] | PU/ PD | LVCMOS |
| NA | B19 | sdrc_d14 | 0 | IO | L | Z | 0 | vdds_mem | Yes | 4 [(12)] | PU/ PD | LVCMOS |
| NA | A19 | sdrc_d15 | 0 | IO | L | Z | 0 | vdds_mem | Yes | 4 [(12)] | PU/ PD | LVCMOS |
| NA | B3 | sdrc_d16 | 0 | IO | L | Z | 0 | vdds_mem | Yes | 4 [(12)] | PU/ PD | LVCMOS |
| NA | A3 | sdrc_d17 | 0 | IO | L | Z | 0 | vdds_mem | Yes | 4 [(12)] | PU/ PD | LVCMOS |
| NA | B5 | sdrc_d18 | 0 | IO | L | Z | 0 | vdds_mem | Yes | 4 [(12)] | PU/ PD | LVCMOS |
| NA | A5 | sdrc_d19 | 0 | IO | L | Z | 0 | vdds_mem | Yes | 4 [(12)] | PU/ PD | LVCMOS |
| NA | B8 | sdrc_d20 | 0 | IO | L | Z | 0 | vdds_mem | Yes | 4 [(12)] | PU/ PD | LVCMOS |
| NA | A8 | sdrc_d21 | 0 | IO | L | Z | 0 | vdds_mem | Yes | 4 [(12)] | PU/ PD | LVCMOS |
| NA | B9 | sdrc_d22 | 0 | IO | L | Z | 0 | vdds_mem | Yes | 4 [(12)] | PU/ PD | LVCMOS |
| NA | A9 | sdrc_d23 | 0 | IO | L | Z | 0 | vdds_mem | Yes | 4 [(12)] | PU/ PD | LVCMOS |
| NA | B21 | sdrc_d24 | 0 | IO | L | Z | 0 | vdds_mem | Yes | 4 [(12)] | PU/ PD | LVCMOS |
| NA | A21 | sdrc_d25 | 0 | IO | L | Z | 0 | vdds_mem | Yes | 4 [(12)] | PU/ PD | LVCMOS |
| NA | D22 | sdrc_d26 | 0 | IO | L | Z | 0 | vdds_mem | Yes | 4 [(12)] | PU/ PD | LVCMOS |
| NA | D23 | sdrc_d27 | 0 | IO | L | Z | 0 | vdds_mem | Yes | 4 [(12)] | PU/ PD | LVCMOS |
| NA | E22 | sdrc_d28 | 0 | IO | L | Z | 0 | vdds_mem | Yes | 4 [(12)] | PU/ PD | LVCMOS |
| NA | E23 | sdrc_d29 | 0 | IO | L | Z | 0 | vdds_mem | Yes | 4 [(12)] | PU/ PD | LVCMOS |
| NA | G22 | sdrc_d30 | 0 | IO | L | Z | 0 | vdds_mem | Yes | 4 [(12)] | PU/ PD | LVCMOS |
| NA | G23 | sdrc_d31 | 0 | IO | L | Z | 0 | vdds_mem | Yes | 4 [(12)] | PU/ PD | LVCMOS |
| NA | AB21 | sdrc_ba0 | 0 | O | 0 | 0 | 0 | vdds_mem | No | 4 [(12)] | NA | LVCMOS |
| NA | AC21 | sdrc_ba1 | 0 | O | 0 | 0 | 0 | vdds_mem | No | 4 [(12)] | NA | LVCMOS |

## Table 2-1. Ball Characteristics (CBP Pkg.)[3]  (continued)

| BALL BOTTOM [1] | BALL TOP [1] | PIN NAME [2] | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | POWER [8] | HYS [9] | BUFFER STRENGTH (mA) [10] | PULLUP /DOWN TYPE [11] | IO CELL [12] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| NA | N22 | sdrc_a0 | 0 | O | 0 | 0 | 0 | vdds_mem | No | 4 (12) | NA | LVCMOS |
| NA | N23 | sdrc_a1 | 0 | O | 0 | 0 | 0 | vdds_mem | No | 4 (12) | NA | LVCMOS |
| NA | P22 | sdrc_a2 | 0 | O | 0 | 0 | 0 | vdds_mem | No | 4 (12) | NA | LVCMOS |
| NA | P23 | sdrc_a3 | 0 | O | 0 | 0 | 0 | vdds_mem | No | 4 (12) | NA | LVCMOS |
| NA | R22 | sdrc_a4 | 0 | O | 0 | 0 | 0 | vdds_mem | No | 4 (12) | NA | LVCMOS |
| NA | R23 | sdrc_a5 | 0 | O | 0 | 0 | 0 | vdds_mem | No | 4 (12) | NA | LVCMOS |
| NA | T22 | sdrc_a6 | 0 | O | 0 | 0 | 0 | vdds_mem | No | 4 (12) | NA | LVCMOS |
| NA | T23 | sdrc_a7 | 0 | O | 0 | 0 | 0 | vdds_mem | No | 4 (12) | NA | LVCMOS |
| NA | U22 | sdrc_a8 | 0 | O | 0 | 0 | 0 | vdds_mem | No | 4 (12) | NA | LVCMOS |
| NA | U23 | sdrc_a9 | 0 | O | 0 | 0 | 0 | vdds_mem | No | 4 (12) | NA | LVCMOS |
| NA | V22 | sdrc_a10 | 0 | O | 0 | 0 | 0 | vdds_mem | No | 4 (12) | NA | LVCMOS |
| NA | V23 | sdrc_a11 | 0 | O | 0 | 0 | 0 | vdds_mem | No | 4 (12) | NA | LVCMOS |
| NA | W22 | sdrc_a12 | 0 | O | 0 | 0 | 0 | vdds_mem | No | 4 (12) | NA | LVCMOS |
| NA | W23 | sdrc_a13 | 0 | O | 0 | 0 | 0 | vdds_mem | No | 4 (12) | NA | LVCMOS |
| NA | Y22 | sdrc_a14 | 0 | O | 0 | 0 | 0 | vdds_mem | No | 4 (12) | NA | LVCMOS |
| NA | M22 | sdrc_ncs0 | 0 | O | 1 | 1 | 0 | vdds_mem | No | 4 (12) | NA | LVCMOS |
| NA | M23 | sdrc_ncs1 | 0 | O | 1 | 1 | 0 | vdds_mem | No | 4 (12) | NA | LVCMOS |
| NA | A11 | sdrc_clk | 0 | IO | L | 0 | 0 | vdds_mem | Yes | 4 (12) | PU/ PD | LVCMOS |
| NA | B11 | sdrc_nclk | 0 | O | 1 | 1 | 0 | vdds_mem | No | 4 (12) | NA | LVCMOS |
| NA | J22 | sdrc_cke0 | 0 | O | H | 1 | 7 | vdds_mem | Yes | 4 (12) | PU/ PD | LVCMOS |
| | | safe_mode_out1[13] | 7 | | | | | | | | | |
| NA | J23 | sdrc_cke1 | 0 | O | H | 1 | 7 | vdds_mem | NA | 4 (12) | PU/ PD | LVCMOS |
| | | safe_mode_out1[13] | 7 | | | | | | | | | |
| NA | L23 | sdrc_nras | 0 | O | 1 | 1 | 0 | vdds_mem | No | 4 (12) | NA | LVCMOS |
| NA | L22 | sdrc_ncas | 0 | O | 1 | 1 | 0 | vdds_mem | No | 4 (12) | NA | LVCMOS |
| NA | K23 | sdrc_nwe | 0 | O | 1 | 1 | 0 | vdds_mem | No | 4 (12) | NA | LVCMOS |
| NA | C1 | sdrc_dm0 | 0 | O | 0 | 0 | 0 | vdds_mem | No | 4 (12) | NA | LVCMOS |
| NA | A17 | sdrc_dm1 | 0 | O | 0 | 0 | 0 | vdds_mem | No | 4 (12) | NA | LVCMOS |
| NA | A6 | sdrc_dm2 | 0 | O | 0 | 0 | 0 | vdds_mem | No | 4 (12) | NA | LVCMOS |
| NA | A20 | sdrc_dm3 | 0 | O | 0 | 0 | 0 | vdds_mem | No | 4 (12) | NA | LVCMOS |
| NA | C2 | sdrc_dqs0 | 0 | IO | L | Z | 0 | vdds_mem | Yes | 4 (12) | PU/ PD | LVCMOS |
| NA | B17 | sdrc_dqs1 | 0 | IO | L | Z | 0 | vdds_mem | Yes | 4 (12) | PU/ PD | LVCMOS |
| NA | B6 | sdrc_dqs2 | 0 | IO | L | Z | 0 | vdds_mem | Yes | 4 (12) | PU/ PD | LVCMOS |
| NA | B20 | sdrc_dqs3 | 0 | IO | L | Z | 0 | vdds_mem | Yes | 4 (12) | PU/ PD | LVCMOS |
| N4 | AC15 | gpmc_a1 | 0 | O | L | L | 7 | vdds_mem | Yes | 8 | PU/ PD | LVCMOS |
| | | gpio_34 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | | | | | | | | | |
| M4 | AB15 | gpmc_a2 | 0 | O | L | L | 7 | vdds_mem | Yes | 8 | PU/ PD | LVCMOS |
| | | gpio_35 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | | | | | | | | | |
| L4 | AC16 | gpmc_a3 | 0 | O | L | L | 7 | vdds_mem | Yes | 8 | PU/ PD | LVCMOS |
| | | gpio_36 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | | | | | | | | | |
| K4 | AB16 | gpmc_a4 | 0 | O | L | L | 7 | vdds_mem | Yes | 8 | PU/ PD | LVCMOS |
| | | gpio_37 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | | | | | | | | | |
| T3 | AC17 | gpmc_a5 | 0 | O | L | L | 7 | vdds_mem | Yes | 8 | PU/ PD | LVCMOS |
| | | gpio_38 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | | | | | | | | | |
| R3 | AB17 | gpmc_a6 | 0 | O | H | H | 7 | vdds_mem | Yes | 8 | PU/ PD | LVCMOS |
| | | gpio_39 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | | | | | | | | | |

## Table 2-1. Ball Characteristics (CBP Pkg.)(3)  (continued)

| BALL BOTTOM [1] | BALL TOP [1] | PIN NAME [2] | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | POWER [8] | HYS [9] | BUFFER STRENGTH (mA) [10] | PULLUP /DOWN TYPE [11] | IO CELL [12] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| N3 | AC18 | gpmc_a7 | 0 | O | H | H | 7 | vdds_mem | Yes | 8 | PU/ PD | LVCMOS |
|  |  | gpio_40 | 4 | IO |  |  |  |  |  |  |  |  |
|  |  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| M3 | AB18 | gpmc_a8 | 0 | O | H | H | 7 | vdds_mem | Yes | 8 | PU/ PD | LVCMOS |
|  |  | gpio_41 | 4 | IO |  |  |  |  |  |  |  |  |
|  |  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| L3 | AC19 | gpmc_a9 | 0 | O | H | H | 7 | vdds_mem | Yes | 8 | PU/ PD | LVCMOS |
|  |  | sys_ndmareq2 | 1 | I |  |  |  |  |  |  |  |  |
|  |  | gpio_42 | 4 | IO |  |  |  |  |  |  |  |  |
|  |  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| K3 | AB19 | gpmc_a10 | 0 | O | H | H | 7 | vdds_mem | Yes | 8 | PU/ PD | LVCMOS |
|  |  | sys_ndmareq3 | 1 | I |  |  |  |  |  |  |  |  |
|  |  | gpio_43 | 4 | IO |  |  |  |  |  |  |  |  |
|  |  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| NA | AC20 | gpmc_a11 | 0 | O | L | L | 7 | vdds_mem | Yes | 8 | PU/ PD | LVCMOS |
|  |  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| K1 | M2 | gpmc_d0 | 0 | IO | H | H | 0 | vdds_mem | Yes | 8 | PU/ PD | LVCMOS |
| L1 | M1 | gpmc_d1 | 0 | IO | H | H | 0 | vdds_mem | Yes | 8 | PU/ PD | LVCMOS |
| L2 | N2 | gpmc_d2 | 0 | IO | H | H | 0 | vdds_mem | Yes | 8 | PU/ PD | LVCMOS |
| P2 | N1 | gpmc_d3 | 0 | IO | H | H | 0 | vdds_mem | Yes | 8 | PU/ PD | LVCMOS |
| T1 | R2 | gpmc_d4 | 0 | IO | H | H | 0 | vdds_mem | Yes | 8 | PU/ PD | LVCMOS |
| V1 | R1 | gpmc_d5 | 0 | IO | H | H | 0 | vdds_mem | Yes | 8 | PU/ PD | LVCMOS |
| V2 | T2 | gpmc_d6 | 0 | IO | H | H | 0 | vdds_mem | Yes | 8 | PU/ PD | LVCMOS |
| W2 | T1 | gpmc_d7 | 0 | IO | H | H | 0 | vdds_mem | Yes | 8 | PU/ PD | LVCMOS |
| H2 | AB3 | gpmc_d8 | 0 | IO | H | H | 0 | vdds_mem | Yes | 8 | PU/ PD | LVCMOS |
|  |  | gpio_44 | 4 | IO |  |  |  |  |  |  |  |  |
|  |  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| K2 | AC3 | gpmc_d9 | 0 | IO | H | H | 0 | vdds_mem | Yes | 8 | PU/ PD | LVCMOS |
|  |  | gpio_45 | 4 | IO |  |  |  |  |  |  |  |  |
|  |  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| P1 | AB4 | gpmc_d10 | 0 | IO | H | H | 0 | vdds_mem | Yes | 8 | PU/ PD | LVCMOS |
|  |  | gpio_46 | 4 | IO |  |  |  |  |  |  |  |  |
|  |  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| R1 | AC4 | gpmc_d11 | 0 | IO | H | H | 0 | vdds_mem | Yes | 8 | PU/ PD | LVCMOS |
|  |  | gpio_47 | 4 | IO |  |  |  |  |  |  |  |  |
|  |  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| R2 | AB6 | gpmc_d12 | 0 | IO | H | H | 0 | vdds_mem | Yes | 8 | PU/ PD | LVCMOS |
|  |  | gpio_48 | 4 | IO |  |  |  |  |  |  |  |  |
|  |  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| T2 | AC6 | gpmc_d13 | 0 | IO | H | H | 0 | vdds_mem | Yes | 8 | PU/ PD | LVCMOS |
|  |  | gpio_49 | 4 | IO |  |  |  |  |  |  |  |  |
|  |  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| W1 | AB7 | gpmc_d14 | 0 | IO | H | H | 0 | vdds_mem | Yes | 8 | PU/ PD | LVCMOS |
|  |  | gpio_50 | 4 | IO |  |  |  |  |  |  |  |  |
|  |  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| Y1 | AC7 | gpmc_d15 | 0 | IO | H | H | 0 | vdds_mem | Yes | 8 | PU/ PD | LVCMOS |
|  |  | gpio_51 | 4 | IO |  |  |  |  |  |  |  |  |
|  |  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| G4 | Y2 | gpmc_ncs0 | 0 | O | 1 | 1 | 0 | vdds_mem | NA | 8 | NA | LVCMOS |
| H3 | Y1 | gpmc_ncs1 | 0 | O | H | 1 | 0 | vdds_mem | Yes | 8 | PU/ PD | LVCMOS |
|  |  | gpio_52 | 4 | IO |  |  |  |  |  |  |  |  |
|  |  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |

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## Table 2-1. Ball Characteristics (CBP Pkg.)[3]  (continued)

| BALL BOTTOM [1] | BALL TOP [1] | PIN NAME [2] | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | POWER [8] | HYS [9] | BUFFER STRENGTH (mA) [10] | PULLUP /DOWN TYPE [11] | IO CELL [12] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| V8 | NA | gpmc_ncs2 | 0 | O | H | H | 7 | vdds_mem | Yes | 8 | PU/ PD | LVCMOS |
|  |  | gpio_53 | 4 | IO |  |  |  |  |  |  |  |  |
|  |  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| U8 | NA | gpmc_ncs3 | 0 | O | H | H | 7 | vdds_mem | Yes | 8 | PU/ PD | LVCMOS |
|  |  | sys_ndmareq0 | 1 | I |  |  |  |  |  |  |  |  |
|  |  | gpio_54 | 4 | IO |  |  |  |  |  |  |  |  |
|  |  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| T8 | NA | gpmc_ncs4 | 0 | O | H | H | 7 | vdds_mem | Yes | 8 | PU/ PD | LVCMOS |
|  |  | sys_ndmareq1 | 1 | I |  |  |  |  |  |  |  |  |
|  |  | mcbsp4_clkx | 2 | IO |  |  |  |  |  |  |  |  |
|  |  | gpt_9_pwm_evt | 3 | IO |  |  |  |  |  |  |  |  |
|  |  | gpio_55 | 4 | IO |  |  |  |  |  |  |  |  |
|  |  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| R8 | NA | gpmc_ncs5 | 0 | O | H | H | 7 | vdds_mem | Yes | 8 | PU/ PD | LVCMOS |
|  |  | sys_ndmareq2 | 1 | I |  |  |  |  |  |  |  |  |
|  |  | mcbsp4_dr | 2 | I |  |  |  |  |  |  |  |  |
|  |  | gpt_10_pwm_evt | 3 | IO |  |  |  |  |  |  |  |  |
|  |  | gpio_56 | 4 | IO |  |  |  |  |  |  |  |  |
|  |  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| P8 | NA | gpmc_ncs6 | 0 | O | H | H | 7 | vdds_mem | Yes | 8 | PU/ PD | LVCMOS |
|  |  | sys_ndmareq3 | 1 | I |  |  |  |  |  |  |  |  |
|  |  | mcbsp4_dx | 2 | IO |  |  |  |  |  |  |  |  |
|  |  | gpt_11_pwm_evt | 3 | IO |  |  |  |  |  |  |  |  |
|  |  | gpio_57 | 4 | IO |  |  |  |  |  |  |  |  |
|  |  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| N8 | NA | gpmc_ncs7 | 0 | O | H | H | 7 | vdds_mem | Yes | 8 | PU/ PD | LVCMOS |
|  |  | gpmc_io_dir | 1 | O |  |  |  |  |  |  |  |  |
|  |  | mcbsp4_fsx | 2 | IO |  |  |  |  |  |  |  |  |
|  |  | gpt_8_pwm_evt | 3 | IO |  |  |  |  |  |  |  |  |
|  |  | gpio_58 | 4 | IO |  |  |  |  |  |  |  |  |
|  |  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| T4 | W2 | gpmc_clk | 0 | O | L | 0 | 0 | vdds_mem | Yes | 8 | PU/ PD | LVCMOS |
|  |  | gpio_59 | 4 | IO |  |  |  |  |  |  |  |  |
|  |  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| F3 | W1 | gpmc_nadv_ale | 0 | O | 0 | 0 | 0 | vdds_mem | NA | 8 | PU/ PD | LVCMOS |
| G2 | V2 | gpmc_noe | 0 | O | 1 | 1 | 0 | vdds_mem | NA | 8 | PU/ PD | LVCMOS |
| F4 | V1 | gpmc_nwe | 0 | O | 1 | 1 | 0 | vdds_mem | NA | 8 | PU/ PD | LVCMOS |
| G3 | AC12 | gpmc_nbe0_cle | 0 | O | L | 0 | 0 | vdds_mem | Yes | 8 | PU/ PD | LVCMOS |
|  |  | gpio_60 | 4 | IO |  |  |  |  |  |  |  |  |
|  |  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| U3 | NA | gpmc_nbe1 | 0 | O | L | L | 7 | vdds_mem | Yes | 8 | PU/ PD | LVCMOS |
|  |  | gpio_61 | 4 | IO |  |  |  |  |  |  |  |  |
|  |  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| H1 | AB10 | gpmc_nwp | 0 | O | L | 0 | 0 | vdds_mem | Yes | 8 | PU/ PD | LVCMOS |
|  |  | gpio_62 | 4 | IO |  |  |  |  |  |  |  |  |
|  |  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| M8 | AB12 | gpmc_wait0 | 0 | I | H | H | 0 | vdds_mem | Yes | NA | PU/ PD | LVCMOS |
| L8 | AC10 | gpmc_wait1 | 0 | I | H | H | 7 | vdds_mem | Yes | 8 | PU/ PD | LVCMOS |
|  |  | gpio_63 | 4 | IO |  |  |  |  |  |  |  |  |
|  |  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| K8 | NA | gpmc_wait2 | 0 | I | H | H | 7 | vdds_mem | Yes | 8 | PU/ PD | LVCMOS |
|  |  | uart4_tx | 2 | O |  |  |  |  |  |  |  |  |
|  |  | gpio_64 | 4 | IO |  |  |  |  |  |  |  |  |
|  |  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |

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Product Folder Link(s): DM3730  DM3725

## Table 2-1. Ball Characteristics (CBP Pkg.)[3]  (continued)

| BALL BOTTOM [1] | BALL TOP [1] | PIN NAME [2] | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | POWER [8] | HYS [9] | BUFFER STRENGTH (mA) [10] | PULLUP /DOWN TYPE [11] | IO CELL [12] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| J8 | NA | gpmc_wait3 | 0 | I | H | H | 7 | vdds_mem | Yes | 8 | PU/ PD | LVCMOS |
| | | sys_ndmareq1 | 1 | I | | | | | | | | |
| | | uart4_rx | 2 | I | | | | | | | | |
| | | gpio_65 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | | | | | | | | | |
| D28 | NA | dss_pclk | 0 | O | H | H | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| | | gpio_66 | 4 | IO | | | | | | | | |
| | | hw_dbg12 | 5 | O | | | | | | | | |
| | | safe_mode | 7 | | | | | | | | | |
| D26 | NA | dss_hsync | 0 | O | H | H | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| | | gpio_67 | 4 | IO | | | | | | | | |
| | | hw_dbg13 | 5 | O | | | | | | | | |
| | | safe_mode | 7 | | | | | | | | | |
| D27 | NA | dss_vsync | 0 | O | H | H | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| | | gpio_68 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | | | | | | | | | |
| E27 | NA | dss_acbias | 0 | O | L | L | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| | | gpio_69 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | | | | | | | | | |
| AG22 | NA | dss_data0 | 0 | IO | L | L | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| | | uart1_cts | 2 | I | | | | | | NA | | |
| | | gpio_70 | 4 | IO | | | | | | 8 | | |
| | | safe_mode | 7 | | | | | | | 8 | | |
| AH22 | NA | dss_data1 | 0 | IO | L | L | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| | | uart1_rts | 2 | O | | | | | | 8 | | |
| | | gpio_71 | 4 | IO | | | | | | 8 | | |
| | | safe_mode | 7 | | | | | | | 8 | | |
| AG23 | NA | dss_data2 | 0 | IO | L | L | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| | | gpio_72 | 4 | IO | | | | | | 8 | | |
| | | safe_mode | 7 | | | | | | | 8 | | |
| AH23 | NA | dss_data3 | 0 | IO | L | L | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| | | gpio_73 | 4 | IO | | | | | | 8 | | |
| | | safe_mode | 7 | | | | | | | 8 | | |
| AG24 | NA | dss_data4 | 0 | IO | L | L | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| | | uart3_rx_irrx | 2 | I | | | | | | NA | | |
| | | gpio_74 | 4 | IO | | | | | | 8 | | |
| | | safe_mode | 7 | | | | | | | 8 | | |
| AH24 | NA | dss_data5 | 0 | IO | L | L | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| | | uart3_tx_irtx | 2 | O | | | | | | 8 | | |
| | | gpio_75 | 4 | IO | | | | | | 8 | | |
| | | safe_mode | 7 | | | | | | | 8 | | |
| E26 | NA | dss_data6 | 0 | IO | L | L | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| | | uart1_tx | 2 | O | | | | | | | | |
| | | gpio_76 | 4 | IO | | | | | | | | |
| | | hw_dbg14 | 5 | O | | | | | | | | |
| | | safe_mode | 7 | | | | | | | | | |
| F28 | NA | dss_data7 | 0 | IO | L | L | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| | | uart1_rx | 2 | I | | | | | | | | |
| | | gpio_77 | 4 | IO | | | | | | | | |
| | | hw_dbg15 | 5 | O | | | | | | | | |
| | | safe_mode | 7 | | | | | | | | | |

## Table 2-1. Ball Characteristics (CBP Pkg.)[3] (continued)

| BALL BOTTOM [1] | BALL TOP [1] | PIN NAME [2] | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | POWER [8] | HYS [9] | BUFFER STRENGTH (mA) [10] | PULLUP /DOWN TYPE [11] | IO CELL [12] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| F27 | NA | dss_data8 | 0 | IO | L | L | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
|  |  | uart3_rx_irrx | 2 | I |  |  |  |  |  |  |  |  |
|  |  | gpio_78 | 4 | IO |  |  |  |  |  |  |  |  |
|  |  | hw_dbg16 | 5 | O |  |  |  |  |  |  |  |  |
|  |  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| G26 | NA | dss_data9 | 0 | IO | L | L | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
|  |  | uart3_tx_irtx | 2 | O |  |  |  |  |  |  |  |  |
|  |  | gpio_79 | 4 | IO |  |  |  |  |  |  |  |  |
|  |  | hw_dbg17 | 5 | O |  |  |  |  |  |  |  |  |
|  |  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| AD28 | NA | dss_data10 | 0 | IO | L | L | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
|  |  | gpio_80 | 4 | IO |  |  |  |  |  |  |  |  |
|  |  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| AD27 | NA | dss_data11 | 0 | IO | L | L | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
|  |  | gpio_81 | 4 | IO |  |  |  |  |  |  |  |  |
|  |  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| AB28 | NA | dss_data12 | 0 | IO | L | L | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
|  |  | gpio_82 | 4 | IO |  |  |  |  |  |  |  |  |
|  |  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| AB27 | NA | dss_data13 | 0 | IO | L | L | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
|  |  | gpio_83 | 4 | IO |  |  |  |  |  |  |  |  |
|  |  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| AA28 | NA | dss_data14 | 0 | IO | L | L | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
|  |  | gpio_84 | 4 | IO |  |  |  |  |  |  |  |  |
|  |  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| AA27 | NA | dss_data15 | 0 | IO | L | L | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
|  |  | gpio_85 | 4 | IO |  |  |  |  |  |  |  |  |
|  |  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| G25 | NA | dss_data16 | 0 | IO | L | L | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
|  |  | gpio_86 | 4 | IO |  |  |  |  |  |  |  |  |
|  |  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| H27 | NA | dss_data17 | 0 | IO | L | L | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
|  |  | gpio_87 | 4 | IO |  |  |  |  |  |  |  |  |
|  |  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| H26 | NA | dss_data18 | 0 | IO | L | L | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
|  |  | mcspi3_clk | 2 | IO |  |  |  |  |  |  |  |  |
|  |  | dss_data0 | 3 | IO |  |  |  |  |  |  |  |  |
|  |  | gpio_88 | 4 | IO |  |  |  |  |  |  |  |  |
|  |  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| H25 | NA | dss_data19 | 0 | IO | L | L | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
|  |  | mcspi3_simo | 2 | IO |  |  |  |  |  |  |  |  |
|  |  | dss_data1 | 3 | IO |  |  |  |  |  |  |  |  |
|  |  | gpio_89 | 4 | IO |  |  |  |  |  |  |  |  |
|  |  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| E28 | NA | dss_data20 | 0 | O | H | H | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
|  |  | mcspi3_somi | 2 | IO |  |  |  |  |  |  |  |  |
|  |  | dss_data2 | 3 | IO |  |  |  |  |  |  |  |  |
|  |  | gpio_90 | 4 | IO |  |  |  |  |  |  |  |  |
|  |  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| J26 | NA | dss_data21 | 0 | O | L | L | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
|  |  | mcspi3_cs0 | 2 | IO |  |  |  |  |  |  |  |  |
|  |  | dss_data3 | 3 | IO |  |  |  |  |  |  |  |  |
|  |  | gpio_91 | 4 | IO |  |  |  |  |  |  |  |  |
|  |  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |

Product Folder Link(s): DM3730  DM3725

## Table 2-1. Ball Characteristics (CBP Pkg.)[3] (continued)

| BALL BOTTOM [1] | BALL TOP [1] | PIN NAME [2] | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | POWER [8] | HYS [9] | BUFFER STRENGTH (mA) [10] | PULLUP /DOWN TYPE [11] | IO CELL [12] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| AC27 | NA | dss_data22 | 0 | O | L | L | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| | | mcspi3_cs1 | 2 | O | | | | | | | | |
| | | dss_data4 | 3 | IO | | | | | | | | |
| | | gpio_92 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | | | | | | | | | |
| AC28 | NA | dss_data23 | 0 | O | L | L | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| | | dss_data5 | 3 | IO | | | | | | | | |
| | | gpio_93 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | | | | | | | | | |
| W28 | NA | cvideo2_out | 0 | AO | 0 | 0 | 0 | vdda_dac | NA | NA(4) | NA | 10-bit DAC |
| Y28 | NA | cvideo1_out | 0 | AO | 0 | 0 | 0 | vdda_dac | NA | NA(4) | NA | 10-bit DAC |
| Y27 | NA | cvideo1_vfb | 0 | AO | 0 | NA | 0 | vdda_dac | NA | NA(10) | NA | 10-bit DAC |
| W27 | NA | cvideo2_vfb | 0 | AO | 0 | NA | 0 | vdda_dac | NA | NA(10) | NA | 10-bit DAC |
| W26 | NA | cvideo1_rset | 0 | AIO | 0 | NA | 0 | vdda_dac | No | NA | NA | 10-bit DAC |
| A24 | NA | cam_hs | 0 | IO | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | gpio_94 | 4 | IO | | | | | | | | |
| | | hw_dbg0 | 5 | O | | | | | | | | |
| | | safe_mode | 7 | | | | | | | | | |
| A23 | NA | cam_vs | 0 | IO | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | gpio_95 | 4 | IO | | | | | | | | |
| | | hw_dbg1 | 5 | O | | | | | | | | |
| | | safe_mode | 7 | | | | | | | | | |
| C25 | NA | cam_xclka | 0 | O | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | gpio_96 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | | | | | | | | | |
| C27 | NA | cam_pclk | 0 | I | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | gpio_97 | 4 | IO | | | | | | | | |
| | | hw_dbg2 | 5 | O | | | | | | | | |
| | | safe_mode | 7 | | | | | | | | | |
| C23 | NA | cam_fld | 0 | IO | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | cam_global_reset | 2 | IO | | | | | | | | |
| | | gpio_98 | 4 | IO | | | | | | | | |
| | | hw_dbg3 | 5 | O | | | | | | | | |
| | | safe_mode | 7 | | | | | | | | | |
| AG17 | NA | cam_d0 | 0 | I | L | L | 7 | vdds | Yes | NA | PU/PD | LVCMOS |
| | | gpio_99 | 4 | I | | | | | | | | |
| | | safe_mode | 7 | | | | | | | | | |
| AH17 | NA | cam_d1 | 0 | I | L | L | 7 | vdds | Yes | NA | PU/PD | LVCMOS |
| | | gpio_100 | 4 | I | | | | | | | | |
| | | safe_mode | 7 | | | | | | | | | |
| B24 | NA | cam_d2 | 0 | I | L | L | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| | | gpio_101 | 4 | IO | | | | | | | | |
| | | hw_dbg4 | 5 | O | | | | | | | | |
| | | safe_mode | 7 | | | | | | | | | |
| C24 | NA | cam_d3 | 0 | I | L | L | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| | | gpio_102 | 4 | IO | | | | | | | | |
| | | hw_dbg5 | 5 | O | | | | | | | | |
| | | safe_mode | 7 | | | | | | | | | |
| D24 | NA | cam_d4 | 0 | I | L | L | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| | | gpio_103 | 4 | IO | | | | | | | | |
| | | hw_dbg6 | 5 | O | | | | | | | | |
| | | safe_mode | 7 | | | | | | | | | |
| A25 | NA | cam_d5 | 0 | I | L | L | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| | | gpio_104 | 4 | IO | | | | | | | | |

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## Table 2-1. Ball Characteristics (CBP Pkg.)[3] (continued)

| BALL BOTTOM [1] | BALL TOP [1] | PIN NAME [2] | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | POWER [8] | HYS [9] | BUFFER STRENGTH (mA) [10] | PULLUP /DOWN TYPE [11] | IO CELL [12] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | hw_dbg7 | 5 | O | | | | | | | | |
| | | safe_mode | 7 | | | | | | | | | |
| K28 | NA | cam_d6 | 0 | I | L | L | 7 | vdds | Yes | NA | PU/ PD | LVCMOS |
| | | gpio_105 | 4 | I | | | | | | | | |
| | | safe_mode | 7 | | | | | | | | | |
| L28 | NA | cam_d7 | 0 | I | L | L | 7 | vdds | Yes | NA | PU/ PD | LVCMOS |
| | | gpio_106 | 4 | I | | | | | | | | |
| | | safe_mode | 7 | | | | | | | | | |
| K27 | NA | cam_d8 | 0 | I | L | L | 7 | vdds | Yes | NA | PU/ PD | LVCMOS |
| | | gpio_107 | 4 | I | | | | | | | | |
| | | safe_mode | 7 | | | | | | | | | |
| L27 | NA | cam_d9 | 0 | I | L | L | 7 | vdds | Yes | NA | PU/ PD | LVCMOS |
| | | gpio_108 | 4 | I | | | | | | | | |
| | | safe_mode | 7 | | | | | | | | | |
| B25 | NA | cam_d10 | 0 | I | L | L | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| | | gpio_109 | 4 | IO | | | | | | | | |
| | | hw_dbg8 | 5 | O | | | | | | | | |
| | | safe_mode | 7 | | | | | | | | | |
| C26 | NA | cam_d11 | 0 | I | L | L | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| | | gpio_110 | 4 | IO | | | | | | | | |
| | | hw_dbg9 | 5 | O | | | | | | | | |
| | | safe_mode | 7 | | | | | | | | | |
| B26 | NA | cam_xclkb | 0 | O | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | gpio_111 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | | | | | | | | | |
| B23 | NA | cam_wen | 0 | I | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | cam_shutter | 2 | O | | | | | | | | |
| | | gpio_167 | 4 | IO | | | | | | | | |
| | | hw_dbg10 | 5 | O | | | | | | | | |
| | | safe_mode | 7 | | | | | | | | | |
| D25 | NA | cam_strobe | 0 | O | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | gpio_126 | 4 | IO | | | | | | | | |
| | | hw_dbg11 | 5 | O | | | | | | | | |
| | | safe_mode | 7 | | | | | | | | | |
| AG19 | NA | gpio_112 | 4 | I | L | L | 7 | vdds | Yes | NA | PU/PD | LVCMOS |
| | | safe_mode | 7 | | | | | | | | | |
| AH19 | NA | gpio_113 | 4 | I | L | L | 7 | vdds | Yes | NA | PU/PD | LVCMOS |
| | | safe_mode | 7 | | | | | | | | | |
| AG18 | NA | gpio_114 | 4 | I | L | L | 7 | vdds | Yes | NA | PU/PD | LVCMOS |
| | | safe_mode | 7 | - | | | | | | | | |
| AH18 | NA | gpio_115 | 4 | I | L | L | 7 | vdds | Yes | NA | PU/PD | LVCMOS |
| | | safe_mode | 7 | - | | | | | | | | |
| P21 | NA | mcbsp2_fsx | 0 | IO | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | gpio_116 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | | | | | | | | | |
| N21 | NA | mcbsp2_clkx | 0 | IO | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | gpio_117 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | | | | | | | | | |
| R21 | NA | mcbsp2_dr | 0 | I | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | gpio_118 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | | | | | | | | | |
| M21 | NA | mcbsp2_dx | 0 | IO | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | gpio_119 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | | | | | | | | | |

## Table 2-1. Ball Characteristics (CBP Pkg.)[3]  (continued)

| BALL BOTTOM [1] | BALL TOP [1] | PIN NAME [2] | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | POWER [8] | HYS [9] | BUFFER STRENGTH (mA) [10] | PULLUP /DOWN TYPE [11] | IO CELL [12] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| N28 | NA | mmc1_clk | 0 | O | L | L | 7 | vdds_mmc1(15) | Yes | 1 | PU/ PD[5] | LVCMOS |
|  |  | gpio_120 [1] | 4 | IO |  |  |  |  |  |  |  |  |
|  |  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| M27 | NA | mmc1_cmd | 0 | IO | L | L | 7 | vdds_mmc1(15) | Yes | 1 | PU/ PD[5] | LVCMOS |
|  |  | gpio_121 [1] | 4 | IO |  |  |  |  |  |  |  |  |
|  |  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| N27 | NA | mmc1_dat0 | 0 | IO | L | L | 7 | vdds_mmc1(15) | Yes | 1 | PU/ PD [5] | LVCMOS |
|  |  | gpio_122 [1] | 4 | IO |  |  |  |  |  |  |  |  |
|  |  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| N26 | NA | mmc1_dat1 | 0 | IO | L | L | 7 | vdds_mmc1(15) | Yes | 1 | PU/ PD[5] | LVCMOS |
|  |  | gpio_123[1] | 4 | IO |  |  |  |  |  |  |  |  |
|  |  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| N25 | NA | mmc1_dat2 | 0 | IO | L | L | 7 | vdds_mmc1(15) | Yes | 1 | PU/ PD [5] | LVCMOS |
|  |  | gpio_124[1] | 4 | IO |  |  |  |  |  |  |  |  |
|  |  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| P28 | NA | mmc1_dat3 | 0 | IO | L | L | 7 | vdds_mmc1(15) | Yes | 1 | PU/ PD [5] | LVCMOS |
|  |  | gpio_125[1] | 4 | IO |  |  |  |  |  |  |  |  |
|  |  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| P27 | NA | gpio_126[1] | 4 | IO | L | L | 7 | vdds_x | Yes | 1 | PU/ PD [5] | LVCMOS |
|  |  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| P26 | NA | gpio_127[1] | 4 | IO | L | L | 7 | vdds_x | Yes | 1 | PU/ PD[5] | LVCMOS |
|  |  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| R27 | NA | gpio_128 | 4 | IO | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
|  |  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| R25 | NA | gpio_129[1] | 4 | IO | L | L | 7 | vdds_x | Yes | 1 | PU/ PD[5] | LVCMOS |
|  |  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| AE2 | NA | mmc2_clk | 0 | O | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
|  |  | mcspi3_clk | 1 | IO |  |  |  |  |  |  |  |  |
|  |  | gpio_130 | 4 | IO |  |  |  |  |  |  |  |  |
|  |  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| AG5 | NA | mmc2_cmd | 0 | IO | H | H | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
|  |  | mcspi3_simo | 1 | IO |  |  |  |  |  |  |  |  |
|  |  | gpio_131 | 4 | IO |  |  |  |  |  |  |  |  |
|  |  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| AH5 | NA | mmc2_dat0 | 0 | IO | H | H | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
|  |  | mcspi3_somi | 1 | IO |  |  |  |  |  |  |  |  |
|  |  | gpio_132 | 4 | IO |  |  |  |  |  |  |  |  |
|  |  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| AH4 | NA | mmc2_dat1 | 0 | IO | H | H | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
|  |  | gpio_133 | 4 | IO |  |  |  |  |  |  |  |  |
|  |  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| AG4 | NA | mmc2_dat2 | 0 | IO | H | H | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
|  |  | mcspi3_cs1 | 1 | O |  |  |  |  |  |  |  |  |
|  |  | gpio_134 | 4 | IO |  |  |  |  |  |  |  |  |
|  |  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| AF4 | NA | mmc2_dat3 | 0 | IO | H | H | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
|  |  | mcspi3_cs0 | 1 | IO |  |  |  |  |  |  |  |  |
|  |  | gpio_135 | 4 | IO |  |  |  |  |  |  |  |  |
|  |  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| AE4 | NA | mmc2_dat4 | 0 | IO | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |

## Table 2-1. Ball Characteristics (CBP Pkg.)[3]  (continued)

| BALL BOTTOM [1] | BALL TOP [1] | PIN NAME [2] | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | POWER [8] | HYS [9] | BUFFER STRENGTH (mA) [10] | PULLUP /DOWN TYPE [11] | IO CELL [12] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | mmc2_dir_dat0 | 1 | O | | | | | | | | |
| | | mmc3_dat0 | 3 | IO | | | | | | | | |
| | | gpio_136 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | | | | | | | | | |
| AH3 | NA | mmc2_dat5 | 0 | IO | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | mmc2_dir_dat1 | 1 | O | | | | | | | | |
| | | cam_global_reset | 2 | IO | | | | | | | | |
| | | mmc3_dat1 | 3 | IO | | | | | | | | |
| | | gpio_137 | 4 | IO | | | | | | | | |
| | | mm3_rxdp | 6 | IO | | | | | | | | |
| | | safe_mode | 7 | | | | | | | | | |
| AF3 | NA | mmc2_dat6 | 0 | IO | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | mmc2_dir_cmd | 1 | O | | | | | | | | |
| | | cam_shutter | 2 | O | | | | | | | | |
| | | mmc3_dat2 | 3 | IO | | | | | | | | |
| | | gpio_138 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | | | | | | | | | |
| AE3 | NA | mmc2_dat7 | 0 | IO | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | mmc2_clkin | 1 | I | | | | | | | | |
| | | mmc3_dat3 | 3 | IO | | | | | | | | |
| | | gpio_139 | 4 | IO | | | | | | | | |
| | | mm3_rxdm | 6 | IO | | | | | | | | |
| | | safe_mode | 7 | | | | | | | | | |
| AF6 | NA | mcbsp3_dx | 0 | IO | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | uart2_cts | 1 | I | | | | | | | | |
| | | gpio_140 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | | | | | | | | | |
| AE6 | NA | mcbsp3_dr | 0 | I | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | uart2_rts | 1 | O | | | | | | | | |
| | | gpio_141 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | | | | | | | | | |
| AF5 | NA | mcbsp3_clkx | 0 | IO | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | uart2_tx | 1 | O | | | | | | | | |
| | | gpio_142 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | | | | | | | | | |
| AE5 | NA | mcbsp3_fsx | 0 | IO | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | uart2_rx | 1 | I | | | | | | | | |
| | | gpio_143 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | | | | | | | | | |
| AB26 | NA | uart2_cts | 0 | I | H | H | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | mcbsp3_dx | 1 | IO | | | | | | | | |
| | | gpt_9_pwm_evt | 2 | IO | | | | | | | | |
| | | gpio_144 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | | | | | | | | | |
| AB25 | NA | uart2_rts | 0 | O | H | H | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | mcbsp3_dr | 1 | I | | | | | | | | |
| | | gpt_10_pwm_evt | 2 | IO | | | | | | | | |
| | | gpio_145 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | | | | | | | | | |
| AA25 | NA | uart2_tx | 0 | O | H | H | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | mcbsp3_clkx | 1 | IO | | | | | | | | |
| | | gpt_11_pwm_evt | 2 | IO | | | | | | | | |
| | | gpio_146 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | | | | | | | | | |

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## Table 2-1. Ball Characteristics (CBP Pkg.)[3]  (continued)

| BALL BOTTOM [1] | BALL TOP [1] | PIN NAME [2] | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | POWER [8] | HYS [9] | BUFFER STRENGTH (mA) [10] | PULLUP /DOWN TYPE [11] | IO CELL [12] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| AD25 | NA | uart2_rx | 0 | I | H | H | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | mcbsp3_fsx | 1 | IO | | | | | | | | |
| | | gpt_8_pwm_evt | 2 | IO | | | | | | | | |
| | | gpio_147 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | | | | | | | | | |
| AA8 | NA | uart1_tx | 0 | O | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | gpio_148 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | | | | | | | | | |
| AA9 | NA | uart1_rts | 0 | O | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | gpio_149 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | | | | | | | | | |
| W8 | NA | uart1_cts | 0 | I | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | gpio_150 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | | | | | | | | | |
| Y8 | NA | uart1_rx | 0 | I | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | mcbsp1_clkr | 2 | IO | | | | | | | | |
| | | mcspi4_clk | 3 | IO | | | | | | | | |
| | | gpio_151 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | | | | | | | | | |
| AE1 | NA | mcbsp4_clkx | 0 | IO | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | gpio_152 | 4 | IO | | | | | | | | |
| | | mm3_txse0 | 6 | IO | | | | | | | | |
| | | safe_mode | 7 | | | | | | | | | |
| AD1 | NA | mcbsp4_dr | 0 | I | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | gpio_153 | 4 | IO | | | | | | | | |
| | | mm3_rxrcv | 6 | IO | | | | | | | | |
| | | safe_mode | 7 | | | | | | | | | |
| AD2 | NA | mcbsp4_dx | 0 | IO | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | gpio_154 | 4 | IO | | | | | | | | |
| | | mm3_txdat | 6 | IO | | | | | | | | |
| | | safe_mode | 7 | | | | | | | | | |
| AC1 | NA | mcbsp4_fsx | 0 | IO | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | gpio_155 | 4 | IO | | | | | | | | |
| | | mm3_txen_n | 6 | IO | | | | | | | | |
| | | safe_mode | 7 | | | | | | | | | |
| Y21 | NA | mcbsp1_clkr | 0 | IO | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | mcspi4_clk | 1 | IO | | | | | | | | |
| | | gpio_156 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | | | | | | | | | |
| AA21 | NA | mcbsp1_fsr | 0 | IO | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | cam_global_reset | 2 | IO | | | | | | | | |
| | | gpio_157 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | | | | | | | | | |
| V21 | NA | mcbsp1_dx | 0 | IO | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | mcspi4_simo | 1 | IO | | | | | | | | |
| | | mcbsp3_dx | 2 | IO | | | | | | | | |
| | | gpio_158 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | | | | | | | | | |
| U21 | NA | mcbsp1_dr | 0 | I | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | mcspi4_somi | 1 | IO | | | | | | | | |
| | | mcbsp3_dr | 2 | I | | | | | | | | |
| | | gpio_159 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | | | | | | | | | |
| T21 | NA | mcbsp_clks | 0 | I | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |

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## Table 2-1. Ball Characteristics (CBP Pkg.)[3]  (continued)

| BALL BOTTOM [1] | BALL TOP [1] | PIN NAME [2] | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | POWER [8] | HYS [9] | BUFFER STRENGTH (mA) [10] | PULLUP /DOWN TYPE [11] | IO CELL [12] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | cam_shutter | 2 | O | | | | | | | | |
| | | gpio_160 | 4 | IO | | | | | | | | |
| | | uart1_cts | 5 | I | | | | | | | | |
| | | safe_mode | 7 | | | | | | | | | |
| K26 | NA | mcbsp1_fsx | 0 | IO | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | mcspi4_cs0 | 1 | IO | | | | | | | | |
| | | mcbsp3_fsx | 2 | IO | | | | | | | | |
| | | gpio_161 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | | | | | | | | | |
| W21 | NA | mcbsp1_clkx | 0 | IO | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | mcbsp3_clkx | 2 | IO | | | | | | | | |
| | | gpio_162 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | | | | | | | | | |
| H18 | NA | uart3_cts_rctx | 0 | IO | H | H | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | gpio_163 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | | | | | | | | | |
| H19 | NA | uart3_rts_sd | 0 | O | H | H | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | gpio_164 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | | | | | | | | | |
| H20 | NA | uart3_rx_irrx | 0 | I | H | H | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | gpio_165 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | | | | | | | | | |
| H21 | NA | uart3_tx_irtx | 0 | O | H | H | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | gpio_166 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | | | | | | | | | |
| T28 | NA | hsusb0_clk | 0 | I | L | L | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| | | gpio_120 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | | | | | | | | | |
| T25 | NA | hsusb0_stp | 0 | O | H | H | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | gpio_121 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | | | | | | | | | |
| R28 | NA | hsusb0_dir | 0 | I | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | gpio_122 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | | | | | | | | | |
| T26 | NA | hsusb0_nxt | 0 | I | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | gpio_124 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | | | | | | | | | |
| T27 | NA | hsusb0_data0 | 0 | IO | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | uart3_tx_irtx | 2 | O | | | | | | | | |
| | | gpio_125 | 4 | IO | | | | | | | | |
| | | uart2_tx | 5 | O | | | | | | | | |
| | | safe_mode | 7 | | | | | | | | | |
| U28 | NA | hsusb0_data1 | 0 | IO | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | uart3_rx_irrx | 2 | I | | | | | | | | |
| | | gpio_130 | 4 | IO | | | | | | | | |
| | | uart2_rx | 5 | I | | | | | | | | |
| | | safe_mode | 7 | | | | | | | | | |
| U27 | NA | hsusb0_data2 | 0 | IO | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | uart3_rts_sd | 2 | O | | | | | | | | |
| | | gpio_131 | 4 | IO | | | | | | | | |
| | | uart2_rts | 5 | O | | | | | | | | |
| | | safe_mode | 7 | | | | | | | | | |
| U26 | NA | hsusb0_data3 | 0 | IO | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | uart3_cts_rctx | 2 | IO | | | | | | | | |

## Table 2-1. Ball Characteristics (CBP Pkg.)[3] (continued)

| BALL BOTTOM [1] | BALL TOP [1] | PIN NAME [2] | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | POWER [8] | HYS [9] | BUFFER STRENGTH (mA) [10] | PULLUP /DOWN TYPE [11] | IO CELL [12] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | gpio_169 | 4 | IO | | | | | | | | |
| | | uart2_cts | 5 | I | | | | | | | | |
| | | safe_mode | 7 | | | | | | | | | |
| U25 | NA | hsusb0_data4 | 0 | IO | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | gpio_188 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | | | | | | | | | |
| V28 | NA | hsusb0_data5 | 0 | IO | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | gpio_189 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | | | | | | | | | |
| V27 | NA | hsusb0_data6 | 0 | IO | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | gpio_190 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | | | | | | | | | |
| V26 | NA | hsusb0_data7 | 0 | IO | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | gpio_191 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | | | | | | | | | |
| K21 | NA | i2c1_scl | 0 | OD | H | H | 0 | vdds | NA | 3 | PU/ PD[6)(7)] | Open Drain |
| J21 | NA | i2c1_sda | 0 | IOD | H | H | 0 | vdds | Yes | 3 | PU/ PD[6)(7)] | Open Drain |
| AF15 | NA | i2c2_scl | 0 | OD | H | H | 7 | vdds | Yes | 3 | PU/ PD[6) (8)] | Open Drain |
| | | gpio_168 | 4 | IO | | | | | | 4 | | |
| | | safe_mode | 7 | | | | | | | | | |
| AE15 | NA | i2c2_sda | 0 | IOD | H | H | 7 | vdds | Yes | 3 | PU/ PD[6) (8)] | Open Drain |
| | | gpio_183 | 4 | IO | | | | | | 4 | | |
| | | safe_mode | 7 | | | | | | | | | |
| AF14 | NA | i2c3_scl | 0 | OD | H | H | 7 | vdds | Yes | 3 | PU/ PD[6) (8)] | Open Drain |
| | | gpio_184 | 4 | IO | | | | | | 4 | | |
| | | safe_mode | 7 | | | | | | | | | |
| AG14 | NA | i2c3_sda | 0 | IOD | H | H | 7 | vdds | Yes | 3 | PU/ PD[6) (8)] | Open Drain |
| | | gpio_185 | 4 | IO | | | | | | 4 | | |
| | | safe_mode | 7 | | | | | | | | | |
| AD26 | NA | i2c4_scl | 0 | OD | H | H | 0 | vdds | Yes | 3 | PU/ PD[6)(7)] | Open Drain |
| | | sys_ nvmode1 | 1 | O | | | | | | 4 | | |
| | | safe_mode | 7 | | | | | | | | | |
| AE26 | NA | i2c4_sda | 0 | IOD | H | H | 0 | vdds | Yes | 3 | PU/ PD[6)(7)] | Open Drain |
| | | sys_ nvmode2 | 1 | O | | | | | | 4 | | |
| | | safe_mode | 7 | | | | | | | | | |
| J25 | NA | hdq_sio | 0 | IOD | H | H | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | sys_altclk | 1 | I | | | | | | | | |
| | | i2c2_sccbe | 2 | OD | | | | | | | | |
| | | i2c3_sccbe | 3 | OD | | | | | | | | |
| | | gpio_170 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | | | | | | | | | |
| AB3 | NA | mcspi1_clk | 0 | IO | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | mmc2_dat4 | 1 | IO | | | | | | | | |
| | | gpio_171 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | | | | | | | | | |
| AB4 | NA | mcspi1_ simo | 0 | IO | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | mmc2_dat5 | 1 | IO | | | | | | | | |
| | | gpio_172 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | | | | | | | | | |
| AA4 | NA | mcspi1_ somi | 0 | IO | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | mmc2_dat6 | 1 | IO | | | | | | | | |
| | | gpio_173 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | | | | | | | | | |
| AC2 | NA | mcspi1_cs0 | 0 | IO | H | H | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |

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## Table 2-1. Ball Characteristics (CBP Pkg.)[3]  (continued)

| BALL BOTTOM [1] | BALL TOP [1] | PIN NAME [2] | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | POWER [8] | HYS [9] | BUFFER STRENGTH (mA) [10] | PULLUP /DOWN TYPE [11] | IO CELL [12] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | mmc2_dat7 | 1 | IO | | | | | | | | |
| | | gpio_174 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | | | | | | | | | |
| AC3 | NA | mcspi1_cs1 | 0 | O | H | H | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | mmc3_cmd | 3 | IO | | | | | | | | |
| | | gpio_175 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | | | | | | | | | |
| AB1 | NA | mcspi1_cs2 | 0 | O | H | H | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | mmc3_clk | 3 | O | | | | | | | | |
| | | gpio_176 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | | | | | | | | | |
| AB2 | NA | mcspi1_cs3 | 0 | O | H | H | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | hsusb2_ data2 | 3 | IO | | | | | | | | |
| | | gpio_177 | 4 | IO | | | | | | | | |
| | | mm2_txdat | 5 | IO | | | | | | | | |
| | | safe_mode | 7 | | | | | | | | | |
| AA3 | NA | mcspi2_clk | 0 | IO | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | hsusb2_ data7 | 3 | IO | | | | | | | | |
| | | gpio_178 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | | | | | | | | | |
| Y2 | NA | mcspi2_ simo | 0 | IO | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | gpt_9_pwm_evt | 1 | IO | | | | | | | | |
| | | hsusb2_ data4 | 3 | IO | | | | | | | | |
| | | gpio_179 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | | | | | | | | | |
| Y3 | NA | mcspi2_ somi | 0 | IO | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | gpt_10_pwm_evt | 1 | IO | | | | | | | | |
| | | hsusb2_ data5 | 3 | IO | | | | | | | | |
| | | gpio_180 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | | | | | | | | | |
| Y4 | NA | mcspi2_cs0 | 0 | IO | H | H | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | gpt_11_pwm_evt | 1 | IO | | | | | | | | |
| | | hsusb2_ data6 | 3 | IO | | | | | | | | |
| | | gpio_181 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | | | | | | | | | |
| V3 | NA | mcspi2_cs1 | 0 | O | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | gpt_8_pwm_evt | 1 | IO | | | | | | | | |
| | | hsusb2_ data3 | 3 | IO | | | | | | | | |
| | | gpio_182 | 4 | IO | | | | | | | | |
| | | mm2_txen_n | 5 | IO | | | | | | | | |
| | | safe_mode | 7 | | | | | | | | | |
| AE25 | NA | sys_32k | 0 | I | Z | Z | 0 | vdds | Yes | NA | PU/ PD | LVCMOS |
| AE17 | NA | sys_xtalin | 0 | AI | Z | Z | 0 | vdds | Yes | NA | No | LVCMOS Analog |
| AF17 | NA | sys_xtalout | 0 | AO | Z | 0 | 0 | vdds | NA | NA | NA | LVCMOS Analog |
| AF25 | NA | sys_clkreq | 0 | IO | 0 | See [(11)] | 0 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | gpio_1 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | | | | | | | | | |
| AF26 | NA | sys_nirq | 0 | I | H | H | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | gpio_0 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | | | | | | | | | |
| AH25 | NA | sys_nrespwron | 0 | I | Z | Z | 0 | vdds | Yes | NA | No | LVCMOS |
| AF24 | NA | sys_nreswarm | 0 | IOD | 0 | H | 0 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | gpio_30 | 4 | IO | | | | | | | | Open Drain |

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## Table 2-1. Ball Characteristics (CBP Pkg.)[3] (continued)

| BALL BOTTOM [1] | BALL TOP [1] | PIN NAME [2] | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | POWER [8] | HYS [9] | BUFFER STRENGTH (mA) [10] | PULLUP /DOWN TYPE [11] | IO CELL [12] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | safe_mode | 7 | | | | | | | | | |
| AH26 | NA | sys_boot0 | 0 | I | Z | Z | 0 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| | | dss_data18 | 3 | IO | | | | | | | | |
| | | gpio_2 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | | | | | | | | | |
| AG26 | NA | sys_boot1 | 0 | I | Z | Z | 0 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| | | dss_data19 | 3 | IO | | | | | | | | |
| | | gpio_3 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | | | | | | | | | |
| AE14 | NA | sys_boot2 | 0 | I | Z | Z | 0 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| | | gpio_4 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | | | | | | | | | |
| AF18 | NA | sys_boot3 | 0 | I | Z | Z | 0 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| | | dss_data20 | 3 | O | | | | | | | | |
| | | gpio_5 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | | | | | | | | | |
| AF19 | NA | sys_boot4 | 0 | I | Z | Z | 0 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| | | mmc2_dir_dat2 | 1 | O | | | | | | | | |
| | | dss_data21 | 3 | O | | | | | | | | |
| | | gpio_6 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | | | | | | | | | |
| AE21 | NA | sys_boot5 | 0 | I | Z | Z | 0 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| | | mmc2_dir_dat3 | 1 | O | | | | | | | | |
| | | dss_data22 | 3 | O | | | | | | | | |
| | | gpio_7 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | | | | | | | | | |
| AF21 | NA | sys_boot6 | 0 | I | Z | Z | 0 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| | | dss_data23 | 3 | O | | | | | | | | |
| | | gpio_8 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | | | | | | | | | |
| AF22 | NA | sys_off_mode | 0 | O | 0 | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | gpio_9 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | | | | | | | | | |
| AG25 | NA | sys_clkout1 | 0 | O | L | L | 7[14] | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | gpio_10 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | | | | | | | | | |
| AE22 | NA | sys_clkout2 | 0 | O | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | gpio_186 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | | | | | | | | | |
| AA17 | NA | jtag_ntrst | 0 | I | L | L | 0 | vdds | Yes | NA | PU/ PD | LVCMOS |
| AA13 | NA | jtag_tck | 0 | I | L | L | 0 | vdds | Yes | NA | PU/ PD | LVCMOS |
| AA12 | NA | jtag_rtck | 0 | O | L | 0 | 0 | vdds | NA | 4 | PU/ PD | LVCMOS |
| AA18 | NA | jtag_tms_tmsc | 0 | IO | H | H | 0 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| AA20 | NA | jtag_tdi | 0 | I | H | H | 0 | vdds | Yes | NA | PU/ PD | LVCMOS |
| AA19 | NA | jtag_tdo | 0 | O | L | Z | 0 | vdds | NA | 4 | PU/ PD | LVCMOS |
| AA11 | NA | jtag_emu0 | 0 | IO | H | H | 0 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | gpio_11 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | | | | | | | | | |
| AA10 | NA | jtag_emu1 | 0 | IO | H | H | 0 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | gpio_31 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | | | | | | | | | |
| AF10 | NA | etk_clk | 0 | O | H | H | 4 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | mcbsp5_ clkx | 1 | IO | | | | | | | | |
| | | mmc3_clk | 2 | O | | | | | | | | |

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## Table 2-1. Ball Characteristics (CBP Pkg.)[(3)] (continued)

| BALL BOTTOM [1] | BALL TOP [1] | PIN NAME [2] | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | POWER [8] | HYS [9] | BUFFER STRENGTH (mA) [10] | PULLUP /DOWN TYPE [11] | IO CELL [12] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | hsusb1_stp | 3 | O | | | | | | | | |
| | | gpio_12 | 4 | IO | | | | | | | | |
| | | mm1_rxdp | 5 | IO | | | | | | | | |
| | | hw_dbg0 | 7 | O | | | | | | | | |
| AE10 | NA | etk_ctl | 0 | O | H | H | 4 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | mmc3_cmd | 2 | IO | | | | | | | | |
| | | hsusb1_clk | 3 | O | | | | | | | | |
| | | gpio_13 | 4 | IO | | | | | | | | |
| | | hw_dbg1 | 7 | O | | | | | | | | |
| AF11 | NA | etk_d0 | 0 | O | H | H | 4 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | mcspi3_ simo | 1 | IO | | | | | | | | |
| | | mmc3_dat4 | 2 | IO | | | | | | | | |
| | | hsusb1_ data0 | 3 | IO | | | | | | | | |
| | | gpio_14 | 4 | IO | | | | | | | | |
| | | mm1_rxrcv | 5 | IO | | | | | | | | |
| | | hw_dbg2 | 7 | O | | | | | | | | |
| AG12 | NA | etk_d1 | 0 | O | H | H | 4 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | mcspi3_ somi | 1 | IO | | | | | | | | |
| | | hsusb1_ data1 | 3 | IO | | | | | | | | |
| | | gpio_15 | 4 | IO | | | | | | | | |
| | | mm1_txse0 | 5 | IO | | | | | | | | |
| | | hw_dbg3 | 7 | O | | | | | | | | |
| AH12 | NA | etk_d2 | 0 | O | H | H | 4 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | mcspi3_cs0 | 1 | IO | | | | | | | | |
| | | hsusb1_ data2 | 3 | IO | | | | | | | | |
| | | gpio_16 | 4 | IO | | | | | | | | |
| | | mm1_txdat | 5 | IO | | | | | | | | |
| | | hw_dbg4 | 7 | O | | | | | | | | |
| AE13 | NA | etk_d3 | 0 | O | H | H | 4 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | mcspi3_clk | 1 | IO | | | | | | | | |
| | | mmc3_dat3 | 2 | IO | | | | | | | | |
| | | hsusb1_ data7 | 3 | IO | | | | | | | | |
| | | gpio_17 | 4 | IO | | | | | | | | |
| | | hw_dbg5 | 7 | O | | | | | | | | |
| AE11 | NA | etk_d4 | 0 | O | L | L | 4 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | mcbsp5_dr | 1 | I | | | | | | | | |
| | | mmc3_dat0 | 2 | IO | | | | | | | | |
| | | hsusb1_ data4 | 3 | IO | | | | | | | | |
| | | gpio_18 | 4 | IO | | | | | | | | |
| | | hw_dbg6 | 7 | O | | | | | | | | |
| AH9 | NA | etk_d5 | 0 | O | L | L | 4 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | mcbsp5_fsx | 1 | IO | | | | | | | | |
| | | mmc3_dat1 | 2 | IO | | | | | | | | |
| | | hsusb1_ data5 | 3 | IO | | | | | | | | |
| | | gpio_19 | 4 | IO | | | | | | | | |
| | | hw_dbg7 | 7 | O | | | | | | | | |
| AF13 | NA | etk_d6 | 0 | O | L | L | 4 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | mcbsp5_dx | 1 | O | | | | | | | | |
| | | mmc3_dat2 | 2 | IO | | | | | | | | |
| | | hsusb1_ data6 | 3 | IO | | | | | | | | |
| | | gpio_20 | 4 | IO | | | | | | | | |
| | | hw_dbg8 | 7 | O | | | | | | | | |
| AH14 | NA | etk_d7 | 0 | O | L | L | 4 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | mcspi3_cs1 | 1 | O | | | | | | | | |

## Table 2-1. Ball Characteristics (CBP Pkg.)[3] (continued)

| BALL BOTTOM [1] | BALL TOP [1] | PIN NAME [2] | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | POWER [8] | HYS [9] | BUFFER STRENGTH (mA) [10] | PULLUP /DOWN TYPE [11] | IO CELL [12] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | mmc3_dat7 | 2 | IO | | | | | | | | |
| | | hsusb1_ data3 | 3 | IO | | | | | | | | |
| | | gpio_21 | 4 | IO | | | | | | | | |
| | | mm1_txen_n | 5 | IO | | | | | | | | |
| | | hw_dbg9 | 7 | O | | | | | | | | |
| AF9 | NA | etk_d8 | 0 | O | L | L | 4 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | mmc3_dat6 | 2 | IO | | | | | | | | |
| | | hsusb1_dir | 3 | I | | | | | | | | |
| | | gpio_22 | 4 | IO | | | | | | | | |
| | | hw_dbg10 | 7 | O | | | | | | | | |
| AG9 | NA | etk_d9 | 0 | O | L | L | 4 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | mmc3_dat5 | 2 | IO | | | | | | | | |
| | | hsusb1_nxt | 3 | I | | | | | | | | |
| | | gpio_23 | 4 | IO | | | | | | | | |
| | | mm1_rxdm | 5 | IO | | | | | | | | |
| | | hw_dbg11 | 7 | O | | | | | | | | |
| AE7 | NA | etk_d10 | 0 | O | L | L | 4 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | uart1_rx | 2 | I | | | | | | | | |
| | | hsusb2_clk | 3 | O | | | | | | | | |
| | | gpio_24 | 4 | IO | | | | | | | | |
| | | hw_dbg12 | 7 | O | | | | | | | | |
| AF7 | NA | etk_d11 | 0 | O | L | L | 4 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | hsusb2_stp | 3 | O | | | | | | | | |
| | | gpio_25 | 4 | IO | | | | | | | | |
| | | mm2_rxdp | 5 | IO | | | | | | | | |
| | | hw_dbg13 | 7 | O | | | | | | | | |
| AG7 | NA | etk_d12 | 0 | O | L | L | 4 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | hsusb2_dir | 3 | I | | | | | | | | |
| | | gpio_26 | 4 | IO | | | | | | | | |
| | | hw_dbg14 | 7 | O | | | | | | | | |
| AH7 | NA | etk_d13 | 0 | O | L | L | 4 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | hsusb2_nxt | 3 | I | | | | | | | | |
| | | gpio_27 | 4 | IO | | | | | | | | |
| | | mm2_rxdm | 5 | IO | | | | | | | | |
| | | hw_dbg15 | 7 | O | | | | | | | | |
| AG8 | NA | etk_d14 | 0 | O | L | L | 4 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | hsusb2_ data0 | 3 | IO | | | | | | | | |
| | | gpio_28 | 4 | IO | | | | | | | | |
| | | mm2_rxrcv | 5 | IO | | | | | | | | |
| | | hw_dbg16 | 7 | O | | | | | | | | |
| AH8 | NA | etk_d15 | 0 | O | L | L | 4 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | hsusb2_ data1 | 3 | IO | | | | | | | | |
| | | gpio_29 | 4 | IO | | | | | | | | |
| | | mm2_txse0 | 5 | IO | | | | | | | | |
| | | hw_dbg17 | 7 | O | | | | | | | | |
| AH21 | NA | vss | 0 | GND | - | - | - | - | - | - | - | - |
| AG16 | NA | vss | 0 | GND | - | - | - | - | - | - | - | - |
| M28 | NA | vss | 0 | GND | - | - | - | - | - | - | - | - |
| AH20 | NA | cap_vddu_array | 0 | PWR | - | - | - | - | - | - | - | - |
| AG20 | NA | vdds | 0 | PWR | - | - | - | - | - | - | - | - |
| AG21 | NA | vdds | 0 | PWR | - | - | - | - | - | - | - | - |
| H28 | NA | vdds | 0 | PWR | - | - | - | - | - | - | - | - |
| P25 | NA | vdds_x | 0 | PWR | - | - | - | - | - | - | - | - |

Product Folder Link(s): DM3730  DM3725

## Table 2-1. Ball Characteristics (CBP Pkg.)[3] (continued)

| BALL BOTTOM [1] | BALL TOP [1] | PIN NAME [2] | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | POWER [8] | HYS [9] | BUFFER STRENGTH (mA) [10] | PULLUP /DOWN TYPE [11] | IO CELL [12] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| AE9, AE18, AE19, AE24, AC4, Y16, Y18, Y19, Y20, W18, W20, V20, U19, U20, T19, P20, N19, N20, M19, M25, L25, K18, K20, J4, J18, J19, J20, H4, E25, D8, D9, D15, D22, D23 | NA | vdd_core | 0 | PWR | - | - | - | - | - | - | - | - |
| Y9, Y10, Y11, Y14, Y15, W9, W11, W12, W15, U10, T9, T10, R9, R10, N10, M9, M10, L9, L10, K11, K14, K13, J9, J10, J11, J14, J15 | NA | vdd_mpu_iva | 0 | PWR | - | - | - | - | - | - | - | - |
| AH6, U1, R4, J1, J2, G28, F1, F2, D16, C16, C28, B5, B8, B12, B18, B22, A5, A8, A12, A18, A22 | AC5, P1, H1, F23, E1, C23, A4, A7, A10, A15, A18 | vdds_mem | 0 | PWR | - | - | - | - | - | - | - | - |
| AG27, AF8, AF16, AF23, AE8, AE16, AE23, AD3, AD4, W4, F25, F26 | NA | vdds | 0 | PWR | - | - | - | - | - | - | - | - |
| W16 | NA | vdds_sram | 0 | PWR | | | | | | | | |
| K15 | NA | vdda_dplls_dll | 0 | PWR | - | - | - | - | - | - | - | - |
| AA16 | NA | vdda_dpll_per | 0 | PWR | - | - | - | - | - | - | - | - |
| AA14 | NA | vdda_wkup_ bg_bb | 0 | PWR | - | - | - | - | - | - | - | - |
| K25 | NA | vdds_mmc1 | 0 | PWR | - | - | - | - | - | - | - | - |
| V25 | NA | vdda_dac | 0 | PWR | - | - | - | - | - | - | - | - |
| Y26 | NA | vssa_dac | 0 | GND | - | - | - | - | - | - | - | - |

## Table 2-1. Ball Characteristics (CBP Pkg.)[3] (continued)

| BALL BOTTOM [1] | BALL TOP [1] | PIN NAME [2] | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | POWER [8] | HYS [9] | BUFFER STRENGTH (mA) [10] | PULLUP /DOWN TYPE [11] | IO CELL [12] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| AG2, AG3, AG6, AF12, AF20, AE12, AE20, AC25, AC26, Y12, Y13, Y25, W3, W10, W13, W14, W17, W19, W25, V9, V10, V19, U2, U9, T20, R19, R20, R26, P3, P4, P9, P10, P19, N9, M20, L19, L20, L26, K9, K10, K12, K16, K17, K19, J3, J12, J13, J16, J17, G27, E3,E4, D7, D10, D13, D19, D21, C7, C10, C13, C19, C22, B2, B27, A3, A26 | B4, B7, B10, B15, B18, C22, E2, F22, H2, P2, AB5, AB14, AB20 | vss | 0 | GND | - | - | - | - | - | - | - | - |
| AA15 | NA | cap_vddu_wkup_logic | 0 | PWR | - | - | - | - | - | - | - | - |
| AH10, AH11, AH13, AH15, AH16, AG11, AG13, AF1, AF28, AE28, AA1, N1, M1, J28, A15, M2, N2, A1, A2, A27, A28, AG1, AG28, AH1, AH2, AH27, AH28, B1, B28, AA2, AF2, AF27, AG10, AG15, B15, J27, M26 | A12, AA1, AA23, AB11, AB9, AC11, AC13, AC14, AC8, AC9, H23, K1, L1, U1, Y23, A1, A2, A22, A23, AB1, AB23, AC1, AC2, AC22, AC23, B1, B23, AA2, U2, AA22, AB8, AB13, B12, H22, K2, K22, L2 | Feed-Through Pins[9] | - | - | - | - | - | - | - | - | - | - |

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## Table 2-1. Ball Characteristics (CBP Pkg.)[3] (continued)

| BALL BOTTOM [1] | BALL TOP [1] | PIN NAME [2] | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | POWER [8] | HYS [9] | BUFFER STRENGTH (mA) [10] | PULLUP /DOWN TYPE [11] | IO CELL [12] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| G1, A13, A14,A16, A17, B14, B16, B17, C14, C15, C17, D17, D18, H9, H10, H11, H12, H13, H14, H15, H16, H17, A4, A6, A7, A9, A10, A11, A19, A20, A21, B3, B4, B6, B7, B9, B10, B11, B13, B19, B20, B21, C1,C2, C3, C4,C5, C6, C8,C9, C11, C12, C18, C20, C21, D1, D2, D3, D4, D5,D6, D11, D12,D14, D20, E1,E2, AA26, AE27 | AB2, AB22, B2, B22 | No Connect[2] | - | - | | | | | | | | |
| Y17 | NA | sys_xtalgnd | 0 | GND | | | | | | | | |
| U4 | NA | cap_vdd_bb_ mpu_iva | 0 | PWR | | | | | | | | |
| V4 | NA | cap_vdd_sram _mpu_iva | 0 | PWR | | | | | | | | |
| L21 | NA | cap_vdd_sram_core | 0 | PWR | | | | | | | | |

(1) The usage of this GPIO is strongly restricted. For more information, see the GPIO chapter of the *AM/DM37x Multimedia Device Technical Reference Manual* (literature number SPRUGN4).

(2) Pins labeled as "No connect" must be left unconnected. Any connections to these pins may result in unpredictable behavior.

(3) NA in this table stands for "Not Applicable".

(4) The drive strength is fixed regardless of the load. The driver is designed to drive 75-ohm for video applications.

(5) PU = [50 to 100 kΩ] per default or [10 to 50 kΩ] according to the selected mode.
For a full description of the pull-up drive strength programming, see the PRG_SDMMC_PUSTRENGTH configuration register bit field in the System Control Module chapter of the *AM/DM37x Multimedia Device Technical Reference Manual* (literature number SPRUGN4).
PD: 30 to 150 kΩ.

(6) The pullup and pulldown can be either the standard LVCMOS 100-µA drive strength or the I2C pullup and pulldown described below:
Nominal resistance = 1.66 kΩ in high-speed mode with a load range of 5 pF to 12 pF, 4.5 kΩ in standard / fast mode with a load range of 5 pF to 15 pF.

(7) The default buffer configuration is High-Speed I2C point-to-point mode using internal pullup. For a full description of the pull drive strength programming, see prg_i2c1_pullupresx, prg_i2c1_lb1lb0, and prg_sr_pullupresx, prg_sr_lb bits of the CONTROL_PROG_IO1, CONTROL_PROG_IO_WKUP1 control modules in the System Control Module / SCM Programming Model / Feature Settings section and the System Control Module chapter of the *AM/DM37x Multimedia Device Technical Reference Manual* (literature number SPRUGN4) to modify the IO settings if required by the targeted interface application.

(8) The default buffer configuration is standard LVCMOS mode (non-I2C). For a full description of the pull drive strength programming, see PADCONFS bits of CONTROL_PADCONF_X control modules (standard LVCMOS mode), or prg_i2c2_pullupresx, prg_i2c2_lb1lb0, and prg_i2c3_pullupresx, prg_i2c3_lb1lb0 bits of the CONTROL_PROG_IO2, CONTROL_PROG_IO3 control modules (I2C mode) in the System Control Module chapter of the *AM/DM37x Multimedia Device Technical Reference Manual* (literature number SPRUGN4) to modify the IO settings if required by the targeted interface application.

(9) These signals are feed-through balls. For more information, see Table 2-28.

(10) In buffer mode, the drive strength is fixed regardless of the load. The driver is designed to drive 75Ω for video applications. In bypass mode, the drive strength is 0.47 mA.

(11) Depending on the sys_clkreq direction the corresponding reset released state value can be:
– Z if sys_clkreq is used as input
– 1 if sys_clkreq is used as output
For a full description of the sys_clkreq control, see Power, Reset, and Clock Management chapter of the *AM/DM37x Multimedia Device Technical Reference Manual* (literature number SPRUGN4).

(12) The drive strength of these IOs is set according to the programmable load range: 2 pF to 4 pF per default or 4 pF to 12 pF. For a full description of the drive strength programming, see the System Control Module chapter of the *AM/DM37x Multimedia Device Technical*

*Reference Manual* (literature number SPRUGN4).

(13)  In the safe_mode_out1, the buffer is configured to drive 1.

(14)  Mux0 if sys_boot6 is pulled down (clock master).

(15)  If MMC1 functional signals are enabled, vdds_mmc1 for MMC1 must be supplied by a dedicated power source.
      If MMC1 functional signals are disabled, other multiplexed CMOS signals of the interface can be enabled. The interface can be supplied
      by the same power source as vdds. The vdds power source supplies the vdds_mmc1 ball.
      If neither MMC1 functional balls or CMOS signals are enabled, the interface balls are left unconnected with its associated power supply
      (vdda/vssa) grounded.
      For the corresponding setting of the PBIASLITEPWRDNZ0 bit, see the System Control Module / SCM Programming Model /
      Extended-Drain I/Os and PBIAS Cells Programming Guide section of the *AM/DM37x Multimedia Device Technical Reference Manual*
      (literature number SPRUGN4).

## Table 2-2.  Ball Characteristics (CBC Pkg.)[5]

| BALL BOTTOM [1] | BALL TOP [1] | PIN NAME [2] | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | POWER [8] | HYS [9] | BUFFER STRENGTH (mA) [10] | PULLUP /DOWN TYPE [11] | IO CELL [12] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| AE16 | NA | cam_d0 | 0 | I | L | L | 7 | vdda | Yes | NA | PU/ PD | LVCMOS |
|  |  | gpio_99 | 4 | I |  |  |  |  |  |  |  |  |
|  |  | safe_mode | 7 | - |  |  |  |  |  |  |  |  |
| AE15 | NA | cam_d1 | 0 | I | L | L | 7 | vdda | Yes | NA | PU/ PD | LVCMOS |
|  |  | gpio_100 | 4 | I |  |  |  |  |  |  |  |  |
|  |  | safe_mode | 7 | - |  |  |  |  |  |  |  |  |
| AD17 | NA | gpio_112 | 4 | I | L | L | 7 | vdda | Yes | NA | PU/ PD | LVCMOS |
|  |  | safe_mode | 7 | - |  |  |  |  |  |  |  |  |
| AE18 | NA | gpio_114 | 4 | I | L | L | 7 | vdda | Yes | NA | PU/ PD | LVCMOS |
|  |  | safe_mode | 7 | - |  |  |  |  |  |  |  |  |
| AD16 | NA | gpio_113 | 4 | I | L | L | 7 | vdda | Yes | NA | PU/ PD | LVCMOS |
|  |  | safe_mode | 7 | - |  |  |  |  |  |  |  |  |
|  |  | gpio_115 | 4 | I |  |  |  |  |  |  |  |  |  |
| AE17 | NA | safe_mode | 7 | - | L | L | 7 | vdda | Yes | NA | PU/ PD | LVCMOS |
| NA | G20 | sdrc_a0 | 0 | O | 0 | 0 | 0 | vdds | NA | 4 [1] | PU/ PD | LVCMOS |
| NA | K20 | sdrc_a1 | 0 | O | 0 | 0 | 0 | vdds | NA | 4[1] | PU/ PD | LVCMOS |
| NA | J20 | sdrc_a2 | 0 | O | 0 | 0 | 0 | vdds | NA | 4 [1] | PU/ PD | LVCMOS |
| NA | J21 | sdrc_a3 | 0 | O | 0 | 0 | 0 | vdds | NA | 4 [1] | PU/ PD | LVCMOS |
| NA | U21 | sdrc_a4 | 0 | O | 0 | 0 | 0 | vdds | NA | 4 [1] | PU/ PD | LVCMOS |
| NA | R20 | sdrc_a5 | 0 | O | 0 | 0 | 0 | vdds | NA | 4 [1] | PU/ PD | LVCMOS |
| NA | M21 | sdrc_a6 | 0 | O | 0 | 0 | 0 | vdds | NA | 4 [1] | PU/ PD | LVCMOS |
| NA | M20 | sdrc_a7 | 0 | O | 0 | 0 | 0 | vdds | NA | 4 [1] | PU/ PD | LVCMOS |
| NA | N20 | sdrc_a8 | 0 | O | 0 | 0 | 0 | vdds | NA | 4 [1] | PU/ PD | LVCMOS |
| NA | K21 | sdrc_a9 | 0 | O | 0 | 0 | 0 | vdds | NA | 4 [1] | PU/ PD | LVCMOS |
| NA | Y16 | sdrc_a10 | 0 | O | 0 | 0 | 0 | vdds | NA | 4 [1] | PU/ PD | LVCMOS |
| NA | N21 | sdrc_a11 | 0 | O | 0 | 0 | 0 | vdds | NA | 4[1] | PU/ PD | LVCMOS |
| NA | R21 | sdrc_a12 | 0 | O | 0 | 0 | 0 | vdds | NA | 4 [1] | PU/ PD | LVCMOS |
| NA | AA15 | sdrc_a13 | 0 | O | 0 | 0 | 0 | vdds | NA | 4 [1] | PU/ PD | LVCMOS |
| NA | Y12 | sdrc_a14 | 0 | O | 0 | 0 | 0 | vdds | NA | 4 [1] | PU/ PD | LVCMOS |
| NA | AA18 | sdrc_ba0 | 0 | O | 0 | 0 | 0 | vdds | NA | 4 [1] | PU/ PD | LVCMOS |
| NA | V20 | sdrc_ba1 | 0 | O | 0 | 0 | 0 | vdds | NA | 4[1] | PU/ PD | LVCMOS |
| NA | Y15 | sdrc_cke0 | 0 | O | H | 1 | 7 | vdds | NA | 4 [1] | PU/ PD | LVCMOS |
|  |  | safe_mode_out1[6] | 7 |  |  |  |  |  |  |  |  |  |
| NA | Y13 | sdrc_cke1 | 0 | O | H | 1 | 7 | vdds | NA | 4 [1] | PU/ PD | LVCMOS |
|  |  | safe_mode_out1[6] | 7 |  |  |  |  |  |  |  |  |  |
| NA | A12 | sdrc_clk | 0 | IO | L | 0 | 0 | vdds | Yes | 4 [1] | PU/ PD | LVCMOS |
| NA | D1 | sdrc_d0 | 0 | IO | L | Z | 0 | vdds | Yes | 4 [1] | PU/ PD | LVCMOS |
| NA | G1 | sdrc_d1 | 0 | IO | L | Z | 0 | vdds | Yes | 4 [1] | PU/ PD | LVCMOS |
| NA | G2 | sdrc_d2 | 0 | IO | L | Z | 0 | vdds | Yes | 4 [1] | PU/ PD | LVCMOS |
| NA | E1 | sdrc_d3 | 0 | IO | L | Z | 0 | vdds | Yes | 4[1] | PU/ PD | LVCMOS |
| NA | D2 | sdrc_d4 | 0 | IO | L | Z | 0 | vdds | Yes | 4 [1] | PU/ PD | LVCMOS |
| NA | E2 | sdrc_d5 | 0 | IO | L | Z | 0 | vdds | Yes | 4 [1] | PU/ PD | LVCMOS |
| NA | B3 | sdrc_d6 | 0 | IO | L | Z | 0 | vdds | Yes | 4 [1] | PU/ PD | LVCMOS |

## Table 2-2. Ball Characteristics (CBC Pkg.)[5]  (continued)

| BALL BOTTOM [1] | BALL TOP [1] | PIN NAME [2] | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | POWER [8] | HYS [9] | BUFFER STRENGTH (mA) [10] | PULLUP /DOWN TYPE [11] | IO CELL [12] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| NA | B4 | sdrc_d7 | 0 | IO | L | Z | 0 | vdds | Yes | 4 (1) | PU/ PD | LVCMOS |
| NA | A10 | sdrc_d8 | 0 | IO | L | Z | 0 | vdds | Yes | 4 (1) | PU/ PD | LVCMOS |
| NA | B11 | sdrc_d9 | 0 | IO | L | Z | 0 | vdds | Yes | 4 (1) | PU/ PD | LVCMOS |
| NA | A11 | sdrc_d10 | 0 | IO | L | Z | 0 | vdds | Yes | 4 (1) | PU/ PD | LVCMOS |
| NA | B12 | sdrc_d11 | 0 | IO | L | Z | 0 | vdds | Yes | 4(1) | PU/ PD | LVCMOS |
| NA | A16 | sdrc_d12 | 0 | IO | L | Z | 0 | vdds | Yes | 4 (1) | PU/ PD | LVCMOS |
| NA | A17 | sdrc_d13 | 0 | IO | L | Z | 0 | vdds | Yes | 4 (1) | PU/ PD | LVCMOS |
| NA | B17 | sdrc_d14 | 0 | IO | L | Z | 0 | vdds | Yes | 4 (1) | PU/ PD | LVCMOS |
| NA | B18 | sdrc_d15 | 0 | IO | L | Z | 0 | vdds | Yes | 4 (1) | PU/ PD | LVCMOS |
| NA | B7 | sdrc_d16 | 0 | IO | L | Z | 0 | vdds | Yes | 4 (1) | PU/ PD | LVCMOS |
| NA | A5 | sdrc_d17 | 0 | IO | L | Z | 0 | vdds | Yes | 4 (1) | PU/ PD | LVCMOS |
| NA | B6 | sdrc_d18 | 0 | IO | L | Z | 0 | vdds | Yes | 4 (1) | PU/ PD | LVCMOS |
| NA | A6 | sdrc_d19 | 0 | IO | L | Z | 0 | vdds | Yes | 4 (1) | PU/ PD | LVCMOS |
| NA | A8 | sdrc_d20 | 0 | IO | L | Z | 0 | vdds | Yes | 4 (1) | PU/ PD | LVCMOS |
| NA | B9 | sdrc_d21 | 0 | IO | L | Z | 0 | vdds | Yes | 4(1) | PU/ PD | LVCMOS |
| NA | A9 | sdrc_d22 | 0 | IO | L | Z | 0 | vdds | Yes | 4 (1) | PU/ PD | LVCMOS |
| NA | B10 | sdrc_d23 | 0 | IO | L | Z | 0 | vdds | Yes | 4 (1) | PU/ PD | LVCMOS |
| NA | C21 | sdrc_d24 | 0 | IO | L | Z | 0 | vdds | Yes | 4 (1) | PU/ PD | LVCMOS |
| NA | D20 | sdrc_d25 | 0 | IO | L | Z | 0 | vdds | Yes | 4 (1) | PU/ PD | LVCMOS |
| NA | B19 | sdrc_d26 | 0 | IO | L | Z | 0 | vdds | Yes | 4 (1) | PU/ PD | LVCMOS |
| NA | C20 | sdrc_d27 | 0 | IO | L | Z | 0 | vdds | Yes | 4 (1) | PU/ PD | LVCMOS |
| NA | D21 | sdrc_d28 | 0 | IO | L | Z | 0 | vdds | Yes | 4(1) | PU/ PD | LVCMOS |
| NA | E20 | sdrc_d29 | 0 | IO | L | Z | 0 | vdds | Yes | 4 (1) | PU/ PD | LVCMOS |
| NA | E21 | sdrc_d30 | 0 | IO | L | Z | 0 | vdds | Yes | 4 (1) | PU/ PD | LVCMOS |
| NA | G21 | sdrc_d31 | 0 | IO | L | Z | 0 | vdds | Yes | 4(1) | PU/ PD | LVCMOS |
| NA | H1 | sdrc_dm0 | 0 | O | 0 | 0 | 0 | vdds | NA | 4 (1) | PU/ PD | LVCMOS |
| NA | A14 | sdrc_dm1 | 0 | O | 0 | 0 | 0 | vdds | NA | 4 (1) | PU/ PD | LVCMOS |
| NA | A4 | sdrc_dm2 | 0 | O | 0 | 0 | 0 | vdds | NA | 4(1) | PU/ PD | LVCMOS |
| NA | A18 | sdrc_dm3 | 0 | O | 0 | 0 | 0 | vdds | NA | 4 (1) | PU/ PD | LVCMOS |
| NA | C2 | sdrc_dqs0 | 0 | IO | L | Z | 0 | vdds | Yes | 4 (1) | PU/ PD | LVCMOS |
| NA | B15 | sdrc_dqs1 | 0 | IO | L | Z | 0 | vdds | Yes | 4 (1) | PU/ PD | LVCMOS |
| NA | B8 | sdrc_dqs2 | 0 | IO | L | Z | 0 | vdds | Yes | 4 (1) | PU/ PD | LVCMOS |
| NA | A19 | sdrc_dqs3 | 0 | IO | L | Z | 0 | vdds | Yes | 4 (1) | PU/ PD | LVCMOS |
| NA | U20 | sdrc_ncas | 0 | O | 1 | 1 | 0 | vdds | NA | 4 (1) | PU/ PD | LVCMOS |
| NA | B13 | sdrc_nclk | 0 | O | 1 | 1 | 0 | vdds | NA | 4 (1) | PU/ PD | LVCMOS |
| NA | T21 | sdrc_ncs0 | 0 | O | 1 | 1 | 0 | vdds | NA | 4 (1) | PU/ PD | LVCMOS |
| NA | T20 | sdrc_ncs1 | 0 | O | 1 | 1 | 0 | vdds | NA | 4 (1) | PU/ PD | LVCMOS |
| NA | V21 | sdrc_nras | 0 | O | 1 | 1 | 0 | vdds | NA | 4 (1) | PU/ PD | LVCMOS |
| NA | Y18 | sdrc_nwe | 0 | O | 1 | 1 | 0 | vdds | NA | 4 (1) | PU/ PD | LVCMOS |
| AE21 | NA | dss_data0 | 0 | IO | L | L | 7 | vdda | Yes | 8 | PU/ PD | LVCMOS |
|  |  | uart1_cts | 2 | I |  |  |  |  |  | NA |  |  |
|  |  | gpio_70 | 4 | IO |  |  |  |  |  | 8 |  |  |
|  |  | safe_mode | 7 | - |  |  |  |  |  | 8 |  |  |
| AE22 | NA | dss_data1 | 0 | IO | L | L | 7 | vdda | Yes | 8 | PU/ PD | LVCMOS |
|  |  | uart1_rts | 2 | O |  |  |  |  |  | 8 |  |  |
|  |  | gpio_71 | 4 | IO |  |  |  |  |  | 8 |  |  |
|  |  | safe_mode | 7 | - |  |  |  |  |  | 8 |  |  |
| AE23 | NA | dss_data2 | 0 | IO | L | L | 7 | vdda | Yes | 8 | PU/ PD | LVCMOS |
|  |  | gpio_72 | 4 | IO |  |  |  |  |  | 8 |  |  |
|  |  | safe_mode | 7 | - |  |  |  |  |  | 8 |  |  |
| AE24 | NA | dss_data3 | 0 | IO | L | L | 7 | vdda | Yes | 8 | PU/ PD | LVCMOS |
|  |  | gpio_73 | 4 | IO |  |  |  |  |  | 8 |  |  |
|  |  | safe_mode | 7 | - |  |  |  |  |  | 8 |  |  |
| AD23 | NA | dss_data4 | 0 | IO | L | L | 7 | vdda | Yes | 8 | PU/ PD | LVCMOS |
|  |  | uart3_rx_irrx | 2 | I |  |  |  |  |  | NA |  |  |

## Table 2-2. Ball Characteristics (CBC Pkg.)[5]  (continued)

| BALL BOTTOM [1] | BALL TOP [1] | PIN NAME [2] | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | POWER [8] | HYS [9] | BUFFER STRENGTH (mA) [10] | PULLUP /DOWN TYPE [11] | IO CELL [12] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | gpio_74 | 4 | IO | | | | | | 8 | | |
| | | safe_mode | 7 | - | | | | | | 8 | | |
| AD24 | NA | dss_data5 | 0 | IO | L | L | 7 | vdda | Yes | 8 | PU/ PD | LVCMOS |
| | | uart3_tx_irtx | 2 | O | | | | | | 8 | | |
| | | gpio_75 | 4 | IO | | | | | | 8 | | |
| | | safe_mode | 7 | - | | | | | | 8 | | |
| AC26 | NA | dss_data10 | 0 | IO | L | L | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| | | gpio_80 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| AD26 | NA | dss_data11 | 0 | IO | L | L | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| | | gpio_81 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| AA25 | NA | dss_data12 | 0 | IO | L | L | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| | | gpio_82 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| Y25 | NA | dss_data13 | 0 | IO | L | L | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| | | gpio_83 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| AA26 | NA | dss_data14 | 0 | IO | L | L | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| | | gpio_84 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| AB26 | NA | dss_data15 | 0 | IO | L | L | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| | | gpio_85 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| F25 | NA | dss_data20 | 0 | O | H | H | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| | | mcspi3_somi | 2 | IO | | | | | | | | |
| | | dss_data2 | 3 | IO | | | | | | | | |
| | | gpio_90 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| AC25 | NA | dss_data22 | 0 | O | L | L | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| | | mcspi3_cs1 | 2 | O | | | | | | | | |
| | | dss_data4 | 3 | IO | | | | | | | | |
| | | gpio_92 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| AB25 | NA | dss_data23 | 0 | O | L | L | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| | | dss_data5 | 3 | IO | | | | | | | | |
| | | gpio_93 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| G25 | NA | dss_pclk | 0 | O | H | H | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| | | gpio_66 | 4 | IO | | | | | | | | |
| | | hw_dbg12 | 5 | O | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| J2 | NA | gpmc_a1 | 0 | O | L | L | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| | | gpio_34 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| H1 | NA | gpmc_a2 | 0 | O | L | L | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| | | gpio_35 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| H2 | NA | gpmc_a3 | 0 | O | L | L | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| | | gpio_36 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| G2 | NA | gpmc_a4 | 0 | O | L | L | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| | | gpio_37 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| F1 | NA | gpmc_a5 | 0 | O | L | L | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |

## Table 2-2. Ball Characteristics (CBC Pkg.)[5]  (continued)

| BALL BOTTOM [1] | BALL TOP [1] | PIN NAME [2] | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | POWER [8] | HYS [9] | BUFFER STRENGTH (mA) [10] | PULLUP /DOWN TYPE [11] | IO CELL [12] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | gpio_38 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| F2 | NA | gpmc_a6 | 0 | O | H | H | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| | | gpio_39 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| E1 | NA | gpmc_a7 | 0 | O | H | H | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| | | gpio_40 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| E2 | NA | gpmc_a8 | 0 | O | H | H | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| | | gpio_41 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| D1 | NA | gpmc_a9 | 0 | O | H | H | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| | | sys_ndmareq2 | 1 | I | | | | | | | | |
| | | gpio_42 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| D2 | NA | gpmc_a10 | 0 | O | H | H | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| | | sys_ndmareq3 | 1 | I | | | | | | | | |
| | | gpio_43 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| N1 | L1 | gpmc_clk | 0 | O | L | 0 | 0 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| | | gpio_59 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| AA2 | U2 | gpmc_d0 | 0 | IO | H | H | 0 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| AA1 | U1 | gpmc_d1 | 0 | IO | H | H | 0 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| AC2 | V2 | gpmc_d2 | 0 | IO | H | H | 0 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| AC1 | V1 | gpmc_d3 | 0 | IO | H | H | 0 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| AE5 | AA3 | gpmc_d4 | 0 | IO | H | H | 0 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| AD6 | AA4 | gpmc_d5 | 0 | IO | H | H | 0 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| AD5 | Y3 | gpmc_d6 | 0 | IO | H | H | 0 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| AC5 | Y4 | gpmc_d7 | 0 | IO | H | H | 0 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| V1 | R1 | gpmc_d8 | 0 | IO | H | H | 0 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| | | gpio_44 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| Y1 | T1 | gpmc_d9 | 0 | IO | H | H | 0 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| | | gpio_45 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| T1 | N1 | gpmc_d10 | 0 | IO | H | H | 0 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| | | gpio_46 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| U2 | P2 | gpmc_d11 | 0 | IO | H | H | 0 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| | | gpio_47 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| U1 | P1 | gpmc_d12 | 0 | IO | H | H | 0 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| | | gpio_48 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| P1 | M1 | gpmc_d13 | 0 | IO | H | H | 0 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| | | gpio_49 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| L2 | J2 | gpmc_d14 | 0 | IO | H | H | 0 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| | | gpio_50 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| M2 | K2 | gpmc_d15 | 0 | IO | H | H | 0 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| | | gpio_51 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| AD10 | AA9 | gpmc_nadv_ale | 0 | O | 0 | 0 | 0 | vdds | NA | 8 | NA | LVCMOS |

## Table 2-2. Ball Characteristics (CBC Pkg.)[5]  (continued)

| BALL BOTTOM [1] | BALL TOP [1] | PIN NAME [2] | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | POWER [8] | HYS [9] | BUFFER STRENGTH (mA) [10] | PULLUP /DOWN TYPE [11] | IO CELL [12] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| K2 | NA | gpmc_nbe0_cle | 0 | O | L | 0 | 0 | vdds | Yes | 8 | PU/ PD | LVCMOS |
|  |  | gpio_60 | 4 | IO |  |  |  |  |  |  |  |  |
|  |  | safe_mode | 7 | - |  |  |  |  |  |  |  |  |
| J1 | NA | gpmc_nbe1 | 0 | O | L | L | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
|  |  | gpio_61 | 4 | IO |  |  |  |  |  |  |  |  |
|  |  | safe_mode | 7 | - |  |  |  |  |  |  |  |  |
| AD8 | AA8 | gpmc_ncs0 | 0 | O | 1 | 1 | 0 | vdds | NA | 8 | NA | LVCMOS |
| AD1 | W1 | gpmc_ncs1 | 0 | O | H | 1 | 0 | vdds | Yes | 8 | PU/ PD | LVCMOS |
|  |  | gpio_52 | 4 | IO |  |  |  |  |  |  |  |  |
|  |  | safe_mode | 7 | - |  |  |  |  |  |  |  |  |
| A3 | NA | gpmc_ncs2 | 0 | O | H | H | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
|  |  | gpio_53 | 4 | IO |  |  |  |  |  |  |  |  |
|  |  | safe_mode | 7 | - |  |  |  |  |  |  |  |  |
| B6 | NA | gpmc_ncs3 | 0 | O | H | H | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
|  |  | sys_ndmareq0 | 1 | I |  |  |  |  |  |  |  |  |
|  |  | gpio_54 | 4 | IO |  |  |  |  |  |  |  |  |
|  |  | safe_mode | 7 | - |  |  |  |  |  |  |  |  |
| B4 | NA | gpmc_ncs4 | 0 | O | H | H | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
|  |  | sys_ndmareq1 | 1 | I |  |  |  |  |  |  |  |  |
|  |  | mcbsp4_clkx | 2 | IO |  |  |  |  |  |  |  |  |
|  |  | gpt_9_pwm_evt | 3 | IO |  |  |  |  |  |  |  |  |
|  |  | gpio_55 | 4 | IO |  |  |  |  |  |  |  |  |
|  |  | safe_mode | 7 | - |  |  |  |  |  |  |  |  |
| C4 | NA | gpmc_ncs5 | 0 | O | H | H | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
|  |  | sys_ndmareq2 | 1 | I |  |  |  |  |  |  |  |  |
|  |  | mcbsp4_dr | 2 | I |  |  |  |  |  |  |  |  |
|  |  | gpt_10_pwm_evt | 3 | IO |  |  |  |  |  |  |  |  |
|  |  | gpio_56 | 4 | IO |  |  |  |  |  |  |  |  |
|  |  | safe_mode | 7 | - |  |  |  |  |  |  |  |  |
| B5 | NA | gpmc_ncs6 | 0 | O | H | H | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
|  |  | sys_ndmareq3 | 1 | I |  |  |  |  |  |  |  |  |
|  |  | mcbsp4_dx | 2 | IO |  |  |  |  |  |  |  |  |
|  |  | gpt_11_pwm_evt | 3 | IO |  |  |  |  |  |  |  |  |
|  |  | gpio_57 | 4 | IO |  |  |  |  |  |  |  |  |
|  |  | safe_mode | 7 | - |  |  |  |  |  |  |  |  |
| C5 | NA | gpmc_ncs7 | 0 | O | H | H | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
|  |  | gpmc_io_dir | 1 | O |  |  |  |  |  |  |  |  |
|  |  | mcbsp4_fsx | 2 | IO |  |  |  |  |  |  |  |  |
|  |  | gpt_8_pwm_evt | 3 | IO |  |  |  |  |  |  |  |  |
|  |  | gpio_58 | 4 | IO |  |  |  |  |  |  |  |  |
|  |  | safe_mode | 7 | - |  |  |  |  |  |  |  |  |
| N2 | L2 | gpmc_noe | 0 | O | 1 | 1 | 0 | vdds | NA | 8 | NA | LVCMOS |
| M1 | K1 | gpmc_nwe | 0 | O | 1 | 1 | 0 | vdds | NA | 8 | NA | LVCMOS |
| AC6 | Y5 | gpmc_nwp | 0 | O | L | 0 | 0 | vdds | Yes | 8 | PU/ PD | LVCMOS |
|  |  | gpio_62 | 4 | IO |  |  |  |  |  |  |  |  |
|  |  | safe_mode | 7 | - |  |  |  |  |  |  |  |  |
| AC11 | Y10 | gpmc_wait0 | 0 | I | H | H | 0 | vdds | Yes | NA | PU/ PD | LVCMOS |
| AC8 | Y8 | gpmc_wait1 | 0 | I | H | H | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
|  |  | gpio_63 | 4 | IO |  |  |  |  |  |  |  |  |
|  |  | safe_mode | 7 | - |  |  |  |  |  |  |  |  |
| B3 | NA | gpmc_wait2 | 0 | I | H | H | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
|  |  | uart4_tx | 2 | O |  |  |  |  |  |  |  |  |
|  |  | gpio_64 | 4 | IO |  |  |  |  |  |  |  |  |
|  |  | safe_mode | 7 | - |  |  |  |  |  |  |  |  |
| C6 | NA | gpmc_wait3 | 0 | I | H | H | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |

Product Folder Link(s): DM3730  DM3725

## Table 2-2.  Ball Characteristics (CBC Pkg.)[5]  (continued)

| BALL BOTTOM [1] | BALL TOP [1] | PIN NAME [2] | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | POWER [8] | HYS [9] | BUFFER STRENGTH (mA) [10] | PULLUP /DOWN TYPE [11] | IO CELL [12] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | sys_ndmareq1 | 1 | I | | | | | | | | |
| | | uart4_rx | 2 | I | | | | | | | | |
| | | gpio_65 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| W19 | NA | hsusb0_clk | 0 | I | L | L | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| | | gpio_120 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| V20 | NA | hsusb0_data0 | 0 | IO | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | uart3_tx_irtx | 2 | O | | | | | | | | |
| | | gpio_125 | 4 | IO | | | | | | | | |
| | | uart2_tx | 5 | O | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| Y20 | NA | hsusb0_data1 | 0 | IO | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | uart3_rx_irrx | 2 | I | | | | | | | | |
| | | gpio_130 | 4 | IO | | | | | | | | |
| | | uart2_rx | 5 | I | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| V18 | NA | hsusb0_data2 | 0 | IO | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | uart3_rts_sd | 2 | O | | | | | | | | |
| | | gpio_131 | 4 | IO | | | | | | | | |
| | | uart2_rts | 5 | O | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| W20 | NA | hsusb0_data3 | 0 | IO | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | uart3_cts_rctx | 2 | IO | | | | | | | | |
| | | gpio_169 | 4 | IO | | | | | | | | |
| | | uart2_cts | 5 | I | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| W17 | NA | hsusb0_data4 | 0 | IO | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | gpio_188 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| Y18 | NA | hsusb0_data5 | 0 | IO | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | gpio_189 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| Y19 | NA | hsusb0_data6 | 0 | IO | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | gpio_190 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| Y17 | NA | hsusb0_data7 | 0 | IO | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | gpio_191 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| V19 | NA | hsusb0_dir | 0 | I | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | gpio_122 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| W18 | NA | hsusb0_nxt | 0 | I | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | gpio_124 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| U20 | NA | hsusb0_stp | 0 | O | H | H | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | gpio_121 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| U15 | NA | jtag_ntrst | 0 | I | L | L | 0 | vdds | Yes | NA | PU/ PD | LVCMOS |
| W13 | NA | jtag_rtck | 0 | O | L | 0 | 0 | vdds | NA | 4 | PU/ PD | LVCMOS |
| V14 | NA | jtag_tck | 0 | I | L | L | 0 | vdds | Yes | NA | PU/ PD | LVCMOS |
| U16 | NA | jtag_tdi | 0 | I | H | H | 0 | vdds | Yes | NA | PU/ PD | LVCMOS |
| Y13 | NA | jtag_tdo | 0 | O | L | Z | 0 | vdds | NA | 4 | PU/ PD | LVCMOS |
| V15 | NA | jtag_tms_tmsc | 0 | IO | H | H | 0 | vdds | Yes | 4 | PU/ PD | LVCMOS |

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Product Folder Link(s): *DM3730  DM3725*

## Table 2-2. Ball Characteristics (CBC Pkg.)[5] (continued)

| BALL BOTTOM [1] | BALL TOP [1] | PIN NAME [2] | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | POWER [8] | HYS [9] | BUFFER STRENGTH (mA) [10] | PULLUP /DOWN TYPE [11] | IO CELL [12] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| N19 | NA | mmc1_clk | 0 | O | L | L | 7 | vdds_mmc1(13) | Yes | 1 | PU/ PD(3) | LVCMOS |
| | | gpio_120(8) | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| L18 | NA | mmc1_cmd | 0 | IO | L | L | 7 | vdds_mmc1(13) | Yes | 1 | PU/ PD(3) | LVCMOS |
| | | gpio_121(8) | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| M19 | NA | mmc1_dat0 | 0 | IO | L | L | 7 | vdds_mmc1(13) | Yes | 1 | PU/ PD(3) | LVCMOS |
| | | gpio_122(8) | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| M18 | NA | mmc1_dat1 | 0 | IO | L | L | 7 | vdds_mmc1(13) | Yes | 1 | PU/ PD(3) | LVCMOS |
| | | gpio_123(8) | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| K18 | NA | mmc1_dat2 | 0 | IO | L | L | 7 | vdds_mmc1(13) | Yes | 1 | PU/ PD(3) | LVCMOS |
| | | gpio_124(8) | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| N20 | NA | mmc1_dat3 | 0 | IO | L | L | 7 | vdds_mmc1(13) | Yes | 1 | PU/ PD(3) | LVCMOS |
| | | gpio_125(8) | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| M20 | NA | gpio_126(8) | 4 | IO | L | L | 7 | vdds_x | Yes | 1 | PU/PD(3) | LVCMOS |
| | | safe_mode | 7 | - | | | | | | | | |
| P17 | NA | gpio_127(8) | 4 | IO | L | L | 7 | vdds_x | Yes | 1 | PU/PD(3) | LVCMOS |
| | | safe_mode | 7 | - | | | | | | | | |
| P18 | NA | gpio_128 | 4 | IO | L | L | 7 | vdds | Yes | 4 | PU/PD | LVCMOS |
| | | safe_mode | 7 | - | | | | | | | | |
| P19 | NA | gpio_129(8) | 4 | IO | L | L | 7 | vdds_x | Yes | 1 | PU/PD (3) | LVCMOS |
| | | safe_mode | 7 | - | | | | | | | | |
| J25 | NA | i2c1_scl | 0 | OD | H | H | 0 | vdds | NA | 3 | PU/ PD(9) (10) | Open Drain |
| J24 | NA | i2c1_sda | 0 | IOD | H | H | 0 | vdds | Yes | 3 | PU/ PD(9) (10) | LVCMOS Open Drain |
| C2 | NA | i2c2_scl | 0 | OD | H | H | 7 | vdds | Yes | 3 | PU/ PD(9)(11) | LVCMOS Open Drain |
| | | gpio_168 | 4 | IO | | | | | | 4 | | |
| | | safe_mode | 7 | - | | | | | | 4 | | |
| C1 | NA | i2c2_sda | 0 | IOD | H | H | 7 | vdds | Yes | 3 | PU/ PD(9)(11) | LVCMOS Open Drain |
| | | gpio_183 | 4 | IO | | | | | | 4 | | |
| | | safe_mode | 7 | - | | | | | | 4 | | |
| AB4 | NA | i2c3_scl | 0 | OD | H | H | 7 | vdds | Yes | 3 | PU/ PD(9)(11) | LVCMOS Open Drain |
| | | gpio_184 | 4 | IO | | | | | | 4 | | |
| | | safe_mode | 7 | - | | | | | | 4 | | |
| AC4 | NA | i2c3_sda | 0 | IOD | H | H | 7 | vdds | Yes | 3 | PU/ PD(9)(11) | LVCMOS Open Drain |
| | | gpio_185 | 4 | IO | | | | | | 4 | | |
| | | safe_mode | 7 | - | | | | | | 4 | | |
| U19 | NA | mcbsp1_clkr | 0 | IO | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | mcspi4_clk | 1 | IO | | | | | | | | |
| | | gpio_156 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| T17 | NA | mcbsp1_clkx | 0 | IO | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | mcbsp3_clkx | 2 | IO | | | | | | | | |
| | | gpio_162 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |

## Table 2-2. Ball Characteristics (CBC Pkg.)[5] (continued)

| BALL BOTTOM [1] | BALL TOP [1] | PIN NAME [2] | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | POWER [8] | HYS [9] | BUFFER STRENGTH (mA) [10] | PULLUP /DOWN TYPE [11] | IO CELL [12] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| T20 | NA | mcbsp1_dr | 0 | I | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
|  |  | mcspi4_somi | 1 | IO |  |  |  |  |  |  |  |  |
|  |  | mcbsp3_dr | 2 | I |  |  |  |  |  |  |  |  |
|  |  | gpio_159 | 4 | IO |  |  |  |  |  |  |  |  |
|  |  | safe_mode | 7 | - |  |  |  |  |  |  |  |  |
| U17 | NA | mcbsp1_dx | 0 | IO | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
|  |  | mcspi4_simo | 1 | IO |  |  |  |  |  |  |  |  |
|  |  | mcbsp3_dx | 2 | IO |  |  |  |  |  |  |  |  |
|  |  | gpio_158 | 4 | IO |  |  |  |  |  |  |  |  |
|  |  | safe_mode | 7 | - |  |  |  |  |  |  |  |  |
| V17 | NA | mcbsp1_fsr | 0 | IO | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
|  |  | cam_global_reset | 2 | IO |  |  |  |  |  |  |  |  |
|  |  | gpio_157 | 4 | IO |  |  |  |  |  |  |  |  |
|  |  | safe_mode | 7 | - |  |  |  |  |  |  |  |  |
| P20 | NA | mcbsp1_fsx | 0 | IO | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
|  |  | mcspi4_cs0 | 1 | IO |  |  |  |  |  |  |  |  |
|  |  | mcbsp3_fsx | 2 | IO |  |  |  |  |  |  |  |  |
|  |  | gpio_161 | 4 | IO |  |  |  |  |  |  |  |  |
|  |  | safe_mode | 7 | - |  |  |  |  |  |  |  |  |
| R18 | NA | mcbsp2_clkx | 0 | IO | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
|  |  | gpio_117 | 4 | IO |  |  |  |  |  |  |  |  |
|  |  | safe_mode | 7 | - |  |  |  |  |  |  |  |  |
| T18 | NA | mcbsp2_dr | 0 | I | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
|  |  | gpio_118 | 4 | IO |  |  |  |  |  |  |  |  |
|  |  | safe_mode | 7 | - |  |  |  |  |  |  |  |  |
| R19 | NA | mcbsp2_dx | 0 | IO | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
|  |  | gpio_119 | 4 | IO |  |  |  |  |  |  |  |  |
|  |  | safe_mode | 7 | - |  |  |  |  |  |  |  |  |
| U18 | NA | mcbsp2_fsx | 0 | IO | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
|  |  | gpio_116 | 4 | IO |  |  |  |  |  |  |  |  |
|  |  | safe_mode | 7 | - |  |  |  |  |  |  |  |  |
| P9 | NA | mcspi1_clk | 0 | IO | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
|  |  | mmc2_dat4 | 1 | IO |  |  |  |  |  |  |  |  |
|  |  | gpio_171 | 4 | IO |  |  |  |  |  |  |  |  |
|  |  | safe_mode | 7 | - |  |  |  |  |  |  |  |  |
| R7 | NA | mcspi1_cs0 | 0 | IO | H | H | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
|  |  | mmc2_dat7 | 1 | IO |  |  |  |  |  |  |  |  |
|  |  | gpio_174 | 4 | IO |  |  |  |  |  |  |  |  |
|  |  | safe_mode | 7 | - |  |  |  |  |  |  |  |  |
| R9 | NA | mcspi1_cs2 | 0 | O | H | H | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
|  |  | mmc3_clk | 3 | O |  |  |  |  |  |  |  |  |
|  |  | gpio_176 | 4 | IO |  |  |  |  |  |  |  |  |
|  |  | safe_mode | 7 | - |  |  |  |  |  |  |  |  |
| P8 | NA | mcspi1_simo | 0 | IO | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
|  |  | mmc2_dat5 | 1 | IO |  |  |  |  |  |  |  |  |
|  |  | gpio_172 | 4 | IO |  |  |  |  |  |  |  |  |
|  |  | safe_mode | 7 | - |  |  |  |  |  |  |  |  |
| P7 | NA | mcspi1_somi | 0 | IO | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
|  |  | mmc2_dat6 | 1 | IO |  |  |  |  |  |  |  |  |
|  |  | gpio_173 | 4 | IO |  |  |  |  |  |  |  |  |
|  |  | safe_mode | 7 | - |  |  |  |  |  |  |  |  |
| W7 | NA | mcspi2_clk | 0 | IO | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
|  |  | hsusb2_data7 | 3 | IO |  |  |  |  |  |  |  |  |
|  |  | gpio_178 | 4 | IO |  |  |  |  |  |  |  |  |
|  |  | safe_mode | 7 | - |  |  |  |  |  |  |  |  |

## Table 2-2. Ball Characteristics (CBC Pkg.)[5] (continued)

| BALL BOTTOM [1] | BALL TOP [1] | PIN NAME [2] | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | POWER [8] | HYS [9] | BUFFER STRENGTH (mA) [10] | PULLUP /DOWN TYPE [11] | IO CELL [12] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| V8 | NA | mcspi2_cs0 | 0 | IO | H | H | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | gpt_11_pwm_evt | 1 | IO | | | | | | | | |
| | | hsusb2_data6 | 3 | IO | | | | | | | | |
| | | gpio_181 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| W8 | NA | mcspi2_simo | 0 | IO | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | gpt_9_pwm_evt | 1 | IO | | | | | | | | |
| | | hsusb2_data4 | 3 | IO | | | | | | | | |
| | | gpio_179 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| U8 | NA | mcspi2_somi | 0 | IO | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | gpt_10_pwm_evt | 1 | IO | | | | | | | | |
| | | hsusb2_data5 | 3 | IO | | | | | | | | |
| | | gpio_180 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| W10 | NA | mmc2_clk | 0 | O | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | mcspi3_clk | 1 | IO | | | | | | | | |
| | | gpio_130 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| R10 | NA | mmc2_cmd | 0 | IO | H | H | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | mcspi3_simo | 1 | IO | | | | | | | | |
| | | gpio_131 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| T10 | NA | mmc2_dat0 | 0 | IO | H | H | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | mcspi3_somi | 1 | IO | | | | | | | | |
| | | gpio_132 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| T9 | NA | mmc2_dat1 | 0 | IO | H | H | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | gpio_133 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| U10 | NA | mmc2_dat2 | 0 | IO | H | H | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | mcspi3_cs1 | 1 | O | | | | | | | | |
| | | gpio_134 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| U9 | NA | mmc2_dat3 | 0 | IO | H | H | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | mcspi3_cs0 | 1 | IO | | | | | | | | |
| | | gpio_135 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| V10 | NA | mmc2_dat4 | 0 | IO | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | mmc2_dir_dat0 | 1 | O | | | | | | | | |
| | | mmc3_dat0 | 3 | IO | | | | | | | | |
| | | gpio_136 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| R2 | NA | uart1_rts | 0 | O | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | gpio_149 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| H3 | NA | uart1_rx | 0 | I | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | mcbsp1_clkr | 2 | IO | | | | | | | | |
| | | mcspi4_clk | 3 | IO | | | | | | | | |
| | | gpio_151 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| L4 | NA | uart1_tx | 0 | O | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | gpio_148 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| Y24 | NA | uart2_cts | 0 | I | H | H | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |

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## Table 2-2. Ball Characteristics (CBC Pkg.)[5] (continued)

| BALL BOTTOM [1] | BALL TOP [1] | PIN NAME [2] | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | POWER [8] | HYS [9] | BUFFER STRENGTH (mA) [10] | PULLUP /DOWN TYPE [11] | IO CELL [12] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | mcbsp3_dx | 1 | IO | | | | | | | | |
| | | gpt_9_pwm_evt | 2 | IO | | | | | | | | |
| | | gpio_144 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| AA24 | NA | uart2_rts | 0 | O | H | H | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | mcbsp3_dr | 1 | I | | | | | | | | |
| | | gpt_10_pwm_evt | 2 | IO | | | | | | | | |
| | | gpio_145 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| AD21 | NA | uart2_rx | 0 | I | H | H | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | mcbsp3_fsx | 1 | IO | | | | | | | | |
| | | gpt_8_pwm_evt | 2 | IO | | | | | | | | |
| | | gpio_147 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| AD22 | NA | uart2_tx | 0 | O | H | H | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | mcbsp3_clkx | 1 | IO | | | | | | | | |
| | | gpt_11_pwm_evt | 2 | IO | | | | | | | | |
| | | gpio_146 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| F23 | NA | uart3_cts_rctx | 0 | IO | H | H | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | gpio_163 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| F24 | NA | uart3_rts_sd | 0 | O | H | H | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | gpio_164 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| H24 | NA | uart3_rx_irrx | 0 | I | H | H | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | gpio_165 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| G24 | NA | uart3_tx_irtx | 0 | O | H | H | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | gpio_166 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| J23 | NA | hdq_sio | 0 | IOD | H | H | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS Open Drain |
| | | sys_altclk | 1 | I | | | | | | | | |
| | | i2c2_sccbe | 2 | OD | | | | | | | | |
| | | i2c3_sccbe | 3 | OD | | | | | | | | |
| | | gpio_170 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| AD15 | NA | i2c4_scl | 0 | OD | H | H | 0 | vdds | Yes | 3 | PU/ PD[9] [10] | LVCMOS Open Drain |
| | | sys_nvmode1 | 1 | O | | | | | | 4 | | |
| | | safe_mode | 7 | - | | | | | | 4 | | |
| W16 | NA | i2c4_sda | 0 | IOD | H | H | 0 | vdds | Yes | 3 | PU/ PD[9] [10] | LVCMOS Open Drain |
| | | sys_nvmode2 | 1 | O | | | | | | 4 | | |
| | | safe_mode | 7 | - | | | | | | 4 | | |
| F3 | NA | sys_boot0 | 0 | I | Z | Z | 0 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| | | dss_data18 | 3 | IO | | | | | | | | |
| | | gpio_2 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| D3 | NA | sys_boot1 | 0 | I | Z | Z | 0 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| | | dss_data19 | 3 | IO | | | | | | | | |
| | | gpio_3 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| C3 | NA | sys_boot2 | 0 | I | Z | Z | 0 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| | | gpio_4 | 4 | IO | | | | | | | | |

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Product Folder Link(s): *DM3730  DM3725*

## Table 2-2. Ball Characteristics (CBC Pkg.)(5) (continued)

| BALL BOTTOM [1] | BALL TOP [1] | PIN NAME [2] | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | POWER [8] | HYS [9] | BUFFER STRENGTH (mA) [10] | PULLUP /DOWN TYPE [11] | IO CELL [12] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | safe_mode | 7 | - | | | | | | | | |
| E3 | NA | sys_boot3 | 0 | I | Z | Z | 0 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| | | dss_data20 | 3 | O | | | | | | | | |
| | | gpio_5 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| E4 | NA | sys_boot4 | 0 | I | Z | Z | 0 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| | | mmc2_dir_dat2 | 1 | O | | | | | | | | |
| | | dss_data21 | 3 | O | | | | | | | | |
| | | gpio_6 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| G3 | NA | sys_boot5 | 0 | I | Z | Z | 0 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| | | mmc2_dir_dat3 | 1 | O | | | | | | | | |
| | | dss_data22 | 3 | O | | | | | | | | |
| | | gpio_7 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| D4 | NA | sys_boot6 | 0 | I | Z | Z | 0 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| | | dss_data23 | 3 | O | | | | | | | | |
| | | gpio_8 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| AE14 | NA | sys_clkout1 | 0 | O | L | L | 7(12) | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | gpio_10 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| W11 | NA | sys_clkout2 | 0 | O | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | gpio_186 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| W15 | NA | sys_clkreq | 0 | IO | 0 | see (7) | 0 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | gpio_1 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| V16 | NA | sys_nirq | 0 | I | H | H | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | gpio_0 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| V13 | NA | sys_nrespwron | 0 | I | Z | Z | 0 | vdds | Yes | NA | No | LVCMOS |
| AD7 | AA5 | sys_nreswarm | 0 | IOD | 0 | H | 0 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | gpio_30 | 4 | IO | | | | | | | | Open Drain |
| | | safe_mode | 7 | - | | | | | | | | |
| V12 | NA | sys_off_mode | 0 | O | 0 | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | gpio_9 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| AF19 | NA | sys_xtalin | 0 | AI | Z | Z | 0 | vdds | Yes | NA | NA | LVCMOS Analog |
| AF20 | NA | sys_xtalout | 0 | AO | Z | 0 | 0 | vdds | NA | NA | NA | Analog |
| W26 | NA | cvideo1_out | 0 | AO | 0 | 0 | 0 | vdda_dac | NA | NA | NA | 10-bit DAC |
| V26 | NA | cvideo2_out | 0 | AO | 0 | 0 | 0 | vdda_dac | NA | NA | NA | 10-bit DAC |
| W25 | NA | cvideo1_vfb | 0 | AO | 0 | NA | 0 | vdda_dac | NA | NA | NA | 10-bit DAC |
| U24 | NA | cvideo2_vfb | 0 | AO | 0 | NA | 0 | vdda_dac | NA | NA | NA | 10-bit DAC |
| V23 | NA | cvideo1_rset | 0 | AIO | Z | NA | 0 | vdda_dac | No | NA | NA | 10-bit DAC |
| AE20 | NA | sys_32k | 0 | I | Z | Z | 0 | vdds | Yes | NA | PU/ PD | LVCMOS |
| A24 | NA | cam_d2 | 0 | I | L | L | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| | | gpio_101 | 4 | IO | | | | | | | | |
| | | hw_dbg4 | 5 | O | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| B24 | NA | cam_d3 | 0 | I | L | L | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| | | gpio_102 | 4 | IO | | | | | | | | |
| | | hw_dbg5 | 5 | O | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |

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## Table 2-2. Ball Characteristics (CBC Pkg.)[5] (continued)

| BALL BOTTOM [1] | BALL TOP [1] | PIN NAME [2] | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | POWER [8] | HYS [9] | BUFFER STRENGTH (mA) [10] | PULLUP /DOWN TYPE [11] | IO CELL [12] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| D24 | NA | cam_d4 | 0 | I | L | L | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| | | gpio_103 | 4 | IO | | | | | | | | |
| | | hw_dbg6 | 5 | O | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| C24 | NA | cam_d5 | 0 | I | L | L | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| | | gpio_104 | 4 | IO | | | | | | | | |
| | | hw_dbg7 | 5 | O | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| D25 | NA | cam_d10 | 0 | I | L | L | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| | | gpio_109 | 4 | IO | | | | | | | | |
| | | hw_dbg8 | 5 | O | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| E26 | NA | cam_d11 | 0 | I | L | L | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| | | gpio_110 | 4 | IO | | | | | | | | |
| | | hw_dbg9 | 5 | O | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| B23 | NA | cam_fld | 0 | IO | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | cam_global_reset | 2 | IO | | | | | | | | |
| | | gpio_98 | 4 | IO | | | | | | | | |
| | | hw_dbg3 | 5 | O | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| C23 | NA | cam_hs | 0 | IO | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | gpio_94 | 4 | IO | | | | | | | | |
| | | hw_dbg0 | 5 | O | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| C26 | NA | cam_pclk | 0 | I | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | gpio_97 | 4 | IO | | | | | | | | |
| | | hw_dbg2 | 5 | O | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| D26 | NA | cam_strobe | 0 | O | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | gpio_126 | 4 | IO | | | | | | | | |
| | | hw_dbg11 | 5 | O | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| C25 | NA | cam_xclka | 0 | O | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | gpio_96 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| E25 | NA | cam_xclkb | 0 | O | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | gpio_111 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| P25 | NA | cam_d6 | 0 | I | L | L | 7 | vdds | Yes | NA | PU/ PD | SubLVDS |
| | | gpio_105 | 4 | I | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| P26 | NA | cam_d7 | 0 | I | L | L | 7 | vdds | Yes | NA | PU/ PD | SubLVDS |
| | | gpio_106 | 4 | I | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| N25 | NA | cam_d8 | 0 | I | L | L | 7 | vdds | NA | NA | PU/ PD | SubLVDS |
| | | gpio_107 | 4 | I | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| N26 | NA | cam_d9 | 0 | I | L | L | 7 | vdds | NA | NA | PU/ PD | SubLVDS |
| | | gpio_108 | 4 | I | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| D23 | NA | cam_vs | 0 | IO | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | gpio_95 | 4 | IO | | | | | | | | |
| | | hw_dbg1 | 5 | O | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |

## Table 2-2. Ball Characteristics (CBC Pkg.)[5] (continued)

| BALL BOTTOM [1] | BALL TOP [1] | PIN NAME [2] | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | POWER [8] | HYS [9] | BUFFER STRENGTH (mA) [10] | PULLUP /DOWN TYPE [11] | IO CELL [12] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A23 | NA | cam_wen | 0 | I | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
|  |  | cam_shutter | 2 | O |  |  |  |  |  |  |  |  |
|  |  | gpio_167 | 4 | IO |  |  |  |  |  |  |  |  |
|  |  | hw_dbg10 | 5 | O |  |  |  |  |  |  |  |  |
|  |  | safe_mode | 7 | - |  |  |  |  |  |  |  |  |
| F26 | NA | dss_acbias | 0 | O | L | L | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
|  |  | gpio_69 | 4 | IO |  |  |  |  |  |  |  |  |
|  |  | safe_mode | 7 | - |  |  |  |  |  |  |  |  |
| G26 | NA | dss_data6 | 0 | IO | L | L | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
|  |  | uart1_tx | 2 | O |  |  |  |  |  |  |  |  |
|  |  | gpio_76 | 4 | IO |  |  |  |  |  |  |  |  |
|  |  | hw_dbg14 | 5 | O |  |  |  |  |  |  |  |  |
|  |  | safe_mode | 7 | - |  |  |  |  |  |  |  |  |
| H25 | NA | dss_data7 | 0 | IO | L | L | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
|  |  | uart1_rx | 2 | I |  |  |  |  |  |  |  |  |
|  |  | gpio_77 | 4 | IO |  |  |  |  |  |  |  |  |
|  |  | hw_dbg15 | 5 | O |  |  |  |  |  |  |  |  |
|  |  | safe_mode | 7 | - |  |  |  |  |  |  |  |  |
| H26 | NA | dss_data8 | 0 | IO | L | L | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
|  |  | uart3_rx_irrx | 2 | I |  |  |  |  |  |  |  |  |
|  |  | gpio_78 | 4 | IO |  |  |  |  |  |  |  |  |
|  |  | hw_dbg16 | 5 | O |  |  |  |  |  |  |  |  |
|  |  | safe_mode | 7 | - |  |  |  |  |  |  |  |  |
| J26 | NA | dss_data9 | 0 | IO | L | L | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
|  |  | uart3_tx_irtx | 2 | O |  |  |  |  |  |  |  |  |
|  |  | gpio_79 | 4 | IO |  |  |  |  |  |  |  |  |
|  |  | hw_dbg17 | 5 | O |  |  |  |  |  |  |  |  |
|  |  | safe_mode | 7 | - |  |  |  |  |  |  |  |  |
| L25 | NA | dss_data16 | 0 | IO | L | L | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
|  |  | gpio_86 | 4 | IO |  |  |  |  |  |  |  |  |
|  |  | safe_mode | 7 | - |  |  |  |  |  |  |  |  |
| L26 | NA | dss_data17 | 0 | IO | L | L | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
|  |  | gpio_87 | 4 | IO |  |  |  |  |  |  |  |  |
|  |  | safe_mode | 7 | - |  |  |  |  |  |  |  |  |
| M24 | NA | dss_data18 | 0 | IO | L | L | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
|  |  | mcspi3_clk | 2 | IO |  |  |  |  |  |  |  |  |
|  |  | dss_data0 | 3 | IO |  |  |  |  |  |  |  |  |
|  |  | gpio_88 | 4 | IO |  |  |  |  |  |  |  |  |
|  |  | safe_mode | 7 | - |  |  |  |  |  |  |  |  |
| M26 | NA | dss_data19 | 0 | IO | L | L | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
|  |  | mcspi3_simo | 2 | IO |  |  |  |  |  |  |  |  |
|  |  | dss_data1 | 3 | IO |  |  |  |  |  |  |  |  |
|  |  | gpio_89 | 4 | IO |  |  |  |  |  |  |  |  |
|  |  | safe_mode | 7 | - |  |  |  |  |  |  |  |  |
| N24 | NA | dss_data21 | 0 | O | L | L | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
|  |  | mcspi3_cs0 | 2 | IO |  |  |  |  |  |  |  |  |
|  |  | dss_data3 | 3 | IO |  |  |  |  |  |  |  |  |
|  |  | gpio_91 | 4 | IO |  |  |  |  |  |  |  |  |
|  |  | safe_mode | 7 | - |  |  |  |  |  |  |  |  |
| K24 | NA | dss_hsync | 0 | O | H | H | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
|  |  | gpio_67 | 4 | IO |  |  |  |  |  |  |  |  |
|  |  | hw_dbg13 | 5 | O |  |  |  |  |  |  |  |  |
|  |  | safe_mode | 7 | - |  |  |  |  |  |  |  |  |
| M25 | NA | dss_vsync | 0 | O | H | H | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
|  |  | gpio_68 | 4 | IO |  |  |  |  |  |  |  |  |

Product Folder Link(s): DM3730  DM3725

### Table 2-2. Ball Characteristics (CBC Pkg.)[5] (continued)

| BALL BOTTOM [1] | BALL TOP [1] | PIN NAME [2] | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | POWER [8] | HYS [9] | BUFFER STRENGTH (mA) [10] | PULLUP /DOWN TYPE [11] | IO CELL [12] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | safe_mode | 7 | - | | | | | | | | |
| R8 | NA | mcspi1_cs1 | 0 | O | H | H | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | mmc3_cmd | 3 | IO | | | | | | | | |
| | | gpio_175 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| T8 | NA | mcspi1_cs3 | 0 | O | H | H | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | hsusb2_data2 | 3 | IO | | | | | | | | |
| | | gpio_177 | 4 | IO | | | | | | | | |
| | | mm2_txdat | 5 | IO | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| V9 | NA | mcspi2_cs1 | 0 | O | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | gpt_8_pwm_evt | 1 | IO | | | | | | | | |
| | | hsusb2_data3 | 3 | IO | | | | | | | | |
| | | gpio_182 | 4 | IO | | | | | | | | |
| | | mm2_txen_n | 5 | IO | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| T19 | NA | mcbsp_clks | 0 | I | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | cam_shutter | 2 | O | | | | | | | | |
| | | gpio_160 | 4 | IO | | | | | | | | |
| | | uart1_cts | 5 | I | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| AB2 | NA | etk_clk | 0 | O | H | H | 4 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | mcbsp5_clkx | 1 | IO | | | | | | | | |
| | | mmc3_clk | 2 | O | | | | | | | | |
| | | hsusb1_stp | 3 | O | | | | | | | | |
| | | gpio_12 | 4 | IO | | | | | | | | |
| | | mm1_rxdp | 5 | IO | | | | | | | | |
| | | hw_dbg0 | 7 | O | | | | | | | | |
| AB3 | NA | etk_ctl | 0 | O | H | H | 4 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | mmc3_cmd | 2 | IO | | | | | | | | |
| | | hsusb1_clk | 3 | O | | | | | | | | |
| | | gpio_13 | 4 | IO | | | | | | | | |
| | | hw_dbg1 | 7 | O | | | | | | | | |
| AC3 | NA | etk_d0 | 0 | O | H | H | 4 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | mcspi3_simo | 1 | IO | | | | | | | | |
| | | mmc3_dat4 | 2 | IO | | | | | | | | |
| | | hsusb1_data0 | 3 | IO | | | | | | | | |
| | | gpio_14 | 4 | IO | | | | | | | | |
| | | mm1_rxrcv | 5 | IO | | | | | | | | |
| | | hw_dbg2 | 7 | O | | | | | | | | |
| AD4 | NA | etk_d1 | 0 | O | H | H | 4 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | mcspi3_somi | 1 | IO | | | | | | | | |
| | | hsusb1_data1 | 3 | IO | | | | | | | | |
| | | gpio_15 | 4 | IO | | | | | | | | |
| | | mm1_txse0 | 5 | IO | | | | | | | | |
| | | hw_dbg3 | 7 | O | | | | | | | | |
| AD3 | NA | etk_d2 | 0 | O | H | H | 4 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | mcspi3_cs0 | 1 | IO | | | | | | | | |
| | | hsusb1_data2 | 3 | IO | | | | | | | | |
| | | gpio_16 | 4 | IO | | | | | | | | |
| | | mm1_txdat | 5 | IO | | | | | | | | |
| | | hw_dbg4 | 7 | O | | | | | | | | |
| AA3 | NA | etk_d3 | 0 | O | H | H | 4 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | mcspi3_clk | 1 | IO | | | | | | | | |
| | | mmc3_dat3 | 2 | IO | | | | | | | | |

**Table 2-2. Ball Characteristics (CBC Pkg.)[5] (continued)**

| BALL BOTTOM [1] | BALL TOP [1] | PIN NAME [2] | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | POWER [8] | HYS [9] | BUFFER STRENGTH (mA) [10] | PULLUP /DOWN TYPE [11] | IO CELL [12] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | hsusb1_data7 | 3 | IO | | | | | | | | |
| | | gpio_17 | 4 | IO | | | | | | | | |
| | | hw_dbg5 | 7 | O | | | | | | | | |
| Y3 | NA | etk_d4 | 0 | O | L | L | 4 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | mcbsp5_dr | 1 | I | | | | | | | | |
| | | mmc3_dat0 | 2 | IO | | | | | | | | |
| | | hsusb1_data4 | 3 | IO | | | | | | | | |
| | | gpio_18 | 4 | IO | | | | | | | | |
| | | hw_dbg6 | 7 | O | | | | | | | | |
| AB1 | NA | etk_d5 | 0 | O | L | L | 4 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | mcbsp5_fsx | 1 | IO | | | | | | | | |
| | | mmc3_dat1 | 2 | IO | | | | | | | | |
| | | hsusb1_data5 | 3 | IO | | | | | | | | |
| | | gpio_19 | 4 | IO | | | | | | | | |
| | | hw_dbg7 | 7 | O | | | | | | | | |
| AE3 | NA | etk_d6 | 0 | O | L | L | 4 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | mcbsp5_dx | 1 | O | | | | | | | | |
| | | mmc3_dat2 | 2 | IO | | | | | | | | |
| | | hsusb1_data6 | 3 | IO | | | | | | | | |
| | | gpio_20 | 4 | IO | | | | | | | | |
| | | hw_dbg8 | 7 | O | | | | | | | | |
| AD2 | NA | etk_d7 | 0 | O | L | L | 4 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | mcspi3_cs1 | 1 | O | | | | | | | | |
| | | mmc3_dat7 | 2 | IO | | | | | | | | |
| | | hsusb1_data3 | 3 | IO | | | | | | | | |
| | | gpio_21 | 4 | IO | | | | | | | | |
| | | mm1_txen_n | 5 | IO | | | | | | | | |
| | | hw_dbg9 | 7 | O | | | | | | | | |
| AA4 | NA | etk_d8 | 0 | O | L | L | 4 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | mmc3_dat6 | 2 | IO | | | | | | | | |
| | | hsusb1_dir | 3 | I | | | | | | | | |
| | | gpio_22 | 4 | IO | | | | | | | | |
| | | hw_dbg10 | 7 | O | | | | | | | | |
| V2 | NA | etk_d9 | 0 | O | L | L | 4 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | mmc3_dat5 | 2 | IO | | | | | | | | |
| | | hsusb1_nxt | 3 | I | | | | | | | | |
| | | gpio_23 | 4 | IO | | | | | | | | |
| | | mm1_rxdm | 5 | IO | | | | | | | | |
| | | hw_dbg11 | 7 | O | | | | | | | | |
| AE4 | NA | etk_d10 | 0 | O | L | L | 4 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | uart1_rx | 2 | I | | | | | | | | |
| | | hsusb2_clk | 3 | O | | | | | | | | |
| | | gpio_24 | 4 | IO | | | | | | | | |
| | | hw_dbg12 | 7 | O | | | | | | | | |
| AF6 | NA | etk_d11 | 0 | O | L | L | 4 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | hsusb2_stp | 3 | O | | | | | | | | |
| | | gpio_25 | 4 | IO | | | | | | | | |
| | | mm2_rxdp | 5 | IO | | | | | | | | |
| | | hw_dbg13 | 7 | O | | | | | | | | |
| AE6 | NA | etk_d12 | 0 | O | L | L | 4 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | hsusb2_dir | 3 | I | | | | | | | | |
| | | gpio_26 | 4 | IO | | | | | | | | |
| | | hw_dbg14 | 7 | O | | | | | | | | |
| AF7 | NA | etk_d13 | 0 | O | L | L | 4 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | hsusb2_nxt | 3 | I | | | | | | | | |

## Table 2-2. Ball Characteristics (CBC Pkg.)(5) (continued)

| BALL BOTTOM [1] | BALL TOP [1] | PIN NAME [2] | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | POWER [8] | HYS [9] | BUFFER STRENGTH (mA) [10] | PULLUP /DOWN TYPE [11] | IO CELL [12] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | gpio_27 | 4 | IO | | | | | | | | |
| | | mm2_rxdm | 5 | IO | | | | | | | | |
| | | hw_dbg15 | 7 | O | | | | | | | | |
| AF9 | NA | etk_d14 | 0 | O | L | L | 4 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | hsusb2_data0 | 3 | IO | | | | | | | | |
| | | gpio_28 | 4 | IO | | | | | | | | |
| | | mm2_rxrcv | 5 | IO | | | | | | | | |
| | | hw_dbg16 | 7 | O | | | | | | | | |
| AE9 | NA | etk_d15 | 0 | O | L | L | 4 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | hsusb2_data1 | 3 | IO | | | | | | | | |
| | | gpio_29 | 4 | IO | | | | | | | | |
| | | mm2_txse0 | 5 | IO | | | | | | | | |
| | | hw_dbg17 | 7 | O | | | | | | | | |
| Y15 | NA | jtag_emu0 | 0 | IO | H | H | 0 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | gpio_11 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| Y14 | NA | jtag_emu1 | 0 | IO | H | H | 0 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | gpio_31 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| U3 | NA | mcbsp3_clkx | 0 | IO | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | uart2_tx | 1 | O | | | | | | | | |
| | | gpio_142 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| N3 | NA | mcbsp3_dr | 0 | I | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | uart2_rts | 1 | O | | | | | | | | |
| | | gpio_141 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| P3 | NA | mcbsp3_dx | 0 | IO | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | uart2_cts | 1 | I | | | | | | | | |
| | | gpio_140 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| W3 | NA | mcbsp3_fsx | 0 | IO | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | uart2_rx | 1 | I | | | | | | | | |
| | | gpio_143 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| V3 | NA | mcbsp4_clkx | 0 | IO | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | gpio_152 | 4 | IO | | | | | | | | |
| | | mm3_txse0 | 6 | IO | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| U4 | NA | mcbsp4_dr | 0 | I | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | gpio_153 | 4 | IO | | | | | | | | |
| | | mm3_rxrcv | 6 | IO | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| R3 | NA | mcbsp4_dx | 0 | IO | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | gpio_154 | 4 | IO | | | | | | | | |
| | | mm3_txdat | 6 | IO | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| T3 | NA | mcbsp4_fsx | 0 | IO | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | gpio_155 | 4 | IO | | | | | | | | |
| | | mm3_txen_n | 6 | IO | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| M3 | NA | mmc2_dat5 | 0 | IO | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | mmc2_dir_dat1 | 1 | O | | | | | | | | |
| | | cam_global_reset | 2 | IO | | | | | | | | |
| | | mmc3_dat1 | 3 | IO | | | | | | | | |

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## Table 2-2. Ball Characteristics (CBC Pkg.)[5] (continued)

| BALL BOTTOM [1] | BALL TOP [1] | PIN NAME [2] | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | POWER [8] | HYS [9] | BUFFER STRENGTH (mA) [10] | PULLUP /DOWN TYPE [11] | IO CELL [12] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | gpio_137 | 4 | IO | | | | | | | | |
| | | mm3_rxdp | 6 | IO | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| L3 | NA | mmc2_dat6 | 0 | IO | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | mmc2_dir_cmd | 1 | O | | | | | | | | |
| | | cam_shutter | 2 | O | | | | | | | | |
| | | mmc3_dat2 | 3 | IO | | | | | | | | |
| | | gpio_138 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| K3 | NA | mmc2_dat7 | 0 | IO | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | mmc2_clkin | 1 | I | | | | | | | | |
| | | mmc3_dat3 | 3 | IO | | | | | | | | |
| | | gpio_139 | 4 | IO | | | | | | | | |
| | | mm3_rxdm | 6 | IO | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| W2 | NA | uart1_cts | 0 | I | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | | gpio_150 | 4 | IO | | | | | | | | |
| | | safe_mode | 7 | - | | | | | | | | |
| AC16 | NA | vss | 0 | GND | | | | | | | | |
| AD18 | NA | vdds | 0 | PWR | | | | | | | | |
| L19 | NA | vss | 0 | GND | | | | | | | | |
| AC19 | NA | vss | 0 | GND | | | | | | | | |
| AD19 | NA | vdds | 0 | PWR | | | | | | | | |
| L20 | NA | vdds | 0 | PWR | | | | | | | | |
| P23 | NA | vdds_x | 0 | PWR | | | | | | | | |
| AE19 | NA | cap_vddu_array | 0 | PWR | | | | | | | | |
| AC21, D15, G11, G18, H20, M7, M17, R20, T7, Y8, Y12 | NA | vdd_core | 0 | PWR | - | - | - | - | - | - | - | - |
| D13, G9, G12, H7, K11, L9, M9, M10, N7, N8, P10, U7, U11, U13, V7, V11, W9, Y9, Y11 | NA | vdd_mpu_iva | 0 | PWR | - | - | - | - | - | - | - | - |
| A18, AC7, AC15, AC18, AC24, AD20, AE10, C11, D9, E24, G4, J15, J18, L7, L24, M4, T4, T24, W24, Y4, AB24 | A3, A15, B5, F2, F21, L20, W21 | vdds | 0 | PWR | - | - | - | - | - | - | - | - |
| U12 | NA | vdds_sram | 0 | PWR | - | - | - | - | - | - | - | - |
| K13 | NA | vdda_dplls_dll | 0 | PWR | - | - | - | - | - | - | - | - |
| U14 | NA | vdda_dpll_per | 0 | PWR | - | - | - | - | - | - | - | - |
| W14 | NA | vdda_wkup_bg_bb | 0 | PWR | - | - | - | - | - | - | - | - |
| N23 | NA | vdds_mmc1 | 0 | PWR | - | - | - | - | - | - | - | - |
| V25 | NA | vdda_dac | 0 | PWR | - | - | - | - | - | - | - | - |
| V24 | NA | vssa_dac | 0 | GND | - | - | - | - | - | - | - | - |

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## Table 2-2. Ball Characteristics (CBC Pkg.)[5] (continued)

| BALL BOTTOM [1] | BALL TOP [1] | PIN NAME [2] | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | POWER [8] | HYS [9] | BUFFER STRENGTH (mA) [10] | PULLUP /DOWN TYPE [11] | IO CELL [12] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A6, A8, A13, AB5, AB22, AC10, AD14, AD25, AE7, B2, B25, C12, D7, D10, D12, D14, D18, D20, E22, G1, G8, G10, G20, G23, H4, K1, K15, K25, L10, L17, L23, N4, N10, N17, R1, R4, R17, T23, U25, W1, W4, W23, Y7, Y10, Y16, Y26 | A7, A13, B14, C1, F1, F20, H2, H20, L21, M2, P20, R2, W20 Y6, Y11, AA7, AA16 | vss | 0 | GND | - | - | - | - | - | - | - | - |
| K14 | NA | cap_vddu_wkup_logic | 0 | PWR | - | - | - | - | - | - | - | - |
| A1, L1, T2, Y2, AE2, AF4, AF5, AF8, AF10, AF12, AF13, AF14, AF15, AF17, AF16, A20, AF21, AF18, AF24, AF22, A25, AE25, AF25, A26, B26, K26, U26, AE26, AF26 | A1, J1, N2, T2, W2, Y2, AA6, Y7, Y9, AA10, AA11, AA12, AA13, Y14, AA14, B16, Y17, AA17, Y19, AA19, A20, Y20, AA20, A21, B21, H21, P21, Y21, AA21 | Feed-Through Pins[4] | - | - | - | - | - | - | - | - | - | - |

## Table 2-2. Ball Characteristics (CBC Pkg.)[5] (continued)

| BALL BOTTOM [1] | BALL TOP [1] | PIN NAME [2] | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | POWER [8] | HYS [9] | BUFFER STRENGTH (mA) [10] | PULLUP /DOWN TYPE [11] | IO CELL [12] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A2, AF1, B1,D5, K23, A5, A7, A9, A10, A11, A12, A14, A15, A16, A17, A19, A21, A22, AA23, AB23, AC9, AC12, AC13, AC14, AC17, AC20, AC22, AC23, AD9, AD11, AD12, AD13, AE1, AE8, AE11, AE12, AE13, AF2, AF3, AF11, B7, B8, B9, B10, B11, B12, B13, B14, B15, B16, B17, B18, B19, B20, B21, B22, C7, C8, C9, C10, C13, C14, C15, C16, C17, C18, C19, C20, C21, C22, D8, D11, D16, D17, D19, D21, D22, E23, F4, G7, G13, G14, G15, G16, G17, G19, H8, H9, H10, H11, H12, H13, H14, H15, H16, H17, H18, H19, H23, J3, J4, J7, J8, J9, J10, J11, J12, J13, J14, J16, J17, J19, J20, K4, K7, K8, K9, K10, K12, K16, K17, K19, L8, M8, M23, N18, P2, P4, P24, R23, R24, R25, R26, T25, T26, U23, V4, W12, Y23 | A2, AA1, AA2,B1, B2, B20, Y1 | No Connect[2] | - | - | - | - | - | - | - | - | - | - |
| AF23 | NA | sys_xtalgnd | 0 | GND | | | | | | | | |
| A4 | NA | gpmc_a11 | 0 | O | L | L | 7 | vdds | Yes | 8 | PU/PD | LVCMOS |
|  |  | safe_mode | 7 | | | | | | | | | |
| D6 | NA | cap_vdd_bb_mpu_iva | 0 | PWR | | | | | | | | |
| N9 | NA | cap_vdd_sram_mpu_iva | 0 | PWR | | | | | | | | |
| K20 | NA | cap_vdd_sram_core | 0 | PWR | | | | | | | | |

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(1)  The drive strength of these IOs is set according to the programmable load range: 2 pF to 4 pF per default or 4 pF to 12 pF. For a full description of the drive strength programming, see the System Control Module chapter of the *AM/DM37x Multimedia Device Technical Reference Manual* (literature number SPRUGN4).

(2)  Pins labeled as "No connect" must be left unconnected. Any connections to these pins may result in unpredictable behavior.

(3)  PU = [50 to 100 kΩ] per default or [10 to 50 kΩ] according to the selected mode.
For a full description of the pull-up drive strength programming, see the PRG_SDMMC_PUSTRENGTH configuration register bit field in the System Control Module chapter of the *AM/DM37x Multimedia Device Technical Reference Manual* (literature number SPRUGN4).
PD: 30 to 150 kΩ.

(4)  These signals are feed-through balls. For more information, see Table 2-27.

(5)  NA in this table stands for "Not Applicable".

(6)  In the safe_mode_out1, the buffer is configured to drive 1.

(7)  Depending on the sys_clkreq direction the corresponding reset released state value can be:
  –  Z if sys_clkreq is used as input
  –  1 if sys_clkreq is used as output
For a full description of the sys_clkreq control, see Power, Reset, and Clock Management chapter of the *AM/DM37x Multimedia Device Technical Reference Manual* (literature number SPRUGN4).

(8)  The usage of this GPIO is strongly restricted. For more information, see the General-Purpose Interface chapter of the *AM/DM37x Multimedia Device Technical Reference Manual* (literature number SPRUGN4).

(9)  The pullup and pulldown can be either the standard LVCMOS 100-μA drive strength or the I2C pullup and pulldown described as follows: Nominal resistance = 1.66 kΩ in high-speed mode with a load range of 5 pF to 12 pF, 4.5 kΩ in standard / fast mode with a load range of 5 pF to 15 pF.

(10)  The default buffer configuration is High-Speed I2C point-to-point mode using internal pullup. For a full description of the pull drive strength programming, see prg_i2c1_pullupresx, prg_i2c1_lb1lb0, and prg_sr_pullupresx, prg_sr_lb bits of the CONTROL_PROG_IO1, CONTROL_PROG_IO_WKUP1 control modules in the System Control Module chapter of the *AM/DM37x Multimedia Device Technical Reference Manual* (literature number SPRUGN4) to modify the IO settings if required by the targeted interface application.

(11)  The default buffer configuration is standard LVCMOS mode (non-I2C). For a full description of the pull drive strength programming, see PADCONFS bits of CONTROL_PADCONF_X control modules (standard LVCMOS mode), or prg_i2c2_pullupresx, prg_i2c2_lb1lb0, and prg_i2c3_pullupresx, prg_i2c3_lb1lb0 bits of the CONTROL_PROG_IO2, CONTROL_PROG_IO3 control modules (I2C mode) in the System Control Module chapter of the *AM/DM37x Multimedia Device Technical Reference Manual* (literature number SPRUGN4) to modify the IO settings if required by the targeted interface application.

(12)  Mux0 if sys_boot6 is pulled down (clock master).

(13)  If MMC1 functional signals are enabled, vdds_mmc1 for MMC1 must be supplied by a dedicated power source.
If MMC1 functional signals are disabled, other multiplexed CMOS signals of the interface can be enabled. The interface can be supplied by the same power source as vdds. The vdds power source supplies the vdds_mmc1 ball.
If neither MMC1 functional balls or CMOS signals are enabled, the interface balls are left unconnected with its associated power supply (vdda/vssa) grounded.
For the corresponding setting of the PBIASLITEPWRDNZ0 bit, see the System Control Module / SCM Programming Model / Extended-Drain I/Os and PBIAS Cells Programming Guide section of the *AM/DM37x Multimedia Device Technical Reference Manual* (literature number SPRUGN4).

## Table 2-3. Ball Characteristics (CUS Pkg.)[1]

| BALL NUMBER [1] | PIN NAME [2] | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | POWER [8] | HYS [9] | BUFFER STRENGTH (mA) [10] | PULLUP /DOWN TYPE [11] | IO CELL [12] |
|---|---|---|---|---|---|---|---|---|---|---|---|
| D7 | sdrc_d0 | 0 | IO | L | Z | 0 | vdds_mem | Yes | 4[8] | PU/ PD | LVCMOS |
| C5 | sdrc_d1 | 0 | IO | L | Z | 0 | vdds_mem | Yes | 4[8] | PU/ PD | LVCMOS |
| C6 | sdrc_d2 | 0 | IO | L | Z | 0 | vdds_mem | Yes | 4[8] | PU/ PD | LVCMOS |
| B5 | sdrc_d3 | 0 | IO | L | Z | 0 | vdds_mem | Yes | 4[8] | PU/ PD | LVCMOS |
| D9 | sdrc_d4 | 0 | IO | L | Z | 0 | vdds_mem | Yes | 4[8] | PU/ PD | LVCMOS |
| D10 | sdrc_d5 | 0 | IO | L | Z | 0 | vdds_mem | Yes | 4[8] | PU/ PD | LVCMOS |
| C7 | sdrc_d6 | 0 | IO | L | Z | 0 | vdds_mem | Yes | 4[8] | PU/ PD | LVCMOS |
| B7 | sdrc_d7 | 0 | IO | L | Z | 0 | vdds_mem | Yes | 4[8] | PU/ PD | LVCMOS |
| B11 | sdrc_d8 | 0 | IO | L | Z | 0 | vdds_mem | Yes | 4[8] | PU/ PD | LVCMOS |
| C12 | sdrc_d9 | 0 | IO | L | Z | 0 | vdds_mem | Yes | 4[8] | PU/ PD | LVCMOS |
| B12 | sdrc_d10 | 0 | IO | L | Z | 0 | vdds_mem | Yes | 4[8] | PU/ PD | LVCMOS |
| D13 | sdrc_d11 | 0 | IO | L | Z | 0 | vdds_mem | Yes | 4[8] | PU/ PD | LVCMOS |
| C13 | sdrc_d12 | 0 | IO | L | Z | 0 | vdds_mem | Yes | 4[8] | PU/ PD | LVCMOS |
| B14 | sdrc_d13 | 0 | IO | L | Z | 0 | vdds_mem | Yes | 4[8] | PU/ PD | LVCMOS |
| A14 | sdrc_d14 | 0 | IO | L | Z | 0 | vdds_mem | Yes | 4[8] | PU/ PD | LVCMOS |
| B15 | sdrc_d15 | 0 | IO | L | Z | 0 | vdds_mem | Yes | 4[8] | PU/ PD | LVCMOS |
| C9 | sdrc_d16 | 0 | IO | L | Z | 0 | vdds_mem | Yes | 4[8] | PU/ PD | LVCMOS |

## Table 2-3. Ball Characteristics (CUS Pkg.)[1] (continued)

| BALL NUMBER [1] | PIN NAME [2] | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | POWER [8] | HYS [9] | BUFFER STRENGTH (mA) [10] | PULLUP /DOWN TYPE [11] | IO CELL [12] |
|---|---|---|---|---|---|---|---|---|---|---|---|
| E12 | sdrc_d17 | 0 | IO | L | Z | 0 | vdds_mem | Yes | 4[8] | PU/ PD | LVCMOS |
| B8 | sdrc_d18 | 0 | IO | L | Z | 0 | vdds_mem | Yes | 4[8] | PU/ PD | LVCMOS |
| B9 | sdrc_d19 | 0 | IO | L | Z | 0 | vdds_mem | Yes | 4[8] | PU/ PD | LVCMOS |
| C10 | sdrc_d20 | 0 | IO | L | Z | 0 | vdds_mem | Yes | 4[8] | PU/ PD | LVCMOS |
| B10 | sdrc_d21 | 0 | IO | L | Z | 0 | vdds_mem | Yes | 4[8] | PU/ PD | LVCMOS |
| D12 | sdrc_d22 | 0 | IO | L | Z | 0 | vdds_mem | Yes | 4[8] | PU/ PD | LVCMOS |
| E13 | sdrc_d23 | 0 | IO | L | Z | 0 | vdds_mem | Yes | 4[8] | PU/ PD | LVCMOS |
| E15 | sdrc_d24 | 0 | IO | L | Z | 0 | vdds_mem | Yes | 4[8] | PU/ PD | LVCMOS |
| D15 | sdrc_d25 | 0 | IO | L | Z | 0 | vdds_mem | Yes | 4[8] | PU/ PD | LVCMOS |
| C15 | sdrc_d26 | 0 | IO | L | Z | 0 | vdds_mem | Yes | 4[8] | PU/ PD | LVCMOS |
| B16 | sdrc_d27 | 0 | IO | L | Z | 0 | vdds_mem | Yes | 4[8] | PU/ PD | LVCMOS |
| C16 | sdrc_d28 | 0 | IO | L | Z | 0 | vdds_mem | Yes | 4[8] | PU/ PD | LVCMOS |
| D16 | sdrc_d29 | 0 | IO | L | Z | 0 | vdds_mem | Yes | 4[8] | PU/ PD | LVCMOS |
| B17 | sdrc_d30 | 0 | IO | L | Z | 0 | vdds_mem | Yes | 4[8] | PU/ PD | LVCMOS |
| B18 | sdrc_d31 | 0 | IO | L | Z | 0 | vdds_mem | Yes | 4 [8] | PU/ PD | LVCMOS |
| C18 | sdrc_ba0 | 0 | O | 0 | 0 | 0 | vdds_mem | NA | 4[8] | PU/ PD | LVCMOS |
| D18 | sdrc_ba1 | 0 | O | 0 | 0 | 0 | vdds_mem | NA | 4[8] | PU/ PD | LVCMOS |
| A4 | sdrc_a0 | 0 | O | 0 | 0 | 0 | vdds_mem | NA | 4[8] | PU/ PD | LVCMOS |
| B4 | sdrc_a1 | 0 | O | 0 | 0 | 0 | vdds_mem | NA | 4 [8] | PU/ PD | LVCMOS |
| D6 | sdrc_a2 | 0 | O | 0 | 0 | 0 | vdds_mem | NA | 4[8] | PU/ PD | LVCMOS |
| B3 | sdrc_a3 | 0 | O | 0 | 0 | 0 | vdds_mem | NA | 4[8] | PU/ PD | LVCMOS |
| B2 | sdrc_a4 | 0 | O | 0 | 0 | 0 | vdds_mem | NA | 4[8] | PU/ PD | LVCMOS |
| C3 | sdrc_a5 | 0 | O | 0 | 0 | 0 | vdds_mem | NA | 4[8] | PU/ PD | LVCMOS |
| E3 | sdrc_a6 | 0 | O | 0 | 0 | 0 | vdds_mem | NA | 4 [8] | PU/ PD | LVCMOS |
| F6 | sdrc_a7 | 0 | O | 0 | 0 | 0 | vdds_mem | NA | 4[8] | PU/ PD | LVCMOS |
| E10 | sdrc_a8 | 0 | O | 0 | 0 | 0 | vdds_mem | NA | 4[8] | PU/ PD | LVCMOS |
| E9 | sdrc_a9 | 0 | O | 0 | 0 | 0 | vdds_mem | NA | 4[8] | PU/ PD | LVCMOS |
| E7 | sdrc_a10 | 0 | O | 0 | 0 | 0 | vdds_mem | NA | 4[8] | PU/ PD | LVCMOS |
| G6 | sdrc_a11 | 0 | O | 0 | 0 | 0 | vdds_mem | NA | 4[8] | PU/ PD | LVCMOS |
| G7 | sdrc_a12 | 0 | O | 0 | 0 | 0 | vdds_mem | NA | 4[8] | PU/ PD | LVCMOS |
| F7 | sdrc_a13 | 0 | O | 0 | 0 | 0 | vdds_mem | NA | 4[8] | PU/ PD | LVCMOS |
| F9 | sdrc_a14 | 0 | O | 0 | 0 | 0 | vdds_mem | NA | 4[8] | PU/ PD | LVCMOS |
| A19 | sdrc_ncs0 | 0 | O | 1 | 1 | 0 | vdds_mem | NA | 4[8] | PU/ PD | LVCMOS |
| B19 | sdrc_ncs1 | 0 | O | 1 | 1 | 0 | vdds_mem | NA | 4[8] | PU/ PD | LVCMOS |
| A10 | sdrc_clk | 0 | IO | L | 0 | 0 | vdds_mem | Yes | 4[8] | PU/ PD | LVCMOS |
| A11 | sdrc_nclk | 0 | O | 1 | 1 | 0 | vdds_mem | NA | 4[8] | PU/ PD | LVCMOS |
| B20 | sdrc_cke0 | 0 | O | H | 1 | 7 | vdds_mem | NA | 4[8] | PU/ PD | LVCMOS |
|  | safe_mode_out1[9] | 7 |  |  |  |  |  |  |  |  |  |
| C20 | sdrc_cke1 | 0 | O | H | 1 | 7 | vdds_mem | NA | 4[8] | PU/ PD | LVCMOS |
|  | safe_mode_out1[9] | 7 |  |  |  |  |  |  |  |  |  |
| D19 | sdrc_nras | 0 | O | 1 | 1 | 0 | vdds_mem | NA | 4[8] | PU/ PD | LVCMOS |
| C19 | sdrc_ncas | 0 | O | 1 | 1 | 0 | vdds_mem | NA | 4[8] | PU/ PD | LVCMOS |
| A20 | sdrc_nwe | 0 | O | 1 | 1 | 0 | vdds_mem | NA | 4 [8] | PU/ PD | LVCMOS |
| B6 | sdrc_dm0 | 0 | O | 0 | 0 | 0 | vdds_mem | NA | 4[8] | PU/ PD | LVCMOS |
| B13 | sdrc_dm1 | 0 | O | 0 | 0 | 0 | vdds_mem | NA | 4[8] | PU/ PD | LVCMOS |
| A7 | sdrc_dm2 | 0 | O | 0 | 0 | 0 | vdds_mem | NA | 4[8] | PU/ PD | LVCMOS |
| A16 | sdrc_dm3 | 0 | O | 0 | 0 | 0 | vdds_mem | NA | 4[8] | PU/ PD | LVCMOS |
| A5 | sdrc_dqs0 | 0 | IO | L | Z | 0 | vdds_mem | Yes | 4[8] | PU/ PD | LVCMOS |
| A13 | sdrc_dqs1 | 0 | IO | L | Z | 0 | vdds_mem | Yes | 4[8] | PU/ PD | LVCMOS |
| A8 | sdrc_dqs2 | 0 | IO | L | Z | 0 | vdds_mem | Yes | 4[8] | PU/ PD | LVCMOS |
| A17 | sdrc_dqs3 | 0 | IO | L | Z | 0 | vdds_mem | Yes | 4[8] | PU/ PD | LVCMOS |
| K4 | gpmc_a1 | 0 | O | L | L | 7 | vdds_mem | Yes | 8 | PU/ PD | LVCMOS |
|  | gpio_34 | 4 | IO |  |  |  |  |  |  |  |  |
|  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| K3 | gpmc_a2 | 0 | O | L | L | 7 | vdds_mem | Yes | 8 | PU/ PD | LVCMOS |

Product Folder Link(s): DM3730  DM3725

## Table 2-3. Ball Characteristics (CUS Pkg.)[1]  (continued)

| BALL NUMBER [1] | PIN NAME [2] | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | POWER [8] | HYS [9] | BUFFER STRENGTH (mA) [10] | PULLUP /DOWN TYPE [11] | IO CELL [12] |
|---|---|---|---|---|---|---|---|---|---|---|---|
|  | gpio_35 | 4 | IO |  |  |  |  |  |  |  |  |
|  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| K2 | gpmc_a3 | 0 | O | L | L | 7 | vdds_mem | Yes | 8 | PU/ PD | LVCMOS |
|  | gpio_36 | 4 | IO |  |  |  |  |  |  |  |  |
|  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| J4 | gpmc_a4 | 0 | O | L | L | 7 | vdds_mem | Yes | 8 | PU/ PD | LVCMOS |
|  | gpio_37 | 4 | IO |  |  |  |  |  |  |  |  |
|  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| J3 | gpmc_a5 | 0 | O | L | L | 7 | vdds_mem | Yes | 8 | PU/ PD | LVCMOS |
|  | gpio_38 | 4 | IO |  |  |  |  |  |  |  |  |
|  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| J2 | gpmc_a6 | 0 | O | H | H | 7 | vdds_mem | Yes | 8 | PU/ PD | LVCMOS |
|  | gpio_39 | 4 | IO |  |  |  |  |  |  |  |  |
|  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| J1 | gpmc_a7 | 0 | O | H | H | 7 | vdds_mem | Yes | 8 | PU/ PD | LVCMOS |
|  | gpio_40 | 4 | IO |  |  |  |  |  |  |  |  |
|  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| H1 | gpmc_a8 | 0 | O | H | H | 7 | vdds_mem | Yes | 8 | PU/ PD | LVCMOS |
|  | gpio_41 | 4 | IO |  |  |  |  |  |  |  |  |
|  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| H2 | gpmc_a9 | 0 | O | H | H | 7 | vdds_mem | Yes | 8 | PU/ PD | LVCMOS |
|  | sys_ndmareq2 | 1 | I |  |  |  |  |  |  |  |  |
|  | gpio_42 | 4 | IO |  |  |  |  |  |  |  |  |
|  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| G2 | gpmc_a10 | 0 | O | H | H | 7 | vdds_mem | Yes | 8 | PU/ PD | LVCMOS |
|  | sys_ndmareq3 | 1 | I |  |  |  |  |  |  |  |  |
|  | gpio_43 | 4 | IO |  |  |  |  |  |  |  |  |
|  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| L2 | gpmc_d0 | 0 | IO | H | H | 0 | vdds_mem | Yes | 8 | PU/ PD | LVCMOS |
| M1 | gpmc_d1 | 0 | IO | H | H | 0 | vdds_mem | Yes | 8 | PU/ PD | LVCMOS |
| M2 | gpmc_d2 | 0 | IO | H | H | 0 | vdds_mem | Yes | 8 | PU/ PD | LVCMOS |
| N2 | gpmc_d3 | 0 | IO | H | H | 0 | vdds_mem | Yes | 8 | PU/ PD | LVCMOS |
| M3 | gpmc_d4 | 0 | IO | H | H | 0 | vdds_mem | Yes | 8 | PU/ PD | LVCMOS |
| P1 | gpmc_d5 | 0 | IO | H | H | 0 | vdds_mem | Yes | 8 | PU/ PD | LVCMOS |
| P2 | gpmc_d6 | 0 | IO | H | H | 0 | vdds_mem | Yes | 8 | PU/ PD | LVCMOS |
| R1 | gpmc_d7 | 0 | IO | H | H | 0 | vdds_mem | Yes | 8 | PU/ PD | LVCMOS |
| R2 | gpmc_d8 | 0 | IO | H | H | 0 | vdds_mem | Yes | 8 | PU/ PD | LVCMOS |
|  | gpio_44 | 4 | IO |  |  |  |  |  |  |  |  |
|  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| T2 | gpmc_d9 | 0 | IO | H | H | 0 | vdds_mem | Yes | 8 | PU/ PD | LVCMOS |
|  | gpio_45 | 4 | IO |  |  |  |  |  |  |  |  |
|  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| U1 | gpmc_d10 | 0 | IO | H | H | 0 | vdds_mem | Yes | 8 | PU/ PD | LVCMOS |
|  | gpio_46 | 4 | IO |  |  |  |  |  |  |  |  |
|  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| R3 | gpmc_d11 | 0 | IO | H | H | 0 | vdds_mem | Yes | 8 | PU/ PD | LVCMOS |
|  | gpio_47 | 4 | IO |  |  |  |  |  |  |  |  |
|  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| T3 | gpmc_d12 | 0 | IO | H | H | 0 | vdds_mem | Yes | 8 | PU/ PD | LVCMOS |
|  | gpio_48 | 4 | IO |  |  |  |  |  |  |  |  |
|  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| U2 | gpmc_d13 | 0 | IO | H | H | 0 | vdds_mem | Yes | 8 | PU/ PD | LVCMOS |
|  | gpio_49 | 4 | IO |  |  |  |  |  |  |  |  |
|  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| V1 | gpmc_d14 | 0 | IO | H | H | 0 | vdds_mem | Yes | 8 | PU/ PD | LVCMOS |

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## Table 2-3. Ball Characteristics (CUS Pkg.)[(1)] (continued)

| BALL NUMBER [1] | PIN NAME [2] | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | POWER [8] | HYS [9] | BUFFER STRENGTH (mA) [10] | PULLUP /DOWN TYPE [11] | IO CELL [12] |
|---|---|---|---|---|---|---|---|---|---|---|---|
|  | gpio_50 | 4 | IO |  |  |  |  |  |  |  |  |
|  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| V2 | gpmc_d15 | 0 | IO | H | H | 0 | vdds_mem | Yes | 8 | PU/ PD | LVCMOS |
|  | gpio_51 | 4 | IO |  |  |  |  |  |  |  |  |
|  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| E2 | gpmc_ncs0 | 0 | O | 1 | 1 | 0 | vdds_mem | NA | 8 | NA | LVCMOS |
| D2 | gpmc_ncs3 | 0 | O | H | H | 7 | vdds_mem | Yes | 8 | PU/ PD | LVCMOS |
|  | sys_ndmareq0 | 1 | I |  |  |  |  |  |  |  |  |
|  | gpio_54 | 4 | IO |  |  |  |  |  |  |  |  |
|  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| F4 | gpmc_ncs4 | 0 | O | H | H | 7 | vdds_mem | Yes | 8 | PU/ PD | LVCMOS |
|  | sys_ndmareq1 | 1 | I |  |  |  |  |  |  |  |  |
|  | mcbsp4_ clkx | 2 | IO |  |  |  |  |  |  |  |  |
|  | gpt_9_pwm_evt | 3 | IO |  |  |  |  |  |  |  |  |
|  | gpio_55 | 4 | IO |  |  |  |  |  |  |  |  |
|  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| G5 | gpmc_ncs5 | 0 | O | H | H | 7 | vdds_mem | Yes | 8 | PU/ PD | LVCMOS |
|  | sys_ndmareq2 | 1 | I |  |  |  |  |  |  |  |  |
|  | mcbsp4_dr | 2 | I |  |  |  |  |  |  |  |  |
|  | gpt_10_pwm_evt | 3 | IO |  |  |  |  |  |  |  |  |
|  | gpio_56 | 4 | IO |  |  |  |  |  |  |  |  |
|  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| F3 | gpmc_ncs6 | 0 | O | H | H | 7 | vdds_mem | Yes | 8 | PU/ PD | LVCMOS |
|  | sys_ndmareq3 | 1 | I |  |  |  |  |  |  |  |  |
|  | mcbsp4_dx | 2 | IO |  |  |  |  |  |  |  |  |
|  | gpt_11_pwm_evt | 3 | IO |  |  |  |  |  |  |  |  |
|  | gpio_57 | 4 | IO |  |  |  |  |  |  |  |  |
|  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| G4 | gpmc_ncs7 | 0 | O | H | H | 7 | vdds_mem | Yes | 8 | PU/ PD | LVCMOS |
|  | gpmc_io_dir | 1 | O |  |  |  |  |  |  |  |  |
|  | mcbsp4_fsx | 2 | IO |  |  |  |  |  |  |  |  |
|  | gpt_8_pwm_evt | 3 | IO |  |  |  |  |  |  |  |  |
|  | gpio_58 | 4 | IO |  |  |  |  |  |  |  |  |
|  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| W2 | gpmc_clk | 0 | O | L | 0 | 0 | vdds_mem | Yes | 8 | PU/ PD | LVCMOS |
|  | gpio_59 | 4 | IO |  |  |  |  |  |  |  |  |
|  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| F1 | gpmc_nadv_ale | 0 | O | 0 | 0 | 0 | vdds_mem | NA | 8 | PU/ PD | LVCMOS |
| F2 | gpmc_noe | 0 | O | 1 | 1 | 0 | vdds_mem | NA | 8 | PU/ PD | LVCMOS |
| G3 | gpmc_nwe | 0 | O | 1 | 1 | 0 | vdds_mem | NA | 8 | PU/ PD | LVCMOS |
| K5 | gpmc_nbe0_cle | 0 | O | L | 0 | 0 | vdds_mem | Yes | 8 | PU/ PD | LVCMOS |
|  | gpio_60 | 4 | IO |  |  |  |  |  |  |  |  |
|  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| L1 | gpmc_nbe1 | 0 | O | L | L | 7 | vdds_mem | Yes | 8 | PU/ PD | LVCMOS |
|  | gpio_61 | 4 | IO |  |  |  |  |  |  |  |  |
|  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| E1 | gpmc_nwp | 0 | O | L | 0 | 0 | vdds_mem | Yes | 8 | PU/ PD | LVCMOS |
|  | gpio_62 | 4 | IO |  |  |  |  |  |  |  |  |
|  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| C1 | gpmc_wait0 | 0 | I | H | H | 0 | vdds_mem | Yes | NA | PU/ PD | LVCMOS |
| C2 | gpmc_wait3 | 0 | I | H | H | 7 | vdds_mem | Yes | 8 | PU/ PD | LVCMOS |
|  | sys_ndmareq1 | 1 | I |  |  |  |  |  |  |  |  |
|  | uart4_rx | 2 | I |  |  |  |  |  |  |  |  |
|  | gpio_65 | 4 | IO |  |  |  |  |  |  |  |  |
|  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |

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## Table 2-3. Ball Characteristics (CUS Pkg.)[(1)] (continued)

| BALL NUMBER [1] | PIN NAME [2] | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | POWER [8] | HYS [9] | BUFFER STRENGTH (mA) [10] | PULLUP /DOWN TYPE [11] | IO CELL [12] |
|---|---|---|---|---|---|---|---|---|---|---|---|
| G22 | dss_pclk | 0 | O | H | H | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| | gpio_66 | 4 | IO | | | | | | | | |
| | hw_dbg12 | 5 | O | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | |
| E22 | dss_hsync | 0 | O | H | H | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| | gpio_67 | 4 | IO | | | | | | | | |
| | hw_dbg13 | 5 | O | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | |
| F22 | dss_vsync | 0 | O | H | H | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| | gpio_68 | 4 | IO | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | |
| J21 | dss_acbias | 0 | O | L | L | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| | gpio_69 | 4 | IO | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | |
| AC19 | dss_data0 | 0 | IO | L | L | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| | uart1_cts | 2 | I | | | | | | NA | | |
| | gpio_70 | 4 | IO | | | | | | 8 | | |
| | safe_mode | 7 | | | | | | | 8 | | |
| AB19 | dss_data1 | 0 | IO | L | L | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| | uart1_rts | 2 | O | | | | | | 8 | | |
| | gpio_71 | 4 | IO | | | | | | 8 | | |
| | safe_mode | 7 | | | | | | | 8 | | |
| AD20 | dss_data2 | 0 | IO | L | L | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| | gpio_72 | 4 | IO | | | | | | 8 | | |
| | safe_mode | 7 | | | | | | | 8 | | |
| AC20 | dss_data3 | 0 | IO | L | L | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| | gpio_73 | 4 | IO | | | | | | 8 | | |
| | safe_mode | 7 | | | | | | | 8 | | |
| AD21 | dss_data4 | 0 | IO | L | L | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| | uart3_rx_ irrx | 2 | I | | | | | | NA | | |
| | gpio_74 | 4 | IO | | | | | | 8 | | |
| | safe_mode | 7 | | | | | | | 8 | | |
| AC21 | dss_data5 | 0 | IO | L | L | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| | uart3_tx_ irtx | 2 | O | | | | | | 8 | | |
| | gpio_75 | 4 | IO | | | | | | 8 | | |
| | safe_mode | 7 | | | | | | | 8 | | |
| D24 | dss_data6 | 0 | IO | L | L | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| | uart1_tx | 2 | O | | | | | | | | |
| | gpio_76 | 4 | IO | | | | | | | | |
| | hw_dbg14 | 5 | O | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | |
| E23 | dss_data7 | 0 | IO | L | L | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| | uart1_rx | 2 | I | | | | | | | | |
| | gpio_77 | 4 | IO | | | | | | | | |
| | hw_dbg15 | 5 | O | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | |
| E24 | dss_data8 | 0 | IO | L | L | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| | uart3_rx_irrx | 2 | I | | | | | | | | |
| | gpio_78 | 4 | IO | | | | | | | | |
| | hw_dbg16 | 5 | O | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | |
| F23 | dss_data9 | 0 | IO | L | L | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| | uart3_tx_irtx | 2 | O | | | | | | | | |
| | gpio_79 | 4 | IO | | | | | | | | |
| | hw_dbg17 | 5 | O | | | | | | | | |

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Product Folder Link(s): *DM3730  DM3725*

## Table 2-3. Ball Characteristics (CUS Pkg.)[(1)] (continued)

| BALL NUMBER [1] | PIN NAME [2] | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | POWER [8] | HYS [9] | BUFFER STRENGTH (mA) [10] | PULLUP /DOWN TYPE [11] | IO CELL [12] |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | safe_mode | 7 | | | | | | | | | |
| AC22 | dss_data10 | 0 | IO | L | L | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| | gpio_80 | 4 | IO | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | |
| AC23 | dss_data11 | 0 | IO | L | L | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| | gpio_81 | 4 | IO | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | |
| AB22 | dss_data12 | 0 | IO | L | L | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| | gpio_82 | 4 | IO | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | |
| Y22 | dss_data13 | 0 | IO | L | L | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| | gpio_83 | 4 | IO | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | |
| W22 | dss_data14 | 0 | IO | L | L | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| | gpio_84 | 4 | IO | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | |
| V22 | dss_data15 | 0 | IO | L | L | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| | gpio_85 | 4 | IO | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | |
| J22 | dss_data16 | 0 | IO | L | L | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| | gpio_86 | 4 | IO | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | |
| G23 | dss_data17 | 0 | IO | L | L | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| | gpio_87 | 4 | IO | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | |
| G24 | dss_data18 | 0 | IO | L | L | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| | mcspi3_clk | 2 | IO | | | | | | | | |
| | dss_data0 | 3 | IO | | | | | | | | |
| | gpio_88 | 4 | IO | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | |
| H23 | dss_data19 | 0 | IO | L | L | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| | mcspi3_simo | 2 | IO | | | | | | | | |
| | dss_data1 | 3 | IO | | | | | | | | |
| | gpio_89 | 4 | IO | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | |
| D23 | dss_data20 | 0 | O | H | H | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| | mcspi3_somi | 2 | IO | | | | | | | | |
| | dss_data2 | 3 | IO | | | | | | | | |
| | gpio_90 | 4 | IO | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | |
| K22 | dss_data21 | 0 | O | L | L | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| | mcspi3_cs0 | 2 | IO | | | | | | | | |
| | dss_data3 | 3 | IO | | | | | | | | |
| | gpio_91 | 4 | IO | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | |
| V21 | dss_data22 | 0 | O | L | L | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| | mcspi3_cs1 | 2 | O | | | | | | | | |
| | dss_data4 | 3 | IO | | | | | | | | |
| | gpio_92 | 4 | IO | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | |
| W21 | dss_data23 | 0 | O | L | L | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| | dss_data5 | 3 | IO | | | | | | | | |
| | gpio_93 | 4 | IO | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | |
| AA23 | cvideo2_out | 0 | AO | 0 | 0 | 0 | vdda_dac | NA | NA[(6)] | NA | 10-bit DAC |

## Table 2-3. Ball Characteristics (CUS Pkg.)[(1)] (continued)

| BALL NUMBER [1] | PIN NAME [2] | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | POWER [8] | HYS [9] | BUFFER STRENGTH (mA) [10] | PULLUP /DOWN TYPE [11] | IO CELL [12] |
|---|---|---|---|---|---|---|---|---|---|---|---|
| AB24 | cvideo1_out | 0 | AO | 0 | 0 | 0 | vdda_dac | NA | NA[(6)] | NA | 10-bit DAC |
| AB23 | cvideo1_vfb | 0 | AO | 0 | NA | 0 | vdda_dac | NA | NA[(7)] | NA | 10-bit DAC |
| Y23 | cvideo2_vfb | 0 | AO | 0 | NA | 0 | vdda_dac | NA | NA[(7)] | NA | 10-bit DAC |
| Y24 | cvideo1_rset | 0 | AIO | 0 | NA | 0 | vdda_dac | No | NA | NA | 10-bit DAC |
| A22 | cam_hs | 0 | IO | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
|  | gpio_94 | 4 | IO |  |  |  |  |  |  |  |  |
|  | hw_dbg0 | 5 | O |  |  |  |  |  |  |  |  |
|  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| E18 | cam_vs | 0 | IO | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
|  | gpio_95 | 4 | IO |  |  |  |  |  |  |  |  |
|  | hw_dbg1 | 5 | O |  |  |  |  |  |  |  |  |
|  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| B22 | cam_ xclka | 0 | O | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
|  | gpio_96 | 4 | IO |  |  |  |  |  |  |  |  |
|  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| J19 | cam_pclk | 0 | I | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
|  | gpio_97 | 4 | IO |  |  |  |  |  |  |  |  |
|  | hw_dbg2 | 5 | O |  |  |  |  |  |  |  |  |
|  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| H24 | cam_fld | 0 | IO | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
|  | cam_global_reset | 2 | IO |  |  |  |  |  |  |  |  |
|  | hw_dbg3 | 5 | O |  |  |  |  |  |  |  |  |
|  | gpio_98 | 4 | IO |  |  |  |  |  |  |  |  |
|  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| AB18 | cam_d0 | 0 | I | L | L | 7 | vdds | Yes | NA | PU/ PD | LVCMOS |
|  | gpio_99 | 4 | I |  |  |  |  |  |  |  |  |
|  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| AC18 | cam_d1 | 0 | I | L | L | 7 | vdds | Yes | NA | PU/ PD | LVCMOS |
|  | gpio_100 | 4 | I |  |  |  |  |  |  |  |  |
|  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| G19 | cam_d2 | 0 | I | L | L | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
|  | gpio_101 | 4 | IO |  |  |  |  |  |  |  |  |
|  | hw_dbg4 | 5 | O |  |  |  |  |  |  |  |  |
|  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| F19 | cam_d3 | 0 | I | L | L | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
|  | gpio_102 | 4 | IO |  |  |  |  |  |  |  |  |
|  | hw_dbg5 | 5 | O |  |  |  |  |  |  |  |  |
|  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| G20 | cam_d4 | 0 | I | L | L | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
|  | gpio_103 | 4 | IO |  |  |  |  |  |  |  |  |
|  | hw_dbg6 | 5 | O |  |  |  |  |  |  |  |  |
|  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| B21 | cam_d5 | 0 | I | L | L | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
|  | gpio_104 | 4 | IO |  |  |  |  |  |  |  |  |
|  | hw_dbg7 | 5 | O |  |  |  |  |  |  |  |  |
|  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| L24 | cam_d6 | 0 | I | L | L | 7 | vdds | Yes | NA | PU/ PD | LVCMOS |
|  | gpio_105 | 4 | I |  |  |  |  |  |  |  |  |
|  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| K24 | cam_d7 | 0 | I | L | L | 7 | vdds | Yes | NA | PU/ PD | LVCMOS |
|  | gpio_106 | 4 | I |  |  |  |  |  |  |  |  |
|  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| J23 | cam_d8 | 0 | I | L | L | 7 | vdds | Yes | NA | PU/ PD | LVCMOS |
|  | gpio_107 | 4 | I |  |  |  |  |  |  |  |  |
|  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |

## Table 2-3. Ball Characteristics (CUS Pkg.)[(1)] (continued)

| BALL NUMBER [1] | PIN NAME [2] | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | POWER [8] | HYS [9] | BUFFER STRENGTH (mA) [10] | PULLUP /DOWN TYPE [11] | IO CELL [12] |
|---|---|---|---|---|---|---|---|---|---|---|---|
| K23 | cam_d9 | 0 | I | L | L | 7 | vdds | Yes | NA | PU/ PD | LVCMOS |
| | gpio_108 | 4 | I | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | |
| F21 | cam_d10 | 0 | I | L | L | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| | gpio_109 | 4 | IO | | | | | | | | |
| | hw_dbg8 | 5 | O | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | |
| G21 | cam_d11 | 0 | I | L | L | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| | gpio_110 | 4 | IO | | | | | | | | |
| | hw_dbg9 | 5 | O | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | |
| C22 | cam_ xclkb | 0 | O | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | gpio_111 | 4 | IO | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | |
| F18 | cam_wen | 0 | I | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | cam_ shutter | 2 | O | | | | | | | | |
| | gpio_167 | 4 | IO | | | | | | | | |
| | hw_dbg10 | 5 | O | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | |
| J20 | cam_ strobe | 0 | O | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | gpio_126 | 4 | IO | | | | | | | | |
| | hw_dbg11 | 5 | O | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | |
| V20 | mcbsp2_fsx | 0 | IO | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | gpio_116 | 4 | IO | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | |
| T21 | mcbsp2_ clkx | 0 | IO | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | gpio_117 | 4 | IO | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | |
| V19 | mcbsp2_dr | 0 | I | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | gpio_118 | 4 | IO | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | |
| R20 | mcbsp2_dx | 0 | IO | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | gpio_119 | 4 | IO | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | |
| M23 | mmc1_clk | 0 | O | L | L | 7 | vdds_mmc1[(14)] | Yes | 1 | PU/ PD [(4)] | LVCMOS |
| | gpio_120 [(5)] | 4 | IO | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | |
| L23 | mmc1_cmd | 0 | IO | L | L | 7 | vdds_mmc1[(14)] | Yes | 1 | PU/ PD[(4)] | LVCMOS |
| | gpio_121 [(5)] | 4 | IO | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | |
| M22 | mmc1_dat0 | 0 | IO | L | L | 7 | vdds_mmc1[(14)] | Yes | 1 | PU/ PD[(4)] | LVCMOS |
| | gpio_122 [(5)] | 4 | IO | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | |
| M21 | mmc1_dat1 | 0 | IO | L | L | 7 | vdds_mmc1[(14)] | Yes | 1 | PU/ PD[(4)] | LVCMOS |
| | gpio_123[(5)] | 4 | IO | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | |
| M20 | mmc1_dat2 | 0 | IO | L | L | 7 | vdds_mmc1[(14)] | Yes | 1 | PU/ PD[(4)] | LVCMOS |
| | gpio_124[(5)] | 4 | IO | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | |
| N23 | mmc1_dat3 | 0 | IO | L | L | 7 | vdds_mmc1[(14)] | Yes | 1 | PU/ PD[(4)] | LVCMOS |

Product Folder Link(s): DM3730  DM3725

## Table 2-3. Ball Characteristics (CUS Pkg.)[1] (continued)

| BALL NUMBER [1] | PIN NAME [2] | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | POWER [8] | HYS [9] | BUFFER STRENGTH (mA) [10] | PULLUP /DOWN TYPE [11] | IO CELL [12] |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | gpio_125[5] | 4 | IO | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | |
| N22 | gpio_126[5] | 4 | IO | L | L | 7 | vdds_x | Yes | 1 | PU/ PD[4] | LVCMOS |
| | safe_mode | 7 | | | | | | | | | |
| P24 | gpio_129[5] | 4 | IO | L | L | 7 | vdds_x | Yes | 1 | PU/ PD [4] | LVCMOS |
| | safe_mode | 7 | | | | | | | | | |
| Y1 | mmc2_clk | 0 | O | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | mcspi3_clk | 1 | IO | | | | | | | | |
| | gpio_130 | 4 | IO | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | |
| AB5 | mmc2_cmd | 0 | IO | H | H | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | mcspi3_ simo | 1 | IO | | | | | | | | |
| | gpio_131 | 4 | IO | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | |
| AB3 | mmc2_ dat0 | 0 | IO | H | H | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | mcspi3_ somi | 1 | IO | | | | | | | | |
| | gpio_132 | 4 | IO | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | |
| Y3 | mmc2_ dat1 | 0 | IO | H | H | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | gpio_133 | 4 | IO | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | |
| W3 | mmc2_ dat2 | 0 | IO | H | H | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | mcspi3_cs1 | 1 | O | | | | | | | | |
| | gpio_134 | 4 | IO | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | |
| V3 | mmc2_ dat3 | 0 | IO | H | H | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | mcspi3_cs0 | 1 | IO | | | | | | | | |
| | gpio_135 | 4 | IO | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | |
| AB2 | mmc2_ dat4 | 0 | IO | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | mmc2_dir_dat0 | 1 | O | | | | | | | | |
| | mmc3_dat0 | 3 | IO | | | | | | | | |
| | gpio_136 | 4 | IO | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | |
| AA2 | mmc2_ dat5 | 0 | IO | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | mmc2_dir_dat1 | 1 | O | | | | | | | | |
| | cam_global_reset | 2 | IO | | | | | | | | |
| | mmc3_dat1 | 3 | IO | | | | | | | | |
| | gpio_137 | 4 | IO | | | | | | | | |
| | mm3_rxdp | 6 | IO | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | |
| Y2 | mmc2_dat6 | 0 | IO | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | mmc2_dir_cmd | 1 | O | | | | | | | | |
| | cam_shutter | 2 | O | | | | | | | | |
| | mmc3_dat2 | 3 | IO | | | | | | | | |
| | gpio_138 | 4 | IO | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | |
| AA1 | mmc2_dat7 | 0 | IO | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | mmc2_clkin | 1 | I | | | | | | | | |
| | mmc3_dat3 | 3 | IO | | | | | | | | |
| | gpio_139 | 4 | IO | | | | | | | | |
| | mm3_rxdm | 6 | IO | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | |
| V6 | mcbsp3_dx | 0 | IO | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | uart2_cts | 1 | I | | | | | | | | |

## Table 2-3. Ball Characteristics (CUS Pkg.)[(1)] (continued)

| BALL NUMBER [1] | PIN NAME [2] | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | POWER [8] | HYS [9] | BUFFER STRENGTH (mA) [10] | PULLUP /DOWN TYPE [11] | IO CELL [12] |
|---|---|---|---|---|---|---|---|---|---|---|---|
|  | gpio_140 | 4 | IO |  |  |  |  |  |  |  |  |
|  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| V5 | mcbsp3_dr | 0 | I | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
|  | uart2_rts | 1 | O |  |  |  |  |  |  |  |  |
|  | gpio_141 | 4 | IO |  |  |  |  |  |  |  |  |
|  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| W4 | mcbsp3_ clkx | 0 | IO | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
|  | uart2_tx | 1 | O |  |  |  |  |  |  |  |  |
|  | gpio_142 | 4 | IO |  |  |  |  |  |  |  |  |
|  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| V4 | mcbsp3_fsx | 0 | IO | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
|  | uart2_rx | 1 | I |  |  |  |  |  |  |  |  |
|  | gpio_143 | 4 | IO |  |  |  |  |  |  |  |  |
|  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| W7 | uart1_tx | 0 | O | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
|  | gpio_148 | 4 | IO |  |  |  |  |  |  |  |  |
|  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| W6 | uart1_rts | 0 | O | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
|  | gpio_149 | 4 | IO |  |  |  |  |  |  |  |  |
|  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| AC2 | uart1_cts | 0 | I | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
|  | gpio_150 | 4 | IO |  |  |  |  |  |  |  |  |
|  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| V7 | uart1_rx | 0 | I | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
|  | mcbsp1_ clkr | 2 | IO |  |  |  |  |  |  |  |  |
|  | mcspi4_clk | 3 | IO |  |  |  |  |  |  |  |  |
|  | gpio_151 | 4 | IO |  |  |  |  |  |  |  |  |
|  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| W19 | mcbsp1_ clkr | 0 | IO | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
|  | mcspi4_clk | 1 | IO |  |  |  |  |  |  |  |  |
|  | gpio_156 | 4 | IO |  |  |  |  |  |  |  |  |
|  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| AB20 | mcbsp1_fsr | 0 | IO | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
|  | cam_global_reset | 2 | IO |  |  |  |  |  |  |  |  |
|  | gpio_157 | 4 | IO |  |  |  |  |  |  |  |  |
|  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| W18 | mcbsp1_dx | 0 | IO | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
|  | mcspi4_ simo | 1 | IO |  |  |  |  |  |  |  |  |
|  | mcbsp3_dx | 2 | IO |  |  |  |  |  |  |  |  |
|  | gpio_158 | 4 | IO |  |  |  |  |  |  |  |  |
|  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| Y18 | mcbsp1_dr | 0 | I | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
|  | mcspi4_ somi | 1 | IO |  |  |  |  |  |  |  |  |
|  | mcbsp3_dr | 2 | I |  |  |  |  |  |  |  |  |
|  | gpio_159 | 4 | IO |  |  |  |  |  |  |  |  |
|  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| AA18 | mcbsp_clks | 0 | I | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
|  | cam_ shutter | 2 | O |  |  |  |  |  |  |  |  |
|  | gpio_160 | 4 | IO |  |  |  |  |  |  |  |  |
|  | uart1_cts | 5 | I |  |  |  |  |  |  |  |  |
|  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| AA19 | mcbsp1_fsx | 0 | IO | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
|  | mcspi4_cs0 | 1 | IO |  |  |  |  |  |  |  |  |
|  | mcbsp3_fsx | 2 | IO |  |  |  |  |  |  |  |  |
|  | gpio_161 | 4 | IO |  |  |  |  |  |  |  |  |

## Table 2-3. Ball Characteristics (CUS Pkg.)[1]  (continued)

| BALL NUMBER [1] | PIN NAME [2] | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | POWER [8] | HYS [9] | BUFFER STRENGTH (mA) [10] | PULLUP /DOWN TYPE [11] | IO CELL [12] |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | safe_mode | 7 | | | | | | | | | |
| V18 | mcbsp1_ clkx | 0 | IO | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | mcbsp3_ clkx | 2 | IO | | | | | | | | |
| | gpio_162 | 4 | IO | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | |
| A23 | uart3_cts_ rctx | 0 | IO | H | H | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | gpio_163 | 4 | IO | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | |
| B23 | uart3_rts_ sd | 0 | O | H | H | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | gpio_164 | 4 | IO | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | |
| B24 | uart3_rx_ irrx | 0 | I | H | H | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | gpio_165 | 4 | IO | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | |
| C23 | uart3_tx_ irtx | 0 | O | H | H | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | gpio_166 | 4 | IO | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | |
| R21 | hsusb0_clk | 0 | I | L | L | 7 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| | gpio_120 | 4 | IO | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | |
| R23 | hsusb0_stp | 0 | O | H | H | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | gpio_121 | 4 | IO | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | |
| P23 | hsusb0_dir | 0 | I | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | gpio_122 | 4 | IO | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | |
| R22 | hsusb0_nxt | 0 | I | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | gpio_124 | 4 | IO | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | |
| T24 | hsusb0_ data0 | 0 | IO | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | uart3_tx_ irtx | 2 | O | | | | | | | | |
| | gpio_125 | 4 | IO | | | | | | | | |
| | uart2_tx | 5 | O | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | |
| T23 | hsusb0_ data1 | 0 | IO | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | uart3_rx_ irrx | 2 | I | | | | | | | | |
| | gpio_130 | 4 | IO | | | | | | | | |
| | uart2_rx | 5 | I | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | |
| U24 | hsusb0_ data2 | 0 | IO | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | uart3_rts_ sd | 2 | O | | | | | | | | |
| | gpio_131 | 4 | IO | | | | | | | | |
| | uart2_rts | 5 | O | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | |
| U23 | hsusb0_data3 | 0 | IO | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | uart3_cts_ rctx | 2 | IO | | | | | | | | |
| | gpio_169 | 4 | IO | | | | | | | | |
| | uart2_cts | 5 | I | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | |
| W24 | hsusb0_ data4 | 0 | IO | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | gpio_188 | 4 | IO | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | |
| V23 | hsusb0_ data5 | 0 | IO | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | gpio_189 | 4 | IO | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | |

## Table 2-3. Ball Characteristics (CUS Pkg.)[1]  (continued)

| BALL NUMBER [1] | PIN NAME [2] | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | POWER [8] | HYS [9] | BUFFER STRENGTH (mA) [10] | PULLUP /DOWN TYPE [11] | IO CELL [12] |
|---|---|---|---|---|---|---|---|---|---|---|---|
| W23 | hsusb0_ data6 | 0 | IO | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
|  | gpio_190 | 4 | IO |  |  |  |  |  |  |  |  |
|  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| T22 | hsusb0_ data7 | 0 | IO | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
|  | gpio_191 | 4 | IO |  |  |  |  |  |  |  |  |
|  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| K20 | i2c1_scl | 0 | OD | H | H | 0 | vdds | NA | 3 | PU/ PD[10][11] | Open Drain |
| K21 | i2c1_sda | 0 | IOD | H | H | 0 | vdds | Yes | 3 | PU/ PD[10][11] | Open Drain |
| AC15 | i2c2_scl | 0 | OD | H | H | 7 | vdds | Yes | 3 | PU/ PD[10][12] | Open Drain |
|  | gpio_168 | 4 | IO |  |  |  |  |  | 4 |  |  |
|  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| AC14 | i2c2_sda | 0 | IOD | H | H | 7 | vdds | Yes | 3 | PU/ PD[10][12] | Open Drain |
|  | gpio_183 | 4 | IO |  |  |  |  |  | 4 |  |  |
|  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| AC13 | i2c3_scl | 0 | OD | H | H | 7 | vdds | Yes | 3 | PU/ PD[10][12] | Open Drain |
|  | gpio_184 | 4 | IO |  |  |  |  |  | 4 |  |  |
|  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| AC12 | i2c3_sda | 0 | IOD | H | H | 7 | vdds | Yes | 3 | PU/ PD[10][12] | Open Drain |
|  | gpio_185 | 4 | IO |  |  |  |  |  | 4 |  |  |
|  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| Y16 | i2c4_scl | 0 | OD | H | H | 0 | vdds | Yes | 3 | PU/ PD[10][11] | Open Drain |
|  | sys_nvmode1 | 1 | O |  |  |  |  |  | 4 |  |  |
|  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| Y15 | i2c4_sda | 0 | IOD | H | H | 0 | vdds | Yes | 3 | PU/ PD[10][11] | Open Drain |
|  | sys_nvmode2 | 1 | O |  |  |  |  |  | 4 |  |  |
|  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| A24 | hdq_sio | 0 | IOD | H | H | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
|  | sys_altclk | 1 | I |  |  |  |  |  |  |  |  |
|  | i2c2_sccbe | 2 | OD |  |  |  |  |  |  |  |  |
|  | i2c3_sccbe | 3 | OD |  |  |  |  |  |  |  |  |
|  | gpio_170 | 4 | IO |  |  |  |  |  |  |  |  |
|  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| T5 | mcspi1_clk | 0 | IO | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
|  | mmc2_dat4 | 1 | IO |  |  |  |  |  |  |  |  |
|  | gpio_171 | 4 | IO |  |  |  |  |  |  |  |  |
|  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| R4 | mcspi1_ simo | 0 | IO | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
|  | mmc2_dat5 | 1 | IO |  |  |  |  |  |  |  |  |
|  | gpio_172 | 4 | IO |  |  |  |  |  |  |  |  |
|  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| T4 | mcspi1_ somi | 0 | IO | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
|  | mmc2_dat6 | 1 | IO |  |  |  |  |  |  |  |  |
|  | gpio_173 | 4 | IO |  |  |  |  |  |  |  |  |
|  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| T6 | mcspi1_cs0 | 0 | IO | H | H | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
|  | mmc2_dat7 | 1 | IO |  |  |  |  |  |  |  |  |
|  | gpio_174 | 4 | IO |  |  |  |  |  |  |  |  |
|  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| R5 | mcspi1_cs3 | 0 | O | H | H | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
|  | hsusb2_ data2 | 3 | IO |  |  |  |  |  |  |  |  |
|  | gpio_177 | 4 | IO |  |  |  |  |  |  |  |  |
|  | mm2_txdat | 5 | IO |  |  |  |  |  |  |  |  |
|  | safe_mode | 7 |  |  |  |  |  |  |  |  |  |
| N5 | mcspi2_clk | 0 | IO | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
|  | hsusb2_ data7 | 3 | IO |  |  |  |  |  |  |  |  |

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Product Folder Link(s): DM3730  DM3725

## Table 2-3. Ball Characteristics (CUS Pkg.)[(1)] (continued)

| BALL NUMBER [1] | PIN NAME [2] | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | POWER [8] | HYS [9] | BUFFER STRENGTH (mA) [10] | PULLUP /DOWN TYPE [11] | IO CELL [12] |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | gpio_178 | 4 | IO | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | |
| N4 | mcspi2_ simo | 0 | IO | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | gpt_9_pwm_evt | 1 | IO | | | | | | | | |
| | hsusb2_ data4 | 3 | IO | | | | | | | | |
| | gpio_179 | 4 | IO | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | |
| N3 | mcspi2_ somi | 0 | IO | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | gpt_10_pwm_evt | 1 | IO | | | | | | | | |
| | hsusb2_ data5 | 3 | IO | | | | | | | | |
| | gpio_180 | 4 | IO | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | |
| M5 | mcspi2_cs0 | 0 | IO | H | H | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | gpt_11_pwm_evt | 1 | IO | | | | | | | | |
| | hsusb2_ data6 | 3 | IO | | | | | | | | |
| | gpio_181 | 4 | IO | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | |
| M4 | mcspi2_cs1 | 0 | O | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | gpt_8_pwm_evt | 1 | IO | | | | | | | | |
| | hsusb2_ data3 | 3 | IO | | | | | | | | |
| | gpio_182 | 4 | IO | | | | | | | | |
| | mm2_txen_n | 5 | IO | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | |
| AA16 | sys_32k | 0 | I | Z | Z | 0 | vdds | Yes | NA | PU/ PD | LVCMOS |
| AD15 | sys_xtalin | 0 | AI | Z | Z | 0 | vdds | Yes | NA | No | Analog |
| AD14 | sys_xtalout | 0 | AO | Z | 0 | 0 | vdds | NA | NA | NA | Analog |
| Y13 | sys_clkreq | 0 | IO | 0 | see [(3)] | 0 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | gpio_1 | 4 | IO | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | |
| W16 | sys_nirq | 0 | I | H | H | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | gpio_0 | 4 | IO | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | |
| AA10 | sys_nrespwron | 0 | I | Z | Z | 0 | vdds | Yes | NA | No | LVCMOS |
| Y10 | sys_nreswarm | 0 | IOD | 0 | H | 0 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | gpio_30 | 4 | IO | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | |
| AB12 | sys_boot0 | 0 | I | Z | Z | 0 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| | dss_data18 | 3 | IO | | | | | | | | |
| | gpio_2 | 4 | IO | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | |
| AC16 | sys_boot1 | 0 | I | Z | Z | 0 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| | dss_data19 | 3 | IO | | | | | | | | |
| | gpio_3 | 4 | IO | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | |
| AD17 | sys_boot2 | 0 | I | Z | Z | 0 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| | gpio_4 | 4 | IO | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | |
| AD18 | sys_boot3 | 0 | I | Z | Z | 0 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| | dss_data20 | 3 | O | | | | | | | | |
| | gpio_5 | 4 | IO | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | |
| AC17 | sys_boot4 | 0 | I | Z | Z | 0 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| | mmc2_dir_dat2 | 1 | O | | | | | | | | |
| | dss_data21 | 3 | O | | | | | | | | |
| | gpio_6 | 4 | IO | | | | | | | | |

## Table 2-3. Ball Characteristics (CUS Pkg.)[1] (continued)

| BALL NUMBER [1] | PIN NAME [2] | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | POWER [8] | HYS [9] | BUFFER STRENGTH (mA) [10] | PULLUP /DOWN TYPE [11] | IO CELL [12] |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | safe_mode | 7 | | | | | | | | | |
| AB16 | sys_boot5 | 0 | I | Z | Z | 0 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| | mmc2_dir_dat3 | 1 | O | | | | | | | | |
| | dss_data22 | 3 | O | | | | | | | | |
| | gpio_7 | 4 | IO | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | |
| AA15 | sys_boot6 | 0 | I | Z | Z | 0 | vdds | Yes | 8 | PU/ PD | LVCMOS |
| | dss_data23 | 3 | O | | | | | | | | |
| | gpio_8 | 4 | IO | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | |
| AD23 | sys_off_ mode | 0 | O | 0 | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | gpio_9 | 4 | IO | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | |
| Y7 | sys_clkout1 | 0 | O | L | L | 7[13] | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | gpio_10 | 4 | IO | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | |
| AA6 | sys_clkout2 | 0 | O | L | L | 7 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | gpio_186 | 4 | IO | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | |
| AB7 | jtag_ntrst | 0 | I | L | L | 0 | vdds | Yes | NA | PU/ PD | LVCMOS |
| AB6 | jtag_tck | 0 | I | L | L | 0 | vdds | Yes | NA | PU/ PD | LVCMOS |
| AA7 | jtag_rtck | 0 | O | L | 0 | 0 | vdds | NA | 4 | PU/ PD | LVCMOS |
| AA9 | jtag_tms_tmsc | 0 | IO | H | H | 0 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| AB10 | jtag_tdi | 0 | I | H | H | 0 | vdds | Yes | NA | PU/ PD | LVCMOS |
| AB9 | jtag_tdo | 0 | O | L | Z | 0 | vdds | NA | 4 | PU/ PD | LVCMOS |
| AC24 | jtag_emu0 | 0 | IO | H | H | 0 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | gpio_11 | 4 | IO | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | |
| AD24 | jtag_emu1 | 0 | IO | H | H | 0 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | gpio_31 | 4 | IO | | | | | | | | |
| | safe_mode | 7 | | | | | | | | | |
| AC1 | etk_clk | 0 | O | H | H | 4 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | mcbsp5_ clkx | 1 | IO | | | | | | | | |
| | mmc3_clk | 2 | O | | | | | | | | |
| | hsusb1_stp | 3 | O | | | | | | | | |
| | gpio_12 | 4 | IO | | | | | | | | |
| | mm1_rxdp | 5 | IO | | | | | | | | |
| | hw_dbg0 | 7 | O | | | | | | | | |
| AD3 | etk_ctl | 0 | O | H | H | 4 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | mmc3_cmd | 2 | IO | | | | | | | | |
| | hsusb1_clk | 3 | O | | | | | | | | |
| | gpio_13 | 4 | IO | | | | | | | | |
| | hw_dbg1 | 7 | O | | | | | | | | |
| AD6 | etk_d0 | 0 | O | H | H | 4 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | mcspi3_ simo | 1 | IO | | | | | | | | |
| | mmc3_dat4 | 2 | IO | | | | | | | | |
| | hsusb1_ data0 | 3 | IO | | | | | | | | |
| | gpio_14 | 4 | IO | | | | | | | | |
| | mm1_rxrcv | 5 | IO | | | | | | | | |
| | hw_dbg2 | 7 | O | | | | | | | | |
| AC6 | etk_d1 | 0 | O | H | H | 4 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | mcspi3_ somi | 1 | IO | | | | | | | | |
| | hsusb1_ data1 | 3 | IO | | | | | | | | |
| | gpio_15 | 4 | IO | | | | | | | | |
| | mm1_txse0 | 5 | IO | | | | | | | | |

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## Table 2-3. Ball Characteristics (CUS Pkg.)[1] (continued)

| BALL NUMBER [1] | PIN NAME [2] | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | POWER [8] | HYS [9] | BUFFER STRENGTH (mA) [10] | PULLUP /DOWN TYPE [11] | IO CELL [12] |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | hw_dbg3 | 7 | O | | | | | | | | |
| AC7 | etk_d2 | 0 | O | H | H | 4 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | mcspi3_cs0 | 1 | IO | | | | | | | | |
| | hsusb1_ data2 | 3 | IO | | | | | | | | |
| | gpio_16 | 4 | IO | | | | | | | | |
| | mm1_txdat | 5 | IO | | | | | | | | |
| | hw_dbg4 | 7 | O | | | | | | | | |
| AD8 | etk_d3 | 0 | O | H | H | 4 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | mcspi3_clk | 1 | IO | | | | | | | | |
| | mmc3_dat3 | 2 | IO | | | | | | | | |
| | hsusb1_ data7 | 3 | IO | | | | | | | | |
| | gpio_17 | 4 | IO | | | | | | | | |
| | hw_dbg5 | 7 | O | | | | | | | | |
| AC5 | etk_d4 | 0 | O | L | L | 4 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | mcbsp5_dr | 1 | I | | | | | | | | |
| | mmc3_dat0 | 2 | IO | | | | | | | | |
| | hsusb1_ data4 | 3 | IO | | | | | | | | |
| | gpio_18 | 4 | IO | | | | | | | | |
| | hw_dbg6 | 7 | O | | | | | | | | |
| AD2 | etk_d5 | 0 | O | L | L | 4 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | mcbsp5_fsx | 1 | IO | | | | | | | | |
| | mmc3_dat1 | 2 | IO | | | | | | | | |
| | hsusb1_ data5 | 3 | IO | | | | | | | | |
| | gpio_19 | 4 | IO | | | | | | | | |
| | hw_dbg7 | 7 | O | | | | | | | | |
| AC8 | etk_d6 | 0 | O | L | L | 4 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | mcbsp5_dx | 1 | O | | | | | | | | |
| | mmc3_dat2 | 2 | IO | | | | | | | | |
| | hsusb1_ data6 | 3 | IO | | | | | | | | |
| | gpio_20 | 4 | IO | | | | | | | | |
| | hw_dbg8 | 7 | O | | | | | | | | |
| AD9 | etk_d7 | 0 | O | L | L | 4 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | mcspi3_cs1 | 1 | O | | | | | | | | |
| | mmc3_dat7 | 2 | IO | | | | | | | | |
| | hsusb1_ data3 | 3 | IO | | | | | | | | |
| | gpio_21 | 4 | IO | | | | | | | | |
| | mm1_txen_n | 5 | IO | | | | | | | | |
| | hw_dbg9 | 7 | O | | | | | | | | |
| AC4 | etk_d8 | 0 | O | L | L | 4 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | mmc3_dat6 | 2 | IO | | | | | | | | |
| | hsusb1_dir | 3 | I | | | | | | | | |
| | gpio_22 | 4 | IO | | | | | | | | |
| | hw_dbg10 | 7 | O | | | | | | | | |
| AD5 | etk_d9 | 0 | O | L | L | 4 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | mmc3_dat5 | 2 | IO | | | | | | | | |
| | hsusb1_nxt | 3 | I | | | | | | | | |
| | gpio_23 | 4 | IO | | | | | | | | |
| | mm1_rxdm | 5 | IO | | | | | | | | |
| | hw_dbg11 | 7 | O | | | | | | | | |
| AC3 | etk_d10 | 0 | O | L | L | 4 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | uart1_rx | 2 | I | | | | | | | | |
| | hsusb2_clk | 3 | O | | | | | | | | |
| | gpio_24 | 4 | IO | | | | | | | | |
| | hw_dbg12 | 7 | O | | | | | | | | |
| AC9 | etk_d11 | 0 | O | L | L | 4 | vdds | Yes | 4 | PU/ PD | LVCMOS |

## Table 2-3. Ball Characteristics (CUS Pkg.)[(1)] (continued)

| BALL NUMBER [1] | PIN NAME [2] | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | POWER [8] | HYS [9] | BUFFER STRENGTH (mA) [10] | PULLUP /DOWN TYPE [11] | IO CELL [12] |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | hsusb2_stp | 3 | O | | | | | | | | |
| | gpio_25 | 4 | IO | | | | | | | | |
| | mm2_rxdp | 5 | IO | | | | | | | | |
| | hw_dbg13 | 7 | O | | | | | | | | |
| AC10 | etk_d12 | 0 | O | L | L | 4 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | hsusb2_dir | 3 | I | | | | | | | | |
| | gpio_26 | 4 | IO | | | | | | | | |
| | hw_dbg14 | 7 | O | | | | | | | | |
| AD11 | etk_d13 | 0 | O | L | L | 4 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | hsusb2_nxt | 3 | I | | | | | | | | |
| | gpio_27 | 4 | IO | | | | | | | | |
| | mm2_rxdm | 5 | IO | | | | | | | | |
| | hw_dbg15 | 7 | O | | | | | | | | |
| AC11 | etk_d14 | 0 | O | L | L | 4 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | hsusb2_ data0 | 3 | IO | | | | | | | | |
| | gpio_28 | 4 | IO | | | | | | | | |
| | mm2_rxrcv | 5 | IO | | | | | | | | |
| | hw_dbg16 | 7 | O | | | | | | | | |
| AD12 | etk_d15 | 0 | O | L | L | 4 | vdds | Yes | 4 | PU/ PD | LVCMOS |
| | hsusb2_ data1 | 3 | IO | | | | | | | | |
| | gpio_29 | 4 | IO | | | | | | | | |
| | mm2_txse0 | 5 | IO | | | | | | | | |
| | hw_dbg17 | 7 | O | | | | | | | | |
| E16, F15, F16, G15, G16, H15, J6, J7, J8, K6, K7, K8 | vdds_mem | 0 | PWR | - | - | - | - | - | - | - | - |
| F12, F13, G12, G13, H12, H13, J17, J18, K17, K18, K19, L14, L15, M14, M15, R17, R18, R19, T17, T18, T19, T20 | vdd_core | 0 | PWR | - | - | - | - | - | - | - | - |
| F10, G9, G10, H9, H10, J9, J10, L11, L12, M6, M7, M8, M12, N6, N7, N8, R6, R7, R8, T7, T8, U12, U13, V12, V13, W12, W13 | vdd_mpu_iva | 0 | PWR | - | - | - | - | - | - | - | - |
| H8 | vdds_x | 0 | PWR | - | - | - | - | - | - | - | - |
| M17, M18, M19, N17, N18, N19, U10, V9, V10, W9, W10, Y9 | vdds | 0 | PWR | - | - | - | - | - | - | - | - |
| N24 | vdds_mmc1 | 0 | PWR | - | - | - | - | - | - | - | - |
| Y12 | cap_vddu_ wkup_logic | 0 | PWR | - | - | - | - | - | - | - | - |
| U8 | cap_vdd_sram_mpu_ iva | 0 | PWR | - | - | - | - | - | - | - | - |
| H17 | cap_vdd_sram_core | 0 | PWR | - | - | - | - | - | - | - | - |
| G18 | vdda_dplls_dll | 0 | PWR | - | - | - | - | - | - | - | - |
| U17 | vdda_dpll_per | 0 | PWR | - | - | - | - | - | - | - | - |
| AA12 | vdds_sram | 0 | PWR | - | - | - | - | - | - | - | - |
| AA13 | vdda_wkup_bg_bb | 0 | PWR | - | - | - | - | - | - | - | - |

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## Table 2-3. Ball Characteristics (CUS Pkg.)[1] (continued)

| BALL NUMBER [1] | PIN NAME [2] | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | POWER [8] | HYS [9] | BUFFER STRENGTH (mA) [10] | PULLUP /DOWN TYPE [11] | IO CELL [12] |
|---|---|---|---|---|---|---|---|---|---|---|---|
| N21 | cap_vdd_bb_mpu_iva | 0 | PWR | - | - | - | - | - | - | - | - |
| N20 | cap_vddu_array | 0 | PWR | - | - | - | - | - | - | - | - |
| AB15 | vssa_dac | 0 | GND | - | - | - | - | - | - | - | - |
| AB13 | vdda_dac | 0 | PWR | - | - | - | - | - | - | - | - |
| H11, H14, H16, J11, J12, J13, J14, J15, J16, K10, K11, K14, K15, L8, L10, L13, L17, M9, M10, M11, M13, M16, N9, N10, N11, N12, N13, N14, N15, N16, P8, P10, P11, P12, P13, P14, P15, P17, R10, R11, R14, R15, T9, T10, T11, T12, T13, T14, T15, T16, U9, U11, U14, U15, U16, V15, V16 | vss | 0 | GND | - | - | - | - | - | - | - | - |
| AD1, A1, A2, B1 | No Connect[2] | - | - | - | - | - | - | - | - | - | - |
| W15 | sys_xtalgnd | 0 | GND | - | - | - | - | - | - | - | - |

(1)  NA in this table stands for "Not Applicable".

(2)  Pins labeled as "No connect" must be left unconnected. Any connections to these pins may result in unpredictable behavior.

(3)  Depending on the sys_clkreq direction the corresponding reset released state value can be:
–   Z if sys_clkreq is used as input
–   1 if sys_clkreq is used as output
For a full description of the sys_clkreq control, see Power, Reset, and Clock Management chapter of the *AM/DM37x Multimedia Device Technical Reference Manual* (literature number SPRUGN4).

(4)  PU = [50 to 100 kΩ] per default or [10 to 50 kΩ] according to the selected mode. For a full description of the pull-up drive strength programming, see the PRG_SDMMC_PUSTRENGTH configuration register bit field in the System Control Module chapter of the *AM/DM37x Multimedia Device Technical Reference Manual* (literature number SPRUGN4). PD: 30 to 150 kΩ.

(5)  The usage of this GPIO is strongly restricted. For more information, see the General-Purpose Interface chapter of the *AM/DM37x Multimedia Device Technical Reference Manual* (literature number SPRUGN4).

(6)  The drive strength is fixed regardless of the load. The driver is designed to drive 75Ω for video applications.

(7)  In buffer mode, the drive strength is fixed regardless of the load. The driver is designed to drive 75Ω for video applications. In bypass mode, the drive strength is 0.47 mA.

(8)  The drive strength of these IOs is set according to the programmable load range: 2 pF to 4 pF per default or 4 pF to 12 pF. For a full description of the drive strength programming, see the System Control Module chapter of the *AM/DM37x Multimedia Device Technical Reference Manual* (literature number SPRUGN4).

(9)  In the safe_mode_out1, the buffer is configured to drive 1.

(10)  The pullup and pulldown can be either the standard LVCMOS 100-µA drive strength or the I2C pullup and pulldown described below: Nominal resistance = 1.66 kΩ in high-speed mode with a load range of 5 pF to 12 pF, 4.5 kΩ in standard / fast mode with a load range of 5 pF to 15 pF.

(11)  The default buffer configuration is High-Speed I2C point-to-point mode using internal pullup. For a full description of the pull drive strength programming, see prg_i2c1_pullupresx, prg_i2c1_lb1lb0, and prg_sr_pullupresx, prg_sr_lb bits of the CONTROL_PROG_IO1, CONTROL_PROG_IO_WKUP1 control modules in the System Control Module / SCM Programming Model / Feature Settings section and the System Control Module chapter of the *AM/DM37x Multimedia Device Technical Reference Manual* (literature number SPRUGN4) to modify the IO settings if required by the targeted interface application.

(12)  The default buffer configuration is standard LVCMOS mode (non-I2C). For a full description of the pull drive strength programming, see PADCONFS bits of CONTROL_PADCONF_X control modules (standard LVCMOS mode), or prg_i2c2_pullupresx, prg_i2c2_lb1lb0, and prg_i2c3_pullupresx, prg_i2c3_lb1lb0 bits of the CONTROL_PROG_IO2, CONTROL_PROG_IO3 control modules (I2C mode) in the System Control Module chapter of the *AM/DM37x Multimedia Device Technical Reference Manual* (literature number SPRUGN4) to modify the IO settings if required by the targeted interface application.

(13)  Mux0 if sys_boot6 is pulled down (clock master).

(14) If MMC1 functional signals are enabled, vdds_mmc1 for MMC1 must be supplied by a dedicated power source.
If MMC1 functional signals are disabled, other multiplexed CMOS signals of the interface can be enabled. The interface can be supplied by the same power source as vdds. The vdds power source supplies the vdds_mmc1 ball.
If neither MMC1 functional balls or CMOS signals are enabled, the interface balls are left unconnected with its associated power supply (vdda/vssa) grounded.
For the corresponding setting of the PBIASLITEPWRDNZ0 bit, see the System Control Module / SCM Programming Model / Extended-Drain I/Os and PBIAS Cells Programming Guide section of the *AM/DM37x Multimedia Device Technical Reference Manual* (literature number SPRUGN4).

## 2.4 Multiplexing Characteristics

Table 2-4 provides a description of the multiplexing on the CBP, CBC, and CUS packages, respectively.

**Note**: The following does not take into account subsystem pin multiplexing options. Subsystem pin multiplexing options are described in Section 2.5, *Signal Description.* For more information, see the System Control Module / System Control Module Functional Description / Pad Functional Multiplexing and Configuration section of the *AM/DM37x Multimedia Device Technical Reference Manual* (literature number SPRUGN4).

### Table 2-4. Multiplexing Characteristics

| CBP | | CBC | | CUS | MODE 0 | MODE 1 | MODE 2 | MODE 3 | MODE 4 | MODE 5 | MODE 6 | MODE 7 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bottom | Top | Bottom | Top | | | | | | | | | |
| NA | J2 | NA | D1 | D7 | sdrc_d0 | | | | | | | |
| NA | J1 | NA | G1 | C5 | sdrc_d1 | | | | | | | |
| NA | G2 | NA | G2 | C6 | sdrc_d2 | | | | | | | |
| NA | G1 | NA | E1 | B5 | sdrc_d3 | | | | | | | |
| NA | F2 | NA | D2 | D9 | sdrc_d4 | | | | | | | |
| NA | F1 | NA | E2 | D10 | sdrc_d5 | | | | | | | |
| NA | D2 | NA | B3 | C7 | sdrc_d6 | | | | | | | |
| NA | D1 | NA | B4 | B7 | sdrc_d7 | | | | | | | |
| NA | B13 | NA | A10 | B11 | sdrc_d8 | | | | | | | |
| NA | A13 | NA | B11 | C12 | sdrc_d9 | | | | | | | |
| NA | B14 | NA | A11 | B12 | sdrc_d10 | | | | | | | |
| NA | A14 | NA | B12 | D13 | sdrc_d11 | | | | | | | |
| NA | B16 | NA | A16 | C13 | sdrc_d12 | | | | | | | |
| NA | A16 | NA | A17 | B14 | sdrc_d13 | | | | | | | |
| NA | B19 | NA | B17 | A14 | sdrc_d14 | | | | | | | |
| NA | A19 | NA | B18 | B15 | sdrc_d15 | | | | | | | |
| NA | B3 | NA | B7 | C9 | sdrc_d16 | | | | | | | |
| NA | A3 | NA | A5 | E12 | sdrc_d17 | | | | | | | |
| NA | B5 | NA | B6 | B8 | sdrc_d18 | | | | | | | |
| NA | A5 | NA | A6 | B9 | sdrc_d19 | | | | | | | |
| NA | B8 | NA | A8 | C10 | sdrc_d20 | | | | | | | |
| NA | A8 | NA | B9 | B10 | sdrc_d21 | | | | | | | |
| NA | B9 | NA | A9 | D12 | sdrc_d22 | | | | | | | |
| NA | A9 | NA | B10 | E13 | sdrc_d23 | | | | | | | |
| NA | B21 | NA | C21 | E15 | sdrc_d24 | | | | | | | |
| NA | A21 | NA | D20 | D15 | sdrc_d25 | | | | | | | |
| NA | D22 | NA | B19 | C15 | sdrc_d26 | | | | | | | |
| NA | D23 | NA | C20 | B16 | sdrc_d27 | | | | | | | |
| NA | E22 | NA | D21 | C16 | sdrc_d28 | | | | | | | |
| NA | E23 | NA | E20 | D16 | sdrc_d29 | | | | | | | |
| NA | G22 | NA | E21 | B17 | sdrc_d30 | | | | | | | |
| NA | G23 | NA | G21 | B18 | sdrc_d31 | | | | | | | |
| NA | AB21 | NA | AA18 | C18 | sdrc_ba0 | | | | | | | |
| NA | AC21 | NA | V20 | D18 | sdrc_ba1 | | | | | | | |
| NA | N22 | NA | G20 | A4 | sdrc_a0 | | | | | | | |
| NA | N23 | NA | K20 | B4 | sdrc_a1 | | | | | | | |
| NA | P22 | NA | J20 | D6 | sdrc_a2 | | | | | | | |
| NA | P23 | NA | J21 | B3 | sdrc_a3 | | | | | | | |
| NA | R22 | NA | U21 | B2 | sdrc_a4 | | | | | | | |
| NA | R23 | NA | R20 | C3 | sdrc_a5 | | | | | | | |
| NA | T22 | NA | M21 | E3 | sdrc_a6 | | | | | | | |
| NA | T23 | NA | M20 | F6 | sdrc_a7 | | | | | | | |
| NA | U22 | NA | N20 | E10 | sdrc_a8 | | | | | | | |
| NA | U23 | NA | K21 | E9 | sdrc_a9 | | | | | | | |

## Table 2-4. Multiplexing Characteristics (continued)

| CBP | | CBC | | CUS | MODE 0 | MODE 1 | MODE 2 | MODE 3 | MODE 4 | MODE 5 | MODE 6 | MODE 7 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bottom | Top | Bottom | Top | | | | | | | | | |
| NA | V22 | NA | Y16 | E7 | sdrc_a10 | | | | | | | |
| NA | V23 | NA | N21 | G6 | sdrc_a11 | | | | | | | |
| NA | W22 | NA | R21 | G7 | sdrc_a12 | | | | | | | |
| NA | W23 | NA | AA15 | F7 | sdrc_a13 | | | | | | | |
| NA | Y22 | NA | Y12 | F9 | sdrc_a14 | | | | | | | |
| NA | M22 | NA | T21 | A19 | sdrc_ncs0 | | | | | | | |
| NA | M23 | NA | T20 | B19 | sdrc_ncs1 | | | | | | | |
| NA | A11 | NA | A12 | A10 | sdrc_clk | | | | | | | |
| NA | B11 | NA | B13 | A11 | sdrc_nclk | | | | | | | |
| NA | J22 | NA | Y15 | B20 | sdrc_cke0 | | | | | | | safe_mode_out1 |
| NA | J23 | NA | Y13 | C20 | sdrc_cke1 | | | | | | | safe_mode_out1 |
| NA | L23 | NA | V21 | D19 | sdrc_nras | | | | | | | |
| NA | L22 | NA | U20 | C19 | sdrc_ncas | | | | | | | |
| NA | K23 | NA | Y18 | A20 | sdrc_nwe | | | | | | | |
| NA | C1 | NA | H1 | B6 | sdrc_dm0 | | | | | | | |
| NA | A17 | NA | A14 | B13 | sdrc_dm1 | | | | | | | |
| NA | A6 | NA | A4 | A7 | sdrc_dm2 | | | | | | | |
| NA | A20 | NA | A18 | A16 | sdrc_dm3 | | | | | | | |
| NA | C2 | NA | C2 | A5 | sdrc_dqs0 | | | | | | | |
| NA | B17 | NA | B15 | A13 | sdrc_dqs1 | | | | | | | |
| NA | B6 | NA | B8 | A8 | sdrc_dqs2 | | | | | | | |
| NA | B20 | NA | A19 | A17 | sdrc_dqs3 | | | | | | | |
| N4 | AC15 | J2 | NA | K4 | gpmc_a1 | | | | gpio_34 | | | safe_mode |
| M4 | AB15 | H1 | NA | K3 | gpmc_a2 | | | | gpio_35 | | | safe_mode |
| L4 | AC16 | H2 | NA | K2 | gpmc_a3 | | | | gpio_36 | | | safe_mode |
| K4 | AB16 | G2 | NA | J4 | gpmc_a4 | | | | gpio_37 | | | safe_mode |
| T3 | AC17 | F1 | NA | J3 | gpmc_a5 | | | | gpio_38 | | | safe_mode |
| R3 | AB17 | F2 | NA | J2 | gpmc_a6 | | | | gpio_39 | | | safe_mode |
| N3 | AC18 | E1 | NA | J1 | gpmc_a7 | | | | gpio_40 | | | safe_mode |
| M3 | AB18 | E2 | NA | H1 | gpmc_a8 | | | | gpio_41 | | | safe_mode |
| L3 | AC19 | D1 | NA | H2 | gpmc_a9 | sys_ndmareq2 | | | gpio_42 | | | safe_mode |
| K3 | AB19 | D2 | NA | G2 | gpmc_a10 | sys_ndmareq3 | | | gpio_43 | | | safe_mode |
| NA | AC20 | A4 | NA | NA | gpmc_a11 | | | | | | | safe_mode |
| K1 | M2 | AA2 | U2 | L2 | gpmc_d0 | | | | | | | |
| L1 | M1 | AA1 | U1 | M1 | gpmc_d1 | | | | | | | |
| L2 | N2 | AC2 | V2 | M2 | gpmc_d2 | | | | | | | |
| P2 | N1 | AC1 | V1 | N2 | gpmc_d3 | | | | | | | |
| T1 | R2 | AE5 | AA3 | M3 | gpmc_d4 | | | | | | | |
| V1 | R1 | AD6 | AA4 | P1 | gpmc_d5 | | | | | | | |
| V2 | T2 | AD5 | Y3 | P2 | gpmc_d6 | | | | | | | |
| W2 | T1 | AC5 | Y4 | R1 | gpmc_d7 | | | | | | | |
| H2 | AB3 | V1 | R1 | R2 | gpmc_d8 | | | | gpio_44 | | | safe_mode |
| K2 | AC3 | Y1 | T1 | T2 | gpmc_d9 | | | | gpio_45 | | | safe_mode |
| P1 | AB4 | T1 | N1 | U1 | gpmc_d10 | | | | gpio_46 | | | safe_mode |

## Table 2-4. Multiplexing Characteristics (continued)

| CBP | | CBC | | CUS | MODE 0 | MODE 1 | MODE 2 | MODE 3 | MODE 4 | MODE 5 | MODE 6 | MODE 7 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bottom | Top | Bottom | Top | | | | | | | | | |
| R1 | AC4 | U2 | P2 | R3 | gpmc_d11 | | | | gpio_47 | | | safe_mode |
| R2 | AB6 | U1 | P1 | T3 | gpmc_d12 | | | | gpio_48 | | | safe_mode |
| T2 | AC6 | P1 | M1 | U2 | gpmc_d13 | | | | gpio_49 | | | safe_mode |
| W1 | AB7 | L2 | J2 | V1 | gpmc_d14 | | | | gpio_50 | | | safe_mode |
| Y1 | AC7 | M2 | K2 | V2 | gpmc_d15 | | | | gpio_51 | | | safe_mode |
| G4 | Y2 | AD8 | AA8 | E2 | gpmc_ncs0 | | | | | | | |
| H3 | Y1 | AD1 | W1 | NA | gpmc_ncs1 | | | | gpio_52 | | | safe_mode |
| V8 | NA | A3 | NA | NA | gpmc_ncs2 | | | | gpio_53 | | | safe_mode |
| U8 | NA | B6 | NA | D2 | gpmc_ncs3 | sys_ndmareq0 | | | gpio_54 | | | safe_mode |
| T8 | NA | B4 | NA | F4 | gpmc_ncs4 | sys_ndmareq1 | mcbsp4_clkx | gpt_9_pwm_evt | gpio_55 | | | safe_mode |
| R8 | NA | C4 | NA | G5 | gpmc_ncs5 | sys_ndmareq2 | mcbsp4_dr | gpt_10_pwm_evt | gpio_56 | | | safe_mode |
| P8 | NA | B5 | NA | F3 | gpmc_ncs6 | sys_ndmareq3 | mcbsp4_dx | gpt_11_pwm_evt | gpio_57 | | | safe_mode |
| N8 | NA | C5 | NA | G4 | gpmc_ncs7 | gpmc_io_dir | mcbsp4_fsx | gpt_8_pwm_evt | gpio_58 | | | safe_mode |
| T4 | W2 | N1 | L1 | W2 | gpmc_clk | | | | gpio_59 | | | safe_mode |
| F3 | W1 | AD10 | AA9 | F1 | gpmc_nadv_ale | | | | | | | |
| G2 | V2 | N2 | L2 | F2 | gpmc_noe | | | | | | | |
| F4 | V1 | M1 | K1 | G3 | gpmc_nwe | | | | | | | |
| G3 | AC12 | K2 | NA | K5 | gpmc_nbe0_cle | | | | gpio_60 | | | safe_mode |
| U3 | NA | J1 | NA | L1 | gpmc_nbe1 | | | | gpio_61 | | | safe_mode |
| H1 | AB10 | AC6 | Y5 | E1 | gpmc_nwp | | | | gpio_62 | | | safe_mode |
| M8 | AB12 | AC11 | Y10 | C1 | gpmc_wait0 | | | | | | | |
| L8 | AC10 | AC8 | Y8 | NA | gpmc_wait1 | | | | gpio_63 | | | safe_mode |
| K8 | NA | B3 | NA | NA | gpmc_wait2 | | uart4_tx | | gpio_64 | | | safe_mode |
| J8 | NA | C6 | NA | C2 | gpmc_wait3 | sys_ndmareq1 | uart4_rx[3] | | gpio_65 | | | safe_mode |
| D28 | NA | G25 | NA | G22 | dss_pclk | | | | gpio_66 | hw_dbg12 | | safe_mode |
| D26 | NA | K24 | NA | E22 | dss_hsync | | | | gpio_67 | hw_dbg13 | | safe_mode |
| D27 | NA | M25 | NA | F22 | dss_vsync | | | | gpio_68 | | | safe_mode |
| E27 | NA | F26 | NA | J21 | dss_acbias | | | | gpio_69 | | | safe_mode |
| AG22 | NA | AE21 | NA | AC19 | dss_data0 | | uart1_cts | | gpio_70 | | | safe_mode |
| AH22 | NA | AE22 | NA | AB19 | dss_data1 | | uart1_rts | | gpio_71 | | | safe_mode |
| AG23 | NA | AE23 | NA | AD20 | dss_data2 | | | | gpio_72 | | | safe_mode |
| AH23 | NA | AE24 | NA | AC20 | dss_data3 | | | | gpio_73 | | | safe_mode |
| AG24 | NA | AD23 | NA | AD21 | dss_data4 | | uart3_rx_irrx | | gpio_74 | | | safe_mode |
| AH24 | NA | AD24 | NA | AC21 | dss_data5 | | uart3_tx_irtx | | gpio_75 | | | safe_mode |
| E26 | NA | G26 | NA | D24 | dss_data6 | | uart1_tx | | gpio_76 | hw_dbg14 | | safe_mode |

### Table 2-4. Multiplexing Characteristics (continued)

| CBP | | CBC | | CUS | MODE 0 | MODE 1 | MODE 2 | MODE 3 | MODE 4 | MODE 5 | MODE 6 | MODE 7 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bottom | Top | Bottom | Top | | | | | | | | | |
| F28 | NA | H25 | NA | E23 | dss_data7 | | uart1_rx | | gpio_77 | hw_dbg15 | | safe_mode |
| F27 | NA | H26 | NA | E24 | dss_data8 | | uart3_rx_irrx | | gpio_78 | hw_dbg16 | | safe_mode |
| G26 | NA | J26 | NA | F23 | dss_data9 | | uart3_tx_irtx | | gpio_79 | hw_dbg17 | | safe_mode |
| AD28 | NA | AC26 | NA | AC22 | dss_data10 | | | | gpio_80 | | | safe_mode |
| AD27 | NA | AD26 | NA | AC23 | dss_data11 | | | | gpio_81 | | | safe_mode |
| AB28 | NA | AA25 | NA | AB22 | dss_data12 | | | | gpio_82 | | | safe_mode |
| AB27 | NA | Y25 | NA | Y22 | dss_data13 | | | | gpio_83 | | | safe_mode |
| AA28 | NA | AA26 | NA | W22 | dss_data14 | | | | gpio_84 | | | safe_mode |
| AA27 | NA | AB26 | NA | V22 | dss_data15 | | | | gpio_85 | | | safe_mode |
| G25 | NA | L25 | NA | J22 | dss_data16 | | | | gpio_86 | | | safe_mode |
| H27 | NA | L26 | NA | G23 | dss_data17 | | | | gpio_87 | | | safe_mode |
| H26 | NA | M24 | NA | G24 | dss_data18 | | mcspi3_clk | dss_data0 | gpio_88 | | | safe_mode |
| H25 | NA | M26 | NA | H23 | dss_data19 | | mcspi3_simo | dss_data1 | gpio_89 | | | safe_mode |
| E28 | NA | F25 | NA | D23 | dss_data20 | | mcspi3_somi | dss_data2 | gpio_90 | | | safe_mode |
| J26 | NA | N24 | NA | K22 | dss_data21 | | mcspi3_cs0 | dss_data3 | gpio_91 | | | safe_mode |
| AC27 | NA | AC25 | NA | V21 | dss_data22 | | mcspi3_cs1 | dss_data4 | gpio_92 | | | safe_mode |
| AC28 | NA | AB25 | NA | W21 | dss_data23 | | | dss_data5 | gpio_93 | | | safe_mode |
| W28 | NA | V26 | NA | AA23 | cvideo2_out | | | | | | | |
| Y28 | NA | W26 | NA | AB24 | cvideo1_out | | | | | | | |
| Y27 | NA | W25 | NA | AB23 | cvideo1_vfb | | | | | | | |
| W27 | NA | U24 | NA | Y23 | cvideo2_vfb | | | | | | | |
| W26 | NA | V23 | NA | Y24 | cvideo1_rset | | | | | | | |
| A24 | NA | C23 | NA | A22 | cam_hs | | | | gpio_94 | hw_dbg0 | | safe_mode |
| A23 | NA | D23 | NA | E18 | cam_vs | | | | gpio_95 | hw_dbg1 | | safe_mode |
| C25 | NA | C25 | NA | B22 | cam_xclka | | | | gpio_96 | | | safe_mode |
| C27 | NA | C26 | NA | J19 | cam_pclk | | | | gpio_97 | hw_dbg2 | | safe_mode |
| C23 | NA | B23 | NA | H24 | cam_fld | | cam_global_reset | | gpio_98 | hw_dbg3 | | safe_mode |
| AG17 | NA | AE16 | NA | AB18 | cam_d0 | | | | gpio_99[1] | | | safe_mode |
| AH17 | NA | AE15 | NA | AC18 | cam_d1 | | | | gpio_100[1] | | | safe_mode |
| B24 | NA | A24 | NA | G19 | cam_d2 | | | | gpio_101 | hw_dbg4 | | safe_mode |
| C24 | NA | B24 | NA | F19 | cam_d3 | | | | gpio_102 | hw_dbg5 | | safe_mode |
| D24 | NA | D24 | NA | G20 | cam_d4 | | | | gpio_103 | hw_dbg6 | | safe_mode |
| A25 | NA | C24 | NA | B21 | cam_d5 | | | | gpio_104 | hw_dbg7 | | safe_mode |
| K28 | NA | P25 | NA | L24 | cam_d6 | | | | gpio_105[1] | | | safe_mode |
| L28 | NA | P26 | NA | K24 | cam_d7 | | | | gpio_106[1] | | | safe_mode |

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## Table 2-4. Multiplexing Characteristics (continued)

| CBP Bottom | CBP Top | CBC Bottom | CBC Top | CUS | MODE 0 | MODE 1 | MODE 2 | MODE 3 | MODE 4 | MODE 5 | MODE 6 | MODE 7 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| K27 | NA | N25 | NA | J23 | cam_d8 | | | | gpio_107[1] | | | safe_mode |
| L27 | NA | N26 | NA | K23 | cam_d9 | | | | gpio_108[1] | | | safe_mode |
| B25 | NA | D25 | NA | F21 | cam_d10 | | | | gpio_109 | hw_dbg8 | | safe_mode |
| C26 | NA | E26 | NA | G21 | cam_d11 | | | | gpio_110 | hw_dbg9 | | safe_mode |
| B26 | NA | E25 | NA | C22 | cam_xclkb | | | | gpio_111 | | | safe_mode |
| B23 | NA | A23 | NA | F18 | cam_wen | | cam_shutter | | gpio_167 | hw_dbg10 | | safe_mode |
| D25 | NA | D26 | NA | J20 | cam_strobe | | | | gpio_126 | hw_dbg11 | | safe_mode |
| AG19 | NA | AD17 | NA | NA | | | | | gpio_112[1] | | | safe_mode |
| AH19 | NA | AD16 | NA | NA | | | | | gpio_113[1] | | | safe_mode |
| AG18 | NA | AE18 | NA | NA | | | | | gpio_114[1] | | | safe_mode |
| AH18 | NA | AE17 | NA | NA | | | | | gpio_115[1] | | | safe_mode |
| P21 | NA | U18 | NA | V20 | mcbsp2_fsx | | | | gpio_116 | | | safe_mode |
| N21 | NA | R18 | NA | T21 | mcbsp2_clkx | | | | gpio_117 | | | safe_mode |
| R21 | NA | T18 | NA | V19 | mcbsp2_dr | | | | gpio_118 | | | safe_mode |
| M21 | NA | R19 | NA | R20 | mcbsp2_dx | | | | gpio_119 | | | safe_mode |
| N28 | NA | N19 | NA | M23 | mmc1_clk | | | | gpio_120[2] | | | safe_mode |
| M27 | NA | L18 | NA | L23 | mmc1_cmd | | | | gpio_121[2] | | | safe_mode |
| N27 | NA | M19 | NA | M22 | mmc1_dat0 | | | | gpio_122[2] | | | safe_mode |
| N26 | NA | M18 | NA | M21 | mmc1_dat1 | | | | gpio_123[2] | | | safe_mode |
| N25 | NA | K18 | NA | M20 | mmc1_dat2 | | | | gpio_124[2] | | | safe_mode |
| P28 | NA | N20 | NA | N23 | mmc1_dat3 | | | | gpio_125[2] | | | safe_mode |
| P27 | NA | M20 | NA | N22 | | | | | gpio_126[2] | | | safe_mode |
| P26 | NA | P17 | NA | NA | | | | | gpio_127[2] | | | safe_mode |
| R27 | NA | P18 | NA | NA | | | | | gpio_128 | | | safe_mode |
| R25 | NA | P19 | NA | P24 | | | | | gpio_129[2] | | | safe_mode |
| AE2 | NA | W10 | NA | Y1 | mmc2_clk | mcspi3_clk | | | gpio_130 | | | safe_mode |
| AG5 | NA | R10 | NA | AB5 | mmc2_cmd | mcspi3_simo | | | gpio_131 | | | safe_mode |
| AH5 | NA | T10 | NA | AB3 | mmc2_dat0 | mcspi3_somi | | | gpio_132 | | | safe_mode |
| AH4 | NA | T9 | NA | Y3 | mmc2_dat1 | | | | gpio_133 | | | safe_mode |
| AG4 | NA | U10 | NA | W3 | mmc2_dat2 | mcspi3_cs1 | | | gpio_134 | | | safe_mode |
| AF4 | NA | U9 | NA | V3 | mmc2_dat3 | mcspi3_cs0 | | | gpio_135 | | | safe_mode |
| AE4 | NA | V10 | NA | AB2 | mmc2_dat4 | mmc2_dir_dat0 | | mmc3_dat0 | gpio_136 | | | safe_mode |
| AH3 | NA | M3 | NA | AA2 | mmc2_dat5 | mmc2_dir_dat1 | cam_global_reset | mmc3_dat1 | gpio_137 | | mm3_rxdp | safe_mode |

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**Table 2-4. Multiplexing Characteristics (continued)**

| CBP | | CBC | | CUS | MODE 0 | MODE 1 | MODE 2 | MODE 3 | MODE 4 | MODE 5 | MODE 6 | MODE 7 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bottom | Top | Bottom | Top | | | | | | | | | |
| AF3 | NA | L3 | NA | Y2 | mmc2_dat6 | mmc2_dir_cmd | cam_shutter | mmc3_dat2 | gpio_138 | | | safe_mode |
| AE3 | NA | K3 | NA | AA1 | mmc2_dat7 | mmc2_clkin | | mmc3_dat3 | gpio_139 | | mm3_rxdm | safe_mode |
| AF6 | NA | P3 | NA | V6 | mcbsp3_dx | uart2_cts | | | gpio_140 | | | safe_mode |
| AE6 | NA | N3 | NA | V5 | mcbsp3_dr | uart2_rts | | | gpio_141 | | | safe_mode |
| AF5 | NA | U3 | NA | W4 | mcbsp3_clkx | uart2_tx | | | gpio_142 | | | safe_mode |
| AE5 | NA | W3 | NA | V4 | mcbsp3_fsx | uart2_rx | | | gpio_143 | | | safe_mode |
| AB26 | NA | Y24 | NA | NA | uart2_cts | mcbsp3_dx | gpt_9_pwm_evt | | gpio_144 | | | safe_mode |
| AB25 | NA | AA24 | NA | NA | uart2_rts | mcbsp3_dr | gpt_10_pwm_evt | | gpio_145 | | | safe_mode |
| AA25 | NA | AD22 | NA | NA | uart2_tx | mcbsp3_clkx | gpt_11_pwm_evt | | gpio_146 | | | safe_mode |
| AD25 | NA | AD21 | NA | NA | uart2_rx | mcbsp3_fsx | gpt_8_pwm_evt | | gpio_147 | | | safe_mode |
| AA8 | NA | L4 | NA | W7 | uart1_tx | | | | gpio_148 | | | safe_mode |
| AA9 | NA | R2 | NA | W6 | uart1_rts | | | | gpio_149 | | | safe_mode |
| W8 | NA | W2 | NA | AC2 | uart1_cts | | | | gpio_150 | | | safe_mode |
| Y8 | NA | H3 | NA | V7 | uart1_rx | | mcbsp1_clkr | mcspi4_clk | gpio_151 | | | safe_mode |
| AE1 | NA | V3 | NA | NA | mcbsp4_clkx | | | | gpio_152 | | mm3_txse0 | safe_mode |
| AD1 | NA | U4 | NA | NA | mcbsp4_dr | | | | gpio_153 | | mm3_rxrcv | safe_mode |
| AD2 | NA | R3 | NA | NA | mcbsp4_dx | | | | gpio_154 | | mm3_txdat | safe_mode |
| AC1 | NA | T3 | NA | NA | mcbsp4_fsx | | | | gpio_155 | | mm3_txen_n | safe_mode |
| Y21 | NA | U19 | NA | W19 | mcbsp1_clkr | mcspi4_clk | | | gpio_156 | | | safe_mode |
| AA21 | NA | V17 | NA | AB20 | mcbsp1_fsr | | cam_global_reset | | gpio_157 | | | safe_mode |
| V21 | NA | U17 | NA | W18 | mcbsp1_dx | mcspi4_simo | mcbsp3_dx | | gpio_158 | | | safe_mode |
| U21 | NA | T20 | NA | Y18 | mcbsp1_dr | mcspi4_somi | mcbsp3_dr | | gpio_159 | | | safe_mode |
| T21 | NA | T19 | NA | AA18 | mcbsp_clks | | cam_shutter | | gpio_160 | uart1_cts | | safe_mode |
| K26 | NA | P20 | NA | AA19 | mcbsp1_fsx | mcspi4_cs0 | mcbsp3_fsx | | gpio_161 | | | safe_mode |
| W21 | NA | T17 | NA | V18 | mcbsp1_clkx | | mcbsp3_clkx | | gpio_162 | | | safe_mode |
| H18 | NA | F23 | NA | A23 | uart3_cts_rctx | | | | gpio_163 | | | safe_mode |
| H19 | NA | F24 | NA | B23 | uart3_rts_sd | | | | gpio_164 | | | safe_mode |
| H20 | NA | H24 | NA | B24 | uart3_rx_irrx | | | | gpio_165 | | | safe_mode |
| H21 | NA | G24 | NA | C23 | uart3_tx_irtx | | | | gpio_166 | | | safe_mode |
| T28 | NA | W19 | NA | R21 | hsusb0_clk | | | | gpio_120 | | | safe_mode |
| T25 | NA | U20 | NA | R23 | hsusb0_stp | | | | gpio_121 | | | safe_mode |
| R28 | NA | V19 | NA | P23 | hsusb0_dir | | | | gpio_122 | | | safe_mode |
| T26 | NA | W18 | NA | R22 | hsusb0_nxt | | | | gpio_124 | | | safe_mode |

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**Table 2-4. Multiplexing Characteristics (continued)**

| CBP | | CBC | | CUS | MODE 0 | MODE 1 | MODE 2 | MODE 3 | MODE 4 | MODE 5 | MODE 6 | MODE 7 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bottom | Top | Bottom | Top | | | | | | | | | |
| T27 | NA | V20 | NA | T24 | hsusb0_data0 | | uart3_tx_irtx | | gpio_125 | uart2_tx | | safe_mode |
| U28 | NA | Y20 | NA | T23 | hsusb0_data1 | | uart3_rx_irrx | | gpio_130 | uart2_rx | | safe_mode |
| U27 | NA | V18 | NA | U24 | hsusb0_data2 | | uart3_rts_sd | | gpio_131 | uart2_rts | | safe_mode |
| U26 | NA | W20 | NA | U23 | hsusb0_data3 | | uart3_cts_rctx | | gpio_169 | uart2_cts | | safe_mode |
| U25 | NA | W17 | NA | W24 | hsusb0_data4 | | | | gpio_188 | | | safe_mode |
| V28 | NA | Y18 | NA | V23 | hsusb0_data5 | | | | gpio_189 | | | safe_mode |
| V27 | NA | Y19 | NA | W23 | hsusb0_data6 | | | | gpio_190 | | | safe_mode |
| V26 | NA | Y17 | NA | T22 | hsusb0_data7 | | | | gpio_191 | | | safe_mode |
| K21 | NA | J25 | NA | K20 | i2c1_scl | | | | | | | |
| J21 | NA | J24 | NA | K21 | i2c1_sda | | | | | | | |
| AF15 | NA | C2 | NA | AC15 | i2c2_scl | | | | gpio_168 | | | safe_mode |
| AE15 | NA | C1 | NA | AC14 | i2c2_sda | | | | gpio_183 | | | safe_mode |
| AF14 | NA | AB4 | NA | AC13 | i2c3_scl | | | | gpio_184 | | | safe_mode |
| AG14 | NA | AC4 | NA | AC12 | i2c3_sda | | | | gpio_185 | | | safe_mode |
| AD26 | NA | AD15 | NA | Y16 | i2c4_scl | sys_nvmode1 | | | | | | safe_mode |
| AE26 | NA | W16 | NA | Y15 | i2c4_sda | sys_nvmode2 | | | | | | safe_mode |
| J25 | NA | J23 | NA | A24 | hdq_sio | sys_altclk | i2c2_sccbe | i2c3_sccbe | gpio_170 | | | safe_mode |
| AB3 | NA | P9 | NA | T5 | mcspi1_clk | mmc2_dat4 | | | gpio_171 | | | safe_mode |
| AB4 | NA | P8 | NA | R4 | mcspi1_simo | mmc2_dat5 | | | gpio_172 | | | safe_mode |
| AA4 | NA | P7 | NA | T4 | mcspi1_somi | mmc2_dat6 | | | gpio_173 | | | safe_mode |
| AC2 | NA | R7 | NA | T6 | mcspi1_cs0 | mmc2_dat7 | | | gpio_174 | | | safe_mode |
| AC3 | NA | R8 | NA | NA | mcspi1_cs1 | | | mmc3_cmd | gpio_175 | | | safe_mode |
| AB1 | NA | R9 | NA | NA | mcspi1_cs2 | | | mmc3_clk | gpio_176 | | | safe_mode |
| AB2 | NA | T8 | NA | R5 | mcspi1_cs3 | | | hsusb2_data2 | gpio_177 | mm2_txdat | | safe_mode |
| AA3 | NA | W7 | NA | N5 | mcspi2_clk | | | hsusb2_data7 | gpio_178 | | | safe_mode |
| Y2 | NA | W8 | NA | N4 | mcspi2_simo | gpt_9_pwm_evt | | hsusb2_data4 | gpio_179 | | | safe_mode |
| Y3 | NA | U8 | NA | N3 | mcspi2_somi | gpt_10_pwm_evt | | hsusb2_data5 | gpio_180 | | | safe_mode |
| Y4 | NA | V8 | NA | M5 | mcspi2_cs0 | gpt_11_pwm_evt | | hsusb2_data6 | gpio_181 | | | safe_mode |
| V3 | NA | V9 | NA | M4 | mcspi2_cs1 | gpt_8_pwm_evt | | hsusb2_data3 | gpio_182 | mm2_txen_n | | safe_mode |
| AE25 | NA | AE20 | NA | AA16 | sys_32k | | | | | | | |
| AE17 | NA | AF19 | NA | AD15 | sys_xtalin | | | | | | | |
| AF17 | NA | AF20 | NA | AD14 | sys_xtalout | | | | | | | |
| AF25 | NA | W15 | NA | Y13 | sys_clkreq | | | | gpio_1 | | | safe_mode |
| AF26 | NA | V16 | NA | W16 | sys_nirq | | | | gpio_0 | | | safe_mode |
| AH25 | NA | V13 | NA | AA10 | sys_nrespwron | | | | | | | |

## Table 2-4. Multiplexing Characteristics (continued)

| CBP | | CBC | | CUS | MODE 0 | MODE 1 | MODE 2 | MODE 3 | MODE 4 | MODE 5 | MODE 6 | MODE 7 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bottom | Top | Bottom | Top | | | | | | | | | |
| AF24 | NA | AD7 | AA5 | Y10 | sys_nreswarm | | | | gpio_30 | | | safe_mode |
| AH26 | NA | F3 | NA | AB12 | sys_boot0 | | | dss_data18 | gpio_2 | | | safe_mode |
| AG26 | NA | D3 | NA | AC16 | sys_boot1 | | | dss_data19 | gpio_3 | | | safe_mode |
| AE14 | NA | C3 | NA | AD17 | sys_boot2 | | | | gpio_4 | | | safe_mode |
| AF18 | NA | E3 | NA | AD18 | sys_boot3 | | | dss_data20 | gpio_5 | | | safe_mode |
| AF19 | NA | E4 | NA | AC17 | sys_boot4 | mmc2_dir_dat2 | | dss_data21 | gpio_6 | | | safe_mode |
| AE21 | NA | G3 | NA | AB16 | sys_boot5 | mmc2_dir_dat3 | | dss_data22 | gpio_7 | | | safe_mode |
| AF21 | NA | D4 | NA | AA15 | sys_boot6 | | | dss_data23 | gpio_8 | | | safe_mode |
| AF22 | NA | V12 | NA | AD23 | sys_off_mode | | | | gpio_9 | | | safe_mode |
| AG25 | NA | AE14 | NA | Y7 | sys_clkout1 | | | | gpio_10 | | | safe_mode |
| AE22 | NA | W11 | NA | AA6 | sys_clkout2 | | | | gpio_186 | | | safe_mode |
| AA17 | NA | U15 | NA | AB7 | jtag_ntrst | | | | | | | |
| AA13 | NA | V14 | NA | AB6 | jtag_tck | | | | | | | |
| AA12 | NA | W13 | NA | AA7 | jtag_rtck | | | | | | | |
| AA18 | NA | V15 | NA | AA9 | jtag_tms_tmsc | | | | | | | |
| AA20 | NA | U16 | NA | AB10 | jtag_tdi | | | | | | | |
| AA19 | NA | Y13 | NA | AB9 | jtag_tdo | | | | | | | |
| AA11 | NA | Y15 | NA | AC24 | jtag_emu0 | | | | gpio_11 | | | safe_mode |
| AA10 | NA | Y14 | NA | AD24 | jtag_emu1 | | | | gpio_31 | | | safe_mode |
| AF10 | NA | AB2 | NA | AC1 | etk_clk | mcbsp5_clkx | mmc3_clk | hsusb1_stp | gpio_12 | mm1_rxdp | | hw_dbg0 |
| AE10 | NA | AB3 | NA | AD3 | etk_ctl | | mmc3_cmd | hsusb1_clk | gpio_13 | | | hw_dbg1 |
| AF11 | NA | AC3 | NA | AD6 | etk_d0 | mcspi3_simo | mmc3_dat4 | hsusb1_data0 | gpio_14 | mm1_rxrcv | | hw_dbg2 |
| AG12 | NA | AD4 | NA | AC6 | etk_d1 | mcspi3_somi | | hsusb1_data1 | gpio_15 | mm1_txse0 | | hw_dbg3 |
| AH12 | NA | AD3 | NA | AC7 | etk_d2 | mcspi3_cs0 | | hsusb1_data2 | gpio_16 | mm1_txdat | | hw_dbg4 |
| AE13 | NA | AA3 | NA | AD8 | etk_d3 | mcspi3_clk | mmc3_dat3 | hsusb1_data7 | gpio_17 | | | hw_dbg5 |
| AE11 | NA | Y3 | NA | AC5 | etk_d4 | mcbsp5_dr | mmc3_dat0 | hsusb1_data4 | gpio_18 | | | hw_dbg6 |
| AH9 | NA | AB1 | NA | AD2 | etk_d5 | mcbsp5_fsx | mmc3_dat1 | hsusb1_data5 | gpio_19 | | | hw_dbg7 |
| AF13 | NA | AE3 | NA | AC8 | etk_d6 | mcbsp5_dx | mmc3_dat2 | hsusb1_data6 | gpio_20 | | | hw_dbg8 |
| AH14 | NA | AD2 | NA | AD9 | etk_d7 | mcspi3_cs1 | mmc3_dat7 | hsusb1_data3 | gpio_21 | mm1_txen_n | | hw_dbg9 |
| AF9 | NA | AA4 | NA | AC4 | etk_d8 | | mmc3_dat6 | hsusb1_dir | gpio_22 | | | hw_dbg10 |
| AG9 | NA | V2 | NA | AD5 | etk_d9 | | mmc3_dat5 | hsusb1_nxt | gpio_23 | mm1_rxdm | | hw_dbg11 |
| AE7 | NA | AE4 | NA | AC3 | etk_d10 | | uart1_rx | hsusb2_clk | gpio_24 | | | hw_dbg12 |
| AF7 | NA | AF6 | NA | AC9 | etk_d11 | | | hsusb2_stp | gpio_25 | mm2_rxdp | | hw_dbg13 |
| AG7 | NA | AE6 | NA | AC10 | etk_d12 | | | hsusb2_dir | gpio_26 | | | hw_dbg14 |
| AH7 | NA | AF7 | NA | AD11 | etk_d13 | | | hsusb2_nxt | gpio_27 | mm2_rxdm | | hw_dbg15 |

## Table 2-4. Multiplexing Characteristics (continued)

| CBP | | CBC | | CUS | MODE 0 | MODE 1 | MODE 2 | MODE 3 | MODE 4 | MODE 5 | MODE 6 | MODE 7 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Bottom** | **Top** | **Bottom** | **Top** | | | | | | | | | |
| AG8 | NA | AF9 | NA | AC11 | etk_d14 | | | hsusb2_data0 | gpio_28 | mm2_rxrcv | | hw_dbg 16 |
| AH8 | NA | AE9 | NA | AD12 | etk_d15 | | | hsusb2_data1 | gpio_29 | mm2_txse0 | | hw_dbg 17 |
| AC4, J4, H4, D8, AE9, D9, D15, Y16, AE18, Y18, W18, K18, J18, AE19, Y19, U19, T19, N19, M19, J19, Y20, W20, V20, U20, P20, N20, K20, J20, D22, D23, AE24, M25, L25, E25 | NA | AC21, D15, G11, G18, H20, M7, M17, R20, T7, Y8, Y12 | NA | F12, F13, G12, G13, H12, H13, J17, J18, K17, K18, K19, L14, L15, M14, M15, R17, R18, R19, T17, T18, T19, T20 | vdd_core | | | | | | | |
| Y9, W9, T9, R9, M9, L9, J9, Y10, U10, T10, R10, N10, M10, L10, J10, Y11, W11, K11, J11, W12, K13, Y14, K14, J14, Y15, W15, J15 | NA | D13, G9, G12, H7, K11, L9, M9, M10, N7, N8, P10, U7, U11, U13, V7, V11, W9, Y9, Y11 | NA | F10, G9, G10, H9, H10, J9, J10, L11, L12, M6, M7, M8, M12, N6, N7, N8, R6, R7, R8, T7, T8, U12, U13, V12, V13, W12, W13 | vdd_mpu_iva | | | | | | | |
| U4 | NA | D6 | NA | N21 | cap_vdd_bb_mpu_iva | | | | | | | |
| AA15 | NA | K14 | NA | Y12 | cap_vddu_wkup_logic | | | | | | | |
| K15 | NA | K13 | NA | G18 | vdda_dplls_dll | | | | | | | |
| W16 | NA | U12 | NA | AA12 | vdds_sram | | | | | | | |
| AD3, AD4, W4, AF8, AE8, AF16, AE16, AF23, AE23, F25, F26, AG27 | NA | A18, AC7, AC15, AC18, AC24, AD20, AE10, C11, D9, E24, G4, J15, J18, L7, L24, M4, T4, T24, W24, Y4, AB24 | A3,A15,B5,F2,F21,L20,W21 | M17, M18, M19, N17, N18, N19, U10, V9, V10, W9, W10, Y9 | vdds | | | | | | | |
| U1, J1, F1, J2, F2, R4, B5, A5, AH6, B8, A8, B12, A12, D16, C16, B18, A18, B22, A22, G28, C28 | AC5, P1, H1, F23, E1, C23, A4, A7, A10, A15, A18 | NA | NA | E16, F15, F16, G15, G16, H15, J6, J7, J8, K6, K7, K8 | vdds_mem | | | | | | | |
| AA16 | NA | U14 | NA | U17 | vdda_dpll_per | | | | | | | |
| AA14 | NA | W14 | NA | AA13 | vdda_wkup_bg_bb | | | | | | | |

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## Table 2-4. Multiplexing Characteristics (continued)

| CBP | | CBC | | CUS | MODE 0 | MODE 1 | MODE 2 | MODE 3 | MODE 4 | MODE 5 | MODE 6 | MODE 7 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bottom | Top | Bottom | Top | | | | | | | | | |
| AG2, U2, B2, AG3, W3, P3, J3, E3, A3, P4, E4, AG6, D7, C7, V9, U9, P9, N9, K9, W10, V10, P10, K10, D10, C10, AF12, AE12, Y12, K12, J12, Y13, W13, J13, D13, C13, W14, K16, J16, W17, K17, J17, W19, V19, R19, P19, L19, K19, D19, C19, AF20, AE20, T20, AG15, AF2, AF27, B15, J27, M2, M26, N2, AA2, AG10, AC25, AC26, Y25, W25, M20, L20, L26, G27, D21, C22, B27, A26, R20, R26 | B4, B7, B10, B15, B18, C22, E2, F22, H2, P2, AB5, AB14, AB20 | A6, A8, A13, AB5, AB22, AC10, AD14, AD25, AE7, B2, B25, C12, D7, D10, D12, D14, D18, D20, E22, G1, G8, G10, G20, G23, H4, K1, K15, K25, L10, L17, L23, N4, N10, N17, R1, R4, R17, T23, U25, W1, W4, W23, Y7, Y10, Y16, Y26 | A7, A13, B14, C1, F1, F20, H2, H20, L21, M2, P20, R2, W20 Y6, Y11, AA7, AA16 | H11, H14, H16, J11, J12, J13, J14, J15, J16, K10, K11, K14, K15, L8, L10, L13, L17, M9, M10, M11, M13, M16, N9, N10, N11, N12, N13, N14, N15, N16, P8, P10, P11, P12, P13, P14, P15, P17, R10, R11, R14, R15, T9, T10, T11, T12, T13, T14, T15, T16, U9, U11, U14, U15, U16, V15, V16 | vss | | | | | | | |
| V25 | NA | V25 | NA | AB13 | vdda_dac | | | | | | | |
| Y26 | NA | V24 | NA | AB15 | vssa_dac | | | | | | | |
| K25 | NA | N23 | NA | N24 | vdds_mmc1 | | | | | | | |
| P25 | NA | P23 | NA | H8 | vdds_x | | | | | | | |
| AG21 | NA | AD19 | NA | NA | vdds | | | | | | | |
| AH20 | NA | AE19 | NA | N20 | cap_vddu_array | | | | | | | |
| AH21 | NA | AC19 | NA | NA | vss | | | | | | | |
| AG16 | NA | AC16 | NA | NA | vss | | | | | | | |
| AG20 | NA | AD18 | NA | NA | vdds | | | | | | | |
| M28 | NA | L19 | NA | NA | vss | | | | | | | |
| H28 | NA | L20 | NA | NA | vdds | | | | | | | |
| V4 | NA | N9 | NA | U8 | cap_vdd_sram_mpu_iva | | | | | | | |
| L21 | NA | K20 | NA | H17 | cap_vdd_sram_core | | | | | | | |
| Y17 | NA | AF23 | NA | W15 | sys_xtalgnd | | | | | | | |

(1) This GPIO is only an input (and not an output).

(2) The usage of this GPIO is strongly restricted. For more information, see the General-Purpose Interface chapter of the *AM/DM37x Multimedia Device Technical Reference Manual* (literature number SPRUGN4).

(3) UART4 is only available on CBP and CBC packages.

## 2.5 Signal Description

Many signals are available on multiple pins according to the software configuration of the pin multiplexing options.

1. **SIGNAL NAME:** The signal name

2. **DESCRIPTION:** Description of the signal

3. **TYPE:** Type = Ball type for this specific function:
   - I = Input
   - O = Output
   - Z = High-impedance
   - D = Open Drain
   - DS = Differential
   - A = Analog

4. **BALL BOTTOM:** Associated ball(s) bottom

5. **BALL TOP:** Associated ball(s) top

6. **SUBSYSTEM PIN MULTIPLEXING:** Contains a list of the pin multiplexing options at the module/subsystem level. The pin function is selected at the module/system level.

   **Note**: The Subsystem Multiplexing Signals are not described in the following tables. For more information, see the System Control Module / System Control Module Functional Description / Pad Functional Multiplexing and Configuration section of the *AM/DM37x Multimedia Device Technical Reference Manual* (literature number SPRUGN4).

### 2.5.1 External Memory Interfaces

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**NOTE**

For more information, see Memory Subsystem / General-Purpose Memory Controller / GPMC Environment section of the *AM/DM37x Multimedia Device Technical Reference Manual* (literature number SPRUGN4).

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**Table 2-5. External Memory Interfaces – GPMC Signals Description[1]**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | BALL BOTTOM (CBP Pkg.) [4] | BALL TOP (CBP Pkg.) [5] | BALL BOTTOM (CBC Pkg.) [4] | BALL TOP (CBC Pkg.) [5] | BALL BOTTOM (CUS Pkg.) [4] | SUBSYSTEM PIN MULTIPLEXING [6] |
|---|---|---|---|---|---|---|---|---|
| gpmc_a1 | GPMC output address bit 1 / extended multiplexed address gpmc_a17 | O | N4 / K1 | AC15 / M2 | J2 / AA2 | NA / U2 | K4 / L2 | - / gpmc_d0 |
| gpmc_a2 | GPMC output address bit 2 / extended multiplexed address gpmc_a18 | O | M4 / L1 | AB15 / M1 | H1 / AA1 | NA / U1 | K3 / M1 | - / gpmc_d1 |
| gpmc_a3 | GPMC output address bit 3 / extended multiplexed address gpmc_a19 | O | L4 / L2 | AC16 / N2 | H2 / AC2 | NA / V2 | K2 / M2 | - / gpmc_d2 |
| gpmc_a4 | GPMC output address bit 4 / extended multiplexed address gpmc_a20 | O | K4 / P2 | AB16 / N1 | G2 / AC1 | NA / V1 | J4 / N2 | - / gpmc_d3 |
| gpmc_a5 | GPMC output address bit 5 / extended multiplexed address gpmc_a21 | O | T3 / T1 | AC17 / R2 | F1 / AE5 | NA / AA3 | J3 / M3 | - / gpmc_d4 |
| gpmc_a6 | GPMC output address bit 6 / extended multiplexed address gpmc_a22 | O | R3 / V1 | AB17 / R1 | F2 / AD6 | NA / AA4 | J2/ P1 | - / gpmc_d5 |
| gpmc_a7 | GPMC output address bit 7 / extended multiplexed address gpmc_a23 | O | N3 / V2 | AC18 / T2 | E1 / AD5 | NA / Y3 | J1/ P2 | - / gpmc_d6 |
| gpmc_a8 | GPMC output address bit 8 / extended multiplexed address gpmc_a24 | O | M3 / W2 | AB18 / T1 | E2 / AC5 | NA / Y4 | H1/ R1 | - / gpmc_d7 |

### Table 2-5. External Memory Interfaces − GPMC Signals Description[1] (continued)

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | BALL BOTTOM (CBP Pkg.) [4] | BALL TOP (CBP Pkg.) [5] | BALL BOTTOM (CBC Pkg.) [4] | BALL TOP (CBC Pkg.) [5] | BALL BOTTOM (CUS Pkg.) [4] | SUBSYSTEM PIN MULTIPLEXING [6] |
|---|---|---|---|---|---|---|---|---|
| gpmc_a9 | GPMC output address bit 9 / extended multiplexed address gpmc_a25 | O | L3 / H2 | AC19 / AB3 | D1 / V1 | NA / R1 | H2/ R2 | - / gpmc_d8 |
| gpmc_a10 | GPMC output address bit 10 / extended multiplexed address gpmc_a26 | O | K3 / K2 | AB19 / AC3 | D2 / Y1 | T1 | G2/ T2 | - / gpmc_d9 |
| gpmc_a11 | GPMC output address bit 11 / extended multiplexed address gpmc_a27 | O | NC / P1 | AC20 / AB4 | A4 / T1 | - / N1 | NA | - / gpmc_d10 |
| gpmc_a12 | General-purpose memory address bit 12 | O | R1 | AC4 | U2 | P2 | R3 | gpmc_d11 |
| gpmc_a13 | General-purpose memory address bit 13 | O | R2 | AB6 | U1 | P1 | T3 | gpmc_d12 |
| gpmc_a14 | General-purpose memory address bit 14 | O | T2 | AC6 | P1 | M1 | U2 | gpmc_d13 |
| gpmc_a15 | General-purpose memory address bit 15 | O | W1 | AB7 | L2 | J2 | V1 | gpmc_d14 |
| gpmc_a16 | General-purpose memory address bit 16 | O | Y1 | AC7 | M2 | K2 | V2 | gpmc_d15 |
| gpmc_a17 | General-purpose memory address bit 17 | O | N4 | AC15 | J2 | NA | K4 | gpmc_a1 |
| gpmc_a18 | General-purpose memory address bit 18 | O | M4 | AB15 | H1 | NA | K3 | gpmc_a2 |
| gpmc_a19 | General-purpose memory address bit 19 | O | L4 | AC16 | H2 | NA | K2 | gpmc_a3 |
| gpmc_a20 | General-purpose memory address bit 20 | O | K4 | AB16 | G2 | NA | J4 | gpmc_a4 |
| gpmc_a21 | General-purpose memory address bit 21 | O | T3 | AC17 | F1 | NA | J3 | gpmc_a5 |
| gpmc_a22 | General-purpose memory address bit 22 | O | R3 | AB17 | F2 | NA | J2 | gpmc_a6 |
| gpmc_a23 | General-purpose memory address bit 23 | O | N3 | AC18 | E1 | NA | J1 | gpmc_a7 |
| gpmc_a24 | General-purpose memory address bit 24 | O | M3 | AB18 | E2 | NA | H1 | gpmc_a8 |
| gpmc_a25 | General-purpose memory address bit 25 | O | L3 | AC19 | D1 | NA | H2 | gpmc_a9 |
| gpmc_a26 | General-purpose memory address bit 26 | O | K3 | AB19 | D2 | NA | G2 | gpmc_a10 |
| gpmc_d0 | GPMC data bit 0 / multiplexed address gpmc_a1 | IO | K1 | M2 | AA2 | U2 | L2 | gpmc_d0 |
| gpmc_d1 | GPMC data bit 1 / multiplexed address gpmc_a2 | IO | L1 | M1 | AA1 | U1 | M1 | gpmc_d1 |
| gpmc_d2 | GPMC data bit 2 / multiplexed address gpmc_a3 | IO | L2 | N2 | AC2 | V2 | M2 | gpmc_d2 |
| gpmc_d3 | GPMC data bit 3 / multiplexed address gpmc_a4 | IO | P2 | N1 | AC1 | V1 | N2 | gpmc_d3 |
| gpmc_d4 | GPMC data bit 4 / multiplexed address gpmc_a5 | IO | T1 | R2 | AE5 | AA3 | M3 | gpmc_d4 |
| gpmc_d5 | GPMC data bit 5 / multiplexed address gpmc_a6 | IO | V1 | R1 | AD6 | AA4 | P1 | gpmc_d5 |
| gpmc_d6 | GPMC data bit 6 / multiplexed address gpmc_a7 | IO | V2 | T2 | AD5 | Y3 | P2 | gpmc_d6 |
| gpmc_d7 | GPMC data bit 7 / multiplexed address gpmc_a8 | IO | W2 | T1 | AC5 | Y4 | R1 | gpmc_d7 |
| gpmc_d8 | GPMC data bit 8 / multiplexed address gpmc_a9 | IO | H2 | AB3 | V1 | R1 | R2 | gpmc_d8 |
| gpmc_d9 | GPMC data bit 9 / multiplexed address gpmc_a10 | IO | K2 | AC3 | Y1 | T1 | T2 | gpmc_d9 |

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## Table 2-5. External Memory Interfaces − GPMC Signals Description[1] (continued)

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | BALL BOTTOM (CBP Pkg.) [4] | BALL TOP (CBP Pkg.) [5] | BALL BOTTOM (CBC Pkg.) [4] | BALL TOP (CBC Pkg.) [5] | BALL BOTTOM (CUS Pkg.) [4] | SUBSYSTEM PIN MULTIPLEXING [6] |
|---|---|---|---|---|---|---|---|---|
| gpmc_d10 | GPMC data bit 10 / multiplexed address gpmc_a11 | IO | P1 | AB4 | T1 | N1 | U1 | gpmc_d10 |
| gpmc_d11 | GPMC data bit 11 / multiplexed address gpmc_a12 | IO | R1 | AC4 | U2 | P2 | R3 | gpmc_d11 |
| gpmc_d12 | GPMC data bit 12 / multiplexed address gpmc_a13 | IO | R2 | AB6 | U1 | P1 | T3 | gpmc_d12 |
| gpmc_d13 | GPMC data bit 13 / multiplexed address gpmc_a14 | IO | T2 | AC6 | P1 | M1 | U2 | gpmc_d13 |
| gpmc_d14 | GPMC data bit 14 / multiplexed address gpmc_a15 | IO | W1 | AB7 | L2 | J2 | V1 | gpmc_d14 |
| gpmc_d15 | GPMC data bit 15 / multiplexed address gpmc_a16 | IO | Y1 | AC7 | M2 | K2 | V2 | gpmc_d15 |
| gpmc_ncs0 | GPMC Chip Select bit 0 | O | G4 | Y2 | AD8 | AA8 | E2 | NA |
| gpmc_ncs1 | GPMC Chip Select bit 1 | O | H3 | Y1 | AD1 | W1 | NA | NA |
| gpmc_ncs2 | GPMC Chip Select bit 2 | O | V8 | NA | A3 | NA | NA | NA |
| gpmc_ncs3 | GPMC Chip Select bit 3 | O | U8 | NA | B6 | NA | D2 | NA |
| gpmc_ncs4 | GPMC Chip Select bit 4 | O | T8 | NA | B4 | NA | F4 | NA |
| gpmc_ncs5 | GPMC Chip Select bit 5 | O | R8 | NA | C4 | NA | G5 | NA |
| gpmc_ncs6 | GPMC Chip Select bit 6 | O | P8 | NA | B5 | NA | F3 | NA |
| gpmc_ncs7 | GPMC Chip Select bit 7 | O | N8 | NA | C5 | NA | G4 | NA |
| gpmc_io_dir | GPMC IO direction control for use with external transceivers | O | N8 | NA | C5 | NA | G4 | NA |
| gpmc_clk | GPMC clock | O | T4 | W2 | N1 | L1 | W2 | NA |
| gpmc_nadv_ale | Address Valid or Address Latch Enable | O | F3 | W1 | AD10 | AA9 | F1 | NA |
| gpmc_noe | Output Enable | O | G2 | V2 | N2 | L2 | F2 | NA |
| gpmc_nwe | Write Enable | O | F4 | V1 | M1 | K1 | G3 | NA |
| gpmc_nbe0_cle | Lower Byte Enable. Also used for Command Latch Enable | O | G3 | AC12 | K2 | NA | K5 | NA |
| gpmc_nbe1 | Upper Byte Enable | O | U3 | NA | J1 | NA | L1 | NA |
| gpmc_nwp | Flash Write Protect | O | H1 | AB10 | AC6 | Y5 | E1 | NA |
| gpmc_wait0 | External indication of wait | I | M8 | AB12 | AC11 | Y10 | C1 | NA |
| gpmc_wait1 | External indication of wait | I | L8 | AC10 | AC8 | Y8 | NA | NA |
| gpmc_wait2 | External indication of wait | I | K8 | NA | B3 | NA | NA | NA |
| gpmc_wait3 | External indication of wait | I | J8 | NA | C6 | NA | C2 | NA |

(1)  NA in table stands for "Not Applicable".

### NOTE

For more information, see Memory Subsystem / SDRAM Controller (SDRC) Subsystem / SDRC Subsystem Environment section of the *AM/DM37x Multimedia Device Technical Reference Manual* (literature number SPRUGN4).

## Table 2-6. External Memory Interfaces – SDRC Signals Description[1]

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | BALL BOTTOM (CBP Pkg.) [4](2) | BALL TOP (CBP Pkg.) [5] | BALL BOTTOM (CBC Pkg.) [4](2) | BALL TOP (CBC Pkg.) [5] | BALL BOTTOM (CUS Pkg.) [4] |
|---|---|---|---|---|---|---|---|
| sdrc_d0 | SDRAM data bit 0 | IO | NA | J2 | NA | D1 | D7 |
| sdrc_d1 | SDRAM data bit 1 | IO | NA | J1 | NA | G1 | C5 |
| sdrc_d2 | SDRAM data bit 2 | IO | NA | G2 | NA | G2 | C6 |
| sdrc_d3 | SDRAM data bit 3 | IO | NA | G1 | NA | E1 | B5 |
| sdrc_d4 | SDRAM data bit 4 | IO | NA | F2 | NA | D2 | D9 |
| sdrc_d5 | SDRAM data bit 5 | IO | NA | F1 | NA | E2 | D10 |
| sdrc_d6 | SDRAM data bit 6 | IO | NA | D2 | NA | B3 | C7 |
| sdrc_d7 | SDRAM data bit 7 | IO | NA | D1 | NA | B4 | B7 |
| sdrc_d8 | SDRAM data bit 8 | IO | NA | B13 | NA | A10 | B11 |
| sdrc_d9 | SDRAM data bit 9 | IO | NA | A13 | NA | B11 | C12 |
| sdrc_d10 | SDRAM data bit 10 | IO | NA | B14 | NA | A11 | B12 |
| sdrc_d11 | SDRAM data bit 11 | IO | NA | A14 | NA | B12 | D13 |
| sdrc_d12 | SDRAM data bit 12 | IO | NA | B16 | NA | A16 | C13 |
| sdrc_d13 | SDRAM data bit 13 | IO | NA | A16 | NA | A17 | B14 |
| sdrc_d14 | SDRAM data bit 14 | IO | NA | B19 | NA | B17 | A14 |
| sdrc_d15 | SDRAM data bit 15 | IO | NA | A19 | NA | B18 | B15 |
| sdrc_d16 | SDRAM data bit 16 | IO | NA | B3 | NA | B7 | C9 |
| sdrc_d17 | SDRAM data bit 17 | IO | NA | A3 | NA | A5 | E12 |
| sdrc_d18 | SDRAM data bit 18 | IO | NA | B5 | NA | B6 | B8 |
| sdrc_d19 | SDRAM data bit 19 | IO | NA | A5 | NA | A6 | B9 |
| sdrc_d20 | SDRAM data bit 20 | IO | NA | B8 | NA | A8 | C10 |
| sdrc_d21 | SDRAM data bit 21 | IO | NA | A8 | NA | B9 | B10 |
| sdrc_d22 | SDRAM data bit 22 | IO | NA | B9 | NA | A9 | D12 |
| sdrc_d23 | SDRAM data bit 23 | IO | NA | A9 | NA | B10 | E13 |
| sdrc_d24 | SDRAM data bit 24 | IO | NA | B21 | NA | C21 | E15 |
| sdrc_d25 | SDRAM data bit 25 | IO | NA | A21 | NA | D20 | D15 |
| sdrc_d26 | SDRAM data bit 26 | IO | NA | D22 | NA | B19 | C15 |
| sdrc_d27 | SDRAM data bit 27 | IO | NA | D23 | NA | C20 | B16 |
| sdrc_d28 | SDRAM data bit 28 | IO | NA | E22 | NA | D21 | C16 |
| sdrc_d29 | SDRAM data bit 29 | IO | NA | E23 | NA | E20 | D16 |
| sdrc_d30 | SDRAM data bit 30 | IO | NA | G22 | NA | E21 | B17 |
| sdrc_d31 | SDRAM data bit 31 | IO | NA | G23 | NA | G21 | B18 |
| sdrc_ba0 | SDRAM bank select 0 | O | NA | AB21 | NA | AA18 | C18 |
| sdrc_ba1 | SDRAM bank select 1 | O | NA | AC21 | NA | V20 | D18 |
| sdrc_a0 | SDRAM address bit 0 | O | NA | N22 | NA | G20 | A4 |
| sdrc_a1 | SDRAM address bit 1 | O | NA | N23 | NA | K20 | B4 |
| sdrc_a2 | SDRAM address bit 2 | O | NA | P22 | NA | J20 | D6 |
| sdrc_a3 | SDRAM address bit 3 | O | NA | P23 | NA | J21 | B3 |
| sdrc_a4 | SDRAM address bit 4 | O | NA | R22 | NA | U21 | B2 |
| sdrc_a5 | SDRAM address bit 5 | O | NA | R23 | NA | R20 | C3 |
| sdrc_a6 | SDRAM address bit 6 | O | NA | T22 | NA | M21 | E3 |
| sdrc_a7 | SDRAM address bit 7 | O | NA | T23 | NA | M20 | F6 |
| sdrc_a8 | SDRAM address bit 8 | O | NA | U22 | NA | N20 | E10 |
| sdrc_a9 | SDRAM address bit 9 | O | NA | U23 | NA | K21 | E9 |
| sdrc_a10 | SDRAM address bit 10 | O | NA | V22 | NA | Y16 | E7 |
| sdrc_a11 | SDRAM address bit 11 | O | NA | V23 | NA | N21 | G6 |
| sdrc_a12 | SDRAM address bit 12 | O | NA | W22 | NA | R21 | G7 |
| sdrc_a13 | SDRAM address bit 13 | O | NA | W23 | NA | AA15 | F7 |
| sdrc_a14 | SDRAM address bit 14 | O | NA | Y22 | NA | Y12 | F9 |

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**Table 2-6. External Memory Interfaces – SDRC Signals Description[1] (continued)**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | BALL BOTTOM (CBP Pkg.) [4][2] | BALL TOP (CBP Pkg.) [5] | BALL BOTTOM (CBC Pkg.) [4][2] | BALL TOP (CBC Pkg.) [5] | BALL BOTTOM (CUS Pkg.) [4] |
|---|---|---|---|---|---|---|---|
| sdrc_ncs0 | Chip select 0 | O | NA | M22 | NA | T21 | A19 |
| sdrc_ncs1 | Chip select 1 | O | NA | M23 | NA | T20 | B19 |
| sdrc_clk | Clock | IO | NA | A11 | NA | A12 | A10 |
| sdrc_nclk | Clock Invert | O | NA | B11 | NA | B13 | A11 |
| sdrc_cke0 | Clock Enable 0 | O | NA | J22 | NA | Y15 | B20 |
| sdrc_cke1 | Clock Enable 1 | O | NA | J23 | NA | Y13 | C20 |
| sdrc_nras | SDRAM Row Access | O | NA | L23 | NA | V21 | D19 |
| sdrc_ncas | SDRAM column address strobe | O | NA | L22 | NA | U20 | C19 |
| sdrc_nwe | SDRAM write enable | O | NA | K23 | NA | Y18 | A20 |
| sdrc_dm 0 | Data Mask 0 | O | NA | C1 | NA | H1 | B6 |
| sdrc_ dm1 | Data Mask 1 | O | NA | A17 | NA | A14 | B13 |
| sdrc_ dm2 | Data Mask 2 | O | NA | A6 | NA | A4 | A7 |
| sdrc_dm 3 | Data Mask 3 | O | NA | A20 | NA | A18 | A16 |
| sdrc_dqs0 | Data Strobe 0 | IO | NA | B17 | NA | C2 | A5 |
| sdrc_dqs1 | Data Strobe 1 | IO | NA | NA | NA | B15 | A13 |
| sdrc_dqs2 | Data Strobe 2 | IO | NA | NA | NA | B8 | A8 |
| sdrc_dqs3 | Data Strobe 3 | IO | NA | B20 | NA | A19 | A17 |

(1)  NA in this table stands for "Not Applicable".

(2)  For a list of pins not supported on a particular package, see Table 2-4.

## 2.5.2 Video Interfaces

### Table 2-7. Video Interfaces – CAM Signals Description

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | BALL BOTTOM (CBP Pkg.) [4] | BALL BOTTOM (CBC Pkg.) [4] | BALL BOTTOM (CUS Pkg.) [4] |
|---|---|---|---|---|---|
| cam_hs | Camera Horizontal Synchronization | IO | A24 | C23 | A22 |
| cam_vs | Camera Vertical Synchronization | IO | A23 | D23 | E18 |
| cam_xclka | Camera Clock Output a | O | C25 | C25 | B22 |
| cam_xclkb | Camera Clock Output b | O | B26 | E25 | C22 |
| cam_d0 | Camera digital image data bit 0 | I | AG17 | AE16 | AB18 |
| cam_d1 | Camera digital image data bit 1 | I | AH17 | AE15 | AC18 |
| cam_d2 | Camera digital image data bit 2 | I | B24 | A24 | G19 |
| cam_d3 | Camera digital image data bit 3 | I | C24 | B24 | F19 |
| cam_d4 | Camera digital image data bit 4 | I | D24 | D24 | G20 |
| cam_d5 | Camera digital image data bit 5 | I | A25 | C24 | B21 |
| cam_d6 | Camera digital image data bit 6 | I | K28 | P25 | L24 |
| cam_d7 | Camera digital image data bit 7 | I | L28 | P26 | K24 |
| cam_d8 | Camera digital image data bit 8 | I | K27 | N25 | J23 |
| cam_d9 | Camera digital image data bit 9 | I | L27 | N26 | K23 |
| cam_d10 | Camera digital image data bit 10 | I | B25 | D25 | F21 |
| cam_d11 | Camera digital image data bit 11 | I | C26 | E26 | G21 |
| cam_fld | Camera field identification | IO | C23 | B23 | H24 |
| cam_pclk | Camera pixel clock | I | C27 | C26 | J19 |
| cam_wen | Camera Write Enable | I | B23 | A23 | F18 |
| cam_strobe | Flash strobe control signal | O | D25 | D26 | J20 |
| cam_global_reset | Global reset is used strobe synchronization | IO | C23 / AH3 / AA21 | B23/M3/V17 | H24/ AA2/ AB20 |
| cam_shutter | Mechanical shutter control signal | O | B23 / AF3 / T21 | A23 / T19/ L3 | F18/ Y2/ AA18 |

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### NOTE

For more information, see Display Subsystem / Display Subsystem Environment section of the *AM/DM37x Multimedia Device Technical Reference Manual* (literature number SPRUGN4).

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### Table 2-8. Video Interfaces – DSS Signals Description

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | BALL BOTTOM (CBP Pkg.) [4] | BALL BOTTOM (CBC Pkg.) [4] | BALL BOTTOM (CUS Pkg.) [4] |
|---|---|---|---|---|---|
| dss_pclk | LCD Pixel Clock | O | D28 | G25 | G22 |
| dss_hsync | LCD Horizontal Synchronization | O | D26 | K24 | E22 |
| dss_vsync | LCD Vertical Synchronization | O | D27 | M25 | F22 |
| dss_acbias | AC bias control (STN) or pixel data enable (TFT) output | O | E27 | F26 | J21 |
| dss_data0 | LCD Pixel Data bit 0 | O | AG22 / H26 | AE21 / M24 | AC19 / G24 |
| dss_data1 | LCD Pixel Data bit 1 | O | AH22 / H25 | AE22 / M26 | AB19 / H23 |
| dss_data2 | LCD Pixel Data bit 2 | O | AG23 / E28 | AE23 / F25 | AD20 / D23 |
| dss_data3 | LCD Pixel Data bit 3 | O | AH23 / J26 | AE24 / N24 | AC20 / K22 |
| dss_data4 | LCD Pixel Data bit 4 | O | AG24 / AC27 | AD23 / AC25 | AD21 / V21 |
| dss_data5 | LCD Pixel Data bit 5 | O | AH24 / AC28 | AD24 / AB25 | AC21 / W21 |
| dss_data6 | LCD Pixel Data bit 6 | O | E26 | G26 | D24 |
| dss_data7 | LCD Pixel Data bit 7 | O | F28 | H25 | E23 |
| dss_data8 | LCD Pixel Data bit 8 | O | F27 | H26 | E24 |
| dss_data9 | LCD Pixel Data bit 9 | O | G26 | J26 | F23 |
| dss_data10 | LCD Pixel Data bit 10 | O | AD28 | AC26 | AC22 |

## Table 2-8. Video Interfaces − DSS Signals Description (continued)

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | BALL BOTTOM (CBP Pkg.) [4] | BALL BOTTOM (CBC Pkg.) [4] | BALL BOTTOM (CUS Pkg.) [4] |
|---|---|---|---|---|---|
| dss_data11 | LCD Pixel Data bit 11 | O | AD27 | AD26 | AC23 |
| dss_data12 | LCD Pixel Data bit 12 | O | AB28 | AA25 | AB22 |
| dss_data13 | LCD Pixel Data bit 13 | O | AB27 | Y25 | Y22 |
| dss_data14 | LCD Pixel Data bit 14 | O | AA28 | AA26 | W22 |
| dss_data15 | LCD Pixel Data bit 15 | O | AA27 | AB26 | V22 |
| dss_data16 | LCD Pixel Data bit 16 | O | G25 | L25 | J22 |
| dss_data17 | LCD Pixel Data bit 17 | O | H27 | L26 | G23 |
| dss_data18 | LCD Pixel Data bit 18 | O | H26 / AH26 | M24 / F3 | G24 / AB12 |
| dss_data19 | LCD Pixel Data bit 19 | O | H25 / AG26 | M26 / D3 | H23 / AC16 |
| dss_data20 | LCD Pixel Data bit 20 | O | E28 / AF18 | F25 / E3 | D23 / AD18 |
| dss_data21 | LCD Pixel Data bit 21 | O | J26 / AF19 | N24 / E4 | K22 / AC17 |
| dss_data22 | LCD Pixel Data bit 22 | O | AC27 / AE21 | AC25 / G23 | V21 / AB16 |
| dss_data23 | LCD Pixel Data bit 23 | O | AC28 / AF21 | AB25 / D4 | W21 / AA15 |

## Table 2-9. Video Interfaces − RFBI Signals Description

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | BALL BOTTOM (CBP Pkg.) [4] | BALL BOTTOM (CBC Pkg.) [4] | BALL BOTTOM (CUS Pkg.) [4] | SUBSYSTEM PIN MULTIPLEXING [6] |
|---|---|---|---|---|---|---|
| rfbi_a0 | RFBI command/data control | O | E27 | F26 | J21 | dss_acbias |
| rfbi_cs0 | 1st LCD chip select | O | D26 | K24 | E22 | dss_hsync |
| rfbi_da0 | RFBI data bus 0 | IO | AG22 / H26 | AE21 / M24 | AC19 / G24 | dss_data0 |
| rfbi_da1 | RFBI data bus 1 | IO | AH22 / H25 | AE22 / M26 | AB19 / H23 | dss_data1 |
| rfbi_da2 | RFBI data bus 2 | IO | AG23 / E28 | AE23 / F25 | AD20 / D23 | dss_data2 |
| rfbi_da3 | RFBI data bus 3 | IO | AH23 / J26 | AE24 / N24 | AC20 / K22 | dss_data3 |
| rfbi_da4 | RFBI data bus 4 | IO | AG24 / AC27 | AD23 / AC25 | AD21 / V21 | dss_data4 |
| rfbi_da5 | RFBI data bus 5 | IO | AH24 / AC28 | AD24 / AB25 | AC21 / W21 | dss_data5 |
| rfbi_da6 | RFBI data bus 6 | IO | E26 | G26 | D24 | dss_data6 |
| rfbi_da7 | RFBI data bus 7 | IO | F28 | H25 | E23 | dss_data7 |
| rfbi_da8 | RFBI data bus 8 | IO | F27 | H26 | E24 | dss_data8 |
| rfbi_da9 | RFBI data bus 9 | IO | G26 | J26 | F23 | dss_data9 |
| rfbi_da10 | RFBI data bus 10 | IO | AD28 | AC26 | AC22 | dss_data10 |
| rfbi_da11 | RFBI data bus 11 | IO | AD27 | AD26 | AC23 | dss_data11 |
| rfbi_da12 | RFBI data bus 12 | IO | AB28 | AA25 | AB22 | dss_data12 |
| rfbi_da13 | RFBI data bus 13 | IO | AB27 | Y25 | Y22 | dss_data13 |
| rfbi_da14 | RFBI data bus 14 | IO | AA28 | AA26 | W22 | dss_data14 |
| rfbi_da15 | RFBI data bus 15 | IO | AA27 | AB26 | V22 | dss_data15 |
| rfbi_rd | Read enable for RFBI | O | D28 | G25 | G22 | dss_pclk |
| rfbi_wr | Write Enable for RFBI | O | D27 | M25 | F22 | dss_vsync |
| rfbi_te_vsync0 | tearing effect removal and Vsync input from 1st LCD | I | G25 | L25 | J22 | dss_data16 |
| rfbi_hsync0 | Hsync for 1st LCD | I | H27 | L26 | G23 | dss_data17 |
| rfbi_te_vsync1 | tearing effect removal and Vsync input from 2nd LCD | I | H26 / AH26 | M24 / F3 | G24 / AB12 | dss_data18 |
| rfbi_hsync1 | Hsync for 2nd LCD | I | H25 / AG26 | M26 / D3 | H23 / AC16 | dss_data19 |
| rfbi_cs1 | 2nd LCD chip select | O | E28 / AF18 | F25 / E3 | D23 / AD18 | dss_data20 |

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## Table 2-10. Video Interfaces − TV Signals Description

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | BALL BOTTOM (CBP Pkg.) [4] | BALL BOTTOM (CBC Pkg.) [4] | BALL BOTTOM (CUS Pkg.) [4] |
|---|---|---|---|---|---|
| cvideo1_out | TV analog output Composite: cvideo1_out | AO | Y28 | W26 | AB24 |
| cvideo2_out | TV analog output S-VIDEO: cvideo2_out | AO | W28 | V26 | AA23 |
| cvideo1_vfb | cvideo1_vfb: Feedback through external resistor to composite | AO | Y27 | W25 | AB23 |
| cvideo2_vfb | cvideo2_vfb: Feedback through external resistor to S-VIDEO | AO | W27 | U24 | Y23 |
| cvideo1_rset | cvideo1 input reference current resistor setting | AIO | W26 | V23 | Y24 |

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### 2.5.3 Serial Communication Interfaces

For more information, see HDQ/1-Wire / HDQ/1-Wire Environment section of the *AM/DM37x Multimedia Device Technical Reference Manual* (literature number SPRUGN4).

#### Table 2-11. Serial Communication Interfaces − HDQ/1-Wire Signals Description

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | BALL BOTTOM (CBP Pkg.) [4] | BALL BOTTOM (CBC Pkg.) [4] | BALL BOTTOM (CUS Pkg.) [4] |
|---|---|---|---|---|---|
| hdq_sio | Bidirectional HDQ 1-Wire control and data Interface. Output is open drain. | IOD | J25 | J23 | A24 |

For more information, see Multimaster High-Speed I2C Controller / HS I2C Environment section of the *AM/DM37x Multimedia Device Technical Reference Manual* (literature number SPRUGN4).

#### Table 2-12. Serial Communication Interfaces − I²C Signals Description

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | BALL BOTTOM (CBP Pkg.) [4] | BALL BOTTOM (CBC Pkg.) [4] | BALL BOTTOM (CUS Pkg.) [4] |
|---|---|---|---|---|---|
| **INTER-INTEGRATED CIRCUIT INTERFACE (I2C1)** | | | | | |
| i2c1_scl | I²C Master Serial clock. Output is open drain. | OD | K21 | J25 | K20 |
| i2c1_sda | I²C Serial Bidirectional Data. Output is open drain. | IOD | J21 | J24 | K21 |
| **INTER-INTEGRATED CIRCUIT INTERFACE (I2C3)** | | | | | |
| i2c3_scl | I²C Master Serial clock. Output is open drain. | OD | AF14 | AB4 | AC13 |
| i2c3_sda | I²C Serial Bidirectional Data. Output is open drain. | IOD | AG14 | AC4 | AC12 |
| i2c3_sccbe | Serial Camera Control Bus Enable | OD | J25 | J23 | A24 |
| **INTER-INTEGRATED CIRCUIT INTERFACE (I2C2)** | | | | | |
| i2c2_scl | I²C Master Serial clock. Output is open drain. | OD | AF15 | C2 | AC15 |
| i2c2_sda | I²C Serial Bidirectional Data. Output is open drain. | IOD | AE15 | C1 | AC14 |
| i2c2_sccbe | Serial Camera Control Bus Enable | OD | J25 | J23 | A24 |

For more information, see Power Reset and Clock Management / PRCM Introduction to Power Management / SmartReflex Voltage-Control Overview section of the *AM/DM37x Multimedia Device Technical Reference Manual* (literature number SPRUGN4).

#### Table 2-13. Serial Communication Interfaces − SmartReflex Signals Description[(1)]

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | BALL BOTTOM (CBP Pkg.) [4] | BALL BOTTOM (CBC Pkg.) [4] | BALL BOTTOM (CUS Pkg.) [4] |
|---|---|---|---|---|---|
| **INTER-INTEGRATED CIRCUIT INTERFACE (I2C4)** | | | | | |
| i2c4_scl | I²C Master Serial clock. Output is open drain. | OD | AD26 | AD15 | Y16 |
| i2c4_sda | I²C Serial Bidirectional Data. Output is open drain. | IOD | AE26 | W16 | Y15 |

(1) For more information on SmartReflex voltage control, see the PRCM chapter of the *AM/DM37x Multimedia Device Technical Reference Manual* (literature number SPRUGN4).

For more information, see Multi-Channel Buffered Serial Port / McBSP Environment section of the *AM/DM37x Multimedia Device Technical Reference Manual* (literature number SPRUGN4).

#### Table 2-14. Serial Communication Interfaces − McBSP LP Signals Description

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | BALL BOTTOM (CBP Pkg.) [4] | BALL BOTTOM (CBC Pkg.) [4] | BALL BOTTOM (CUS Pkg.) [4] |
|---|---|---|---|---|---|
| **MULTICHANNEL SERIAL (McBSP LP 1)** | | | | | |

**Table 2-14. Serial Communication Interfaces – McBSP LP Signals Description (continued)**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | BALL BOTTOM (CBP Pkg.) [4] | BALL BOTTOM (CBC Pkg.) [4] | BALL BOTTOM (CUS Pkg.) [4] |
|---|---|---|---|---|---|
| mcbsp1_dr | Received serial data | I | U21 | T20 | Y18 |
| mcbsp1_clkr | Receive Clock | IO | Y8 / Y21 | U19 / H3 | V7 / W19 |
| mcbsp1_fsr | Receive frame synchronization | IO | AA21 | V17 | AB20 |
| mcbsp1_dx | Transmitted serial data | O | V21 | U17 | W18 |
| mcbsp1_clkx | Transmit clock | IO | W21 | T17 | V18 |
| mcbsp1_fsx | Transmit frame synchronization | IO | K26 | P20 | AA19 |
| mcbsp_clks | External clock input (shared by McBSP1, 2, 3, 4, and 5) | I | T21 | T19 | AA18 |
| **MULTICHANNEL SERIAL (McBSP LP 2)** | | | | | |
| mcbsp2_dr | Received serial data | I | R21 | T18 | V19 |
| mcbsp2_dx | Transmitted serial data | O | M21 | R19 | R20 |
| mcbsp2_clkx | Combined serial clock | IO | N21 | R18 | T21 |
| mcbsp2_fsx | Combined frame synchronization | IO | P21 | U18 | V20 |
| **MULTICHANNEL SERIAL (McBSP LP 3)** | | | | | |
| mcbsp3_dr | Received serial data | I | AE6 / AB25 / U21 | T20 / AA24 / N3 | V5 / Y18 |
| mcbsp3_dx | Transmitted serial data | O | AF6 / AB26 / V21 | U17 / Y24 / P3 | V6 / W18 |
| mcbsp3_clkx | Combined serial clock | IO | AF5 / AA25 / W21 | T17 / AD22 / U3 | W4 / V18 |
| mcbsp3_fsx | Combined frame synchronization | IO | AE5 / AD25 / K26 | P20 / AD21 / W3 | V4 / AA19 |
| **MULTICHANNEL SERIAL (McBSP LP 4)** | | | | | |
| mcbsp4_dr | Received serial data | I | R8 / AD1 | C4 / U4 | G5 |
| mcbsp4_dx | Transmitted serial data | O | P8 / AD2 | B5 / R3 | F3 |
| mcbsp4_clkx | Combined serial clock | IO | T8 / AE1 | B4 / V3 | F4 |
| mcbsp4_fsx | Combined frame synchronization | IO | N8 / AC1 | C5 / T3 | G4 |
| **MULTICHANNEL SERIAL (McBSP LP 5)** | | | | | |
| mcbsp5_dr | Received serial data | I | AE11 | Y3 | AC5 |
| mcbsp5_dx | Transmitted serial data | O | AF13 | AE3 | AC8 |
| mcbsp5_clkx | Combined serial clock | IO | AF10 | AB2 | AC1 |
| mcbsp5_fsx | Combined frame synchronization | IO | AH9 | AB1 | AD2 |

For more information, see Multichannel SPI / McSPI Environment section of the *AM/DM37x Multimedia Device Technical Reference Manual* (literature number SPRUGN4).

**Table 2-15. Serial Communication Interfaces – McSPI Signals Description**[1]

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | BALL BOTTOM (CBP Pkg.) [4] | BALL BOTTOM (CBC Pkg.) [4] | BALL BOTTOM (CUS Pkg.) [4] |
|---|---|---|---|---|---|
| **MULTICHANNEL SERIAL PORT INTERFACE (McSPI1)** | | | | | |
| mcspi1_clk | SPI Clock | IO | AB3 | P9 | T5 |
| mcspi1_simo | Slave data in, master data out | IO | AB4 | P8 | R4 |
| mcspi1_somi | Slave data out, master data in | IO | AA4 | P7 | T4 |
| mcspi1_cs0 | SPI Enable 0, polarity configured by software | IO | AC2 | R7 | T6 |
| mcspi1_cs1 | SPI Enable 1, polarity configured by software | O | AC3 | R8 | NA |
| mcspi1_cs2 | SPI Enable 2, polarity configured by software | O | AB1 | R9 | NA |
| mcspi1_cs3 | SPI Enable 3, polarity configured by software | O | AB2 | T8 | R5 |
| **MULTICHANNEL SERIAL PORT INTERFACE (McSPI2)** | | | | | |
| mcspi2_clk | SPI Clock | IO | AA3 | W7 | N5 |
| mcspi2_simo | Slave data in, master data out | IO | Y2 | W8 | N4 |
| mcspi2_somi | Slave data out, master data in | IO | Y3 | U8 | N3 |
| mcspi2_cs0 | SPI Enable 0, polarity configured by software | IO | Y4 | V8 | M5 |

**Table 2-15. Serial Communication Interfaces – McSPI Signals Description(1) (continued)**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | BALL BOTTOM (CBP Pkg.) [4] | BALL BOTTOM (CBC Pkg.) [4] | BALL BOTTOM (CUS Pkg.) [4] |
|---|---|---|---|---|---|
| mcspi2_cs1 | SPI Enable 1, polarity configured by software | O | V3 | V9 | M4 |
| **MULTICHANNEL SERIAL PORT INTERFACE (McSPI3)** | | | | | |
| mcspi3_clk | SPI Clock | IO | H26 / AE2 / AE13 | W10 / M24 / AA3 | G24 / Y1 / AD8 |
| mcspi3_simo | Slave data in, master data out | IO | H25 / AG5 / AF11 | R10 / M26 / AC3 | H23 / AB5 / AD6 |
| mcspi3_somi | Slave data out, master data in | IO | E28 / AH5 / AG12 | F25 / T10 / AD4 | D23 / AB3 / AC6 |
| mcspi3_cs0 | SPI Enable 0, polarity configured by software | IO | J26 / AF4 / AH12 | U9 / N24 / AD3 | K22 / V3 / AC7 |
| mcspi3_cs1 | SPI Enable 1, polarity configured by software | O | AC27 / AG4 / AH14 | AC25 / U10 / AD2 | V21 / W3 / AD9 |
| **MULTICHANNEL SERIAL PORT INTERFACE (McSPI4)** | | | | | |
| mcspi4_clk | SPI Clock | IO | Y8 / Y21 | U19 / H3 | V7 / W19 |
| mcspi4_simo | Slave data in, master data out | IO | V21 | U17 | W18 |
| mcspi4_somi | Slave data out, master data in | IO | U21 | T20 | Y18 |
| mcspi4_cs0 | SPI Enable 0, polarity configured by software | IO | K26 | P20 | AA19 |

(1) NA in this table stands for "Not applicable".

For more information, see UART/IrDA/CIR / UART/IrDA/CIR Environment section of the *AM/DM37x Multimedia Device Technical Reference Manual* (literature number SPRUGN4).

**Table 2-16. Serial Communication Interfaces – UARTs Signals Description**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | BALL BOTTOM (CBP Pkg.) [4] | BALL BOTTOM (CBC Pkg.) [4] | BALL BOTTOM (CUS Pkg.) [4] |
|---|---|---|---|---|---|
| **UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER (UART1)** | | | | | |
| uart1_cts | UART1 Clear To Send | I | AG22 / W8 / T21 | AE21 / T19 / W2 | AC19 / AC2 / AA18 |
| uart1_rts | UART1 Request To Send | O | AH22 / AA9 | AE22 / R2 | W6 / AB19 |
| uart1_rx | UART1 Receive data | I | F28 / Y8 / AE7 | H3 / H25 / AE4 | E23 / V7 / AC3 |
| uart1_tx | UART1 Transmit data | O | E26 / AA8 | L4 / G26 | D24 / W7 |
| **UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER (UART2)** | | | | | |
| uart2_cts | UART2 Clear To Send | I | AF6 / AB26 / U26 | Y24/ P3/ W20 | V6/ U23 |
| uart2_rts | UART2 Request To Send | O | AE6 / AB25 / U27 | AA24/ N3/ V18 | V5/ U24 |
| uart2_rx | UART2 Receive data | I | AE5 / AD25/ U28 | W3/ AD21/ Y20 | T23/ V4 |
| uart2_tx | UART2 Transmit data | O | AF5 / AA25/ T27 | U3/AD22/V20 | T24/ W4 |
| **UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER (UART3) / IrDA** | | | | | |
| uart3_cts_rctx | UART3 Clear To Send (input), Remote TX (output) | IO | H18 / U26 | W20 / F23 | A23 / U23 |
| uart3_rts_sd | UART3 Request To Send, IR enable | O | H19 / U27 | V18 / F24 | B23 / U24 |
| uart3_rx_irrx | UART3 Receive data, IR and Remote RX | I | AG24 / H20 / U28 / F27 | AD23 / Y20 / H24/ H26 | AD21 / B24 / T23 / E24 |
| uart3_tx_irtx | UART3 Transmit data, IR TX | O | AH24 / H21 / T27/ G26 | AD24 / V20 / J29 / G24 | AC21 / C23 / T24/ F23 |
| **UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER (UART4) / IrDA** | | | | | |
| uart4_rx | UART4 Receive data | I | J8 | C6 | NA |
| uart4_tx | UART4 Transmit data | O | K8 | B3 | NA |

For more information, see High-Speed USB Host Subsystem and High-Speed USB OTG Controller / High-Speed USB Host Subsystem / High-Speed USB Host Subsystem Environment section of the *AM/DM37x Multimedia Device Technical Reference Manual* (literature number SPRUGN4).

**Table 2-17. Serial Communication Interfaces – USB Signals Description** Section 4.3.6

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | BALL BOTTOM (CBP Pkg.) [4] | BALL BOTTOM (CBC Pkg.) [4] | BALL BOTTOM (CUS Pkg.) [4] |
|---|---|---|---|---|---|
| **HIGH-SPEED UNIVERSAL SERIAL BUS INTERFACE (HSUSB0)** | | | | | |

## Table 2-17. Serial Communication Interfaces – USB Signals Description[Section 4.3.6] (continued)

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | BALL BOTTOM (CBP Pkg.) [4] | BALL BOTTOM (CBC Pkg.) [4] | BALL BOTTOM (CUS Pkg.) [4] |
|---|---|---|---|---|---|
| hsusb0_clk | Dedicated for external transceiver 60-MHz clock input to PHY | I | T28 | W19 | R21 |
| hsusb0_stp | Dedicated for external transceiver Stop signal | O | T25 | U20 | R23 |
| hsusb0_dir | Dedicated for external transceiver Data direction control from PHY | I | R28 | V19 | P23 |
| hsusb0_nxt | Dedicated for external transceiver Next signal from PHY | I | T26 | W18 | R22 |
| hsusb0_data0 | Dedicated for external transceiver Bidirectional data bus | IO | T27 | V20 | T24 |
| hsusb0_data1 | Dedicated for external transceiver Bidirectional data bus | IO | U28 | Y20 | T23 |
| hsusb0_data2 | Dedicated for external transceiver Bidirectional data bus | IO | U27 | V18 | U24 |
| hsusb0_data3 | Dedicated for external transceiver Bidirectional data bus | IO | U26 | W20 | U23 |
| hsusb0_data4 | Dedicated for external transceiver Bidirectional data bus additional signals for 12-pin ULPI operation | IO | U25 | W17 | W24 |
| hsusb0_data5 | Dedicated for external transceiver Bidirectional data bus additional signals for 12-pin ULPI operation | IO | V28 | Y18 | V23 |
| hsusb0_data6 | Dedicated for external transceiver Bidirectional data bus additional signals for 12-pin ULPI operation | IO | V27 | Y19 | W23 |
| hsusb0_data7 | Dedicated for external transceiver Bidirectional data bus additional signals for 12-pin ULPI operation | IO | V26 | Y17 | T22 |
| **MM_FSUSB3** | | | | | |
| mm3_rxdm | Vminus receive data (not used in 3- or 4-pin configurations) | IO | AE3 | K3 | NA |
| mm3_rxdp | Vplus receive data (not used in 3- or 4-pin configurations) | IO | AH3 | M3 | NA |
| mm3_rxrcv | Differential receiver signal input (not used in 3-pin mode) | IO | AD1 | U4 | NA |
| mm3_txse0 | Single-ended zero. Used as VM in 4-pin VP_VM mode. | IO | AE1 | V3 | NA |
| mm3_txdat | USB data. Used as VP in 4-pin VP_VM mode. | IO | AD2 | R3 | NA |
| mm3_txen_n | Transmit enable | IO | AC1 | T3 | NA |
| **MM_FSUSB2** | | | | | |
| mm2_rxdm | Vminus receive data (not used in 3- or 4-pin configurations) | IO | AH7 | AF7 | AD11 |
| mm2_rxdp | Vplus receive data (not used in 3- or 4-pin configurations) | IO | AF7 | AF6 | AC9 |
| mm2_rxrcv | Differential receiver signal input (not used in 3-pin mode) | IO | AG8 | AF9 | AC11 |
| mm2_txse0 | Single-ended zero. Used as VM in 4-pin VP_VM mode. | IO | AH8 | AE9 | AD12 |
| mm2_txdat | USB data. Used as VP in 4-pin VP_VM mode. | IO | AB2 | T8 | R5 |
| mm2_txen_n | Transmit enable | IO | V3 | V9 | M4 |
| **MM_FSUSB1** | | | | | |
| mm1_rxdm | Vminus receive data (not used in 3- or 4-pin configurations) | IO | AG9 | V2 | AD5 |
| mm1_rxdp | Vplus receive data (not used in 3- or 4-pin configurations) | IO | AF10 | AB2 | AC1 |
| mm1_rxrcv | Differential receiver signal input (not used in 3-pin mode) | IO | AF11 | AC3 | AD6 |
| mm1_txse0 | Single-ended zero. Used as VM in 4-pin VP_VM mode. | IO | AG12 | AD4 | AC6 |
| mm1_txdat | USB data. Used as VP in 4-pin VP_VM mode. | IO | AH12 | AD3 | AC7 |
| mm1_txen_n | Transmit enable | IO | AH14 | AD2 | AD9 |
| **HSUSB2** | | | | | |
| hsusb2_clk | Dedicated for external transceiver 60-MHz clock input to PHY | O | AE7 | AE4 | AC3 |
| hsusb2_stp | Dedicated for external transceiver Stop signal | O | AF7 | AF6 | AC9 |
| hsusb2_dir | Dedicated for external transceiver Data direction control from PHY | I | AG7 | AE6 | AC10 |
| hsusb2_nxt | Dedicated for external transceiver Next signal from PHY | I | AH7 | AF7 | AD11 |
| hsusb2_data0 | Dedicated for external transceiver Bidirectional data bus | IO | AG8 | AF9 | AC11 |
| hsusb2_data1 | Dedicated for external transceiver Bidirectional data bus | IO | AH8 | AE9 | AD12 |
| hsusb2_data2 | Dedicated for external transceiver Bidirectional data bus | IO | AB2 | T8 | R5 |
| hsusb2_data3 | Dedicated for external transceiver Bidirectional data bus | IO | V3 | V9 | M4 |
| hsusb2_data4 | Dedicated for external transceiver Bidirectional data bus additional signals for 12-pin ULPI operation | IO | Y2 | W8 | N4 |
| hsusb2_data5 | Dedicated for external transceiver Bidirectional data bus additional signals for 12-pin ULPI operation | IO | Y3 | U8 | N3 |
| hsusb2_data6 | Dedicated for external transceiver Bidirectional data bus additional signals for 12-pin ULPI operation | IO | Y4 | V8 | M5 |

### Table 2-17. Serial Communication Interfaces – USB Signals Description[Section 4.3.6] (continued)

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | BALL BOTTOM (CBP Pkg.) [4] | BALL BOTTOM (CBC Pkg.) [4] | BALL BOTTOM (CUS Pkg.) [4] |
|---|---|---|---|---|---|
| hsusb2_data7 | Dedicated for external transceiver Bidirectional data bus additional signals for 12-pin ULPI operation | IO | AA3 | W7 | N5 |
| **HSUSB1** | | | | | |
| hsusb1_clk | Dedicated for external transceiver 60-MHz clock input to PHY | O | AE10 | AB3 | AD3 |
| hsusb1_stp | Dedicated for external transceiver Stop signal | O | AF10 | AB2 | AC1 |
| hsusb1_dir | Dedicated for external transceiver data direction control from PHY | I | AF9 | AA4 | AC4 |
| hsusb1_nxt | Dedicated for external transceiver Next signal from PHY | I | AG9 | V2 | AD5 |
| hsusb1_data0 | Dedicated for external transceiver Bidirectional data bus | IO | AF11 | AC3 | AD6 |
| hsusb1_data1 | Dedicated for external transceiver Bidirectional data bus | IO | AG12 | AD4 | AC6 |
| hsusb1_data2 | Dedicated for external transceiver Bidirectional data bus | IO | AH12 | AD3 | AC7 |
| hsusb1_data3 | Dedicated for external transceiver Bidirectional data bus | IO | AH14 | AD2 | AD9 |
| hsusb1_data4 | Dedicated for external transceiver Bidirectional data bus additional signals for 12-pin ULPI operation | IO | AE11 | Y3 | AC5 |
| hsusb1_data5 | Dedicated for external transceiver Bidirectional data bus additional signals for 12-pin ULPI operation | IO | AH9 | AB1 | AD2 |
| hsusb1_data6 | Dedicated for external transceiver Bidirectional data bus additional signals for 12-pin ULPI operation | IO | AF13 | AE3 | AC8 |
| hsusb1_data7 | Dedicated for external transceiver Bidirectional data bus additional signals for 12-pin ULPI operation | IO | AE13 | AA3 | AD8 |

- NA in this table stands for "Not applicable".
- This pin is not supported on the CUS package.

### 2.5.4 Removable Media Interfaces

For more information, see MMC/SDIO Card Interface / MMC/SDIO Environment section of the *AM/DM37x Multimedia Device Technical Reference Manual* (literature number SPRUGN4).

**Table 2-18. Removable Media Interfaces – MMC/SDIO Signals Description**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | BALL BOTTOM (CBP Pkg.) [4] | BALL BOTTOM (CBC Pkg.) [4] | BALL BOTTOM (CUS Pkg.) [4] |
|---|---|---|---|---|---|
| MULTIMEDIA MEMORY CARD (MMC1) / SECURE DIGITAL IO (SDIO1) | | | | | |
| mmc1_clk | MMC/SD Output Clock | O | N28 | N19 | M23 |
| mmc1_cmd | MMC/SD command signal | IO | M27 | L18 | L23 |
| mmc1_dat0 | MMC/SD Card Data bit 0 / SPI Serial Input | IO | N27 | M19 | M22 |
| mmc1_dat1 | MMC/SD Card Data bit 1 | IO | N26 | M18 | M21 |
| mmc1_dat2 | MMC/SD Card Data bit 2 | IO | N25 | K18 | M20 |
| mmc1_dat3 | MMC/SD Card Data bit 3 | IO | P28 | N20 | N23 |
| MULTIMEDIA MEMORY CARD (MMC2) / SECURE DIGITAL IO (SDIO2) | | | | | |
| mmc2_clk | MMC/SD Output Clock | O | AE2 | W10 | Y1 |
| mmc2_dir_dat0 | Direction control for DAT0 signal case an external transceiver used | O | AE4 | V10 | AB2 |
| mmc2_dir_dat1 | Direction control for DAT1 and DAT3 signals case an external transceiver used | O | AH3 | M3 | AA2 |
| mmc2_dir_dat2 | Direction control for DAT2 signal case an external transceiver used | O | AF19 | E4 | AC17 |
| mmc2_dir_dat3 | Direction control for DAT4, DAT5, DAT6, and DAT7 signals case an external transceiver used | O | AE21 | G3 | AB16 |
| mmc2_clkin | MMC/SD input Clock | I | AE3 | K3 | AA1 |
| mmc2_dat0 | MMC/SD Card Data bit 0 | IO | AH5 | T10 | AB3 |
| mmc2_dat1 | MMC/SD Card Data bit 1 | IO | AH4 | T9 | Y3 |
| mmc2_dat2 | MMC/SD Card Data bit 2 | IO | AG4 | U10 | W3 |
| mmc2_dat3 | MMC/SD Card Data bit 3 | IO | AF4 | U9 | V3 |
| mmc2_dat4 | MMC/SD Card Data bit 4 | IO | AE4 / AB3 | P9 / V10 | AB2 / T5 |
| mmc2_dat5 | MMC/SD Card Data bit 5 | IO | AH3 / AB4 | M3/P8 | AA2 / R4 |
| mmc2_dat6 | MMC/SD Card Data bit 6 | IO | AF3 / AA4 | L3/P7 | Y2 / T4 |
| mmc2_dat7 | MMC/SD Card Data bit 7 | IO | AE3 / AC2 | K3/R7 | AA1 / T6 |
| mmc2_dir_cmd | Direction control for CMD signal case an external transceiver is used | O | AF3 | L3 | Y2 |
| mmc2_cmd | MMC/SD command signal | IO | AG5 | R10 | AB5 |
| MULTIMEDIA MEMORY CARD (MMC3) / SECURE DIGITAL IO (SDIO3) | | | | | |
| mmc3_clk | MMC/SD Output Clock | O | AB1 / AF10 | R9 / AB2 | AC1 |
| mmc3_cmd | MMC/SD command signal | IO | AC3 / AE10 | R8 / AB3 | AD3 |
| mmc3_dat0 | MMC/SD Card Data bit 0 / SPI Serial Input | IO | AE4 / AE11 | V10 / Y3 | AB2 / AC5 |
| mmc3_dat1 | MMC/SD Card Data bit 1 | IO | AH3 / AH9 | M3/AB1 | AA2 / AD2 |
| mmc3_dat2 | MMC/SD Card Data bit 2 | IO | AF3 / AF13 | L3/AE3 | Y2 / AC8 |
| mmc3_dat3 | MMC/SD Card Data bit 3 | IO | AE3 / AE13 | K3/AA3 | AA1 / AD8 |
| mmc3_dat4 | MMC/SD Card Data bit 4 | IO | AF11 | AC3 | AD6 |
| mmc3_dat5 | MMC/SD Card Data bit 5 | IO | AG9 | V2 | AD5 |
| mmc3_dat6 | MMC/SD Card Data bit 6 | IO | AF9 | AA4 | AC4 |
| mmc3_dat7 | MMC/SD Card Data bit 7 | IO | AH14 | AD2 | AD9 |

### 2.5.5 Test Interfaces

**Table 2-19. Test Interfaces – ETK Signals Description**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | BALL BOTTOM (CBP Pkg.) [4] | BALL BOTTOM (CBC Pkg.) [4] | BALL BOTTOM (CUS Pkg.) [4] |
|---|---|---|---|---|---|
| etk_ctl | ETK trace ctl | O | AE10 | AB3 | AD3 |
| etk_clk | ETK trace clock | O | AF10 | AB2 | AC1 |
| etk_d0 | ETK data 0 | O | AF11 | AC3 | AD6 |
| etk_d1 | ETK data 1 | O | AG12 | AD4 | AC6 |
| etk_d2 | ETK data 2 | O | AH12 | AD3 | AC7 |
| etk_d3 | ETK data 3 | O | AE13 | AA3 | AD8 |
| etk_d4 | ETK data 4 | O | AE11 | Y3 | AC5 |
| etk_d5 | ETK data 5 | O | AH9 | AB1 | AD2 |
| etk_d6 | ETK data 6 | O | AF13 | AE3 | AC8 |
| etk_d7 | ETK data 7 | O | AH14 | AD2 | AD9 |
| etk_d8 | ETK data 8 | O | AF9 | AA4 | AC4 |
| etk_d9 | ETK data 9 | O | AG9 | V2 | AD5 |
| etk_d10 | ETK data 10 | O | AE7 | AE4 | AC3 |
| etk_d11 | ETK data 11 | O | AF7 | AF6 | AC9 |
| etk_d12 | ETK data 12 | O | AG7 | AE6 | AC10 |
| etk_d13 | ETK data 13 | O | AH7 | AF7 | AD11 |
| etk_d14 | ETK data 14 | O | AG8 | AF9 | AC11 |
| etk_d15 | ETK data 15 | O | AH8 | AE9 | AD12 |

**Table 2-20. Test Interfaces – JTAG Signals Description**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | BALL BOTTOM (CBP Pkg.) [4] | BALL BOTTOM (CBC Pkg.) [4] | BALL BOTTOM (CUS Pkg.) [4] |
|---|---|---|---|---|---|
| jtag_ntrst | Test Reset | I | AA17 | U15 | AB7 |
| jtag_tck | Test Clock | I | AA13 | V14 | AB6 |
| jtag_rtck | ARM Clock Emulation | O | AA12 | W13 | AA7 |
| jtag_tms_tmsc | Test Mode Select | IO | AA18 | V15 | AA9 |
| jtag_tdi | Test Data Input | I | AA20 | U16 | AB10 |
| jtag_tdo | Test Data Output | O | AA19 | Y13 | AB9 |
| jtag_emu0 | Test emulation 0 | IO | AA11 | Y15 | AC24 |
| jtag_emu1 | Test emulation 1 | IO | AA10 | Y14 | AD24 |

**Table 2-21. Test Interfaces − SDTI Signals Description**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | BALL BOTTOM (CBP Pkg.) [4] | BALL BOTTOM (CBC Pkg.) [4] | BALL BOTTOM (CUS Pkg.) [4] | SUBSYSTEM SIGNAL MULTIPLEXING [6] |
|---|---|---|---|---|---|---|
| sdti_clk | Serial clock dual edge | O | AF7 / AA11 / AG8 | AF6 / Y15 / AF9 | AC9 / AC24 / AC11 | etk_d11 / jtag_emu0 / etk_d14 |
| sdti_txd0 | Serial data out (System Trace messages) | O | AG7 / AA10 / AA11 | AE6 / Y14 / Y15 | AC10 / AD24 / AC24 | etk_d12 / jtag_emu1 / jtag_emu0 |
| sdti_txd1 | Serial data out (System Trace messages) | O | AH7 / AA10 | AF7 / Y14 | AD11 / AD24 | etk_d13 / jtag_emu1 |
| sdti_txd2 | Serial data out (System Trace messages) | O | AG8 | AF9 | AC11 | etk_d14 |
| sdti_txd3 | Serial data out (System Trace messages) | O | AH8 | AE9 | AD12 | etk_d15 |

**Table 2-22. Test Interfaces − HWDBG Signals Description**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | BALL BOTTOM (CBP Pkg.) [4] | BALL BOTTOM (CBC Pkg.) [4] | BALL BOTTOM (CUS Pkg.) [4] |
|---|---|---|---|---|---|
| hw_dbg0 | Debug signal 0 | O | A24 / AF10 | C23/AB2 | AC1/A22 |
| hw_dbg1 | Debug signal 1 | O | A23 / AE10 | D23/AB3 | AD3/E18 |
| hw_dbg2 | Debug signal 2 | O | C27/ AF11 | C26/AC3 | AD6/J19 |
| hw_dbg3 | Debug signal 3 | O | C23 / AG12 | B23/AD4 | AC6/H24 |
| hw_dbg4 | Debug signal 4 | O | B24 / AH12 | A24/AD3 | AC7/G19 |
| hw_dbg5 | Debug signal 5 | O | C24 / AE13 | B24/AA3 | AD8/F19 |
| hw_dbg6 | Debug signal 6 | O | D24 / AE11 | D24/Y3 | AC5/G20 |
| hw_dbg7 | Debug signal 7 | O | A25 / AH9 | C24/AB1 | AD2/B21 |
| hw_dbg8 | Debug signal 8 | O | B25 / AF13 | D25/AE3 | AC8/F21 |
| hw_dbg9 | Debug signal 9 | O | C26 / AH14 | E26/AD2 | AD9/G21 |
| hw_dbg10 | Debug signal 10 | O | B23 / AF9 | A23/AA4 | AC4/F18 |
| hw_dbg11 | Debug signal 11 | O | D25 / AG9 | D26/V2 | AD5/J20 |
| hw_dbg12 | Debug signal 12 | O | D28 / AE7 | G25/AE4 | AC3/G22 |
| hw_dbg13 | Debug signal 13 | O | D26 / AF7 | K24/AF6 | AC9/E22 |
| hw_dbg14 | Debug signal 14 | O | E26 / AG7 | G26/AE6 | AC10/D24 |
| hw_dbg15 | Debug signal 15 | O | F28 / AH7 | H25/AF7 | AD11/E23 |
| hw_dbg16 | Debug signal 16 | O | F27 / AG8 | H26/AF9 | AC11/E24 |
| hw_dbg17 | Debug signal 17 | O | G26 / AH8 | J26/AE9 | AD12/F23 |

### 2.5.6 Miscellaneous

For more information, see Timers / GP Timers / GP Timers Environment section of the *AM/DM37x Multimedia Device Technical Reference Manual* (literature number SPRUGN4).

**Table 2-23. Miscellaneous − GP Timer Signals Description**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | BALL BOTTOM (CBP Pkg.) [4] | BALL BOTTOM (CBC Pkg.) [4] | BALL BOTTOM (CUS Pkg.) [4] |
|---|---|---|---|---|---|
| gpt_8_pwm_evt | PWM or event for GP timer 8 | IO | N8 / AD25 / V3 | C5 / AD21/ V9 | G4/ M4 |
| gpt_9_pwm_evt | PWM or event for GP timer 9 | IO | T8 / AB26 / Y2 | B4 / W8 / Y24 | F4 / N4 |
| gpt_10_pwm_evt | PWM or event for GP timer 10 | IO | R8 / AB25 / Y3 | C4 / U8 / AA24 | G5 / N3 |
| gpt_11_pwm_evt | PWM or event for GP timer 11 | IO | P8 / AA25 / Y4 | B5 / V8 / AD22 | F3 / M5 |

### 2.5.7 General-Purpose IOs

For more information, see General-Purpose Interface / General-Purpose Interface Environment section of the *AM/DM37x Multimedia Device Technical Reference Manual* (literature number SPRUGN4).

**Table 2-24. General-Purpose IOs Signals Description**[(1)]

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | BALL BOTTOM (CBP Pkg.) [4] | BALL BOTTOM (CBC Pkg.) [4] | BALL BOTTOM (CUS Pkg.) [4] |
|---|---|---|---|---|---|
| gpio_0 | General-purpose IO 0 | IO | AF26 | V16 | W16 |
| gpio_1 | General-purpose IO 1 | IO | AF25 | W15 | Y13 |
| gpio_2 | General-purpose IO 2 | IO | AH26 | F3 | AB12 |
| gpio_3 | General-purpose IO 3 | IO | AG26 | D3 | AC16 |
| gpio_4 | General-purpose IO 4 | IO | AE14 | C3 | AD17 |
| gpio_5 | General-purpose IO 5 | IO | AF18 | E3 | AD18 |
| gpio_6 | General-purpose IO 6 | IO | AF19 | E4 | AC17 |
| gpio_7 | General-purpose IO 7 | IO | AE21 | G3 | AB16 |
| gpio_8 | General-purpose IO 8 | IO | AF21 | D4 | AA15 |
| gpio_9 | General-purpose IO 9 | IO | AF22 | V12 | AD23 |
| gpio_10 | General-purpose IO 10 | IO | AG25 | AE14 | Y7 |
| gpio_11 | General-purpose IO 11 | IO | AA11 | Y15 | AC24 |
| gpio_12 | General-purpose IO 12 | IO | AF10 | AB2 | AC1 |
| gpio_13 | General-purpose IO 13 | IO | AE10 | AB3 | AD3 |
| gpio_14 | General-purpose IO 14 | IO | AF11 | AC3 | AD6 |
| gpio_15 | General-purpose IO 15 | IO | AG12 | AD4 | AC6 |
| gpio_16 | General-purpose IO 16 | IO | AH12 | AD3 | AC7 |
| gpio_17 | General-purpose IO 17 | IO | AE13 | AA3 | AD8 |
| gpio_18 | General-purpose IO 18 | IO | AE11 | Y3 | AC5 |
| gpio_19 | General-purpose IO 19 | IO | AH9 | AB1 | AD2 |
| gpio_20 | General-purpose IO 20 | IO | AF13 | AE3 | AC8 |
| gpio_21 | General-purpose IO 21 | IO | AH14 | AD2 | AD9 |
| gpio_22 | General-purpose IO 22 | IO | AF9 | AA4 | AC4 |
| gpio_23 | General-purpose IO 23 | IO | AG9 | V2 | AD5 |
| gpio_24 | General-purpose IO 24 | IO | AE7 | AE4 | AC3 |
| gpio_25 | General-purpose IO 25 | IO | AF7 | AF6 | AC9 |
| gpio_26 | General-purpose IO 26 | IO | AG7 | AE6 | AC10 |
| gpio_27 | General-purpose IO 27 | IO | AH7 | AF7 | AD11 |
| gpio_28 | General-purpose IO 28 | IO | AG8 | AF9 | AC11 |
| gpio_29 | General-purpose IO 29 | IO | AH8 | AE9 | AD12 |
| gpio_30 | General-purpose IO 30 | IO | AF24 | AD7 | Y10 |
| gpio_31 | General-purpose IO 31 | IO | AA10 | Y14 | AD24 |
| gpio_34 | General-purpose IO 34 | IO | N4 | J2 | K4 |
| gpio_35 | General-purpose IO 35 | IO | M4 | H1 | K3 |
| gpio_36 | General-purpose IO 36 | IO | L4 | H2 | K2 |
| gpio_37 | General-purpose IO 37 | IO | K4 | G2 | J4 |
| gpio_38 | General-purpose IO 38 | IO | T3 | F1 | J3 |
| gpio_39 | General-purpose IO 39 | IO | R3 | F2 | J2 |
| gpio_40 | General-purpose IO 40 | IO | N3 | E1 | J1 |
| gpio_41 | General-purpose IO 41 | IO | M3 | E2 | H1 |
| gpio_42 | General-purpose IO 42 | IO | L3 | D1 | H2 |
| gpio_43 | General-purpose IO 43 | IO | K3 | D2 | G2 |
| gpio_44 | General-purpose IO 44 | IO | H2 | V1 | R2 |
| gpio_45 | General-purpose IO 45 | IO | K2 | Y1 | T2 |
| gpio_46 | General-purpose IO 46 | IO | P1 | T1 | U1 |
| gpio_47 | General-purpose IO 47 | IO | R1 | U2 | R3 |

### Table 2-24. General-Purpose IOs Signals Description[(1)] (continued)

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | BALL BOTTOM (CBP Pkg.) [4] | BALL BOTTOM (CBC Pkg.) [4] | BALL BOTTOM (CUS Pkg.) [4] |
|---|---|---|---|---|---|
| gpio_48 | General-purpose IO 48 | IO | R2 | U1 | T3 |
| gpio_49 | General-purpose IO 49 | IO | T2 | P1 | U2 |
| gpio_50 | General-purpose IO 50 | IO | W1 | L2 | V1 |
| gpio_51 | General-purpose IO 51 | IO | Y1 | M2 | V2 |
| gpio_52 | General-purpose IO 52 | IO | H3 | AD1 | NA |
| gpio_53 | General-purpose IO 53 | IO | V8 | A3 | NA |
| gpio_54 | General-purpose IO 54 | IO | U8 | B6 | D2 |
| gpio_55 | General-purpose IO 55 | IO | T8 | B4 | F4 |
| gpio_56 | General-purpose IO 56 | IO | R8 | C4 | G5 |
| gpio_57 | General-purpose IO 57 | IO | P8 | B5 | F3 |
| gpio_58 | General-purpose IO 58 | IO | N8 | C5 | G4 |
| gpio_59 | General-purpose IO 59 | IO | T4 | N1 | W2 |
| gpio_60 | General-purpose IO 60 | IO | G3 | K2 | K5 |
| gpio_61 | General-purpose IO 61 | IO | U3 | J1 | L1 |
| gpio_62 | General-purpose IO 62 | IO | H1 | AC6 | E1 |
| gpio_63 | General-purpose IO 63 | IO | L8 | AC8 | NA |
| gpio_64 | General-purpose IO 64 | IO | K8 | B3 | NA |
| gpio_65 | General-purpose IO 65 | IO | J8 | C6 | C2 |
| gpio_66 | General-purpose IO 66 | IO | D28 | G25 | G22 |
| gpio_67 | General-purpose IO 67 | IO | D26 | K24 | E22 |
| gpio_68 | General-purpose IO 68 | IO | D27 | M25 | F22 |
| gpio_69 | General-purpose IO 69 | IO | E27 | F26 | J21 |
| gpio_70 | General-purpose IO 70 | IO | AG22 | AE21 | AC19 |
| gpio_71 | General-purpose IO 71 | IO | AH22 | AE22 | AB19 |
| gpio_72 | General-purpose IO 72 | IO | AG23 | AE23 | AD20 |
| gpio_73 | General-purpose IO 73 | IO | AH23 | AE24 | AC20 |
| gpio_74 | General-purpose IO 74 | IO | AG24 | AD23 | AD21 |
| gpio_75 | General-purpose IO 75 | IO | AH24 | AD24 | AC21 |
| gpio_76 | General-purpose IO 76 | IO | E26 | G26 | D24 |
| gpio_77 | General-purpose IO 77 | IO | F28 | H25 | E23 |
| gpio_78 | General-purpose IO 78 | IO | F27 | H26 | E24 |
| gpio_79 | General-purpose IO 79 | IO | G26 | J26 | F23 |
| gpio_80 | General-purpose IO 80 | IO | AD28 | AC26 | AC22 |
| gpio_81 | General-purpose IO 81 | IO | AD27 | AD26 | AC23 |
| gpio_82 | General-purpose IO 82 | IO | AB28 | AA25 | AB22 |
| gpio_83 | General-purpose IO 83 | IO | AB27 | Y25 | Y22 |
| gpio_84 | General-purpose IO 84 | IO | AA28 | AA26 | W22 |
| gpio_85 | General-purpose IO 85 | IO | AA27 | AB26 | V22 |
| gpio_86 | General-purpose IO 86 | IO | G25 | L25 | J22 |
| gpio_87 | General-purpose IO 87 | IO | H27 | L26 | G23 |
| gpio_88 | General-purpose IO 88 | IO | H26 | M24 | G24 |
| gpio_89 | General-purpose IO 89 | IO | H25 | M26 | H23 |
| gpio_90 | General-purpose IO 90 | IO | E28 | F25 | D23 |
| gpio_91 | General-purpose IO 91 | IO | J26 | N24 | K22 |
| gpio_92 | General-purpose IO 92 | IO | AC27 | AC25 | V21 |
| gpio_93 | General-purpose IO 93 | IO | AC28 | AB25 | W21 |
| gpio_94 | General-purpose IO 94 | IO | A24 | C23 | A22 |
| gpio_95 | General-purpose IO 95 | IO | A23 | D23 | E18 |
| gpio_96 | General-purpose IO 96 | IO | C25 | C25 | B22 |
| gpio_97 | General-purpose IO 97 | IO | C27 | C26 | J19 |
| gpio_98 | General-purpose IO 98 | IO | C23 | B23 | H24 |

### Table 2-24. General-Purpose IOs Signals Description[(1)]  (continued)

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | BALL BOTTOM (CBP Pkg.) [4] | BALL BOTTOM (CBC Pkg.) [4] | BALL BOTTOM (CUS Pkg.) [4] |
|---|---|---|---|---|---|
| gpio_99 | General-purpose IO 99 | I | AG17 | AE16 | AB18 |
| gpio_100 | General-purpose IO 100 | I | AH17 | AE15 | AC18 |
| gpio_101 | General-purpose IO 101 | IO | B24 | A24 | G19 |
| gpio_102 | General-purpose IO 102 | IO | C24 | B24 | F19 |
| gpio_103 | General-purpose IO 103 | IO | D24 | D24 | G20 |
| gpio_104 | General-purpose IO 104 | IO | A25 | C24 | B21 |
| gpio_105 | General-purpose IO 105 | I | K28 | P25 | L24 |
| gpio_106 | General-purpose IO 106 | I | L28 | P26 | K24 |
| gpio_107 | General-purpose IO 107 | I | K27 | N25 | J23 |
| gpio_108 | General-purpose IO 108 | I | L27 | N26 | K23 |
| gpio_109 | General-purpose IO 109 | IO | B25 | D25 | F21 |
| gpio_110 | General-purpose IO 110 | IO | C26 | E26 | G21 |
| gpio_111 | General-purpose IO 111 | IO | B26 | E25 | C22 |
| gpio_112 | General-purpose IO 112 | I | AG19 | AD17 | NA |
| gpio_113 | General-purpose IO 113 | I | AH19 | AD16 | NA |
| gpio_114 | General-purpose IO 114 | I | AG18 | AE18 | NA |
| gpio_115 | General-purpose IO 115 | I | AH18 | AE17 | NA |
| gpio_116 | General-purpose IO 116 | IO | P21 | U18 | V20 |
| gpio_117 | General-purpose IO 117 | IO | N21 | R18 | T21 |
| gpio_118 | General-purpose IO 118 | IO | R21 | T18 | V19 |
| gpio_119 | General-purpose IO 119 | IO | M21 | R19 | R20 |
| gpio_120 | General-purpose IO 120 | IO | N28[(3)] / T28 | W19 / N19[(3)] | M23[(3)] / R21 |
| gpio_121 | General-purpose IO 121 | IO | M27[(3)] / T25 | U20 / L18[(3)] | L23[(3)] / R23 |
| gpio_122 | General-purpose IO 122 | IO | N27[(3)] / R28 | V19 / M19[(3)] | M22[(3)] / P23 |
| gpio_123 | General-purpose IO 123 | IO | N26[(3)] | M18[(3)] | M21[(3)] |
| gpio_124 | General-purpose IO 124 | IO | N25[(3)] / T26 | W18 / K18[(3)] | M20[(3)]/R22 |
| gpio_125 | General-purpose IO 125 | IO | P28[(3)] / T27 | V20 / N20[(3)] | N23[(3)]/T24 |
| gpio_126 | General-purpose IO 126 | IO | D25 / P27[(3)] | M20[(3)] / D26 | J20 / N22[(3)] |
| gpio_127 | General-purpose IO 127 | IO | P26[(3)] | P17[(3)] | NA |
| gpio_128 | General-purpose IO 128 | IO | R27 | P18 | NA |
| gpio_129 | General-purpose IO 129 | IO | R25[(3)] | P19[(3)] | P24[(3)] |
| gpio_130 | General-purpose IO 130 | IO | AE2 / U28 | Y20 / W10 | Y1 / T23 |
| gpio_131 | General-purpose IO 131 | IO | AG5 / U27 | V18 / R10 | AB5 / U24 |
| gpio_132 | General-purpose IO 132 | IO | AH5 | T10 | AB3 |
| gpio_133 | General-purpose IO 133 | IO | AH4 | T9 | Y3 |
| gpio_134 | General-purpose IO 134 | IO | AG4 | U10 | W3 |
| gpio_135 | General-purpose IO 135 | IO | AF4 | U9 | V3 |
| gpio_136 | General-purpose IO 136 | IO | AE4 | V10 | AB2 |
| gpio_137 | General-purpose IO 137 | IO | AH3 | M3 | AA2 |
| gpio_138 | General-purpose IO 138 | IO | AF3 | L3 | Y2 |
| gpio_139 | General-purpose IO 139 | IO | AE3 | K3 | AA1 |
| gpio_140 | General-purpose IO 140 | IO | AF6 | P3 | V6 |
| gpio_141 | General-purpose IO 141 | IO | AE6 | N3 | V5 |
| gpio_142 | General-purpose IO 142 | IO | AF5 | U3 | W4 |
| gpio_143 | General-purpose IO 143 | IO | AE5 | W3 | V4 |
| gpio_144 | General-purpose IO 144 | IO | AB26 | Y24 | NA |
| gpio_145 | General-purpose IO 145 | IO | AB25 | AA24 | NA |
| gpio_146 | General-purpose IO 146 | IO | AA25 | AD22 | NA |
| gpio_147 | General-purpose IO 147 | IO | AD25 | AD21 | NA |
| gpio_148 | General-purpose IO 148 | IO | AA8 | L4 | W7 |
| gpio_149 | General-purpose IO 149 | IO | AA9 | R2 | W6 |

**Table 2-24. General-Purpose IOs Signals Description(1) (continued)**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | BALL BOTTOM (CBP Pkg.) [4] | BALL BOTTOM (CBC Pkg.) [4] | BALL BOTTOM (CUS Pkg.) [4] |
|---|---|---|---|---|---|
| gpio_150 | General-purpose IO 150 | IO | W8 | W2 | AC2 |
| gpio_151 | General-purpose IO 151 | IO | Y8 | H3 | V7 |
| gpio_152 | General-purpose IO 152 | IO | AE1 | V3 | NA |
| gpio_153 | General-purpose IO 153 | IO | AD1 | U4 | NA |
| gpio_154 | General-purpose IO 154 | IO | AD2 | R3 | NA |
| gpio_155 | General-purpose IO 155 | IO | AC1 | T3 | NA |
| gpio_156 | General-purpose IO 156 | IO | Y21 | U19 | W19 |
| gpio_157 | General-purpose IO 157 | IO | AA21 | V17 | AB20 |
| gpio_158 | General-purpose IO 158 | IO | V21 | U17 | W18 |
| gpio_159 | General-purpose IO 159 | IO | U21 | T20 | Y18 |
| gpio_160 | General-purpose IO 160 | IO | T21 | T19 | AA18 |
| gpio_161 | General-purpose IO 161 | IO | K26 | P20 | AA19 |
| gpio_162 | General-purpose IO 162 | IO | W21 | T17 | V18 |
| gpio_163 | General-purpose IO 163 | IO | H18 | F23 | A23 |
| gpio_164 | General-purpose IO 164 | IO | H19 | F24 | B23 |
| gpio_165 | General-purpose IO 165 | IO | H20 | H24 | B24 |
| gpio_166 | General-purpose IO 166 | IO | H21 | G24 | C23 |
| gpio_167 | General-purpose IO 167 | IO | B23 | A23 | F18 |
| gpio_168 | General-purpose IO 168 | IO | AF15 | C2 | AC15 |
| gpio_169 | General-purpose IO 169 | IO | U26 | W20 | U23 |
| gpio_170 | General-purpose IO 170 | IO | J25 | J23 | A24 |
| gpio_171 | General-purpose IO 171 | IO | AB3 | P9 | T5 |
| gpio_172 | General-purpose IO 172 | IO | AB4 | P8 | R4 |
| gpio_173 | General-purpose IO 173 | IO | AA4 | P7 | T4 |
| gpio_174 | General-purpose IO 174 | IO | AC2 | R7 | T6 |
| gpio_175 | General-purpose IO 175 | IO | AC3 | R8 | NA |
| gpio_176 | General-purpose IO 176 | IO | AB1 | R9 | NA |
| gpio_177 | General-purpose IO 177 | IO | AB2 | T8 | R5 |
| gpio_178 | General-purpose IO 178 | IO | AA3 | W7 | N5 |
| gpio_179 | General-purpose IO 179 | IO | Y2 | W8 | N4 |
| gpio_180 | General-purpose IO 180 | IO | Y3 | U8 | N3 |
| gpio_181 | General-purpose IO 181 | IO | Y4 | V8 | M5 |
| gpio_182 | General-purpose IO 182 | IO | V3 | V9 | M4 |
| gpio_183 | General-purpose IO 183 | IO | AE15 | C1 | AC14 |
| gpio_184 | General-purpose IO 184 | IO | AF14 | AB4 | AC13 |
| gpio_185 | General-purpose IO 185 | IO | AG14 | AC4 | AC12 |
| gpio_186 | General-purpose IO 186 | IO | AE22 | W11 | AA6 |
| gpio_188 | General-purpose IO 188 | IO | U25 | W17 | W24 |
| gpio_189 | General-purpose IO 189 | IO | V28 | Y18 | V23 |
| gpio_190 | General-purpose IO 190 | IO | V27 | Y19 | W23 |
| gpio_191 | General-purpose IO 191 | IO | V26 | Y17 | T22 |

(1) NA in table stands for "Not Applicable".

(2) The subsystem pin multiplexing options are not described in Table 2-1 and Table 2-4.

(3) The usage of this GPIO is strongly restricted. For more information, see the General-Purpose Interface / General-Purpose Interface Environment section of the *AM/DM37x Multimedia Device Technical Reference Manual* (literature number SPRUGN4).

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### 2.5.8 Power Supplies

**Note**: For more information, see Power Reset and Clock Management / PRCM Environment and the Power, Reset, and Clock Management / PRCM Functional Description / PRCM Voltage Management Functional Description sections of the *AM/DM37x Multimedia Device Technical Reference Manual* (literature number SPRUGN4).

**Table 2-25. Power Supplies Signals Description[1]**

| SIGNAL NAME [1] | DESCRIPTION [2] | BALL BOTTOM (CBP Pkg.) [4] | BALL TOP (CBP Pkg.) [2][5] | BALL BOTTOM (CBC Pkg.) [4] | BALL TOP (CBC Pkg.) [2][5] | BALL BOTTOM (CUS Pkg.) [2] [4] |
|---|---|---|---|---|---|---|
| vdd_mpu_iva | MPU/IVA power supply | Y9 / W9 / T9 / R9 / M9 / L9 / J9 / Y10 / U10 / T10 / R10 / N10 / M10 / L10 / J10 / Y11 / W11 / K11 / J11 / W12 / K13 / Y14 / K14 / J14 / Y15 / W15 / J15 | NA | H7/ N7/ U7/ V7/ N8/ G9/ L9/ M9/ W9/ Y9/ M10/ P10/ K11/ U11/ V11/ Y11/ G12/ D13/ U13 | NA | W13/ W12/ V13/ V12/ U13/ U12/ T8/ T7/ R8/ R7/ R6/ N8/ N7/ N6/ M12/ M8/ M7/ M6/ L12/ L11/ J10/ J9/ H10/ H9/ G10/ G9/F10 |
| vdd_core | Core power domain | AC4 / J4 / H4 / D8 / AE9 / D9 / D15 / Y16 / AE18 / Y18 / W18 / K18 / J18 / AE19 / Y19 / U19 / T19 / N19 / M19 / J19 / Y20 / W20 / V20 / U20 / P20 / N20 / K20 / J20 / D22 / D23 / AE24 / M25 / L25 / E25 | NA | M7/ T7/ Y8/ G11/ Y12/ D15/ M17/ G18/ H20/ R20/ AC21 | NA | T20/ T19/ T18/ T17/ R19/ R18/ R17/ M15/ M14/ L15/ L14/ K19/ K18/ K17/ J18/ J17/ H13/ H12/ G13/ G12/ F13/ F12 |
| cap_vddu_wkup_logic | Decoupling capacitor for WKUP/EMU domains (logic) | AA15 | NA | K14 | NA | Y12 |
| vdda_dplls_dll | Input power for the analog part of the MPU, CORE DPLLs, IVA, and the DLL | K15 | NA | K13 | NA | G18 |
| vdda_dac | Video DAC power plane | V25 | NA | V25 | NA | AB13 |
| vssa_dac | Video DAC ground plane | Y26 | NA | V24 | NA | AB15 |
| vdds | 1.8-V power for standard IOs | AD3 / AD4 / W4 / AF8 / AE8 / AF16 / AE16 / AF23 / AE23 / F25 / F26 / AG27 | NA | G4/ M4/ T4/ Y4/ L7/ AC7/ D9/ AE10/ C11/ J15/ AC15/ A18/ J18/ AC18/ AD20/ E24/ L24/ T24/ W24/ AC24 / AB24 | A3 / A15 / B5 / F2 / F21/ L20 / W21 | Y9 / W10 / W9 / V10 / V9 / U10 / N19 / N18 / N17 / M19 / M18 / M17 |
| vdds_mem | Memory IO power plane | U1 / J1 / F1 / J2 / F2 / R4 / B5 / A5 / AH6 / B8 / A8 / B12 / A12 / D16 / C16 / B18 / A18 / B22 / A22 / G28 / C28 | AC5 / P1 / H1 / F23 / E1 / C23 / A4 / A7 / A10 / A15 / A18 | NA | NA | K8 / K7 / K6 / J8 / J7 / J6 / H15 / G16 / G15 / F16 / F15 / E16 |
| vdda_dpll_per | Input power for the analog part of the Peripheral DPLLs | AA16 | NA | U14 | NA | U17 |
| vdda_wkup_bg_bb | For wakeup LDO and VDDA (2 LDOs SRAM and BG) | AA14 | NA | W14 | NA | AA13 |

## Table 2-25. Power Supplies Signals Description[1] (continued)

| SIGNAL NAME [1] | DESCRIPTION [2] | BALL BOTTOM (CBP Pkg.) [4] | BALL TOP (CBP Pkg.) [2][5] | BALL BOTTOM (CBC Pkg.) [4] | BALL TOP (CBC Pkg.) [2][5] | BALL BOTTOM (CUS Pkg.) [2] [4] |
|---|---|---|---|---|---|---|
| vss | Ground | AG2 / U2 / B2 / AG3 / W3 / P3 / J3 / E3 / A3 / P4 / E4 / AG6 / D7 / C7 / V9 / U9 / P9 / N9 / K9 / W10 / V10 / P10 / K10 / D10 / C10 / AF12 / AE12 / Y12 / K12 / J12 / Y13 / W13 / J13 / D13 / C13 / W14 / K16 / J16 / W17 / K17 / J17 / W19 / V19 / R19 / P19 / L19 / K19 / D19 / C19 / AF20 / AE20 / T20 / R20 / M20 / L20 / D21 / C22 / AC25 / Y25 / W25 / AC26 / R26 / L26 / A26 / G27 / B27 | H2 / B18 / AB5 / AB14 / AB20 / P2 / F22 / E2 / C22 / B4 / B7 / B10 / B15 | G1/ K1/ R1/ W1/ B2/ H4/ N4/ R4/ W4/ AB5/ A6/ D7/ Y7/AE7/ A8/ G8/ D10/ G10/ L10/ N10/ Y10/ AC10/ C12/ D12/A13/ D14/ AD14/ K15/ Y16/ L17/ N17/ R17/ D18/ D20/G20/ E22/ AB22/ G23/ L23/ T23/ W23/ B25/ K25/U25/ AD25 / Y26 | C1/ F1/ H2/ M2/ R2/ Y6/AA7/ Y11/ AA16/ W20/P20/ L21/ H20/ F20/ B14/A13/ A7 | V16/ V15/ U16/ U15/ U14/ U11/ U9/T16/ T15/ T14/ T13/ T12/ T11/ T10/ T9/ R15/ R14/ R11/ R10/ P17/ P15/ P14/ P13/P12/ P11/ P10/ P8/ N16/ N15/ N14/ N13/ N12/ N11/ N10/ N9/ M16/ M13/ M11/ M10/ M9/ L17/ L13/ L10/ L8/ K15/ K14/ K11/ K10/ J16/ J15/ J14/ J13/ J12/ J11/H16/ H14/ H11 |
| vdds_sram | SRAM LDOs | W16 | NA | U12 | NA | AA12 |
| vdds_mmc1 | Input power for MMC1 dual voltage buffers | K25 | NA | N23 | NA | N24 |
| vdds_x | Power supply for dual voltage GPIOs | P25 | NA | P23 | NA | H8 |
| vss | Ground | M28 | NA | L19 | NA | NA |
| vdds | IO power plane | AG20 | NA | AD18 | NA | NA |
| vss | Ground | AG16 | NA | AC16 | NA | NA |
| vdds | IO power plane | H28 | NA | L20 | NA | NA |
| cap_vdd_sram_mpu_iva | Decoupling capacitor for SRAM in processor domains | V4 | NA | N9 | NA | U8 |
| cap_vdd_sram_core | Decoupling capacitor for CORE domain (SRAM) | L21 | NA | K20 | NA | H17 |
| vdds | IO power plane | AG21 | NA | AD19 | NA | NA |
| cap_vddu_array | Decoupling capacitor for WKUP/EMU domains (array) | AH20 | NA | AE19 | NA | N20 |
| vss | Ground | AH21 | NA | AC19 | NA | NA |
| cap_vdd_bb_mpu_iva | Decoupling capacitor for processor domains (bb) | U4 | NA | D6 | NA | N21 |
| sys_xtalgnd | Kelvin ground | Y17 | NA | AF23 | NA | W15 |

(1) NA in this table stands for "Not applicable".

(2) For a list of pins not supported on a particular package, see Table 2-4.

## 2.5.9 System and Miscellaneous Terminals

**Note**: For more information, see the Power, Reset, and Clock Management / PRCM Environment section of the *AM/DM37x Multimedia Device Technical Reference Manual* (literature number SPRUGN4).

### Table 2-26. System and Miscellaneous Signals Description[1]

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | BALL BOTTOM (CBP Pkg.) [4] | BALL TOP (CBP Pkg.) [2][5] | BALL BOTTOM (CBC Pkg.) [4] | BALL TOP (CBC Pkg.) [2][5] | BALL BOTTOM (CUS Pkg.) [4] |
|---|---|---|---|---|---|---|---|
| sys_32k | 32-kHz clock input | I | AE25 | NA | AE20 | NA | AA16 |
| sys_xtalin | Main input clock. Oscillator input or LVCMOS at 19.2, 13, or 12 MHz. | AI-I | AE17 | NA | AF19 | NA | AD15 |
| sys_xtalout | Output of oscillator | AO | AF17 | NA | AF20 | NA | AD14 |
| sys_altclk | Alternate clock source selectable for GPTIMERs (maximum 54 MHz), USB (48 MHz), or NTSC/PAL (54 MHz) | I | J25 | NA | J23 | NA | A24 |
| sys_clkreq | Request from device for system clock (open source type) | IO | AF25 | NA | W15 | NA | Y13 |
| sys_clkout1 | Configurable output clock1 | O | AG25 | NA | AE14 | NA | Y7 |
| sys_clkout2 | Configurable output clock2 | O | AE22 | NA | W11 | NA | AA6 |
| sys_boot0 | Boot configuration mode bit 0 | I | AH26 | NA | F3 | NA | AB12 |
| sys_boot1 | Boot configuration mode bit 1 | I | AG26 | NA | D3 | NA | AC16 |
| sys_boot2 | Boot configuration mode bit 2 | I | AE14 | NA | C3 | NA | AD17 |
| sys_boot3 | Boot configuration mode bit 3 | I | AF18 | NA | E3 | NA | AD18 |
| sys_boot4 | Boot configuration mode bit 4 | I | AF19 | NA | E4 | NA | AC17 |
| sys_boot5 | Boot configuration mode bit 5 | I | AE21 | NA | G3 | NA | AB16 |
| sys_boot6 | Boot configuration mode bit 6 | I | AF21 | NA | D4 | NA | AA15 |
| sys_nrespwron | Power On Reset | I | AH25 | NA | V13 | NA | AA10 |
| sys_nreswarm | Warm Boot Reset (open drain output) | IOD | AF24 | NA | AD7 | AA5 | Y10 |
| sys_nirq | External FIQ input | I | AF26 | NA | V16 | NA | W16 |
| sys_nvmode1 | Indicates the voltage mode | O | AD26 | NA | AD15 | NA | Y16 |
| sys_nvmode2 | Indicates the voltage mode | O | AE26 | NA | W16 | NA | Y15 |
| sys_off_mode | Indicates the voltage mode | O | AF22 | NA | V12 | NA | AD23 |
| sys_ndmareq0 | External A request 0 (system expansion). Level (active low) or edge (falling) selectable. | I | U8 | NA | B6 | NA | D2 |
| sys_ndmareq1 | External A request 1 (system expansion). Level (active low) or edge (falling) selectable. | I | T8 / J8 | NA | B4 / C6 | NA | F4 / C2 |
| sys_ndmareq2 | External A request 2 (system expansion). Level (active low) or edge (falling) selectable. | I | L3 / R8 | NA | D1 / C4 | NA | H2 / G5 |
| sys_ndmareq3 | External A request 3 (system expansion). Level (active low) or edge (falling) selectable. | I | K3 / P8 | NA | D2 / B5 | NA | G2 / F3 |

(1) NA in this table stands for "Not applicable".

(2) For a list of pins not supported on a particular package, see Table 2-4.

### Table 2-27. CBC Package Feed-Through Balls

| JEDEC 14x14mm, 0.65mm, 152ball | JEDEC DESCRIPTION [1] | BALL TOP | BALL BOTTOM | FEED-THROUGH BALL NAME |
|---|---|---|---|---|
| NC | No Connect | A1 | A1 | pop_a1_a1 |
| d-vdd | DDR Supply | J1 | L1 | pop_j1_l1 |
| NC | No Connect | AA1 | AF1 | NC |
| f-vdd | Flash Supply | N2 | T2 | pop_n2_t2 |
| f-vdd | Flash Supply | T2 | Y2 | pop_t2_y2 |
| NC | No Connect | W2 | AE2 | pop_w2_ae2 |
| NC | No Connect | Y2 | AF4 | pop_y2_af4 |
| f-vdd | Flash Supply | AA6 | AF5 | pop_aa6_af5 |
| f-vdd | Flash Supply | Y7 | AF8 | pop_y7_af8 |

### Table 2-27. CBC Package Feed-Through Balls (continued)

| NC, Int | No Connect; Interrupt when using OneNAND POP | Y9 | AF10 | pop_y9_af10 |
|---|---|---|---|---|
| f-nbe0, cle0 | No Connect/CLE | AA10 | AF12 | pop_aa10_af12 |
| d-vdd | DDR Supply/ POP FLASH vpp supply | AA11 | AF13 | pop_aa11_af13 |
| d-tq | No Connect/ DDR die temperature sensor | AA12 | AF14 | pop_aa12_af14 |
| vss | Shared Ground | AA13 | AF15 | pop_aa13_af15 |
| d-vdd | DDR Supply | Y14 | AF17 | pop_y14_af17 |
| d-vddq | DDR Supply | AA14 | AF16 | pop_aa14_af16 |
| d-vdd | DDR Supply | B16 | A20 | pop_b16_a20 |
| vss | Shared Ground | Y17 | AF21 | pop_y17_af21 |
| d-vdd | DDR Supply | AA17 | AF18 | pop_aa17_af18 |
| vss | Shared Ground | Y19 | AF24 | pop_y19_af24 |
| d-vddq | DDR Supply | AA19 | AF22 | pop_aa19_af22 |
| NC | No Connect | A20 | A25 | pop_a20_a25 |
| NC | No Connect | Y20 | AE25 | pop_y20_ae25 |
| NC | No Connect | AA20 | AF25 | pop_aa20_af25 |
| NC | No Connect | A21 | A26 | pop_a21_a26 |
| NC | No Connect | B21 | B26 | pop_b21_b26 |
| d-vdd | DDR Supply | H21 | K26 | pop_h21_k26 |
| d-vdd | DDR Supply | P21 | U26 | pop_p21_u26 |
| NC | No Connect | Y21 | AE26 | pop_y21_ae26 |
| NC | No Connect | AA21 | AF26 | pop_aa21_af26 |

(1) For more details on the feedthrough pin connections, please refer to the PoP memory datasheet.

### Table 2-28. CBP Package Feed-Through Balls

| JEDEC 12x12, 0.5mm, 168ball | JEDEC DESCRIPTION [1] | BALL TOP | BALL BOTTOM | FEED-THROUGH BALL NAME |
|---|---|---|---|---|
| d-vdd | DDR Supply | A12 | A15 | pop_a12_a15 |
| d-vdd | DDR Supply | AA23 | AE28 | pop_aa23_ae28 |
| d-vdd | DDR Supply | H23 | AF28 | pop_h23_af28 |
| d-vdd | DDR Supply | K1 | J28 | pop_k1_j28 |
| d-vdd | DDR Supply | Y23 | M1 | pop_y23_m1 |
| f-vdd | Flash Supply | AA1 | AA1 | pop_aa1_aa1 |
| f-vdd | Flash Supply | AC8 | AF1 | pop_ac8_af1 |
| f-vdd | Flash Supply | AC13 | AH10 | pop_ac13_ah10 |
| f-vdd | Flash Supply | L1 | AH15 | pop_l1_ah15 |
| f-vdd | Flash Supply | U1 | N1 | pop_u1_n1 |
| f-vpp | Flash vpp supply | AC11 | AH13 | pop_ac11_ah13 |
| NC, int0 | No Connect/PoP OneNAND interrupt | AB9 | AG11 | pop_ab9_ag11 |
| NC, int1 | No Connect/PoP OneNAND interrupt | AC9 | AH11 | pop_ac9_ah11 |
| NC | No Connect | A1 | A1 | NC |
| NC | No Connect | A2 | A2 | NC |
| NC | No Connect | A22 | A27 | pop_a22_a27 |
| NC | No Connect | A23 | A28 | pop_a23_a28 |
| NC | No Connect | AB1 | AG1 | pop_ab1_ag1 |
| NC | No Connect | AB23 | AG28 | pop_ab23_ag28 |
| NC | No Connect | AC1 | AH1 | pop_ac1_ah1 |
| NC | No Connect | AC2 | AH2 | pop_ac2_ah2 |
| NC | No Connect | AC22 | AH27 | pop_ac22_ah27 |
| NC | No Connect | AC23 | AH28 | pop_ac23_ah28 |

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**Table 2-28. CBP Package Feed-Through Balls (continued)**

| NC | No Connect | B1 | B1 | NC |
|---|---|---|---|---|
| NC | No Connect | B23 | B28 | pop_b23_b28 |
| f-rst#, rp# | Flash reset | AB11 | AG13 | pop_ab11_ag13 |
| d-tq | DDR temperature alert | AC14 | AH16 | pop_ac14_ah16 |
| vss | Shared Ground | AA2 | AA2 | pop_aa2_aa2 |
| vss | Shared Ground | U2 | AF2 | pop_u2_af2 |
| vss | Shared Ground | AA22 | AF27 | pop_aa22_af27 |
| vss | Shared Ground | AB8 | AG10 | pop_ab8_ag10 |
| vss | Shared Ground | AB13 | AG15 | pop_ab13_ag15 |
| vss | Shared Ground | B12 | B15 | pop_b12_b15 |
| vss | Shared Ground | H22 | J27 | pop_h22_j27 |
| vss | Shared Ground | K2 | M2 | pop_k2_m2 |
| vss | Shared Ground | K22 | M26 | pop_k22_m26 |
| vss | Shared Ground | L2 | N2 | pop_l2_n2 |

(1) For more details on the feedthrough pin connections, please refer to the PoP memory datasheet.

# 3 Electrical Characteristics

**NOTE**

For more information, see the Power Reset and Clock Management / PRCM Environment section of the AM/DM37x Multimedia Device Technical Reference Manual (literature number SPRUGN4).

## 3.1 Absolute Maximum Ratings

Stresses beyond those listed as absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under "Recommended Operating Conditions" is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

**Table 3-1. Absolute Maximum Rating over Junction Temperature Range**

| PARAMETER | | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| vdd_mpu_iva | Supply voltage range for MPU / IVA domain | | | −0.5 | 1.5 | V |
| vdd_core | Supply voltage range for core domain | | | −0.5 | 1.5 | V |
| vdda_wkup_bg_bb | Supply voltage range for wake-up domain (internal LDO) | | | −0.5 | 2.1 | V |
| vdda_dplls_dll | Supply voltage for MPU, IVA, Core DPLLs, and DLL | | | −0.5 | 2.1 | V |
| vdda_dpll_per | Supply voltage for DPLLs (peripherals) | | | −0.5 | 2.1 | V |
| vdds_sram | Supply voltage for SRAM LDOs | | | −0.5 | 2.1 | V |
| vdda_dac | Supply voltage for video buffers and DAC | | | −0.5 | 2.1 | V |
| vdds | Supply voltage for 1.8-V I/O macros | | | −0.5 | 2.1 | V |
| vdds_mem | Supply voltage for memory buffers | | | −0.5 | 2.1 | V |
| vdds_mmc1 | Supply voltage range for mmc1 dual voltage IOs | | | −0.5 | 3.8 | V |
| vdds_x | Supply voltage range for dual voltage GPIOs | | | −0.5 | 3.8 | V |
| $V_{ESD}$ | ESD stress voltage[1] | HBM (Human Body Model)[2] | JTAG[9] | 200 | | V |
| | | | CAM[6] | 400 | | |
| | | | GPMC[8] | 500 | | |
| | | | Other signals | 1000 | | |
| | | CDM (Charged Device Model)[3] | | 250 | | |
| $I_{IOI}$ | Current-pulse injection on each IO pin[5] | | | 200 | | mA |
| $I_{clamp}$ | Clamp current for an input or output | | | −20 | 20 | mA |
| $T_{STG}$ [4] | Storage temperature range | | | −65 | 150 | °C |

(1) Electrostatic discharge (ESD) to measure device sensitivity/immunity to damage caused by electrostatic discharges into the device.

(2) Level listed above is the passing level per ANSI/ESDA/JEDEC JS-001-2010. JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process, and manufacturing with less than 500V HBM is possible if necessary precautions are taken. Pins listed as 1000V may actually have higher performance.

(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101E. JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process. Pins listed as 250V may actually have higher performance.

(4) For tape and reel the storage temperature range is [–10°C; +50°C] with a maximum relative humidity of 70%. It is recommended returning to ambient room temperature before usage.

(5) Each device is tested with an IO pin injection of 200 mA with a stress voltage of 1.5 times the maximum Vdd at room temperature.

(6) Corresponding signals: cam_d0, cam_d1, cam_d6, cam_d7, cam_d8, cam_d9. Refer to Multiplexing Characteristics to determine the ball information per package.

(7) Corresponding signals: dss_data0, dss_data1, dss_data2, dss_data3, dss_data4, dss_data5. Refer to Multiplexing Characteristics to determine the ball information per package.

(8) Corresponding signals: All 46 GPMC interface signals (vdds_mem is not included to this exception list). Refer to Multiplexing Characteristics to determine the ball information per package.

(9) Corresponding signals: All 8 JTAG interface signals (jtag_emu0, jtag_emu1, jtag_ntrst, jtag_rtck, jtag_tck, jtag_tdi, jtag_tdo, jtag_tms_tmsc). Refer to Multiplexing Characteristics to determine the ball information per package.

Table 3-2 summarizes the power consumption at the ball level.

**Table 3-2. Maximum Current Ratings at Ball Level** [3]

| PARAMETER | | | MAX | UNIT |
|---|---|---|---|---|
| **SIGNAL** | **DESCRIPTION** | | | |
| vdd_mpu_iva[7] | Maximum current rating for MPU / IVA domain | Processors | DM3730/DM3725 (1G Hz) | 1400[1][4] | mA |
| | | | DM3730/DM3725 (800M Hz) | 1200[5] | |
| | | | DM3730/DM3725 (600M Hz) | 800[5] | |
| vdd_core[1] | Maximum current rating for core domain | Core | DM3730 | 300 | mA |
| | | | DM3725 | 230 | |
| vdds | Maximum current rating for 1.8-V I/O macros | | | 60 | mA |
| vdds_mem | Maximum current rating for memory buffers | | | 35 | mA |
| vdds_mmc1[2] | Maximum current rating for mmc1 dual voltage buffers | | | 20 | mA |
| vdds_x | Maximum current rating for GPIO dual voltage buffers | | | 2 | mA |
| vdda_wkup_bg_bb | Maximum current rating for wake-up, bandgap and VBB LDOs | | | 5 | mA |
| vdda_dac | Maximum current rating for video buffers and DAC | | | 60 | mA |
| vdda_dplls_dll | Maximum current rating for MPU, IVA, core DPLLs and DLL | | | 30 | mA |
| vdda_dpll_per | Maximum current rating for DPLLs (peripherals) | | | 10 | mA |
| vdds_sram | Maximum current rating for SRAM LDOs (common) | | | 41 | mA |

(1) With SmartReflex[TM] enabled.

(2) MMC card and I/O card are not included.

(3) The maximum current ratings documented in this table are preliminary data which are subject to change.

(4) Conditions used for maximum current ratings are worst case:
   – $T_J$ is up to 90C
   – Cold process is used
   – $V_{DD1}$ (vdd_mpu_iva) supplies 1.38 V (maximum voltage supported)

In these conditions, the current listed as 1400mV is the addition of the:
   – Current when running Dhrystone on ARM@1GHz multiplied by a factor x1.5 (to take care of NEON activity)
   – Current when running H.264 on IVA@800MHz with a x1.1 factor (to take care of more aggressive SW than H.264)

(5) Conditions used for maximum current ratings are worst case:
   – $T_J$ is up to 90C
   – Hot process is used
   – $V_{DD1}$ (vdd_mpu_iva) nominal OPP voltage:
      – DM3730 (800M Hz): @1.27V
      – DM3730 (600M Hz): @1.14V

(6) This maximum vdd_mpu_iva current is observed at OPP1G operating point.

(7) Depending on the microprocessor chosen, the IVA feature may or may not be supported. See the Features section for more information on device features.

## 3.2 Recommended Operating Conditions

The device is used under the recommended operating conditions described in Table 3-4. The POH information in Table 3-3 is provided solely for your convenience and does not extend or modify the warranty provided under TI's standard terms and conditions for TI semiconductor products.

### Table 3-3. Reliability Data

| JUNCTION TEMP | TOTAL DEVICE LIFETIME | ≥OPP130 MAX TIME | OPP1G MAX TIME |
|---|---|---|---|
| @105C | 89K POH | Not available | Not available |
| @90C | 100K POH | 45K | 25K(1) |
| @75C | >100K POH | 100K POH | 75K |

(1)  If device is only operated at OPP1G, then POH can be extended to 35K POH.

---

**NOTE**

Logic functions and parameter values are not assured out of the range specified in the recommended operating conditions.

---

### Table 3-4. Recommended Operating Conditions

| PARAMETER | DESCRIPTION | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| vdd_mpu_iva | Supply voltage range for ARM / IVA domain | | | See(1) | | V |
| | Maximum Noise (peak-peak) | | | 40 | | mV$_{PP}$ |
| vdd_core | Supply voltage range for core domain | | | See(1) | | V |
| | Maximum Noise (peak-peak) | | | 40 | | mV$_{PP}$ |
| vdds | Supply voltage for 1.8-V I/O macros | | 1.71 | 1.80 | 1.91 | V |
| | Maximum Noise (peak-peak) | Oscillator IO (Crystal or Square modes) | | 40 | | mV$_{PP}$ |
| | | Others | | 90 | | |
| vdds_mem | Supply voltage for memory buffers | | 1.71 | 1.80 | 1.91 | V |
| | Maximum Noise (peak-peak) | | | 90 | | mV$_{PP}$ |
| vdds_mmc1 | Supply voltage range for mmc1 dual voltage IOs | 1.8-V mode | 1.71 | 1.80 | 1.91 | V |
| | | 3.0-V mode | 2.70 | 3.00 to 3.30 | 3.60 | |
| | Noise (peak-peak) | 1.8-V mode | | 90 | | mV$_{PP}$ |
| | | 3.0-V mode | | 150 | | |
| vdds_x | Supply voltage range for x dual voltage IOs | 1.8-V mode | 1.71 | 1.80 | 1.91 | V |
| | | 3.0-V mode | 2.70 | 3.00 | 3.60 | |
| | Maximum Noise (peak-peak) | 1.8-V mode | | 90 | | mV$_{PP}$ |
| | | 3.0-V mode | | 150 | | |
| vdda_wkup_bg_bb | Supply voltage range for wake-up LDO | | 1.71 | 1.80 | 1.91 | V |
| | Maximum Noise (peak-peak) | | | 50 | | mV$_{PP}$ |
| vdda_dac | Analog supply voltage for Video DAC | | 1.71 | 1.80 | 1.91 | V |
| | Maximum Noise (peak-peak) for a frequency from 0 to 100 kHz (For a frequency > 100 kHz, decreases 20 dB/dec) | | | 30 | | mV$_{PP}$ |
| vdds_sram | Supply voltage for SRAM LDOs | | 1.71 | 1.80 | 1.91 | V |
| | Maximum Noise (peak-peak) | | | 50 | | mV$_{PP}$ |
| vdda_dplls_dll | Supply voltage for MPU, IVA, core DPLLs and DLL | | 1.71 | 1.80 | 1.91 | V |
| | Maximum Noise (peak-peak) For any frequency | | | 30 | | mV$_{PP}$ |

**Table 3-4. Recommended Operating Conditions (continued)**

| PARAMETER | DESCRIPTION | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| vdda_dpll_per | Supply voltage for DPLLs (peripherals) | | 1.71 | 1.80 | 1.91 | V |
| | Maximum Noise (peak-peak) For any frequency | | | 50 | | mV$_{PP}$ |
| vssa_dac | Ground for video buffers and DAC | | | 0 | | V |
| vss | Main ground | | | 0 | | V |
| T$_J$ | Operating junction temperature range | Commercial Temperature | 0 | | 90 | °C |
| | | Industrial Temperature | -40 | | 90 | |
| | | Extended Temperature | -40 | | 105 | |

(1) See Section 4.3.4, *Processor Clocks*. OPP voltage values may change following the silicon characterization result.

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Product Folder Link(s): *DM3730  DM3725*

## 3.3 DC Electrical Characteristics

Table 3-5 summarizes the dc electrical characteristics.

Note: The interfaces or signals described in Table 3-5 correspond to the interfaces or signals available in multiplexing mode 0. All interfaces or signals multiplexed on the balls / pins described in Table 3-5 have the same DC electrical characteristics.

**Table 3-5. DC Electrical Characteristics**

| PARAMETER | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| **SDRC Mode (CBP Balls[19]: C14 / B14 / C15 / B16 / D17 / C17 / B17 / D18 / H9 / H10 / H11 / H12 / A13 / A14 / H16 / H17 / H14 / H13 / H15 / A16 / A17)[4]** | | | | | |
| $V_{IH}$ | High-level input voltage | 0.7 * vdds_mem | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.3 * vdds_mem | V |
| $V_{HYS}$ [1] | Hysteresis voltage at an input | 0.07 | | | V |
| $V_{OH}$ | High-level output voltage, driver enabled, pullup or pulldown disabled    $I_{OH}$ = −4 mA | 0.8 * vdds_mem | | vdds_mem | V |
| $V_{OL}$ | Low-level output voltage, driver enabled, pullup or pulldown disabled    $I_{OL}$ = 4 mA | 0 | | 0.2 * vdds_mem | V |
| $C_{IN}$ | Input capacitance | | | 1.15 | pF |
| $t_{TIN}$ [2] | Input recommended rise, $t_{RIN}$, and fall time, $t_{FIN}$ (measured between 20% and 80% at PAD) | | | 10 | ns |
| $t_{ROUT}$ [2] | Output maximum rise time (rise time, $t_{ROUT}$, evaluated between 20% and 80% at PAD) @ maximum load | | | 1.15 | ns |
| $t_{FOUT}$ [2] | Output maximum fall time (fall time, $t_{FOUT}$, evaluated between 20% and 80% at PAD) @ maximum load | | | 1.10 | ns |
| $C_{OUT}$ | Load capacitance    DS0 = 0 [3] | 2 | | 4 | pF |
| | DS0 = 1 [3] | 4 | | 12 | |
| **MMC Interface 1 Mode (CBP Balls[19]: N28 / M27 / N27 / N26 / N25 / P28)** | | | | | |
| **1.8-V Mode** | | | | | |
| $V_{IH}$ | High-level input voltage | 0.70 * vdds_mmc1 | | vdds_mmc1 + 0.3 | V |
| $V_{IL}$ | Low-level input voltage | −0.3 | | 0.30 * vdds_mmc1 | V |
| $V_{OH}$ | High-level output voltage with 100-μA sink current $I_{OH}$ | vdds_mmc1 − 0.2 | | | V |
| $V_{OL}$ | Low-level output voltage with 100-μA sink current at vdds_mmc1 minimum | | | 0.2 | V |
| $V_{HYS}$ [1] | Hysteresis voltage at an input | 0.1 | | | V |
| $t_{TIN}$ [2] | Input transition time ($t_{RIN}$ or $t_{FIN}$ evaluated between 10% and 90% at PAD)    Normal Mode (SPEEDCTRL = 1)[4] | | | 3 | ns |
| | High-Speed (SPEEDCTRL = 0)[4] | | | 8 | |
| $C_{OUT}$ | Load capacitance | 10 | | 30 | pF |
| $L_{OUT}$ | Line inductance (except vdds_mmc1) | | | 16 | nH |
| **3.0-V Mode** | | | | | |
| $V_{IH}$ | High-level input voltage | 0.625 * vdds_mmc1 | | vdds_mmc1 + 0.3 | V |
| $V_{IL}$ | Low-level input voltage | −0.3 | | 0.25 * vdds_mmc1 | V |
| $V_{OH}$ | High-level output voltage with 100-μA sink current $I_{OH}$ | 0.75 * vdds_mmc1 | | | V |
| $V_{OL}$ | Low-level output voltage with 100-μA source current at vdds_mmc1 minimum | | | 0.125 * vdds_mmc1 | V |
| $V_{HYS}$ [1] | Hysteresis voltage at an input | 0.05 | | | V |

## Table 3-5. DC Electrical Characteristics (continued)

| PARAMETER | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{TIN}$[2] | Input transition time ($t_{RIN}$ or $t_{FIN}$ evaluated between 10% and 90% at PAD) | Normal Mode (SPEEDCTRL = 1)[4] | | | 3 | ns |
| | | High-Speed (SPEEDCTRL = 0)[4] | | | 8 | |
| $C_{OUT}$ | Load capacitance | | 10 | | 30 | pF |
| $L_{OUT}$ | Line inductance (except vdds_mmc1) | | | | 16 | nH |
| **GPIO Mode (CBP Balls[19]: P27 / P26 / R25)** | | | | | | |
| **1.8-V Mode** | | | | | | |
| $V_{IH}$ | High-level input voltage | | 0.70 * vdds_x | | vdds_x + 0.3 | V |
| $V_{IL}$ | Low-level input voltage | | −0.3 | | 0.20 * vdds_x | V |
| $V_{OH}$ | High-level output voltage with 20-µA sink current $I_{OH}$ | | 0.8 * vdds_x | | vdds_x + 0.3 | V |
| $V_{OL}$ | Low-level output voltage with 1-mA source current at vdds_x minimum | | −0.3 | | 0.4 | V |
| $V_{HYS}$[1] | Hysteresis voltage at an input | | 0.1 | | | V |
| $t_{TIN}$[2] | Input transition time ($t_{RIN}$ or $t_{FIN}$ evaluated between 10% and 90% at PAD) | Normal Mode (SPEEDCTRL = 1)[4] | | | 35 | ns |
| $C_{IN}$ | Input capacitance | | | | 2.5 | pF |
| $C_{OUT}$ | Load capacitance | | | | 30 | pF |
| $L_{OUT}$ | Line inductance (except vdds_x) | | | | 16 | nH |
| **3.0-V Mode** | | | | | | |
| $V_{IH}$ | High-level input voltage | | 0.70 * vdds_x | | vdds_x + 0.3 | V |
| $V_{IL}$ | Low-level input voltage | | −0.3 | | 0.20 * vdds_x | V |
| $V_{OH}$ | High-level output voltage with 20-µA sink current $I_{OH}$ | | 0.7 * vdds_x | | vdds_x + 0.3 | V |
| $V_{OL}$ | Low-level output voltage with 1-mA source current at vdds_sim minimum | | −0.3 | | 0.4 | V |
| $V_{HYS}$[1] | Hysteresis voltage at an input | | 0.05 | | | V |
| $t_{TIN}$[2] | Input transition time ($t_{RIN}$ or $t_{FIN}$ evaluated between 10% and 90% at PAD) | Normal Mode (SPEEDCTRL = 1)[4] | | | 35 | ns |
| $C_{IN}$ | Input capacitance | | | | 2.5 | pF |
| $C_{OUT}$ | Load capacitance | | | | 30 | pF |
| $L_{OUT}$ | Line inductance (except vdds_x) | | | | 16 | nH |
| **I2C Mode (CBP Balls[19]: K21 / J21 / AF15 / AE15 / AF14 / AG14 / AD26 / AE26) [6]** | | | | | | |
| **Standard Mode** | | | | | | |
| $V_{IH}$ | High-level input voltage | | 0.7 * vdds | | vdds + 0.5 | V |
| $V_{IL}$ | Low-level input voltage | | −0.5 | | 0.3 * vdds | V |
| $V_{HYS}$[1] | Hysteresis voltage at an input | | 0.15 | | | V |
| $V_{OL}$ | Low-level output voltage open-drain at 3-mA sink current | | NA[18] | | NA[18] | V |
| $I_I$ | Input current at each I/O pin with an input voltage between 0.1 * vdds to 0.9 * vdds | | −10 | | 10 | µA |
| $C_I$ | Capacitance for each I/O pin | | | | 10 | pF |
| $t_{FOUT}$[5] | Output fall time from $V_{IHmin}$ to $V_{ILmax}$ with a bus capacitance $C_B$ from 10 pF to 400 pF | | | | 250 | ns |
| $t_{ROUT}$[5] | Output rise time with a capacitive load from 10 pF to 150 pF with internal pullup | | 20 + 0.1$C_B$ | | 250 | ns |
| **Fast Mode** | | | | | | |
| $V_{IH}$ | High-level input voltage | | 0.7 * vdds | | vdds + 0.5 | V |
| $V_{IL}$ | Low-level input voltage | | −0.5 | | 0.3 * vdds | V |

## Table 3-5. DC Electrical Characteristics (continued)

| PARAMETER | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{HYS}$ [1] | Hysteresis voltage at an input | 0.15 | | | V |
| $V_{OL}$ | Low-level output voltage open-drain at 3-mA sink current | 0 | | 0.2 * vdds | V |
| $I_I$ | Input current at each I/O pin with an input voltage between 0.1 * vdds to 0.9 * vdds | −10 | | 10 | µA |
| $C_I$ | Capacitance for each I/O pin | | | 10 | pF |
| $t_{FOUT}$[5] | Output fall time from $V_{IHmin}$ to $V_{ILmax}$ with a bus capacitance $C_B$ from 10 pF to 400 pF | $20 + 0.1C_B$ | | 250 | ns |
| $t_{ROUT}$[5] | Output rise time with a capacitive load from 10 pF to 150 pF with internal pullup | $20 + 0.1C_B$ | | 250 | ns |
| **High-Speed Mode** | | | | | |
| $V_{IH}$ | High-level input voltage | 0.7 * vdds | | vdds + 0.5 | V |
| $V_{IL}$ | Low-level input voltage | −0.5 | | 0.3 * vdds | V |
| $V_{HYS}$ [1] | Hysteresis voltage at an input | 0.15 | | | V |
| $V_{OL}$ | Low-level output voltage open-drain at 3-mA sink current | 0 | | 0.2 * vdds | V |
| $I_I$ | Input current at each I/O pin with an input voltage between 0.1 * vdds to 0.9 * vdds | −10 | | 10 | µA |
| $C_I$ | Capacitance for each I/O pin | | | 10 | pF |
| $t_{FOUT}$[5][6] | Output fall time with a capacitive load from 10 pF to 100 pF at 3-mA sink current | 10 | | 40 | ns |
| | Output fall time with a capacitive load of 400 pF at 3-mA sink current | 20 | | 80 | ns |
| $t_{ROUT}$[5] | Output rise time with a capacitive load from 10 pF to 80 pF with internal pullup | 10 | | 40 | ns |
| **Standard LVCMOS Mode** | | | | | |
| $V_{IH}$ | High-level input voltage | 0.7 * vdds | | vdds | V |
| $V_{IL}$ | Low-level input voltage | −0.5 | | 0.3 * vdds | V |
| $V_{OH}$ | High-level output voltage at 4-mA sink current | vdds − 0.45 | | | V |
| $V_{OL}$ | Low-level output voltage at 4-mA sink current | | | 0.45 | V |
| $C_{IN}$ | Input capacitance | | | 1.15 | pF |
| $t_{TIN}$ [2] | Input transition time ($t_{RIN}$ or $t_{FIN}$ evaluated between 10% and 90% at PAD) | | | 10 | ns |
| $t_{TOUT}$ | Output transition time at 40-pF load ($t_{ROUT}$ or $t_{FOUT}$ evaluated between 10% and 90% at PAD) | | | 10 | ns |
| **MIPI D-PHY Interface** | | | | | |
| **MIPI D-PHY Interface - GPI Mode (CBP Balls[19]: AG19 / AH19 / AG18 / AH18 / K28 / L28 / K27 / AG17 / AH17)** | | | | | |
| $V_{IH}$[7] | High-level input voltage | 0.65 * vdds_x[14] | | vdds_x + 0.3[14] | V |
| $V_{IL}$[8] | Low-level input voltage | −0.3 | | 0.35 * vdds_x[14] | V |
| $V_{HYS}$ [1] | Hysteresis voltage at an input | 0.15 | | | V |
| $C_{IN}$ | Input capacitance | | | 1.3 | pF |
| $t_{TIN}$ [2] | Input transition time ($t_{RIN}$ or $t_{FIN}$ evaluated between 10% and 90% at PAD) | | | 10 | ns |
| **Other Balls** | | | | | |
| **Common to "Other Balls"** | | | | | |
| $V_{IH}$ | High-level input voltage | 0.65 * vdds | | vdds + 0.3 | V |
| $V_{IL}$ | Low-level input voltage | −0.3 | | 0.35 * vdds | V |
| $V_{HYS}$ [1] | Hysteresis voltage at an input | 0.15 | | | V |
| $V_{OH}$ | High-level output voltage, driver enabled, pullup or pulldown disabled | $I_{OH} = -X$[17] mA | vdds − 0.45 | | | V |
| $V_{OL}$ | Low-level output voltage, driver enabled, pullup or pulldown disabled | $I_{OL} = X$[17] mA | | | 0.45 | V |
| **Differences Between "Other Balls"** | | | | | |

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## Table 3-5. DC Electrical Characteristics (continued)

| PARAMETER | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| **Input Capacitance and Input Transition Time** | | | | | | |
| **sys_xtalin pin (CBP Ball[19]: AE17)** | | | | | | |
| $C_{IN}$ | Input capacitance | | 1.00 | 1.15 | 1.35 | pF |
| $t_{TIN}$[2] | Input transition time (rise time, $t_{RIN}$ or fall time, $t_{FIN}$ evaluated between 10% and 90% at PAD) | | | | 10 | ns |
| **JTAG interface (CBP Balls[19]: AA17 / AA13 / AA12 / AA18 / AA20 / AA19 / AA11 / AA10)** | | | | | | |
| $C_{IN}$ | Input capacitance | | | | 2.20 | pF |
| $t_{TIN}$[2] | Input transition time (rise time, $t_{RIN}$ or fall time, $t_{FIN}$ evaluated between 10% and 90% at PAD) | | | | 10 | ns |
| **Otherwise** | | | | | | |
| $C_{IN}$ | Input capacitance | | | | 1.15 | pF |
| $t_{TIN}$[2] | Input transition time (rise time, $t_{RIN}$ or fall time, $t_{FIN}$ evaluated between 10% and 90% at PAD) | | | | 10 | ns |
| **Output Capacitance Load and Output Transition Time** | | | | | | |
| **sys_32k, sys_clkreq, sys_off_mode, sys_clkout1, sys_nirq, uart3_cts_rctx, uart3_rts_sd, uart3_rx_irrx, uart3_tx_irtx, hdq_sio (CBP Balls[19]: R27 / AE25 / AF25 / AF22 / AG25 / AF26 / H18 / H19 / H20 / H21 / J25)** | | | | | | |
| $t_{TOUT}$ | Output transition time (rise time, $t_{ROUT}$ or fall time, $t_{FOUT}$ evaluated between 10% and 90% at PAD) | DS[1:0] = 00[3] | 1[15] | | 15[16] | ns |
| $C_{TOUT}$ | Output load | | 4 | | 60 | pF |
| $t_{TOUT}$ | Output transition time (rise time, $t_{ROUT}$ or fall time, $t_{FOUT}$ evaluated between 10% and 90% at PAD) | DS[1:0] = 10[3] | 0.4[15] | | 5[16] | ns |
| $C_{TOUT}$ | Output load | | 2 | | 21 | pF |
| $t_{TOUT}$ | Output transition time (rise time, $t_{ROUT}$ or fall time, $t_{FOUT}$ evaluated between 10% and 90% at PAD) | DS[1:0] = 01[3] | 0.6[15] | | 7[16] | ns |
| $C_{TOUT}$ | Output load | | 7 | | 33 | pF |
| **CAM, HSUSB0, MMC2, UART1, UART2, McBSP, McSPI, ETK Interfaces, sys_clkout2 (CBP Ball[19]: AE22)** | | | | | | |
| $t_{TOUT}$ | Output transition time (rise time, $t_{ROUT}$ or fall time, $t_{FOUT}$ evaluated between 10% and 90% at PAD) | | 1.5 | | 5 | ns |
| $C_{TOUT}$ | Output load | | 2 | | 22 | pF |
| **Otherwise** | | | | | | |
| $t_{TOUT}$ | Output transition time (rise time, $t_{ROUT}$ or fall time, $t_{FOUT}$ evaluated between 10% and 90% at PAD) | | 0.6 | | 2.4[17] | ns |
| $C_{TOUT}$ | Output load | | 2 | | 22 | pF |
| **Hysteresis** | | | | | | |
| **sys_xtalin pin (CBP Ball[19]: AE17)** | | | | | | |
| $V_{HYS}$ [1] | Hysteresis voltage at an input | | 0.25 | | | V |
| **hsusb0_clk (CBP Ball[19]: T28)** | | | | | | |
| $V_{HYS}$ [1] | Hysteresis voltage at an input | | 0.07 | | | V |
| **Otherwise** | | | | | | |
| $V_{HYS}$[1] | Hysteresis voltage at an input | | 0.15 | | | V |

(1) $V_{hys}$ is the magnitude of the difference between the positive-going threshold voltage $V_{T+}$ and the negative-going threshold voltage $V_{T-}$. Some receivers, but not all, are designed for hysteresis. $V_{hys}$ applies only to those that are.

(2) The $t_{IN}$ ($t_{RIN}$ and $t_{FIN}$ also) value is the recommended condition. The $t_{IN}$ ($t_{RIN}$ and $t_{FIN}$ also) mismatch causes additional delay time inside the device then leads to ac timing invalidation in this DM.

The $t_{IN}$ ($t_{RIN}$ and $t_{FIN}$ also) mismatch does not necessarily mean functional failure. This global value may be overridden on a per interface basis if another value is explicitly defined for that interface in the Timing Requirements and Switching Characteristics chapter of the data manual.

(3) For a full description of the DS0 load compensation register configuration, see the description of the CONTROL_PROG_IO1 configuration registers in System Control Module / Programming Model / Feature Settings / SDRC I/O Drive Strength Selection section of the *AM/DM37x Multimedia Device Technical Reference Manual* (literature number SPRUGN4).

(4) For a full description of the SPEEDCTRL speed register configuration, see the description of the CONTROL_PROG_IO1 configuration registers in System Control Module / Programming Model / Feature Settings section of the *AM/DM37x Multimedia Device Technical Reference Manual* (literature number SPRUGN4).

(5) Rise and fall times are specified for (0.3 * vdds) to (0.7 * vdds).

(6) For capacitive load from 100 pF to 400 pF, fall time should be linearly interpolated:
$t_{Fmin} = (1 + (Load – 100\ pF) / 300\ pF) * 10\ ns$
$t_{Fmax} = (1 + (Load – 100\ pF) / 300\ pF) * 40\ ns$

(7) $V_{IH}$ is the voltage at which the receiver is required to detect a high state in the input signal.

(8) $V_{IL}$ is the voltage at which the receiver is required to detect a low state in the input signal. $V_{IL}$ is larger than the maximum single-ended line voltage during HS transmission. Therefore, both LP receivers will detect low during HS signaling.

(9) This value includes a ground difference of 50 mV between the transmitter and the receiver, the status common-mode level tolerance and variations below 450 MHz.

(10) Common mode is defined as the average voltage level of DX and DY: $V_{CM} = (V_{(DX)} + V_{(DY)})/2$. Common mode ripple may be due to rise-fall time and transmission line impairments in the PCB.

(11) Value when driving into differential load impedance anywhere in the range 80 to 125 Ω.

(12) ULPM stands for Ultra Low Power Mode.

(13) UI = 1 / (2 * fh), where fh is the fundamental frequency of HS data transmission. For example, for 800 Mbps fh is 400 MHz.

(14) vdda_x can be vdda_csiphy1 or vdda_csiphy2 depending on the interface used.

(15) At minimum load.

(16) At maximum load. Caution: This creates EMI parasitics up to 1.2 ns.

(17) For more information about IOH / IOL values, see one of the tables in the Ball Characteristics section, column "BUFFER DRIVE STRENGTH (mA) ".

(18) No $V_{OL}$ specifications are applicable in Standard mode.

(19) For associated CBC and CUS balls, please refer to the Section 2.4, *Multiplexing Characteristics* table.

## 3.4 External Capacitors

To improve module performance, decoupling capacitors are required to suppress the switching noise generated by high frequency and to stabilize the supply voltage. A decoupling capacitor is most effective when it is close to the device, because this minimizes the inductance of the circuit board wiring and interconnects.

### 3.4.1 Voltage Decoupling Capacitors

Table 3-6 summarizes the Core voltage decoupling characteristics.

#### 3.4.1.1 Core Voltage Decoupling Capacitors

To improve module performance, decoupling capacitors are required to suppress the switching noise generated by high frequency and to stabilize the supply voltage. A decoupling capacitor is most effective when it is close to the device, because this minimizes the inductance of the circuit board wiring and interconnects.

**Table 3-6. Core Voltage Decoupling Characteristics**

| PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|
| $C_{vdd\_core}$ [1] | 0.6 | 1.2 | 1.8 | µF |
| $C_{vdd\_mpu\_iva}$ [2] | | See [2] | | µF |

(1) The typical value corresponds to 2 capacitors of 470 nF, plus 3 capacitors of 100 nF. Except for the decoupling capacitance values, the PCB rules of the PCB Design Requirements for VDD_MPU_IVA Power Distribution Network for TI OMAP3630, AM37xx, and DM37xx Microprocessors (SPRABJ7) application note can be used.

(2) For more information regarding the vdd_mpu_iva decoupling capacitance recommendations, see the PCB Design Requirements for VDD_MPU_IVA Power Distribution Network for TI OMAP3630, AM37xx, and DM37xx Microprocessors (SPRABJ7) application note.

#### 3.4.1.2 IO and Analog Voltage Decoupling Capacitors

Table 3-7 summarizes the power supply decoupling capacitor characteristics.

**Table 3-7. Power Supply Decoupling Capacitor Characteristics**

| PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|
| $C_{vdds}$ [1][2] | 200 | 400 | 600 | nF |
| $C_{vdds\_mem}$ [1][3] | 350 | 700 | 1050 | nF |
| $C_{vdds\_mmc1}$ [4] | 50 | 100 | 150 | nF |
| $C_{vdds\_x}$ [4] | 50 | 100 | 150 | nF |
| $C_{vdda\_dplls\_dll}$ [4] | 50 | 100 | 150 | nF |
| $C_{vdda\_dpll\_per}$ [4] | 50 | 100 | 150 | nF |
| $C_{vdds\_sram}$ [4] | 110 | 220 | 330 | nF |
| $C_{vdda\_wkup\_bg\_bb}$ [4] | 240 | 470 | 700 | nF |
| $C_{vdda\_dac}$ [4] | 50 | 100 | 150 | nF |

(1) In power plan configuration.

(2) The typical value corresponds to 4 capacitors of 100 nF.

(3) The typical value corresponds to 7 capacitors of 100 nF.

(4) In power rail configuration.

### 3.4.2 Output Capacitors

The capacitors at the outputs are required to stabilize the internal LDO supply voltages. The capacitors must be placed as close as possible to the balls.

Table 3-8 summarizes the power supply decoupling characteristics.

**Table 3-8. Output Capacitor Characteristics**

| PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|
| $C_{cap\_vdd\_sram\_mpu\_iva}$ | 0.7 | 1 | 1.3 | µF |
| $C_{cap\_vdd\_sram\_core}$ | 0.7 | 1 | 1.3 | µF |
| $C_{cap\_vddu\_wkup\_logic}$ | 0.7 | 1 | 1.3 | µF |
| $C_{cap\_vddu\_array}$ | 0.7 | 1 | 1.3 | µF |
| $C_{cap\_vdd\_bb\_mpu\_iva}$ | 0.7 | 1 | 1.3 | µF |

Figure 3-1 illustrates an example of the external capacitors.
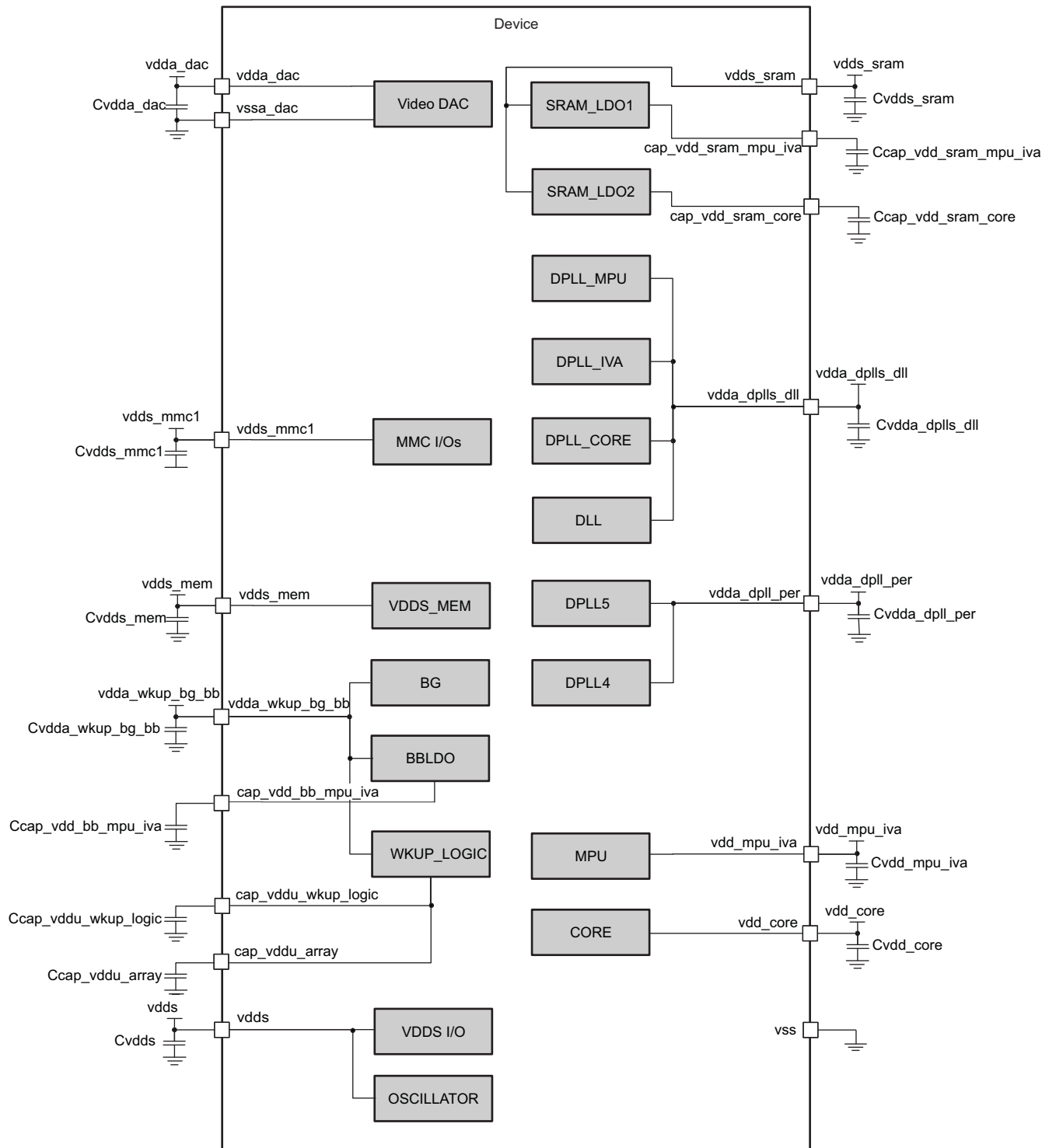


**Figure 3-1. External Capacitors**

**NOTE**

- Decoupling capacitors must be placed as closed as possible of the power ball. Choose the ground located closest to the power pin for each decoupling capacitor. In case of interconnecting powers, first insert the decoupling capacitor and then interconnect the powers.
- The decoupling capacitor value depends on the board characteristics.

## 3.5 Power-Up and Power-Down Sequences

This section provides the timing requirements for the device hardware signals.

**NOTE**

- If the MMC dual voltages interfaces are used with 1.8-V or 3.0-V, then the power-up and power-down sequences specified in the Figure 3-2 and Figure 3-3 must be followed carefully to avoid any significant current consumption.
- If the MMC dual voltages interfaces are used with 1.8-V only (3.0-V is never used), then vdds_mmc1, vdds_x may be connected to the main power supply vdds so that they ramp up together before vdd_core.

### 3.5.1 Power-Up Sequence

**NOTE**

For more information, see the Power, Reset, and Clock Management / PRCM Functional Description / PRCM Reset Manager Functional Description / Reset Sequences of the *AM/DM37x Multimedia Device Technical Reference Manual* (literature number SPRUGN4).

Figure 3-2 shows the power-up sequence.
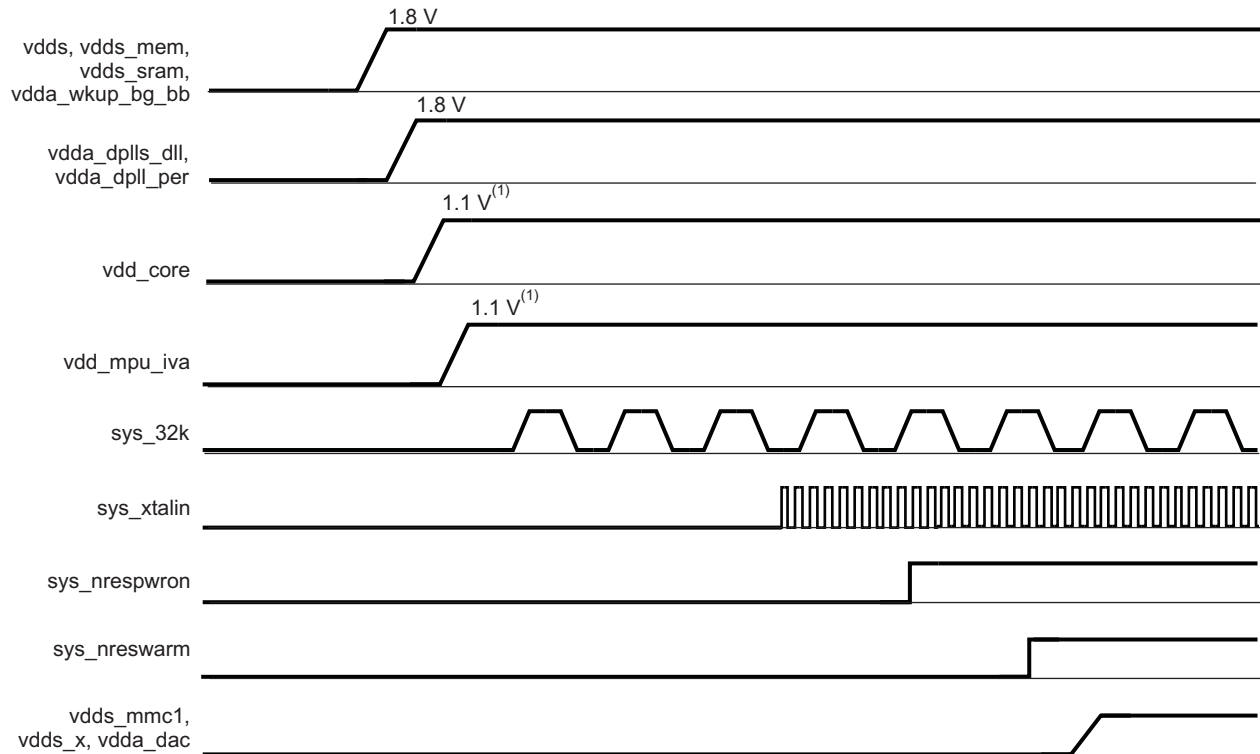
(1)   1.2 V supported.

(2)   If an external square clock is provided, it could be started after sys_nrespwron release, provided it is clean, i.e. no glitch, stable frequency and duty cycle.

(3)   sys_32k can be turned on any time between the vdds ramp-up and the sys_nrespwron release.

**Figure 3-2. Power-Up Sequence**

### 3.5.2   Power-Down Sequence

The following steps give two examples of power-down sequence supported by the DM37x device.

1.   Put the DM37x device under reset (sys_nrespwron)

2.   Stop all signals driven to its balls (sys_32k, sys_xtalin)

3.   Either:

   (a)   Shutdown all power domains at once. This sequence is described in black color in Figure 3-3.

   (b)   Or, if the shutdown is sequenced, you must follow these steps (described in dash style blue color in Figure 3-3):

   –   Turn off all complex IO domains (vdds_mmc1, vdds_x)

   –   Turn off all the core and MPU domains (vdd_core, vdd_mpu_iva)

   –   Turn off all DPLL domains (vdda_dplls_dll, vdda_dpll_per)

   –   Turn off all sram LDOs (vdds_sram)

   –   Turn off all reference domains (vdda_wkup_bg_bb)

   –   Turn off all standard IO domains (vdds, vdds_mem)

Figure 3-3 shows both power-down sequences: one of them is described in black color, and the other one in dash style blue.
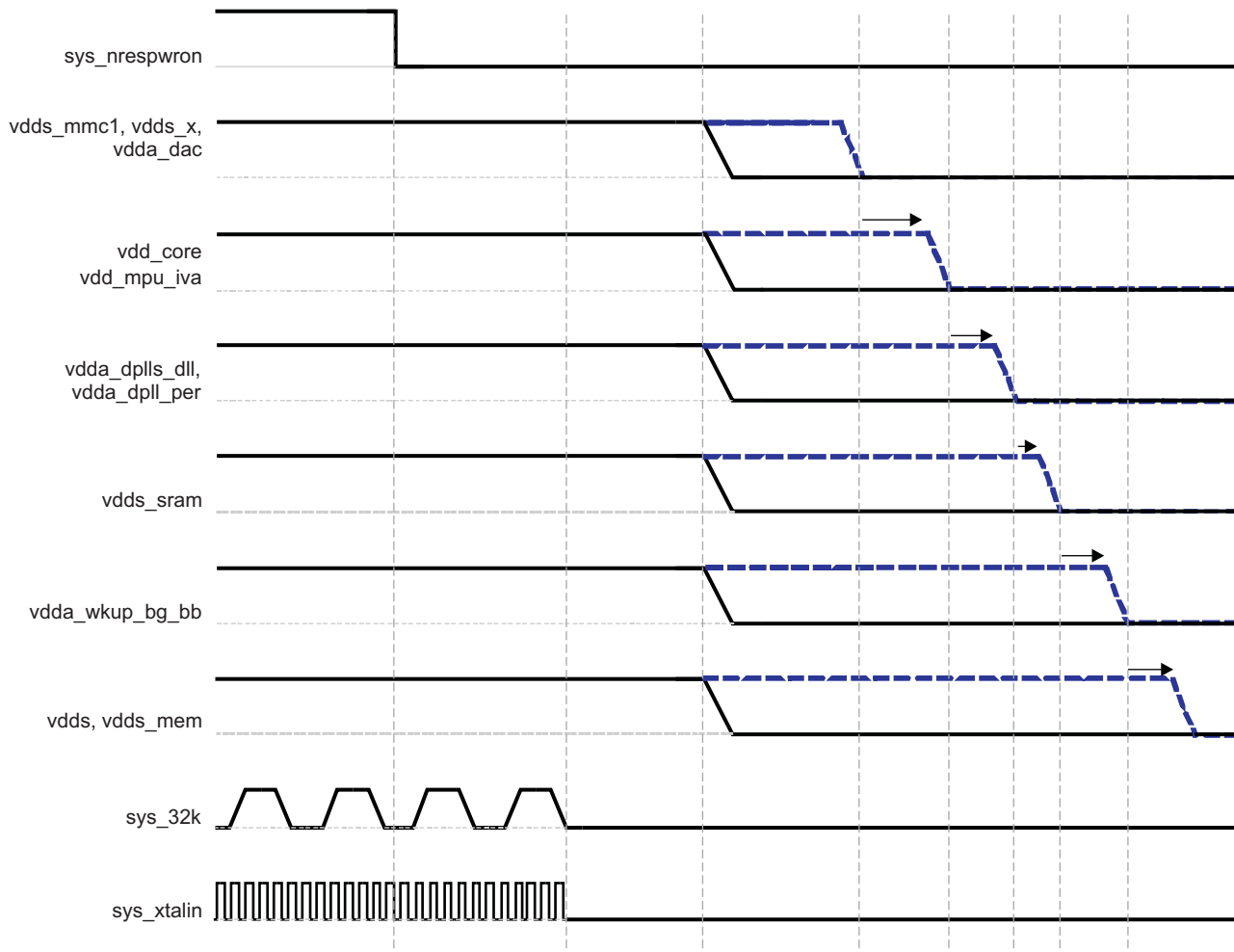
A.  sys_32k can be turned off any time between the sys_nrespwron assertion and the vdds shut down.

**Figure 3-3. Power-Down Sequence**

**Alternate power-down sequence**:

*   vdd_mpu_iva shuts down before vdd_core.
*   vdda_sram, vdda_wkup_bg_bb, vdds and vdds_mem shut down simultaneously.
*   vdda_dplls_dll and vdda_dpll_per shut down anytime between all complex IO domains shut down and vdda_sram shuts down.

# 4 Clock Specifications

**NOTE**

For more information, see the Power, Reset, and Clock Management / PRCM Environment / External Clock Signal and Power, Reset and Clock Management / PRCM Functional Description / PRCM Clock Manager Functional Description sections of the *AM/DM37x Multimedia Device Technical Reference Manual* (SPRUGN4).

Figure 4-1 shows external input clock sources and output clocks.
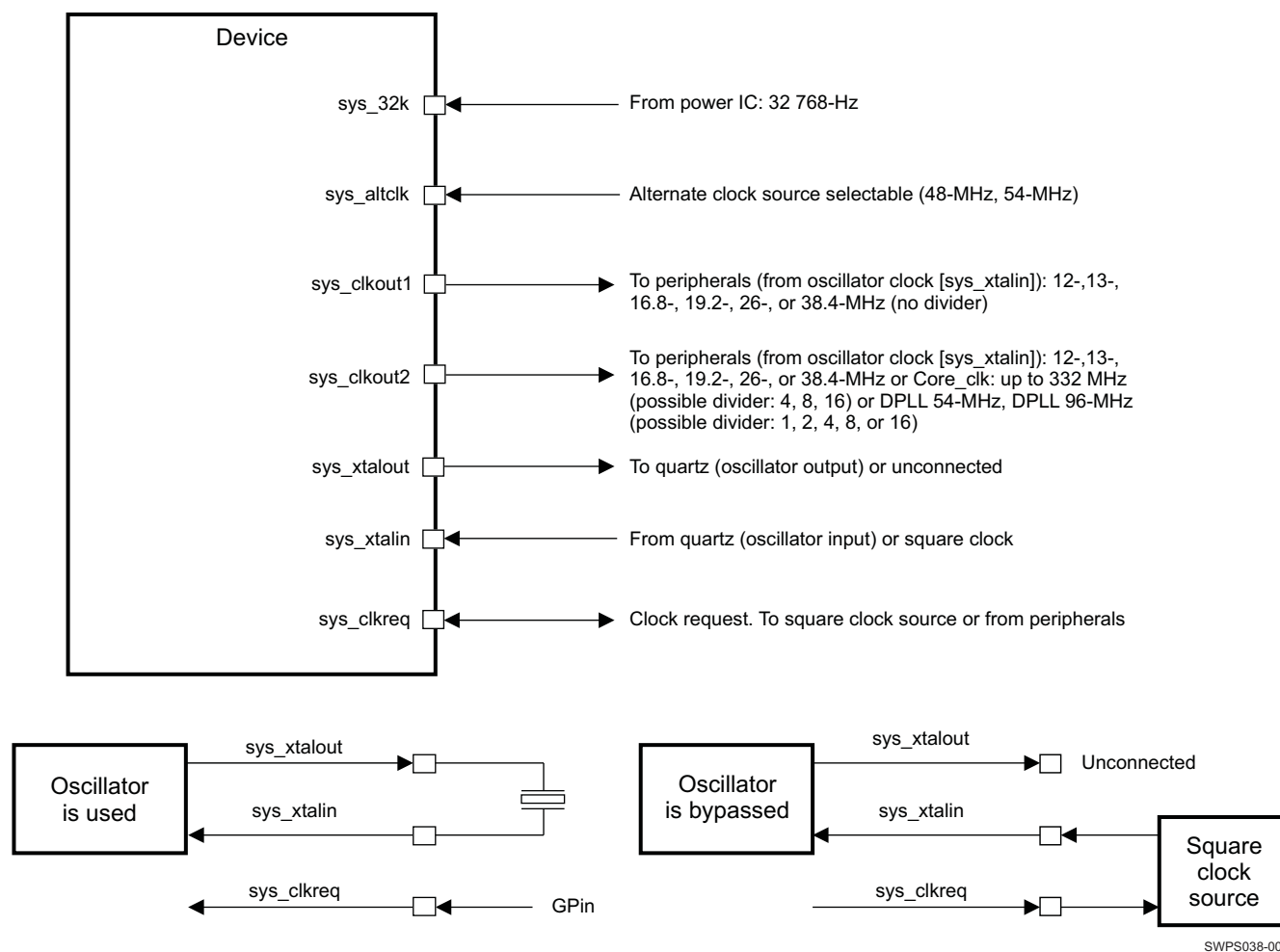


**Figure 4-1. Clock Interface**

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The device operation requires the following three input clocks:

- The sys_32k 32-kHz clock is used for low frequency operation. It supplies the wake-up domain for operation in lowest power mode (off mode). This clock is provided through the sys_32k pin.
- The sys_altclk system alternative clock can be used (through the sys_altclk pin) to provide alternative 48 MHz or 54 MHz.
- The sys_xtalin / sys_xtalout system input clock (12, 13, 16.8, 19.2, 26, or 38.4 MHz) is used to generate the main source clock of the device. It supplies the DPLLs as well as several other modules. The system input clock can be connected to either:
  - A crystal oscillator clock managed by sys_xtalin and sys_xtalout. In this case, the sys_clkreq is used as an input (GPIN).
  - A CMOS digital clock through the sys_xtalin pin. In this case, the sys_clkreq is used as an output to request the external system clock.

The device outputs externally two clocks:

- sys_clkout1 can output the oscillator clock (12, 13, 16.8, 19.2, 26, or 38.4 MHz) at any time. It can be controlled by software or externally using sys_clkreq control. When the device is in the off state, the sys_clkreq can be asserted to enable the oscillator and activate the sys_clkout1 without waking up the device. The off state polarity of sys_clkout1 is programmable.
- sys_clkout2 can output the oscillator clock (12, 13, 16.8, 19.2, 26, or 38.4 MHz), core_clk (core DPLL output), 96 MHz or 54 MHz. It can be divided by 2, 4, 8, or 16 and its off state polarity is programmable. This output is active only when the core power domain is active.

## 4.1 Input Clock Specifications

### 4.1.1 Input Clock Requirements

Table 4-1 illustrates the requirements to supply a clock to the device.

**Table 4-1. Input Clock Requirements [4]**

| PAD | CLOCK FREQUENCY | | STABILITY | DUTY CYCLE | JITTER | TRANSITION |
|---|---|---|---|---|---|---|
| sys_32k | 32.768 kHz | | +/- 200 ppm | - | - | <10 ns |
| sys_xtalout sys_xtalin | 12, 13, 16.8, or 19.2 MHz | Crystal | ±50 ppm (±5 ppm)[1] | - | - | - |
| | 12, 13, 16.8, 19.2, 26, or 38.4 MHz | Square | ±50 ppm (±5 ppm)[1] | 45% to 55% | X%[2] * tc(xtalin)[3] - 200ps | 10 ns |
| sys_altclk | 48 or 54 MHz | | +/-50 ppm | 49% to 51% | <1% | 10 ns |

(1) ± 50 ppm is the clock frequency stability/accuracy and ± 5 ppm takes into account the aging effects.

(2) Depending on the internal system clock divider configuration (PRCM.PRM_CLKSRC_CTRL[7:6], SYSCLKDIV bit field), the sys_xtalin input clock can be divided by 2 to provide the standard system clock (SYS_CLK) frequencies.

For more information, see the Power, Reset, and Clock Management chapter of the *AM/DM37x Multimedia Device Technical Reference Manual* (SPRUGN4). In X%, X represents then the internal system clock divider with following possible values: X = 1 or 2.

(3) tc(xtalin) is the sys_xtalin cycle time of the clock coming to sys_xtalin ball.

(4) In this table, the transition times are calculated for 10%-90% of VDDS. For more information on the corresponding VDDS power supply name, please see the Ball Characteristics table corresponding to your package. The POWER column defines the VDDS power supply for each ball.

### 4.1.2 sys_xtalin / sys_xtalout External Crystal

An external crystal is connected to the device pins. Figure 4-2 describes the crystal implementation.
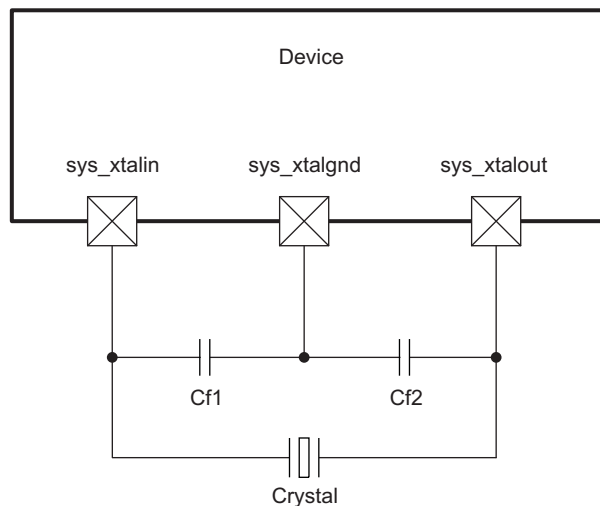


**Figure 4-2. Crystal Implementation**

1. When the crystal oscillator is in bypass mode (crystal implementation is unused), the sys_xtalgnd ball is not connected.

The crystal must be in the fundamental mode of operation and parallel resonant. Table 4-2 summarizes the required electrical constraints.

**Table 4-2. Crystal Electrical Characteristics[1]**

| NAME | DESCRIPTION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $f_p$ | Parallel resonance crystal frequency[1] | | 12, 13, 16.8, or 19.2 | | MHz |
| $C_{f1}$ | $C_{f1}$ load capacitance for crystal parallel resonance with $C_{f1} = C_{f2}$ | 12 | | 24 | pF |
| $C_{f2}$ | $C_{f2}$ load capacitance for crystal parallel resonance with $C_{f1} = C_{f2}$ | 12 | | 24 | pF |
| ESR($C_{f1}$,$C_{f2}$)[2] | Frequency 12 MHz , Negative resistor at nominal 500 Ω, Negative resistor at worst case 300 Ω | | | 100 | Ω |
| | Frequency 13 MHz, Negative resistor at nominal 400 Ω, Negative resistor at worst case 240 Ω | | | 80 | Ω |
| | Frequency 16.8 MHz and 19.2 MHz, Negative resistor at nominal 300 Ω, Negative resistor at worst case 180 Ω | | | 60 | Ω |
| $C_o$ | Crystal shunt capacitance | | | 4.5 | pF |
| DL | Crystal drive level | | | 0.5 | mW |

(1) Measured with the load capacitance specified by the crystal manufacturer. This load is defined by the foot capacitances tied in series. If $C_L = 20$ pF, then both foot capacitors will be $C_{f1} = C_{f2} = 40$ pF. Parasitic capacitance from package and board must also be taken in account.

(2) The crystal motional resistance $R_m$ is related to the equivalent series resistance (ESR) by the following formula:
$ESR = R_m * (1 + (C_O * C_{f1} * C_{f2} / (C_{f1} + C_{f2})))^2$.

When selecting a crystal, the system design must take into account the temperature and aging characteristics of a crystal versus the user environment and expected lifetime of the system.

Table 4-3 details the switching characteristics of the oscillator and the requirements of the input clock.

**Table 4-3. Oscillator Switching Characteristics—Crystal Mode**

| NAME | DESCRIPTION | MIN | TYP | MAX | UNIT |
|------|-------------|-----|-----|-----|------|
| $f_p$ | Oscillation frequency | | 12, 13, 16.8, or 19.2 | | MHz |
| $t_{sX}$ | Start-up time[1] [2] | 3 | | | ms |

(1)  Start-up time is defined as the time the oscillator takes to gain sys_xtalin amplitude enough to have 45% to 55% duty cycle at the core input from the time power down (PWRDN) is released. Start-up time is a strong function of crystal parameters. At power-on reset, the time is adjustable using the pin itself. The reset must be released when the oscillator or clock source is stable. To switch from bypass mode to crystal or from crystal mode to bypass mode, there is a waiting time about 100 μs; however, if the chip comes from bypass mode to crystal mode then the crystal will start-up after time mentioned in the $t_{sX}$ parameter.

(2)  Before the processor boots up and the oscillator is set to bypass mode, there is a waiting time when the internal oscillator is in application mode and receives a square wave. The switching time in this case is about 100 μs.

### 4.1.3  sys_xtalin Squarer Input Clock

Table 4-4 summarizes the base oscillator electrical characteristics.

**Table 4-4. Oscillator Electrical Characteristics—Bypass Mode**

| NAME | DESCRIPTION | MIN | TYP | MAX | UNIT |
|------|-------------|-----|-----|-----|------|
| f | Frequency | | 12, 13, 16.8, 19.2, 26, or 38.4 | | MHz |
| $C_i$ | Input Capacitance | 1.00 | 1.15 | 1.35 | pF |
| $R_i$ | Input Resistance | 160 | 216 | 280 | Ω |
| $t_{sX}$ | Start-up time[1] | | See[2] | | ms |

(1)  To switch from bypass mode to crystal mode or from crystal mode to bypass mode, there is a waiting time about 100 μs; however, if the chip comes from bypass mode to crystal mode then the crystal will start-up after time mentioned in Table 4-3, $t_{sX}$ parameter above.

(2)  Before the processor boots up and the oscillator is set to bypass mode, there is a waiting time when the internal oscillator is in application mode and receives a square wave. The switching time in this case is about 100 μs.

Table 4-5 details the squarer input clock timing requirements.

**Table 4-5. sys_xtalin Squarer Input Clock Timing Requirements—Bypass Mode [5]**

| NAME | DESCRIPTION | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| OCS0 | $1 / t_{c(xtalin)}$ | Frequency, sys_xtalin | 12, 13, 16.8, 19.2, 26, or 38.4 | | | MHz |
| OCS1 | $t_{w(xtalin)}$ | Pulse duration, sys_xtalin low or high | $0.45 * t_{c(xtalin)}$ | | $0.55 * t_{c(xtalin)}$ | ns |
| | $t_{J(xtalin)}$ | Peak-to-peak jitter[1], sys_xtalin | | | X%[2] * tc(xtalin) [3] - 200 | ps |
| | $t_{R(xtalin)}$ | Rise time, sys_xtalin | | | 10 | ns |
| | $t_{F(xtalin)}$ | Fall time, sys_xtalin | | | 10 | ns |
| | $t_{J(xtalin)}$ | Frequency stability, sys_xtalin | | | +/-50 (+/-5ppm)[4] | ppm |

(1)
  – Peak-to-peak jitter is meant here as follows:
    – The maximum value is the difference between the longest measured clock period and the expected clock period
    – The minimum value is the difference between the shortest measured clock period and the expected clock period Maximum and minimum are obtained on a statistical population of 300 period samples and expressed relative to the expected clock period

(2) Depending on the internal system clock divider configuration (PRCM.PRM_CLKSRC_CTRL[7:6], SYSCLKDIV bit field), the sys_xtalin input clock can be divided by 2 to provide the standard system clock (SYS_CLK) frequencies. For more information, see the Power, Reset, and Clock Management chapter of the *AM/DM37x Multimedia Device Technical Reference Manual* (SPRUGN4). In X%, X represents then the internal system clock divider with following possible values: X = 1 or 2.

(3) tc(xtalin) is the sys_xtalin cycle time of the clock coming to sys_xtalin ball.

(4) ±50 ppm is the clock frequency stability/accuracy and ±5 ppm takes into account the aging effects.

(5) In this table, the transition times are calculated for 10%-90% of VDDS. For more information on the corresponding VDDS power supply name, please see the Ball Characteristics table corresponding to your package. The POWER column defines the VDDS power supply for each ball.



SWPS038-008
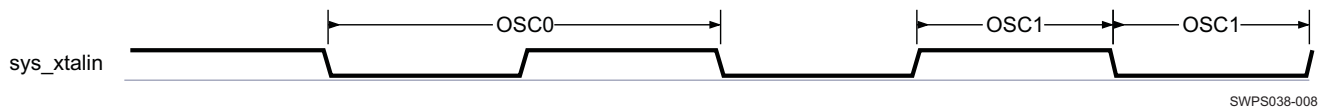
**Figure 4-3. sys_xtalin Squarer Input Clock**

### 4.1.4 sys_32k CMOS Input Clock

Table 4-6 summarizes the electrical characteristics of the sys_32k input clock.

**Table 4-6. sys_32k Input Clock Electrical Characteristics**

| NAME | DESCRIPTION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| f | Frequency, sys_32k | | 32.768 | | kHz |
| $C_i$ | Input capacitance | | | 1.6 | pF |
| $R_i$ | Input resistance | 3 | | $10^6$ | MΩ |

Table 4-7 details the input requirements of the sys_32k input clock.

**Table 4-7. sys_32k Input Clock Timing Requirements[1]**

| NAME | DESCRIPTION | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| CK0 | $1 / t_{c(32k)}$ | Frequency, sys_32k | | 32.768 | | kHz |
| | $t_{R(32k)}$ | Rise time, sys_32k | | | 10 | ns |
| | $t_{F(32k)}$ | Fall time, sys_32k | | | 10 | ns |
| | $t_{J(32k)}$ | Frequency stability, sys_32k | | | 200 | ppm |

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(1) In this table, the transition times are calculated for 10%-90% of VDDS. For more information on the corresponding VDDS power supply name, please see the Ball Characteristics table corresponding to your package. The POWER column defines the VDDS power supply for each ball.



SWPS038-009
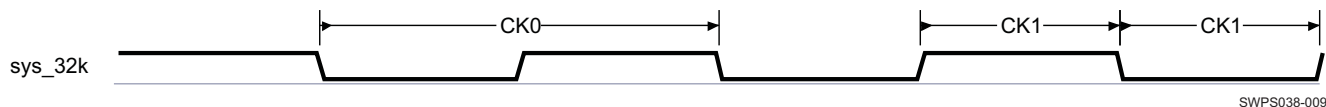
**Figure 4-4. sys_32k Input Clock**

### 4.1.5 sys_altclk CMOS Input Clock

Table 4-8 summarizes the electrical characteristics of the sys_altclk input clock.

**Table 4-8. sys_altclk Input Clock Electrical Characteristics**

| NAME | DESCRIPTION | MIN | TYP | MAX | UNIT |
|------|-------------|-----|-----|-----|------|
| f | Frequency, sys_altclk | | 48 or 54 | | MHz |
| Ci | Input capacitance | | | 1.6 | pF |
| Ri | Input resistance | 3 | | $10^6$ | MΩ |

Table 4-9 details the input requirements of the sys_altclk input clock.

**Table 4-9. sys_altclk Input Clock Timing Requirements[2]**

| NAME | | DESCRIPTION | MIN | TYP | MAX | UNIT |
|------|------|-------------|-----|-----|-----|------|
| ALT0 | $1 / t_{c(altclk)}$ | Frequency, sys_altclk | | 48 or 54 | | MHz |
| ALT1 | $t_{w(altclk)}$ | Pulse duration, sys_altclk low or high | $0.49 * t_{c(altclk)}$ | | $0.51 * t_{c(altclk)}$ | ns |
| | $t_{J(altclk)}$ | Peak-to-peak jitter[1], sys_altclk | -1% | | 1% | |
| | $t_{R(altclk)}$ | Rise time, sys_altclk | | | 10 | ns |
| | $t_{F(altclk)}$ | Fall time, sys_altclk | | | 10 | ns |
| | $t_{J(altclk)}$ | Frequency stability, sys_altclk | | | 50 | ppm |

(1) Peak-to-peak jitter is meant here as follows:
   – The maximum value is the difference between the longest measured clock period and the expected clock period
   – The minimum value is the difference between the shortest measured clock period and the expected clock period Maximum and minimum are obtained on a statistical population of 300 period samples and expressed relative to the expected clock period

(2) In this table, the transition times are calculated for 10%-90% of VDDS. For more information on the corresponding VDDS power supply name, please see the Ball Characteristics table corresponding to your package. The POWER column defines the VDDS power supply for each ball.



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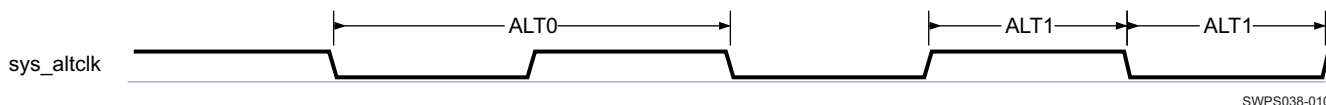
**Figure 4-5. sys_altclk Input Clock**

## 4.2 Output Clocks Specifications

### 4.2.1 sys_clkout1 Output Clock

Table 4-10 summarizes the sys_clkout1 ouput clock electrical characteristics.

**Table 4-10. sys_clkout1 Output Clock Electrical Characteristics**

| NAME | DESCRIPTION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| f | Frequency, sys_clkout1 | sys_xtalin / sys_xtalout clock frequency | | | MHz |
| SC[0:1] = 00[1] | | | | | |
| $C_L$ | Load capacitance (transmission line load + far end load) | 4 | | 60 | pF |
| $Z_T$ | Transmission line impedance | 30 | | 70 | Ω |
| $L_T$ | Transmission line length | 2 | | 20 | cm |
| SC[0:1] = 01[1] | | | | | |
| $C_L$ | Load capacitance (transmission line load + far end load) | 7 | | 33 | pF |
| $Z_T$ | Transmission line impedance | 30 | | 70 | Ω |
| $L_T$ | Transmission line length | 2 | | 8 | cm |
| SC[0:1] = 10[1] | | | | | |
| $C_L$ | Load capacitance (transmission line load + far end load) | 2 | | 21 | pF |
| $Z_T$ | Transmission line impedance | 30 | | 70 | Ω |
| $L_T$ | Transmission line length | 1 | | 6 | cm |

(1) The mode is configured by bits SC0 and SC1 of the IO cell. For more details, see the *AM/DM37x Multimedia Device Technical Reference Manual* (SPRUGN4).

Table 4-11 details the sys_clkout1 ouput clock switching characteristics.

**Table 4-11. sys_clkout1 Output Clock Switching Characteristics[6]**

| NAME | | DESCRIPTION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| CO0 | $1 / t_{c(CLKOUT1)}$ | Frequency, sys_clkout1 | sys_xtalin/sys_xtalout clock frequency | | | MHz |
| SC[0:1] = 00[1] | | | | | | |
| | $C_L$ | Load capacitance | 4 | | 60 | pF |
| | $t_J$ | Peak-to-peak jitter | | | X[5] + 693 | ps |
| | $t_{JC2C}$ | Cycle-to-cycle jitter | | | X[5] + 705 | ps |
| | $t_{W(CLKOUT1)}$ | Pulse duration, sys_clkout1 low or high | $0.45*t_{c(CLKOUT1)}$ | | $0.55*t_{c(CLKOUT1)}$ | |
| | $t_{R(CLKOUT1)}$ | Rise time, sys_clkout1 | 1[2] [4] | | 15[3] | ns |
| | $t_{F(CLKOUT1)}$ | Fall time, sys_clkout1 | 1[2] [4] | | 15[3] | ns |
| SC[0:1] = 01[1] | | | | | | |
| | $C_L$ | Load capacitance | 7 | | 33 | pF |
| | $t_J$ | Peak-to-peak jitter | | | X[5] + 543 | ps |
| | $t_{JC2C}$ | Cycle-to-cycle jitter | | | X[5] + 555 | ps |
| | $t_{W(CLKOUT1)}$ | Pulse duration, sys_clkout1 low or high | $0.45*t_{c(CLKOUT1)}$ | | $0.55*t_{c(CLKOUT1)}$ | |
| | $t_{R(CLKOUT1)}$ | Rise time, sys_clkout1 | 0.6[2] [4] | | 7[3] | ns |
| | $t_{F(CLKOUT1)}$ | Fall time, sys_clkout1 | 0.6[2] [4] | | 7[3] | ns |
| SC[0:1] = 10[1] | | | | | | |
| | $C_L$ | Load capacitance | 2 | | 21 | pF |
| | $t_J$ | Peak-to-peak jitter | | | X[5] + 603 | ps |
| | $t_{JC2C}$ | Cycle-to-cycle jitter | | | X[5] + 615 | ps |
| | $t_{W(CLKOUT1)}$ | Pulse duration, sys_clkout1 low or high | $0.47*t_{c(CLKOUT1)}$ | | $0.53*t_{c(CLKOUT1)}$ | |
| | $t_{R(CLKOUT1)}$ | Rise time, sys_clkout1 | 0.4[2] [4] | | 5[3] | ns |

**Table 4-11. sys_clkout1 Output Clock Switching Characteristics[6] (continued)**

| NAME | | DESCRIPTION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| | $t_{F(CLKOUT1)}$ | Fall time, sys_clkout1 | 0.4[2] [4] | | 5[3] | ns |

(1) The mode is configured by bits SC0 and SC1 of the IO cell. For more details, see the *AM/DM37x Multimedia Device Technical Reference Manual* (SPRUGN4).

(2) At minimum load

(3) At maximum load (Maximum frequency 20 MHz)

(4) Caution: this creates EMI parasitics up to 1.2 ns

(5) X parameter corresponds to the input jitter contribution added at sys_xtalin input pin. For more information regarding the sys_xtalin input jitter requirement, see Section 4.1.1.

(6) In this table, the transition times are calculated for 10%-90% of VDDS. For more information on the corresponding VDDS power supply name, please see the Ball Characteristics table corresponding to your package. The POWER column defines the VDDS power supply for each ball.



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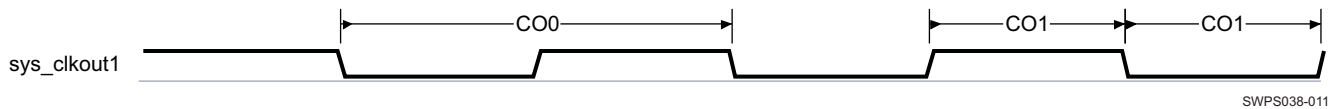
**Figure 4-6. sys_clkout1 Output Clock**

## 4.2.2  sys_clkout2 Output Clock

Table 4-12 summarizes the sys_clkout2 ouput clock electrical characteristics.

**Table 4-12. sys_clkout2 Output Clock Electrical Characteristics**

| NAME | DESCRIPTION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| f | Frequency, sys_clkout2 | sys_xtalin clock or core_dpll clock[1] or 54 MHz, 96 MHz[2] | | | MHz |
| $C_L$ | Load capacitance | 2 | | 22 | pF |
| $Z_T$ | Transmission line impedance | 30 | | 70 | Ω |
| $L_T$ | Transmission line length | 1 | | 6 | cm |

(1) Possible divider: 4, 8, or 16.

(2) Possible divider: 1, 2, 4, 8, or 16.

Table 4-13 details the sys_clkout2 ouput clock switching characteristics.

**Table 4-13. sys_clkout2 Output Clock Switching Characteristics[8]**

| NAME | | DESCRIPTION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| CO0 | $1 / t_{c(CLKOUT2)}$ | Frequency, sys_clkout2 | sys_xtalin clock or core_dpll clock[3] or 54 MHz, 96 MHz[4] | | | MHz |
| | $t_{c(xtalin)}$ | Cycle time, sys_xtalin | | | 1 / sys_xtalin (MHz) | ns |
| | $t_{c(coredpll)}$ | Cycle time, core_dpll (DPLL3) [7] | | | 1 / core_dpll (MHz) | ns |
| | $t_{c(54mhz)}$ | Cycle time, 54MHz clock (DPLL4) [7] | | | 18.52 | ns |
| | $t_{c(96mhz)}$ | Cycle time, 96MHz clock (DPLL4) [7] | | | 10.42 | ns |
| CO1 | $t_{w(CLKOUT2)}$ | Pulse duration, sys_clkout2 low or high | 0.49*tc(clkout2) | | 0.51*tc(clkout2) | ns |

**Table 4-13. sys_clkout2 Output Clock Switching Characteristics[8] (continued)**

| NAME | DESCRIPTION | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_J$ [5] | Peak-to-peak jitter | Source clock: sys_xtalin | | | X%[6] * $t_{c(xtalin)}$ + 200 | ps |
| | | Source clock: core_dpll | | | 4% * $t_{c(coredpll)}$ + 200 | ps |
| | | Source clock: 54MHz | | | 4% * $t_{c(54mhz)}$ + 200 | ps |
| | | Source clock: 96MHz | | | 4% * $t_{c(96mhz)}$ + 200 | ps |
| $t_{R(CLKOUT2)}$ | Rise time, sys_clkout2 | | 1.5[1] | | 5[2] | ns |
| $t_{F(CLKOUT2)}$ | Fall time, sys_clkout2 | | 1.5[1] | | 5[2] | ns |

(1)  At minimum load

(2)  At maximum load (maximum frequency 104 MHz)

(3)  Possible divider: 4, 8, 16

(4)  Possible divider: 1, 2, 4, 8, or 16

(5)  Peak-to-peak jitter is meant here as follows:

– The maximum value is the difference between the longest measured clock period and the expected clock period
– The minimum value is the difference between the shortest measured clock period and the expected clock period

Maximum and minimum are obtained on a statistical population of 300 period samples and expressed relative to the expected clock period.

(6)  Depending on the internal system clock divider configuration (PRCM.PRM_CLKSRC_CTRL[7:6], SYSCLKDIV bit field), the sys_xtalin input clock can be divided by 2 to provide the standard system clock (SYS_CLK) frequencies. For more information, see the Power, Reset, and Clock Management / PRCM Functional Description / PRCM Clock Manager Functional Description / External Clock I/Os / External Clock Inputs / High-Frequency System Clock section of *AM/DM37x Multimedia Device Technical Reference Manual* (literature number SPRUGN4).

In X%, X represents then the internal system clock divider with following possible values: X = 1 or 2.

(7)  This cycle time specified here is the clock period of the clock going out of sys_clkout2.

(8)  In this table, the transition times are calculated for 10%-90% of VDDS. For more information on the corresponding VDDS power supply name, please see the Ball Characteristics table corresponding to your package. The POWER column defines the VDDS power supply for each ball.
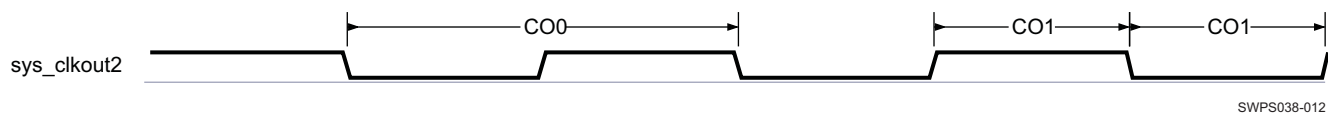


SWPS038-012

**Figure 4-7. sys_clkout2 Output Clock**

## 4.3  DPLL and DLL Specifications

> **NOTE**
>
> For more information, see Power, Reset, and Clock Management / PRCM Functional Description / PRCM Clock Manager Functional Description / Internal Clock Generation / DPLLs section of the *AM/DM37x Multimedia Device Technical Reference Manual* (SPRUGN4).

The applicative subsystem integrates six DPLLs and a DLL. The PRM and CM drive those listed below.

The main DPLLs are:
• DPLL1 (MPU)
• DPLL2 (IVA)
• DPLL3 (Core)
• DPLL4 (Peripherals)
• DPLL5 (Second peripherals DPLL)

### 4.3.1 DPLL Characteristics

Table 4-14 summarizes the DPLL characteristics and assumes testing over recommended operating conditions.

**Table 4-14. DPLL1 - DPLL2 - DPLL3 - DPLL5 Characteristics**

| NAME | DESCRIPTION | MIN | TYP | MAX | UNIT | COMMENTS |
|------|-------------|-----|-----|-----|------|----------|
| vdda_dplls_dll | Supply voltage for DPLLs (MPU, IVA, and Core) and DLL | 1.71 | 1.8 | 1.91 | V | |
| vdda_dpll_per | Supply voltage for DPLL (Peripherals) | 1.71 | 1.8 | 1.91 | V | |
| $f_{input}$ | CLKINP Input frequency | 0.032 | | 52 | MHz | FINP |
| $f_{internal}$ | Internal reference frequency | 0.032 | | 52 | MHz | REFCLK |
| $f_{CLKINPHIF}$ | CLKINPHIF Input frequency | 10 | | 1000 | MHz | FINPHIF |
| $f_{CLKINPULOW}$ | CLKINPULOW Input frequency | 0.001 | | 800 | MHz | |
| $f_{CLKOUT}$ | CLKOUT output frequency | 10[1] | | 1000[2] | MHz | [M / (N + 1)] * FINP * [1 / M2] |
| $f_{CLKOUTx2}$ | CLKOUTx2 output frequency | 20[1] | | 2000[2] | MHz | 2 * [M / (N + 1)] * FINP * [1 / M2] |
| $f_{CLKOUTHIF}$ | CLKOUTHIF output frequency | 10[3] | | 1000[4] | MHz | FINPHIF / M3 |
| | | 20[3] | | 2000[4] | | 2 * [M / (N + 1)] * FINP * [1 / M3] |
| $f_{DCOCLKLDO}$ | DCOCLKLDO output frequency | 20 | | 2000 | MHz | 2 * [M / (N + 1)] * FINP |
| $t_{lock}$ | Frequency lock time | | | 1.9 + 350*REFCLK | µs | |
| $p_{lock}$ | Phase lock time | | | 1.9 + 500*REFCLK | µs | |
| $t_{relock-L}$ | Relock time—Frequency lock[5] (Low power bypass) | | | 1.9 + 70*REFCLK | µs | DPLL in low-power mode: lowcurrstdby = 1 |
| $p_{relock-L}$ | Relock time—Phase lock[5] (Low power bypass) | | | 1.9 + 120*REFCLK | µs | DPLL in low-power mode: lowcurrstdby = 1 |
| $t_{relock-F}$ | Relock time—Frequency lock[5] (Fast relock bypass) | | | 0.05 + 70*REFCLK | µs | DPLL in normal mode: lowcurrstdby = 0 |
| $p_{relock-F}$ | Relock time—Phase lock[5] (Fast relock bypass) | | | 0.05 + 120*REFCLK | µs | DPLL in normal mode: lowcurrstdby = 0 |

(1) The minimum frequencies on CLKOUT and CLKOUTX2 are assuming M2 = 1. For M2 > 1, the minimum frequency on these clocks will further scale down by factor of M2.

(2) The maximum frequencies on CLKOUT and CLKOUTX2 are assuming M2 = 1.

(3) The minimum frequency on CLKOUTHIF is assuming M3 = 1. For M3 > 1, the minimum frequency on this clock will further scale down by factor of M3.

(4) The maximum frequency on CLKOUTHIF is assuming M3 = 1.

(5) Relock time assumes typical operating conditions, 10°C maximum temperature drift.

**Table 4-15. DPLL4 Characteristics**

| NAME | DESCRIPTION | MIN | TYP | MAX | UNIT | COMMENTS |
|------|-------------|-----|-----|-----|------|----------|
| vdda_dpll_per | Supply voltage for DPLL (peripherals) | 1.71 | 1.8 | 1.91 | V | |
| $f_{input}$ | CLKINP input clock frequency | 0.5 | | 60 | MHz | FINP |
| $f_{internal}$ | REFCLK internal reference frequency | 0.5 | | 2.5 | MHz | REFCLK |
| $f_{CLKINPULOW}$ | CLKINPULOW bypass input frequency | 0.001 | | 800 | MHz | |
| $f_{CLKOUT}$ | CLKOUT output clock frequency | 10[1] | | 2000[2] | MHz | [M / (N + 1)] * FINP * [1 / M2] |
| $f_{DCOCLKLDO}$ | Internal oscillator (DCO) output clock frequency | 500 | | 2000 | MHz | [M / (N + 1)] * FINP |
| $t_{lock}$ | Frequency lock time | | | 350*REFCLK | µs | |
| $p_{lock}$ | Phase lock time | | | 500*REFCLK | µs | |
| $t_{relock-L}$ | Relock time—Frequency lock[3] (Low power bypass) | | | 7.5 + 30*REFCLKs | µs | DPLL in low-power mode: lowcurrstdby = 1 |

### Table 4-15. DPLL4 Characteristics (continued)

| NAME | DESCRIPTION | MIN | TYP | MAX | UNIT | COMMENTS |
|---|---|---|---|---|---|---|
| p$_{relock-L}$ | Relock time—Phase lock[3] (Low power bypass) | | | 7.5 + 125*REFCLKs | µs | DPLL in low-power mode: lowcurrstdby = 1 |
| t$_{relock-F}$ | Relock time—Frequency lock[3] (Fast relock bypass) | | | NA | µs | |
| p$_{relock-F}$ | Relock time—Phase lock[3] (Fast relock bypass) | | | NA | µs | |

(1)  The minimum frequency on CLKOUT is assuming M2 = 1. For M2 > 1, the minimum frequency on this clock will further scale down by factor of M2.

(2)  The maximum frequency on CLKOUT is assuming M2 = 1.

(3)  Relock time assumes typical operating conditions, 10°C maximum temperature drift.

## 4.3.2   DLL Characteristics

Table 4-16 summarizes the DLL characteristics and assumes testing over recommended operating conditions.

### Table 4-16. DLL Characteristics

| NAME | DESCRIPTION | MIN | TYP | MAX | UNIT | COMMENTS |
|---|---|---|---|---|---|---|
| vdda_dplls_dll | Supply voltage for DPLLs (MPU, IVA, and Core) and DLL | 1.71 | 1.8 | 1.91 | V | |
| f$_{input}$ | Input clock frequency [1] | 66 | 120 | 200 | MHz | Either application mode 0 and 1 |
| t$_{lock}$ | Lock time | | | 500 | Clocks | |
| t$_{relock}$ | Relock time (Mode transitions through idle mode) | | | 500 | ns | IDLE to MODEMAXDELAY |
| | | | 250 | 450 | Clocks | IDLE to APPLICATION MODE 1 or 0 |
| | | | 1.88 | 3.38 | µs | IDLE to APPLICATION MODE @133 MHz |
| | | | 1.50 | 2.71 | µs | IDLE to APPLICATION MODE @166 MHz |
| | | | 1.25 | 2.25 | µs | IDLE to APPLICATION MODE @200 MHz |

(1)  Maximum frequency for nominal conditions.

### 4.3.3 DPLL and DLL Noise Isolation

The noise filters (decoupling capacitors) are required to suppress the switching noise generated by high frequency and to stabilize the supply voltage.

A noise filter is most effective when it is close to the device, because this minimizes the inductance of the circuit board wiring and interconnects.

Figure 4-8 illustrates an example of a noise filter.
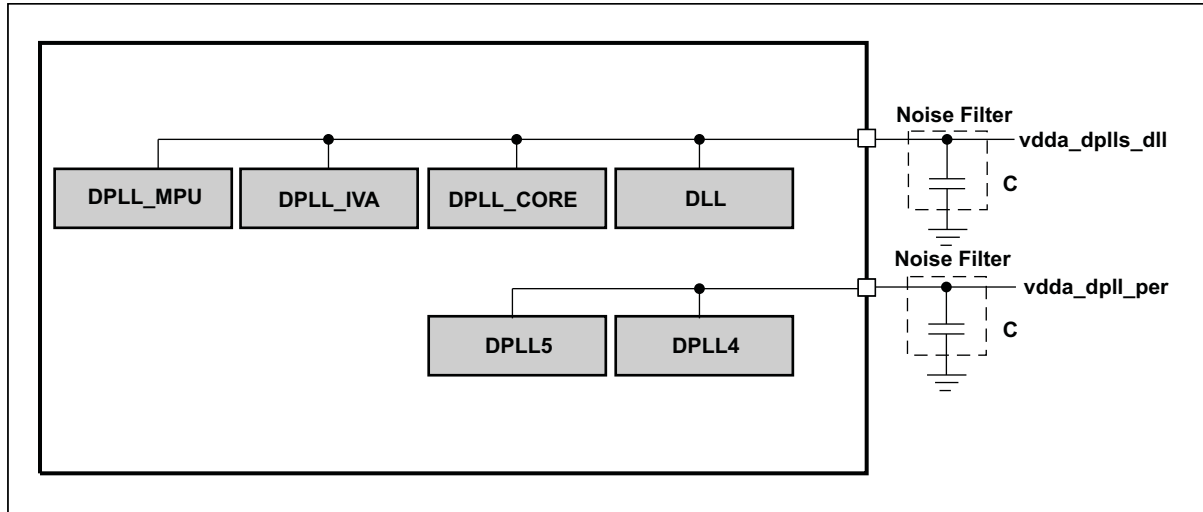


A. This circuit is provided only as an example.
B. The filter must be located as close as possible to the device.

**Figure 4-8. DPLL Noise Filter**

Table 4-17 specifies the noise filter requirements.

**Table 4-17. DPLL Noise Filter Requirements(1)**

| NAME | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|
| Filtering capacitor | 50 | 100 | 150 | nF |

(1) For more information, see IO and Analog Voltage Decoupling Capacitors.

### 4.3.4 Processor Clocks

Table 4-18 through Table 4-20 show the clocks AC performance values.

**Table 4-18. Processor Voltages Without SmartReflex™**

| | RETENTION | OPP50 | | | OPP100 | | | OPP130(3) | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | MIN | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX |
| VDD1(1) (2) (V) | 0.8 | 0.92 | 0.97 | 1.02 | 1.08 | 1.14 | 1.2 | 1.21 | 1.27 | 1.33 |

(1) At ball level.

(2) Minimum OPP voltage values defined in this table include any voltage transient.

(3) OPP130 is not available above $T_J$ of 90C.

**Table 4-19. Processor Voltages With SmartReflex™**

| | RETENTION | OPP50 | | | OPP100 | | | OPP130(4) | | | OPP1G (4) (5)(6) | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | MIN | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX |

### Table 4-19. Processor Voltages With SmartReflex™ (continued)

| | RETENTION | OPP50 | | | OPP100 | | | OPP130[4] | | | OPP1G [4] [5][6] | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| VDD1[1] [2] [3] (V) | 0.8 | 0.92 | 0.97 | 1.02 | 1.08 | 1.14 | 1.2 | 1.21 | 1.27 | 1.33 | 1.28 | 1.33 | 1.38 |

(1) At ball level.

(2) These VDD1 (vdd_mpu_iva) values are the required voltage ranges prior to enabling the SmartReflex AVS feature. After calibration, the minimum voltage may be lower than this specification.

(3) Minimum OPP voltage values defined in this table include any voltage transient.

(4) OPP130 and OPP1G are not available above $T_J$ of 90C.

(5) OPP1G is a high performance operating point which has following requirements:
  – ABB LDO must be set to FBB (Forward Body Bias) mode when switching to this OPP. It requires having a 1µF capacitor connected to cap_vdd_bb_mpu_iva.
  – AVS (Adaptive Voltage Scaling) power technique must be used to achieve optimum operating voltage.

(6) Based on DM3730 PCB constraints, the vdd_mpu_iva (VDD1) voltage value calibrated before enabling SmartReflex™ is recommended to be 1.38V. Minimum (1.28V) and typical (1.33V) values provided can be achieved only with very good power delivery network design. For more information on vdd_mpu_iva power delivery network design requirements, see the PCB Design Requirements for VDD_MPU_IVA Power Distribution Network for TI OMAP3630, AM37xx, and DM37xx Microprocessors (SPRABJ7) application note.

### Table 4-20. Processor Clocks

| Description | Source Clock | OPP50 | | OPP100 | | OPP130 | | OPP1G [2] | |
|---|---|---|---|---|---|---|---|---|---|
| | | Max Freq.(MHz) | Ratio | Max Freq.(MHz) | Ratio | Max Freq.(MHz) | Ratio | Max Freq.(MHz) | Ratio |
| DPLL1 Locked Frequency | - | 1200 | - | 1200 | - | 1600 | - | 2000 | - |
| DPLL1CLKOUT_M2 | DPLL1 Locked Frequency | 300 | 2 *(M2 = 2)[1][4] | 600 | 2 *(M2 = 1)[1][4] | 800 | 2 *(M2 = 1)[1][4] | 1000 | 2 *(M2 = 1)[1][4] |
| DPLL2 Locked Frequency | - | 1040 | - | 1040 | - | 1320 | - | 1600 | - |
| DPLL2CLKOUT_M2 | DPLL2 Locked Frequency | 260 | 2 *(M2 = 2)[1][4] | 520 | 2 *(M2 = 2)[1][4] | 660 | 2 *(M2 = 2)[1][4] | 800 | 2 *(M2 = 2)[1][4] |
| ARM_FCLK | DPLL1CLKOUT_M2 | 300 | 1 | 600 | 1 | 800 | 1 | 1000 | 1 |
| IVA_CLK | DPLL2CLKOUT_M2 | 260 | 1 | 520 | 1 | 660 | 1 | 800 | 1 |

(1) This ratio is configurable by software programming. For more information, see the *AM/DM37x Multimedia Device Technical Reference Manual* (SPRUGN4).

(2) OPP1G is a high performance operating point which has following requirements:
  – ABB LDO must be set to FBB (Forward Body Bias) mode when switching to this OPP. It requires having a 1µF capacitor connected to cap_vdd_bb_mpu_iva.
  – AVS (Adaptive Voltage Scaling) power technique must be used to achieve optimum operating voltage.

(3) For more information about ARM_FCLK and IVA2_CLK processor clocks configuration, see the Power, Reset, and Clock Management / PRCM Functional Description / PRCM Clock Manager Functional Description / Clock Configurations / Processor Clock Configurations section or the MPU Subsystem / MPU Subsystem Integration / MPU Subsystem Clock and Reset Distribution / Clock Distribution section of the *AM/DM37x Multimedia Device Technical Reference Manual* (SPRUGN4).

(4) The DPLL ratios documented in this table are recommended ratios. Other values may apply.

### 4.3.5 Device Core Clocks

Table 4-21 and Table 4-22 show the device core clocks AC performance values.

**Table 4-21. Device Core Voltages**

| | RETENTION | OPP50 | | | OPP100 | | |
|---|---|---|---|---|---|---|---|
| | MIN | MIN | TYP | MAX | MIN | TYP | MAX |
| VDD2 [1] [2] [3] (V) | 0.8 | 0.90 | 0.95 | 1.00 | 1.08 | 1.14 | 1.20 |

(1) At ball level.

(2) Minimum OPP voltage values defined in this table include any voltage transient.

(3) When SmartReflex™ is not used, these values define the required voltage range. When SmartReflex™ will be used, these voltages are the required voltage range prior to enabling the SmartReflex™ feature. After calibration, the minimum voltage may be lower than this specification.

**Table 4-22. Device Core Clocks**

| Description | Source | OPP50 | | | | | | OPP100 | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Max Freq.(MHz) | Ratio | Max Freq.(MHz) | Ratio | Max Freq.(MHz) | Ratio | Max Freq.(MHz) | Ratio | Max Freq.(MHz) | Ratio | Max Freq.(MHz) | Ratio |
| DPLL3 Locked Frequency | - | 800 | - | 664 | - | 400 | - | 800 | - | 664 | - | 532 | - |
| DPLL3CLKOUT_M2 | DPLL3 Locked Frequency | 200 | $2*(M2 = 2)$[1][2] | 166 | $2*(M2 = 1)$[1][2] | 200 | $2*(M2 = 1)$[1][2] | 400 | $2*(M2 = 1)$[1][2] | 332 | $2*(M2 = 1)$[1][2] | 266 | $2*(M2 = 1)$[1][2] |
| CORE_CLK | DPLL3CLKOUT_M2 | 200 | 1 | 166 | 1 | 200 | 1 | 400 | 1 | 332 | 1 | 266 | 1 |
| L3_ICLK | CORE_CLK | 100 | 2[1] | 83 | 2[1] | 100 | 2[1] | 200 | 2[1] | 166 | 2[1] | 133 | 2[1] |
| L4_ICLK | L3_ICLK | 50 | 2[1] | 41.5 | 2[1] | 50 | 2[1] | 100 | 2[1] | 83 | 2[1] | 66.5 | 2[1] |
| SDRC_CLK | L3_ICLK | 100 | 1 | 83 | 1 | 100 | 1 | 200 | 1 | 166 | 1 | 133 | 1 |
| GPMC_CLK | L3_ICLK | 50 | 2[1] | 41.5 | 2[1] | 50 | 2[1] | 100 | 2[1] | 83 | 2[1] | 66.5 | 2[1] |

(1) This ratio is configurable by software programming. For more information, see the *AM/DM37x Multimedia Device Technical Reference Manual* (SPRUGN4).

(2) The DPLL ratios documented in this table are recommended ratios. Other values may apply.

### 4.3.6 Graphic Accelerator (SGX) Clocks

Table 4-23 and Table 4-24 show the recommended $V_{DD2}$ (corresponding to vdd_core, Core and SGX voltage at ball level) voltages ranges and the standard graphic accelerator (SGX) clocks speed characteristics vs $V_{DD2}$.

**Table 4-23. Graphic Accelerator Voltages**

| | OPP 100 [2] | | |
|---|---|---|---|
| | MIN | TYPICAL | MAX |
| $V_{DD2}$[1][3][4] (V) | 1.08 | 1.14 | 1.20 |

(1) At ball level.

(2) SGX (Graphic Accelerator) is not available in the OPP50 operating point.

(3) When SmartReflex™ is not used, these values define the required voltage range. When SmartReflex™ will be used, these voltages are the required voltage range prior to enabling the SmartReflex™ feature. After calibration, the minimum voltage may be lower than this specification.

(4) Minimum OPP voltage values defined in this table include any voltage transient.

## Table 4-24. Graphic Accelerator Clocks[2]

| Description | Source Clock | OPP 100[2] | | | | | |
|---|---|---|---|---|---|---|---|
| | | Max Freq (MHz) | Ratio | Max Freq (MHz) | Ratio | Max Freq (MHz) | Ratio |
| DPLL3 Locked Frequency | | 800 | | 664 | | 532 | |
| DPLL4 Locked Frequency | | 1728 | | 1728 | | 1728 | |
| DPLL3CLKOUTX2_M2 | DPLL3 Locked Frequency | 800 | 1 * (M2 = 1)[1][3] | 664 | 1 * (M2 = 1)[1][3] | 532 | 1 * (M2 = 1)[1][3] |
| DPLL3CLKOUT_M2 | DPLL3 Locked Frequency | 400 | 2 * (M2 = 1)[1][3] | 332 | 2 * (M2 = 1)[1][3] | 266 | 2 * (M2 = 1)[1][3] |
| DPLL4CLKOUT_M2 | DPLL4 Locked Frequency | 192 | 1 * (M2 = 9)[1][3] | 192 | 1 * (M2 = 9)[1][3] | 192 | 1 * (M2 = 9)[1][3] |
| CORE_CLK | DPLL4 Locked Frequency | 400 | 1 | 332 | 1 | 266 | 1 |
| COREX2_CLK | DPLL3CLKOUTX2_M2 | 800 | 1 | 664 | 1 | 532 | 1 |
| SGX_192M_FCLK | DPLL4CLKOUT_M2 | 192 | 1 | 192 | 1 | 192 | 1 |
| SGX – Option 1 | CORE_CLK | 200 | 2 | 166 | 2 | 133 | 2 |
| SGX – Option 2 | COREX2_CLK | | | | | 177.3 | 3 |
| SGX – Option 3 | SGX_192M_FCLK | 192 | 1 | 192 | 1 | 192 | 1 |

(1) This ratio is configurable by software programming. For more information, see the *AM/DM37x Multimedia Device Technical Reference Manual* (SPRUGN4).

(2) SGX (Graphic Accelerator) is not available in OPP50 operating point.

(3) The DPLL ratios documented in this table are recommended ratios. Other values may apply.

# 5 Video DAC Specifications

**NOTE**

For more information regarding the VideoDAC architecture, see the Display Subsystem / Display Subsystem Functional Description / Video Encoder Functionalities / Video DAC Stage—Architecture and Control section of *AM/DM37x Technical Reference Manual* (literature number SPRUGN4).

## 5.1 TVOUT Buffer Mode (DAC + Buffer)

**NOTE**

AVDAC normal mode (DAC + Buffer), higher values of the DAC input code provided by the Video Encoder will result in lower output voltage due to the inverting configuration of the TVOUT Buffer. See Figure 5-4 for more details on the relation between the composite video signal levels and the DAC code values for normal mode of operation.

In AVDAC bypass mode (DAC only), higher values of the DAC input code will result in higher output voltage, as the TVOUT Buffer path is bypassed.

The connection for this TVOUT buffer mode (DAC + Buffer) normal mode of operation is shown in Figure 5-1. The default mode of operation is dc coupling. For more information regarding the recommended values of the external components, see Section 5.4, *Electrical Specifications Over Recommended Operating Conditions*.



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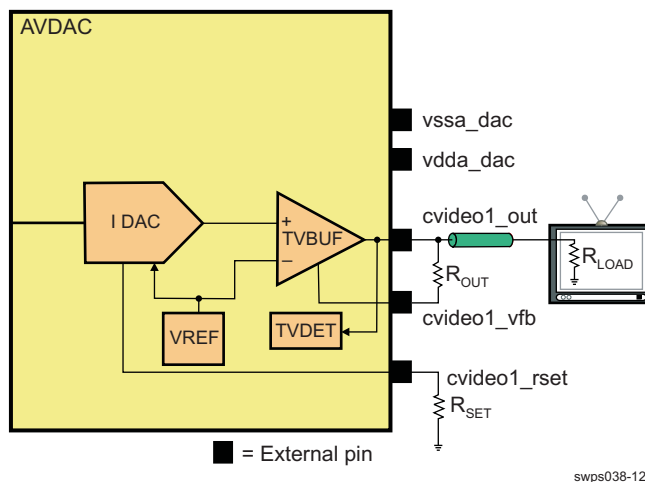
**Figure 5-1. Recommended Loading Conditions for TVOUT Buffer Mode(1)**

(1) In single-channel configuration only channel-1 is used.

## 5.2 TVOUT Bypass Mode (DAC Only)

In this case, TVOUT bypass input is high and the TVOUT buffer is bypassed (for more information, see Section 5.5, *TVOUT Bypass Mode Specifications (DAC-Only) Electrical Specifications Over Recommended Operating Conditions*). Figure 5-2 shows the connection. For more information regarding the recommended values of the external components, see Section 5.4, *Electrical Specifications Over Recommended Operating Conditions.*
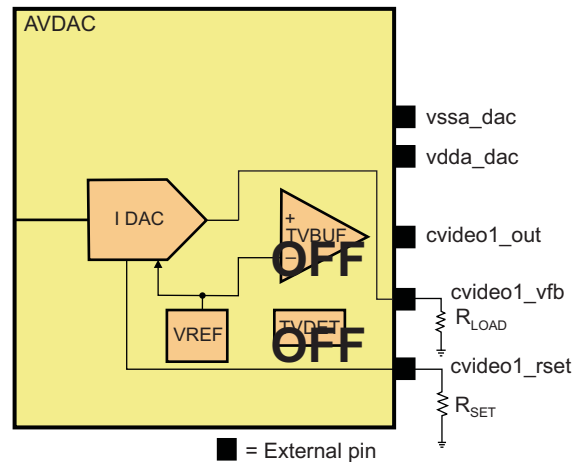


**Figure 5-2. Recommended Loading Conditions for TVOUT Bypass Mode(1)**

(1) In single-channel configuration only channel-1 is used.

## 5.3 TVOUT Bypass Mode in Dual-Channel Configuration

In this case, TVOUT bypass input is high and the TVOUT buffer is bypassed (for more information, see Section 5.5, *TVOUT Bypass Mode Specifications (DAC-Only) Electrical Specifications Over Recommended Operating Conditions*). Figure 5-3 shows the connection. For more information regarding the recommended values of the external components, see Section 5.4, *Electrical Specifications Over Recommended Operating Conditions.*
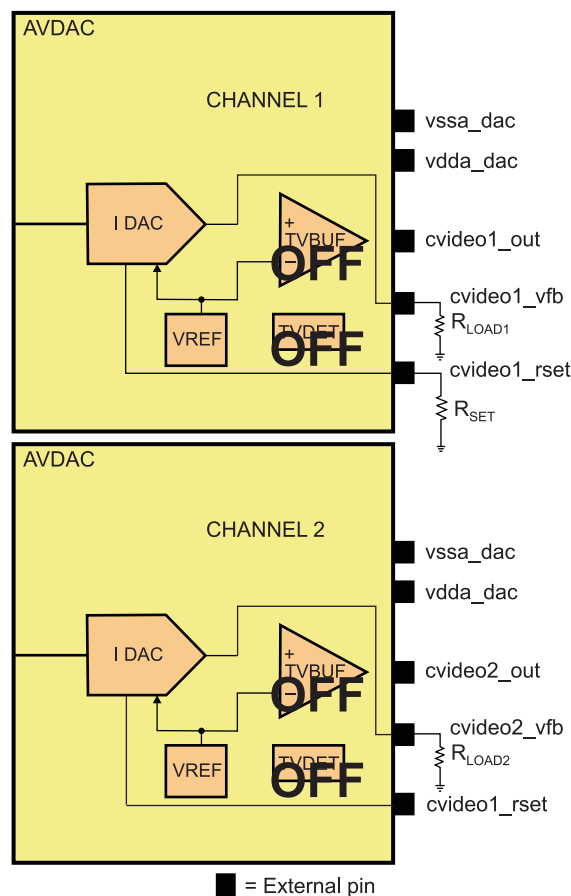


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**Figure 5-3. Recommended Loading Conditions for TVOUT Bypass Mode in Dual-Channel Configuration(1)**

(1) Here are some connections recommendations:
- An external resistor $R_{SET}$ = 10 kΩ (±1%) is recommended to be connected to the cvideo1_rset signal of Channel 1.
- The cvideo1_rset signal of Channel 2 is left unconnected.
- External resistors $R_{LOAD1LOAD2}$ = 1.5 kΩ (±1%) is recommended to be connected to cvideo1_vfb or cvideo2_vfb each channel.

## 5.4 Electrical Specifications Over Recommended Operating Conditions

### NOTE
High-swing mode is the default mode. The low-swing mode is not compliant with the NTSC and PAL video-standards. It shall be used only for backwards compatibility to AM/DM37x.

- TVOUT DC High Swing Mode:
  - $R_{OUT1/2}$ = 2.7 kΩ (±1%)
  - $R_{SET}$ = 4.7 kΩ (±1%)
  - $R_{LOAD}$ = 75 Ω (±5%)
  - $Z_{CABLE}$ = 75 Ω (±5%)
- TVOUT DC Low Swing Mode:
  - $R_{OUT1/2}$ = 2.7 kΩ (±1%)
  - $R_{SET}$ = 6.8 kΩ (±1%)
  - $R_{LOAD}$ = 75 Ω (±5%)
  - $Z_{CABLE}$ = 75 Ω (±5%)
- TVOUT AC High Swing Mode:
  - $R_{OUT1/2}$ = 2.7 kΩ (±1%)
  - $R_{SET}$ = 4.7 kΩ (±1%)
  - $R_{LOAD}$ = 75 Ω (±5%)
  - $Z_{CABLE}$ = 75 Ω (±5%)
  - $C_{AC}$ = 220 µF (±5%)
- TVOUT AC Low Swing Mode:
  - $R_{OUT1/2}$ = 2.7 kΩ (±1%)
  - $R_{SET}$ = 6.8 kΩ (±1%)
  - $R_{LOAD}$ = 75 Ω (±5%)
  - $Z_{CABLE}$ = 75 Ω (±5%)
  - $C_{AC}$ = 220 µF (±5%)

### Table 5-1. DAC – Static Electrical Specifications[8]

| PARAMETER | | CONDITIONS/ASSUMPTIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| R | Resolution | | | | 10 | | Bits |
| **DC ACCURACY** | | | | | | | |
| INL[1] | Integral Non-Linearity (INL) | 50 to 111 input code range | | –6 | | 6 | LSB |
| | Integral Non-Linearity (INL) Signal video range | 111 to 895 input code range | | –4 | | 4 | |
| | Integral Non-Linearity (INL) Synchronization pulse | 783 to 1007 input code range | | –5 | | 5 | |
| DNL[2] | Differential nonlinearity | 111 to 895 input code range | | –2.5 | | 2.5 | LSB |
| **ANALOG OUTPUT** | | | | | | | |
| - | Output voltage | 0 to 1023 input code range, $R_{LOAD}$ = 75 Ω | Low-swing mode | 0.70 | 0.88 | 1.00 | V |
| | | | High-swing mode | 1.2 | 1.3 | 1.5 | |
| - | Gain error | - | Low-swing mode | –20 | | 20 | % FS |
| | | | High-swing mode | –10 | | 10 | |
| $R_{VOUT}$ | Output impedance | | | 67.5 | 75.0 | 82.5 | Ω |
| **REFERENCE** | | | | | | | |
| $V_{REF}$ | Internal Band Gap Voltage Reference | | | | 0.55 | | V |

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**Table 5-1. DAC − Static Electrical Specifications[8] (continued)**

| PARAMETER | | | CONDITIONS/ASSUMPTIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **POWER CONSUMPTION** | | | | | | | |
| $I_{vdda-up}$ | Analog Supply Current[4] | DC mode No load | Average current on vdda_dac, no load, 2 channels<br>Input code 50 (maximum output voltage) | 4.5 | 6.5 | 8.5 | mA |
| | | AC mode No load | | 19 | 28 | 37 | |
| | | Full load 75-Ω load | | 19 | 28 | 37 | |
| $I_{vdda-up}$ (peak) | Peak analog supply current | | Lasts less than 1 ns | | 60 | | mA |
| $I_{vdd-up}$ | Digital supply current[5] | | Average current, measured at $f_{CLK}$ = 54 MHz,<br>$f_{OUT}$ = 2 MHz sine wave, vdd = 1.1 V | | | 2 | mA |
| $I_{vdd-up}$ (peak) | Peak digital supply current[6] | | Peak current, full-scale transition lasting less than 1 ns | | 8 | | mA |
| $I_{vdda-down}$[9] | Analog supply current, total power down[9] | | T = 30ºC, vdda_dac = 1.8 V, no load | | | 12 | µA |
| $I_{vdda-stdby}$[9] | Analog supply current, standby mode[9] | | Bandgap and internal LDO are ON, all other analog blocks are OFF, no load, T = 30 Cº | 90 | 180 | 270 | µA |
| $I_{vdd-down(pm)}$[9] | Digital supply current, total power down[9] | | T = 30ºC, Full or Partial Power Management | Low-swing mode | | | 2 | µA |
| | | | | High-swing mode | | | 6 | |
| $I_{vdd-down(nopm)}$ | Digital supply current, total power down (no power management) | | T = 30ºC, VDD = 1.1 V, no Power Management | | | 60 | µA |

(1) The INL is measured at the output of the DAC (accessible at an external pin during bypass mode). The INL at code 783 equals 0.

(2) The DNL is measured at the output of the DAC (accessible at an external pin during bypass mode). The INL at code 783 equals 0.

(3) Reference PSR measures the effect of a supply disturbance at cvideo1_out and cvideo2_out.

(4) The analog supply current $I_{vdda}$ is directly proportional to the full-scale output current IFS and is insensitive to $f_{CLK}$.

(5) The digital supply current $I_{VDD}$ is dependent on the digital input waveform, the DAC update rate $f_{CLK}$, and the digital supply VDD.

(6) The peak digital supply current occurs at full-scale transition for duration less than 1 ns.

(7) See Section 5.6, *Analog Supply (vdda_dac) Noise Requirements*, for actual maximum ripple allowed on vdda_dac.

(8) For more information on code range definition, see Figure 5-4.

(9) For more information on AVDAC power-up, power-down, and standby mode configurations, see Display Subsystem / Display Subsystem Functional Description / Video Encoder Functionalities / Video DAC Stage Power Management section of *AM/DM37x Technical Reference Manual* (literature number SPRUGN4).

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**NOTE**

High-swing mode is the default mode. The low-swing mode is not compliant with the NTSC and PAL video-standards. It is used only for backwards compatibility to AM/DM37x.

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## Table 5-2. Video DAC − Dynamic Electrical Specifications[6]

| PARAMETER | CONDITIONS/ASSUMPTIONS | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $f_{CLK}$[1] | Output update rate | Equal to input clock frequency | | | 54 | 60 | MHz |
| | Clock jitter | RMS clock jitter required in order to assure 10-bit accuracy | | | 40 | 70 | ps |
| | Attenuation at 5.1 MHz | Corner frequency for signal | DC mode | | | 1.5 | dB |
| | | | AC mode | | | | |
| BW | Signal bandwidth | 3 dB | DC mode | | 6 | | MHz |
| | | | AC mode | | | | |
| | Differential gain[2] | 111 to 895 input code range | DC mode | –5% | | 5% | |
| | | | AC mode | –5% | | 5% | |
| | Differential phase[2] | 111 to 895 input code range | DC mode | –3º | | 3º | |
| | | | AC mode | –3º | | 3º | |
| SFDR | Within bandwidth 1 kHz to 6 MHz | $f_{CLK}$ = 54 MHz, $f_{OUT}$ = 1 MHz, sine wane input, 111 to 895 input code range | DC mode | 40 | 50 | 70 | dB |
| | | | AC mode | | | | |
| SNR | Within bandwidth 1 kHz to 6 MHz | $f_{CLK}$ = 54 MHz, $f_{OUT}$ = 1 MHz, sine wane input, 256 to 768 input code range | DC mode | 50 | 54 | 75 | dB |
| | | | AC mode | | | | |
| PSR[4] | Power supply rejection (up to 6 MHz) | 100 mVpp at 6 MHz, input code 895 | | | 6[4] | | dB |
| Crosstalk | Between the two video channels | | | | –50 | –40 | dB |
| $C_{Load}$ | TVOUT (cvideo_out1 and cvideo_out2) stability, TVOUT decoupling capacity | Total decoupling capacity from cvideo_out1 or cvideo_out2 to ground, $C_{Load1}$ | | | | 300 | pF |
| $C_{TOT}$ | TVOUT stability, total TVOUT decoupling capacity | Total decoupling capacity: $C_{TOT}$ = $C_{Load1}$ + $C_{Load2}$ | | | | 600 | pF |

(1)  For internal input clock information, see the DSS chapter of *AM/DM37x Technical Reference Manual* (literature number SPRUGN4).

(2)  The differential gain and phase value is for dc coupling. Note that there is degradation for the ac coupling. The Differential Gain and Phase are measured with respect to the gain and phase of the burst signal (–20 to 20 IRE)

(3)  The SNR value is for dc coupling.

(4)  PSR measures the effect of a supply disturbance at cvideo1_out and cvideo2_out.

(5)  The flat band measurement is done at 500 kHz for characterizing the attenuation at 5.1 MHz.

(6)  For more information on code range definition, see Figure 5-4.

Figure 5-4 describes the composite video signal levels.
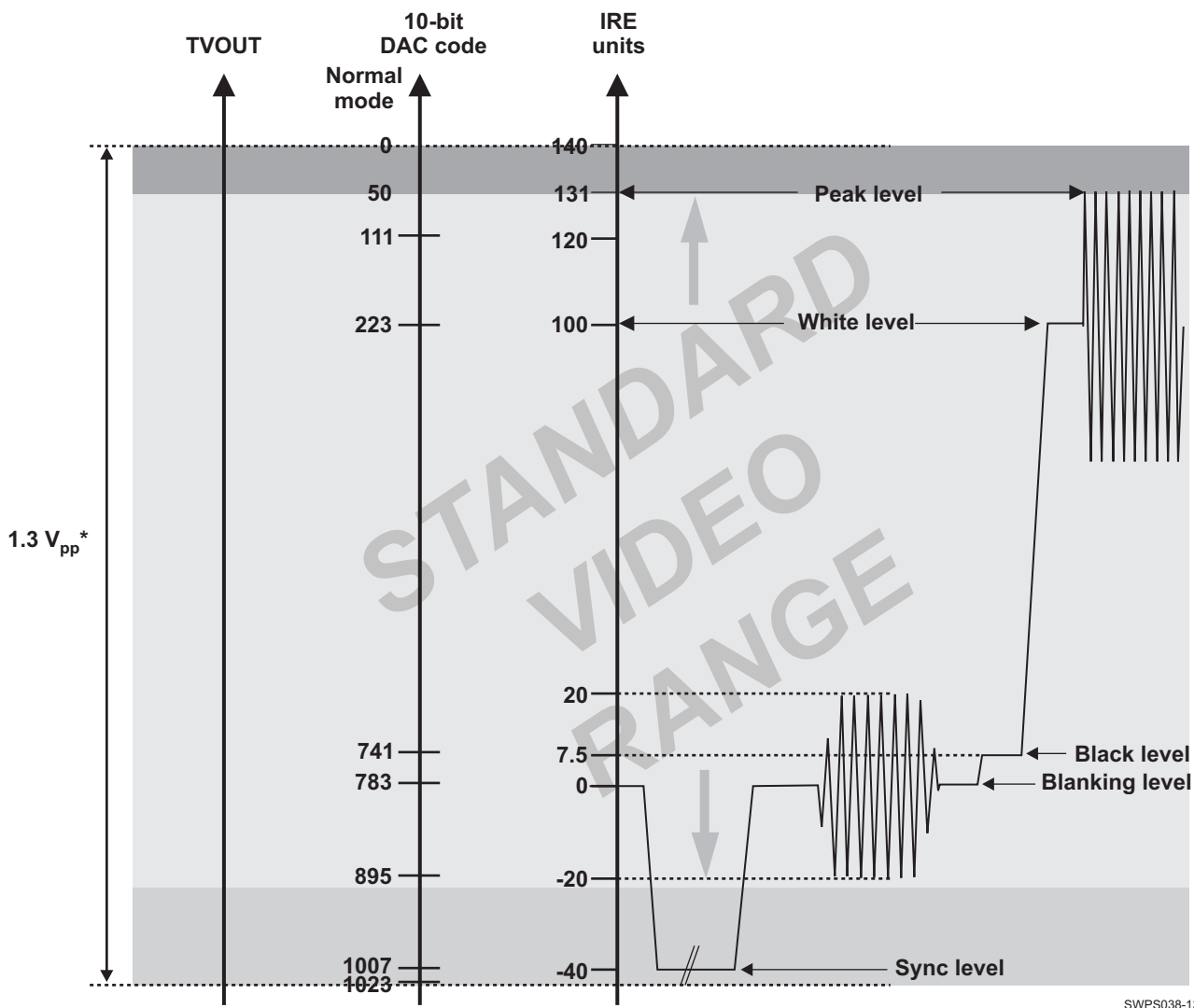


**Figure 5-4. Composite Video Signal Levels(1)(2)**

(1) The 1.3 V$_{PP}$ (peak-to-peak) is referring to the output signal at cvideo1_out in the DAC + Buffer composite-video mode.
Note that the 1.3 V$_{PP}$ must apply to both cvideo1_out and cvideo2_out in DAC + Buffer s-video mode (dual-DAC mode configured for ac or dc coupling).

(2) In AVDAC normal mode (DAC + Buffer), higher values of the DAC input code provided by the Video Encoder will result in lower output voltage due to the inverting configuration of the TVOUT Buffer. See Figure 5-4 for more details on the relation between the composite video signal levels and the DAC code values for normal mode of operation.
In AVDAC bypass mode (DAC only), higher values of the DAC input code will result in higher output voltage, as the TVOUTBuffer path is bypassed.

## 5.5 TVOUT Bypass Mode Specifications (DAC-Only) Electrical Specifications Over Recommended Operating Conditions

**NOTE**
The electrical characteristics for single- and dual-channel bypass modes are the same except that the active current will double in the dual-channel configuration.

- Bypass Mode
  - $R_{LOAD}$ = 1.5 kΩ (±1%)
  - $R_{SET}$ = 10 kΩ (±1%)

### Table 5-3. DAC—Static Electrical Specifications—Bypass Mode[2]

| | PARAMETER | CONDITIONS/ASSUMPTIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| R | Resolution | | | 10 | | Bits |
| **DC ACCURACY** | | | | | | |
| INL[1] | Integral nonlinearity (INL) | 37 to 954 input code range, $R_{LOAD}$ = 1.5 kΩ | –1 | | 1 | LSB |
| DNL[1] | Differential nonlinearity | 37 to 954 input code range, $R_{LOAD}$ = 1.5 kΩ | –1 | | 1 | LSB |
| **ANALOG OUTPUT** | | | | | | |
| - | Output voltage | $R_{LOAD}$ = 1.5 kΩ | 0.6 | 0.7 | 0.77 | V |
| - | Output current | $R_{LOAD}$ = 1.5 kΩ | 0.6 | 0.7 | 0.77 | V |
| - | Gain error | - | –10 | | 10 | % FS |
| **POWER CONSUMPTION** | | | | | | |
| $I_{vdda-up}$ | Analog supply current | Average current on vdda_dac, $R_{LOAD}$ = 1.5 kΩ Input code 1023 | 0.7 | 1.0 | 1.4 | mA |
| $I_{vdda-down}$ | Analog supply current, total power down | T = 30C°, vdda_dac = 1.8 V, no load | | | 12 | µA |
| $I_{vdda-stdby}$ | Analog supply current, standby mode | Bandgap and internal LDO are ON, all other analog blocks are OFF, no load, T = 30C° | 90 | 180 | 270 | µA |

(1) In bypass mode, output node is cvideo1_out and cvideo2_out nodes. For more information, see Section 5.2, *TVOUT Bypass Mode (DAC Only)* or Section 5.3, *TVOUT Bypass Mode in Dual-Channel Configuration*.

(2) For more information on code range definition, see Figure 5-4.

### Table 5-4. Video DAC—Dynamic Electrical Specifications—Bypass Mode

| | PARAMETER | CONDITIONS/ASSUMPTIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $f_{CLK}$ | Output update rate | Equal to input clock frequency | | 54 | 60 | MHz |
| | Clock jitter | RMS clock jitter required in order to assure 10-bit accuracy | | 40 | 70 | ps |
| BW | Signal bandwidth | 3dB | | 6 | | MHz |
| SFDR | Within bandwidth 1 kHz to 6 MHz | $f_{CLK}$ = 54 MHz, $f_{OUT}$ = 1 MHz, sine wave input, 111 to 895 input code range | 40 | 50 | 70 | dB |
| SNR | Within bandwidth 1 kHz to 6 MHz | $f_{CLK}$ = 54 MHz, $f_{OUT}$ = 1 MHz, sine wave input, 256 to 768 input code range | 50 | 54 | 75 | dB |
| PSR | Power supply rejection (up to 6 MHz) | 100 mVpp at 6 MHz, input code 895 | | 6[1] | | dB |

(1) For more information on code range definition, see Figure 5-4.

## 5.6 Analog Supply (vdda_dac) Noise Requirements

In order to assure 10-bit accuracy of the DAC analog output, the analog supply vdda_dac has to meet the noise requirements stated in this section.

The DAC Power Supply Rejection Ratio (PSRR) is defined as the relative variation of the full-scale output current divided by the supply variation. Thus, it is expressed in percentage of Full-Scale Range (FSR) per volt of supply variation as shown in the following equation:

$$PSRR_{DAC} = \frac{100 \cdot \dfrac{\Delta I_{OUT}}{I_{OUTFS}}}{V_{AC}} \qquad \left[\% \, FSR \middle/ V\right]$$

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Depending on frequency, the PSRR is defined in Table 5-5.

**Table 5-5. Video DAC − Power Supply Rejection Ratio**

| Supply Noise Frequency | PSRR % FSR/V |
|---|---|
| 0 to 100 kHz | 1 |
| > 100 kHz | The rejection decreases 20 dB/dec. Example: at 1 MHz the PSRR is 10% of FSR/V. |

A graphic representation is shown in Figure 5-5.
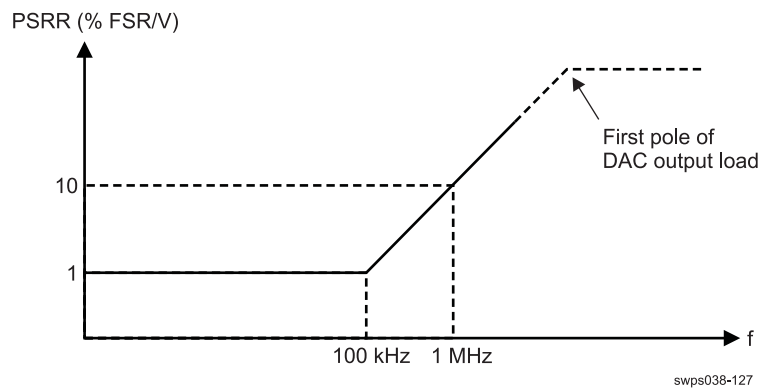


**Figure 5-5. Video DAC − Power Supply Rejection Ratio**

To ensure that the DAC SFDR specification is met, the PSRR values and the clock jitter requirements translate to the following limits on vdda_dac (for the Video DAC).

The maximum peak-to-peak noise on vdda (ripple) is defined in Table 5-6.

**Table 5-6. Video DAC − Maximum Peak-to-Peak Noise on vdda_dac**

| Tone Frequency | Maximum Peak-to-Peak Noise on vdda_dac |
|---|---|
| 0 to 100 kHz | < 30 mV$_{PP}$ |
| > 100 kHz | Decreases 20 dB/dec. Example: at 1 MHz the maximum is 3 mV$_{PP}$ |

The maximum noise spectral density (white noise) is defined in Table 5-7.

**Table 5-7. Video DAC − Maximum Noise Spectral Density**

| Supply Noise Bandwidth | Maximum Supply Noise Density |
|---|---|
| 0 to 100 kHz | < 20 μV / √Hz |
| > 100 kHz | Decreases 20 dB/dec. Example: at 1 MHz the maximum noise density is 2 μV / √Hz |

Because the DAC PSRR deteriorates at a rate of 20 dB/dec after 100 kHz, it is highly recommended to have vdda_dac low pass filtered (proper decoupling) (see the illustrated application: Section 5.7, *External Component Value Choice*).

## 5.7 External Component Value Choice

The output current $I_{DACOUT}$ appearing at the output of the 10-bit DAC is a function of both the input code DAC_CODE (ranging from 0 to 1023) and $I_{DACMAX}$ and can be expressed as:

$$I_{DACOUT} = I_{REF} * (DAC\_CODE / 120) \quad (1)$$

The maximum output current $I_{DACMAX}$ from the DAC is given by:

$$I_{DACMAX} = I_{REF} * 1023 / 120 \quad (2)$$

The reference current, $I_{REF}$, is set by a combination of internal and external resistors in series, $R_{REF}$, and an internal reference voltage, $V_{REF}$, and is given by:

$$I_{REF} = V_{REF} / R_{REF} \quad (3)$$

Typically, $V_{REF} = 0.55$ V and $R_{REF} = 9.4$ kΩ in TVOUT High-Swing mode.

The video signal voltage at cvideo_out1 and cvideo_out2 nodes can be written as (excluding the offset voltage):

$$V_{TVOUT} = 35 * R_{LOAD} * I_{DACMAX} * (1 - DAC\_CODE / 1023) \quad (4)$$

Figure 5-6 shows the cvideo_out1 and cvideo_out2 transfer function. Regarding the typical composite video signal levels versus the DAC input code, for more information on code range definition, see Figure 5-4.

Regarding the typical values of the typical values for $R_{out1/2}$ and $R_{set}$ resistors, as well for $C_{out}$ capacitor, for different modes of the TV display interface, see the Display Subsystem / Display Subsystem Environment / TV Display Support section of *AM/DM37x Technical Reference Manual* (literature number SPRUGN4).
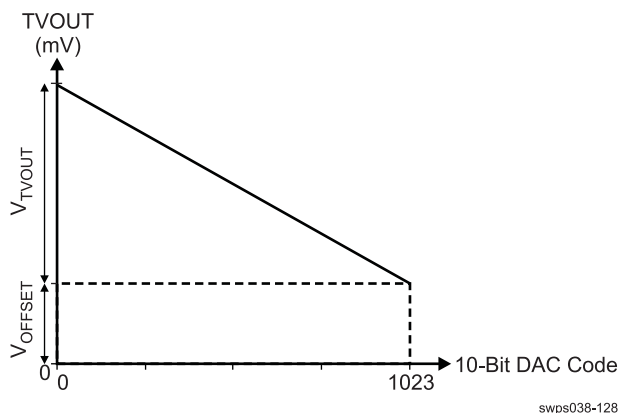


**Figure 5-6. cvideo_out1 and cvideo_ou2 Transfer Function**

**NOTE**
The dc levels (Voffset) will be shifted due to process variations.

# 6 Timing Requirements and Switching Characteristics

## 6.1 Timing Test Conditions

All timing requirements and switching characteristics are valid over the recommended operating conditions unless otherwise specified.

## 6.2 Interface Clock Specifications

### 6.2.1 Interface Clock Terminology

The interface clock is used at the system level to sequence the data and/or to control transfers accordingly with the interface protocol.

### 6.2.2 Interface Clock Frequency

The two interface clock characteristics are:
- The maximum clock frequency
- The maximum operating frequency

The interface clock frequency documented in this document is the maximum clock frequency, which corresponds to the maximum frequency programmable on this output clock. This frequency defines the maximum limit supported by the device IC and doesn't take into account any system consideration (PCB, Peripherals).

The system designer will have to consider these system considerations and the device IC timing characteristics as well, to define properly the maximum operating frequency, which corresponds to the maximum frequency supported to transfer the data on this interface.

### 6.2.3 Clock Jitter Specifications

Jitter is a phase noise, which may alter different characteristics of a clock signal. The jitter specified in this document is the time difference between the typical cycle period and the actual cycle period affected by noise sources on the clock. The cycle (or period) jitter terminology will be used to identify this type of jitter.



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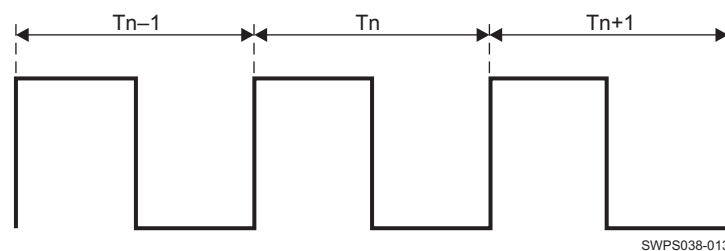
**Figure 6-1. Cycle (or Period) Jitter**

**NOTE**

Max. Cycle Jitter = Max (Ti)

Min. Cycle Jitter = Min (Ti)

Jitter Standard Deviation (or RMS Jitter) = Standard Deviation (Ti)

### 6.2.4 Clock Duty Cycle Error

The maximum duty cycle error is the difference between the absolute value of the maximum high-level pulse duration or the maximum low-level pulse duration and the typical pulse duration value.
- Maximum pulse duration = Typical pulse duration + maximum duty cycle error
- Minimum pulse duration = Typical pulse duration - maximum duty cycle error

## 6.3 Timing Parameters

The timing parameter symbols used in the timing requirements and switching characteristics tables are created in accordance with JEDEC Standard 100. To shorten the symbols, some of pin names and other related terminologies have been abbreviated as follows:

**Table 6-1. Timing Parameters**

| SUBSCRIPTS | |
|---|---|
| **SYMBOL** | **PARAMETER** |
| c | Cycle time (period) |
| d | Delay time |
| dis | Disable time |
| en | Enable time |
| h | Hold time |
| su | Setup time |
| START | Start bit |
| t | Transition time |
| v | Valid time |
| w | Pulse duration (width) |
| X | Unknown, changing, or don't care level |
| F | Fall time |
| H | High |
| L | Low |
| R | Rise time |
| V | Valid |
| IV | Invalid |
| AE | Active edge |
| FE | First edge |
| LE | Last edge |
| Z | High impedance |

## 6.4 External Memory Interfaces

The device includes the following external memory interfaces:

- General-purpose memory controller (GPMC)
- SDRAM controller (SDRC)

### 6.4.1 General-Purpose Memory Controller (GPMC)

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**NOTE**

For more information, see Memory Subsystem / General-Purpose Memory Controller section of the *AM/DM37x Multimedia Device Technical Reference Manual* (literature number SPRUGN4).

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The GPMC is the unified memory controller used to interface external memory devices such as:

- Asynchronous SRAM-like memories and ASIC devices
- Asynchronous page mode and synchronous burst NOR flash
- NAND flash

#### 6.4.1.1 GPMC/NOR Flash—Synchronous Mode

Table 6-3 and Table 6-4 assume testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-2 through Figure 6-6).

**Table 6-2. GPMC/NOR Flash Timing Conditions—Synchronous Mode**

| TIMING CONDITION PARAMETER | | VALUE | UNIT |
|---|---|---|---|
| **Input Conditions** | | | |
| $t_R$ | Input signal rise time | 1.8 | ns |
| $t_F$ | Input signal fall time | 1.8 | ns |
| **Output Conditions** | | | |
| $C_{LOAD}$ | Output load capacitance[1] | 12 | pF |

(1)  The load setting of the IO buffer: LB0 = 1.

**Table 6-3. GPMC/NOR Flash Timing Requirements—Synchronous Mode[1]**

| NO. | PARAMETER | | OPP100 | | OPP50 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| F12 | $t_{su(dV\text{-}clkH)}$ | Setup time, input data gpmc_d[15:0] valid before output clock gpmc_clk high | 2.3 | | 2.3 | | ns |
| F13 | $t_{h(clkH\text{-}dV)}$ | Hold time, input data gpmc_d[15:0] valid after output clock gpmc_clk high | 1.5 | | 1.5 | | ns |
| F21 | $t_{su(waitV\text{-}clkH)}$ | Setup time, input wait gpmc_waitx[2] valid before output clock gpmc_clk high | 2.3 | | 2.3 | | ns |
| F22 | $t_{h(clkH\text{-}waitV)}$ | Hold time, input wait gpmc_waitx[2] valid after output clock gpmc_clk high | 1.9 | | 1.9 | | ns |

(1)  See Section 4.3.4, *Processor Clocks*.

(2)  In gpmc_waitx, x is equal to 0, 1, 2, or 3.

**Table 6-4. GPMC/NOR Flash Switching Characteristics—Synchronous Mode[2] [18]**

| NO. | PARAMETER | | OPP100 | | OPP50 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| F0 | $1 / t_{c(clk)}$ | Frequency[15], output clock gpmc_clk | | 100 | | 100 | MHz |
| F1 | $t_{w(clkH)}$ | Typical pulse duration, output clock gpmc_clk high | 0.5P[12] | | 0.5P[12] | | ns |
| F1 | $t_{w(clkL)}$ | Typical pulse duration, output clock gpmc_clk low | 0.5P[12] | | 0.5P[12] | | ns |

**Table 6-4. GPMC/NOR Flash Switching Characteristics—Synchronous Mode[2] [18]  (continued)**

| NO. | PARAMETER | | OPP100 | | OPP50 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| | $t_{dc(clk)}$ | Duty cycle error, output clock gpmc_clk | −500 | 500 | −500 | 500 | ps |
| | $t_{J(clk)}$ | Jitter standard deviation[16], output clock gpmc_clk | | 33.33 | | 33.33 | ps |
| | $t_{R(clk)}$ | Rise time, output clock gpmc_clk | | 1.6 | | 1.6 | ns |
| | $t_{F(clk)}$ | Fall time, output clock gpmc_clk | | 1.6 | | 1.6 | ns |
| | $t_{R(do)}$ | Rise time, output data gpmc_d[15:0] | | 2 | | 2 | ns |
| | $t_{F(do)}$ | Fall time, output data gpmc_d[15:0] | | 2 | | 2 | ns |
| F2 | $t_{d(clkH-ncsV)}$ | Delay time, output clock gpmc_clk rising edge to output chip select gpmc_ncsx[11] transition | $F^{(6)} − 1.9$ | $F^{(6)} + 3.3$ | $F^{(6)} − 1.9$ | $F^{(6)} + 3.3$ | ns |
| F3 | $t_{d(clkH-ncsIV)}$ | Delay time, output clock gpmc_clk rising edge to output chip select gpmc_ncsx[11] invalid | $E^{(5)} − 1.9$ | $E^{(5)} + 3.3$ | $E^{(5)} − 1.9$ | $E^{(5)} + 3.3$ | ns |
| F4 | $t_{d(aV-clk)}$ | Delay time, output address gpmc_a[27:1] valid to output clock gpmc_clk first edge | $B^{(2)} − 4.1$ | $B^{(2)} + 2.1$ | $B^{(2)} − 4.1$ | $B^{(2)} + 2.1$ | ns |
| F5 | $t_{d(clkH-aIV)}$ | Delay time, output clock gpmc_clk rising edge to output address gpmc_a[27:1] invalid | −2.1 | | −2.1 | | ns |
| F6 | $t_{d(nbeV-clk)}$ | Delay time, output lower byte enable/command latch enable gpmc_nbe0_cle, output upper byte enable gpmc_nbe1 valid to output clock gpmc_clk first edge | $B^{(2)} − 1.2$ | $B^{(2)} + 2.2$ | $B^{(2)} − 1.2$ | $B^{(2)} + 2.2$ | ns |
| F7 | $t_{d(clkH-nbeIV)}$ | Delay time, output clock gpmc_clk rising edge to output lower byte enable/command latch enable gpmc_nbe0_cle, output upper byte enable gpmc_nbe1 invalid | $D^{(4)} − 2.2$ | $D^{(4)} + 1.2$ | $D^{(4)} − 2.2$ | $D^{(4)} + 1.2$ | ns |
| F8 | $t_{d(clkH-nadv)}$ | Delay time, output clock gpmc_clk rising edge to output address valid/address latch enable gpmc_nadv_ale transition | $G^{(7)} + 0.8$ | $G^{(7)} + 2.2$ | $G^{(7)} + 0.8$ | $G^{(7)} + 2.2$ | ns |
| F9 | $t_{d(clkH-nadvIV)}$ | Delay time, output clock gpmc_clk rising edge to output address valid/address latch enable gpmc_nadv_ale invalid | $D^{(4)} − 1.9$ | $D^{(4)} + 4.1$ | $D^{(4)} − 1.9$ | $D^{(4)} + 4.1$ | ns |
| F10 | $t_{d(clkH-noe)}$ | Delay time, output clock gpmc_clk rising edge to output enable gpmc_noe transition | $H^{(8)} − 2.1$ | $H^{(8)} + 2.1$ | $H^{(8)} − 2.1$ | $H^{(8)} + 2.1$ | ns |
| F11 | $t_{d(clkH-noeIV)}$ | Delay time, output clock gpmc_clk rising edge to output enable gpmc_noe invalid | $E^{(5)} − 2.1$ | $E^{(5)} + 2.1$ | $E^{(5)} − 2.1$ | $E^{(5)} + 2.1$ | ns |
| F14 | $t_{d(clkH-nwe)}$ | Delay time, output clock gpmc_clk rising edge to output write enable gpmc_nwe transition | $I^{(9)} − 1.9$ | $I^{(9)} + 4.1$ | $I^{(9)} − 1.9$ | $I^{(9)} + 4.1$ | ns |
| F15 | $t_{d(clkH-do)}$ | Delay time, output clock gpmc_clk rising edge to output data gpmc_d[15:0] transition | $J^{(10)} − 1.7$ | $J^{(10)} + 1.2$ | $J^{(10)} − 1.7$ | $J^{(10)} + 1.2$ | ns |
| F17 | $t_{d(clkH-nbe)}$ | Delay time, output clock gpmc_clk rising edge to output lower byte enable/command latch enable gpmc_nbe0_cle transition | $J^{(10)} − 2.2$ | $J^{(10)} + 1.2$ | $J^{(10)} − 2.2$ | $J^{(10)} + 1.2$ | ns |
| F18 | $t_{w(ncsV)}$ | Pulse duration, output chip select gpmc_ncsx[11] low — Read | $A^{(1)}$ | | $A^{(1)}$ | | ns |
| | | Pulse duration, output chip select gpmc_ncsx[11] low — Write | $A^{(1)}$ | | $A^{(1)}$ | | ns |
| F19 | $t_{w(nbeV)}$ | Pulse duration, output lower byte enable/command latch enable gpmc_nbe0_cle, output upper byte enable gpmc_nbe1 low — Read | $C^{(3)}$ | | $C^{(3)}$ | | ns |
| | | Pulse duration, output lower byte enable/command latch enable gpmc_nbe0_cle, output upper byte enable gpmc_nbe1 low — Write | $C^{(3)}$ | | $C^{(3)}$ | | ns |
| F20 | $t_{w(nadvV)}$ | Pulse duration, output address valid/address latch enable gpmc_nadv_ale low — Read | $K^{(13)}$ | | $K^{(13)}$ | | ns |
| | | Pulse duration, output address valid/address latch enable gpmc_nadv_ale low — Write | $K^{(13)}$ | | $K^{(13)}$ | | ns |
| F23 | $t_{d(clkH-iodir)}$ | Delay time, output clock gpmc_clk rising edge to output IO direction control gpmc_io_dir high (IN direction) | $H^{(8)} − 2.1$ | $H^{(8)} + 4.1$ | $H^{(8)} − 2.1$ | $H^{(8)} + 4.1$ | ns |
| F24 | $t_{d(clkH-iodirIV)}$ | Delay time, output clock gpmc_clk rising edge to output IO direction control gpmc_io_dir low (OUT direction) | $M^{(17)} − 2.1$ | $M^{(17)} + 4.1$ | $M^{(17)} − 2.1$ | $M^{(17)} + 4.1$ | ns |

(1) For single read: A = (CSRdOffTime – CSOnTime) * (TimeParaGranularity + 1) * GPMC_FCLK[14]
For burst read: A = (CSRdOffTime – CSOnTime + (n – 1) * PageBurstAccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK[14]
For burst write: A = (CSWrOffTime – CSOnTime + (n – 1) * PageBurstAccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK[14]
With n being the page burst access number.

(2) B = ClkActivationTime * GPMC_FCLK[14]

(3) For single read: C = RdCycleTime * (TimeParaGranularity + 1) * GPMC_FCLK [14]
For burst read: C = (RdCycleTime + (n – 1) * PageBurstAccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK[14]
For burst write: C = (WrCycleTime + (n – 1) * PageBurstAccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK[14]
With n being the page burst access number.

(4) For single read: D = (RdCycleTime – AccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK[14]
For burst read: D = (RdCycleTime – AccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK[14]
For burst write: D = (WrCycleTime – AccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK[14]

(5) For single read: E = (CSRdOffTime – AccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK[14]
For burst read: E = (CSRdOffTime – AccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK[14]
For burst write: E = (CSWrOffTime – AccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK[14]

(6) For nCS falling edge (CS activated):
  – Case GpmcFCLKDivider = 0:
    – F = 0.5 * CSExtraDelay * GPMC_FCLK[14]
  – Case GpmcFCLKDivider = 1:
    – F = 0.5 * CSExtraDelay * GPMC_FCLK[14] if (ClkActivationTime and CSOnTime are odd) or (ClkActivationTime and CSOnTime are even)
    – F = (1 + 0.5 * CSExtraDelay) * GPMC_FCLK[14] otherwise
  – Case GpmcFCLKDivider = 2:
    – F = 0.5 * CSExtraDelay * GPMC_FCLK[14] if ((CSOnTime – ClkActivationTime) is a multiple of 3)
    – F = (1 + 0.5 * CSExtraDelay) * GPMC_FCLK[14] if ((CSOnTime – ClkActivationTime – 1) is a multiple of 3)
    – F = (2 + 0.5 * CSExtraDelay) * GPMC_FCLK[14] if ((CSOnTime – ClkActivationTime – 2) is a multiple of 3)

(7) For ADV falling edge (ADV activated):
  – Case GpmcFCLKDivider = 0:
    – G = 0.5 * ADVExtraDelay * GPMC_FCLK[14]
  – Case GpmcFCLKDivider = 1:
    – G = 0.5 * ADVExtraDelay * GPMC_FCLK[14] if (ClkActivationTime and ADVOnTime are odd) or (ClkActivationTime and ADVOnTime are even)
    – G = (1 + 0.5 * ADVExtraDelay) * GPMC_FCLK[14] otherwise
  – Case GpmcFCLKDivider = 2:
    – G = 0.5 * ADVExtraDelay * GPMC_FCLK[14] if ((ADVOnTime – ClkActivationTime) is a multiple of 3)
    – G = (1 + 0.5 * ADVExtraDelay) * GPMC_FCLK[14] if ((ADVOnTime – ClkActivationTime – 1) is a multiple of 3)
    – G = (2 + 0.5 * ADVExtraDelay) * GPMC_FCLK[14] if ((ADVOnTime – ClkActivationTime – 2) is a multiple of 3)

  For ADV rising edge (ADV deactivated) in Reading mode:
  – Case GpmcFCLKDivider = 0:
    – G = 0.5 * ADVExtraDelay * GPMC_FCLK[14]
  – Case GpmcFCLKDivider = 1:
    – G = 0.5 * ADVExtraDelay * GPMC_FCLK[14] if (ClkActivationTime and ADVRdOffTime are odd) or (ClkActivationTime and ADVRdOffTime are even)
    – G = (1 + 0.5 * ADVExtraDelay) * GPMC_FCLK[14] otherwise
  – Case GpmcFCLKDivider = 2:
    – G = 0.5 * ADVExtraDelay * GPMC_FCLK[14] if ((ADVRdOffTime – ClkActivationTime) is a multiple of 3)
    – G = (1 + 0.5 * ADVExtraDelay) * GPMC_FCLK[14] if ((ADVRdOffTime – ClkActivationTime – 1) is a multiple of 3)
    – G = (2 + 0.5 * ADVExtraDelay) * GPMC_FCLK[14] if ((ADVRdOffTime – ClkActivationTime – 2) is a multiple of 3)

  For ADV rising edge (ADV deactivated) in Writing mode:
  – Case GpmcFCLKDivider = 0:
    – G = 0.5 * ADVExtraDelay * GPMC_FCLK[14]
  – Case GpmcFCLKDivider = 1:
    – G = 0.5 * ADVExtraDelay * GPMC_FCLK[14] if (ClkActivationTime and ADVWrOffTime are odd) or (ClkActivationTime and ADVWrOffTime are even)
    – G = (1 + 0.5 * ADVExtraDelay) * GPMC_FCLK[14] otherwise
  – Case GpmcFCLKDivider = 2:
    – G = 0.5 * ADVExtraDelay * GPMC_FCLK[14] if ((ADVWrOffTime – ClkActivationTime) is a multiple of 3)
    – G = (1 + 0.5 * ADVExtraDelay) * GPMC_FCLK[14] if ((ADVWrOffTime – ClkActivationTime – 1) is a multiple of 3)
    – G = (2 + 0.5 * ADVExtraDelay) * GPMC_FCLK[14] if ((ADVWrOffTime – ClkActivationTime – 2) is a multiple of 3)

(8) For OE falling edge (OE activated) / IO DIR rising edge (Data Bus input direction):
  – Case GpmcFCLKDivider = 0: o H = 0.5 * OEExtraDelay * GPMC_FCLK[14]
  – Case GpmcFCLKDivider = 1:
    – H = 0.5 * OEExtraDelay * GPMC_FCLK[14] if (ClkActivationTime and OEOnTime are odd) or (ClkActivationTime and OEOnTime are even)
    – H = (1 + 0.5 * OEExtraDelay) * GPMC_FCLK[14] otherwise
  – Case GpmcFCLKDivider = 2:
    – H = 0.5 * OEExtraDelay * GPMC_FCLK[14] if ((OEOnTime – ClkActivationTime) is a multiple of 3)

- H = (1 + 0.5 * OEExtraDelay) * GPMC_FCLK[14] if ((OEOnTime − ClkActivationTime − 1) is a multiple of 3)
- H = (2 + 0.5 * OEExtraDelay) * GPMC_FCLK[14] if ((OEOnTime − ClkActivationTime − 2) is a multiple of 3)

For OE rising edge (OE deactivated):
- Case GpmcFCLKDivider = 0:
  - H = 0.5 * OEExtraDelay * GPMC_FCLK[14]
- Case GpmcFCLKDivider = 1:
  - H = 0.5 * OEExtraDelay * GPMC_FCLK[14] if (ClkActivationTime and OEOffTime are odd) or (ClkActivationTime and OEOffTime are even)
  - H = (1 + 0.5 * OEExtraDelay) * GPMC_FCLK[14] otherwise
- Case GpmcFCLKDivider = 2:
  - H = 0.5 * OEExtraDelay * GPMC_FCLK[14] if ((OEOffTime − ClkActivationTime) is a multiple of 3)
  - H = (1 + 0.5 * OEExtraDelay) * GPMC_FCLK[14] if ((OEOffTime − ClkActivationTime − 1) is a multiple of 3)
  - H = (2 + 0.5 * OEExtraDelay) * GPMC_FCLK[14] if ((OEOffTime − ClkActivationTime − 2) is a multiple of 3)

(9) For WE falling edge (WE activated):
- Case GpmcFCLKDivider = 0:
  - I = 0.5 * WEExtraDelay * GPMC_FCLK[14]
- Case GpmcFCLKDivider = 1:
  - I = 0.5 * WEExtraDelay * GPMC_FCLK[14] if (ClkActivationTime and WEOnTime are odd) or (ClkActivationTime and WEOnTime are even)
  - I = (1 + 0.5 * WEExtraDelay) * GPMC_FCLK[14] otherwise
- Case GpmcFCLKDivider = 2:
  - I = 0.5 * WEExtraDelay * GPMC_FCLK[14] if ((WEOnTime − ClkActivationTime) is a multiple of 3)
  - I = (1 + 0.5 * WEExtraDelay) * GPMC_FCLK[14] if ((WEOnTime − ClkActivationTime − 1) is a multiple of 3)
  - I = (2 + 0.5 * WEExtraDelay) * GPMC_FCLK[14] if ((WEOnTime − ClkActivationTime − 2) is a multiple of 3)

For WE rising edge (WE deactivated):
- Case GpmcFCLKDivider = 0:
  - I = 0.5 * WEExtraDelay * GPMC_FCLK [14]
- Case GpmcFCLKDivider = 1:
  - I = 0.5 * WEExtraDelay * GPMC_FCLK[14] if (ClkActivationTime and WEOffTime are odd) or (ClkActivationTime and WEOffTime are even)
  - I = (1 + 0.5 * WEExtraDelay) * GPMC_FCLK[14] otherwise
- Case GpmcFCLKDivider = 2:
  - I = 0.5 * WEExtraDelay * GPMC_FCLK[14] if ((WEOffTime − ClkActivationTime) is a multiple of 3)
  - I = (1 + 0.5 * WEExtraDelay) * GPMC_FCLK[14] if ((WEOffTime − ClkActivationTime − 1) is a multiple of 3)
  - I = (2 + 0.5 * WEExtraDelay) * GPMC_FCLK[14] if ((WEOffTime − ClkActivationTime − 2) is a multiple of 3)

(10) J = GPMC_FCLK[14]

(11) In gpmc_ncsx, x is equal to 0, 1, 2, 3, 4, 5, 6, or 7. In gpmc_waitx, x is equal to 0, 1, 2, or 3.

(12) P = gpmc_clk period in ns

(13) For read: K = (ADVRdOffTime − ADVOnTime) * (TimeParaGranularity + 1) * GPMC_FCLK[14]
For write: K = (ADVWrOffTime − ADVOnTime) * (TimeParaGranularity + 1) * GPMC_FCLK[14]

(14) GPMC_FCLK is general-purpose memory controller internal functional clock period in ns.

(15) Related to the gpmc_clk output clock maximum and minimum frequencies programmable in the GPMC module by setting the GPMC_CONFIG1_CSx configuration register bit field GpmcFCLKDivider.

(16) The jitter probability density can be approximated by a Gaussian function.

(17) M = (RdCycleTime − AccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK[14]
Above M parameter expression is given as one example of GPMC programming. IO DIR signal will go from IN to OUT after both RdCycleTime and BusTurnAround completion. Behavior of IO direction signal does depend on kind of successive Read/Write accesses performed to Memory and multiplexed or nonmultiplexed memory addressing scheme, bus keeping feature enabled or not. IO DIR behaviour is automatically handled by GPMC controller. For a full description of the gpmc_io_dir feature, see the *AM/DM37x Multimedia Device Technical Reference Manual* (literature number SPRUGN4).

(18) See Section 4.3.4, *Processor Clocks.*
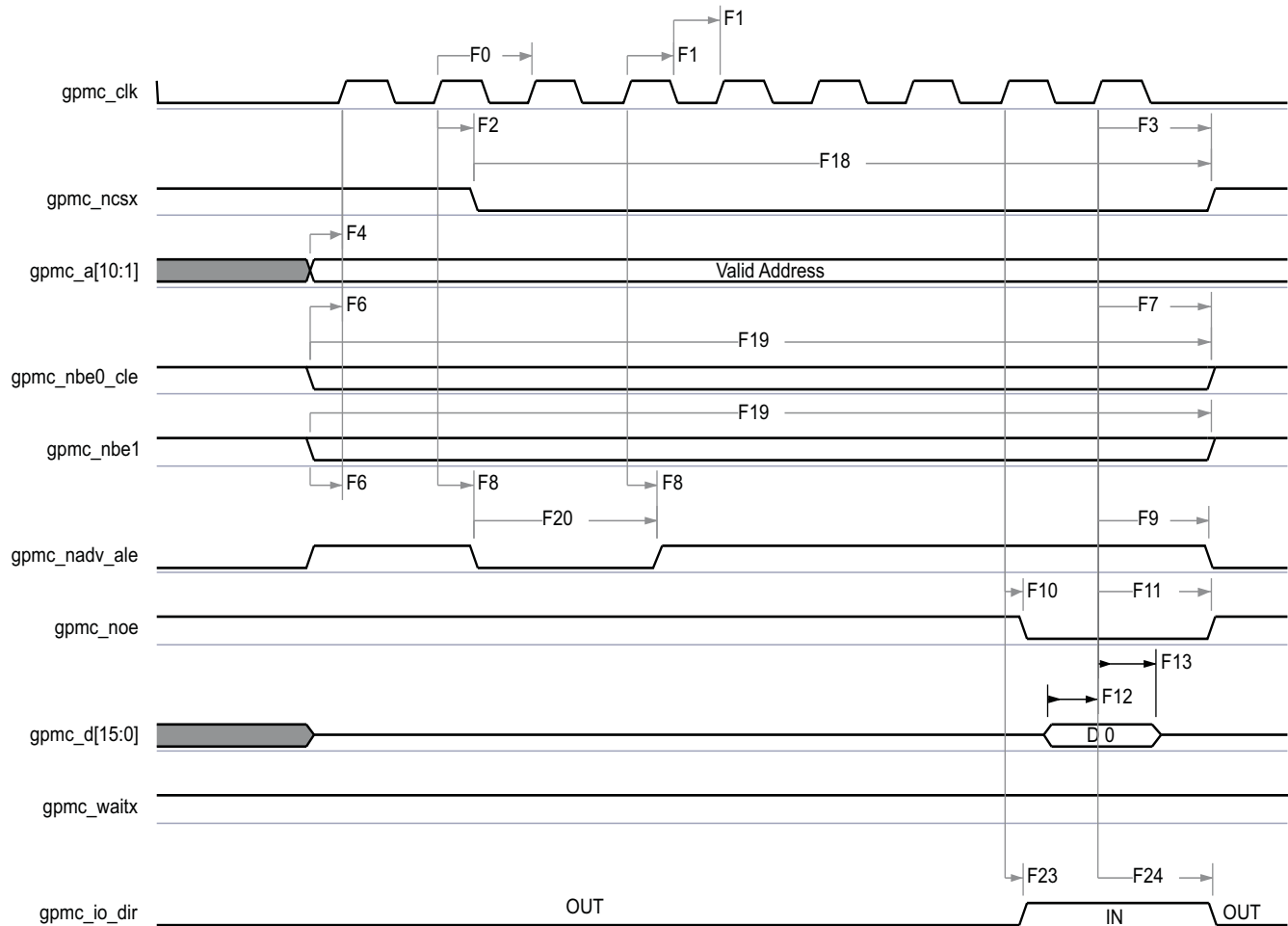
SWPS038-014

(1) In gpmc_ncsx, x is equal to 0, 1, 2, 3, 4, 5, 6, or 7.

(2) In gpmc_waitx, x is equal to 0, 1, 2, or 3.

**Figure 6-2. GPMC/NOR Flash—Synchronous Single Read—(GpmcFCLKDivider = 0)**
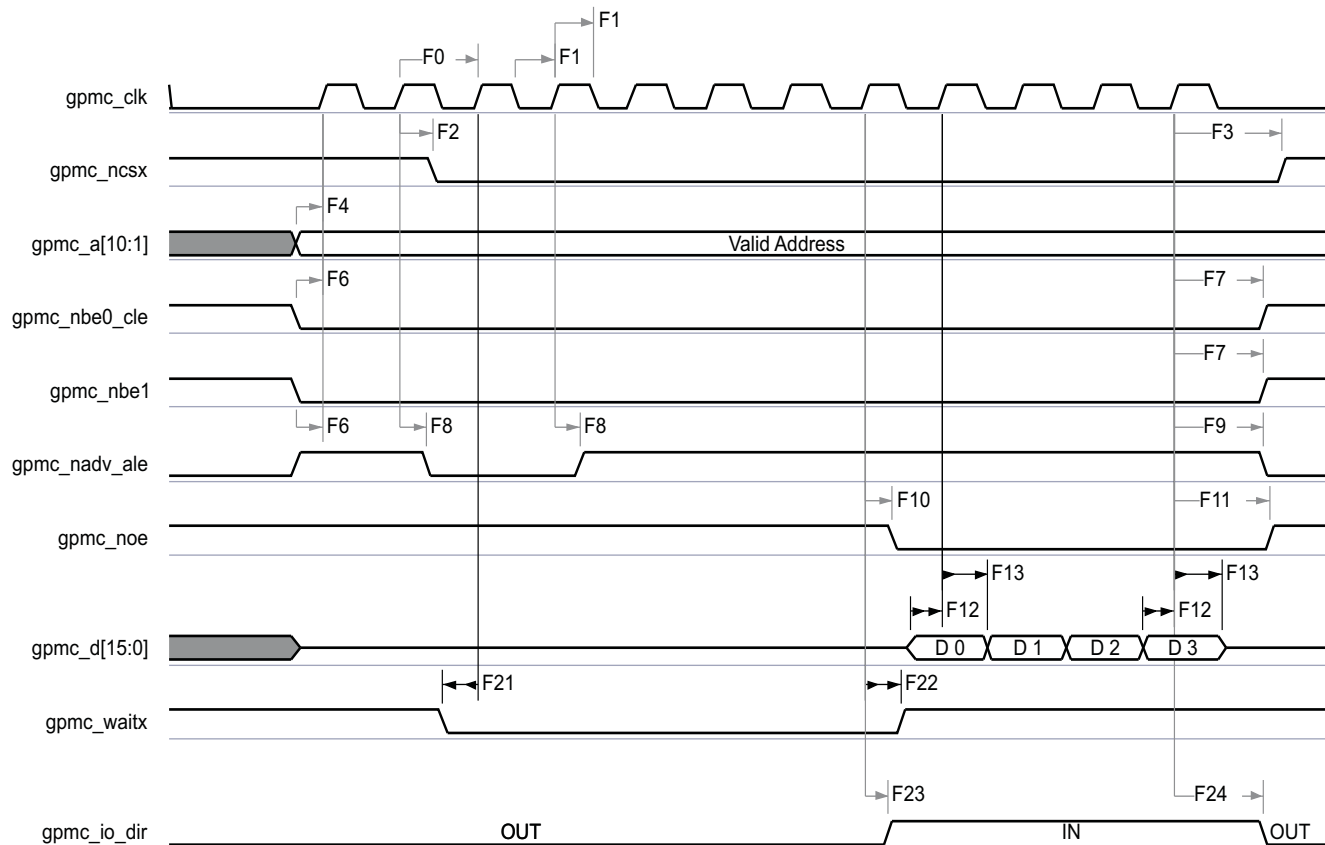
SWPS038-015

(1)  In gpmc_ncsx, x is equal to 0, 1, 2, 3, 4, 5, 6, or 7.
(2)  In gpmc_waitx, x is equal to 0, 1, 2, or 3.

**Figure 6-3. GPMC/NOR Flash—Synchronous Burst Read—4x16-bit (GpmcFCLKDivider = 0)**
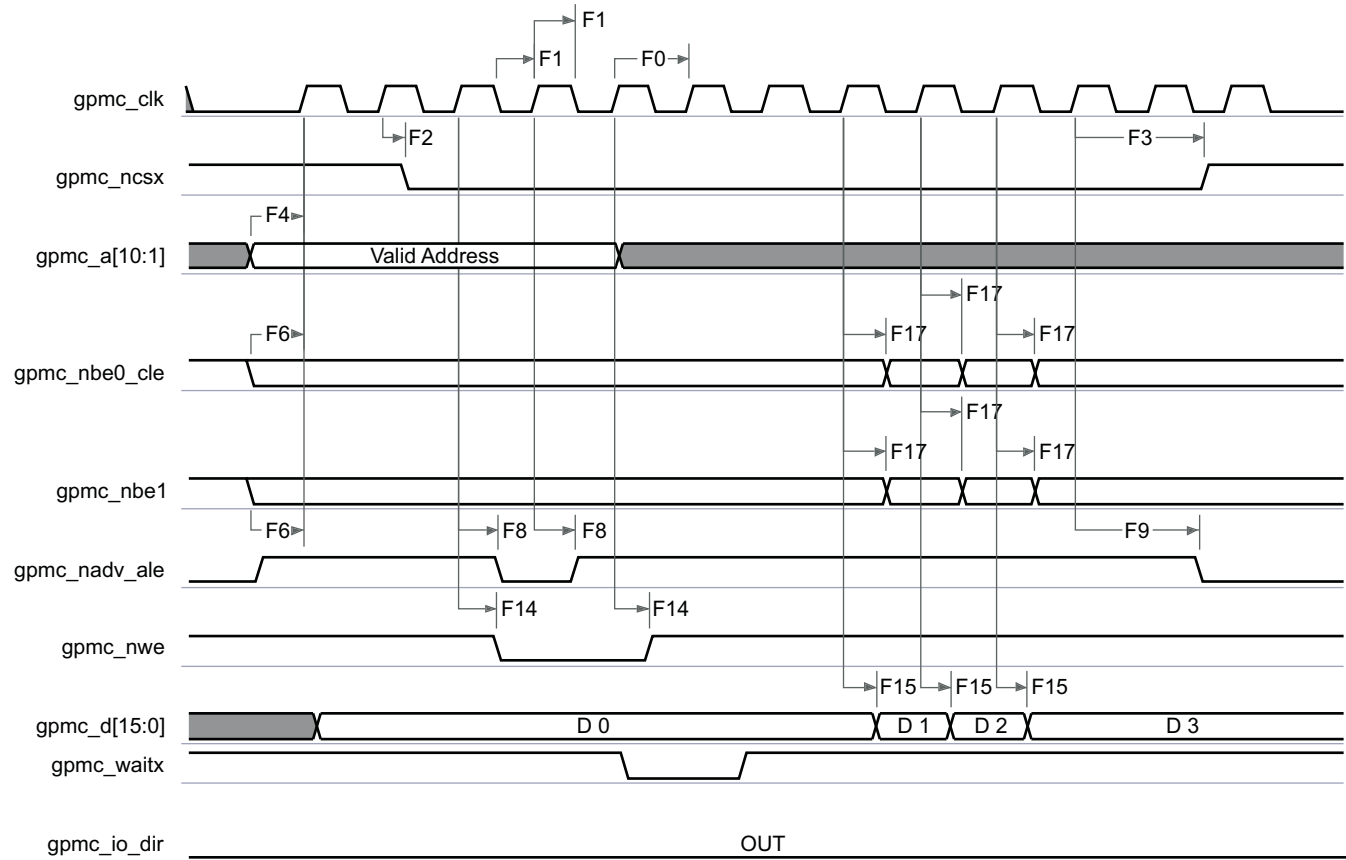
SWPS038-016

(1) In gpmc_ncsx, x is equal to 0, 1, 2, 3, 4, 5, 6, or 7.

(2) In gpmc_waitx, x is equal to 0, 1, 2, or 3.

**Figure 6-4. GPMC/NOR Flash—Synchronous Burst Write—(GpmcFCLKDivider > 0)**
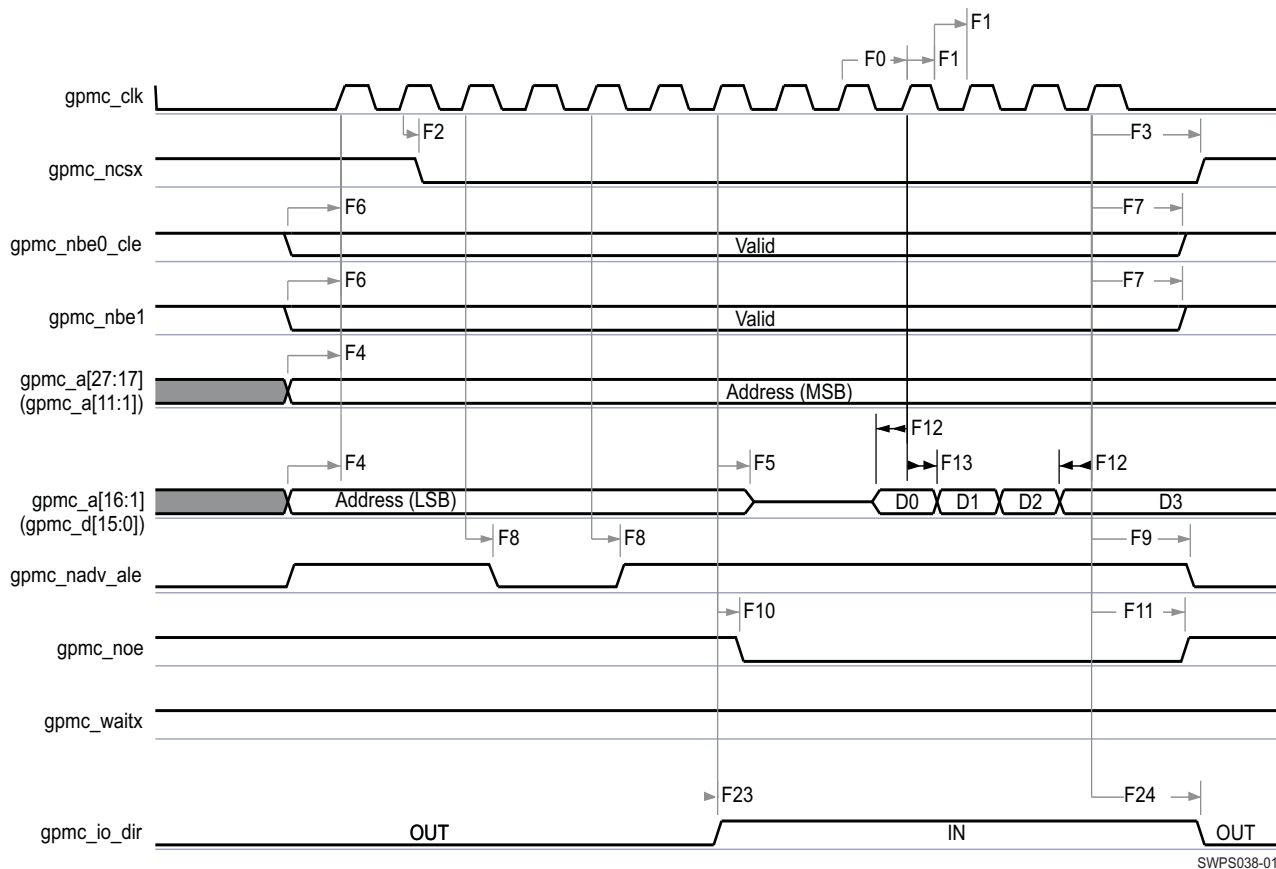
(1)   In gpmc_ncsx, x is equal to 0, 1, 2, 3, 4, 5, 6, or 7.
(2)   In gpmc_waitx, x is equal to 0, 1, 2, or 3.

**Figure 6-5. GPMC/Multiplexed NOR Flash—Synchronous Burst Read**
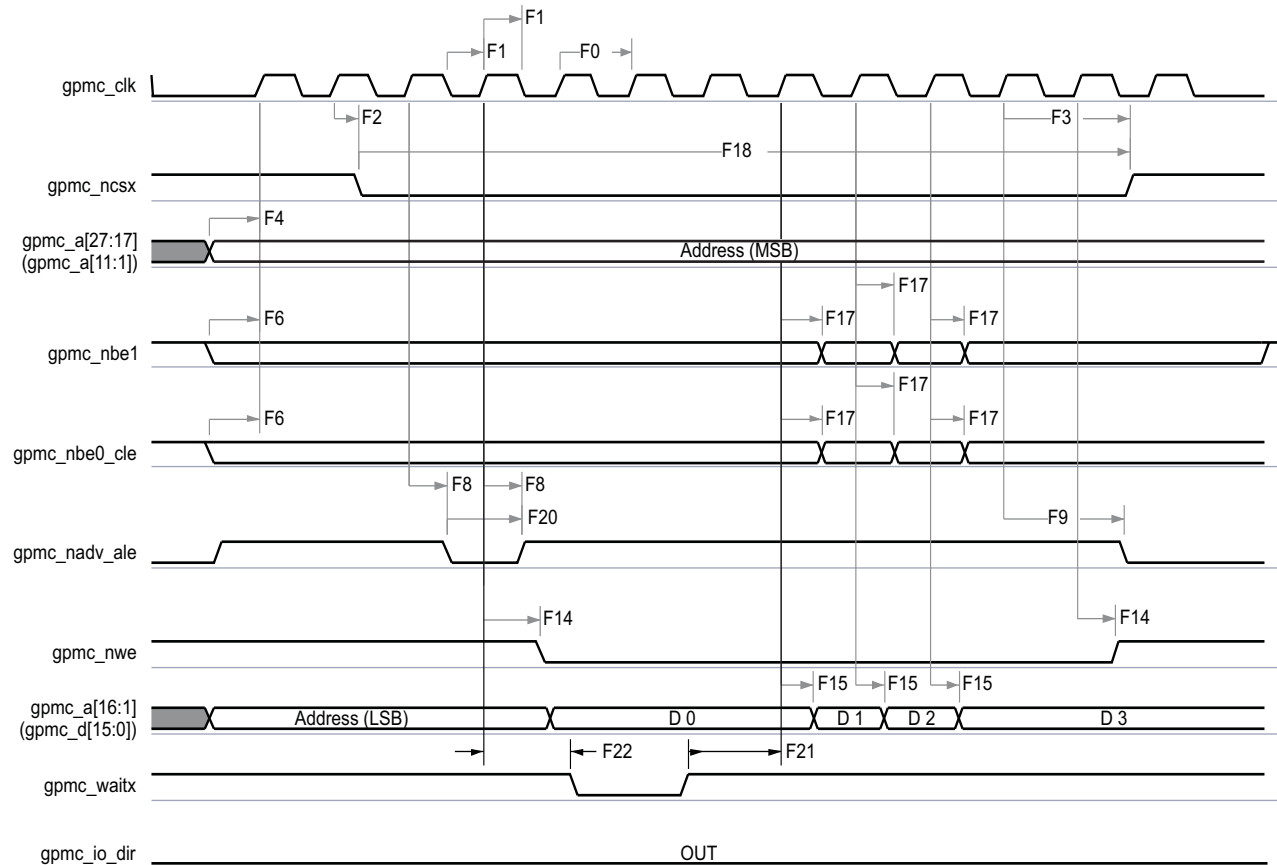
(1)   In gpmc_ncsx, x is equal to 0, 1, 2, 3, 4, 5, 6, or 7.

(2)   In gpmc_waitx, x is equal to 0, 1, 2, or 3.

**Figure 6-6. GPMC/Multiplexed NOR Flash—Synchronous Burst Write**

### 6.4.1.2 GPMC/NOR Flash—Asynchronous Mode

Table 6-6 and Table 6-7 assume testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-7 through Figure 6-12).

#### Table 6-5. GPMC/NOR Flash Timing Conditions—Asynchronous Mode

| TIMING CONDITION PARAMETER | | VALUE | UNIT |
|---|---|---|---|
| **Input Conditions** | | | |
| $t_R$ | Input signal rise time | 1.8 | ns |
| $t_F$ | Input signal fall time | 1.8 | ns |
| **Output Conditions** | | | |
| $C_{LOAD}$ | Output load capacitance[1] | 16 | pF |

(1) The load setting of the IO buffer: LB0 = 0.

#### Table 6-6. GPMC/NOR Flash Internal Timing Parameters—Asynchronous Mode[1] [2] [4]

| NO. | PARAMETER | OPP100 | | OPP50 | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| FI1 | Delay time, output data gpmc_d[15:0] generation from internal functional clock GPMC_FCLK[3] | | 6.6 | | 7.0 | ns |
| FI2 | Delay time, input data gpmc_d[15:0] capture from internal functional clock GPMC_FCLK[3] | | 4.4 | | 7.0 | ns |
| FI3 | Delay time, output chip select gpmc_ncsx generation from internal functional clock GPMC_FCLK[3] | | 6.5 | | 7.0 | ns |
| FI4 | Delay time, output address gpmc_a[27:1] generation from internal functional clock GPMC_FCLK[3] | | 7.6 | | 7.0 | ns |
| FI5 | Delay time, output address gpmc_a[27:1] valid from internal functional clock GPMC_FCLK[3] | | 7.6 | | 7.0 | ns |
| FI6 | Delay time, output lower-byte enable/command latch enable gpmc_nbe0_cle, output upper-byte enable gpmc_nbe1 generation from internal functional clock GPMC_FCLK[3] | | 6.5 | | 7.0 | ns |
| FI7 | Delay time, output enable gpmc_noe generation from internal functional clock GPMC_FCLK[3] | | 5.8 | | 7.0 | ns |
| FI8 | Delay time, output write enable gpmc_nwe generation from internal functional clock GPMC_FCLK[3] | | 7.0 | | 7.0 | ns |
| FI9 | Skew, internal functional clock GPMC_FCLK[3] | | 100 | | 170 | ps |
| FI10 | Delay time, IO direction generation from internal functional clock GPMC_FCLK[3] | | 6.3 | | 7.0 | ps |

(1) The internal parameters table must be used to calculate data access time stored in the corresponding CS register bit field.

(2) Internal parameters are referred to the GPMC functional internal clock which is not provided externally.

(3) GPMC_FCLK is general-purpose memory controller internal functional clock.

(4) See Section 4.3.4, *Processor Clocks*.

## Table 6-7. GPMC/NOR Flash Timing Requirements—Asynchronous Mode[7]

| NO. | PARAMETER | | OPP100 | | OPP50 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| FA5[1] | $t_{acc(d)}$ | Data access time | | H[5] | | H[5] | ns |
| FA20[3] | $t_{acc1-pgmode(d)}$ | Page mode successive data access time | | P[4] | | P[4] | ns |
| FA21[2] | $t_{acc2-pgmode(d)}$ | Page mode first data access time | | H[5] | | H[5] | ns |

(1) The FA5 parameter illustrates the amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input data is internally sampled by active functional clock edge. FA5 value must be stored inside the AccessTime register bit field.

(2) The FA21 parameter illustrates amount of time required to internally sample first input page data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA21 functional clock cycles, first input page data is internally sampled by active functional clock edge. FA21 value must be stored inside the AccessTime register bit field.

(3) The FA20 parameter illustrates amount of time required to internally sample successive input page data. It is expressed in number of GPMC functional clock cycles. After each access to input page data, next input page data is internally sampled by active functional clock edge after FA20 functional clock cycles. The FA20 value must be stored in the PageBurstAccessTime register bit field.

(4) P = PageBurstAccessTime * (TimeParaGranularity + 1) * GPMC_FCLK[6]

(5) H = AccessTime * (TimeParaGranularity + 1) * GPMC_FCLK[6]

(6) GPMC_FCLK is general-purpose memory controller internal functional clock period in ns.

(7) See Section 4.3.4, *Processor Clocks*.

## Table 6-8. GPMC/NOR Flash Switching Characteristics—Asynchronous Mode[16]

| NO. | PARAMETER | | OPP100 | | OPP50 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| | $t_{R(d)}$ | Rise time, output data gpmc_d[15:0] | | 2 | | 2 | ns |
| | $t_{F(d)}$ | Fall time, output data gpmc_d[15:0] | | 2 | | 2 | ns |
| FA0 | $t_{w(nbeV)}$ | Pulse duration, output lower-byte enable/command latch enable gpmc_nbe0_cle, output upper-byte enable gpmc_nbe1 valid time | Read | N[12] | | N[12] | | ns |
| | | | Write | N[12] | | N[12] | | |
| FA1 | $t_{w(ncsV)}$ | Pulse duration, output chip select gpmc_ncsx[13] low | Read | A[1] | | A[1] | | ns |
| | | | Write | A[1] | | A[1] | | |
| FA3 | $t_{d(ncsV-nadvIV)}$ | Delay time, output chip select gpmc_ncsx[13] valid to output address valid/address latch enable gpmc_nadv_ale invalid | Read | B[2] − 0.2 | B[2] + 2.0 | B[2] − 0.2 | B[2] + 2.6 | ns |
| | | | Write | B[2] − 0.2 | B[2] + 2.0 | B[2] − 0.2 | B[2] + 2.6 | |
| FA4 | $t_{d(ncsV-noeIV)}$ | Delay time, output chip select gpmc_ncsx[13] valid to output enable gpmc_noe invalid (Single read) | | C[3] − 0.2 | C[3] + 2.0 | C[3] − 0.2 | C[3] + 2.6 | ns |
| FA9 | $t_{d(aV-ncsV)}$ | Delay time, output address gpmc_a[27:1] valid to output chip select gpmc_ncsx[13] valid | | J[9] − 0.2 | J[9] + 2.0 | J[9] − 0.2 | J[9] + 2.6 | ns |
| FA10 | $t_{d(nbeV-ncsV)}$ | Delay time, output lower-byte enable/command latch enable gpmc_nbe0_cle, output upper-byte enable gpmc_nbe1 valid to output chip select gpmc_ncsx[13] valid | | J[9] − 0.2 | J[9] + 2.0 | J[9] − 0.2 | J[9] + 2.6 | ns |
| FA12 | $t_{d(ncsV-nadvV)}$ | Delay time, output chip select gpmc_ncsx[13] valid to output address valid/address latch enable gpmc_nadv_ale valid | | K[10] − 0.2 | K[10] + 2.0 | K[10] − 0.2 | K[10] + 2.6 | ns |
| FA13 | $t_{d(ncsV-noeV)}$ | Delay time, output chip select gpmc_ncsx[13] valid to output enable gpmc_noe valid | | L[11] − 0.2 | L[11] + 2.0 | L[11] − 0.2 | L[11] + 2.6 | ns |
| FA14 | $t_{d(ncsV-iodir)}$ | Delay time, output chip select gpmc_ncsx[13] valid to output IO direction control gpmc_io_dir high | | L[11] − 0.2 | L[11] + 2.0 | L[11] − 0.2 | L[11] + 2.6 | ns |
| FA15 | $t_{d(ncsV-iodir)}$ | Delay time, output chip select gpmc_ncsx[13] valid to output IO direction control gpmc_io_dir low | | M[14] − 0.2 | M[14] + 2.0 | M[14] − 0.2 | M[14] + 2.6 | ns |

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## Table 6-8. GPMC/NOR Flash Switching Characteristics—Asynchronous Mode[16]  (continued)

| NO. | PARAMETER | | OPP100 | | OPP50 | | UNIT |
|-----|-----------|---|--------|--------|--------|--------|------|
| | | | MIN | MAX | MIN | MAX | |
| FA16 | $t_{w(aIV)}$ | Pulse durationm output address gpmc_a[26:1] invalid between 2 successive R/W accesses | $G^{(7)}$ | | $G^{(7)}$ | | ns |
| FA18 | $t_{d(ncsV-noeIV)}$ | Delay time, output chip select gpmc_ncsx[13] valid to output enable gpmc_noe invalid (Burst read) | $I^{(8)} - 0.2$ | $I^{(8)} + 2.0$ | $I^{(8)} - 0.2$ | $I^{(8)} + 2.6$ | ns |
| FA20 | $t_{w(aV)}$ | Pulse duration, output address gpmc_a[27:1] valid – 2nd, 3rd, and 4th accesses | $D^{(4)}$ | | $D^{(4)}$ | | ns |
| FA25 | $t_{d(ncsV-nweV)}$ | Delay time, output chip select gpmc_ncsx[13] valid to output write enable gpmc_nwe valid | $E^{(5)} - 0.2$ | $E^{(5)} + 2.0$ | $E^{(5)} - 0.2$ | $E^{(5)} + 2.6$ | ns |
| FA27 | $t_{d(ncsV-nweIV)}$ | Delay time, output chip select gpmc_ncsx[13] valid to output write enable gpmc_nwe invalid | $F^{(6)} - 0.2$ | $F^{(6)} + 2.0$ | $F^{(6)} - 0.2$ | $F^{(6)} + 2.6$ | ns |
| FA28 | $t_{d(nweV-dV)}$ | Delay time, output write enable gpmc_ nwe valid to output data gpmc_d[15:0] valid | | 2.0 | | 2.6 | ns |
| FA29 | $t_{d(dV-ncsV)}$ | Delay time, output data gpmc_d[15:0] valid to output chip select gpmc_ncsx[13] valid | $J^{(9)} - 0.2$ | $J^{(9)} + 2.0$ | $J^{(9)} - 0.2$ | $J^{(9)} + 2.6$ | ns |
| FA37 | $t_{d(noeV-aIV)}$ | Delay time, output enable gpmc_noe valid to output address gpmc_a[16:1]_d[15:0] phase end | | 2.0 | | 2.6 | ns |

(1)  For single read: A = (CSRdOffTime – CSOnTime) * (TimeParaGranularity + 1) * GPMC_FCLK[15]
     For single write: A = (CSWrOffTime – CSOnTime) * (TimeParaGranularity + 1) * GPMC_FCLK[15]
     For burst read: A = (CSRdOffTime – CSOnTime + (n – 1) * PageBurstAccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK[15]
     For burst write: A = (CSWrOffTime – CSOnTime + (n – 1) * PageBurstAccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK[15]
     with n being the page burst access number

(2)  For reading: B = ((ADVRdOffTime – CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (ADVExtraDelay – CSExtraDelay)) * GPMC_FCLK[15]
     For writing: B = ((ADVWrOffTime – CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (ADVExtraDelay – CSExtraDelay)) * GPMC_FCLK[15]

(3)  C = ((OEOffTime – CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (OEExtraDelay – CSExtraDelay)) * GPMC_FCLK[15]

(4)  D = PageBurstAccessTime * (TimeParaGranularity + 1) * GPMC_FCLK[15]

(5)  E = ((WEOnTime – CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (WEExtraDelay – CSExtraDelay)) * GPMC_FCLK[15]

(6)  F = ((WEOffTime – CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (WEExtraDelay – CSExtraDelay)) * GPMC_FCLK[15]

(7)  G = Cycle2CycleDelay * GPMC_FCLK[15]

(8)  I = ((OEOffTime + (n – 1) * PageBurstAccessTime – CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (OEExtraDelay – CSExtraDelay)) * GPMC_FCLK[15]

(9)  J = (CSOnTime * (TimeParaGranularity + 1) + 0.5 * CSExtraDelay) * GPMC_FCLK[15]

(10)  K = ((ADVOnTime – CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (ADVExtraDelay – CSExtraDelay)) * GPMC_FCLK[15]

(11)  L = ((OEOnTime – CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (OEExtraDelay – CSExtraDelay)) * GPMC_FCLK[15]

(12)  For single read: N = RdCycleTime * (TimeParaGranularity + 1) * GPMC_FCLK[15]
     For single write: N = WrCycleTime * (TimeParaGranularity + 1) * GPMC_FCLK[15]
     For burst read: N = (RdCycleTime + (n – 1) * PageBurstAccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK[15]
     For burst write: N = (WrCycleTime + (n – 1) * PageBurstAccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK[15]

(13)  In gpmc_ncsx, x is equal to 0, 1, 2, 3, 4, 5, 6, or 7.

(14)  M = ((RdCycleTime – CSOnTime) * (TimeParaGranularity + 1) – 0.5 * CSExtraDelay) * GPMC_FCLK[15]
     Above M parameter expression is given as one example of GPMC programming. IO DIR signal will go from IN to OUT after both RdCycleTime and BusTurnAround completion. Behavior of IO direction signal does depend on kind of successive Read/Write accesses performed to Memory and multiplexed or nonmultiplexed memory addressing scheme, bus keeping feature enabled or not. IO DIR behaviour is automatically handled by GPMC controller. For a full description of the gpmc_io_dir feature, see the *AM/DM37x Multimedia Device Technical Reference Manual* (literature number SPRUGN4).

(15)  GPMC_FCLK is general-purpose memory controller internal functional clock period in ns.

(16)  See Section 4.3.4, *Processor Clocks*.
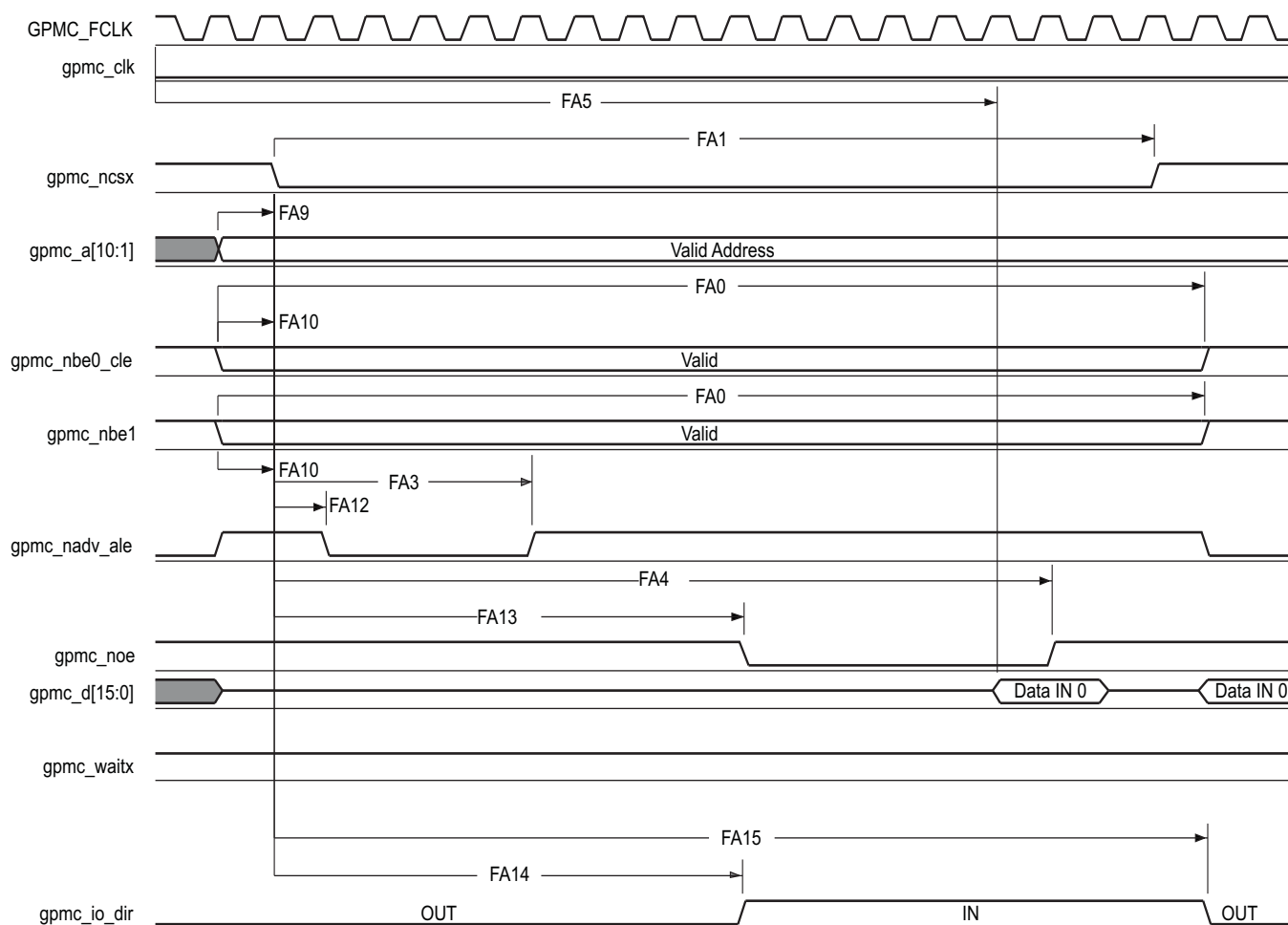
SWPS038-019

(1)  In gpmc_ncsx, x is equal to 0, 1, 2, 3, 4, 5, 6, or 7. In gpmc_waitx, x is equal to 0, 1, 2, or 3.

(2)  FA5 parameter illustrates amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input data will be internally sampled by active functional clock edge. FA5 value must be stored inside AccessTime register bits field.

(3)  GPMC_FCLK is an internal clock (GPMC functional clock) not provided externally.

**Figure 6-7. GPMC / NOR Flash—Asynchronous Read—Single Word**
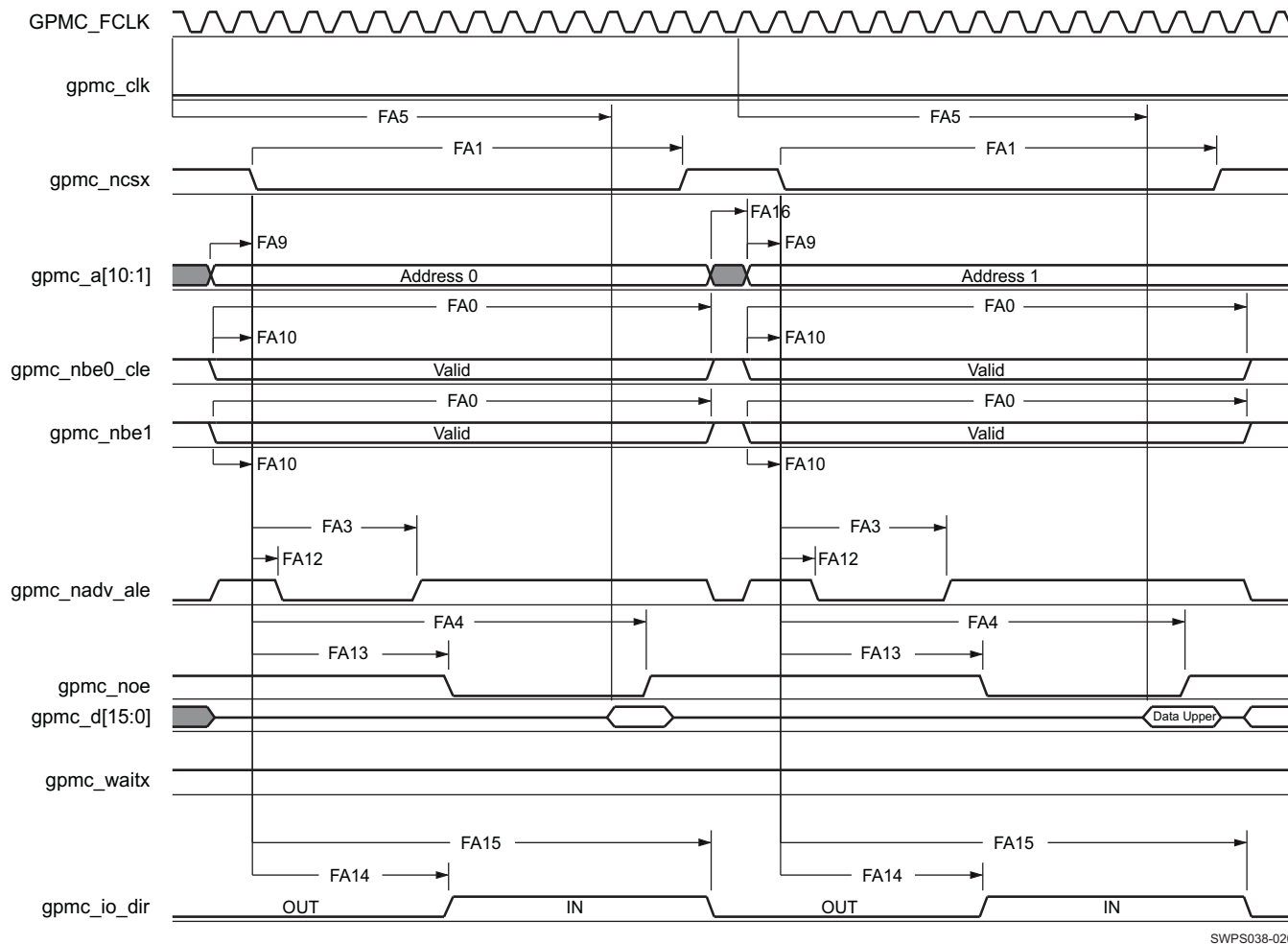
(1) In gpmc_ncsx, x is equal to 0, 1, 2, 3, 4, 5, 6, or 7. In gpmc_waitx, x is equal to 0, 1, 2, or 3.

(2) FA5 parameter illustrates amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input data will be internally sampled by active functional clock edge. FA5 value must be stored inside AccessTime register bits field.

(3) GPMC_FCLK is an internal clock (GPMC functional clock) not provided externally.

**Figure 6-8. GPMC / NOR Flash—Asynchronous Read—32-bit**

SWPS038-021
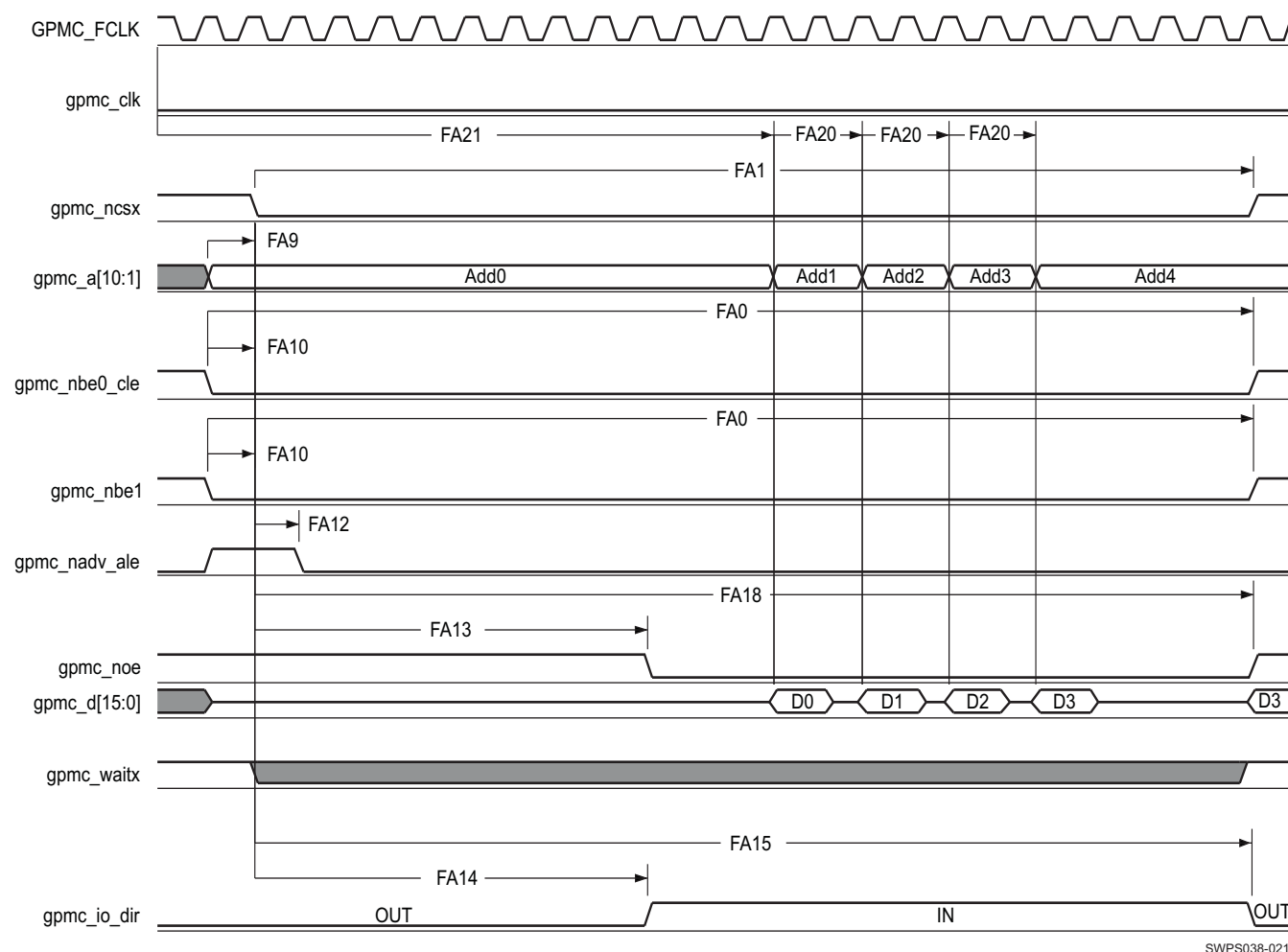
(1) In gpmc_ncsx, x is equal to 0, 1, 2, 3, 4, 5, 6, or 7. In gpmc_waitx, x is equal to 0, 1, 2, or 3.

(2) FA21 parameter illustrates amount of time required to internally sample first input page data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA21 functional clock cycles, first input page data will be internally sampled by active functional clock edge. FA21 calculation must be stored inside AccessTime register bits field.

(3) FA20 parameter illustrates amount of time required to internally sample successive input page data. It is expressed in number of GPMC functional clock cycles. After each access to input page data, next input page data will be internally sampled by active functional clock edge after FA20 functional clock cycles. FA20 is also the duration of address phases for successive input page data (excluding first input page data). FA20 value must be stored in PageBurstAccessTime register bits field.

(4) GPMC_FCLK is an internal clock (GPMC functional clock) not provided externally.

**Figure 6-9. GPMC / NOR Flash—Asynchronous Read—Page Mode 4x16-bit**
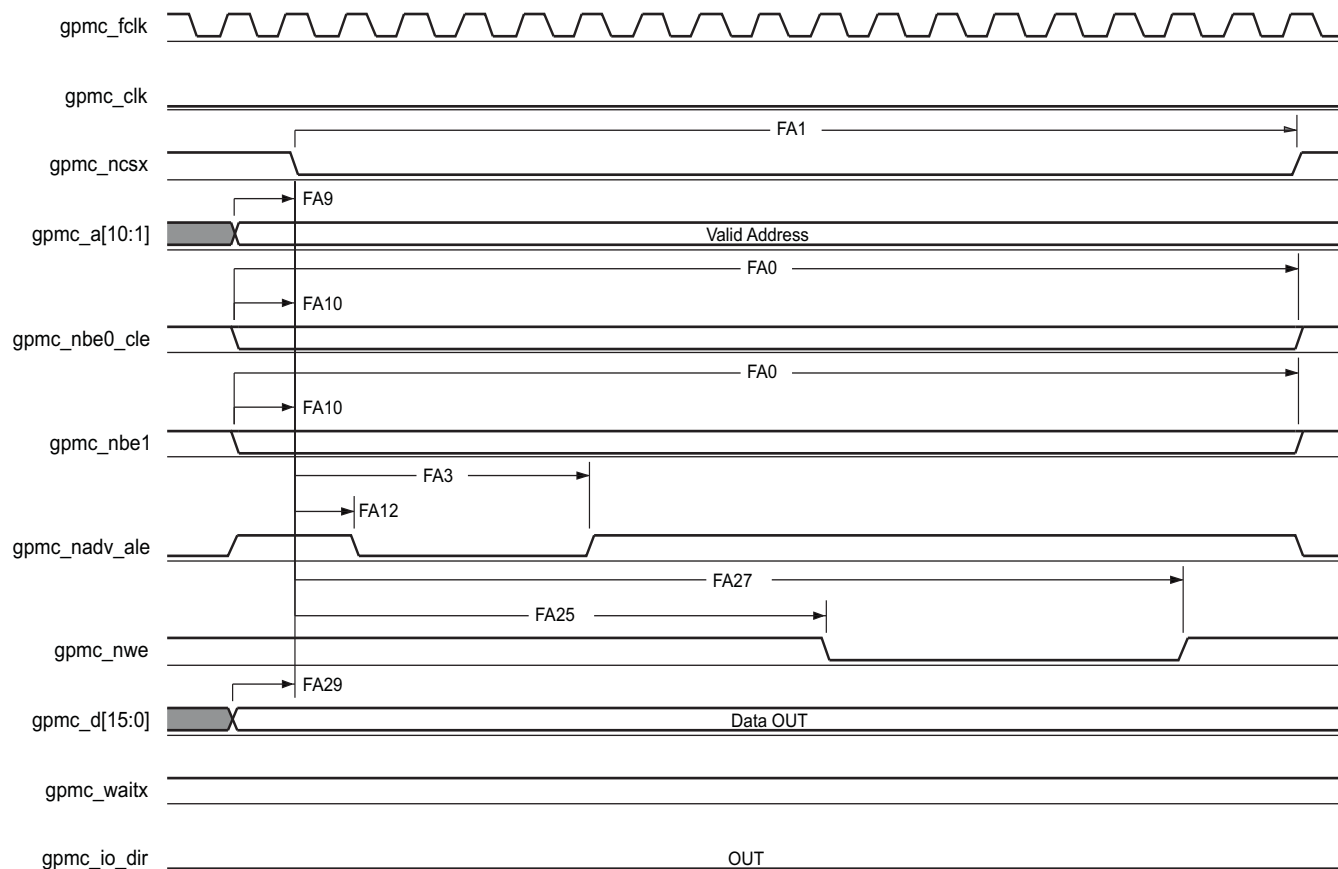
SWPS038-022

(1)   In gpmc_ncsx, x is equal to 0, 1, 2, 3, 4, 5, 6, or 7. In gpmc_waitx, x is equal to 0, 1, 2, or 3.

**Figure 6-10. GPMC / NOR Flash—Asynchronous Write—Single Word**
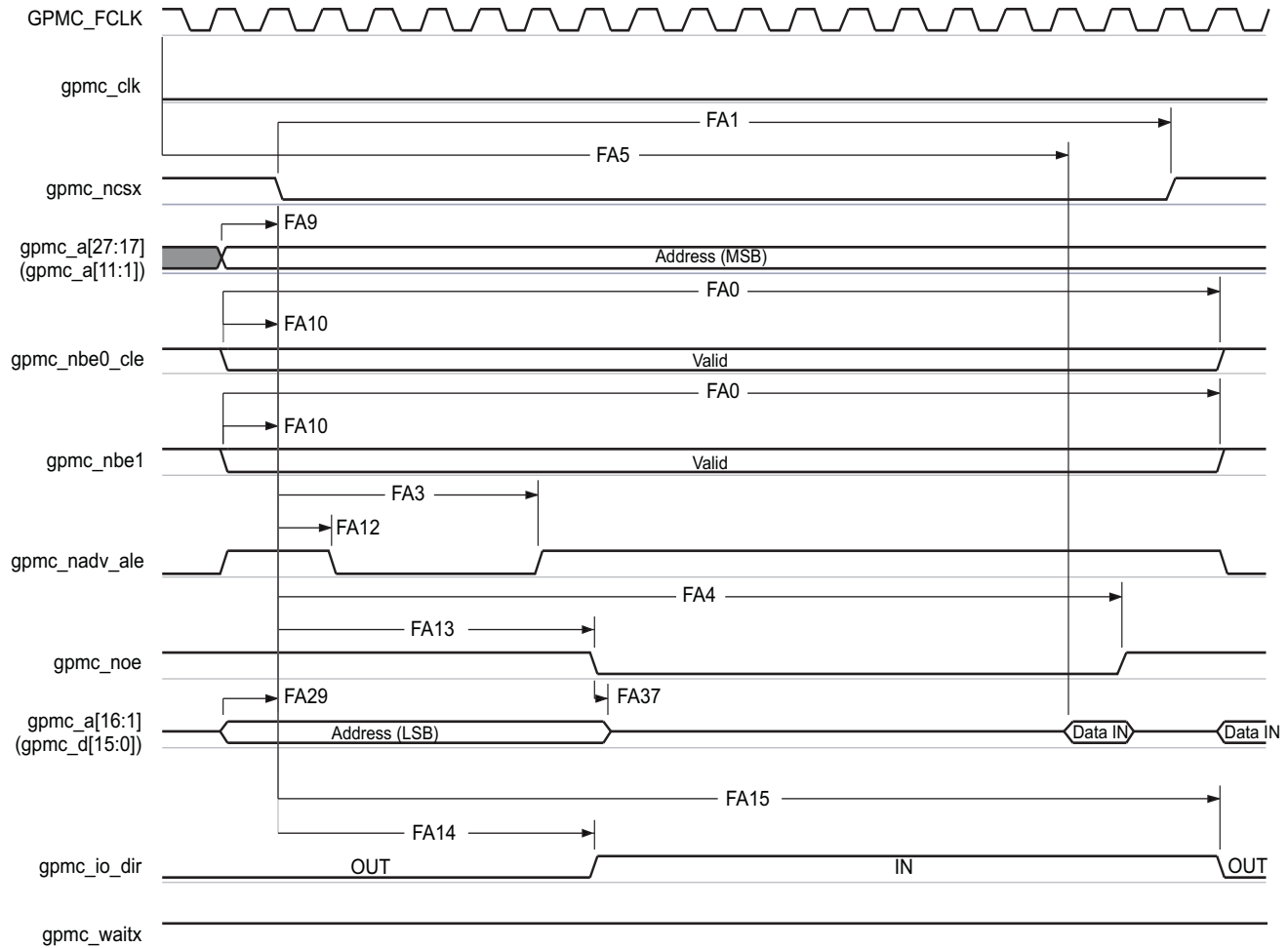
SWPS038-023

(1) In gpmc_ncsx, x is equal to 0, 1, 2, 3, 4, 5, 6, or 7. In gpmc_waitx, x is equal to 0, 1, 2, or 3.

(2) FA5 parameter illustrates amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input data will be internally sampled by active functional clock edge. FA5 value must be stored inside AccessTime register bits field.

(3) GPMC_FCLK is an internal clock (GPMC functional clock) not provided externally.

**Figure 6-11. GPMC / Multiplexed NOR Flash—Asynchronous Read—Single Word**
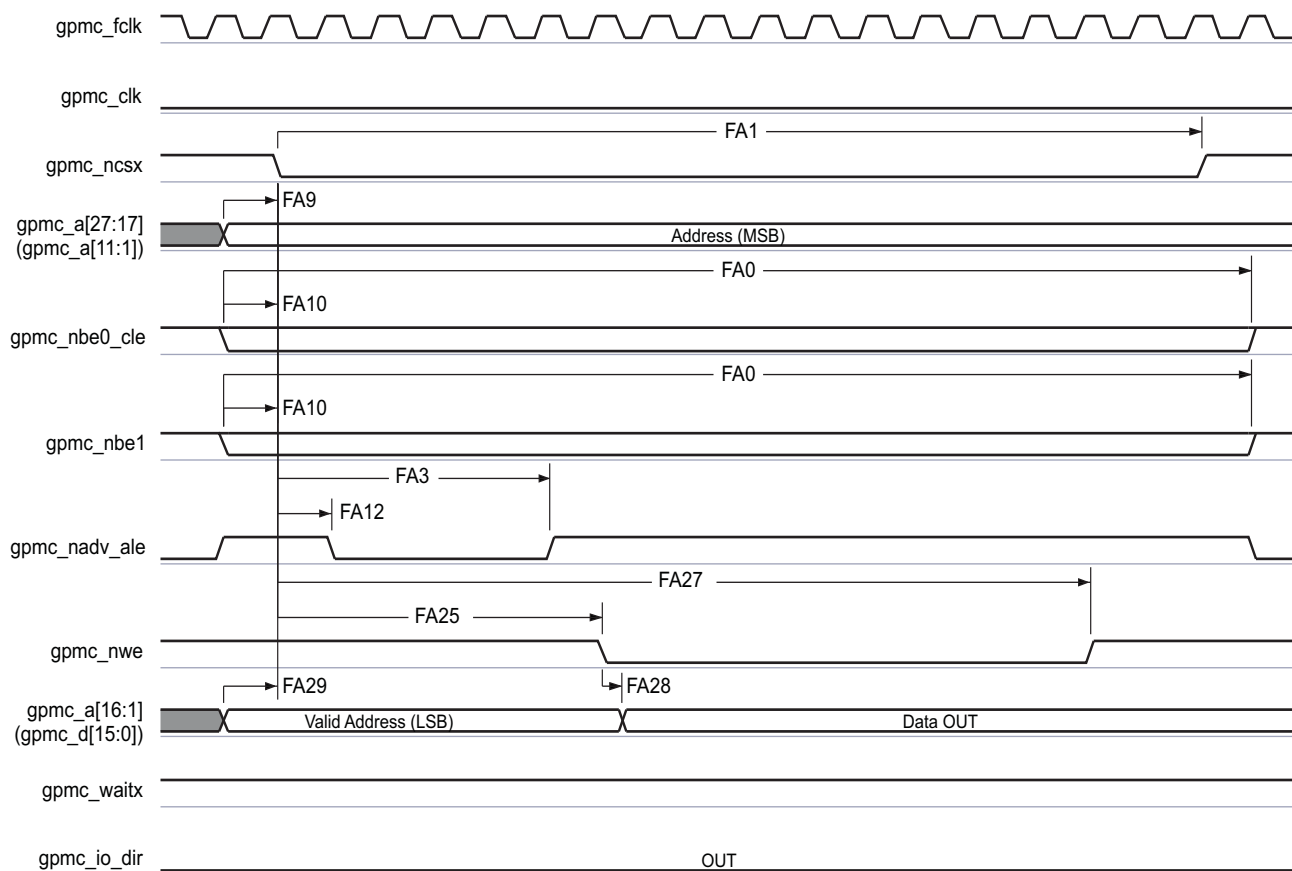
SWPS038-024

(1)    In gpmc_ncsx, x is equal to 0, 1, 2, 3, 4, 5, 6, or 7. In gpmc_waitx, x is equal to 0, 1, 2, or 3.

**Figure 6-12. GPMC / Multiplexed NOR Flash—Asynchronous Write—Single Word**

### 6.4.1.3 GPMC/NAND Flash—Asynchronous Mode

Table 6-10 and Table 6-11 assume testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-13 through Figure 6-16).

**Table 6-9. GPMC/NAND Flash Timing Conditions—Asynchronous Mode**

| TIMING CONDITION PARAMETER | | VALUE | UNIT |
|---|---|---|---|
| **Input Conditions** | | | |
| $t_R$ | Input signal rise time | 1.8 | ns |
| $t_F$ | Input signal fall time | 1.8 | ns |
| **Output Conditions** | | | |
| $C_{LOAD}$ | Output load capacitance[1] | 16 | pF |

(1) The load setting of the IO buffer: LB0 = 0.

**Table 6-10. GPMC/NAND Flash Internal Timing Parameters—Asynchronous Mode[1] [2] [4]**

| NO. | PARAMETER | OPP100 | | OPP50 | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| GNFI1 | Delay time, output data gpmc_d[15:0] generation from internal functional clock GPMC_FCLK[3] | | 6.5 | | 9.1 | ns |
| GNFI2 | Delay time, input data gpmc_d[15:0] capture from internal functional clock GPMC_FCLK[3] | | 4.0 | | 5.6 | ns |
| GNFI3 | Delay time, output chip select gpmc_ncsx generation from internal functional clock GPMC_FCLK[3] | | 6.5 | | 9.1 | ns |
| GNFI4 | Delay time, output address valid/address latch enable gpmc_nadv_ale generation from internal functional clock GPMC_FCLK[3] | | 6.5 | | 9.1 | ns |
| GNFI5 | Delay time, output lower-byte enable/command latch enable gpmc_nbe0_cle generation from internal functional clock GPMC_FCLK[3] | | 6.5 | | 9.1 | ns |
| GNFI6 | Delay time, output enable gpmc_noe generation from internal functional clock GPMC_FCLK[3] | | 6.5 | | 9.1 | ns |
| GNFI7 | Delay time, output write enable gpmc_nwe generation from internal functional clock GPMC_FCLK[3] | | 6.5 | | 9.1 | ns |
| GNFI8 | Skew, functional clock GPMC_FCLK[3] | | 100 | | 170 | ps |

(1) Internal parameters table must be used to calculate data access time stored in the corresponding CS register bit field.

(2) Internal parameters are referred to the GPMC functional internal clock which is not provided externally.

(3) GPMC_FCLK is general-purpose memory controller internal functional clock.

(4) See Section 4.3.4, *Processor Clocks.*

**Table 6-11. GPMC/NAND Flash Timing Requirements—Asynchronous Mode[4]**

| NO. | PARAMETER | | OPP100 | | OPP50 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| GNF12[1] | $t_{acc(d)}$ | Access time, input data gpmc_d[15:0] | | J[2] | | J[2] | ns |

(1) The GNF12 parameter illustrates the amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of the read cycle and after GNF12 functional clock cycles, input data is internally sampled by the active functional clock edge. The GNF12 value must be stored inside AccessTime register bit field.

(2) J = AccessTime * (TimeParaGranularity + 1) * GPMC_FCLK[3]

(3) GPMC_FCLK is general-purpose memory controller internal functional clock period in ns.

(4) See Section 4.3.4, *Processor Clocks.*

## Table 6-12. GPMC/NAND Flash Switching Characteristics—Asynchronous Mode[15]

| NO. | PARAMETER | | OPP100 | | OPP50 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| | $t_{R(d)}$ | Rise time, output data gpmc_d[15:0] | | 2 | | 2 | ns |
| | $t_{F(d)}$ | Fall time, output data gpmc_d[15:0] | | 2 | | 2 | ns |
| GNF0 | $t_{w(nweV)}$ | Pulse duration, output write enable gpmc_nwe valid | $A^{(1)}$ | | $A^{(1)}$ | | ns |
| GNF1 | $t_{d(ncsV-nweV)}$ | Delay time, output chip select gpmc_ncsx[13] valid to output write enable gpmc_nwe valid | $B^{(2)} - 0.2$ | $B^{(2)} + 2.0$ | $B^{(2)} - 0.2$ | $B^{(2)} + 2.6$ | ns |
| GNF2 | $t_{w(cleH-nweV)}$ | Delay time, output lower-byte enable/command latch enable gpmc_nbe0_cle high to output write enable gpmc_nwe valid | $C^{(3)} - 0.2$ | $C^{(3)} + 2.0$ | $C^{(3)} - 0.2$ | $C^{(3)} + 2.6$ | ns |
| GNF3 | $t_{w(nweV-dV)}$ | Delay time, output data gpmc_d[15:0] valid to output write enable gpmc_nwe valid | $D^{(4)} - 0.2$ | $D^{(4)} + 2.0$ | $D^{(4)} - 0.2$ | $D^{(4)} + 2.6$ | ns |
| GNF4 | $t_{w(nweIV-dIV)}$ | Delay time, output write enable gpmc_nwe invalid to output data gpmc_d[15:0] invalid | $E^{(5)} - 0.2$ | $E^{(5)} + 2.0$ | $E^{(5)} - 0.2$ | $E^{(5)} + 2.6$ | ns |
| GNF5 | $t_{w(nweIV-cleIV)}$ | Delay time, output write enable gpmc_nwe invalid to output lower-byte enable/command latch enable gpmc_nbe0_cle invalid | $F^{(6)} - 0.2$ | $F^{(6)} + 2.0$ | $F^{(6)} - 0.2$ | $F^{(6)} + 2.6$ | ns |
| GNF6 | $t_{w(nweIV-ncsIV)}$ | Delay time, output write enable gpmc_nwe invalid to output chip select gpmc_ncsx[13] invalid | $G^{(7)} - 0.2$ | $G^{(7)} + 2.0$ | $G^{(7)} - 0.2$ | $G^{(7)} + 2.6$ | ns |
| GNF7 | $t_{w(aleH-nweV)}$ | Delay time, output address valid/address latch enable gpmc_nadv_ale high to output write enable gpmc_nwe valid | $C^{(3)} - 0.2$ | $C^{(3)} + 2.0$ | $C^{(3)} - 0.2$ | $C^{(3)} + 2.6$ | ns |
| GNF8 | $t_{w(nweIV-aleIV)}$ | Delay time, output write enable gpmc_nwe invalid to output address valid/address latch enable gpmc_nadv_ale invalid | $F^{(6)} - 0.2$ | $F^{(6)} + 2.0$ | $F^{(6)} - 0.2$ | $F^{(6)} + 2.6$ | ns |
| GNF9 | $t_{c(nwe)}$ | Cycle time, write | $H^{(8)}$ | | $H^{(8)}$ | | ns |
| GNF10 | $t_{d(ncsV-noeV)}$ | Delay time, output chip select gpmc_ncsx[13] valid to output enable gpmc_noe valid | $I^{(9)} - 0.2$ | $I^{(9)} + 2.0$ | $I^{(9)} - 0.2$ | $I^{(9)} + 2.6$ | ns |
| GNF13 | $t_{w(noeV)}$ | Pulse duration, output enable gpmc_noe valid | $K^{(10)}$ | | $K^{(10)}$ | | ns |
| GNF14 | $t_{c(noe)}$ | Cycle time, read | $L^{(11)}$ | | $L^{(11)}$ | | ns |
| GNF15 | $t_{w(noeIV-ncsIV)}$ | Delay time, output enable gpmc_noe invalid to output chip select gpmc_ncsx[13] invalid | $M^{(12)} - 0.2$ | $M^{(12)} + 2.0$ | $M^{(12)} - 0.2$ | $M^{(12)} + 2.6$ | ns |

(1)  A = (WEOffTime – WEOnTime) * (TimeParaGranularity + 1) * GPMC_FCLK[14]

(2)  B = ((WEOnTime – CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (WEExtraDelay – CSExtraDelay)) * GPMC_FCLK[14]

(3)  C = ((WEOnTime – ADVOnTime) * (TimeParaGranularity + 1) + 0.5 * (WEExtraDelay – ADVExtraDelay)) * GPMC_FCLK[14]

(4)  D = (WEOnTime * (TimeParaGranularity + 1) + 0.5 * WEExtraDelay) * GPMC_FCLK[14]

(5)  E = ((WrCycleTime – WEOffTime) * (TimeParaGranularity + 1) – 0.5 * WEExtraDelay) * GPMC_FCLK[14]

(6)  F = ((ADVWrOffTime – WEOffTime) * (TimeParaGranularity + 1) + 0.5 * (ADVExtraDelay – WEExtraDelay)) * GPMC_FCLK[14]

(7)  G = ((CSWrOffTime – WEOffTime) * (TimeParaGranularity + 1) + 0.5 * (CSExtraDelay – WEExtraDelay)) * GPMC_FCLK[14]

(8)  H = WrCycleTime * (1 + TimeParaGranularity) * GPMC_FCLK[14]

(9)  I = ((OEOnTime – CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (OEExtraDelay – CSExtraDelay)) * GPMC_FCLK[14]

(10)  K = (OEOffTime – OEOnTime) * (1 + TimeParaGranularity) * GPMC_FCLK[14]

(11)  L = RdCycleTime * (1 + TimeParaGranularity) * GPMC_FCLK[14]

(12)  M = ((CSRdOffTime – OEOffTime) * (TimeParaGranularity + 1) + 0.5 * (CSExtraDelay – OEExtraDelay)) * GPMC_FCLK[14]

(13)  In gpmc_ncsx, x is equal to 0, 1, 2, 3, 4, 5, 6, or 7.

(14)  GPMC_FCLK is general-purpose memory controller internal functional clock period in ns.

(15)  See Section 4.3.4, *Processor Clocks*.
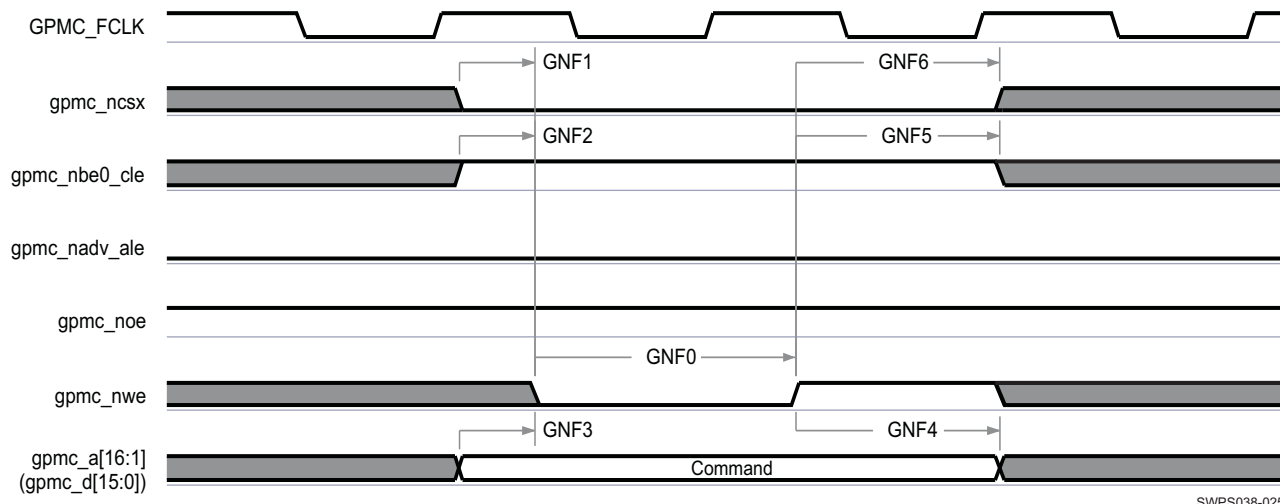
(1)  In gpmc_ncsx, x is equal to 0, 1, 2, 3, 4, 5, 6, or 7.

**Figure 6-13. GPMC / NAND Flash—Command Latch Cycle**
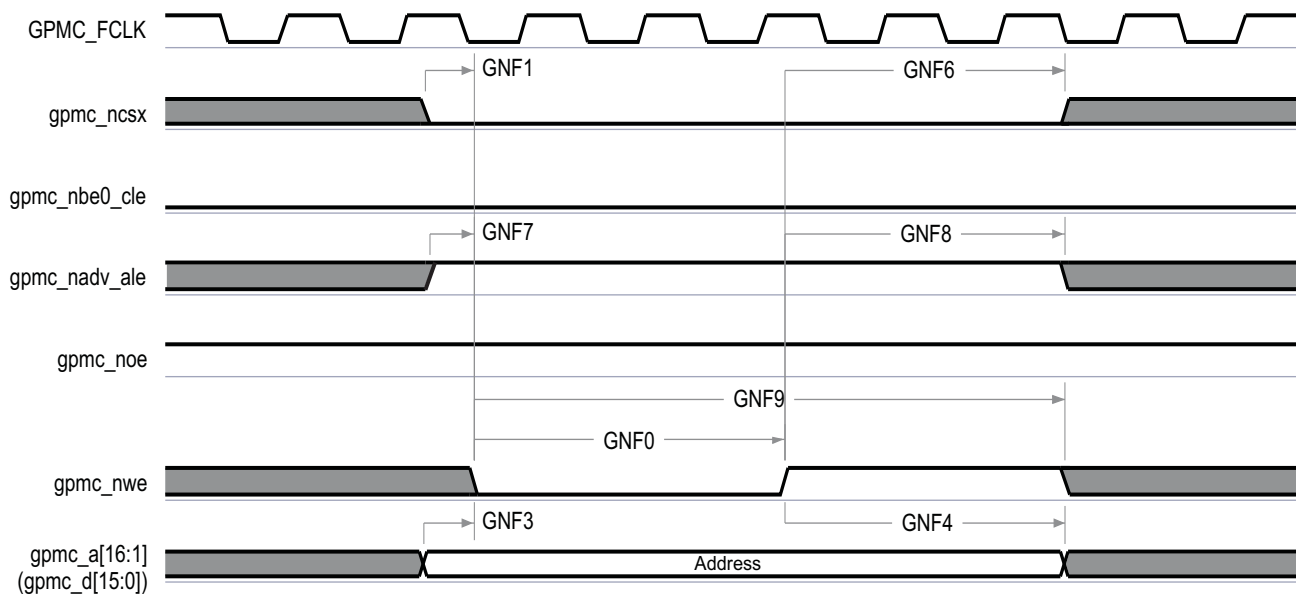


(1)  In gpmc_ncsx, x is equal to 0, 1, 2, 3, 4, 5, 6, or 7.

**Figure 6-14. GPMC / NAND Flash—Address Latch Cycle**

SWPS038-027
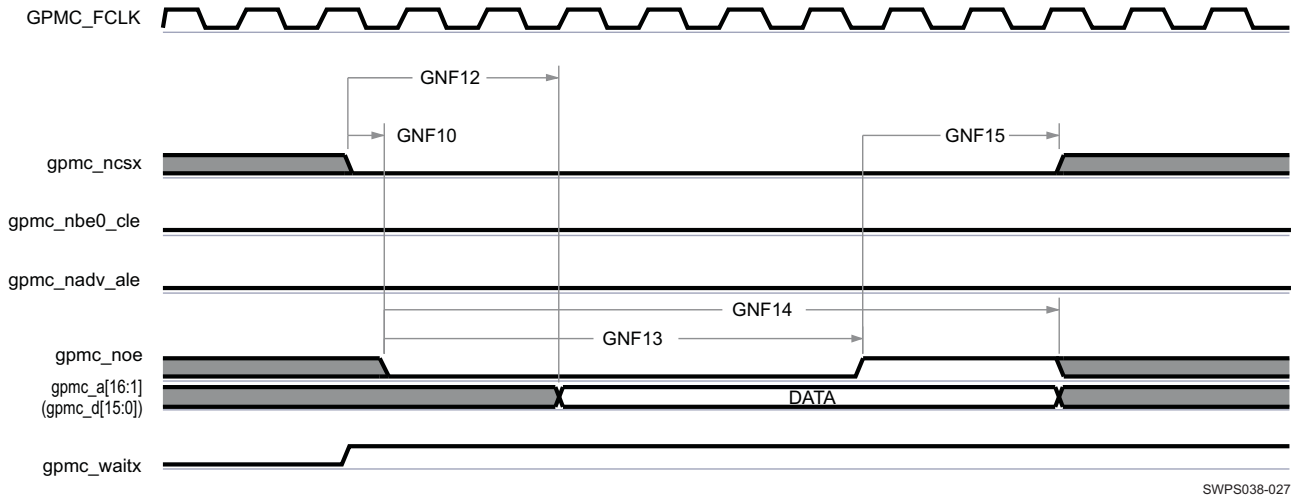
(1) GNF12 parameter illustrates amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after GNF12 functional clock cycles, input data will be internally sampled by active functional clock edge. GNF12 value must be stored inside AccessTime register bits field.

(2) GPMC_FCLK is an internal clock (GPMC functional clock) not provided externally.

(3) In gpmc_ncsx, x is equal to 0, 1, 2, 3, 4, 5, 6, or 7. In gpmc_waitx, x is equal to 0, 1, 2, or 3.

**Figure 6-15. GPMC / NAND Flash—Data Read Cycle**



SWPS038-028
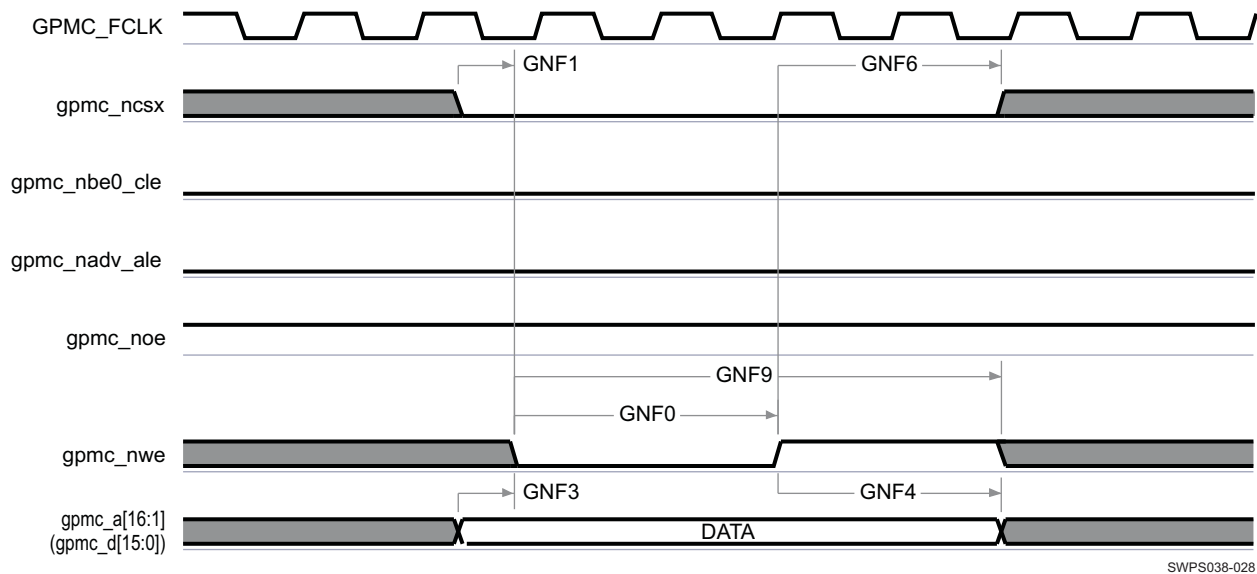
(1) In gpmc_ncsx, x is equal to 0, 1, 2, 3, 4, 5, 6, or 7.

**Figure 6-16. GPMC / NAND Flash—Data Write Cycle**

## 6.4.2 SDRAM Memory Controller (SDRC)

> **NOTE**
>
> For more information, see Memory Subsystem / SDRAM Controller (SDRC) Subsystem section of the *AM/DM37x Multimedia Device Technical Reference Manual* (literature number SPRUGN4).

The SDRAM controller subsystem module provides connectivity between the processor and external DRAM memory components. The module includes support for double-data-rate SDRAM (mobile DDR).

### 6.4.2.1 LPDDR Interface

The LPDDR interface is balled out on the bottom side of the CUS package and on the top side of the POP packages. The LPDDR interface on the top of the POP package has been designed for compatibility any POP LPDDR device with a matching footprint and compliance with the JEDEC LPDDR-266 specification.

This section provides the timing specification for the bottom-side LPDDR interface as a PCB design and manufacturing specification. The design rules constrain PCB trace length, PCB trace skew, signal integrity, cross-talk, and signal timing. These rules, when followed, result in a reliable LPDDR memory system without the need for a complex timing closure process. For more information regarding guidelines for using this LPDDR specification, see the *Understanding TI's PCB Routing Rule-Based DDR Timing Specification* Application Report (literature number SPRAAV0).

#### 6.4.2.1.1 LPDDR Interface Schematic

Figure 6-17 and Figure 6-18 show the LPDDR interface schematics for a LPDDR memory system. The 1 x16 LPDDR system schematic is identical to Figure 6-17 except that the high word LPDDR device is deleted.
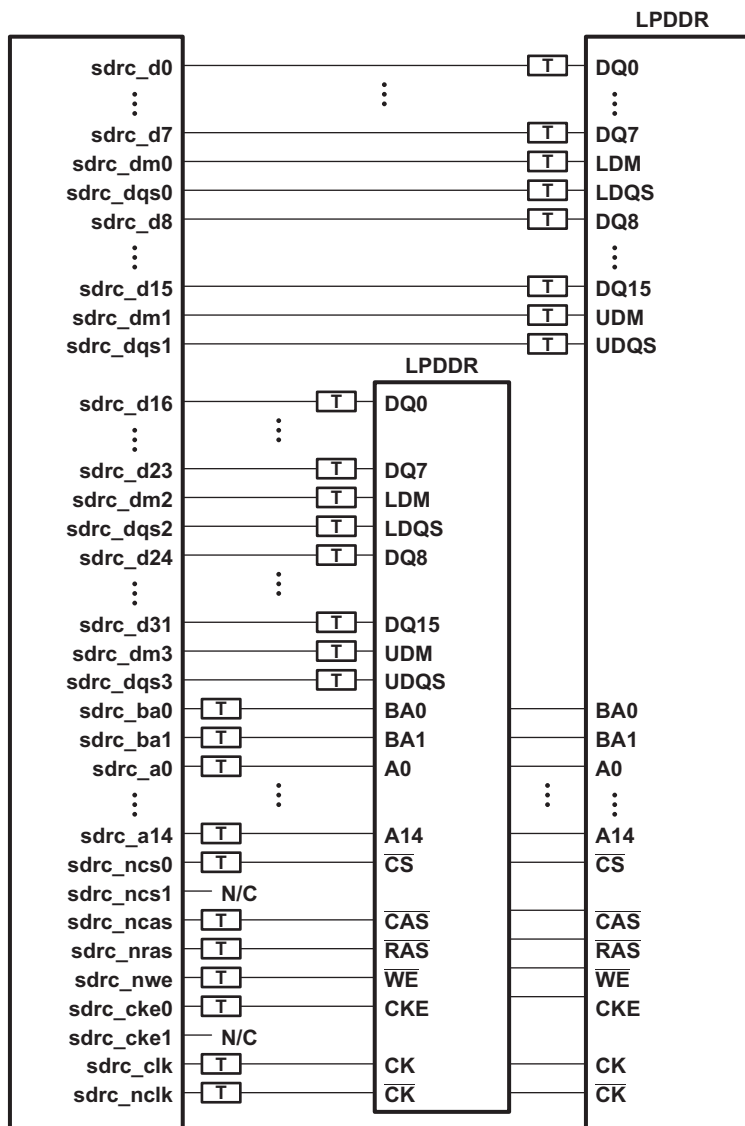
**Figure 6-17. DM37x LPDDR High Level Schematic (x16 memories)**
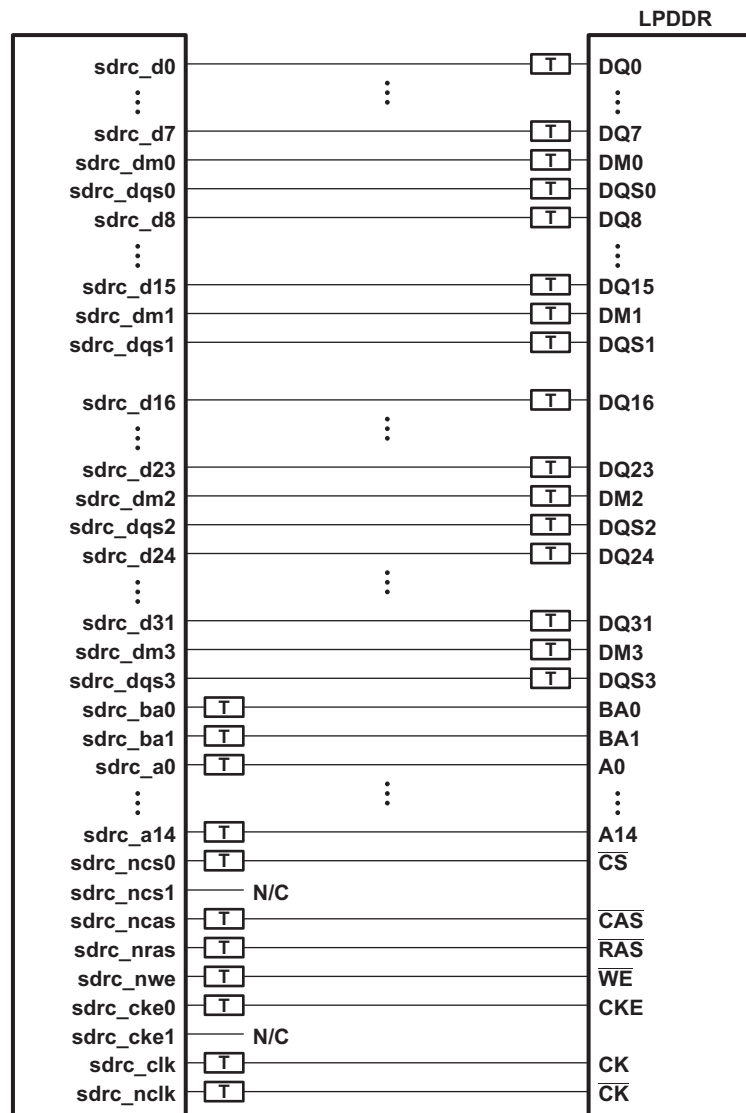
**Figure 6-18. DM37x LPDDR High Level Schematic (x32 memory)**

#### 6.4.2.1.2 Compatible JEDEC LPDDR Devices

Table 6-13 shows the parameters of the JEDEC LPDDR devices that are compatible with this interface. Generally, the LPDDR interface is compatible with x16 and x32 LPDDR266 and LPDDR333 speed grade LPDDR devices.

**Table 6-13. Compatible JEDEC LPDDR Devices**

| NO. | PARAMETER | MIN | MAX | UNIT | NOTES |
|-----|-----------|-----|-----|------|-------|
| 1 | JEDEC LPDDR Device Speed Grade | LPDDR-266 | | | See Note [1] |
| 2 | JEDEC LPDDR Device Bit Width | 16 | 32 | Bits | |
| 3 | JEDEC LPDDR Device Count | 1 | 2 | Devices | See Note [2] |
| 4 | JEDEC LPDDR Device Ball Count | 60 | 90 | Balls | |

(1) Higher LPDDR speed grades are supported due to inherent JEDEC LPDDR backwards compatibility.

(2) 1 x16 LPDDR device is used for 16 bit LPDDR memory system. 1x32 or 2x16 LPDDR devices are used for a 32-bit LPDDR memory system.

### 6.4.2.1.3  PCB Stackup

The minimum stackup required for routing the DM37x is a six layer stack as shown in Table 6-14. Additional layers may be added to the PCB stack up to accommodate other circuitry or to reduce the size of the PCB footprint.

**Table 6-14. DM37x Minimum PCB Stack Up**

| LAYER | TYPE | DESCRIPTION |
|---|---|---|
| 1 | Signal | Top Routing Mostly Horizontal |
| 2 | Plane | Ground |
| 3 | Plane | Power |
| 4 | Signal | Internal Routing |
| 5 | Plane | Ground |
| 6 | Signal | Bottom Routing Mostly Vertical |

**Table 6-15. PCB Stack Up Specifications [4]**

| NO. | PARAMETER | MIN | TYP | MAX | UNIT | NOTES |
|---|---|---|---|---|---|---|
| 1 | PCB Routing/Plane Layers | 6 | | | | |
| 2 | Signal Routing Layers | 3 | | | | |
| 3 | Full ground layers under LPDDR routing region | 2 | | | | |
| 4 | Number of ground plane cuts allowed within LPDDR routing region | | | 0 | | |
| 5 | Number of ground reference planes required for each LPDDR routing layer | 1 | | | | |
| 6 | Number of layers between LPDDR routing layer and reference ground plane | | | 0 | | |
| 7 | PCB Routing Feature Size | | 4 | | Mils | |
| 8 | PCB Trace Width w | | 4 | | Mils | |
| 9 | PCB BGA escape via pad size | | 18 | | Mils | |
| 10 | PCB BGA escape via hole size | | 8 | | Mils | |
| 11 | Device BGA Pad Size | | | | | See Note[1] |
| 12 | LPDDR Device BGA Pad Size | | | | | See Note[2] |
| 13 | Single Ended Impedance, ZO | 50 | | 75 | Ω | |
| 14 | Impedance Control | Z-5 | Z | Z + 5 | Ω | See Note[3] |

(1) See the Flip Chip Ball Grid Array Package (SPRU811) reference guide for device BGA pad size.

(2) See the LPDDR device manufacturer documentation for the LPDDR device BGA pad size.

(3) Z is the nominal singled ended impedance selected for the PCB specified by item 12.

(4) Specific routing guidelines for the CUS package can be found in the AM37x CUS Routing Guidelines (SPRABD4) application note.

### 6.4.2.2  Placement

Figure 6-19 shows the required placement for the DM37x device as well as the LPDDR devices. The dimensions for Figure 6-19 are defined in Table 6-16. The placement does not restrict the side of the PCB that the devices are mounted on. The ultimate purpose of the placement is to limit the maximum trace lengths and allow for proper routing space. For 1x16 and 1x32 LPDDR memory systems, the second LPDDR device is omitted from the placement.
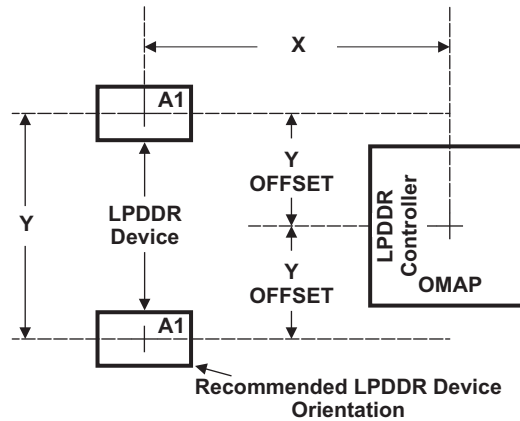
**Figure 6-19. DM37xx and LPDDR Device Placement**

**Table 6-16. Placement Specifications**

| NO. | PARAMETER | MIN | MAX | UNIT | NOTES |
|---|---|---|---|---|---|
| 1 | X | | 1440 | Mils | See Notes[1], [2] |
| 2 | Y | | 1030 | Mils | See Notes[1], [2] |
| 3 | Y Offset | | 525 | Mils | See Notes[1],[2],[3] |
| 4 | LPDDR Keepout Region | | | | See Note[4] |
| 5 | Clearance from non-LPDDR signal to LPDDR Keepout Region | 4 | | w | See Note[5] |

(1) See Figure 6-17 for dimension definitions.

(2) Measurements from center of device to center of LPDDR device.

(3) For 16 bit memory systems it is recommended that Y Offset be as small as possible.

(4) LPDDR keepout region to encompass entire LPDDR routing area.

(5) Non-LPDDR signals allowed within LPDDR keepout region provided they are separated from LPDDR routing layers by a ground plane.

### 6.4.2.3 LPDDR Keep Out Region

The region of the PCB used for the LPDDR circuitry must be isolated from other signals. The LPDDR keep out region is defined for this purpose and is shown in Figure 6-20. The size of this region varies with the placement and LPDDR routing. Additional clearances required for the keep out region are shown in Table 6-16.
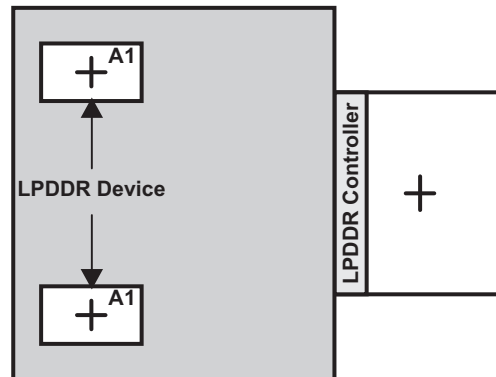
Region should encompass all LPDDR circuitry and varies depending
on placement. Non-LPDDR signals should not be routed on the
LPDDR signal layers within the LPDDR keep out region. Non-LPDDR
signals may be routed in the region provided they are routed on
layers separated from LPDDR signal layers by a ground layer. No
breaks should be allowed in the reference ground layers in this
region. In addition, the 1.8 V power plane should cover the entire keep
out region.

**Figure 6-20. LPDDR Keepout Region**

#### 6.4.2.4 Net Classes

Table 6-17 lists the clock net classes for the LPDDR interface. Table 6-18 lists the signal net classes, and associated clock net classes, for the signals in the LPDDR interface. These net classes are used for the termination and routing rules that follow.

**Table 6-17. Clock Net Class Definitions**

| CLOCK NET CLASS | PIN NAMES |
|---|---|
| CK | sdrc_clk/sdrc_nclk |
| DQS0 | sdrc_dqs0 |
| DQS1 | sdrc_dqs1 |
| DQS2 | sdrc_dqs2 |
| DQS3 | sdrc_dqs3 |

**Table 6-18. Signal Net Class Definitions**

| CLOCK NET CLASS | ASSOCIATED CLOCK NET CLASS | PIN NAMES |
|---|---|---|
| ADDR_CTRL | CK | sdrc_ba[1:0], sdrc_a[14:0], sdrc_ncs[1:0], sdrc_ncas, sdrc_nras, sdrc_nwe, sdrc_cke[1:0] |
| DQ0 | DQS0 | sdrc_d[7:0], sdrc_dm0 |
| DQ1 | DQS1 | sdrc_d[15:8], sdrc_dm1 |
| DQ2 | DQS2 | sdrc_d[23:16], sdrc_dm2 |
| DQ3 | DQS3 | sdrc_d[31:24], sdrc_dm3 |

#### 6.4.2.5 LPDDR Signal Termination

No terminations of any kind are required in order to meet signal integrity and overshoot requirements. Serial terminators are permitted, if desired, to reduce EMI risk; however, serial terminations are the only type permitted. Table 6-19 shows the specifications for the series terminators.

**Table 6-19. LPDDR Signal Terminations**

| NO. | PARAMETER | MIN | TYP | MAX | UNIT | NOTES |
|---|---|---|---|---|---|---|
| 1 | CK Net Class | 0 |  | 10 | Ω | See Note[1] |
| 2 | ADDR_CTRL Net Class | 0 | 22 | Zo | Ω | See Notes[1],[2],[3] |
| 3 | Data Byte Net Classes (DQS0-DQS3, DQ0-DQ3) | 0 | 22 | Zo | Ω | See Notes[1],[2],[3] |

(1) Only series termination is permitted, parallel or SST specifically disallowed.

(2) Terminator values larger than typical only recommended to address EMI issues.

(3) Termination value should be uniform across net class.

## 6.4.2.6 LPDDR CK and ADDR_CTRL Routing

Figure 6-21 shows the topology of the routing for the CK and ADDR_CTRL net classes. The route is a balanced T as it is intended that the length of segments B and C be equal. In addition, the length of A should be maximized.
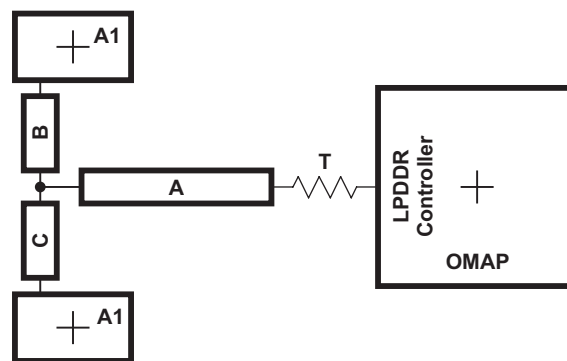


**Figure 6-21. CK and ADDR_CTRL Routing and Topology**

**Table 6-20. CK and ADDR_CTRL Routing Specification [5]**

| NO. | PARAMETER | MIN | TYP | MAX | UNIT | NOTES |
|---|---|---|---|---|---|---|
| 1 | Center to Center CK-CK spacing |  |  | 2w |  |  |
| 2 | CK Differential Pair Skew Length Mismatch[4] |  |  | 25 | Mils | See Note[1] |
| 3 | CK B to C Skew Length Mismatch |  |  | 25 | Mils |  |
| 4 | Center to Center CK to other LPDDR trace spacing | 4w |  |  |  | See Note[2] |
| 5 | CK/ADDR_CTRL nominal trace length | CACLM-50 | CACLM | CACLM+50 | Mils | See Note[3] |
| 6 | ADDR_CTRL to CK Skew Length Mismatch |  |  | 100 | Mils |  |
| 7 | ADDR_CTRL to ADDR_CTRL Skew Length Mismatch |  |  | 100 | Mils |  |
| 8 | Center to Center ADDR_CTRL to other LPDDR trace spacing | 4w |  |  |  | See Note[2] |
| 9 | Center to Center ADDR_CTRL to other ADDR_CTRL trace spacing | 3w |  |  |  | See Note[2] |
| 10 | ADDR_CTRL A to B, ADDR_CTRL A to C Skew Length Mismatch |  |  | 100 | Mils | See Note[1] |
| 11 | ADDR_CTRL B to C Skew Length Mismatch |  |  | 100 | Mils |  |

(1) Series terminator, if used, should be located closest to DM37x.

(2) Center to center spacing is allowed to fall to minimum (w) for up to 500 mils of routed length to accommodate BGA escape and routing congestion.

(3) CACLM is the longest Manhattan distance of the CK and ADDR_CTRL net classes.

(4) Differential impedance should be 100 ohms.

(5) Specific routing guidelines for the CUS package can be found in the AM37x CUS Routing Guidelines (SPRABD4) application note.

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Figure 6-22 shows the topology and routing for the DQS and DQ net classes; the routes are point to point. Skew matching across bytes is not needed nor recommended.
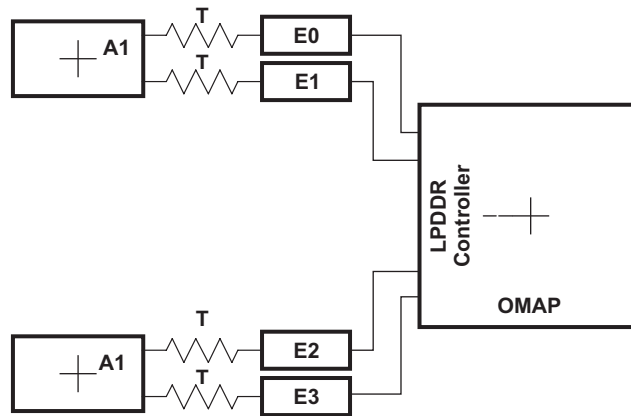


**Figure 6-22. DQS and DQ Routing and Topology**

**Table 6-21. DQS and DQ Routing Specification[1] [6]**

| PARAMETER | MIN | TYP | MAX | UNIT | NOTES |
|---|---|---|---|---|---|
| DQS E Skew Length Mismatch | | | 25 | Mils | |
| Center to Center DQS to other LPDDR trace spacing | 4w | | | | See Note[2] |
| DQS/DQ nominal trace length | DQLM - 50 | DQLM | DQLM + 50 | Mils | See Note[2] |
| DQ to DQS Skew Length Mismatch | | | 100 | Mils | See Note [4] |
| DQ to DQ Skew Length Mismatch | | | 100 | Mils | See Note [4] |
| Center to Center DQ to other LPDDR trace spacing | 4w | | | | See Note[5] |
| Center to Center DQ to other DQ trace spacing | 3w | | | | See Note[2],[3] |
| DQ E Skew Length Mismatch | | | 100 | Mils | |

(1) Series terminator, if used, should be located closest to LPDDR.

(2) Center to center spacing is allowed to fall to minimum (w) for up to 500 mils of routed length to accommodate BGA escape and routing congestion.

(3) DQLM is the longest Manhattan distance of the DQS and DQ net classes.

(4) There is no need, and it is not recommended, to skew match across data bytes. This specification is only relative within a data byte.

(5) DQs from other bytes are considered *other* LPDDR traces.

(6) Specific routing guidelines for the CUS package can be found in the AM37x CUS Routing Guidelines (SPRABD4) application note.

## 6.5 Multimedia Interfaces

### 6.5.1 Camera ISP2P Interface

> **NOTE**
>
> For more information, see Camera ISP chapter of the *AM/DM37x Multimedia Device Technical Reference Manual* (literature number SPRUGN4).

The camera subsystem provides the system interfaces and the processing capability to connect raw, YUV or JPEG image sensor modules to the device for video-preview, video-record and still-image-capture applications.

The camera ISP2P subsystem supports up to two simultaneous pixel flows but only one of them can use the video processing hardware:

- Parallel camera interface + Serial camera interface: one interface data goes through the video processing hardware. The other interface data goes directly to memory
- Serial camera interface + Serial camera interface: one serial interface data goes through the video processing hardware. The other serial interface data goes directly to memory.

The camera ISP2P subsystem supports different camera configurations:

- 10-bit Parallel interface
- 12-bit Parallel interface
- 12-bit Parallel interface

**Note**: For more information, see the Camera ISP / Camera ISP Environment / Camera ISP Connectivity Schemes section of the *AM/DM37x Multimedia Device Technical Reference Manual* (literature number SPRUGN4).

#### 6.5.1.1 Camera Output Clocks (cam_xclka and cam_xclkb)

**Table 6-22. ISP2P cam_xclka and cam_xclkb Output Clocks Switching Characteristics**

| NO. | PARAMETER | | OPP100 | | OPP50 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| ISP15 | $1 / t_{c(xclk)}$ | Frequency[1], output clock cam_xclkn[4] | | 216 | | 216 | MHz |
| ISP16 | $t_{w(xclkH)}$ | Typical pulse duration, output clock cam_xclkn[4] high | 0.5P[2] | | 0.5P[2] | | ns |
| ISP16 | $t_{w(xclkL)}$ | Typical pulse duration, output clock cam_xclkn[4] low | 0.5P[2] | | 0.5P[2] | | ns |
| | $t_{dc(xclk)}$ | Duty cycle error, output clock cam_xclkn[4] | | 0.5 * P[2] - 2.083 | | 0.5 * P[2] - 2.083 | ps |
| | $t_{J(xclk)}$ | Cycle jitter[3], output clock cam_xclkn[4] | | 0.044 * P[2] | | 0.044 * P[2] | ps |
| | $t_{R(xclk)}$ | Rise time, output clock cam_xclkn[4] | | 0.93 | | 0.93 | ns |
| | $t_{F(xclk)}$ | Fall time, output clock cam_xclkn[4] | | 0.93 | | 0.93 | ns |

(1) Related with the cam_xclkn[4] maximum and minimum frequencies programmable in the ISP module.
**NOTE**: You must disable the camera sensor or the camera module to change the frequency configuration. For more information, see the *AM/DM37x Multimedia Device Technical Reference Manual* (literature number SPRUGN4).

(2) P = cam_xclkn[4] period in ns

(3) Maximum cycle jitter supported by cam_xclka and cam_xclkb output clocks.

(4) In cam_xclkn, n is equal to a or b.

### 6.5.1.2 Parallel Camera Interface (CPI)

#### 6.5.1.2.1 CPI—Video and Graphics Digitizer 1.8V Mode

The imaging subsystem deals with the processing of the pixel data coming from an external image sensor or from video and graphics digitizer. It is a key component for the following multimedia applications: video preview, camera viewfinder, video record and still image capture. It supports RAW, RGB, and YUV data processing.

Table 6-24 assumes testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-23 and Figure 6-24).

#### Table 6-23. CPI Timing Conditions—Video and Graphics Digitizer 1.8-V Mode

| TIMING CONDITION PARAMETER | | VALUE | | UNIT |
|---|---|---|---|---|
| | | MIN | MAX | |
| Input Conditions | | | | |
| $t_R$ | Input signal rise time | 80 | 1800 | ps |
| $t_F$ | Input signal fall time | 80 | 1800 | ps |

#### Table 6-24. CPI Timing Requirements—Video and Graphics Digitizer 1.8-V Mode[4] [6]

| NO. | | PARAMETER | OPP100 | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| ISP1 | $1 / t_{c(pclk)}$ | Frequency[1], input pixel clock cam_pclk | | 148.5 | MHz |
| ISP2 | $t_{w(pclkL)}$ | Typical pulse duration, input pixel clock cam_pclk low | 0.5P[2] | | ns |
| ISP3 | $t_{w(pclkH)}$ | Typical pulse duration, input pixel clock cam_pclk high | 0.5P[2] | | ns |
| | $t_{dc(pclk)}$ | Duty cycle error, input pixel clock cam_pclk | | 0.5*P[2] - 3.247 | ns |
| | $t_{J(pclk)}$ | Cycle jitter[3], input pixel clock cam_pclk | | 0.06P[2] | ns |
| ISP4 | $t_{su(vsV-pclkH)}$ | Setup time, input vertical synchronization cam_vs valid before input pixel clock cam_pclk rising/falling edge | 0.75 | | ns |
| ISP5 | $t_{h(pclkH-vsV)}$ | Hold time, input vertical synchronization cam_vs valid after input pixel clock cam_pclk rising/falling edge | 0.96 | | ns |
| ISP6 | $t_{su(hsV-pclkH)}$ | Setup time, input horizontal synchronization cam_hs valid before input pixel clock cam_pclk rising/falling edge | 0.75 | | ns |
| ISP7 | $t_{h(pclkH-hsV)}$ | Hold time, input horizontal synchronization cam_hs valid after input pixel clock cam_pclk rising/falling edge | 0.96 | | ns |
| ISP8 | $t_{su(dV-pclkH)}$ | Setup time, input data cam_d[n:0][5] valid before input pixel clock cam_pclk rising/falling edge | 0.75 | | ns |
| ISP9 | $t_{h(pclkH-dV)}$ | Hold time, input data cam_d[n:0][5] valid after input pixel clock cam_pclk rising/falling edge | 0.96 | | ns |
| ISP10 | $t_{su(wenV-pclkH)}$ | Setup time, input write enable cam_wen valid before input pixel clock cam_pclk rising/falling edge | 0.75 | | ns |
| ISP11 | $t_{h(pclkH-wenV)}$ | Hold time, input write enable cam_wen valid after input pixel clock cam_pclk rising/falling edge | 0.96 | | ns |
| ISP12 | $t_{su(fldV-pclkH)}$ | Setup time, input field identification cam_fld valid before input pixel clock cam_pclk rising/falling edge | 0.75 | | ns |
| ISP13 | $t_{h(pclkH-fldV)}$ | Hold time, input field identification cam_fld valid after input pixel clock cam_pclk rising/falling edge | 0.96 | | ns |

(1) Related with the input maximum frequency supported by the ISP module in 8-bit mode with 8 to 16 data bits conversion bridge enabled.

(2) P = cam_pclk period in ns

(3) Maximum cycle jitter supported by cam_pclk input clock

(4) The timing requirements are assured up to the cycle jitter and duty cycle error conditions specified.

(5) n = 11 (Data bus size is limited to 8 bits. So the bits configuration is either cam_d[7:0] or cam_d[11:4]). Lines not connected must be tied low.

(6) See Section 4.3.4, Processor Clocks.
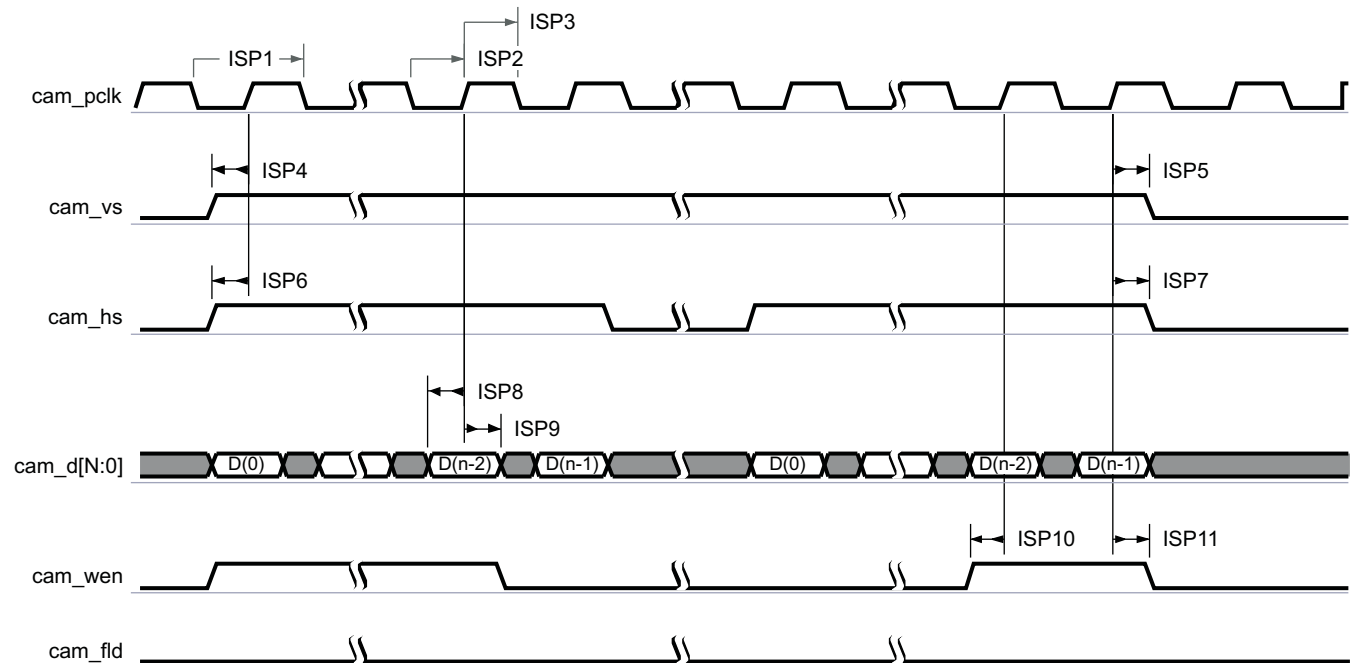
SWPS038-048

(1)   The polarity of cam_pclk, cam_fld, cam_vs, and cam_hs are software configurable. Optionally, the cam_wen signal can be used as an external memory write-enable signal. For further details, see the *AM/DM37x Multimedia Device Technical Reference Manual* (literature number SPRUGN4).

(2)   N = 11 (Data bus size is limited to 8 bits. So the bits configuration is either cam_d[7:0] or cam_d[11:4]). When the number of data lines is less than cam_d[N:0], data lines can be connected to the upper or lower lines of cam_d[N:0]. Lines not connected must be tied low. For more information about video port mapping, see the *AM/DM37x Multimedia Device Technical Reference Manual* (literature number SPRUGN4).

**Figure 6-23. CPI—Video and Graphics Digitizer—1.8-V Progressive Mode**
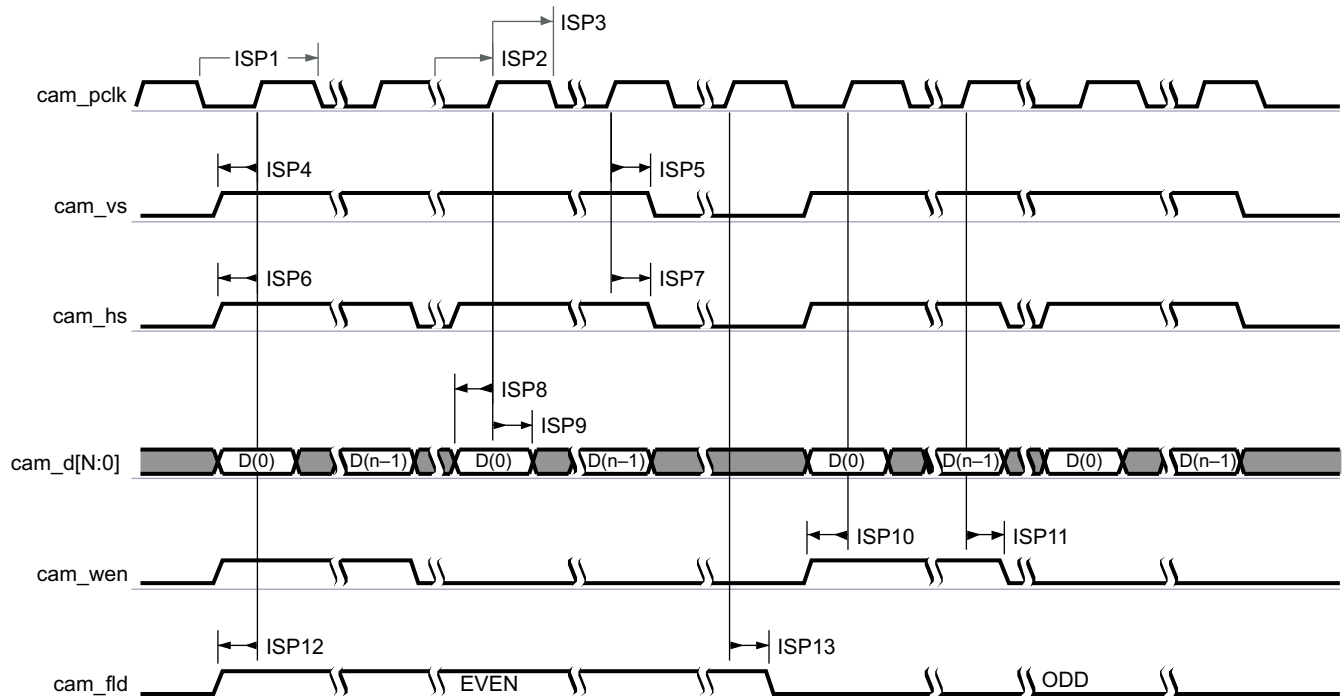
SWPS038-049

(1)  The polarity of cam_pclk, cam_fld, cam_vs, and cam_hs are software configurable. Optionally, the cam_wen signal can be used as an external memory write-enable signal. For further details, see the *AM/DM37x Multimedia Device Technical Reference Manual* (literature number SPRUGN4).

(2)  N = 11 (Data bus size is limited to 8 bits. So the bits configuration is either cam_d[7:0] or cam_d[11:4]). When the number of data lines is less than cam_d[N:0], data lines can be connected to the upper or lower lines of cam_d[N:0]. Lines not connected must be tied low. For more information about video port mapping, see the *AM/DM37x Multimedia Device Technical Reference Manual* (literature number SPRUGN4).

**Figure 6-24. CPI—Video and Graphics Digitizer—1.8-V Interlaced Mode**

### 6.5.1.2.2  CPI—12-Bit SYNC Normal Progressive Mode

Table 6-26 assumes testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-25).

**Table 6-25. CPI Timing Conditions—12-Bit SYNC Normal Progressive Mode[1]**

| TIMING CONDITION PARAMETER | | VALUE | UNIT |
|---|---|---|---|
| **Input Conditions** | | | |
| $t_R$ | Input signal rise time | 2.7 | ns |
| $t_F$ | Input signal fall time | 2.7 | ns |
| **Output Condition** | | | |
| $C_{LOAD}$ | Output load capacitance | 8.6 | pF |

(1)  The load setting of the IO buffer: LB0 = 1.

### Table 6-26. CPI Timing Requirements—12-Bit SYNC Normal Progressive Mode[4] [5]

| NO. | PARAMETER | | OPP100 | | OPP50 | | UNIT |
|-----|-----------|---|--------|-----|-------|-----|------|
| | | | MIN | MAX | MIN | MAX | |
| ISP17 | $1 / t_{c(pclk)}$ | Frequency[1], input pixel clock cam_pclk | | 75 | | 45 | MHz |
| ISP18 | $t_{w(pclkH)}$ | Typical pulse duration, input pixel clock cam_pclk high | 0.5P[2] | | 0.5P[2] | | ns |
| ISP18 | $t_{w(pclkL)}$ | Typical pulse duration, input pixel clock cam_pclk low | 0.5P[2] | | 0.5P[2] | | ns |
| | $t_{dc(pclk)}$ | Duty cycle error, input pixel clock cam_pclk | | 0.5P[2] - 3.465 | | 0.5P[2] - 6.93 | ns |
| | $t_{J(pclk)}$ | Cycle jitter[3], input pixel clock cam_pclk | | 0.0649*P [2] | | 0.0649*P [2] | ns |
| ISP19 | $t_{su(dV-pclkH)}$ | Setup time, input data cam_d[11:0] valid before input pixel clock cam_pclk rising edge | 1.82 | | 3.25 | | ns |
| ISP20 | $t_{h(pclkH-dV)}$ | Hold time, input data cam_d[11:0] valid after input pixel clock cam_pclk rising edge | 1.82 | | 3.25 | | ns |
| ISP21 | $t_{su(dV-vsH)}$ | Setup time, input vertical synchronization cam_vs valid before input pixel clock cam_pclk rising edge | 1.82 | | 3.25 | | ns |
| ISP22 | $t_{h(pclkH-vsV)}$ | Hold time, input vertical synchronization cam_vs valid after input pixel clock cam_pclk rising edge | 1.82 | | 3.25 | | ns |
| ISP23 | $t_{su(dV-hsH)}$ | Setup time, input horizontal synchronization cam_hs valid before input pixel clock cam_pclk rising edge | 1.82 | | 3.25 | | ns |
| ISP24 | $t_{h(pclkH-hsV)}$ | Hold time, input horizontal synchronization cam_hs valid after input pixel clock cam_pclk rising edge | 1.82 | | 3.25 | | ns |
| ISP25 | $t_{su(dV-hsH)}$ | Setup time, input write enable cam_wen valid before input pixel clock cam_pclk rising edge | 1.82 | | 3.25 | | ns |
| ISP26 | $t_{h(pclkH-hsV)}$ | Hold time, input write enable cam_wen valid after input pixel clock cam_pclk rising edge | 1.82 | | 3.25 | | ns |

(1)  Related with the input maximum frequency supported by the ISP module.

(2)  P = cam_pclk period in ns

(3)  Maximum cycle jitter supported by cam_pclk input clock.

(4)  The timing requirements are assured up to the cycle jitter and duty cycle error conditions specified.

(5)  See Section 4.3.4, *Processor Clocks*.

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(1) The polarity of cam_pclk, cam_fld, cam_vs, and cam_hs are configurable. If the cam_hs, cam_vs, and cam_fld signals are output, the signal length can be set.

(2) The parallel camera in SYNC mode supports progressive image sensor modules and 8-, 10-, 11-, or 12-bit data.

(3) When the image sensor has fewer than 12 data lines, it must be connected to the lower data lines and the unused lines must be grounded.

(4) However, it is possible to shift the data to 0, 2, or 4 data internal lanes.

(5) The bit configurations are: cam_d[11:4] or cam_d[7:0] in 8-bit mode, cam_d[11:2] or cam_d[9:0] in 10-bit mode, cam_d[10:0] in 11-bit mode and cam_d[11:0] in 12-bit mode.

(6) Optionally, the data write to memory can be qualified by the external cam_wen signal.

(7) The cam_wen signal can be used as an external memory write-enable signal. The data is stored to memory only if cam_hs, cam_vs, and cam_wen signals are asserted.

(8) In cam_xclki, i can be equal to a or b. See Table 6-22 for ISP15 and ISP16 parameters.

**Figure 6-25. CPI—12-Bit SYNC Normal Progressive Mode**

### 6.5.1.2.3 CPI—8-Bit SYNC Packed Progressive Mode

Table 6-28 assumes testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-26).

**Table 6-27. CPI Timing Conditions—8-Bit SYNC Packed Progressive Mode[1]**

| TIMING CONDITION PARAMETER | | VALUE | UNIT |
|---|---|---|---|
| **Input Conditions** | | | |
| $t_R$ | Input signal rise time | 2.5 | ns |
| $t_F$ | Input signal fall time | 2.5 | ns |
| **Output Condition** | | | |
| $C_{LOAD}$ | Output load capacitance | 8.6 | pF |

(1)  The load setting of the IO buffer: LB0 = 1.

**Table 6-28. CPI Timing Requirements—8-Bit SYNC Packed Progressive Mode[4] [5]**

| NO. | PARAMETER | | OPP100 | | OPP50 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| ISP3 | $1 / t_{c(pclk)}$ | Frequency [1], input pixel clock cam_pclk | | 130 | | 65 | MHz |
| ISP4 | $t_{w(pclkH)}$ | Typical pulse duration, input pixel clock cam_pclk high | $0.5*P^{[2]}$ | | $0.5*P^{[2]}$ | | ns |
| ISP4 | $t_{w(pclkL)}$ | Typical pulse duration, input pixel clock cam_pclk low | $0.5*P^{[2]}$ | | $0.5*P^{[2]}$ | | ns |
| | $t_{dc(pclk)}$ | Duty cycle error, input pixel clock cam_pclk | | $0.5*P^{[2]}$ - 3.465 | | $0.5*P^{[2]}$ - 6.93 | ns |
| | $t_{J(pclk)}$ | Cycle jitter[3], input pixel clock cam_pclk | | $0.0649*P^{[2]}$ | | $0.0649*P^{[2]}$ | ns |
| ISP5 | $t_{su(dV-pclkH)}$ | Setup time, input data cam_d[7:0] valid before input pixel clock cam_pclk rising edge | 1.08 | | 2.27 | | ns |
| ISP6 | $t_{h(pclkH-dV)}$ | Hold time, input data cam_d[7:0] valid after input pixel clock cam_pclk rising edge | 1.08 | | 2.27 | | ns |
| ISP7 | $t_{su(dV-vsH)}$ | Setup time, input vertical synchronization cam_vs valid before input pixel clock cam_pclk rising edge | 1.08 | | 2.27 | | ns |
| ISP8 | $t_{h(pclkH-vsV)}$ | Hold time, input vertical synchronization cam_vs valid after input pixel clock cam_pclk rising edge | 1.08 | | 2.27 | | ns |
| ISP9 | $t_{su(dV-hsH)}$ | Setup time, input horizontal synchronization cam_hs valid before input pixel clock cam_pclk rising edge | 1.08 | | 2.27 | | ns |
| ISP10 | $t_{h(pclkH-hsV)}$ | Hold time, input horizontal synchronization cam_hs valid after input pixel clock cam_pclk rising edge | 1.08 | | 2.27 | | ns |
| ISP11 | $t_{su(dV-hsH)}$ | Setup time, input write enable cam_wen valid before input pixel clock cam_pclk rising edge | 1.08 | | 2.27 | | ns |
| ISP12 | $t_{h(pclkH-hsV)}$ | Hold time, input write enable cam_wen valid after input pixel clock cam_pclk rising edge | 1.08 | | 2.27 | | ns |

(1)  Related with the input maximum frequency supported by the ISP module.

(2)  P = cam_pclk period in ns

(3)  Maximum cycle jitter supported by cam_pclk input clock.

(4)  The timing requirements are assured up to the cycle jitter and duty cycle error conditions specified.

(5)  See Section 4.3.4, *Processor Clocks.*

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(1)   The polarity of cam_pclk, cam_fld, cam_vs, and cam_hs are configurable.

(2)   The image sensor is connected to the lower data lines and the unused lines are grounded. However, it is possible to shift the data to 0, 2, or 4 data internal lanes. The bit configurations are: cam_d[11:4] or cam_d[7:0] in 8-bit packed mode.

(3)   Optionally, the data write to memory can be qualified by the external cam_wen signal. The cam_wen signal can be used as a external memory write-enable signal. The data is stored to memory only if cam_hs, cam_vs, and cam_wen signals are asserted. The polarity of cam_fld is programmable.

(4)   The camera module can pack 8-bit data into 16 bits. It doubles the maximum pixel clock. This mode can be particularly useful to transfer an YCbCr data stream or compressed stream to memory at very high speed.

(5)   In cam_xclki, i can be equal to a or b. See Table 6-22 for ISP15 and ISP16 parameters.

**Figure 6-26. CPI—8-Bit SYNC Packed Progressive Mode**

### 6.5.1.2.4   CPI—12-Bit SYNC Normal Interlaced Mode

Table 6-30 assumes testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-27).

**Table 6-29. CPI Timing Conditions—12-Bit SYNC Normal Interlaced Mode**

| TIMING CONDITION PARAMETER | | VALUE | UNIT |
|---|---|---|---|
| **Input Conditions** | | | |
| $t_R$ | Input signal rise time | 2.7 | ns |
| $t_F$ | Input signal fall time | 2.7 | ns |
| **Output Condition** | | | |
| $C_{LOAD}$ | Output load capacitance[1] | 8.6 | pF |

(1)  The load setting of the IO buffer: LB0 = 1.

## Table 6-30. CPI Timing Requirements—12-Bit SYNC Normal Interlaced Mode[4] [5]

| NO. | PARAMETER | | OPP100 | | OPP50 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| ISP17 | $1 / t_{c(pclk)}$ | Frequency[1], input pixel clock cam_pclk | | 75 | | 45 | MHz |
| ISP18 | $t_{w(pclkH)}$ | Typical pulse duration, input pixel clock cam_pclk high | 0.5P[2] | | 0.5P[2] | | ns |
| ISP18 | $t_{w(pclkL)}$ | Typical pulse duration, input pixel clock cam_pclk low | 0.5P[2] | | 0.5P[2] | | ns |
| | $t_{dc(pclk)}$ | Duty cycle error, input pixel clock cam_pclk | | 0.5*P[2] - 3.465 | | 0.5*P[2] - 6.93 | ns |
| | $t_{J(pclk)}$ | Cycle jitter[3], input pixel clock cam_pclk | | 0.0649*P [2] | | 0.0649*P [2] | ns |
| ISP19 | $t_{su(dV-pclkH)}$ | Setup time, input data cam_d[11:0] valid before input pixel clock cam_pclk rising edge | 1.82 | | 3.25 | | ns |
| ISP20 | $t_{h(pclkH-dV)}$ | Hold time, input data cam_d[11:0] valid after input pixel clock cam_pclk rising edge | 1.82 | | 3.25 | | ns |
| ISP21 | $t_{su(dV-vsH)}$ | Setup time, input vertical synchronization cam_vs valid before input pixel clock cam_pclk rising edge | 1.82 | | 3.25 | | ns |
| ISP22 | $t_{h(pclkH-vsV)}$ | Hold time, input vertical synchronization cam_vs valid after input pixel clock cam_pclk rising edge | 1.82 | | 3.25 | | ns |
| ISP23 | $t_{su(dV-hsH)}$ | Setup time, input horizontal synchronization cam_hs valid before input pixel clock cam_pclk rising edge | 1.82 | | 3.25 | | ns |
| ISP24 | $t_{h(pclkH-hsV)}$ | Hold time, input horizontal synchronization cam_hs valid after input pixel clock cam_pclk rising edge | 1.82 | | 3.25 | | ns |
| ISP25 | $t_{su(dV-hsH)}$ | Setup time, input write enable cam_wen valid before input pixel clock cam_pclk rising edge | 1.82 | | 3.25 | | ns |
| ISP26 | $t_{h(pclkH-hsV)}$ | Hold time, input write enable cam_wen valid after input pixel clock cam_pclk rising edge | 1.82 | | 3.25 | | ns |
| ISP27 | $t_{su(dV-fldH)}$ | Setup time, input field identification cam_fld valid before input pixel clock cam_pclk rising edge | 1.82 | | 3.25 | | ns |
| ISP28 | $t_{h(pclkH-fldV)}$ | Hold time, input field identification cam_fld valid after input pixel clock cam_pclk rising edge | 1.82 | | 3.25 | | ns |

(1)  Related with the input maximum frequency supported by the ISP module.

(2)  P = cam_pclk period in ns

(3)  Maximum cycle jitter supported by cam_pclk input clock.

(4)  The timing requirements are assured up to the cycle jitter and duty cycle error conditions specified.

(5)  See Section 4.3.4, *Processor Clocks*.
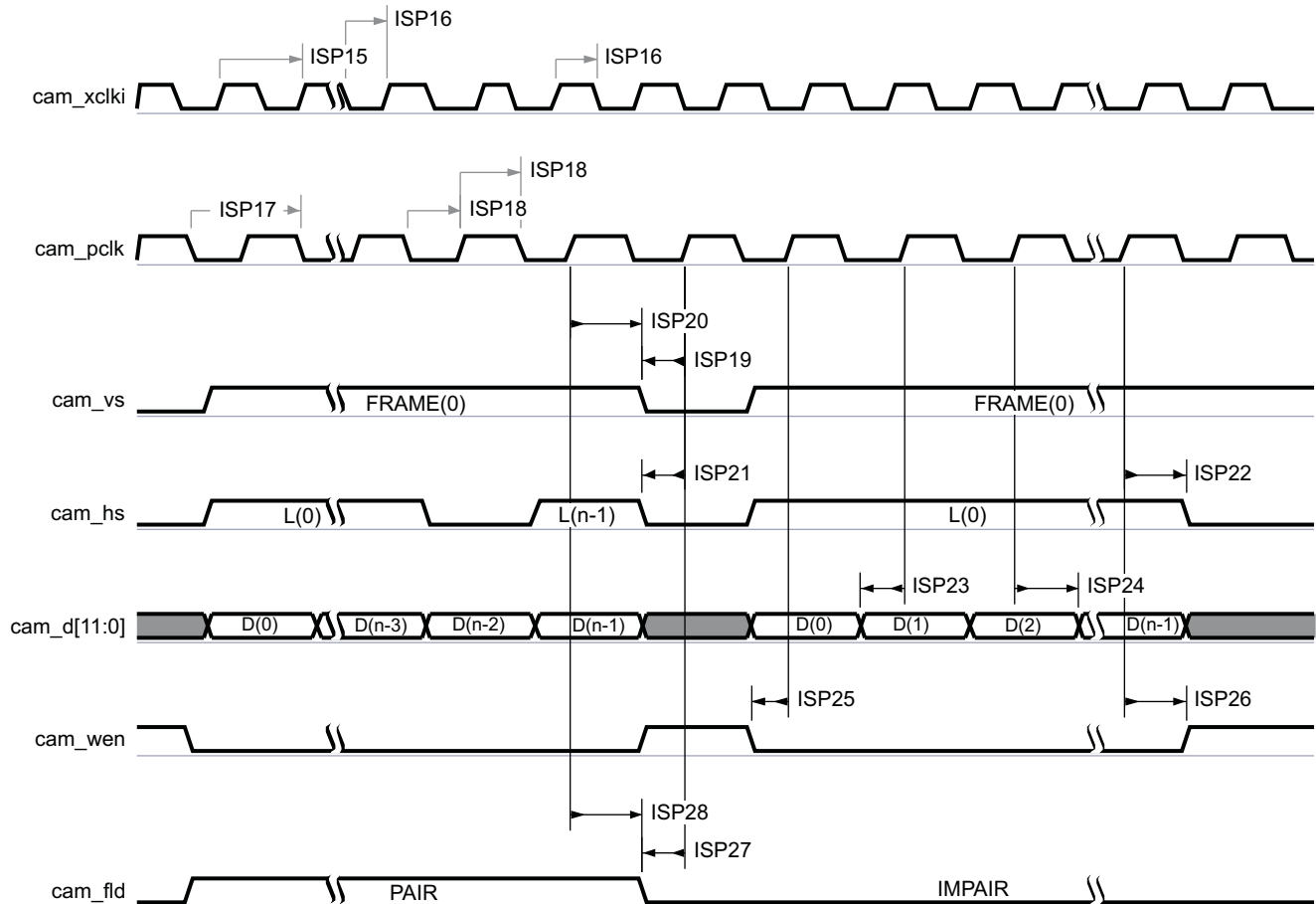
SWPS038-052

(1)   The polarity of cam_pclk, cam_fld, cam_vs, and cam_hs are configurable. If the cam_hs, cam_vs, and cam_fld signals are output, the signal length can be set.

(2)   The parallel camera in SYNC mode supports interlaced image sensor modules and 8-, 10-, 11-, or 12-bit data.

(3)   When the image sensor has fewer than 12 data lines, it is connected to the lower data lines and the unused lines are grounded.

(4)   It is possible to shift the data to 0, 2, or 4 data internal lanes.

(5)   The bit configurations are: cam_d[11:4] or cam_d[7:0] in 8-bit mode, cam_d[11:2] or cam_d[9:0] in 10-bit mode, cam_d[10:0] in 11-bit mode and cam_d[11:0] in 12-bit mode.

(6)   Optionally, the data write to memory can be qualified by the external cam_wen signal.

(7)   The cam_wen signal can be used as an external memory write-enable signal. The data is stored to memory only if cam_hs, cam_vs, and cam_wen signals are asserted.

(8)   In cam_xclki, i can be equal to a or b. See Table 6-22 for ISP15 and ISP16 parameters.

**Figure 6-27. CPI—12-bit SYNC Normal Interlaced ModeSection 5.3**

### 6.5.1.2.5 CPI—8-Bit SYNC Packed Interlaced Mode

Table 6-32 assumes testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-28).

#### Table 6-31. CPI Timing Conditions—8-Bit SYNC Packed Interlaced Mode

| TIMING CONDITION PARAMETER | | VALUE | UNIT |
|---|---|---|---|
| **Input Conditions** | | | |
| $t_R$ | Input signal rise time | 2.5 | ns |
| $t_F$ | Input signal fall time | 2.5 | ns |
| **Output Condition** | | | |
| $C_{LOAD}$ | Output load capacitance[1] | 8.6 | pF |

(1) The load setting of the IO buffer: LB0 = 1.

#### Table 6-32. CPI Timing Requirements—8-Bit SYNC Packed Interlaced Mode[4] [5]

| NO. | PARAMETER | | OPP100 | | OPP50 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| ISP3 | $1 / t_{c(pclk)}$ | Frequency[1], input pixel clock cam_pclk | | 130 | | 65 | MHz |
| ISP4 | $t_{w(pclkH)}$ | Typical pulse duration, input pixel clock cam_pclk high | 0.5P[2] | | 0.5P[2] | | ns |
| ISP4 | $t_{w(pclkL)}$ | Typical pulse duration, input pixel clock cam_pclk low | 0.5P[2] | | 0.5P[2] | | ns |
| | $t_{dc(pclk)}$ | Duty cycle error, input pixel clock cam_pclk | | 0.5*P[2] - 3.465 | | 0.5*P[2] - 6.93 | ns |
| | $t_{J(pclk)}$ | Cycle jitter[3], input pixel clock cam_pclk | | 0.0649*P[2] | | 0.0649*P[2] | ns |
| ISP5 | $t_{su(dV-pclkH)}$ | Setup time, input data cam_d[8:0] valid before input pixel clock cam_pclk rising edge | 1.08 | | 2.27 | | ns |
| ISP6 | $t_{h(pclkH-dV)}$ | Hold time, input data cam_d[8:0] valid after input pixel clock cam_pclk rising edge | 1.08 | | 2.27 | | ns |
| ISP7 | $t_{su(dV-vsH)}$ | Setup time, input vertical synchronization cam_vs valid before input pixel clock cam_pclk rising edge | 1.08 | | 2.27 | | ns |
| ISP8 | $t_{h(pclkH-vsV)}$ | Hold time, input vertical synchronization cam_vs valid after input pixel clock cam_pclk rising edge | 1.08 | | 2.27 | | ns |
| ISP9 | $t_{su(dV-hsH)}$ | Setup time, input horizontal synchronization cam_hs valid before input pixel clock cam_pclk rising edge | 1.08 | | 2.27 | | ns |
| ISP10 | $t_{h(pclkH-hsV)}$ | Hold time, input horizontal synchronization cam_hs valid after input pixel clock cam_pclk rising edge | 1.08 | | 2.27 | | ns |
| ISP11 | $t_{su(dV-hsH)}$ | Setup time, input write enable cam_wen valid before input pixel clock cam_pclk rising edge | 1.08 | | 2.27 | | ns |
| ISP12 | $t_{h(pclkH-hsV)}$ | Hold time, input write enable cam_wen valid after input pixel clock cam_pclk rising edge | 1.08 | | 2.27 | | ns |
| ISP13 | $t_{su(dV-fldH)}$ | Setup time, input field identification cam_fld valid before input pixel clock cam_pclk rising edge | 1.08 | | 2.27 | | ns |
| ISP14 | $t_{h(pclkH-fldV)}$ | Hold time, input field identification cam_fld valid after input pixel clock cam_pclk rising edge | 1.08 | | 2.27 | | ns |

(1) Related with the input maximum frequency supported by the ISP module.

(2) P = cam_pclk period in ns

(3) Maximum cycle jitter supported by cam_pclk input clock.

(4) The timing requirements are assured up to the cycle jitter and duty cycle error conditions specified.

(5) See Section 4.3.4, *Processor Clocks*.
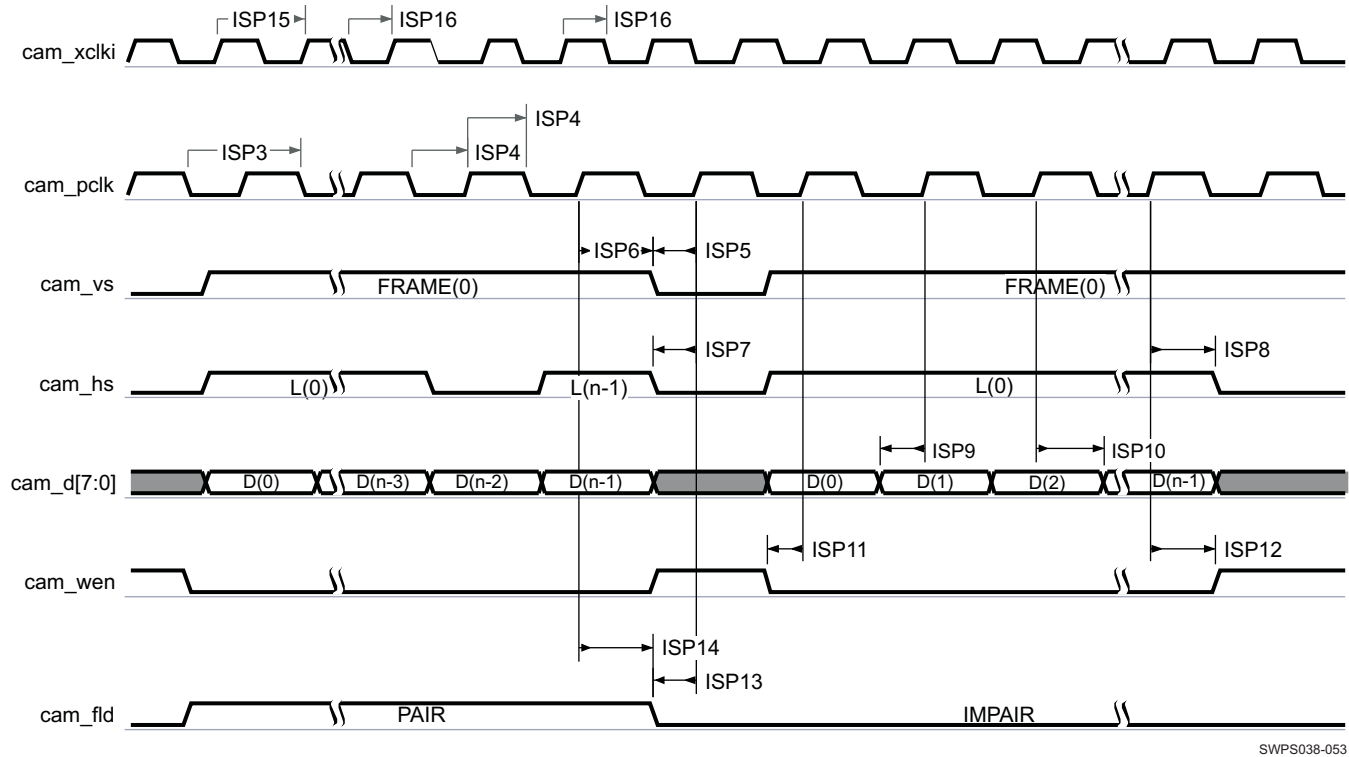
SWPS038-053

(1) The polarity of cam_pclk, cam_fld, cam_vs, and cam_hs are configurable.

(2) The image sensor is connected to the lower data lines and the unused lines are grounded. However, it is possible to shift the data to 0, 2, or 4 data internal lanes. The bit configurations are: cam_d[11:4] or cam_d[7:0] in 8-bit packed mode .

(3) Optionally, the data write to memory can be qualified by the external cam_wen signal. The cam_wen signal can be used as an external memory write-enable signal. The data is stored to memory only if cam_hs, cam_vs, and cam_wen signals are asserted.

(4) The camera module can pack 8-bit data into 16 bits. It doubles the maximum pixel clock. This mode can be particularly useful to transfer a YCbCr data stream or compressed stream to memory at very high speed.

(5) In cam_xclki, i can be equal to a or b. See Table 6-22 for ISP15 and ISP16 parameters.

**Figure 6-28. CPI—8-Bit SYNC Packed Interlaced Mode**

### 6.5.1.2.6  CPI—ITU Mode

Table 6-34 assumes testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-29).

**Table 6-33. CPI Timing Conditions—ITU Mode**

| TIMING CONDITION PARAMETER | | VALUE | UNIT |
|---|---|---|---|
| **Input Conditions** | | | |
| $t_R$ | Input signal rise time | 2.7 | ns |
| $t_F$ | Input signal fall time | 2.7 | ns |
| **Output Condition** | | | |
| $C_{LOAD}$ | Output load capacitance[1] | 8.6 | pF |

(1) The load setting of the IO buffer: LB0 = 1.

## Table 6-34. CPI Timing Requirements—ITU Mode[4] [5]

| NO. | PARAMETER | | OPP100 | | OPP50 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| ISP17 | $1 / t_{c(pclk)}$ | Frequency[1], input pixel clock cam_pclk | | 75 | | 45 | MHz |
| ISP18 | $t_{w(pclkH)}$ | Typical pulse duration, input pixel clock cam_pclk high | 0.5P[2] | | 0.5P[2] | | ns |
| ISP18 | $t_{w(pclkL)}$ | Typical pulse duration, input pixel clock cam_pclk low | 0.5P[2] | | 0.5P[2] | | ns |
| | $t_{dc(pclk)}$ | Duty cycle error, input pixel clock cam_pclk | | 0.5*P[2] - 3.465 | | 0.5*P[2] - 6.93 | ns |
| | $t_{J(pclk)}$ | Cycle jitter[3], input pixel clock cam_pclk | | 0.0649*P [2] | | 0.0649*P [2] | ns |
| ISP23 | $t_{su(dV-pclkH)}$ | Setup time, input data cam_d[9:0] valid before input pixel clock cam_pclk rising edge | 1.82 | | 3.25 | | ns |
| ISP24 | $t_{h(pclkH-dV)}$ | Hold time, input data cam_d[9:0] valid after input pixel clock cam_pclk rising edge | 1.82 | | 3.25 | | ns |

(1) Related with the input maximum frequency supported by the ISP module.

(2) P = cam_pclk period in ns

(3) Maximum cycle jitter supported by cam_pclk input clock.

(4) The timing requirements are assured up to the cycle jitter and duty cycle error conditions specified.

(5) See Section 4.3.4, *Processor Clocks*.
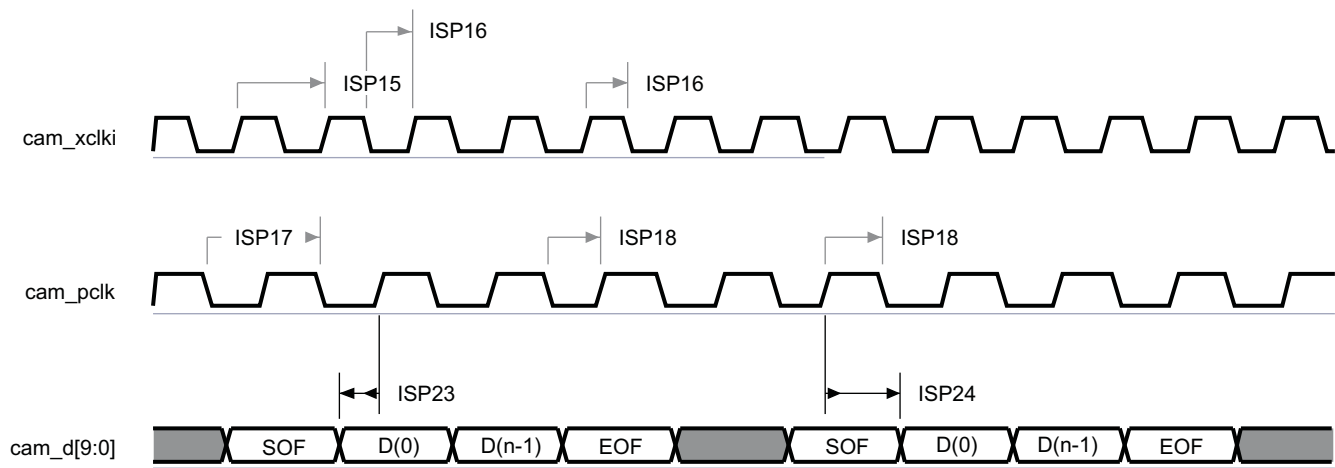


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(1) The unused lines are grounded and the data bus is connected to the lower data lines. However, it is possible to shift the data to 0, 2, or 4 data internal lanes. The different configurations are: cam_d[11:4] or cam_d[7:0] in 8-bit mode and cam_d[11:2] or cam_d[9:0] in 10-bit mode.

(2) The parallel camera in ITU mode supports progressive camera modules.

(3) In cam_xclki, i can be equal to a or b. See Table 6-22 for ISP15 and ISP16 parameters.

**Figure 6-29. CPI—ITU Mode**

## 6.5.2 Display Subsystem (DSS)

**NOTE**

For more information, see Display Subsystem chapter of the *AM/DM37x Multimedia Device Technical Reference Manual* (literature number SPRUGN4).

The display subsystem (DSS) provides the logic to display the video frame from external (SDRAM) or internal (SRAM) memory on an LCD panel or a TV set. The display subsystem integrates the following elements:

- Display controller (DISPC) module
- Remote frame buffer interface (RFBI) module
- NTSC/PAL video encoder
- LCD display with:
  – Parallel Interface

The two display supports can be active at the same time.

### 6.5.2.1 DSS—Parallel Interface

In parallel interface, the paths of the display subsystem modules are the display controller and the RFBI. The display controller has two I/O pad modes and could be in the following configuration:

- Bypass mode (RFBI disabled), which implements the MIPI DPI protocol
- RFBI mode (RFBI enabled), which implements MIPI DBI 2.0 type B protocol

For more information about MIPI DPI and MIPI DBI protocols, see the DSS chapter in the *AM/DM37x Multimedia Device Technical Reference Manual* (literature number SPRUGN4).

#### 6.5.2.1.1 DSS—Parallel Interface—Bypass Mode

Two types of LCD panel are supported:

- Thin film transistor (TFT) or active matrix technology
- Supertwisted nematic (STN) or passive matrix technology

Both configurations are discussed in the following paragraphs.

#### 6.5.2.1.2 DSS—Parallel Interface—Bypass Mode—TFT Mode

Table 6-36 assumes testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-30).

**Table 6-35. DSS Timing Conditions—TFT Mode**

| TIMING CONDITION PARAMETER | | VALUE | | UNIT |
|---|---|---|---|---|
| | | MIN | MAX | |
| **Output Condition** | | | | |
| $C_{LOAD}$ | Output load capacitance[1] | | 10 | pF |

(1)  Buffer strength configuration: LB0 = 1

**Table 6-36. DSS Switching Characteristics—TFT Mode[4]**

| NO. | PARAMETER | | OPP100 | | OPP50 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| DL0 | $t_{d(pclkA-hsync)}$ | Delay time, output pixel clock dss_pclk active edge to output horizontal synchronization dss_hsync transition | –4.215 | 4.215 | –4.658 | 4.658 | ns |
| DL1 | $t_{d(pclkA-vsync)}$ | Delay time, output pixel clock dss_pclk active edge to output vertical synchronization dss_vsync transition | –4.215 | 4.215 | –4.658 | 4.658 | ns |

**Table 6-36. DSS Switching Characteristics—TFT Mode[4] (continued)**

| NO. | PARAMETER | | OPP100 | | OPP50 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| DL2 | $t_{d(pclkA-acbiasA)}$ | Delay time, output pixel clock dss_pclk active edge to output data enable dss_acbias active level | −4.215 | 4.215 | −4.658 | 4.658 | ns |
| DL3 | $t_{d(pclkA-dV)}$ | Delay time, output pixel clock dss_pclk active edge to output data dss_data[23:0] valid | −4.215 | 4.215 | −4.658 | 4.658 | ns |
| DL4 | $1 / t_{c(pclk)}$ | Frequency[2], output pixel clock dss_pclk | | 74.3[3] | | 66[3] | MHz |
| DL5 | $t_{w(pclk)}$ | Pulse duration, output pixel clock dss_pclk low or high | 0.45P[1] | 0.55P[1] [5] | 0.45P[1] | 0.55P[1] [5] | ns |

(1) P = dss_pclk period in ns

(2) The pixel clock frequency is software programmable via the pixel clock divider configuration from 1 to 255 division range in the DISPC_DIVISOR register.

(3) For the DSS (TFT mode) in HD-TV application, to run at full speed (74.3 MHz) it is recommended to use the dss_data[5:0] signals on the dss_data[23:18] balls (H26, H25, E28, J26, AC27, AC28). In that case, the dss_data[23:18] signals are available on the sys_boot0, sys_boot1, sys_boot3, sys_boot4, sys_boot5, and sys_boot6 balls (AH26, AG26, AF18, AF19, AE21, AF21) to run at full speed (74.3 MHz).
If the dss_data[5:0] signals are used on the dss_data[5:0] balls (AG22, AH22, AG23, AH23, AG24, AH24), OPP100 DSS (TFT mode) are limited at 66 MHz. The values may change following the silicon characterization result.

(4) See Section 4.3.4, *Processor Clocks.*

(5) tW(pclk) = 0.66.P when DISPC_DIVISOR[6:0] PCD = 3.
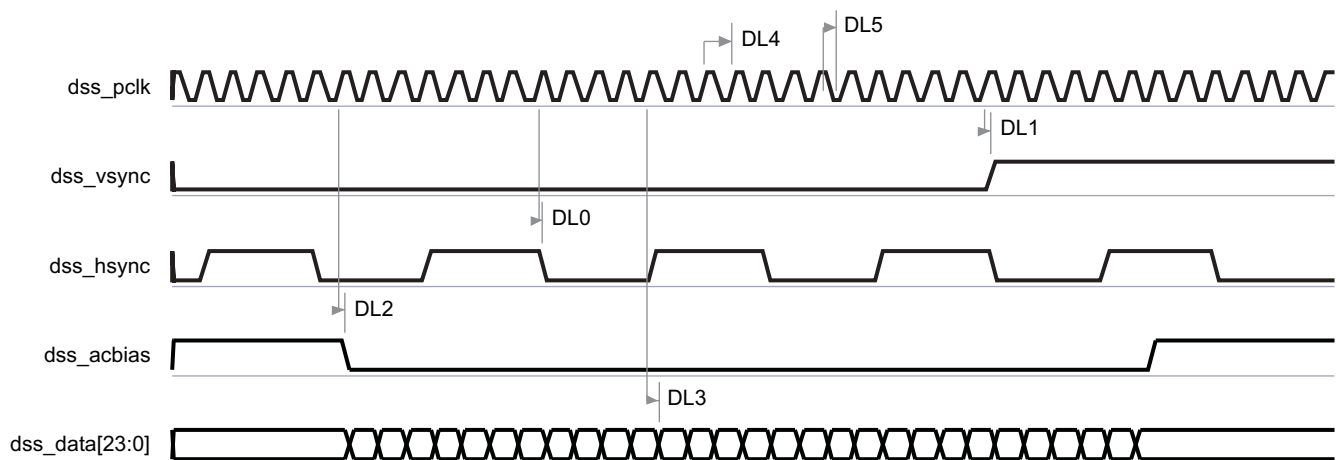


(1) The pixel data bus depends on the use of 8-, 9-, 12-, 16-, 18-, or 24-bit per pixel data output pins.

(2) The pixel clock frequency is programmable.

(3) All timings not illustrated in the waveform are progammable by software, and control signal polarity and driven edge of dss_pclk too.

(4) For more information, see the DSS chapter in the *AM/DM37x Multimedia Device Technical Reference Manual* (literature number SPRUGN4).

**Figure 6-30. DSS—TFT Mode**

### 6.5.2.1.3 DSS—Parallel Interface—Bypass Mode—STN Mode

Table 6-38 assumes testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-31).

**Table 6-37. DSS Timing Conditions—STN Mode**

| TIMING CONDITION PARAMETER | | VALUE | | UNIT |
|---|---|---|---|---|
| | | MIN | MAX | |
| **Output Condition** | | | | |
| $C_{LOAD}$ | Output load capacitance[1] | | 40 | pF |

(1) Buffer strength configuration: LB0 = 1

**Table 6-38. DSS Switching Characteristics—STN Mode[3] [4]**

| NO. | PARAMETER | | OPP100 | | OPP50 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| DL3 | $t_{d(pclkA-dV)}$ | Delay time, output pixel clock dss_pclk active edge to output data dss_data[7:0] valid | –6.868 | 6.868 | –6.868 | 6.868 | ns |
| DL4 | $1 / t_{c(pclk)}$ | Frequency[2], output pixel clock dss_pclk | | 44 | | 44 | MHz |
| DL5 | $t_{w(pclk)}$ | Pulse duration, output pixel clock dss_pclk low or high | 0.45P[1] | 0.55P[1] [5] | 0.45P[1] | 0.55P[1](5) | ns |

(1) P = dss_pclk period in ns

(2) The pixel clock frequency is software programmable via the pixel clock divider configuration from 1 to 255 division range in the DISPC_DIVISOR register.

(3) The DSS in STN mode is used with 4 or 8 pins only; unused pixel data bits always remain low.

(4) See Section 4.3.4, *Processor Clocks*.

(5) tW(pclk) = 0.66P when DISPC_DIVISOR[6:0] PCD = 3.
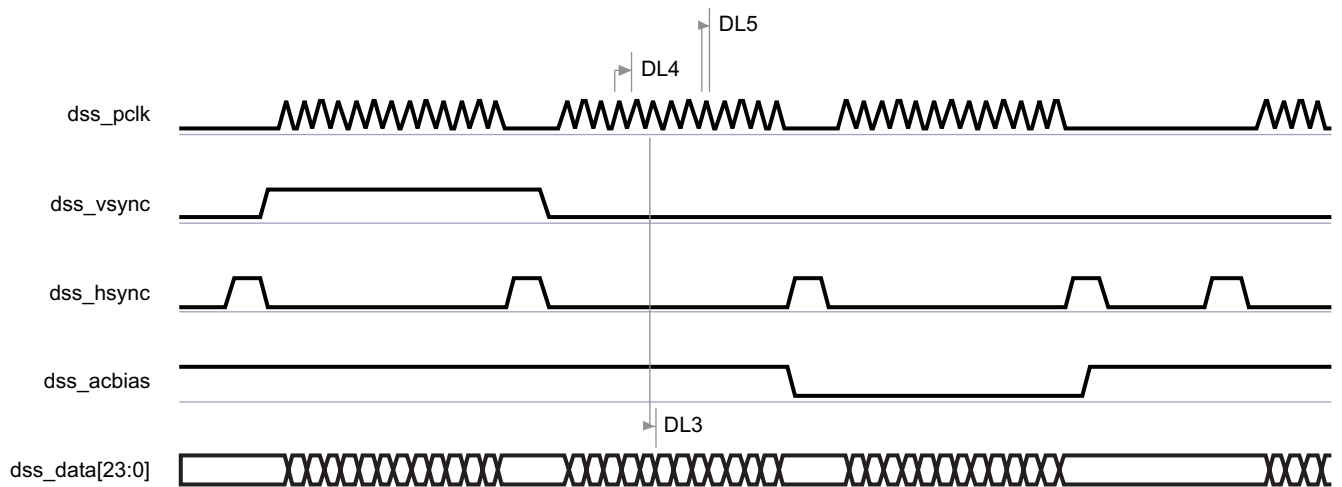


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(1) The pixel data bus depends on the use of 4-, 8-, 12-, 16-, 18-, or 24-bit per pixel data output pins.

(2) All timings not illustrated in the waveform are progammable by software, and control signal polarity and driven edge of dss_pclk too.

(3) dss_vsync width must be programmed to be as small as possible.

(4) The pixel clock frequency is programmable.

(5) For more information, see the DSS chapter in the *AM/DM37x Multimedia Device Technical Reference Manual* (literature number SPRUGN4).

**Figure 6-31. DSS—STN Mode**

### 6.5.2.2   DSS—Parallel Interface— RFBI Mode — Applications

#### 6.5.2.2.1   DSS—Parallel Interface—RFBI Mode— MIPI DBI-B 2.0 —LCD Panel

The Remote Frame Buffer Interface (RFBI) module provides the necessary control signals and data (MIPI® DBI 2.0 type B protocol) to interface to the LCD driver of the LCD panel.

Table 6-40 and Table 6-41 assume testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-32 through Figure 6-34).

#### Table 6-39. DSS Timing Conditions—RFBI Mode—MIPI DBI 2.0 - LCD Panel[2]

| TIMING CONDITION PARAMETER | | VALUE | | UNIT |
|---|---|---|---|---|
| | | MIN | MAX | |
| **Input Conditions** | | | | |
| $t_R$ | Input signal rise time | | 15 | ns |
| $t_F$ | Input signal fall time | | 15 | ns |
| **Output Condition** | | | | |
| $C_{LOAD}$ | Output load capacitance[1] | | 30 | pF |

(1) Buffer strength configuration: LB0 = 1.

(2) For any information regarding the RFBI registers configuration, see Display Subsystem / the Display Subsystem Environment / LCD Support / Parallel Interface / Parallel Interface in RFBI Mode (MIPI DBI Protocol) / Transaction Timing Diagrams section of the *AM/DM37x Multimedia Device Technical Reference Manual* (literature number SPRUGN4).

#### Table 6-40. DSS Timing Requirements—RFBI Mode—MIPI DBI 2.0 - LCD Panel

| NO. | | PARAMETER | OPP100 | | OPP50 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| DR0 | $t_{su(dV-rdH)}$ | Setup time, input data rfbi_da[15:0] valid to output read enable rfbi_rd high | 7.3 | | 6.3 | | ns |
| DR1 | $t_{h(rdH-dIV)}$ | Hold time, output read enable rfbi_rd high to input data rfbi_da[15:0] invalid | 10.6 | | 9.6 | | ns |
| | $t_{d(Data\ sampled)}$ | Input data rfbi_da[15:0] sampled at the end of the access time | N[1] | | N[1] | | ns |

(1) N = (AccessTime) * (TimeParaGranularity + 1) * L4CLK

#### Table 6-41. DSS Switching Characteristics— RFBI Mode— MIPI DBI 2.0 - LCD Panel

| PARAMETER | | OPP100 | | OPP50 | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| $t_{w(wrH)}$ | Pulse duration, output write enable rfbi_wr high | A[1] | | A[1] | | ns |
| $t_{w(wrL)}$ | Pulse duration, output write enable rfbi_wr low | B[2] | | B[2] | | ns |
| $t_{d(a0-wrL)}$ | Delay time, output command/data control rfbi_a0 transition to output write enable rfbi_wr low | C[3] | | C[3] | | ns |
| $t_{d(wrH-a0)}$ | Delay time, output write enable rfbi_wr high to output command/data control rfbi_a0 transition | D[4] | | D[4] | | ns |
| $t_{d(csx-wrL)}$ | Delay time, output chip select rfbi_csx[14] low to output write enable rfbi_wr low | E[5] | | E[5] | | ns |
| $t_{d(wrH-csxH)}$ | Delay time, output write enable rfbi_wr high to output chip select rfbi_csx[14] high | F[6] | | F[6] | | ns |
| $t_{d(dV)}$ | Output data rfbi_da[15:0] valid | G[7] | | G[7] | | ns |
| $t_{d(a0H-rdL)}$ | Delay time, output command/data control rfbi_a0 high to output read enable rfbi_rd low | H[8] | | H[8] | | ns |
| $t_{d(rdIH-a0)}$ | Delay time, output read enable rfbi_rd high to output command/data control rfbi_a0 transition | I[9] | | I[9] | | ns |
| $t_{w(rdH)}$ | Pulse duration, output read enable rfbi_rd high | J[10] | | J[10] | | ns |
| $t_{w(rdL)}$ | Pulse duration, output read enable rfbi_rd low | K[11] | | K[11] | | ns |
| $t_{d(rdL-csxL)}$ | Delay time, output read enable rfbi_rd low to output chip select rfbi_csx[14] low | L[12] | | L[12] | | ns |
| $t_{d(rdH-csxH)}$ | Delay time, output read enable rfbi_rd high to output chip select rfbi_csx[14] high | M[13] | | M[13] | | ns |
| $t_{R(wr)}$ | Rise time, output write enable rfbi_wr | | 10 | | 10 | ns |
| $t_{F(wr)}$ | Fall time, output write enable rfbi_wr | | 10 | | 10 | ns |
| $t_{R(a0)}$ | Rise time, output command/data control rfbi_a0 | | 10 | | 10 | ns |
| $t_{F(a0)}$ | Fall time, output command/data control rfbi_a0 | | 10 | | 10 | ns |
| $t_{R(csx)}$ | Rise time, output chip select rfbi_csx[14] | | 10 | | 10 | ns |

**Table 6-41. DSS Switching Characteristics— RFBI Mode— MIPI DBI 2.0 - LCD Panel (continued)**

| PARAMETER | | OPP100 | | OPP50 | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| $t_{F(csx)}$ | Fall time, output chip select rfbi_csx[14] | | 10 | | 10 | ns |
| $t_{R(d)}$ | Rise time, output data rfbi_da[15:0] | | 10 | | 10 | ns |
| $t_{F(d)}$ | Fall time, output data rfbi_da[15:0] | | 10 | | 10 | ns |
| $t_{R(rd)}$ | Rise time, output read enable rfbi_rd | | 10 | | 10 | ns |
| $t_{F(rd)}$ | Fall time, output read enable rfbi_rd | | 10 | | 10 | ns |

(1)  A = (WECycleTime – WEOffTime) * (TimeParaGranularity + 1) * L4CLK

(2)  B = (WEOffTime – WEOntime) * (TimeParaGranularity + 1) * L4CLK

(3)  C = WEOnTime * (TimeParaGranularity + 1) * L4CLK

(4)  D = (WECycleTime + CSPulseWidth – WEOffTime) * (TimeParaGranularity + 1) * L4CLK if mode Write to Read or Read to Write is enabled

(5)  E = (WEOnTime – CSOnTime) * (TimeParaGranularity + 1) * L4CLK

(6)  F = (CSOffTime – WEOffTime) * (TimeParaGranularity + 1) * L4CLK

(7)  G = WECycleTime * (TimeParaGranularity + 1) * L4CLK

(8)  H = REOnTime * (TimeParaGranularity + 1) * L4CLK

(9)  I = (RECycleTime + CSPulseWidth – REOffTime) * (TimeParaGranularity + 1) * L4CLK if mode Write to Read or Read to Write is enabled

(10) J = (RECycleTime – REOffTime) * (TimeParaGranularity + 1) * L4CLK

(11) K = (REOffTime – REOntime) * (TimeParaGranularity + 1) * L4CLK

(12) L = (REOnTime – CSOnTime) * (TimeParaGranularity + 1) * L4CLK

(13) M = (CSOffTime – REOffTime) * (TimeParaGranularity + 1) * L4CLK

(14) In rfbi_csx, x is equal to 0 or 1.



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(1)  In rfbi_csx, x is equal to 0 or 1.

(2)  rfbi_data[n:0], n up to 15

(3)  For more information, see the DSS chapter in the *AM/DM37x Multimedia Device Technical Reference Manual* (literature number SPRUGN4).

**Figure 6-32. DSS—RFBI Mode—MIPI DBI 2.0 —LCD Panel—Command / Data Write**
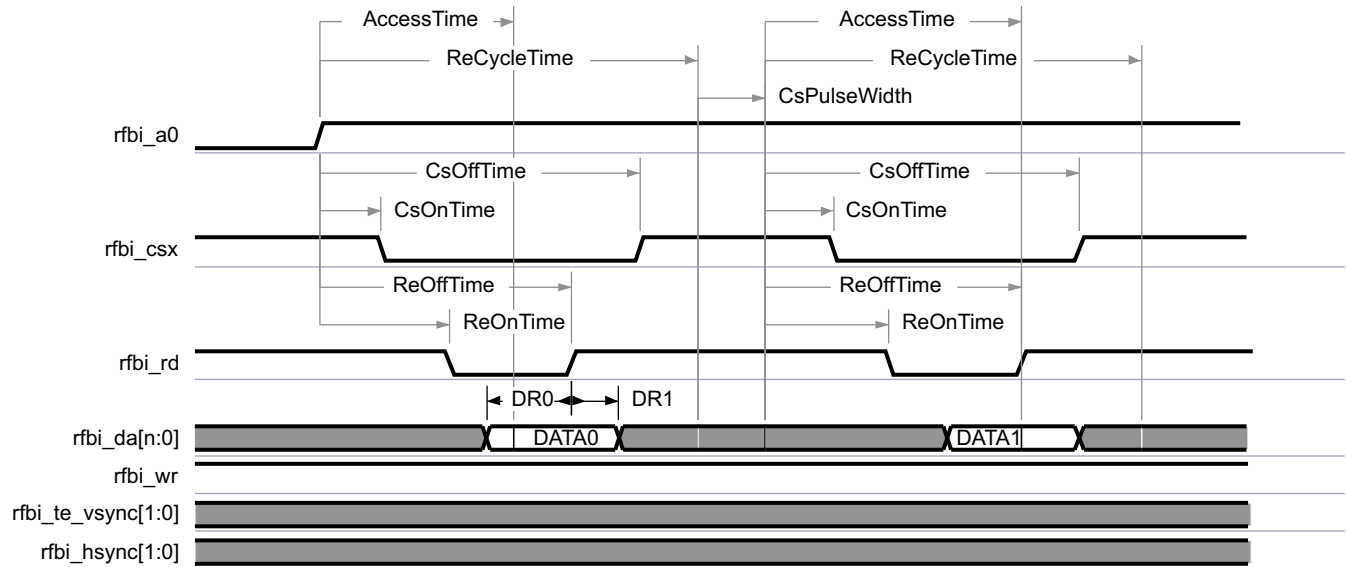
(1)  In rfbi_csx, x is equal to 0 or 1.

(2)  rfbi_data[n:0], n up to 15

(3)  For more information, see the DSS chapter in the *AM/DM37x Multimedia Device Technical Reference Manual* (literature number SPRUGN4).

**Figure 6-33. DSS—RFBI Mode—MIPI DBI 2.0 —LCD Panel—Command / Data Read**
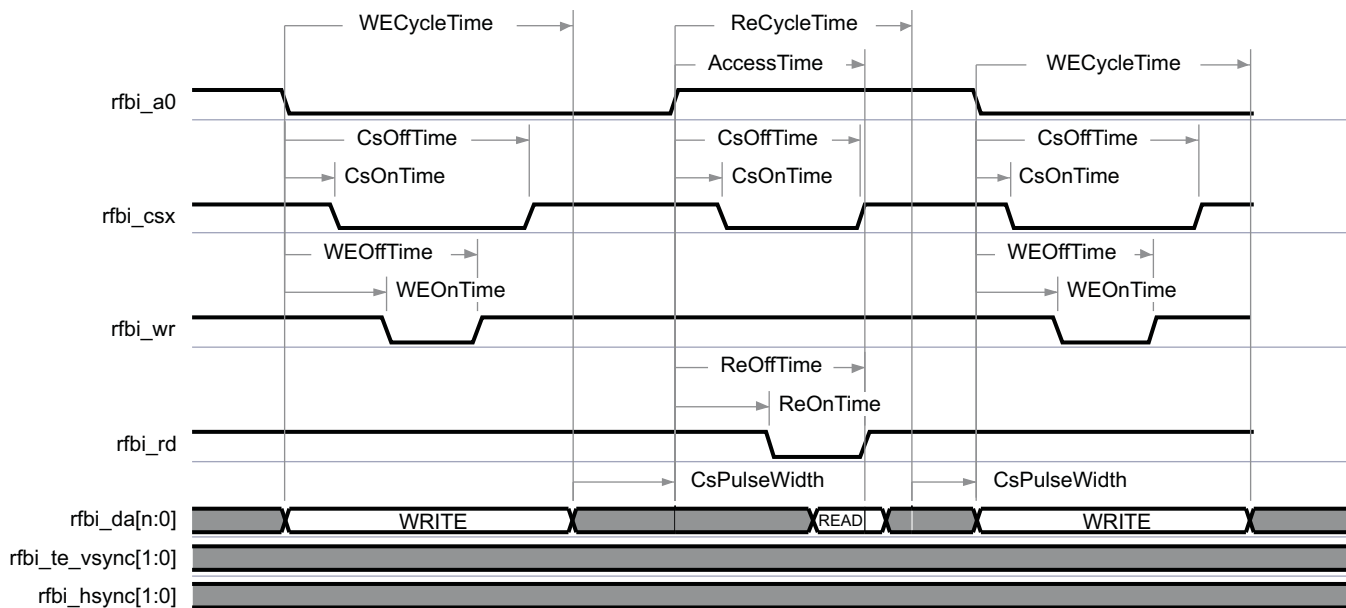


(1)  In rfbi_csx, x is equal to 0 or 1.

(2)  rfbi_data[n:0], n up to 15

(3)  For more information, see the DSS chapter in the *AM/DM37x Multimedia Device Technical Reference Manual* (literature number SPRUGN4).

**Figure 6-34. DSS—RFBI Mode—MIPI DBI 2.0 — LCD Panel—Command / Data Write to Read and Read to Write Modes**

### 6.5.2.2.2 DSS—Parallel Interface—RFBI Mode—Pico DLP

The Remote Frame Buffer Interface (RFBI) module can provide also the necessary control signals and data to interface to the Pico DLP driver of the Pico DLP panel. Table 6-42 assumes testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-35).

**Table 6-42. DSS Timing Conditions—RFBI Mode—Pico DLP**

| TIMING CONDITION PARAMETER | | VALUE | | UNIT |
|---|---|---|---|---|
| | | MIN | MAX | |
| **Output Condition** | | | | |
| $C_{LOAD}$ | Output load capacitance[1] | | 5 | pF |

(1) Buffer strength configuration: LB0 = 0

To use Pico DLP application, RFBI register must be configured as shown in Table 6-43:

**Table 6-43. DSS Register Configuration—RFBI Mode—Pico DLP**

| DESCRIPTION | REGISTER AND BIT FIELD[1] | BIT | VALUES |
|---|---|---|---|
| Selection parallel mode | RFBI_CONFIGi and ParallelMode | [1:0] | 0b11: 16-bit parallel output interface selected |
| Time Granularity (multiplies signal timing latencies by 2). | RFBI_CONFIGi andTimeGranularity | [4] | 0b0: x2 latency disable |
| CS signal assertion time from Start Access Time | RFBI_ONOFF_TIMEi and CSOnTime | [3:0] | 0b0000 |
| CS signal de-assertion time from Start Access Time | RFBI_ONOFF_TIMEi and CSOffTime | [9:4] | 0b000100: 4 cycles |
| WE signal assertion time from Start Access Time | RFBI_ONOFF_TIMEi and WEOnTime | [13:10] | 0b0000 |
| WE signal de-assertion time from Start Access Time | RFBI_ONOFF_TIMEi and WEOffTime | [19:14] | 0b000010: 2 cycles |
| RE signal assertion time from Start Access Time | RFBI_ONOFF_TIMEi and REOnTime | [23:20] | 0b0000 |
| RE signal de-assertion time from Start Access Time | RFBI_ONOFF_TIMEi and REOffTime | [29:24] | 0b000000 |
| Write cycle time | RFBI_CYCLE_TIMEi and WECycleTime | [5:0] | 0b000100: 4 cycles |
| Read cycle time | RFBI_CYCLE_TIMEi and ReCycleTime | [11:6] | 0b000000 |
| CS pulse width | RFBI_CYCLE_TIMEi and CSPulseWidth | [17:12] | 0b000000 |
| Read to Write CS pulse width enable | RFBI_CYCLE_TIMEi and RWEnable | [18] | 0b0 |
| Read to Read CS pulse width enable | RFBI_CYCLE_TIMEi and RREnable | [19] | 0b0 |
| Write to Write CS pulse width enable | RFBI_CYCLE_TIMEi and WWEnable | [20] | 0b0 |
| Write to Read CS pulse width enable | RFBI_CYCLE_TIMEi and WREnable | [21] | 0b0 |
| From Start Access Time to CLK rising edge used for the first data capture | RFBI_CYCLE_TIMEi and AccessTime | [27:22] | 0b000000 |

(1) i is equal to 0 or 1. For more information, see the DSS chapter in the *AM/DM37x Multimedia Device Technical Reference Manual* (literature number SPRUGN4).

### Table 6-44. DSS Switching Characteristics—RFBI Mode—Pico DLP[15][17][18]

| PARAMETER | | OPP100 | | OPP50 | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| $t_{w(wrH)}$ | Pulse duration, output write enable rfbi_wr high | A[1] | | A[1] | | ns |
| $t_{w(wrL)}$ | Pulse duration, output write enable rfbi_wr low | B[2] | | B[2] | | ns |
| $t_{d(a0\text{-}wrL)}$ | Delay time, output command/data control rfbi_a0 transition to output write enable rfbi_wr low | C[3] | | C[3] | | ns |
| $t_{d(wrH\text{-}a0)}$ | Delay time, output write enable rfbi_wr high to output command/data control rfbi_a0 transition | D[4] | | D[4] | | ns |
| $t_{d(csx\text{-}wrL)}$ | Delay time, output chip select rfbi_csx[14] low to output write enable rfbi_wr low | E[5] | | E[5] | | ns |
| $t_{d(wrH\text{-}csxH)}$ | Delay time, output write enable rfbi_wr high to output chip select rfbi_csx[14] high | F[6] | | F[6] | | ns |
| $t_{d(dataV)}$ | Output data rfbi_da[15:0][16] valid | G[7] | | G[7] | | ns |
| $t_{d(Skew)}$ | Skew between output write enable falling rfbi_wr and output data rfbi_da[15:0][16] high or low | 15.5 | | 15.5 | | ns |
| $t_{d(a0H\text{-}rdL)}$ | Delay time, output command/data control rfbi_a0 high to output read enable rfbi_rd low | H[8] | | H[8] | | ns |
| $t_{d(rdlH\text{-}a0)}$ | Delay time, output read enable rfbi_rd high to output command/data control rfbi_a0 transition | I[9] | | I[9] | | ns |
| $t_{w(rdH)}$ | Pulse duration, output read enable rfbi_rd high | J[10] | | J[10] | | ns |
| $t_{w(rdL)}$ | Pulse duration, output read enable rfbi_rd low | K[11] | | K[11] | | ns |
| $t_{d(rdL\text{-}csxL)}$ | Delay time, output read enable rfbi_rd low to output chip select rfbi_csx[14] low | L[12] | | L[12] | | ns |
| $t_{d(rdL\text{-}csxH)}$ | Delay time, output read enable rfbi_rd low to output chip select rfbi_csx[14] high | M[13] | | M[13] | | ns |
| $t_{R(wr)}$ | Rise time, output write enable rfbi_wr | | 7 | | 7 | ns |
| $t_{F(wr)}$ | Fall time, output write enable rfbi_wr | | 7 | | 7 | ns |
| $t_{R(a0)}$ | Rise time, output command/data control rfbi_a0 | | 7 | | 7 | ns |
| $t_{F(a0)}$ | Fall time, output command/data control rfbi_a0 | | 7 | | 7 | ns |
| $t_{R(csx)}$ | Rise time, output chip select rfbi_csx[14] | | 7 | | 7 | ns |
| $t_{F(csx)}$ | Fall time, output chip select rfbi_csx[14] | | 7 | | 7 | ns |
| $t_{R(d)}$ | Rise time, output data rfbi_da[15:0][16] | | 7 | | 7 | ns |
| $t_{F(d)}$ | Fall time, output data rfbi_da[15:0][16] | | 7 | | 7 | ns |
| $t_{R(rd)}$ | Rise time, output read enable rfbi_rd | | 7 | | 7 | ns |
| $t_{F(rd)}$ | Fall time, output read enable rfbi_rd | | 7 | | 7 | ns |
| CsOnTime | CS signal assertion time from Start Access Time - RFBI_ONOFF_TIMEi Register | 0[19] | | | | ns |
| CsOffTime | CS signal de-assertion time from Start Access Time - RFBI_ONOFF_TIMEi Register | 40[19] | | | | ns |
| WeOnTime | WE signal assertion time from Start Access Time - RFBI_ONOFF_TIMEi Register | 0[19] | | | | ns |
| WeOffTime | WE signal de-assertion time from Start Access Time - RFBI_ONOFF_TIMEi Register | 20[19] | | | | ns |
| ReOnTime | RE signal assertion time from Start Access Time - RFBI_ONOFF_TIMEi Register | - | | | | ns |
| ReOffTime | RE signal de-assertion time from Start Access Time - RFBI_ONOFF_TIMEi Register | - | | | | ns |
| WeCycleTime | Write cycle time - RFBI_CYCLE_TIMEi Register | 40[19] | | | | ns |
| ReCycleTime | Read cycle time - RFBI_CYCLE_TIMEi Register | - | | | | ns |
| CsPulseWidth | CS pulse width - RFBI_CYCLE_TIMEi Register | 0[19] | | | | ns |

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(1) A = (WECycleTime – WEOffTime) * (TimeParaGranularity + 1) * L4CLK

(2) B = (WEOffTime – WEOntime) * (TimeParaGranularity + 1) * L4CLK

(3) C = WEOnTime * (TimeParaGranularity + 1) * L4CLK

(4) D = (WECycleTime + CSPulseWidth – WEOffTime) * (TimeParaGranularity + 1) * L4CLK if mode Write to Read or Read to Write is enabled.

(5) E = (WEOnTime – CSOnTime) * (TimeParaGranularity + 1) * L4CLK

(6) F = (CSOffTime – WEOffTime) * (TimeParaGranularity + 1) * L4CLK

(7) G = WECycleTime * (TimeParaGranularity + 1) * L4CLK

(8) H = REOnTime * (TimeParaGranularity + 1) * L4CLK

(9) I = (RECycleTime + CSPulseWidth – REOffTime) * (TimeParaGranularity + 1) * L4CLK if mode Write to Read or Read to Write is enabled.

(10) J = (RECycleTime – REOffTime) * (TimeParaGranularity + 1) * L4CLK

(11) K = (REOffTime – REOntime) * (TimeParaGranularity + 1) * L4CLK

(12) L = (REOnTime – CSOnTime) * (TimeParaGranularity + 1) * L4CLK

(13) M = (CSOffTime – REOffTime) * (TimeParaGranularity + 1) * L4CLK

(14) In rfbi_csx, x is equal to 0 or 1.

(15) See Section 4.3.4, *Processor Clocks*.

(16) 16-bit parallel output interface is selected in DSS register.

(17) At OPP100, L4 clock is 100 MHz and at OPP50, L4 clock is 50 MHz.

(18) rfbi_wr must be at 25 MHz.

(19) These values are calculated by the following formula: RFBI Register (Value) * L4 Clock (ns).
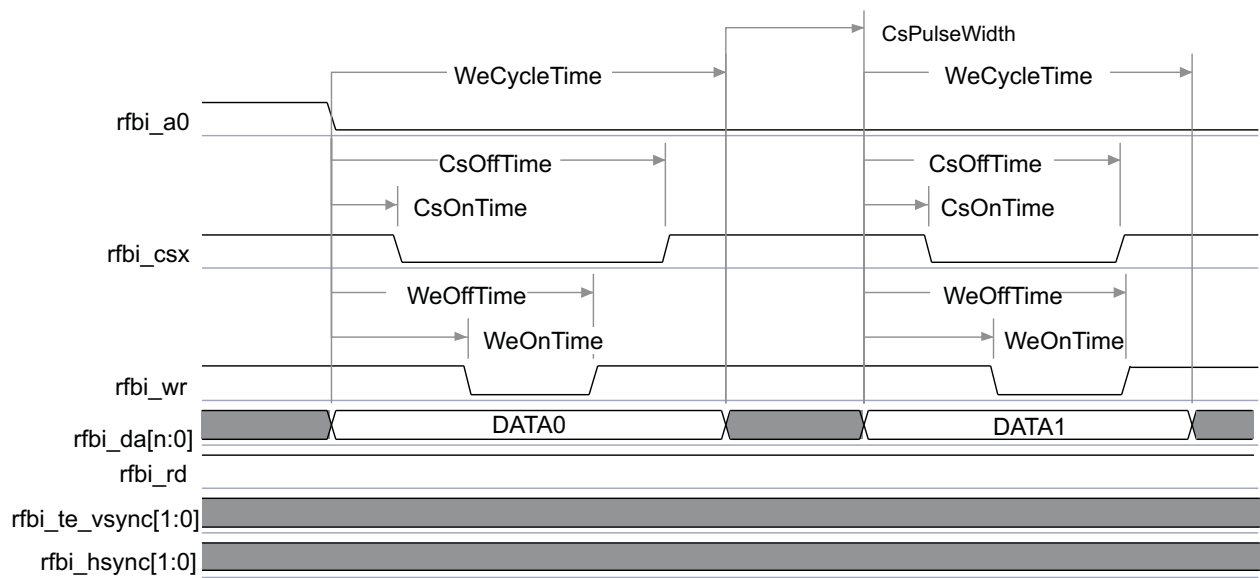


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**Figure 6-35. DSS—RFBI Mode—Pico DLP—Command / Data Write[1][2]**

(1) In rfbi_csx, x is equal to 0 or 1.

(2) rfbi_da[n:0], n up to 15

## 6.6 Serial Communications Interfaces

### 6.6.1 Multichannel Buffered Serial Port (McBSP)

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**NOTE**

For more information, see Multi-Channel Buffered Serial Port chapter of the *AM/DM37x Multimedia Device Technical Reference Manual* (literature number SPRUGN4).

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The Multichannel Buffered Serial Port (McBSP) provides a full duplex direct serial interface between the chip and other devices in a system such as other application chips, codecs. It can accommodate a wide range of peripherals and clocked frame oriented protocols (I2S, PCM, T ) due to its high level of versatility.

McBSP may support two types of data transfer at the system level:

- The full cycle mode, for which one clock period is used to transfer the data, generated on one edge and captured on the same edge (one clock period later).
- The half cycle mode, for which one half clock period is used to transfer the data, generated on one edge and captured on the opposite edge (one half clock period later). Note that a new data is generated only every clock period, which secures the required hold time.

The interface clock (clkx/clkr) activation edge (data/frame sync capture and generation) has to be configured accordingly with the external peripheral (activation edge capability) and the type of data transfer required at the system level.

Depending on the number of pins, McBSP supports either:

- 6-pin mode: dx and dr as data pins; clkx, clkr, fsx, and fsr as control pins
- 4-pin mode: dx and dr as data pins; clkx and fsx pins as control pins. The clkx and fsx pins are internally looped back, via software configuration, respectively to the clkr and fsr internal signals for data receive.

McBSP1 supports the 6-pin mode. McBSP2, 3, 4, and 5 support only the 4-pin mode.

The following sections describe the timing characteristics for applications in normal mode (that is, McBSPx connected to one peripheral) and T applications in multipoint mode.

#### 6.6.1.1 McBSP Timing Conditions—Normal Mode

Table 6-46 through Table 6-70 assume testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-36 through Figure 6-43).

**Table 6-45. McBSP Timing Conditions—Normal Mode**

| TIMING CONDITION PARAMETER | | VALUE | UNIT |
|---|---|---|---|
| **Input Conditions** | | | |
| $t_R$ | Input signal rise time | 2 | ns |
| $t_F$ | Input signal fall time | 2 | ns |
| **Output Condition** | | | |
| $C_{LOAD}$ | Output load capacitance[1] | 10 | pF |

(1) Buffer strength configuration:
   – McBSP4 - Set #1: LB0 = 1.
   – Otherwise: LB0 = 0.

**Table 6-46. McBSP Output Clock Characteristics—Normal Mode[4]**

| PARAMETER | | | | OPP100 | | OPP50 | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | MIN | MAX | |
| McBSP1 | tc(CLK) | Cycle time, mcbsp1_clkx (multiplexing mode 0) / mcbsp1_clkr (multiplexing mode 0 & 2) | | | 48 | | 24 | MHz |
| McBSP2 | tc(CLK) | Cycle time, mcbsp2_clkx (multiplexing mode 0) | | | 48 | | 24 | MHz |
| McBSP3 | tc(CLK) | Cycle time, mcbsp3_clkx | IO set 1 (multiplexing mode 0) | | 32 | | 16 | MHz |
| | | | IO set 2 (multiplexing mode 1) | | 48 | | 24 | |
| | | | IO set 3 (multiplexing mode 2) | | 48 | | 24 | |
| McBSP4 | tc(CLK) | Cycle time, mcbsp4_clkx | IO set 1 (multiplexing mode 0) | | 48 | | 16 | MHz |
| | | | IO set 3 (multiplexing mode 2) | | 32 | | 16 | |
| McBSP5 | tc(CLK) | Cycle time, mcbsp5_clkx | IO set 2 (multiplexing mode 1) | | 32 | | 16 | MHz |
| $t_{W(CLKH)}$ | Typical pulse duration, mcbsp1_clkr / mcbspx_clkx high[2] | | | 0.5*P[1] | | 0.5*P[1] | | ns |
| $t_{W(CLKL)}$ | Typical pulse duration, mcbsp1_clkr / mcbspx_clkx low[2] | | | 0.5*P[1] | | 0.5*P[1] | | ns |
| $t_{dc(CLK)}$ | Duty cycle error, mcbsp1_clkr / mcbspx_clkx[2] | | | −0.75 | 0.75 | −0.75 | 0.75 | ns |
| | Jitter, mcbsp1_clkr / mcbspx_clkx[3] / mcbsp_clks | | | -0.40 | 0.40 | -0.40 | 0.40 | ns |

(1)  P = mcbspy_clkx[2] or mcbsp1_clkr output clock period in ns

(2)  In mcbspy, y is equal to 1, 2, 3, 4, or 5.

(3)  In mcbspx, x identifies the McBSP number: 1, 2, 3, 4, or 5.

(4)  See Section 4.3.4, *Processor Clocks*.

### 6.6.1.1.1  Rising Edge as Activation Mode

### 6.6.1.1.1.1  Timing with Rising Edge as Activation Edge—Receive Mode

## Table 6-47. McBSP1, 2, and 3 (Sets #2 and #3) Timing Requirements—Rising Edge and Receive Mode[1] [2]

| NO. | PARAMETER | | | OPP100 | | OPP50 | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | MIN | MAX | |
| B3 | $t_{su(DRV-CLKAE)}$ | Setup time, mcbspx_dr valid before mcbsp1_clkr / mcbspx_clkx active edge | Master | 4.36 | | 8.63 | | ns |
| | | | Slave | 3.67 | | 7.94 | | ns |
| B4 | $t_{h(CLKAE-DRV)}$ | Hold time, mcbspx_dr valid after mcbsp1_clkr / mcbspx_clkx active edge | Master | 1.01 | | 1.01 | | ns |
| | | | Slave | 0.4 | | 0.4 | | ns |
| B5 | $t_{su(FSV-CLKAE)}$ | Setup time, mcbsp1_fsr / mcbspx_fsx valid before mcbsp1_clkr / mcbspx_clkx active edge | | 3.67 | | 7.94 | | ns |
| B6 | $t_{h(CLKAE-FSV)}$ | Hold time, mcbsp1_fsr / mcbspx_fsx valid after mcbsp1_clkr / mcbspx_clkx active edge | | 0.5 | | 0.5 | | ns |

(1) In mcbspx, x identifies the McBSP number: 1, 2, or 3. Note that for the McBSP3, these timings concern only Set #2 (multiplexing mode on UART pins) and Set #3 (multiplexing mode on McBSP1 pins).

(2) See Section 4.3.4, *Processor Clocks*.

### Table 6-48. McBSP1, 2, and 3 (Sets #2 and #3) Switching Characteristics—Rising Edge and Receive Mode[1] [2]

| NO. | PARAMETER | | OPP100 | | OPP50 | | UNIT |
|-----|-----------|---|--------|-----|-------|-----|------|
| | | | MIN | MAX | MIN | MAX | |
| B2 | $t_{d(CLKAE-FSV)}$ | Delay time, mcbsp1_clkr / mcbspx_clkx active edge to mcbsp1_fsr / mcbspx_fsx valid | 0.7 | 14.79 | 0.7 | 29.58 | ns |

(1) In mcbspx, x identifies the McBSP number: 1, 2, or 3. Note that for the McBSP3, these timings concern only Set #2 (multiplexing mode on UART pins) and Set #3 (multiplexing mode on McBSP1 pins).

(2) See Section 4.3.4, *Processor Clocks*.

### Table 6-49. McBSP4 (Set #1) Timing Requirements—Rising Edge and Receive Mode[1] [2]

| NO. | PARAMETER | | OPP100 | | OPP50 | | UNIT |
|-----|-----------|---|--------|-----|-------|-----|------|
| | | | MIN | MAX | MIN | MAX | |
| B3 | $t_{su(DRV-CLKXAE)}$ | Setup time, mcbspx_dr valid before mcbspx_clkx active edge | Master | 2.87 | | 8.63 | | ns |
| | | | Slave | 3.67 | | 7.94 | | ns |
| B4 | $t_{h(CLKXAE-DRV)}$ | Hold time, mcbspx_dr valid after mcbspx_clkx active edge | Master | 1.01 | | 1.01 | | ns |
| | | | Slave | 0.4 | | 0.4 | | ns |
| B5 | $t_{su(FSXV-CLKXAE)}$ | Setup time, mcbspx_fsx valid before mcbspx_clkx active edge | | 3.67 | | 7.94 | | ns |
| B6 | $t_{h(CLKXAE-FSXV)}$ | Hold time, mcbspx_fsx valid after mcbspx_clkx active edge | | 0.5 | | 0.5 | | ns |

(1) In mcbspx, x identifies the McBSP number: 4. Note that for the McBSP4, these timings concern only Set #1: multiplexing mode by default. The McBSP4 is also multiplexed on GPMC pins (Set #2): the corresponding timings are specified in Table 6-51 and Table 6-52.

(2) See Section 4.3.4, *Processor Clocks*.

### Table 6-50. McBSP4 (Set #1) Switching Characteristics—Rising Edge and Receive Mode[1] [2]

| NO. | PARAMETER | | OPP100 | | OPP50 | | UNIT |
|-----|-----------|---|--------|-----|-------|-----|------|
| | | | MIN | MAX | MIN | MAX | |
| B2 | $t_{d(CLKXAE-FSXV)}$ | Delay time, mcbspx_clkx active edge to mcbspx_fsx valid | 0.7 | 16.56 | 0.7 | 33.12 | ns |

(1) In mcbspx, x identifies the McBSP number: 4. Note that for the McBSP4, these timings concern only Set #1: multiplexing mode by default. The McBSP4 is also multiplexed on GPMC pins (Set #2): the corresponding timings are specified in Table 6-51 and Table 6-52.

(2) See Section 4.3.4, *Processor Clocks*.

### Table 6-51. McBSP3 (Set #1), 4 (Set #2), and 5 Timing Requirements—Rising Edge and Receive Mode[1] [2]

| NO. | PARAMETER | | OPP100 | | OPP50 | | UNIT |
|-----|-----------|---|--------|-----|-------|-----|------|
| | | | MIN | MAX | MIN | MAX | |
| B3 | $t_{su(DRV-CLKXAE)}$ | Setup time, mcbspx_dr valid before mcbspx_clkx active edge | Master | 6.49 | | 12.90 | | ns |
| | | | Slave | 5.80 | | 12.21 | | ns |
| B4 | $t_{h(CLKXAE-DRV)}$ | Hold time, mcbspx_dr valid after mcbspx_clkx active edge | Master | 1.01 | | 1.01 | | ns |
| | | | Slave | 0.4 | | 0.4 | | ns |
| B5 | $t_{su(FSXV-CLKXAE)}$ | Setup time, mcbspx_fsx valid before mcbspx_clkx active edge | | 5.81 | | 12.21 | | ns |
| B6 | $t_{h(CLKXAE-FSXV)}$ | Hold time, mcbspx_fsx valid after mcbspx_clkx active edge | | 0.5 | | 0.5 | | ns |

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(1) In mcbspx, x identifies the McBSP number: 3, 4, or 5. Note that for the McBSP3, these timings concern only Set #1: multiplexing mode by default. The McBSP3 is also multiplexed on UART pins (Set #2) and on McBSP1 pins (Set #3): the corresponding timings are specified in Table 6-47 and Table 6-48.
For the McBSP4, these timings concern only Set #2 (multiplexing mode on GPMC pins).
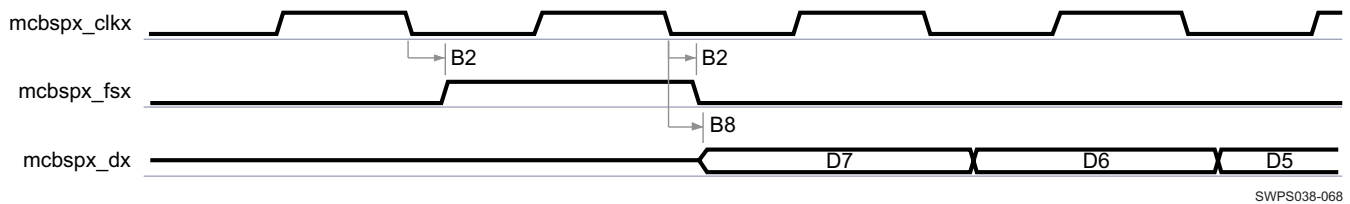
(2) See Section 4.3.4, *Processor Clocks*.

**Table 6-52. McBSP3 (Set #1), 4 (Set #2), and 5 Switching Characteristics—Rising Edge and Receive Mode[1] [2]**

| NO. | PARAMETER | | OPP100 | | OPP50 | | UNIT |
|-----|-----------|---|--------|--------|--------|--------|------|
| | | | MIN | MAX | MIN | MAX | |
| B2 | $t_{d(CLKXAE-FSXV)}$ | Delay time, mcbspx_clkx active edge to mcbspx_fsx valid | 0.7 | 22.18 | 0.7 | 44.37 | ns |

(1) In mcbspx, x identifies the McBSP number: 3, 4, or 5. Note that for the McBSP3, these timings concern only Set #1: multiplexing mode by default. The McBSP3 is also multiplexed on UART pins (Set #2) and on McBSP1 pins (Set #3): the corresponding timings are specified in Table 6-47 and Table 6-48.
For the McBSP4, these timings concern only Set #2 (multiplexing mode on GPMC pins)

(2) See Section 4.3.4, *Processor Clocks*.



SWPS038-062
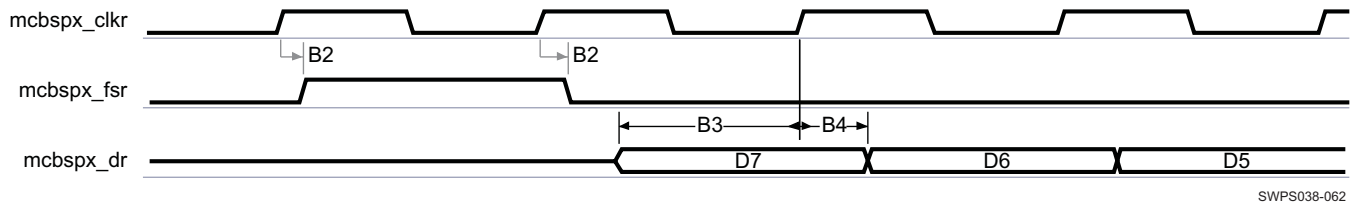
(1) In mcbspx, x identifies the McBSP number: 1, 2, 3, 4, or 5.

**Figure 6-36. McBSP Rising Edge Receive Timing in Master Mode**



SWPS038-063
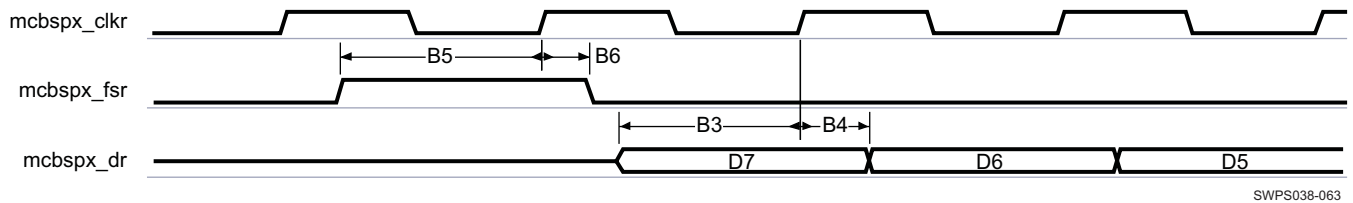
(1) In mcbspx, x identifies the McBSP number: 1, 2, 3, 4, or 5.

**Figure 6-37. McBSP Rising Edge Receive Timing in Slave Mode**

*6.6.1.1.1.2 Timing with Rising Edge as Activation Edge—Transmit Mode*

**Table 6-53. McBSP1, 2, and 3 (Sets #2 and #3) Timing Requirements—Rising Edge and Transmit Mode[1] [2]**

| NO. | PARAMETER | | OPP100 | | OPP50 | | UNIT |
|-----|-----------|---|--------|-----|--------|-----|------|
| | | | MIN | MAX | MIN | MAX | |
| B5 | $t_{su(FSXV-CLKXAE)}$ | Setup time, mcbspx_fsx valid before mcbspx_clkx active edge | 3.67 | | 7.94 | | ns |
| B6 | $t_{h(CLKXAE-FSXV)}$ | Hold time, mcbspx_fsx valid after mcbspx_clkx active edge | 0.5 | | 0.5 | | ns |

(1)  In mcbspx, x identifies the McBSP number: 1, 2, or 3. Note that for the McBSP3, these timings concern only Set #2 (multiplexing mode on UART pins) and Set #3 (multiplexing mode on McBSP1 pins).

(2)  See Section 4.3.4, *Processor Clocks.*

### Table 6-54. McBSP1, 2, and 3 (Sets #2 and #3) Switching Characteristics—Rising Edge and Transmit Mode[1] [2]

| NO. | PARAMETER | | OPP100 | | OPP50 | | UNIT |
|-----|-----------|--|--------|--|-------|--|------|
| | | | MIN | MAX | MIN | MAX | |
| B2 | $t_{d(CLKXAE-FSXV)}$ | Delay time, mcbspx_clkx active edge to mcbspx_fsx valid | 0.7 | 14.79 | 0.7 | 29.58 | ns |
| B8 | $t_{d(CLKXAE-DXV)}$ | Delay time, mcbspx_clkx active edge to mcbspx_dx valid | Master | 0.6 | 14.79 | 0.6 | 29.58 | ns |
| | | | Slave | 0.6 | 13.89 | 0.6 | 28.68 | ns |

(1)  In mcbspx, x identifies the McBSP number: 1, 2, or 3. Note that for the McBSP3, these timings concern only Set #2 (multiplexing mode on UART pins) and Set #3 (multiplexing mode on McBSP1 pins).

(2)  See Section 4.3.4, *Processor Clocks.*

### Table 6-55. McBSP4 (Set #1) Timing Requirements—Rising Edge and Transmit Mode[1] [2]

| NO. | PARAMETER | | OPP100 | | OPP50 | | UNIT |
|-----|-----------|--|--------|--|-------|--|------|
| | | | MIN | MAX | MIN | MAX | |
| B5 | $t_{su(FSXV-CLKXAE)}$ | Setup time, mcbspx_fsx valid before mcbspx_clkx active edge | 3.67 | | 7.94 | | ns |
| B6 | $t_{h(CLKXAE-FSXV)}$ | Hold time, mcbspx_fsx valid after mcbspx_clkx active edge | 0.5 | | 0.5 | | ns |

(1)  In mcbspx, x identifies the McBSP number: 4. Note that for the McBSP4, these timings concern only Set #1: multiplexing mode by default. The McBSP4 is also multiplexed on GPMC pins (Set #2): the corresponding timings are specified in Table 6-57 and Table 6-58.

(2)  See Section 4.3.4, *Processor Clocks.*

### Table 6-56. McBSP4 (Set #1) Switching Characteristics—Rising Edge and Transmit Mode[1] [2]

| NO. | PARAMETER | | OPP100 | | OPP50 | | UNIT |
|-----|-----------|--|--------|--|-------|--|------|
| | | | MIN | MAX | MIN | MAX | |
| B2 | $t_{d(CLKXAE-FSXV)}$ | Delay time, mcbspx_clkx active edge to mcbspx_fsx valid | 0.7 | 16.56 | 0.7 | 33.12 | ns |
| B8 | $t_{d(CLKXAE-DXV)}$ | Delay time, mcbspx_clkx active edge to mcbspx_dx valid | Master | 0.6 | 16.56 | 0.6 | 33.12 | ns |
| | | | Slave | 0.6 | 17.15 | 0.6 | 32.22 | ns |

(1)  In mcbspx, x identifies the McBSP number: 4. Note that for the McBSP4, these timings concern only Set #1: multiplexing mode by default. The McBSP4 is also multiplexed on GPMC pins (Set #2): the corresponding timings are specified in Table 6-57 and Table 6-58.

(2)  See Section 4.3.4, *Processor Clocks.*

### Table 6-57. McBSP3 (Set #1), 4 (Set #2), and 5 Timing Requirements—Rising Edge and Transmit Mode[1] [2]

| NO. | PARAMETER | | OPP100 | | OPP50 | | UNIT |
|-----|-----------|--|--------|--|-------|--|------|
| | | | MIN | MAX | MIN | MAX | |
| B5 | $t_{su(FSXV-CLKXAE)}$ | Setup time, mcbspx_fsx valid before mcbspx_clkx active edge | 5.81 | | 12.21 | | ns |
| B6 | $t_{h(CLKXAE-FSXV)}$ | Hold time, mcbspx_fsx valid after mcbspx_clkx active edge | 0.5 | | 0.5 | | ns |

(1)  In mcbspx, x identifies the McBSP number: 3, 4, or 5. Note that for the McBSP3, these timings concern only Set #1: multiplexing mode by default. The McBSP3 is also multiplexed on UART pins (Set #2) and on McBSP1 pins (Set #3): the corresponding timings are specified in Table 6-53 and Table 6-54.
For the McBSP4, these timings concern only Set #2 (multiplexing mode on GPMC pins).

(2)  See Section 4.3.4, *Processor Clocks.*

**Table 6-58. McBSP3 (Set #1), 4 (Set #2), and 5 Switching Characteristics—Rising Edge and Transmit Mode[1] [2]**

| NO. | PARAMETER | | OPP100 | | OPP50 | | UNIT |
|-----|-----------|---|--------|---|-------|---|------|
| | | | MIN | MAX | MIN | MAX | |
| B2 | $t_{d(CLKXAE-FSXV)}$ Delay time, mcbspx_clkx active edge to mcbspx_fsx valid | | 0.7 | 22.18 | 0.7 | 44.37 | ns |
| B8 | $t_{d(CLKXAE-DXV)}$ Delay time, mcbspx_clkx active edge to mcbspx_dx valid | Master | 0.6 | 21.28 | 0.6 | 43.47 | ns |
| | | Slave | 0.6 | 21.28 | 0.6 | 43.47 | ns |

(1) In mcbspx, x identifies the McBSP number: 3, 4, or 5. Note that for the McBSP3, these timings concern only Set #1: multiplexing mode by default. The McBSP3 is also multiplexed on UART pins (Set #2) and on McBSP1 pins (Set #3): the corresponding timings are specified in Table 6-53 and Table 6-54.
For the McBSP4, these timings concern only Set #2 (multiplexing mode on GPMC pins).

(2) See Section 4.3.4, *Processor Clocks.*



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(1)    In mcbspx, x identifies the McBSP number: 1, 2, 3, 4, or 5.

**Figure 6-38. McBSP Rising Edge Transmit Timing in Master Mode**
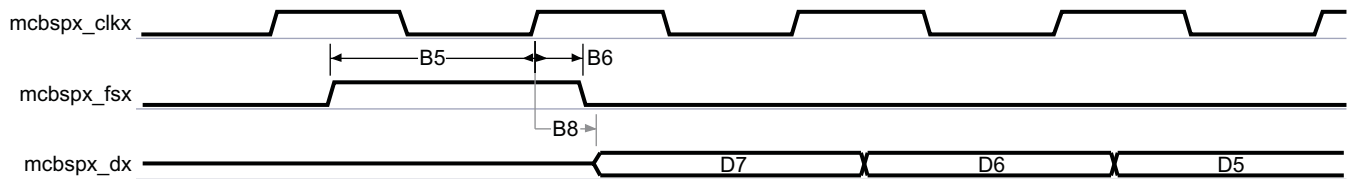


SWPS038-065

(1)    In mcbspx, x identifies the McBSP number: 1, 2, 3, 4, or 5.

**Figure 6-39. McBSP Rising Edge Transmit Timing in Slave Mode**

### 6.6.1.1.2   Falling Edge as Activation Edge

### 6.6.1.1.2.1   Timing with Falling Edge as Activation Edge Mode—Receive Mode

**Table 6-59. McBSP1, 2, 3 (Sets #2 and #3) Timing Requirements—Falling Edge and Receive Mode[1] [2]**

| NO. | PARAMETER | | OPP100 | | OPP50 | | UNIT |
|-----|-----------|---|--------|---|-------|---|------|
| | | | MIN | MAX | MIN | MAX | |
| B3 | $t_{su(DRV-CLKAE)}$ Setup time, mcbspx_dr valid before mcbsp1_clkr / mcbspx_clkx active edge | Master | 4.36 | | 8.63 | | ns |
| | | Slave | 3.67 | | 7.94 | | ns |
| B4 | $t_{h(CLKAE-DRV)}$ Hold time, mcbspx_dr valid after mcbsp1_clkr / mcbspx_clkx active edge | Master | 1.01 | | 1.01 | | ns |
| | | Slave | 0.4 | | 0.4 | | ns |
| B5 | $t_{su(FSV-CLKAE)}$ Setup time, mcbsp1_fsr / mcbspx_fsx valid before mcbsp1_clkr / mcbspx_clkx active edge | | 3.7 | | 7.94 | | ns |
| B6 | $t_{h(CLKAE-FSV)}$ Hold time, mcbsp1_fsr / mcbspx_fsx valid after mcbsp1_clkr / mcbspx_clkx active edge | | 0.5 | | 0.5 | | ns |

(1) In mcbspx, x identifies the McBSP number: 1, 2, or 3. Note that for the McBSP3, these timings concern only Set #2 (multiplexing mode on UART pins) and Set #3 (multiplexing mode on McBSP1 pins).

(2) See Section 4.3.4, *Processor Clocks*.

### Table 6-60. McBSP1, 2, and 3 (Sets #2 and #3) Switching Characteristics—Falling Edge and Receive Mode[1] [2]

| NO. | PARAMETER | | OPP100 | | OPP50 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| B2 | $t_{d(CLKAE-FSV)}$ | Delay time, mcbsp1_clkr / mcbspx_clkx active edge to mcbsp1_fsr / mcbspx_fsx valid | 0.7 | 14.79 | 0.7 | 29.58 | ns |

(1) In mcbspx, x identifies the McBSP number: 1, 2, or 3. Note that for the McBSP3, these timings concern only Set #2 (multiplexing mode on UART pins) and Set #3 (multiplexing mode on McBSP1 pins).

(2) See Section 4.3.4, *Processor Clocks*.

### Table 6-61. McBSP4 (Set #1) Timing Requirements—Falling Edge and Receive Mode[1] [2]

| NO. | PARAMETER | | OPP100 | | OPP50 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| B3 | $t_{su(DRV-CLKXAE)}$ | Setup time, mcbspx_dr valid before mcbspx_clkx active edge | Master | 2.87 | | 8.63 | | ns |
| | | | Slave | 3.67 | | 7.94 | | ns |
| B4 | $t_{h(CLKXAE-DRV)}$ | Hold time, mcbspx_dr valid after mcbspx_clkx active edge | Master | 1.01 | | 1.01 | | ns |
| | | | Slave | 0.4 | | 0.4 | | ns |
| B5 | $t_{su(FSXV-CLKXAE)}$ | Setup time, mcbspx_fsx valid before mcbspx_clkx active edge | | 3.67 | | 7.94 | | ns |
| B6 | $t_{h(CLKXAE-FSXV)}$ | Hold time, mcbspx_fsx valid after mcbspx_clkx active edge | | 0.5 | | 0.5 | | ns |

(1) In mcbspx, x identifies the McBSP number: 4. Note that for the McBSP4, these timings concern only Set #1: multiplexing mode by default. The McBSP4 is also multiplexed on GPMC pins (Set #2): the corresponding timings are specified in Table 6-63 and Table 6-64.

(2) See Section 4.3.4, *Processor Clocks*.

### Table 6-62. McBSP4 (Set #1) Switching Characteristics—Falling Edge and Receive Mode[1] [2]

| NO. | PARAMETER | | OPP100 | | OPP50 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| B2 | $t_{d(CLKXAE-FSXV)}$ | Delay time, mcbspx_clkx active edge to mcbspx_fsx valid | 0.7 | 16.56 | 0.7 | 33.12 | ns |

(1) In mcbspx, x identifies the McBSP number: 4. Note that for the McBSP4, these timings concern only Set #1: multiplexing mode by default. The McBSP4 is also multiplexed on GPMC pins (Set #2): the corresponding timings are specified in Table 6-63 and Table 6-64.

(2) See Section 4.3.4, *Processor Clocks*.

### Table 6-63. McBSP3 (Set #1), 4 (Set #2), and 5 Timing Requirements—Falling Edge and Receive Mode[1] [2]

| NO. | PARAMETER | | OPP100 | | OPP50 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| B3 | $t_{su(DRV-CLKXAE)}$ | Setup time, mcbspx_dr valid before mcbspx_clkx active edge | Master | 6.5 | | 12.9 | | ns |
| | | | Slave | 5.81 | | 12.21 | | ns |
| B4 | $t_{h(CLKXAE-DRV)}$ | Hold time, mcbspx_dr valid after mcbspx_clkx active edge | Master | 1.01 | | 1.01 | | ns |
| | | | Slave | 0.4 | | 0.4 | | ns |
| B5 | $t_{su(FSXV-CLKXAE)}$ | Setup time, mcbspx_fsx valid before mcbspx_clkx active edge | | 5.81 | | 12.21 | | ns |
| B6 | $t_{h(CLKXAE-FSXV)}$ | Hold time, mcbspx_fsx valid after mcbspx_clkx active edge | | 0.5 | | 0.5 | | ns |

(1) In mcbspx, x identifies the McBSP number: 3, 4, or 5. Note that for the McBSP3, these timings concern only Set #1: multiplexing mode by default. The McBSP3 is also multiplexed on UART pins (Set #2) and on McBSP1 pins (Set #3): the corresponding timings are specified in Table 6-59 and Table 6-60.
For the McBSP4, these timings concern only Set #2 (multiplexing mode on GPMC pins).

(2) See Section 4.3.4, *Processor Clocks.*

### Table 6-64. McBSP3 (Set #1), 4 (Set #2), and 5 Switching Characteristics—Falling Edge and Receive Mode[1] [2]

| NO. | PARAMETER | | OPP100 | | OPP50 | | UNIT |
|-----|-----------|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| B2 | $t_{d(CLKXAE-FSXV)}$ | Delay time, mcbspx_clkx active edge to mcbspx_fsx valid | 0.7 | 22.19 | 0.7 | 44.37 | ns |

(1) In mcbspx, x identifies the McBSP number: 3, 4, or 5. Note that for the McBSP3, these timings concern only Set #1: multiplexing mode by default. The McBSP3 is also multiplexed on UART pins (Set #2) and on McBSP1 pins (Set #3): the corresponding timings are specified in Table 6-59 and Table 6-60.

(2) See Section 4.3.4, *Processor Clocks.*



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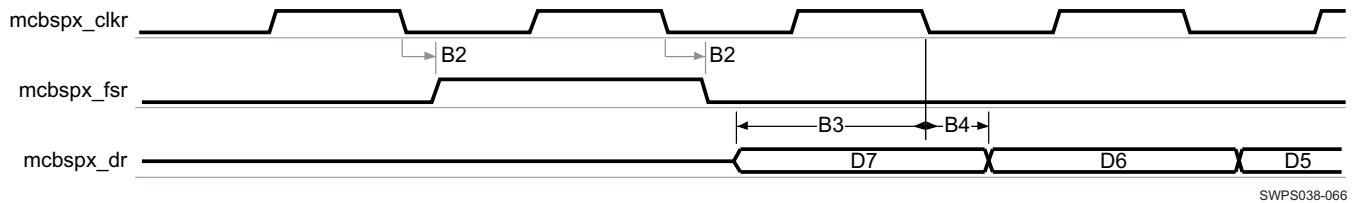
(1) In mcbspx, x identifies the McBSP number: 1, 2, 3, 4, or 5.

**Figure 6-40. McBSP Falling Edge Receive Timing in Master Mode**



SWPS038-067
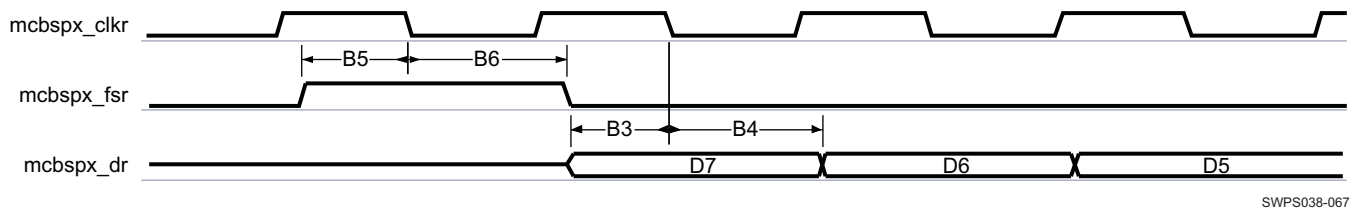
(1) In mcbspx, x identifies the McBSP number: 1, 2, 3, 4, or 5.

**Figure 6-41. McBSP Falling Edge Receive Timing in Slave Mode**

### 6.6.1.1.2.2 Timing with Falling Edge as Activation Edge—Transmit Mode

### Table 6-65. McBSP1, 2, and 3 (Sets #2 and #3) Timing Requirements—Falling Edge and Transmit Mode[1][2]

| NO. | PARAMETER | | OPP100 | | OPP50 | | UNIT |
|-----|-----------|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| B5 | $t_{su(FSXV-CLKXAE)}$ | Setup time, mcbspx_fsx valid before mcbspx_clkx active edge | 3.67 | | 7.94 | | ns |
| B6 | $t_{h(CLKXAE-FSXV)}$ | Hold time, mcbspx_fsx valid after mcbspx_clkx active edge | 0.5 | | 0.5 | | ns |

(1) In mcbspx, x identifies the McBSP number: 1, 2, or 3. Note that for the McBSP3, these timings concern only Set #2 (multiplexing mode on UART pins) and Set #3 (multiplexing mode on McBSP1 pins).

(2) See Section 4.3.4, *Processor Clocks.*

### Table 6-66. McBSP1, 2, and 3 (Sets #2 and #3) Switching Characteristics—Falling Edge and Transmit Mode[1][2]

| NO. | PARAMETER | | OPP100 | | OPP50 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| B2 | $t_{d(CLKXAE-FSXV)}$ | Delay time, mcbspx_clkx active edge to mcbspx_fsx valid | 0.7 | 14.79 | 0.7 | 29.58 | ns |
| B8 | $t_{d(CLKXAE-DXV)}$ | Delay time, mcbspx_clkx active edge to mcbspx_dx valid | Master | 0.6 | 14.79 | 0.6 | 29.58 | ns |
| | | | Slave | 0.6 | 13.89 | 0.6 | 28.68 | ns |

(1) In mcbspx, x identifies the McBSP number: 1, 2, or 3. Note that for the McBSP3, these timings concern only Set #2 (multiplexing mode on UART pins) and Set #3 (multiplexing mode on McBSP1 pins).

(2) See Section 4.3.4, *Processor Clocks.*

### Table 6-67. McBSP4 (Set #1) Timing Requirements—Falling Edge and Transmit Mode[1][2]

| NO. | PARAMETER | OPP100 | | OPP50 | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| B5 | $t_{su(FSXV-CLKXAE)}$ Setup time, mcbspx_fsx valid before mcbspx_clkx active edge | 3.67 | | 7.94 | | ns |
| B6 | $t_{h(CLKXAE-FSXV)}$ Hold time, mcbspx_fsx valid after mcbspx_clkx active edge | 0.5 | | 0.5 | | ns |

(1) In mcbspx, x identifies the McBSP number: 4. Note that for the McBSP4, these timings concern only Set #1: multiplexing mode by default. The McBSP4 is also multiplexed on GPMC pins (Set #2): the corresponding timings are specified in Table 6-69 and Table 6-70.

(2) See Section 4.3.4, *Processor Clocks.*

### Table 6-68. McBSP4 (Set #1) Switching Characteristics—Falling Edge and Transmit Mode[1] [2]

| NO. | PARAMETER | | OPP100 | | OPP50 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| B2 | $t_{d(CLKXAE-FSXV)}$ | Delay time, mcbspx_clkx active edge to mcbspx_fsx valid | 0.7 | 16.56 | 0.7 | 33.12 | ns |
| B8 | $t_{d(CLKXAE-DXV)}$ | Delay time, mcbspx_clkx active edge to mcbspx_dx valid | Master | 0.6 | 16.56 | 0.6 | 33.12 | ns |
| | | | Slave | 0.6 | 17.15 | 0.6 | 32.22 | ns |

(1) In mcbspx, x identifies the McBSP number: 4. Note that for the McBSP4, these timings concern only Set #1: multiplexing mode by default. The McBSP4 is also multiplexed on GPMC pins (Set #2): the corresponding timings are specified in Table 6-69 and Table 6-70.

(2) See Section 4.3.4, *Processor Clocks.*

### Table 6-69. McBSP3 (Set #1), 4 (Set #2), and 5 Timing Requirements—Falling Edge and Transmit Mode[1] [2]

| NO. | PARAMETER | OPP100 | | OPP50 | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| B5 | $t_{su(FSXV-CLKXAE)}$ Setup time, mcbspx_fsx valid before mcbspx_clkx active edge | 5.81 | | 12.21 | | ns |
| B6 | $t_{h(CLKXAE-FSXV)}$ Hold time, mcbspx_fsx valid after mcbspx_clkx active edge | 0.5 | | 0.5 | | ns |

(1) In mcbspx, x identifies the McBSP number: 3, 4, or 5. Note that for the McBSP3, these timings concern only Set #1: multiplexing mode by default. The McBSP3 is also multiplexed on UART pins (Set #2) and on McBSP1 pins (Set #3): the corresponding timings are specified in Table 6-66 and Table 6-67.
For the McBSP4, these timings concern only Set #2 (multiplexing mode on GPMC pins).

(2) See Section 4.3.4, *Processor Clocks.*

### Table 6-70. McBSP3 (Set #1), 4 (Set #2), and 5 Switching Characteristics—Falling Edge and Transmit Mode[1] [2]

| NO. | PARAMETER | | OPP100 | | OPP50 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| B2 | $t_{d(CLKXAE-FSXV)}$ Delay time, mcbspx_clkx active edge to mcbspx_fsx valid | | 0.7 | 22.18 | 0.7 | 44.37 | ns |
| B8 | $t_{d(CLKXAE-DXV)}$ Delay time, mcbspx_clkx active edge to mcbspx_dx valid | Master | 0.6 | 21.28 | 0.6 | 43.47 | ns |
| | | Slave | 0.6 | 21.28 | 0.6 | 43.47 | ns |

(1)  In mcbspx, x identifies the McBSP number: 3, 4, or 5. Note that for the McBSP3, these timings concern only Set #1: multiplexing mode by default. The McBSP3 is also multiplexed on UART pins (Set #2) and on McBSP1 pins (Set #3): the corresponding timings are specified in Table 6-66 and Table 6-67.
For the McBSP4, these timings concern only Set #2 (multiplexing mode on GPMC pins).

(2)  See Section 4.3.4, *Processor Clocks*.



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(1)   In mcbspx, x identifies the McBSP number: 1, 2, 3, 4, or 5.

**Figure 6-42. McBSP Falling Edge Transmit Timing in Master Mode**



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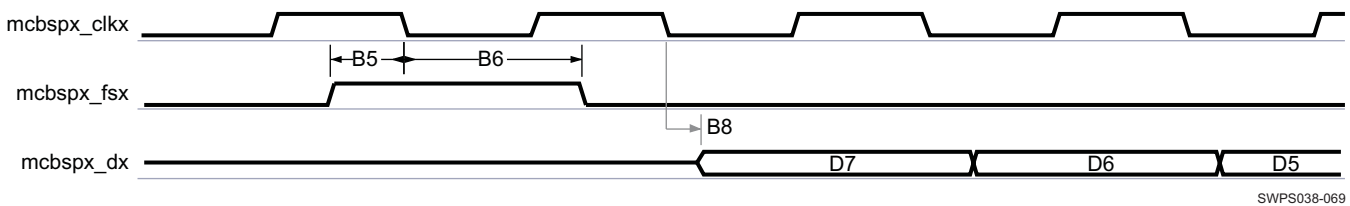
(1)   In mcbspx, x identifies the McBSP number: 1, 2, 3, 4, or 5.

**Figure 6-43. McBSP Falling Edge Transmit Timing in Slave Mode**

#### 6.6.1.2    McBSP in TDM —Multipoint Mode (McBSP3)

For T application in multipoint mode, the processor is considered as a slave. Table 6-72 and Table 6-73 assume testing over the operating conditions and electrical characteristic conditions described below.

### Table 6-71. McBSP3 (Set #3) Timing Conditions—T Multipoint Mode[1]

| TIMING CONDITION PARAMETER | | VALUE | | UNIT |
|---|---|---|---|---|
| | | MIN | MAX | |
| **Input Conditions** | | | | |
| $t_R$ | Input signal rise time | 1.0 | 8.5 | ns |
| $t_F$ | Input signal fall time | 1.0 | 8.5 | ns |
| **Output Condition** | | | | |
| $C_{LOAD}$ | Output load capacitance[2] | | 40 | pF |

(1)  For McBSP3, these timings concern only Set #3 (multiplexing mode in McBSP1 pins)

(2)  The load setting of the IO buffer: LB0 = 0.

### Table 6-72. McBSP3 (Set #3) Timing Requirements—T Multipoint Mode[4]

| NO. | PARAMETER | | OPP100 | | OPP50 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| | $1 / t_{c(clkxH)}$ | Frequency, input clock mcbsp3_clkx | | 6 | | 6 | MHz |

## Table 6-72. McBSP3 (Set #3) Timing Requirements—T Multipoint Mode[4] (continued)

| NO. | PARAMETER | | OPP100 | | OPP50 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| | $t_{w(clkxH)}$ | Pulse duration, input clock mcbsp3_clkx high | 0.5P[1] | | 0.5P[1] | | ns |
| | $t_{w(clkxL)}$ | Pulse duration, input clock mcbsp3_clkx low | 0.5P[1] | | 0.5P[1] | | ns |
| | $t_{dc(clkx)}$ | Duty cycle error, input clock mcbsp3_clkx | −8.14 | 8.14 | −8.14 | 8.14 | ns |
| B3[3] | $t_{su(drV-clkxAE)}$ | Setup time, input data mcbsp3_dr valid before input clock mcbsp3_clkx active edge | 9 | | 9 | | ns |
| B4[3] | $t_{h(clkxAE-drV)}$ | Hold time, input data mcbsp3_dr valid after input clock mcbsp3_clkx active edge | 2.4 | | 2.4 | | ns |
| B5[3] | $t_{su(fsxV-clkxAE)}$ | Setup time, input frame synchronization mcbsp3_fsx valid before input clock mcbsp3_clkx active edge | 9 | | 9 | | ns |
| B6[3] | $t_{h(clkxAE-fsxV)}$ | Hold time, input frame synchronization mcbsp3_fsx valid after input clock mcbsp3_clkx active edge | 2.4 | | 2.4 | | ns |

(1)  P = input clock mcbsp3_clkx period in ns

(2)  For McBSP3, these timings concern only Set #3 (multiplexing mode in McBSP1 pins).

(3)  See Section 6.6.1.1 for corresponding figures.

(4)  See Section 4.3.4, *Processor Clocks*.

## Table 6-73. McBSP3 (Set #3) Switching Characteristics—T Multipoint Mode[1]

| NO. | PARAMETER | | OPP100 | | OPP50 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| B8[2] | $t_{d(clkxAE-dxV)}$ | Delay time, mcbsp3_clkx active edge to output data mcbsp3_dx valid | 0.6 | 15.89 | 0.6 | 28.68 | ns |

(1)  For McBSP3, these timings concern only Set #3 (multiplexing mode in McBSP1 pins).

(2)  See Section 6.6.1.1 for corresponding figures.

## 6.6.2 Multichannel Serial Port Interface (McSPI)

**NOTE**

For more information, see Multichannel SPI chapter of the *AM/DM37x Multimedia Device Technical Reference Manual* (literature number SPRUGN4).

McSPI allows a duplex, synchronous, serial communication between a local host and SPI compliant external devices. The following timings are applicable to the different configurations of McSPI in master/slave mode for any McSPI and any channel (n).

### 6.6.2.1 McSPI—Slave Mode

In slave mode, McSPI initiates data transfer on the data lines (mcspix_somi, mcspix_simo) when it receives an SPI clock (mcspix_clk) from the external SPI master device.

Table 6-75 and Table 6-76 assume testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-44 and Figure 6-45).

**Table 6-74. McSPI Timing Conditions—Slave Mode**

| TIMING CONDITION PARAMETER | | VALUE | UNIT |
|---|---|---|---|
| **Input Conditions** | | | |
| $t_R$ | Input signal rise time | 4 | ns |
| $t_F$ | Input signal fall time | 4 | ns |
| **Output Condition** | | | |
| $C_{LOAD}$ | Output load capacitance[1] | 20 | pF |

(1) The load setting of the IO buffer: LB0 = 1.

**Table 6-75. McSPI Timing Requirements—Slave Mode[1] [3]**

| NO. | PARAMETER | | OPP100 | | OPP50 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| SS0 | $1/t_{c(CLK)}$ | Frequency, mcspix_clk | | 24 | | 12 | MHz |
| SS1 | $t_{w(CLK)}$ | Pulse duration, mcspix_clk high or low | 0.45*P[2] | 0.55*P[2] | 0.45*P[2] | 0.55*P[2] | ns |
| SS2 | $t_{su(SIMOV\text{-}CLKAE)}$ | Setup time, mcspix_simo valid before mcspix_clk active edge | 4.2 | | 9.5 | | ns |
| SS3 | $t_{h(SIMOV\text{-}CLKAE)}$ | Hold time, mcspix_simo valid after mcspix_clk active edge | 4.6 | | 9.9 | | ns |
| SS4 | $t_{su(CS0V\text{-}CLKFE)}$ | Setup time, mcspix_cs0 valid before mcspix_clk first edge | 13.8 | | 28.6 | | ns |
| SS5 | $t_{h(CS0I\text{-}CLKLE)}$ | Hold time, mcspix_cs0 invalid after mcspix_clk last edge | 13.8 | | 28.6 | | ns |

(1) In mcspix, x is equal to 1, 2, 3, or 4.

(2) P = mcspix_clk clock period

(3) See Section 4.3.4, *Processor Clocks*.

**Table 6-76. McSPI Switching Characteristics—Slave Mode[1] [3] [4]**

| NO. | PARAMETER | | OPP100 | | OPP50 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| SS6 | $t_{d(CLKAE-SOMIV)}$ Delay time, mcspix_clk active edge to mcspix_somi shifted | | 1.8 | 15.9 | 3.2 | 31.7 | ns |
| SS7 | $t_{d(CS0AE-SOMIV)}$ Delay time, mcspix_cs0 active edge to mcspix_somi shifted | Modes 0 and 2[2] | | 15.9 | | 31.7 | ns |

(1) In mcspix, x is equal to 1, 2, 3, or 4.

(2) The polarity of mcspix_clk and the active edge (rising or falling) on which mcspix_simo is driven and mcspix_somi is latched is all software configurable:

– mcspix_clk[1] phase programmable with the bit PHA of MCSPI_CH(i)CONF register: PHA = 0 (Modes 0 and 2)
For more information, see the McSPI environment chapter, Data Format Configurations section of the *AM/DM37x Multimedia Device Technical Reference Manual* (literature number SPRUGN4) for modes and phase correspondence description.

(3) This timing applies to all configurations regardless of mcspix_clk polarity and which clock edges are used to drive output data and capture input data.

(4) See Section 4.3.4, *Processor Clocks.*
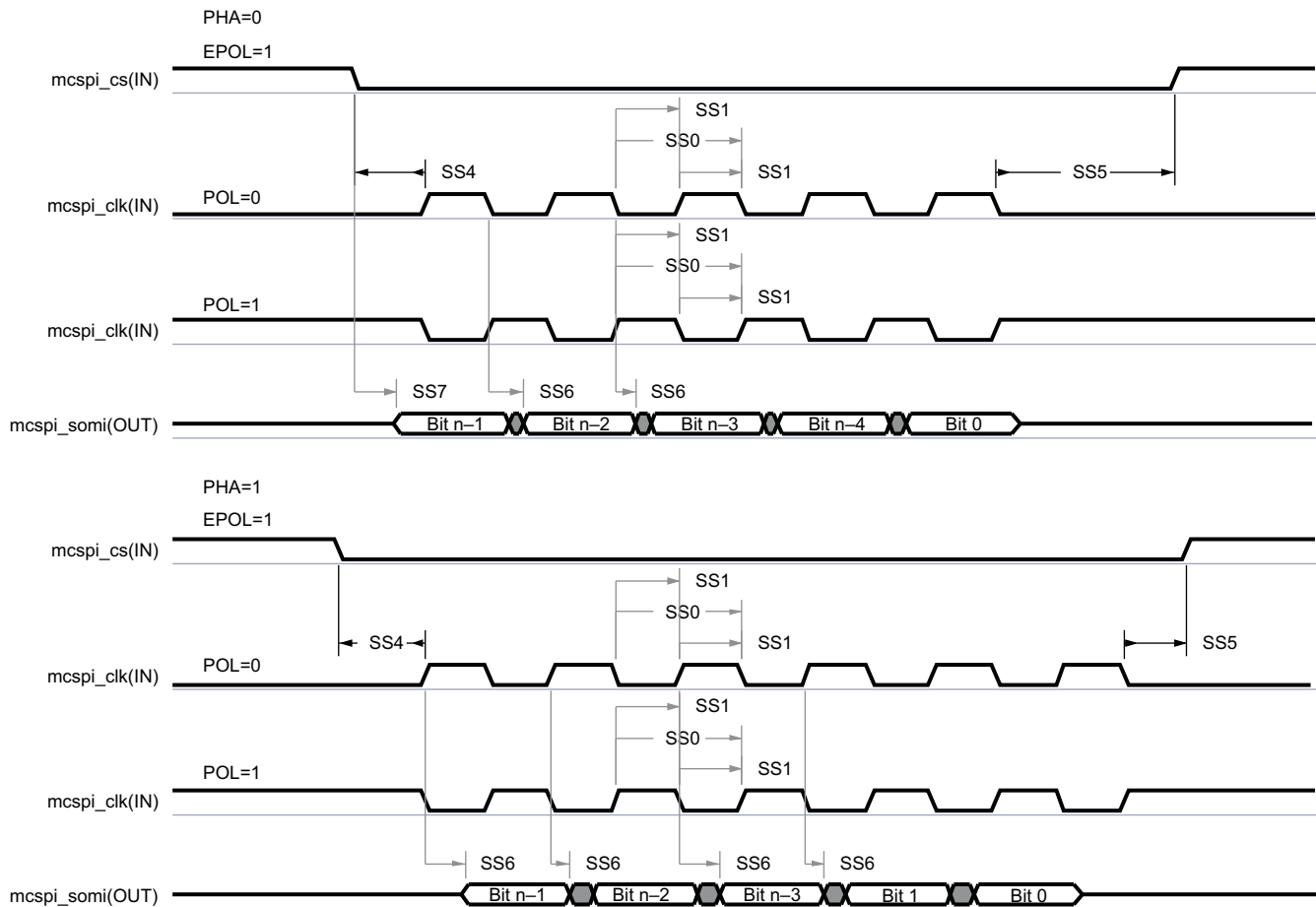


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(1) The active clock edge selection of mcspi_clk (rising or falling) on which mcspi_simo is driven and mcspi_somi data is latched is software configurable with the bit MCSPI_CH(i)CONF[1] = POL and the bit MCSPI_CH(i)CONF[0] = PHA.

(2) The polarity of mcspi_cs is software configurable with the bit MCSPI_CH(i)CONF[6] = EPOL.

**Figure 6-44. McSPI—Slave Mode—Transmit**

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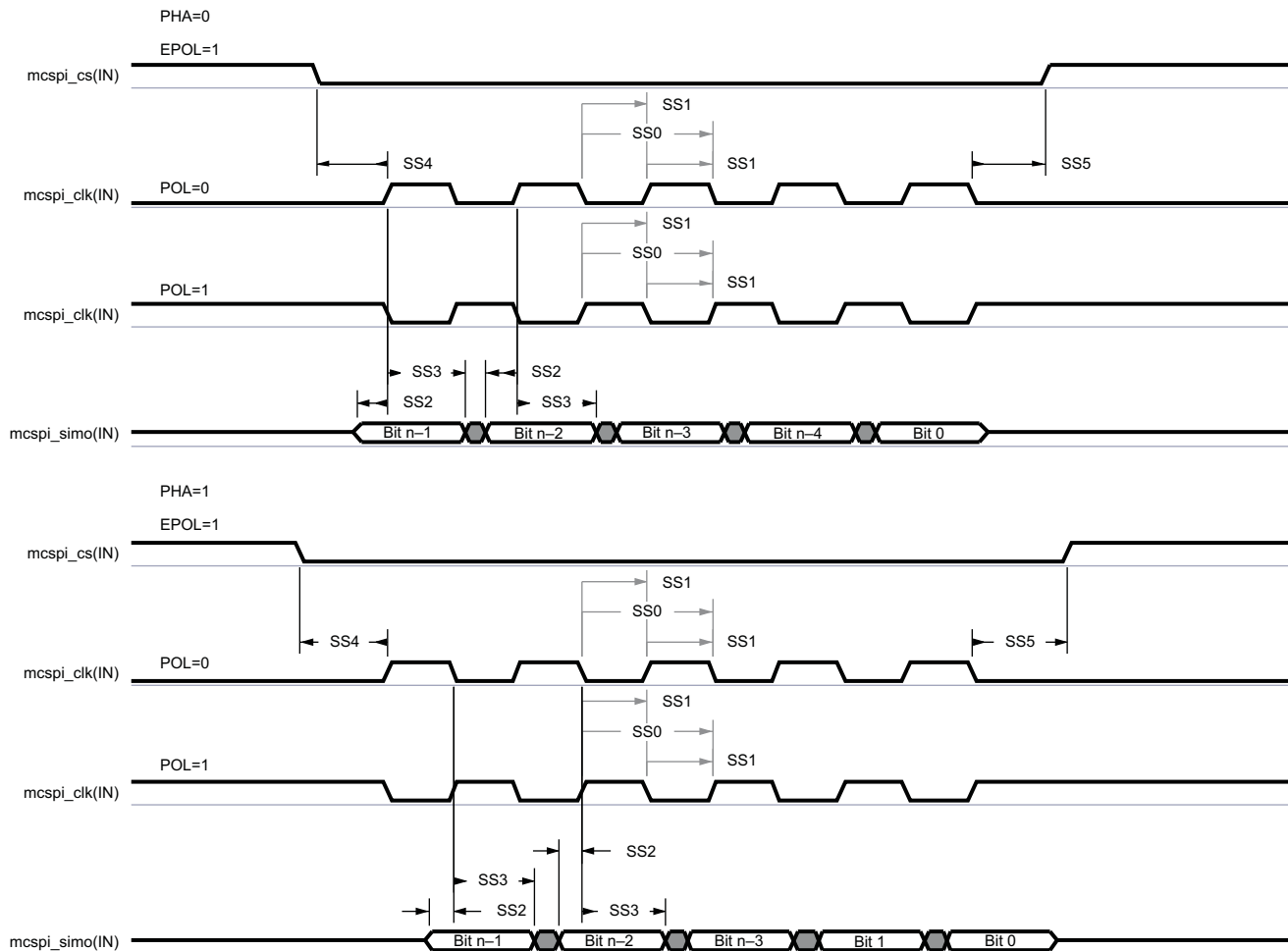
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(1)  The active clock edge selection of mcspi_clk (rising or falling) on which mcspi_simo is driven and mcspi_somi data is latched is software configurable with the bit MCSPI_CH(i)CONF[1] = POL and the bit MCSPI_CH(i)CONF[0] = PHA.

(2)  The polarity of mcspi_cs is software configuable with the bit MCSPI_CH(i)CONF[6] = EPOL.

**Figure 6-45. McSPI—Slave Mode—Receive**

### 6.6.2.2 McSPI—Master Mode

In master mode, McSPI supports multichannel communication. McSPI initiates a data transfer on the data lines (SPIDAT [1:0]) and generates clock (SPICLK) and control signals (SPIEN) to a single SPI slave device at a time.

Table 6-78 and Table 6-81 assume testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-46 and Figure 6-47).

**Table 6-77. McSPI Timing Conditions—Master Mode[1]**

| TIMING CONDITION PARAMETER | | VALUE | | UNIT |
|---|---|---|---|---|
| | | MIN | MAX | |
| **Input Conditions** | | | | |
| $t_R$ | Input signal rise time | | 4 | ns |
| $t_F$ | Input signal fall time | | 4 | ns |
| **Output Conditions** | | | | |
| **McSPI1, McSPI2, McSPI3, and McSPI4** | | | | |
| $C_{LOAD}$ | Output load capacitance for spix_csn signals | | 20 | pF |
| **McSPI2 and McSPI3** | | | | |
| $C_{LOAD}$ | Output load capacitance for spix_clk and spix_simo | | 30 | pF |
| **McSPI1 and McSPI4** | | | | |
| $C_{LOAD}$ | Output load capacitance for spix_clk and spix_simo | | 20 | pF |

(1) Buffer strength configuration: LB0 = 1.

**Table 6-78. McSPI1, 2, and 4 Timing Requirements—Master Mode[1] [2]**

| NO. | PARAMETER | | OPP100 | | OPP50 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| SM2 | $t_{su(SOMIV-CLKAE)}$ | Setup time, mcspix_somi valid before mcspix_clk active edge | 1.1 | | 1.5 | | ns |
| SM3 | $t_{h(SOMIV-CLKAE)}$ | Hold time, mcspix_somi valid after mcspix_clk active edge | 1.9 | | 2.8 | | ns |

(1) In mcspix, x is equal to 1, 2, or 4. In mcspix_csn, n is equal to 0, 1, 2, or 3 for x equal to 1, n is equal to 0 or 1 for x equal to 2 and 4.

(2) See Section 4.3.4, *Processor Clocks.*

**Table 6-79. McSPI1, 2, and 4 Switching Characteristics—Master Mode[1] [6]**

| NO. | PARAMETER | | OPP100 | | OPP50 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| SM0 | $1/t_{c(CLK)}$ | Frequency, mcspix_clk | | 48 | | 24 | MHz |
| SM1 | $t_{w(CLK)}$ | Pulse duration, mcspix_clk high or low | 0.45*P[3] | 0.55*P[3] | 0.45*P[3] | 0.55*P[3] | ns |
| | $t_{R(clk)}$ | Rise time, output clock mcspi1_clk and mcspi4_clk | | 5.72 | | 5.68 | ns |
| | | Rise time, output clock mcspi2_clk | | 7.33 | | 7.31 | |
| | $t_{F(clk)}$ | Fall time, output clock mcspi1_clk and mcspi4_clk | | 5.22 | | 5.21 | ns |
| | | Fall time, output clock mcspi2_clk | | 6.77 | | 6.71 | |
| SM4 | $t_{d(CLKAE-SIMOV)}$ | Delay time, mcspix_clk active edge to mcspix_simo shifted | −2.1 | 5.0 | −2.1 | 11.3 | ns |
| SM5 | $t_{d(CSnA-CLKFE)}$ | Delay time, mcspix_csi active to mcspix_clk first edge | Modes 1 and 3[2] | A[4] − 3.2 | | A[4] − 4.4 | | ns |
| | | | Modes 0 and 2[2] | B[5] − 3.2 | | B[5] − 4.4 | | ns |
| SM6 | $t_{d(CLKLE-CSnI)}$ | Delay time, mcspix_clk last edge to mcspix_csi inactive | Modes 1 and 3[2] | B[5] − 3.2 | | B[5] − 4.4 | | ns |
| | | | Modes 0 and 2[2] | A[4] − 3.2 | | A[4] − 4.4 | | ns |
| SM7 | $t_{d(CSnAE-SIMOV)}$ | Delay time, mcspix_csi active edge to mcspix_simo shifted | | 5.0 | | 11.3 | ns |

(1) In mcspix, x is equal to 1, 2, or 4. In mcspix_csn, n is equal to 0, 1, 2, or 3 for x equal to 1, n is equal to 0 or 1 for x equal to 2 and 4.

(2) The polarity of mcspix_clk and the active edge (rising or falling) on which mcspix_simo is driven and mcspix_somi is latched is all software configurable:
   – mcspix_clk[(1)] phase programmable with the bit PHA of MCSPI_CH(i)CONF register: PHA = 1 (Modes 1 and 3).
   – mcspix_clk[(1)] phase programmable with the bit PHA of MCSPI_CH(i)CONF register: PHA = 0 (Modes 0 and 2).
   For more information, see the McSPI environment chapter, Data Format Configurations section of the *AM/DM37x Multimedia Device Technical Reference Manual* (literature number SPRUGN4) for modes and phase correspondence description.

(3) P = mcspix_clk clock period

(4) Case P = 20.8 ns, A = (TCS+0.5)*P[(3)] (TCS is a bit field of MSPI_CHCONFx[26:25] register).
   Case P > 20.8 ns, A = TCS*P[(3)] (TCS is a bitfield of MSPI_CHCONFx[26:25] register). For more information, see the McSPI chapter of the *AM/DM37x Multimedia Device Technical Reference Manual* (literature number SPRUGN4).

(5) B = TCS*P[(3)] (TCS is a bit field of MSPI_CHCONFx[26:25] register). For more information, see the McSPI chapter of the *AM/DM37x Multimedia Device Technical Reference Manual* (literature number SPRUGN4).

(6) See Section 4.3.4, *Processor Clocks*.

### Table 6-80. McSPI3 Timing Requirements—Master Mode[(1)]

| NO. | PARAMETER | | OPP100 | | OPP50 | | UNIT |
|-----|-----------|---|--------|-----|--------|-----|------|
| | | | MIN | MAX | MIN | MAX | |
| SM2 | $t_{su(SOMIV-CLKAE)}$ | Setup time, mcspi3_somi valid before mcspi3_clk active edge | 1.5 | | 4.3 | | ns |
| SM3 | $t_{h(SOMIV-CLKAE)}$ | Hold time, mcspi3_somi valid after mcspi3_clk active edge | 2.8 | | 5.9 | | ns |

(1) See Section 4.3.4, *Processor Clocks*.

### Table 6-81. McSPI3 Switching Characteristics—Master Mode[(1) (2) (6)]

| NO. | PARAMETER | | OPP100 | | OPP50 | | UNIT |
|-----|-----------|---|--------|-----|--------|-----|------|
| | | | MIN | MAX | MIN | MAX | |
| SM0 | $1/t_{c(CLK)}$ | Frequency, mcspi3_clk | | | 24 | | 12 | MHz |
| SM1 | $t_{w(CLKH)}$ | Pulse duration, mcspi3_clk high or low | | 0.45*P[(3)] | 0.55*P[(3)] | 0.45*P[(3)] | 0.55*P[(3)] | ns |
| | $t_{R(clk)}$ | Rise time, output clock mcspi3_clk | CBP Balls: AE2 / AE13 | | 7.33 | | 7.31 | ns |
| | | | CBP Ball: H26 | | 4.31 | | 4.30 | |
| | $t_{F(clk)}$ | Fall time, output clock mcspi3_clk | CBP Balls: AE2 / AE13 | | 6.77 | | 6.71 | ns |
| | | | CBP Ball: H26 | | 4.0 | | 4.0 | |
| SM4 | $t_{d(CLK-SIMO)}$ | Delay time, mcspi3_clk active edge to mcspi3_simo shifted | | –2.1 | 11.3 | –5.3 | 23.6 | ns |
| SM5 | $t_{d(CSn-CLK)}$ | Delay time, mcspi3_csi active to mcspi3_clk first edge | Modes 1 and 3 | A[(4)] – 4.4 | | A[(4)] – 10.1 | | ns |
| | | | Modes 0 and 2 | B[(5)] – 4.4 | | B[(5)] – 10.1 | | ns |
| SM6 | $t_{d(CLK-CSn)}$ | Delay time, mcspi3_clk last edge to mcspi3_csi inactive | Modes 1 and 3 | B[(5)] – 4.4 | | B[(5)] – 10.1 | | ns |
| | | | Modes 0 and 2 | A[(4)] – 4.4 | | A[(4)] – 10.1 | | ns |
| SM7 | $t_{d(csn-simo)}$ | Delay time, mcspi3_csi active edge to mcspi3_simo shifted | Modes 0 and 2 | | 11.3 | | 23.6 | ns |

(1) In mcspi3_csn, n is equal to 0 or 1. The polarity of mcspi3_clk and the active edge (rising or falling) on which mcspi3_simo is driven and mcspi3_somi is latched is all software configurable.
  – mcspi3_clk phase programmable with the bit PHA of MCSPI_CH(i)CONF register: PHA = 1 (Modes 1 and 3).
  – mcspi3_clk phase programmable with the bit PHA of MCSPI_CH(i)CONF register: PHA = 0 (Modes 0 and 2).
  For more information, see the McSPI environment chapter, Data Format Configurations section of the *AM/DM37x Multimedia Device Technical Reference Manual* (literature number SPRUGN4) for modes and phase correspondence description.

(2) This timing applies to all configurations regardless of McSPI3_CLK polarity and which clock edges are used to drive output data and capture input data.

(3) P = mcspi3_clk clock period

(4) Case P = 20.8 ns, A = (TCS + 0.5)*P[3] (TCS is a bit field of MSPI_CHCONFx[26:25] register).
  Case P > 20.8 ns, A = TCS*P[3] (TCS is a bit field of MSPI_CHCONFx[26:25] register). For more information, see the McSPI chapter of *AM/DM37x Multimedia Device Technical Reference Manual* (literature number SPRUGN4).

(5) B = TCS*P[3] (TCS is a bit field of MSPI_CHCONFx[26:25] register). For more information, see the McSPI chapter of *AM/DM37x Multimedia Device Technical Reference Manual* (literature number SPRUGN4).

(6) See Section 4.3.4, *Processor Clocks*.
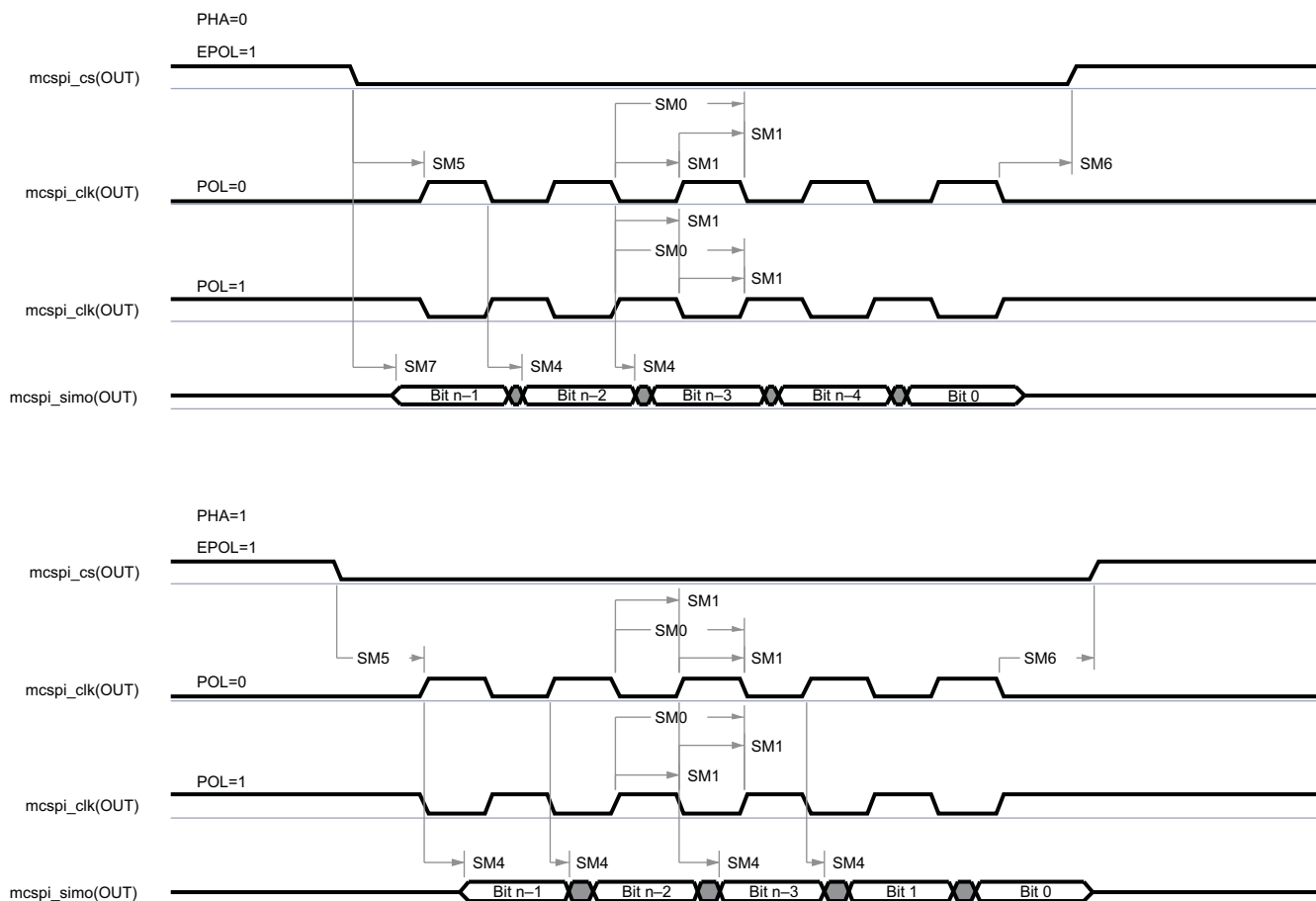


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(1) The active clock edge selection of mcspi_clk (rising or falling) on which mcspi_simo is driven and mcspi_somi data is latched is software configurable with the bit MCSPI_CH(i)CONF[1] = POL and the bit MCSPI_CH(i)CONF[0] = PHA.

(2) The polarity of mcspi_ncs is software configuable with the bit MCSPI_CH(i)CONF[6] = EPOL.

**Figure 6-46. McSPI—Master Mode—Transmit**
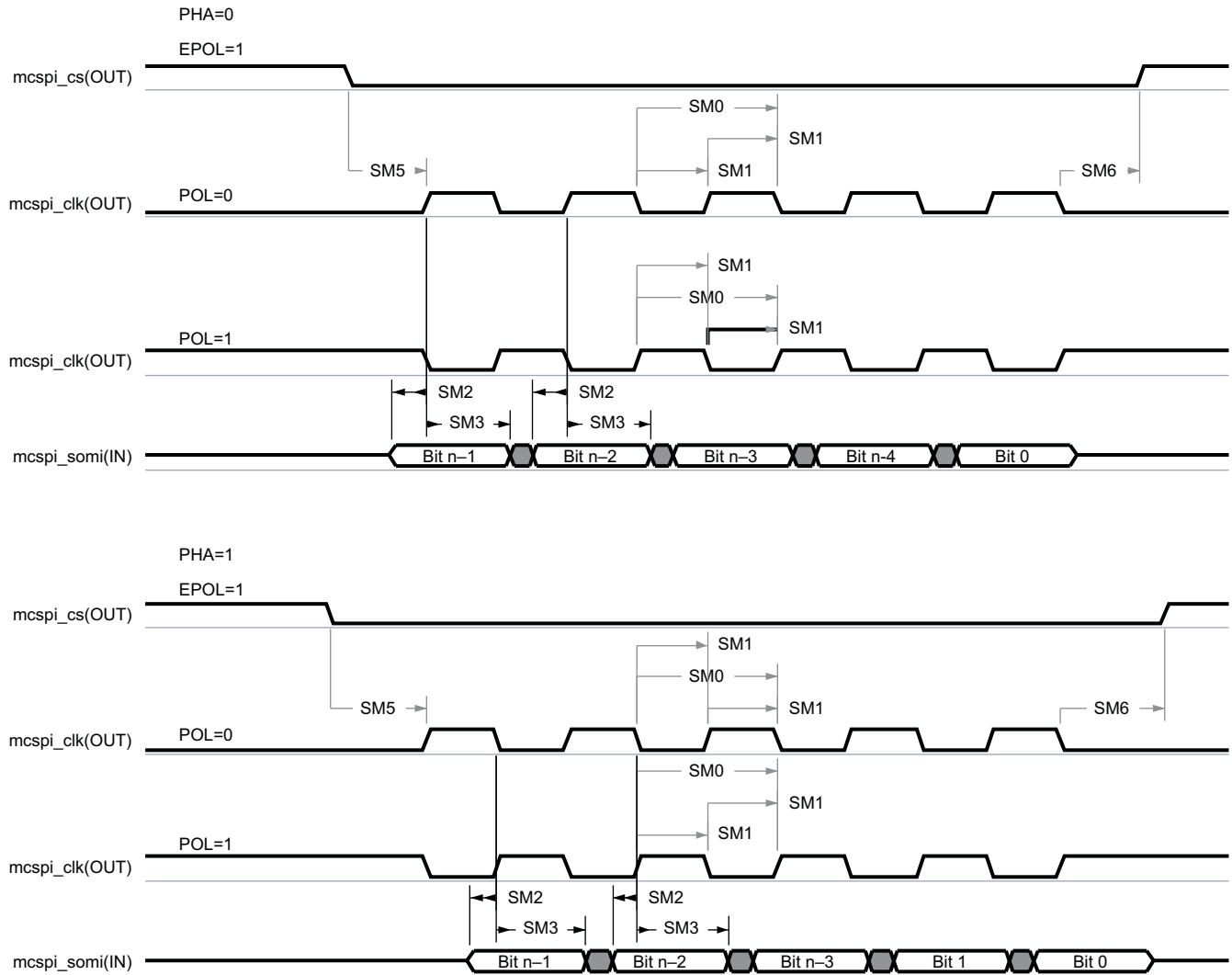
(1) The active clock edge selection of mcspi_clk (rising or falling) on which mcspi_simo is driven and mcspi_somi data is latched is software configurable with the bit MCSPI_CH(i)CONF[1] = POL and the bit MCSPI_CH(i)CONF[0] = PHA.

(2) The polarity of mcspi_ncs is software configuable with the bit MCSPI_CH(i)CONF[6] = EPOL.

**Figure 6-47. McSPI—Master Mode—Receive**

### 6.6.3 Multiport Full-Speed Universal Serial Bus (FS-USB)

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**NOTE**

For more information, see High-Speed USB Host Subsystem and High-Speed USB OTG Controller / High-Speed USB Host Subsystem section of the *AM/DM37x Multimedia Device Technical Reference Manual* (literature number SPRUGN4).

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The processor provides three USB ports working in full- and low-speed data transactions (up to 12Mbit/s). When connected to either a serial link controller or a serial PHY (PHY interface modes) it supports:

- 6-pin (Tx: Dat/Se0 or Tx: Dp/ ) unidirectional mode
- 4-pin bidirectional mode
- 3-pin bidirectional

### 6.6.3.1 FS-USB—Unidirectional Standard 6-pin Mode

Table 6-83 and Table 6-84 assume testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-48).

#### Table 6-82. LS- / FS-USB Timing Conditions—Unidirectional Standard 6-Pin Mode

| TIMING CONDITION PARAMETER | | VALUE | UNIT |
|---|---|---|---|
| **Input Conditions** | | | |
| $t_R$ | Input signal rise time | 2 | ns |
| $t_F$ | Input signal fall time | 2 | ns |
| **Output Condition** | | | |
| $C_{LOAD}$ | Output load capacitance[1] | 15 | pF |

(1) Buffer strength configuration: LB0 = 1.

#### Table 6-83.  LS- / FS-USB Timing Requirements—Unidirectional Standard 6-Pin Mode[1] [2]

| NO. | PARAMETER | | OPP100 | | OPP50 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| FSU1 | $t_{d(vp,vm)}$ | Time duration, mmx_rxdp and mmx_rx low together during transition | | 14 | | 14 | ns |
| FSU2 | $t_{d(vp,vm)}$ | Time duration, mmx_rxdp and mmx_rx high together during transition | | 8 | | 8 | ns |
| FSU3 | $t_{d(rcvU0)}$ | Time duration, mmx_rrxcv undefine during a single end 0 (mmx_rxdp and mmx_rx low together) | | 14 | | 14 | ns |
| FSU4 | $t_{d(rcvU1)}$ | Time duration, mmx_rxrcv undefine during a single end 1 (mmx_rxdp and mmx_rx high together) | | 8 | | 8 | ns |

(1) In mmx, x is equal to 0, 1, or 2.

(2) See Section 4.3.4, *Processor Clocks.*

#### Table 6-84. LS- / FS-USB Switching Characteristics—Unidirectional Standard 6-Pin Mode[1] [2]

| NO. | PARAMETER | | OPP100 | | OPP50 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| FSU5 | $t_{d(txenL-dV)}$ | Delay time, mmx_txen_n low to mmx_txdat valid | 81.8 | 84.8 | 81.8 | 84.8 | ns |
| FSU6 | $t_{d(txenL-se0V)}$ | Delay time, mmx_txen_n low to mmx_txse0 valid | 81.8 | 84.8 | 81.8 | 84.8 | ns |
| FSU7 | $t_{s(d-se0)}$ | Skew between mmx_txdat and mmx_txse0 transition | | 1.5 | | 1.5 | ns |
| FSU8 | $t_{d(dI-txenH)}$ | Delay time, mmx_txdat invalid to mmx_txen_n high | 81.8 | | 81.8 | | ns |
| FSU9 | $t_{d(se0I-txenH)}$ | Delay time, mmx_txse0 invalid to mmx_txen_n high | 81.8 | | 81.8 | | ns |

(1) In mmx, x is equal to 0, 1, or 2.

(2) See Section 4.3.4, *Processor Clocks.*

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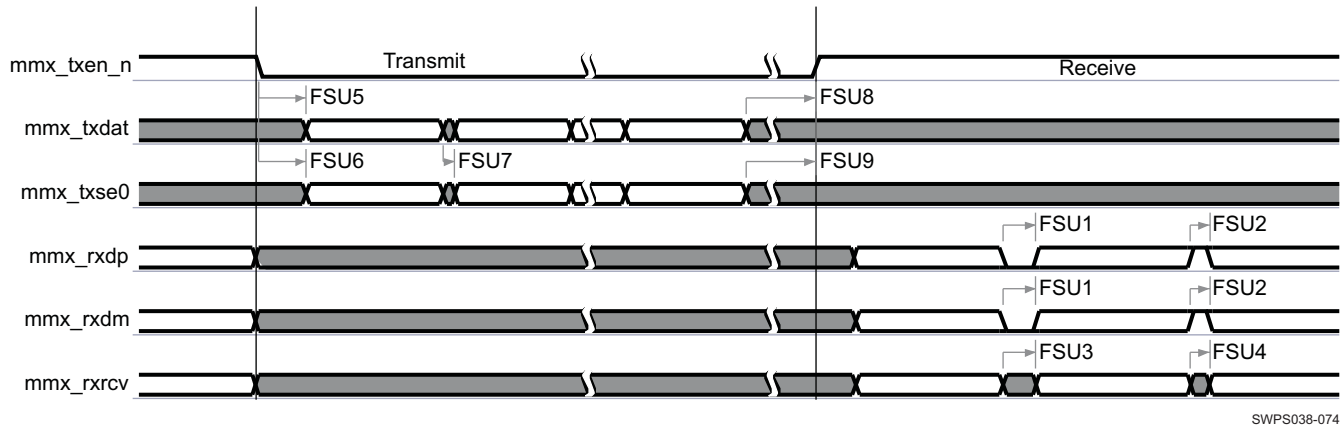
(1) In mmx, x is equal to 0, 1, or 2.

**Figure 6-48. LS- / FS-USB—Unidirectional Standard 6-Pin Mode**

### 6.6.3.2 FS-USB—Bidirectional Standard 4-pin Mode

Table 6-86 and Table 6-87 assume testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-49).

**Table 6-85. LS- / FS-USB Timing Conditions—Bidirectional Standard 4-Pin Mode**

| TIMING CONDITION PARAMETER | | VALUE | UNIT |
|---|---|---|---|
| **Input Conditions** | | | |
| $t_R$ | Input signal rise time | 2 | ns |
| $t_F$ | Input signal fall time | 2 | ns |
| **Output Condition** | | | |
| $C_{LOAD}$ | Output load capacitance[1] | 15 | pF |

(1) Buffer strength configuration: LB0 = 1.

**Table 6-86. LS- / FS-USB Timing Requirements—Bidirectional Standard 4-Pin Mode[1] [2]**

| NO. | PARAMETER | | OPP100 | | OPP50 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| FSU10 | $t_{d(d,se0)}$ | Time duration, mmx_txdat and mmx_txse0 low together during transition | | 14 | | 14 | ns |
| FSU11 | $t_{d(d,se0)}$ | Time duration, mmx_txdat and mmx_txse0 high together during transition | | 8 | | 8 | ns |
| FSU12 | $t_{d(rcvU0)}$ | Time duration, mmx_rrxcv undefine during a single end 0 (mmx_txdat and mmx_txse0 low together) | | 14 | | 14 | ns |
| FSU13 | $t_{d(rcvU1)}$ | Time duration, mmx_rxrcv undefine during a single end 1 (mmx_txdat and mmx_txse0 high together) | | 8 | | 8 | ns |

(1) In mmx, x is equal to 0, 1, or 2.

(2) See Section 4.3.4, *Processor Clocks*.

**Table 6-87. LS- / FS-USB Switching Characteristics—Bidirectional Standard 4-Pin Mode[1] [2]**

| NO. | PARAMETER | | OPP100 | | OPP50 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| FSU14 | $t_{d(txenL-dV)}$ | Delay time, mmx_txen_n low to mmx_txdat valid | 81.8 | 84.8 | 81.8 | 84.8 | ns |
| FSU15 | $t_{d(txenL-se0V)}$ | Delay time, mmx_txen_n low to mmx_txse0 valid | 81.8 | 84.8 | 81.8 | 84.8 | ns |
| FSU16 | $t_{s(d-se0)}$ | Skew between mmx_txdat and mmx_txse0 transition | | 1.5 | | 1.5 | ns |
| FSU17 | $t_{d(dV-txenH)}$ | Delay time, mmx_txdat invalid before mmx_txen_n high | 81.8 | | 81.8 | | ns |

**Table 6-87. LS- / FS-USB Switching Characteristics—Bidirectional Standard 4-Pin Mode[1] [2] (continued)**

| NO. | PARAMETER | | OPP100 | | OPP50 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| FSU18 | $t_{d(se0V-txenH)}$ | Delay time, mmx_txse0 invalid before mmx_txen_n high | 81.8 | | 81.8 | | ns |

(1) In mmx, x is equal to 0, 1, or 2.

(2) See Section 4.3.4, *Processor Clocks*.
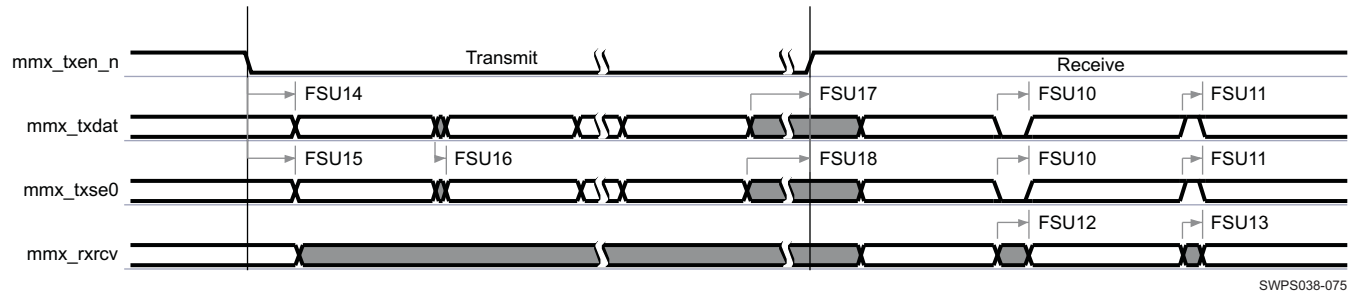


(1) In mmx, x is equal to 0, 1, or 2.

**Figure 6-49. LS- / FS-USB—Bidirectional Standard 4-Pin Mode**

### 6.6.3.3 FS-USB—Bidirectional Standard 3-pin Mode

Table 6-89 and Table 6-90 assume testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-50).

**Table 6-88. LS- / FS-USB Timing Conditions—Bidirectional Standard 3-Pin Mode**

| TIMING CONDITION PARAMETER | | VALUE | UNIT |
|---|---|---|---|
| **Input Conditions** | | | |
| $t_R$ | Input signal rise time | 2 | ns |
| $t_F$ | Input signal fall time | 2 | ns |
| **Output Condition** | | | |
| $C_{LOAD}$ | Output load capacitance[1] | 15 | pF |

(1) Buffer strength configuration: LB0 = 1.

**Table 6-89. LS- / FS-USB Timing Requirements—Bidirectional Standard 3-Pin Mode[1] [2]**

| NO. | PARAMETER | | OPP100 | | OPP50 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| FSU19 | $t_{d(d,se0)}$ | Time duration, mmx_txdat and mmx_txse0 low together during transition | | 14 | | 14 | ns |
| FSU20 | $t_{d(d,se0)}$ | Time duration, mmx_tsdat and mmx_txse0 high together during transition | | 8 | | 8 | ns |

(1) In mmx, x is equal to 0, 1, or 2.

(2) See Section 4.3.4, *Processor Clocks*.

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**Table 6-90. LS- / FS-USB Switching Characteristics—Bidirectional Standard 3-Pin Mode[1] [2]**

| NO. | PARAMETER | | OPP100 | | OPP50 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| FSU21 | $t_{d(txenL-dV)}$ | Delay time, mmx_txen_n low to mmx_txdat valid | 81.8 | 84.8 | 81.8 | 84.8 | ns |
| FSU22 | $t_{d(txenL-se0V)}$ | Delay time, mmx_txen_n low to mmx_txse0 valid | 81.8 | 84.8 | 81.8 | 84.8 | ns |
| FSU23 | $t_{s(d-se0)}$ | Skew between mmx_txdat and mmx_txse0 transition | | 1.5 | | 1.5 | ns |
| FSU24 | $t_{d(dI-txenH)}$ | Delay time, mmx_txdat invalid to mmx_txen_n high | 81.8 | | 81.8 | | ns |
| FSU25 | $t_{d(se0I-txenH)}$ | Delay time, mmx_txse0 invalid to mmx_txen_n high | 81.8 | | 81.8 | | ns |

(1)  In mmx, x is equal to 0, 1, or 2.

(2)  See Section 4.3.4, *Processor Clocks.*
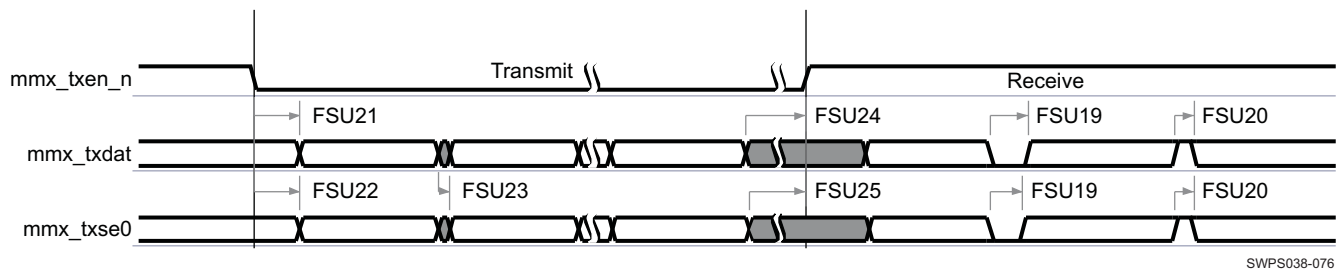


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**Figure 6-50. LS- / FS-USB—Bidirectional Standard 3-Pin Mode[1]**

(1)  In mmx, x is equal to 0, 1, or 2.

## 6.6.4 Multiport High-Speed Universal Serial Bus (HS-USB)

> **NOTE**
>
> For more information, see High-Speed USB Host Subsystem and High-Speed USB OTG Controller / High-Speed USB OTG Controller and High-Speed USB Host Subsystem and High-Speed USB OTG Controller / High-Speed USB Host Subsystem sections of the *AM/DM37x Multimedia Device Technical Reference Manual* (literature number SPRUGN4).

In addition to the full-speed (FS) USB controller, a high-speed (HS) USB OTG controller is incorporated in the device. It allows high-speed transactions (up to 480 Mbit/s) on the USB ports 0, 1, 2, and 3 described below:

- Port 0:
  - 12-bit slave mode (SDR)
- Ports 1 and 2:
  - 12-bit master mode (SDR)
- Port 3:

### 6.6.4.1 HSUSB0—Port 0—12-bit Slave Mode

Table 6-92 and Table 6-93 assume testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-51).

**Table 6-91. HSUSB0 Timing Conditions—12-bit Slave Mode**

| TIMING CONDITION PARAMETER | | VALUE | UNIT |
|---|---|---|---|
| **Input Conditions** | | | |
| $t_R$ | Input signal rise time | 2 | ns |
| $t_F$ | Input signal fall time | 2 | ns |
| **Output Condition** | | | |
| $C_{LOAD}$ | Output load capacitance[1] | 3.5 | pF |

(1) Buffer strength configuration: LB0 = 0.

**Table 6-92. HSUSB0 Timing Requirements—12-bit Slave Mode[3] [4]**

| NO. | PARAMETER | | OPP100 | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| HSU0 | $f_{p(CLK)}$ | hsusb0_clk clock frequency[1] | | 60.03 | MHz |
| | $t_{J(CLK)}$ | Cycle jitter[2], hsusb0_clk | | 500 | ps |
| HSU3 | $t_{s(DIRV-CLKH)}$ | Setup time, hsusb0_dir valid before hsusb0_clk rising edge | 6.68 | | ns |
| | $t_{s(NXTV-CLKH)}$ | Setup time, hsusb0_nxt valid before hsusb0_clk rising edge | 6.68 | | ns |
| HSU4 | $t_{h(CLKH-DIRIV)}$ | Hold time, hsusb0_dir valid after hsusb0_clk rising edge | 0 | | ns |
| | $t_{h(CLKH-NXT/IV)}$ | Hold time, hsusb0_nxt valid after hsusb0_clk rising edge | 0 | | ns |
| HSU5 | $t_{s(DATAV-CLKH)}$ | Setup time, hsusb0_data[0:7] valid before hsusb0_clk rising edge | 6.68 | | ns |
| HSU6 | $t_{h(CLKH-DATIV)}$ | Hold time, hsusb0_data[0:7] valid after hsusb0_clk rising edge | 0 | | ns |

(1) Related with the input maximum frequency supported by the USB module.

(2) Maximum cycle jitter supported by hsusb0_clk input clock

(3) The timing requirements are assured up to the cycle jitter error condition specified.

(4) See Section 4.3.4, *Processor Clocks.*

**Table 6-93. HSUSB0 Switching Characteristics—12-bit Slave Mode[1]**

| NO. | PARAMETER | | OPP100 | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| HSU1 | $t_{d(clkL-STPV)}$ | Delay time, hsusb0_clk high to output usb0_stp valid | | 8.6 | ns |
| | $t_{d(clkL-STPIV)}$ | Delay time, hsusb0_clk high to output usb0_stp invalid | 0 | | ns |
| HSU2 | $t_{d(clkL-DV)}$ | Delay time, hsusb0_clk high to output hsusb0_data[0:7] valid | | 8.6 | ns |
| | $t_{d(clkL-DIV)}$ | Delay time, hsusb0_clk high to output hsusb0_data[0:7] invalid | 0 | | ns |

(1) See Section 4.3.4, *Processor Clocks.*
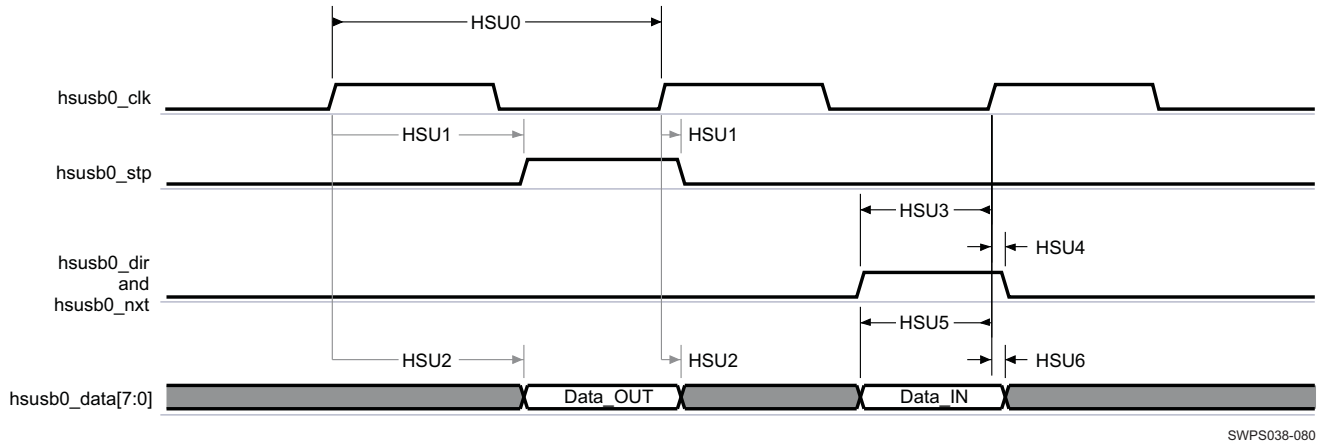


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**Figure 6-51. HSUSB0—12-bit Slave Mode**

### 6.6.4.2 HSUSB1 and HSUSB2—Ports 1 and 2—12-bit Slave Mode

Table 6-95 and Table 6-96 assume testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-52).

**Table 6-94. HSUSB1 and HSUSB2 Timing Conditions—12-bit Master Mode**

| TIMING CONDITION PARAMETER | | VALUE | UNIT |
|---|---|---|---|
| **Input Conditions** | | | |
| $t_R$ | Input signal rise time | 3 | ns |
| $t_F$ | Input signal fall time | 2 | ns |
| **Output Condition** | | | |
| $C_{LOAD}$ | Output load capacitance[1] | 5 | pF |

(1) Buffer strength configuration: LB0 = 0.

**Table 6-95. HSUSB1 and HSUSB2 Timing Requirements—12-bit Master Mode[1] [2]**

| NO. | PARAMETER | | OPP100 | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| HSU3 | $t_{su(dirV-clkH)}$ | Setup time, input direction control hsusbx_dir valid before output clock hsusbx_clk rising edge | 9.3 | | ns |
| | $t_{su(nxtV-clkH)}$ | Setup time, input next signal hsusbx_nxt valid before output clock hsusbx_clk rising edge | 9.3 | | ns |
| HSU4 | $t_{h(clkH-dirIV)}$ | Hold time, input direction control hsusbx_dir valid after output clock hsusbx_clk rising edge | −0.52 | | ns |
| | $t_{h(clkH-nxtIV)}$ | Hold time, input next signal hsusbx_nxt valid after output clock hsusbx_clk rising edge | −0.52 | | ns |
| HSU5 | $t_{su(dV-clkH)}$ | Setup time, input data hsusbx_data[7:0] valid before output clock hsusbx_clk rising edge | 9.3 | | ns |

### Table 6-95. HSUSB1 and HSUSB2 Timing Requirements—12-bit Master Mode[1] [2] (continued)

| NO. | PARAMETER | | OPP100 | | UNIT |
|-----|-----------|---|------|------|------|
| | | | MIN | MAX | |
| HSU6 | $t_{h(clkH-dV)}$ | Hold time, input data hsusbx_data[7:0] valid after output clock hsusbx_clk rising edge | −0.52 | | ns |

(1) In hsusbx, x is equal to 1 or 2.

(2) See Section 4.3.4, *Processor Clocks.*

### Table 6-96. HSUSB1 and HSUSB2 Switching Characteristics—12-bit Master Mode[1] [3]

| NO. | PARAMETER | | OPP100 | | UNIT |
|-----|-----------|---|------|------|------|
| | | | MIN | MAX | |
| HSU0 | $t_{p(clk)}$ | Frequency, output clock hsusbx_clk | | 60 | MHz |
| | $t_{J(clk)}$ | Jitter standard deviation[2], output clock hsusbx_clk | | 400 | ps |
| HSU1 | $t_{d(clkH-stpV)}$ | Delay time, output clock hsusbx_clk rising edge to output stop signal hsusbx_stp valid | | 12.81 | ns |
| | $t_{d(clkH-stpIV)}$ | Delay time, output clock hsusbx_clk rising edge to output stop signal hsusbx_stp invalid | 1.95 | | ns |
| HSU2 | $t_{d(clkH-dV)}$ | Delay time, output clock hsusbx_clk rising edge to output data hsusbx_data[7:0] valid | | 12.81 | ns |
| | $t_{d(clkH-dIV)}$ | Delay time, output clock hsusbx_clk rising edge to output data hsusbx_data[7:0] invalid | 1.95 | | ns |
| | $t_{R(d)}$ | Rise time, output data hsusbx_data[7:0] | | 0 | ns |
| | $t_{F(d)}$ | Fall time, output data hsusbx_data[7:0] | | 0 | ns |

(1) In hsusbx, x is equal to 1 or 2.

(2) The jitter probability density can be approximated by a Gaussian function.

(3) See Section 4.3.4, *Processor Clocks.*
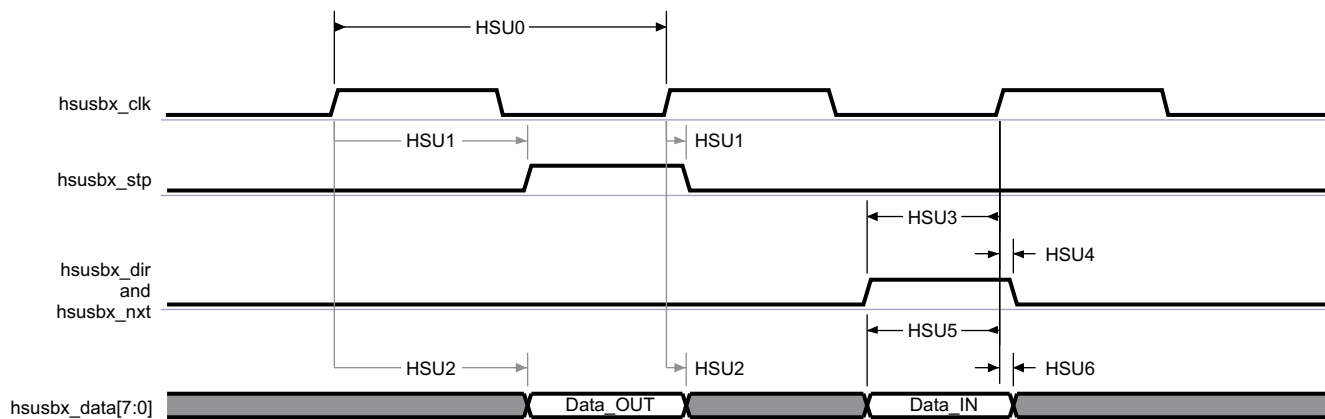


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(1) In hsusbx, x is equal to 1 or 2.

**Figure 6-52. HSUSB1 and HSUSB2—12-bit Master Mode**

## 6.6.5 Inter-Integrated Circuit Interface (I²C)

### NOTE

For more information, see Multimaster High-Speed I2C Controller chapter of the *AM/DM37x Multimedia Device Technical Reference Manual* (literature number SPRUGN4).

The multi-master I²C peripheral provides an interface between two or more devices via an I²C serial bus.

The I$^2$C controller supports the multi-master mode which allows more than one device capable of controlling the bus to be connected to it. Each I$^2$C device is recognized by a unique address and can operates as either transmitter or receiver, according to the function of the device. In addition to being a transmitter or receiver, a device connected to the I$^2$C bus can also be considered as master or slave when performing data transfers. This data transfer is carried out via two serial bidirectional wires:

• An SDA data line
• An SCL clock line

In Figure 6-53 the data transfer is in master or slave configuration with 7-bit addressing format.

The I$^2$C interface is compliant with Philips I$^2$C specification version 2.1. It supports standard mode (up to 100K bits/s), fast mode (up to 400K bits/s) and high-speed mode (up to 3.4Mb/s).

### 6.6.5.1 I$^2$C—Standard and Fast Modes

**Table 6-97. I$^2$C—Standard and Fast Modes**

| NO. | | PARAMETER | STANDARD MODE | | FAST MODE | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| | $f_{scl}$ | Frequency, clock i2cx_scl[4] | | 100 | | 400 | kHz |
| I1 | $t_{w(sclH)}$ | Pulse duration, clock i2cx_scl[4] high | 4.0 | | 0.6 | | µs |
| I2 | $t_{w(sclL)}$ | Pulse duration, clock i2cx_scl[4] low | 4.7 | | 1.3 | | µs |
| I3 | $t_{su(sdaV-sclH)}$ | Setup time, data i2cx_sda[4] valid before clock i2cx_scl[4] active level | 250 | | 100[1] | | ns |
| I4 | $t_{h(sclH-sdaV)}$ | Hold time, data i2cx_sda[4] valid after clock i2cx_scl[4] active level | 0[2] | 3.45[3] | 0[2] | 0.9[3] | µs |
| I5 | $t_{su(sdaL-sclH)}$ | Setup time, clock i2cx_scl[4] high after data i2cx_sda[4] low (for a START[5] condition or a repeated START condition) | 4.7 | | 0.6 | | µs |
| I6 | $t_{h(sclH-sdaH)}$ | Hold time, data i2cx_sda low level after clock i2cx_scl[4] high level (STOP condition) | 4.0 | | 0.6 | | µs |
| I7 | $t_{h(sclH-RSTART)}$ | Hold time, data i2cx_sda[4] low level after clock i2cx_scl[4] high level (for a repeated START condition) | 4.0 | | 0.6 | | µs |
| I8 | $t_{w(sdaH)}$ | Pulse duration, data i2cx_sda[4] high between STOP and START conditions | 4.7[4] | | 1.3 | | µs |
| | $t_{R(scl)}$ | Rise time, clock i2cx_scl[4] | | 1000 | 20 + 0.1$C_B$ | 300 | ns |
| | $t_{F(scl)}$ | Fall time, clock i2cx_scl[4] | | 300 | 20 + 0.1$C_B$ | 300 | ns |
| | $t_{R(sda)}$ | Rise time, data i2cx_sda[4] | | 1000 | 20 + 0.1$C_B$ | 300 | ns |
| | $t_{F(sda)}$ | Fall time, data i2cx_sda[4] | | 300 | 20 + 0.1$C_B$ | 300 | ns |
| | $C_B$ | Capacitive load for each bus line | | 400 | | 400 | pF |

(1) A fast-mode I$^2$C-bus device can be used in a standard-mode I$^2$C-bus system, but the requirement $t_{su(SDAV-SCLH)}$ ≥ 250 ns must then be met. This is automatically the case if the device does not stretch the low period of the i2cx_scl[4]. If such a device does stretch the low period of the i2cx_scl[4], it must output the next data bit to the i2cx_sda[4] line $t_{r(SDA)}$ max + $t_{su(SDAV-SCLH)}$ = 1000 + 250 = 1250 ns (according to the standard-mode I$^2$C-bus specification) before the i2cx_scl[4] line is released.

(2) The device provides (via the I$^2$C bus) a minimum hold time (= I2C_FCLK period x (PSC+1) x 4) for the i2cx_sda[4] signal (see the fall and rise times of i2cx_scl[4]) to bridge the undefined region of the falling edge of i2cx_scl[4].

(3) The maximum $t_{h(SCLH-SDA)}$ has only to be met if the device does not stretch the low period of the i2cx_scl[4] signal.

(4) In i2cx, x is equal to 1, 2, 3, or 4. Note that I2C4 is master transmitter only.

(5) After this time, the first clock is generated.

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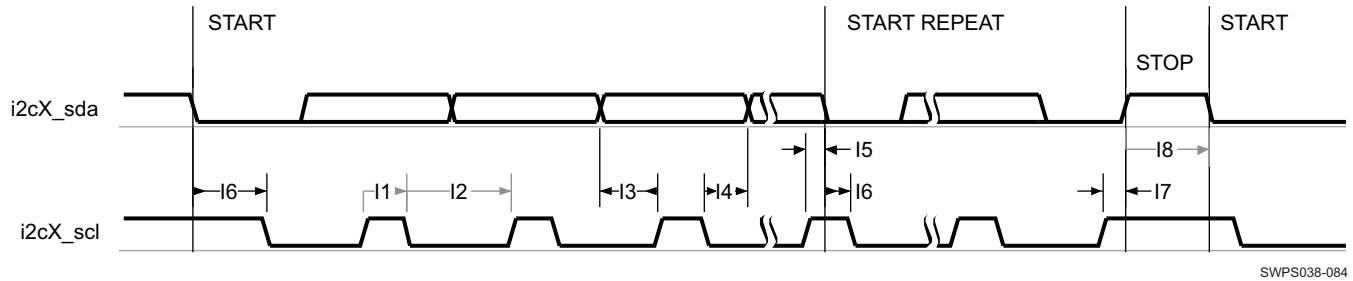
(1)   In i2cX, X is equal to 1, 2, 3, or 4.

**Figure 6-53. I²C—Standard and Fast Modes**

### 6.6.5.2   I²C—High-Speed Mode

**Table 6-98. I²C—High-Speed Mode**

| NO. | | PARAMETER | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| | $f_{scl}$ | Frequency, clock i2cx_scl[3] | | 3.4[5] | MHz |
| I1 | $t_{w(sclH)}$ | Pulse duration, clock i2cx_scl[3] high | 60[1] | | ns |
| I2 | $t_{w(sclL)}$ | Pulse duration, clock i2cx_scl[3] low | 160[1] | | ns |
| I3 | $t_{su(sdaV-sclH)}$ | Setup time, data i2cx_sda[3] valid before clock i2cx_scl[3] active level | 10 | | ns |
| I4 | $t_{h(sclH-sdaV)}$ | Hold time, data i2cx_sda[3] valid after clock i2cx_scl[3] active level | 0[4] | 70 | ns |
| I5 | $t_{su(sdaL-sclH)}$ | Setup time, clock i2cx_scl[3] high after data i2cx_sda[3] low (for a START[2] condition or a repeated START condition) | 160 | | ns |
| I6 | $t_{h(sclH-sdaH)}$ | Hold time, data i2cx_sda[3] low level after clock i2cx_scl[3] high level (STOP condition) | 160 | | ns |
| I7 | $t_{h(sclH-RSTART)}$ | Hold time, data i2cx_sda[3] low level after clock i2cx_scl[3] high level (for a repeated START condition) | 160 | | ns |
| | $t_{R(scl)}$ | Rise time, clock i2cx_scl[3] | 10 | 40 | ns |
| | $t_{R(scl)}$ | Rise time, clock i2cx_scl[3] after a repeated START condition and after a bit acknowledge | 10 | 80 | ns |
| | $t_{F(scl)}$ | Fall time, clock i2cx_scl[3] | 10 | 40 | ns |
| | $t_{R(sda)}$ | Rise time, data i2cx_sda[3] | 10 | 80 | ns |
| | $t_{F(sda)}$ | Fall time, data i2cx_sda[3] | 10 | 80 | ns |
| | $C_B$ | Capacitive load for each bus line | | 100 | pF |

(1)   HS-mode master devices generate a serial clock signal with a high to low ratio of 1 to 2. $t_{w(sclL)} > 2 * t_{w(sclH)}$.

(2)   After this time, the first clock is generated.

(3)   In i2cx, x is equal to 1, 2, 3, or 4. Note that I2C4 is master transmitter only.

(4)   The device provides (via the I²C bus) a minimum hold time (= I2C_FCLK period x 4) for the i2cx_sda[3] signal (see the fall and rise times of i2cx_scl[3]) to bridge the undefined region of the falling edge of i2cx_scl[3].

(5)   The I2C4 clock frequency in high-speed mode is equal to the sys_xtalin input clock frequency divided by 15.



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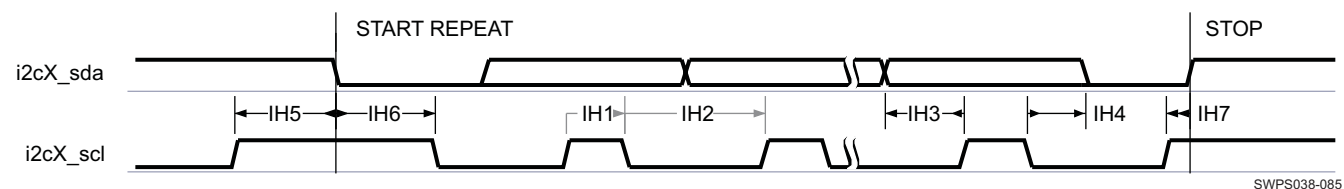
(1)   In i2cX, X is equal to 1, 2, 3, or 4.

**Figure 6-54. I²C—High-Speed Mode**

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### Table 6-99. I²C Correspondence Standard vs Data Manual Timing References

| TI | | STANDARD-I²C | |
|---|---|---|---|
| | | **Standard/Fast Modes** | **High-Speed Mode** |
| | $f_{scl}$ | $F_{SCL}$ | $F_{SCLH}$ |
| I1 | $t_{w(sclH)}$ | $T_{HIGH}$ | $T_{HIGH}$ |
| I2 | $t_{w(sclL)}$ | $T_{LOW}$ | $T_{LOW}$ |
| I3 | $t_{su(sdaV-sclH)}$ | $T_{SU;DAT}$ | $T_{SU;DAT}$ |
| I4 | $t_{h(sclH-sdaV)}$ | $T_{SU;DAT}$ | $T_{SU;DAT}$ |
| I5 | $t_{su(sdaL-sclH)}$ | $T_{SU;STA}$ | $T_{SU;STA}$ |
| I6 | $t_{h(sclH-sdaH)}$ | $T_{HD;STA}$ | $T_{HD;STA}$ |
| I7 | $t_{h(sclH-RSTART)}$ | $T_{SU;STO}$ | $T_{SU;STO}$ |
| I8 | $t_{w(sdaH)}$ | $T_{BUF}$ | |

## 6.6.6 HDQ / 1-Wire Interface (HDQ/1-Wire)

**NOTE**

For more information, see HDQ/1-Wire / HDQ/1-Wire chapter of the *AM/DM37x Multimedia Device Technical Reference Manual* (literature number SPRUGN4).

The module is intended to work with both HDQ and 1-Wire protocols. The protocols use a single wire to communicate between the master and the slave. The protocols employ an asynchronous return to one mechanism where, after any command, the line is pulled high.

### 6.6.6.1 HDQ/1-Wire—HDQ Mode

Table 6-100 and Table 6-102 assume testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-55 through Figure 6-59).

### Table 6-100. HDQ Interface Read Timing

| PARAMETER | DESCRIPTION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $t_{CYCH}$ | Read bit window timing | 190 | | 250 | µs |
| $t_{HW1}$ | Read one data valid after HDQ low | 32[2] | | 66[2] | µs |
| $t_{HW0}$ | Read zero data hold after HDQ low | 70[2] | | 145[2] | µs |
| $t_{RSPS}$ | Response time from HDQ slave device[1] | 190 | | 320 | µs |

(1) Defined by software

(2) If the HDQ slave device drives a logic-low state after $t_{HW0}$ max, it can be interpreted as a break pulse. For more information see Table 6-101 and the HDQ/1-Wire chapter of the *AM/DM37x Multimedia Device Technical Reference Manual* (literature number SPRUGN4).

### Table 6-101. HDQ Sampling Cases[1]

| CASES | FIRST SAMPLING (at 68 µs) | SECOND SAMPLING (at 180 µs) |
|---|---|---|
| 1 | L (logic-low state) | L (logic-low state) |
| 2 | L (logic-low state) | H (logic-high state) |
| 3 | H (logic-high state) | L (logic-low state) |
| 4 | H (logic-high state) | H (logic-high state) |

(1) The different cases can be interpreted as follows:
- Case 1: If a logic-low state is present at the first sampling time and also at the second sampling time, the receive data can be interpreted as a break pulse.
- Case 2: If a logic-low state is present at the first sampling time and a logic-high state is present at the second sampling time, the receive data on the line is a zero (data).
- Case 3: Undefined.
- Case 4: If a logic-high state is present at the first sampling time and also at the second sampling time, the receive data on the line is a one (data).

**Table 6-102. HDQ Write Switching Characteristics**

| PARAMETER | DESCRIPTION | MIN | TYP | MAX | UNIT |
|-----------|-------------|-----|-----|-----|------|
| $t_B$ | Break timing | 190 | | | µs |
| $t_{BR}$ | Break recovery time | 40 | | | µs |
| $t_{CYCD}$ | Write bit windows timing | 190 | | | µs |
| $t_{DW1}$ | Write one data valid after HDQ low | 0.5 | | 50 | µs |
| $t_{DW0}$ | Write zero data hold after HDQ low | 86 | | 145 | µs |
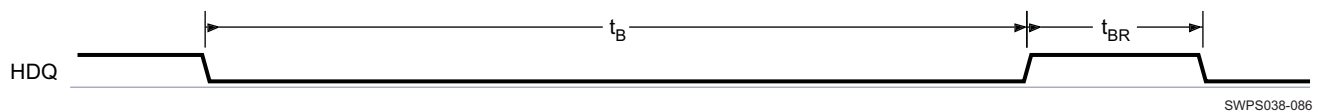
**Figure 6-55. HDQ Break and Break Recovery Timing— HDQ Interface Writing to Slave**
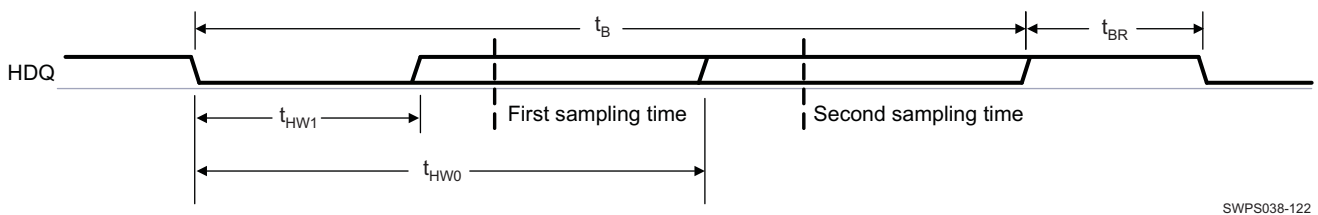
**Figure 6-56. HDQ Break Detection— HDQ Interface Reading Slave**
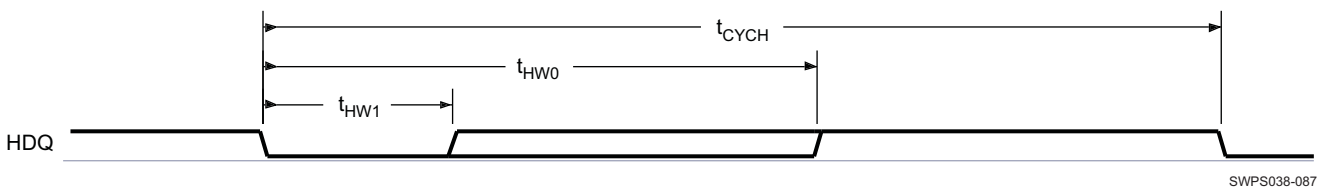
**Figure 6-57. HDQ Interface Bit Read Timing (Data)**
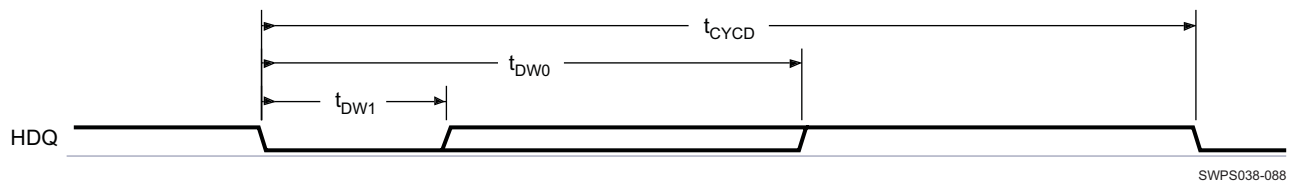
**Figure 6-58. HDQ Interface Bit Write Timing (Command/Address or Data)**
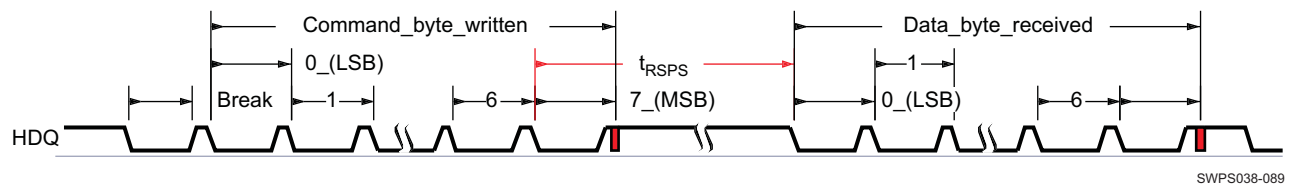
**Figure 6-59. HDQ—Communication**

### 6.6.6.2  HDQ/1-Wire—1-Wire Mode

Table 6-103 and Table 6-104 assume testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-60 through Figure 6-63).

**Table 6-103. HDQ/1-Wire Timing Requirements—1-Wire Mode**

| PARAMETER | DESCRIPTION | MIN | TYP | MAX | UNIT |
|-----------|-------------|-----|-----|-----|------|
| $t_{PDH}$ | Presence pulse delay high | 15 | | 60 | µs |
| $t_{PDL}$ | Presence pulse delay low | 60 | | 240 | µs |
| $t_{RDV}$ | Read data valid time | $t_{LOWR}$ | | 15 | µs |
| $t_{REL}$ | Read data release time | 0 | | 45 | µs |

**Table 6-104. HDQ/1-Wire Switching Characteristics—1-Wire Mode**

| PARAMETER | DESCRIPTION | MIN | TYP | MAX | UNIT |
|-----------|-------------|-----|-----|-----|------|
| $t_{RSTL}$ | Reset time low | 480 | | 960 | µs |
| $t_{RSTH}$ | Reset time high | 480 | | | µs |
| $t_{SLOT}$ | Bit cycle time | 60 | | 120 | µs |
| $t_{LOW1}$ | Write bit-one time | 1 | | 15 | µs |
| $t_{LOW0}$ | Write bit-zero time[2] | 60 | | 120 | µs |
| $t_{REC}$ | Recovery time | 1 | | | µs |
| $t_{LOWR}$ | Read bit strobe time[1] | 1 | | 15 | µs |

(1)  $t_{LOWR}$ (low pulse sent by the master) must be short as possible to maximize the master sampling window.

(2)  $t_{LOW0}$ must be less than $t_{SLOT}$.



SWPS038-090
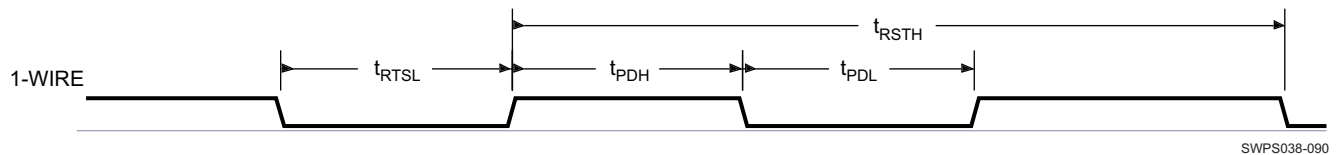
**Figure 6-60. 1-Wire Reset Timing**



SWPS038-091
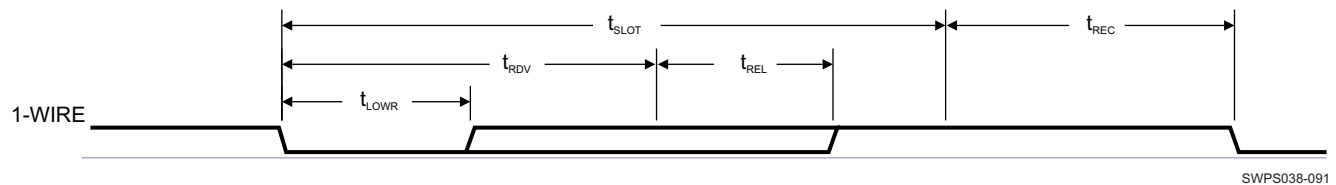
**Figure 6-61. 1-Wire Read Bit Timing (Data)**



SWPS038-123
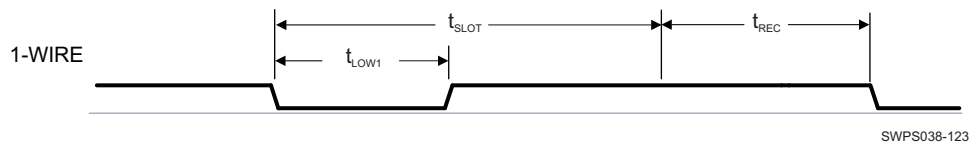
**Figure 6-62. 1-Wire Write Bit-One Timing (Command / Address or Data)**



SWPS038-124
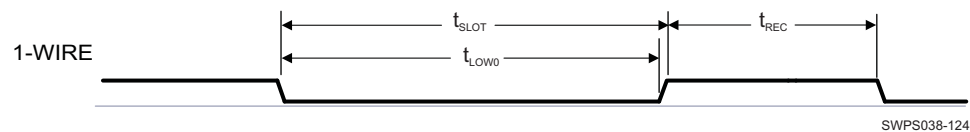
**Figure 6-63. 1-Wire Write Bit-Zero Timing (Command/Address or Data)**

### 6.6.7 Universal Asynchronous Receiver Transmitter (UART)

**NOTE**

For more information, see UART/IrDA/CIR chapter of the *AM/DM37x Multimedia Device Technical Reference Manual* (literature number SPRUGN4).

#### 6.6.7.1 UART

**Table 6-105. UART Switching Characteristics[2]**

| SIGNAL NAME | MUX MODE | DESCRIPTION | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| **Universal Asynchronous Receiver/Transmitter (UART1)** | | | | | | |
| UART1 (uart1_tx): AA8 | 0 | $t_R$, Rise time | | 1.5 | 5.5 | ns |
| | | $t_F$, Fall time | | | | |
| | | $C_L$, Output load | | 2 | 22 | pF |
| UART1 (uart1_rts): AA9 | 0 | $t_R$, Rise time | | 1.5 | 5.5 | ns |
| | | $t_F$, Fall time | | | | |
| | | $C_L$, Output load | | 2 | 22 | pF |
| UART1 (uart1_tx): E26 | 2 | $t_R$, Rise time | | 0.6 | 2.4 | ns |
| | | $t_F$, Fall time | | | | |
| | | $C_L$, Output load | | 2 | 22 | pF |
| UART1 (uart1_rts): AH22 | 2 | $t_R$, Rise time | SC0, SC1 = 00[1] | 1 | 15 | ns |
| | | $t_F$, Fall time | | | | |
| | | $C_L$, Output load | | 4 | 60 | pF |
| | | $t_R$, Rise time | SC0, SC1 = 00[1] | 0.4 | 5 | ns |
| | | $t_F$, Fall time | | | | |
| | | $C_L$, Output load | | 2 | 21 | pF |
| | | $t_R$, Rise time | SC0, SC1 = 00[1] | 0.6 | 7 | ns |
| | | $t_F$, Fall time | | | | |
| | | $C_L$, Output load | | 7 | 33 | pF |
| **Universal Asynchronous Receiver/Transmitter (UART2)** | | | | | | |
| UART2 (uart2_tx): AA25 | 0 | $t_R$, Rise time | | 1.5 | 5.5 | ns |
| | | $t_F$, Fall time | | | | |
| | | $C_L$, Output load | | 2 | 22 | pF |
| UART2 (uart2_rts): AB25 | 0 | $t_R$, Rise time | | 1.5 | 5.5 | ns |
| | | $t_F$, Fall time | | | | |
| | | $C_L$, Output load | | 2 | 22 | pF |
| UART2 (uart2_tx): AF5 | 1 | $t_R$, Rise time | | 1.5 | 5.5 | ns |
| | | $t_F$, Fall time | | | | |
| | | $C_L$, Output load | | 2 | 22 | pF |
| UART2 (uart2_rts): AE6 | 1 | $t_R$, Rise time | | 1.5 | 5.5 | ns |
| | | $t_F$, Fall time | | | | |
| | | $C_L$, Output load | | 2 | 22 | pF |
| UART2 (uart2_tx): T27 | 5 | $t_R$, Rise time | | 1.5 | 5.5 | ns |
| | | $t_F$, Fall time | | | | |
| | | $C_L$, Output load | | 2 | 22 | pF |
| UART2 (uart2_rts): U27 | 5 | $t_R$, Rise time | | 1.5 | 5.5 | ns |
| | | $t_F$, Fall time | | | | |
| | | $C_L$, Output load | | 2 | 22 | pF |
| **Universal Asynchronous Receiver/Transmitter (UART3)** | | | | | | |

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**Table 6-105. UART Switching Characteristics[2] (continued)**

| SIGNAL NAME | MUX MODE | DESCRIPTION | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| UART3 (uart3_cts_rctx): H18 | 0 | $t_R$, Rise time | SC0, SC1 = 00[1] | 1 | 15 | ns |
| | | $t_F$, Fall time | | | | |
| | | $C_L$, Output load | | 4 | 60 | pF |
| | | $t_R$, Rise time | SC0, SC1 = 00[1] | 0.4 | 5 | ns |
| | | $t_F$, Fall time | | | | |
| | | $C_L$, Output load | | 2 | 21 | pF |
| | | $t_R$, Rise time | SC0, SC1 = 00[1] | 0.6 | 7 | ns |
| | | $t_F$, Fall time | | | | |
| | | $C_L$, Output load | | 7 | 33 | pF |
| UART3 (uart3_rts_sd): H19 | 0 | $t_R$, Rise time | SC0, SC1 = 00[1] | 1 | 15 | ns |
| | | $t_F$, Fall time | | | | |
| | | $C_L$, Output load | | 4 | 60 | pF |
| | | $t_R$, Rise time | SC0, SC1 = 00[1] | 0.4 | 5 | ns |
| | | $t_F$, Fall time | | | | |
| | | $C_L$, Output load | | 2 | 21 | pF |
| | | $t_R$, Rise time | SC0, SC1 = 00[1] | 0.6 | 7 | ns |
| | | $t_F$, Fall time | | | | |
| | | $C_L$, Output load | | 7 | 33 | pF |
| UART3 (uart3_tx_irtx): H21 | 0 | $t_R$, Rise time | SC0, SC1 = 00[1] | 1 | 15 | ns |
| | | $t_F$, Fall time | | | | |
| | | $C_L$, Output load | | 4 | 60 | pF |
| | | $t_R$, Rise time | SC0, SC1 = 00[1] | 0.4 | 5 | ns |
| | | $t_F$, Fall time | | | | |
| | | $C_L$, Output load | | 2 | 21 | pF |
| | | $t_R$, Rise time | SC0, SC1 = 00[1] | 0.6 | 7 | ns |
| | | $t_F$, Fall time | | | | |
| | | $C_L$, Output load | | 7 | 33 | pF |
| UART3 (uart3_cts_rctx): U26 | 2 | $t_R$, Rise time | | 1.5 | 5.5 | ns |
| | | $t_F$, Fall time | | | | |
| | | $C_L$, Output load | | 2 | 22 | pF |
| UART3 (uart3_rts_sd): U27 | 2 | $t_R$, Rise time | | 1.5 | 5.5 | ns |
| | | $t_F$, Fall time | | | | |
| | | $C_L$, Output load | | 2 | 22 | pF |
| UART3 (uart3_tx_irtx): AH24 | 2 | $t_R$, Rise time | SC0, SC1 = 00[1] | 1 | 15 | ns |
| | | $t_F$, Fall time | | | | |
| | | $C_L$, Output load | | 4 | 60 | pF |
| | | $t_R$, Rise time | SC0, SC1 = 00[1] | 0.4 | 5 | ns |
| | | $t_F$, Fall time | | | | |
| | | $C_L$, Output load | | 2 | 21 | pF |
| | | $t_R$, Rise time | SC0, SC1 = 00[1] | 0.6 | 7 | ns |
| | | $t_F$, Fall time | | | | |
| | | $C_L$, Output load | | 7 | 33 | pF |
| UART3 (uart3_tx_irtx): G26 | 2 | $t_R$, Rise time | | 0.6 | 2.4 | ns |
| | | $t_F$, Fall time | | | | |
| | | $C_L$, Output load | | 2 | 22 | pF |

### Table 6-105. UART Switching Characteristics[2] (continued)

| SIGNAL NAME | MUX MODE | DESCRIPTION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| UART3 (uart3_tx_irtx): T27 | 2 | $t_R$, Rise time | 1.5 | 5.5 | ns |
| | | $t_F$, Fall time | | | |
| | | $C_L$, Output load | 2 | 22 | pF |
| **Universal Asynchronous Receiver/Transmitter (UART4)** | | | | | |
| UART4 (uart4_tx): K8 | 2 | $t_R$, Rise time | 0.6 | 2.4 | ns |
| | | $t_F$, Fall time | | | |
| | | $C_L$, Output load | 2 | 22 | pF |

(1) The mode is configured by bits SC0 and SC1 of the IO cell. For more details, see the *AM/DM37x Multimedia Device Technical Reference Manual* (literature number SPRUGN4).

(2) Caution: Up to a rise time or a fall time of 1.2 ns, this can create EMI parasitics.

### 6.6.7.2 UART3 IrDA

The IrDA module can operate in three different modes:

*   Slow infrared (SIR) (≤ 115.2 Kbits/s)
*   Medium infrared (MIR) (0.576 Mbits/s and 1.152 Mbits/s)
*   Fast infrared (FIR) (4 Mbits/s)
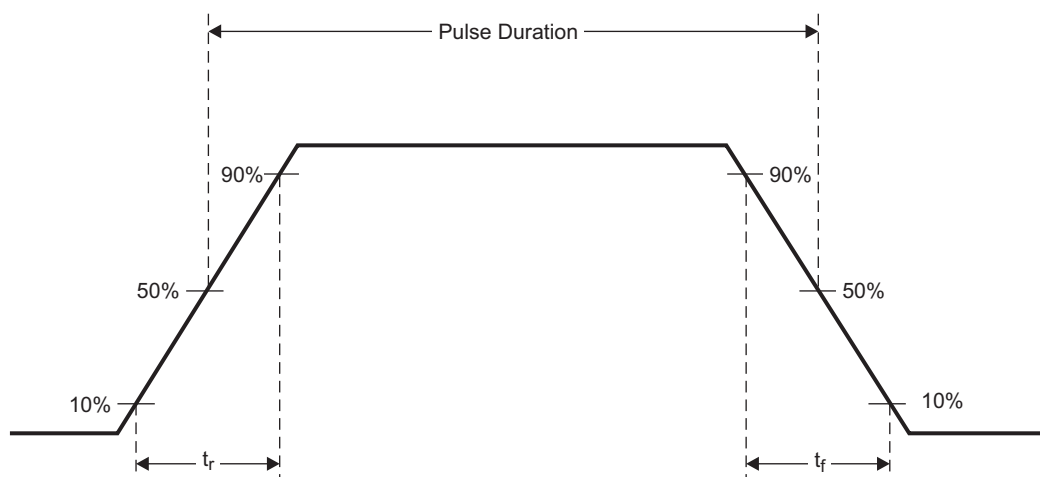


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**Figure 6-64. UART IrDA Pulse Parameters**

### 6.6.7.2.1 UART3 IrDA—Receive Mode

### Table 6-106. UART3 IrDA Signaling Rate and Pulse Duration—Receive Mode

| SIGNALING RATE | ELECTRICAL PULSE DURATION | | | UNIT |
|---|---|---|---|---|
| | MIN | TYP | MAX | |
| **SIR** | | | | |
| 2.4 Kbit/s | 52.17 | 78.13 | 208.33 | µs |
| 9.6 Kbit/s | 13.10 | 19.53 | 52.08 | µs |
| 19.2 Kbit/s | 6.59 | 9.77 | 26.04 | µs |
| 38.4 Kbit/s | 3.34 | 4.88 | 13.02 | µs |
| 57.6 Kbit/s | 2.25 | 3.26 | 8.68 | µs |
| 115.2 Kbit/s | 1.17 | 1.63 | 4.34 | µs |
| **MIR** | | | | |
| 0.576 Mbit/s | 300.55 | 416.67 | 867.86 | ns |

**Table 6-106. UART3 IrDA Signaling Rate and Pulse Duration—Receive Mode (continued)**

| SIGNALING RATE | ELECTRICAL PULSE DURATION | | | UNIT |
|---|---|---|---|---|
| | MIN | TYP | MAX | |
| 1.152 Mbit/s | 192.04 | 208.33 | 433.83 | ns |
| **FIR** | | | | |
| 4.0 Mbit/s (Single pulse) | 62.70 | 125.00 | 170.63 | ns |
| 4.0 Mbit/s (Double pulse) | 208.53 | 250.00 | 291.47 | ns |

**Table 6-107. UART3 IrDA Rise and Fall Times—Receive Mode**

| PARAMETER | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $t_R$ | Rise time, input data uart3_rx_irrx | | | 200 | ns |
| $t_F$ | Fall time, input data uart3_rx_irrx | | | 200 | ns |

#### 6.6.7.2.2  UART3 IrDA—Transmit Mode

**Table 6-108. UART3 IrDA Signaling Rate and Pulse Duration—Transmit Mode**

| SIGNALING RATE | ELECTRICAL PULSE DURATION | | | UNIT |
|---|---|---|---|---|
| | MIN | TYP | MAX | |
| **SIR** | | | | |
| 2.4 Kbit/s | 78.1 | 78.1 | 78.1 | µs |
| 9.6 Kbit/s | 19.5 | 19.5 | 19.5 | µs |
| 19.2 Kbit/s | 9.75 | 9.75 | 9.75 | µs |
| 38.4 Kbit/s | 4.87 | 4.87 | 4.87 | µs |
| 57.6 Kbit/s | 3.25 | 3.25 | 3.25 | µs |
| 115.2 Kbit/s | 1.62 | 1.62 | 1.62 | µs |
| **MIR** | | | | |
| 0.576 Mbit/s | 414 | 416 | 419 | ns |
| 1.152 Mbit/s | 206 | 208 | 211 | ns |
| **FIR** | | | | |
| 4.0 Mbit/s (Single pulse) | 123 | 125 | 128 | ns |
| 4.0 Mbit/s (Double pulse) | 248 | 250 | 253 | ns |

### 6.6.8  Removable Media Interfaces

#### 6.6.8.1  Multimedia Memory Card and Secure Digital IO Card (MMC)

> **NOTE**
>
> For more information, see MMC/SD/SDIO Card Interface chapter of the *AM/DM37x Multimedia Device Technical Reference Manual* (literature number SPRUGN4).

The MMC host controller provides an interface to high-speed and standard MMC, SD memory cards, or SDIO cards. The application interface is responsible for managing transaction semantics. The MMC/SDIO host controller deals with MMC/SDIO protocol at transmission level, packing data, adding CRC, start/end bit, and checking for syntactical correctness.

There are three MMC interfaces on the device:
*   MMC1:
    *   1.8-V / 3-V support
    *   4-bit in Standard MMC, High-Speed MMC, Standard SD, and High-Speed SD modes

- MMC2:
  - 1.8-V support
  - 8-bit without external transceiver
  - 4-bit with external transceiver allowing supporting 3-V peripherals. Transceiver direction control signals are multiplexed with the upper four data bits.
- MMC3:
  - 1.8-V support
  - 8-bit without external transceiver

### 6.6.8.1.1  MMC1 Interface—SD Identification Modes

Table 6-110 and Table 6-111 assume testing over the recommended operating conditions and electrical characteristic conditions below.

#### Table 6-109. MMC1 Interface Timing Conditions—SD Identification Modes

| TIMING CONDITION PARAMETER | | VALUE | UNIT |
|---|---|---|---|
| **Input Conditions** | | | |
| $t_R$ | Input signal rise time | 10 | ns |
| $t_F$ | Input signal fall time | 10 | ns |
| **Output Condition** | | | |
| $C_{LOAD}$ | Output load capacitance[1] | 40 | pF |

(1)  Buffer strength configuration: LB0 = 0.

#### Table 6-110. MMC1 Interface Timing Requirements—SD Identification Modes[1] [2]

| NO. | PARAMETER | | OPP100 | | OPP50 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| **MMC1 Interface (1.8-V IO)** | | | | | | | |
| SD3 | $t_{su(CMDV-CLKIH)}$ | Setup time, mmc1_cmd valid before mmc1_clk rising clock edge | 1198.4 | | 1198.4 | | ns |
| SD4 | $t_{h(CLKIH-CMDIV)}$ | Hold time, mmc1_cmd valid after mmc1_clk rising clock edge | 1249.2 | | 1249.2 | | ns |
| **MMC1 Interface (3.0-V IO)** | | | | | | | |
| SD3 | $t_{su(CMDV-CLKIH)}$ | Setup time, mmc1_cmd valid before mmc1_clk rising clock edge | 1198.4 | | 1198.4 | | ns |
| SD4 | $t_{h(CLKIH-CMDIV)}$ | Hold time, mmc1_cmd valid after mmc1_clk rising clock edge | 1249.2 | | 1249.2 | | ns |

(1)  Corresponding figures showing timing parameters are common with other interface modes. (See SD , HS SD modes).

(2)  See Section 4.3.4, *Processor Clocks*.

#### Table 6-111. MMC1 Interface Switching Characteristics—SD Identification Modes[4] [7]

| NO. | PARAMETER | | OPP100 | | OPP50 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| **SD Identification Mode** | | | | | | | |
| SD1 | $t_{c(clk)}$ | Frequency[1], output clock period | | 0.4 | | 0.4 | MHz |
| SD2 | $t_{W(clkH)}$ | Typical pulse duration, output clock high | X[5]*PO[2] | | X[5]*PO[2] | | ns |
| SD2 | $t_{W(clkL)}$ | Typical pulse duration, output clock low | Y[6]*PO[2] | | Y[6]*PO[2] | | ns |
| | $t_{dc(clk)}$ | Duty cycle error, output clock | | 125 | | 125 | ns |
| | $t_{J(clk)}$ | Jitter standard deviation[3], output clock | | 200 | | 200 | ps |
| **MMC1 Interface (1.8-V IO)** | | | | | | | |
| | $t_{R(clk)}$ | Rise time, output clock | | 10 | | 10 | ns |
| | $t_{F(clk)}$ | Fall time, output clock | | 10 | | 10 | ns |

### Table 6-111. MMC1 Interface Switching Characteristics—SD Identification Modes[4] [7]  (continued)

| NO. | PARAMETER | | OPP100 | | OPP50 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| | $t_{R(data)}$ | Rise time, output data | | 10 | | 10 | ns |
| | $t_{F(data)}$ | Fall time, output data | | 10 | | 10 | ns |
| SD5 | $t_{d(CLKOH-CMD)}$ | Delay time, mmc1_clk rising clock edge to mmc1_cmd transition | 6.3 | 2492.7 | 6.3 | 2492.7 | ns |
| **MMC1 Interface (3.0-V IO)** | | | | | | | |
| | $t_{R(clk)}$ | Rise time, output clock | | 10 | | 10 | ns |
| | $t_{F(clk)}$ | Fall time, output clock | | 10 | | 10 | ns |
| | $t_{R(data)}$ | Rise time, output data | | 10 | | 10 | ns |
| | $t_{F(data)}$ | Fall time, output data | | 10 | | 10 | ns |
| SD5 | $t_{d(CLKOH-CMD)}$ | Delay time, mmc1_clk rising clock edge to mmc1_cmd transition | 6.3 | 2492.7 | 6.3 | 2492.7 | ns |

(1)  Related with the output clock maximum and minimum frequencies programmable in mmc module.

(2)  PO = output clock period in ns

(3)  The jitter probability density can be approximated by a Gaussian function.

(4)  Corresponding figures showing timing parameters are common with other interface modes. (See SD, HS SD modes).

(5)  The X parameter is defined as follows:

| CLKD | X |
|---|---|
| 1 or Even | 0.5 |
| Odd | (trunk[CLKD/2]+1)/CLKD |

All required details about clock division factor CLKD can be found in the *AM/DM37x Multimedia Device Technical Reference Manual* (literature number SPRUGN4).

(6)  The Y parameter is defined as follows:

| CLKD | Y |
|---|---|
| 1 or Even | 0.5 |
| Odd | (trunk[CLKD/2])/CLKD |

All required details about clock division factor CLKD can be found in the *AM/DM37x Multimedia Device Technical Reference Manual* (literature number SPRUGN4).
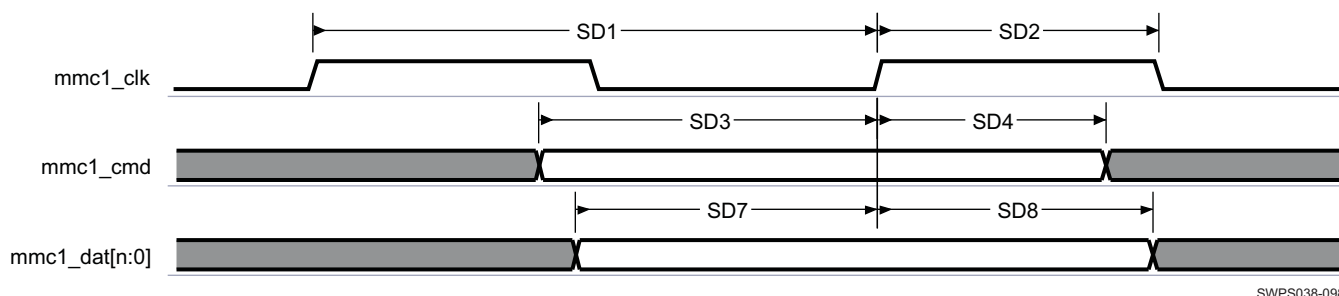
(7)  See Section 4.3.4, *Processor Clocks*.

### 6.6.8.1.2   MMC1 Interface—High-Speed SD Mode

Table 6-113 and Table 6-114 assume testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-65 and Figure 6-66).

### Table 6-112. MMC1 Interface Timing Conditions—High-Speed SD Mode

| TIMING CONDITION PARAMETER | | VALUE | UNIT |
|---|---|---|---|
| **Input Conditions** | | | |
| $t_R$ | Input signal rise time | 3 | ns |
| $t_F$ | Input signal fall time | 3 | ns |
| **Output Condition** | | | |
| $C_{LOAD}$ | Output load capacitance[1] | 40 | pF |

(1)  Buffer strength configuration: SPEEDCTRL = 1.

**Table 6-113. MMC1 Interface Timing Requirements—High-Speed SD Mode[2]**

| NO. | PARAMETER | | OPP100 | | OPP50 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| **MMC1 Interface (1.8-V IO)** | | | | | | | |
| HSSD3 | $t_{su(CMDV-CLKIH)}$ | Setup time, mmc1_cmd valid before mmc1_clk rising clock edge | 5.6 | | 26 | | ns |
| HSSD4 | $t_{h(CLKIH-CMDIV)}$ | Hold time, mmc1_cmd valid after mmc1_clk rising clock edge | 2.3 | | 1.9 | | ns |
| HSSD7 | $t_{su(DATxV-CLKIH)}$ | Setup time, mmc1_dat[n:0][1] valid before mmc1_clk rising clock edge | 5.6 | | 26 | | ns |
| HSSD8 | $t_{h(CLKIH-DATxIV)}$ | Hold time, mmc1_dat[n:0][1] valid after mmc1_clk rising clock edge | 2.3 | | 1.9 | | ns |
| **MMC1 Interface (3.0-V IO)** | | | | | | | |
| HSSD3 | $t_{su(CMDV-CLKIH)}$ | Setup time, mmc1_cmd valid before mmc1_clk rising clock edge | 5.6 | | 26 | | ns |
| HSSD4 | $t_{h(CLKIH-CMDIV)}$ | Hold time, mmc1_cmd valid after mmc1_clk rising clock edge | 2.3 | | 1.9 | | ns |
| HSSD7 | $t_{su(DATxV-CLKIH)}$ | Setup time, mmc1_dat[n:0][1] valid before mmc1_clk rising clock edge | 5.6 | | 26 | | ns |
| HSSD8 | $t_{h(CLKIH-DATxIV)}$ | Hold time, mmc1_dat[n:0][1] valid after mmc1_clk rising clock edge | 2.3 | | 1.9 | | ns |

(1)  In mmc1_dat[n:0], n is equal to 3.

(2)  See Section 4.3.4, *Processor Clocks.*

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### Table 6-114. MMC1 Interface Switching Characteristics—High-Speed SD Mode[7]

| NO. | PARAMETER | | OPP100 | | OPP50 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| **High-Speed SD Mode** | | | | | | | |
| HSSD1 | $t_{c(clk)}$ | Frequency[1], output clock period | | 48 | | 24 | MHz |
| HSSD2 | $t_{W(clkH)}$ | Typical pulse duration, output clock high | X[4]*PO[2] | | X[4]*PO[2] | | ns |
| HSSD2 | $t_{W(clkL)}$ | Typical pulse duration, output clock low | Y[5]*PO[2] | | Y[5]*PO[2] | | ns |
| | $t_{dc(clk)}$ | Duty cycle error, output clock | | 1041.67 | | 2083.33 | ps |
| | $t_{J(clk)}$ | Jitter standard deviation[3], output clock | | 200 | | 200 | ps |
| **MMC1 Interface (1.8-V IO)** | | | | | | | |
| | $t_{R(clk)}$ | Rise time, output clock | | 3 | | 3 | ns |
| | $t_{F(clk)}$ | Fall time, output clock | | 3 | | 3 | ns |
| | $t_{R(data)}$ | Rise time, output data | | 3 | | 3 | ns |
| | $t_{F(data)}$ | Fall time, output data | | 3 | | 3 | ns |
| HSSD5 | $t_{d(CLKOH-CMD)}$ | Delay time, mmc1_clk rising clock edge to mmc1_cmd transition | 3.72 | 14.11 | 4.13 | 34.53 | ns |
| HSSD6 | $t_{d(CLKOH-DATx)}$ | Delay time, mmc1_clk rising clock edge to mmc1_dat[n:0][6] transition | 3.72 | 14.11 | 4.13 | 34.53 | ns |
| **MMC1 Interface (3.0-V IO)** | | | | | | | |
| | $t_{R(clk)}$ | Rise time, output clock | | 3 | | 3 | ns |
| | $t_{F(clk)}$ | Fall time, output clock | | 3 | | 3 | ns |
| | $t_{R(data)}$ | Rise time, output data | | 3 | | 3 | ns |
| | $t_{F(data)}$ | Fall time, output data | | 3 | | 3 | ns |
| HSSD5 | $t_{d(CLKOH-CMD)}$ | Delay time, mmc1_clk rising clock edge to mmc1_cmd transition | 3.72 | 14.11 | 4.13 | 34.53 | ns |
| HSSD6 | $t_{d(CLKOH-DATx)}$ | Delay time, mmc1_clk rising clock edge to mmc1_dat[n:0][6] transition | 3.72 | 14.11 | 4.13 | 34.53 | ns |

(1) Related with the output clock maximum and minimum frequencies programmable in MMC module.

(2) PO = output clock period in ns

(3) The jitter probability density can be approximated by a Gaussian function.

(4) The X parameter is defined as follows:

| CLKD | X |
|---|---|
| 1 or Even | 0.5 |
| Odd | (trunk[CLKD/2]+1)/CLKD |

All required details about clock division factor CLKD can be found in the *AM/DM37x Multimedia Device Technical Reference Manual* (literature number SPRUGN4).

(5) The Y parameter is defined as follows:

| CLKD | Y |
|---|---|
| 1 or Even | 0.5 |
| Odd | (trunk[CLKD/2])/CLKD |

All required details about clock division factor CLKD can be found in the *AM/DM37x Multimedia Device Technical Reference Manual* (literature number SPRUGN4).

(6) In mmc1_dat[n:0], n is equal to 3.

(7) See Section 4.3.4, *Processor Clocks*.

**Figure 6-65. MMC1 Interface—High-Speed SD Mode—Data/Command Receive**



**Figure 6-66. MMC1 Interface—High-Speed SD Mode—Data/Command Transmit**

### 6.6.8.1.3 MMC1 Interface—Standard SD Mode

Table 6-116 and Table 6-117 assume testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-67 and Figure 6-68).

**Table 6-115. MMC1 Interface Timing Conditions—Standard SD Mode**

| TIMING CONDITION PARAMETER | | VALUE | UNIT |
|---|---|---|---|
| **Input Conditions** | | | |
| $t_R$ | Input signal rise time | 10 | ns |
| $t_F$ | Input signal fall time | 10 | ns |
| **Output Condition** | | | |
| $C_{LOAD}$ | Output load capacitance[1] | 40 | pF |

(1) Buffer strength configuration: SPEEDCTRL = 1.

**Table 6-116. MMC1 Interface Timing Requirements—Standard SD Mode[1] [2] [4]**

| NO. | PARAMETER | | OPP100 | | OPP50 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| **MMC1 Interface (1.8-V IO)** | | | | | | | |
| SD3 | $t_{su(CMDV-CLKIH)}$ | Setup time, mmc1_cmd valid before mmc1_clk rising clock edge | 3.3 | | 21.9 | | ns |
| SD4 | $t_{h(CLKIH-CMDIV)}$ | Hold time, mmc1_cmd valid after mmc1_clk rising clock edge | 18.1 | | 36.7 | | ns |
| SD7 | $t_{su(DATxV-CLKIH)}$ | Setup time, mmc1_dat[n:0][3] valid before mmc1_clk rising clock edge | 3.3 | | 21.9 | | ns |
| SD8 | $t_{h(CLKIH-DATxIV)}$ | Hold time, mmc1_dat[n:0][3] valid after mmc1_clk rising clock edge | 18.1 | | 36.7 | | ns |
| **MMC1 Interface (3.0-V IO)** | | | | | | | |
| SD3 | $t_{su(CMDV-CLKIH)}$ | Setup time, mmc1_cmd valid before mmc1_clk rising clock edge | 3.3 | | 21.9 | | ns |

### Table 6-116. MMC1 Interface Timing Requirements—Standard SD Mode[1] [2] [4]  (continued)

| NO. | PARAMETER | | OPP100 | | OPP50 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| SD4 | $t_{h(CLKIH-CMDIV)}$ | Hold time, mmc1_cmd valid after mmc1_clk rising clock edge | 18.1 | | 36.7 | | ns |
| SD7 | $t_{su(DATxV-CLKIH)}$ | Setup time, mmc1_dat[n:0][3] valid before mmc1_clk rising clock edge | 3.3 | | 21.9 | | ns |
| SD8 | $t_{h(CLKIH-DATxIV)}$ | Hold time, mmc1_dat[n:0][3] valid after mmc1_clk rising clock edge | 18.1 | | 36.7 | | ns |

(1)  Timing parameters are referred to output clock specified in Table 6-117.

(2)  The timing requirements are assured for the cycle jitter and duty cycle error conditions specified in Table 6-117.

(3)  In mmc1_dat[n:0], n is equal to 3.

(4)  See Section 4.3.4, *Processor Clocks*.

### Table 6-117. MMC1 Interface Switching Characteristics—Standard SD Mode[7]

| NO. | PARAMETER | | OPP100 | | OPP50 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| **Standard SD Mode** | | | | | | | |
| SD1 | $t_{c(clk)}$ | Frequency[1], output clock period | | 24 | | 12 | MHz |
| SD2 | $t_{W(clkH)}$ | Typical pulse duration, output clock high | X[4]*PO[2] | | X[4]*PO[2] | | ns |
| SD2 | $t_{W(clkL)}$ | Typical pulse duration, output clock low | Y[5]*PO[2] | | Y[5]*PO[2] | | ns |
| | $t_{dc(clk)}$ | Duty cycle error, output clock | | 2083.33 | | 4166.67 | ps |
| | $t_{J(clk)}$ | Jitter standard deviation[3], output clock | | 200 | | 200 | ps |
| **MMC1 Interface (1.8-V)** | | | | | | | |
| | $t_{R(clk)}$ | Rise time, output clock | | 10 | | 10 | ns |
| | $t_{F(clk)}$ | Fall time, output clock | | 10 | | 10 | ns |
| | $t_{R(data)}$ | Rise time, output data | | 10 | | 10 | ns |
| | $t_{F(data)}$ | Fall time, output data | | 10 | | 10 | ns |
| SD5 | $t_{d(CLKOH-CMD)}$ | Delay time, mmc1_clk rising clock edge to mmc1_cmd transition | 6.13 | 35.53 | 6.3 | 77.03 | ns |
| SD6 | $t_{d(CLKOH-DATx)}$ | Delay time, mmc1_clk rising clock edge to mmc1_dat[n:0][6] transition | 6.13 | 35.53 | 6.3 | 77.03 | ns |
| **MMC1 Interface (3.0-V)** | | | | | | | |
| | $t_{R(clk)}$ | Rise time, output clock | | 10 | | 10 | ns |
| | $t_{F(clk)}$ | Fall time, output clock | | 10 | | 10 | ns |
| | $t_{R(data)}$ | Rise time, output data | | 10 | | 10 | ns |
| | $t_{F(data)}$ | Fall time, output data | | 10 | | 10 | ns |
| SD5 | $t_{d(CLKOH-CMD)}$ | Delay time, mmc1_clk rising clock edge to mmc1_cmd transition | 6.13 | 35.53 | 6.3 | 77.03 | ns |
| SD6 | $t_{d(CLKOH-DATx)}$ | Delay time, mmc1_clk rising clock edge to mmc1_dat[n:0][6] transition | 6.13 | 35.53 | 6.3 | 77.03 | ns |

(1)  Related with the output clock maximum and minimum frequencies programmable in MMC module.

(2)  PO = output clock period in ns

(3)  The jitter probability density can be approximated by a Gaussian function.

(4)  The X parameter is defined as follows:

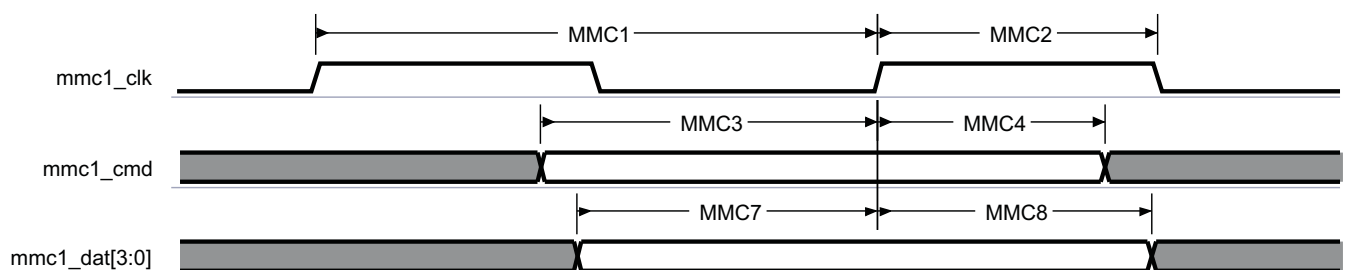| CLKD | X |
|---|---|
| 1 or Even | 0.5 |
| Odd | (trunk[CLKD/2]+1)/CLKD |

All required details about clock division factor CLKD can be found in the *AM/DM37x Multimedia Device Technical Reference Manual* (literature number SPRUGN4).

(5) The Y parameter is defined as follows:

| CLKD | Y |
|---|---|
| 1 or Even | 0.5 |
| Odd | (trunk[CLKD/2])/CLKD |

All required details about clock division factor CLKD can be found in the *AM/DM37x Multimedia Device Technical Reference Manual* (literature number SPRUGN4).

(6) In mmc1_dat[n:0], n is equal to 3.

(7) See Section 4.3.4, *Processor Clocks*.



SWPS038-098

**Figure 6-67. MMC1 Interface—Standard SD Mode—Data/Command Receive**



SWPS038-099
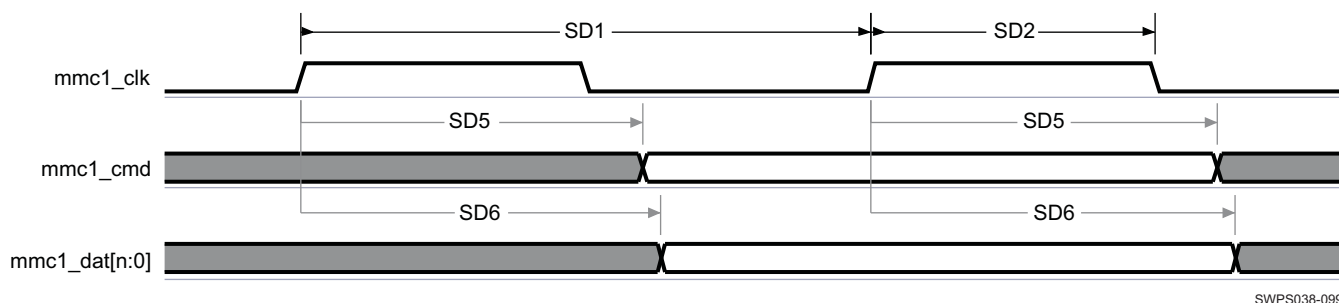
**Figure 6-68. MMC1 Interface—Standard SD Mode—Data/Command Transmit**

### 6.6.8.1.4  *MMC1 Interface—Standard MMC and MMC Identification Modes*

Table 6-119 and Table 6-120 assume testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-69 and Figure 6-70).

### Table 6-118. MMC1 Interface Timing Conditions—Standard MMC and MMC Identification Modes

| TIMING CONDITION PARAMETER | | VALUE | UNIT |
|---|---|---|---|
| **Input Conditions** | | | |
| $t_R$ | Input signal rise time | 3 | ns |
| $t_F$ | Input signal fall time | 3 | ns |
| **Output Conditions** | | | |
| $C_{LOAD}$ | Output load capacitance[1] | 30 | pF |

(1)  Buffer strength configuration: SPEEDCTRL = 1.

### Table 6-119. MMC1 Interface Timing Requirements—Standard MMC and MMC Identification Modes[2] [3] [4]

| NO. | PARAMETER | | OPP100 | | OPP50 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| **MMC1 Interface (1.8-V IO)** | | | | | | | |
| MMC3 | $t_{su(CMDV-CLKIH)}$ | Setup time, mmc1_cmd valid before mmc1_clk rising clock edge | 13.6 | | 55.1 | | ns |
| MMC4 | $t_{h(CLKIH-CMDIV)}$ | Hold time, mmc1_cmd valid after mmc1_clk rising clock edge | 7.7 | | 7.5 | | ns |
| MMC7 | $t_{su(DATxV-CLKIH)}$ | Setup time, mmc1_dat[n:0][1] valid before mmc1_clk rising clock edge | 13.6 | | 55.1 | | ns |
| MMC8 | $t_{h(CLKIH-DATxIV)}$ | Hold time, mmc1_dat[n:0][1] valid after mmc1_clk rising clock edge | 7.7 | | 7.5 | | ns |
| **MMC1 Interface (3.0-V IO)** | | | | | | | |
| MMC3 | $t_{su(CMDV-CLKIH)}$ | Setup time, mmc1_cmd valid before mmc1_clk rising clock edge | 13.6 | | 55.1 | | ns |
| MMC4 | $t_{h(CLKIH-CMDIV)}$ | Hold time, mmc1_cmd valid after mmc1_clk rising clock edge | 7.7 | | 7.5 | | ns |
| MMC7 | $t_{su(DATxV-CLKIH)}$ | Setup time, mmc1_dat[n:0][1] valid before mmc1_clk rising clock edge | 13.6 | | 55.1 | | ns |
| MMC8 | $t_{h(CLKIH-DATxIV)}$ | Hold time, mmc1_dat[n:0][1] valid after mmc1_clk rising clock edge | 7.7 | | 7.5 | | ns |

(1)  In mmc1_dat[n:0], n is equal to 3.

(2)  Timing parameters are referred to output clock specified in Table 6-120.

(3)  The timing requirements are assured for the cycle jitter and duty cycle error conditions specified in Table 6-120.

(4)  See Section 4.3.4, *Processor Clocks*.

### Table 6-120. MMC1 Interface Switching Characteristics—Standard MMC and MMC Identification Modes[7]

| NO. | PARAMETER | | OPP100 | | OPP50 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| **MMC Identification Mode** | | | | | | | |
| MMC1 | $1/t_{c(clk)}$ | Frequency[1], output clk period | | 0.4 | | 0.4 | MHz |
| MMC2 | $t_{W(clkH)}$ | Typical pulse duration, output clk high | X[5]*PO[2] | | X[5]*PO[2] | | ns |
| MMC2 | $t_{W(clkL)}$ | Typical pulse duration, output clk low | Y[6]*PO[2] | | Y[6]*PO[2] | | ns |
| | $t_{dc(clk)}$ | Duty cycle error, output clk | | 125 | | 125 | ns |
| | $t_{J(clk)}$ | Jitter standard deviation[3], output clk | | 200 | | 200 | ps |
| **Standard MMC Identification Mode** | | | | | | | |
| MMC1 | $t_{c(clk)}$ | Frequency[1], output clk period | | 24 | | 12 | MHz |
| MMC2 | $t_{W(clkH)}$ | Typical pulse duration, output clk high | X[5]*PO[2] | | X[5]*PO[2] | | ns |
| MMC2 | $t_{W(clkL)}$ | Typical pulse duration, output clk low | Y[6]*PO[2] | | Y[6]*PO[2] | | ns |
| | $t_{dc(clk)}$ | Duty cycle error, output clk | | 2083.3 | | 4166.7 | ps |
| | $t_{J(clk)}$ | Jitter standard deviation[3], output clk | | 200 | | 200 | ps |
| **MMC1 Interface (1.8-V IO)** | | | | | | | |
| | $t_{R(clk)}$ | Rise time, output clk | | 10 | | 10 | ns |

### Table 6-120. MMC1 Interface Switching Characteristics—Standard MMC and MMC Identification Modes[7] (continued)

| NO. | | PARAMETER | OPP100 | | OPP50 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| | $t_{F(clk)}$ | Fall time, output clk | | 10 | | 10 | ns |
| | $t_{R(data)}$ | Rise time, output data | | 10 | | 10 | ns |
| | $t_{F(data)}$ | Fall time, output data | | 10 | | 10 | ns |
| MMC5 | $t_{d(CLKOH-CMD)}$ | Delay time, mmc1_clk rising clock edge to mmc1_cmd transition | 4.1 | 37.6 | 4.3 | 79 | ns |
| MMC6 | $t_{d(CLKOH-DATx)}$ | Delay time, mmc1_clk rising clock edge to mmc1_dat[n:0][4] transition | 4.1 | 37.6 | 4.3 | 79 | ns |
| **MMC1 Interface (3.0-V IO)** | | | | | | | |
| | $t_{R(clk)}$ | Rise time, output clk | | 10 | | 10 | ns |
| | $t_{F(clk)}$ | Fall time, output clk | | 10 | | 10 | ns |
| | $t_{R(data)}$ | Rise time, output data | | 10 | | 10 | ns |
| | $t_{F(data)}$ | Fall time, output data | | 10 | | 10 | ns |
| MMC5 | $t_{d(CLKOH-CMD)}$ | Delay time, mmc1_clk rising clock edge to mmc1_cmd transition | 4.1 | 37.6 | 4.3 | 79 | ns |
| MMC6 | $t_{d(CLKOH-DATx)}$ | Delay time, mmc1_clk rising clock edge to mmc1_dat[n:0][4] transition | 4.1 | 37.6 | 4.3 | 79 | ns |

(1) Related with the output clock maximum and minimum frequencies programmable in MMC module.

(2) PO = output clock period in ns

(3) The jitter probability density can be approximated by a Gaussian function.

(4) In mmc1_dat[n:0], n is equal to 3.

(5) The X parameter is defined as follows:

| CLKD | X |
|---|---|
| 1 or Even | 0.5 |
| Odd | (trunk[CLKD/2]+1)/CLKD |

All required details about clock division factor CLKD can be found in the *AM/DM37x Multimedia Device Technical Reference Manual* (literature number SPRUGN4).

(6) The Y parameter is defined as follows:

| CLKD | Y |
|---|---|
| 1 or Even | 0.5 |
| Odd | (trunk[CLKD/2])/CLKD |

All required details about clock division factor CLKD can be found in the *AM/DM37x Multimedia Device Technical Reference Manual* (literature number SPRUGN4).

(7) See Section 4.3.4, *Processor Clocks.*



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**Figure 6-69. MMC1 Interface—Standard MMC and MMC Identification Modes—Data/Command Receive**

SWPS038-103
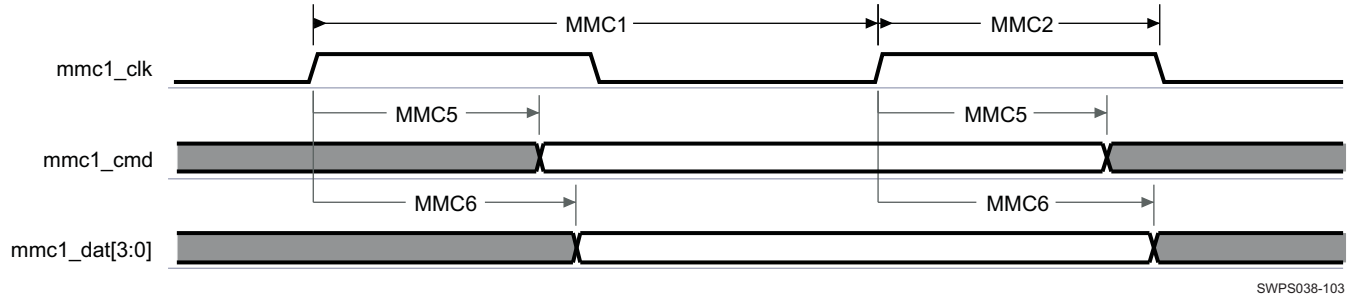
**Figure 6-70. MMC1 Interface—Standard MMC and MMC Identification Modes—Data/Command Transmit**

### 6.6.8.1.5 *MMC1 Interface—High-Speed MMC Mode*

Table 6-122 and Table 6-123 assume testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-71 and Figure 6-72).

**Table 6-121. MMC1 Interface Timing Conditions—High-Speed MMC Mode**

| TIMING CONDITION PARAMETER | | VALUE | UNIT |
|---|---|---|---|
| **Input Conditions** | | | |
| $t_R$ | Input signal rise time | 3 | ns |
| $t_F$ | Input signal fall time | 3 | ns |
| **Output Conditions** | | | |
| $C_{LOAD}$ | Output load capacitance[1] | 30 | pF |

(1) The load setting of the IO buffer: SPEEDCTRL = 1.

**Table 6-122. MMC1 Interface Timing Requirements—High-Speed MMC Mode[2] [3] [4] [5]**

| NO. | PARAMETER | | OPP100 | | OPP50 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| **MMC1 Interface (1.8-V IO)** | | | | | | | |
| MMC3 | $t_{su(CMDV-CLKIH)}$ | Setup time, mmc1_cmd valid before mmc1_clk rising clock edge | 5.6 | | 26.0 | | ns |
| MMC4 | $t_{h(CLKIH-CMDIV)}$ | Hold time, mmc1_cmd valid after mmc1_clk rising clock edge | 2.3 | | 1.9 | | ns |
| MMC7 | $t_{su(DATxV-CLKIH)}$ | Setup time, mmc1_dat[n:0][1] valid before mmc1_clk rising clock edge | 5.6 | | 26.0 | | ns |
| MMC8 | $t_{h(CLKIH-DATxIV)}$ | Hold time, mmc1_dat[n:0][1] valid after mmc1_clk rising clock edge | 2.3 | | 1.9 | | ns |
| **MMC1 Interface (3.0-V IO)** | | | | | | | |
| MMC3 | $t_{su(CMDV-CLKIH)}$ | Setup time, mmc1_cmd valid before mmc1_clk rising clock edge | 5.6 | | 26.0 | | ns |
| MMC4 | $t_{h(CLKIH-CMDIV)}$ | Hold time, mmc1_cmd valid after mmc1_clk rising clock edge | 2.3 | | 1.9 | | ns |
| MMC7 | $t_{su(DATxV-CLKIH)}$ | Setup time, mmc1_dat[n:0][1] valid before mmc1_clk rising clock edge | 5.6 | | 26.0 | | ns |
| MMC8 | $t_{h(CLKIH-DATxIV)}$ | Hold time, mmc1_dat[n:0][1] valid after mmc1_clk rising clock edge | 2.3 | | 1.9 | | ns |

(1) In mmc1_dat[n:0], n is equal to 3.

(2) Timing parameters are referred to output clock specified in Table 6-123.

(3) The timing requirements are assured for the cycle jitter and duty cycle error conditions specified in Table 6-123.

(4) Corresponding figures showing timing parameters are common with the Standard MMC mode figures.

(5) See Section 4.3.4, *Processor Clocks.*

### Table 6-123. MMC1 Interface Switching Characteristics—High-Speed MMC Mode[4] [8]

| NO. | PARAMETER | | OPP100 | | OPP50 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| MMC1 | $t_{c(clk)}$ | Frequency[1], output clk period | | 48 | | 24 | MHz |
| MMC2 | $t_{W(clkH)}$ | Typical pulse duration, output clk high | $X^{[6]}*PO^{[2]}$ | | $X^{[6]}*PO^{[2]}$ | | ns |
| MMC2 | $t_{W(clkL)}$ | Typical pulse duration, output clk low | $Y^{[7]}*PO^{[2]}$ | | $Y^{[7]}*PO^{[2]}$ | | ns |
| | $t_{dc(clk)}$ | Duty cycle error, output clk | | 1041.7 | | 2083.3 | ps |
| | $t_{J(clk)}$ | Jitter standard deviation[3], output clk | | 200 | | 200 | ps |
| **MMC1 Interface (1.8-V IO)** | | | | | | | |
| | $t_{R(clk)}$ | Rise time, output clk | | 3 | | 3 | ns |
| | $t_{F(clk)}$ | Fall time, output clk | | 3 | | 3 | ns |
| | $t_{R(data)}$ | Rise time, output data | | 3 | | 3 | ns |
| | $t_{F(data)}$ | Fall time, output data | | 3 | | 3 | ns |
| MMC5 | $t_{d(CLKOH-CMD)}$ | Delay time, mmc1_clk rising clock edge to mmc1_cmd transition | 3.7 | 14.1 | 4.1 | 34.5 | ns |
| MMC6 | $t_{d(CLKOH-DATx)}$ | Delay time, mmc1_clk rising clock edge to mmc1_dat[n:0][5] transition | 3.7 | 14.1 | 4.1 | 34.5 | ns |
| **MMC1 Interface (3.0-V IO)** | | | | | | | |
| | $t_{R(clk)}$ | Rise time, output clk | | 3 | | 3 | ns |
| | $t_{F(clk)}$ | Fall time, output clk | | 3 | | 3 | ns |
| | $t_{R(data)}$ | Rise time, output data | | 3 | | 3 | ns |
| | $t_{F(clk)}$ | Fall time, output data | | 3 | | 3 | ns |
| MMC5 | $t_{d(CLKOH-CMD)}$ | Delay time, mmc1_clk rising clock edge to mmc1_cmd transition | 3.7 | 14.1 | 4.1 | 34.5 | ns |
| MMC6 | $t_{d(CLKOH-DATx)}$ | Delay time, mmc1_clk rising clock edge to mmc1_dat[n:0][5] transition | 3.7 | 14.1 | 4.1 | 34.5 | ns |

(1) Related with the output clock maximum and minimum frequencies programmable in MMC module.

(2) PO = output clock period in ns

(3) The jitter probability density can be approximated by a Gaussian function.

(4) Corresponding figures showing timing parameters are common with the Standard MMC mode figures.

(5) In MMC1_dat[n:0], n is equal to 3.

(6) The X parameter is defined as follows:

| CLKD | X |
|---|---|
| 1 or Even | 0.5 |
| Odd | (trunk[CLKD/2]+1)/CLKD |

All required details about clock division factor CLKD can be found in the *AM/DM37x Multimedia Device Technical Reference Manual* (literature number SPRUGN4).

(7) The Y parameter is defined as follows:

| CLKD | Y |
|---|---|
| 1 or Even | 0.5 |
| Odd | (trunk[CLKD/2])/CLKD |

All required details about clock division factor CLKD can be found in the *AM/DM37x Multimedia Device Technical Reference Manual* (literature number SPRUGN4).

(8) See Section 4.3.4, *Processor Clocks*.

SWPS038-100
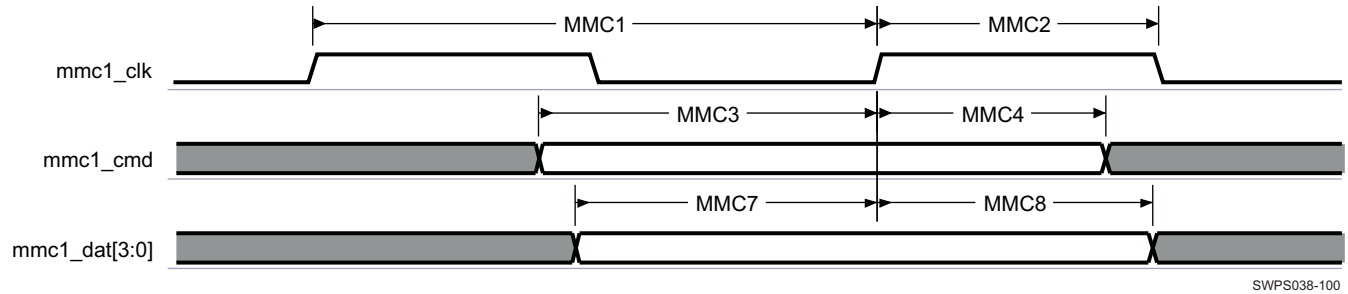
**Figure 6-71. MMC1 Interface—High-Speed MMC Mode—Data/Command Receive**



SWPS038-101
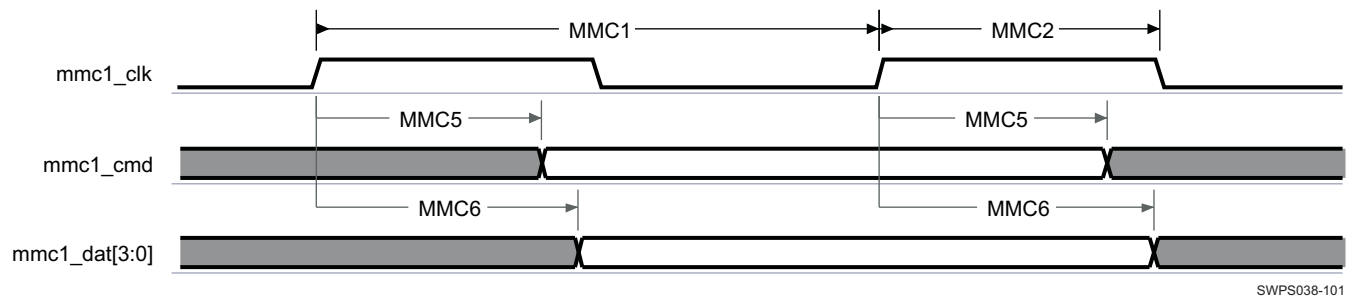
**Figure 6-72. MMC1 Interface—High-Speed MMC Mode—Data/Command Transmit**

### 6.6.8.1.6 MMC2 and MMC3 Interfaces—SDIO Identification Mode

Table 6-125 and Table 6-126 assume testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-73 and Figure 6-74).

**Table 6-124. MMC2 and MMC3 Interfaces Timing Conditions—SDIO Identification Mode**

| TIMING CONDITION PARAMETER | | VALUE | UNIT |
|---|---|---|---|
| **Input Conditions** | | | |
| $t_R$ | Input signal rise time | 10 | ns |
| $t_F$ | Input signal fall time | 10 | ns |
| **Output Condition** | | | |
| $C_{LOAD}$ | Output load capacitance[1] | 5 | pF |

(1) Buffer strength configuration: LB0 = 0

**Table 6-125. MMC2 and MMC3 Interfaces Timing Requirements—SDIO Identification Mode[1][2]**

| NO. | PARAMETER | | OPP100 | | OPP50 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| **MMC2 and MMC3 Interface (1.8-V IO)** | | | | | | | |
| SD3 | $t_{su(CMDV-CLKIH)}$ | Setup time, mmcx_cmd valid before mmcx_clk rising clock edge | 1198.4 | | 1198.4 | | ns |
| SD4 | $t_{h(CLKIH-CMDIV)}$ | Hold time, mmcx_cmd valid after mmcx_clk rising clock edge | 1249.2 | | 1249.2 | | ns |

(1) See Section 4.3.4, *Processor Clocks.*

(2) In mmcx, x is equal to 2 or 3.

### Table 6-126. MMC2 and MMC3 Interfaces Switching Characteristics—SDIO Identification Mode[4][7][7]

| NO. | PARAMETER | | OPP100 | | OPP50 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| **Standard SDIO Mode** | | | | | | | |
| SD1 | $t_{c(clk)}$ | Frequency[1], output clock period | | 0.4 | | 0.4 | MHz |
| SD2 | $t_{W(clkH)}$ | Typical pulse duration, output clock high | $X^{[5]} *$ $PO^{[2]}$ | | $X^{[5]} *$ $PO^{[2]}$ | | ns |
| SD2 | $t_{W(clkL)}$ | Typical pulse duration, output clock low | $Y^{[6]} *$ $PO^{[2]}$ | | $Y^{[6]} *$ $PO^{[2]}$ | | ns |
| | $t_{dc(clk)}$ | Duty cycle error, output clock | | 125 | | 125 | ns |
| | $t_{J(clk)}$ | Jitter standard deviation[3], output clock | | 200 | | 200 | ps |
| | $t_{R(clk)}$ | Rise time, output clock | | 10 | | 10 | ns |
| | $t_{F(clk)}$ | Fall time, output clock | | 10 | | 10 | ns |
| | $t_{R(data)}$ | Rise time, output data | | 10 | | 10 | ns |
| | $t_{F(data)}$ | Fall time, output data | | 10 | | 10 | ns |
| SD5 | $t_{d(CLKOH-CMD)}$ | Delay time, mmcx_clk rising clock edge to mmcx_cmd transition | 6.3 | 2492.7 | 6.3 | 77.03 | ns |

(1)  Related to the output mmcx_clk maximum and minimum frequency.

(2)  P = output mmcx_clk period in ns

(3)  The jitter probability density can be approximated by a Gaussian function.

(4)  Corresponding figures showing timing parameters are common with other interface modes (see SDIO, HS SDIO modes).

(5)  The X parameter is defined as follows:

| CLKD | X |
|---|---|
| 1 or Even | 0.5 |
| Odd | (trunk[CLKD/2]+1)/CLKD |

   All required details about clock division factor CLKD can be found in the *AM/DM37x Multimedia Device Technical Reference Manual* (literature number SPRUGN4).

(6)  The Y parameter is defined as follows:

| CLKD | Y |
|---|---|
| 1 or Even | 0.5 |
| Odd | (trunk[CLKD/2])/CLKD |

   All required details about clock division factor CLKD can be found in the *AM/DM37x Multimedia Device Technical Reference Manual* (literature number SPRUGN4).

(7)  In mmcx, x is equal to 2 or 3.

#### 6.6.8.1.7  MMC2 and MMC3 Interfaces—High-Speed SDIO Mode

Table 6-128 and Table 6-129 assume testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-73 and Figure 6-74).

### Table 6-127. MMC2 and MMC3 Interfaces Timing Conditions—High-Speed SDIO Mode

| TIMING CONDITION PARAMETER | | VALUE | | UNIT |
|---|---|---|---|---|
| | | MIN | MAX | |
| **Input Conditions** | | | | |
| $t_R$ | Input signal rise time | 0.18 | 5.69 | ns |
| $t_F$ | Input signal fall time | 0.19 | 5.70 | ns |
| **Output Condition** | | | | |
| $C_{LOAD}$ | Output load capacitance[1] | | 5 | pF |

(1) Buffer strength configuration for MMC2 and MMC3: LB0 = 0.

**Table 6-128. MMC2 and MMC3 Interfaces Timing Requirements—High-Speed SDIO Mode[2]**

| NO. | PARAMETER | | OPP100 | | OPP50 | | UNIT |
|-----|-----------|-----------|-----|-----|-----|-----|------|
| | | | MIN | MAX | MIN | MAX | |
| HSSD3 | $t_{su(dV-clkH)}$ | Setup time, mmcx_cmd valid before mmcx_clk rising clock edge | 3.4 | | 23.8 | | ns |
| HSSD4 | $t_{h(clkH-dV)}$ | Hold time, mmcx_cmd valid after mmcx_clk rising clock edge | 1.7 | | 1.3 | | ns |
| HSSD7 | $t_{su(dV-clkH)}$ | Setup time, mmcx_dat[n:0][1] valid before mmcx_clk rising clock edge | 3.4 | | 23.8 | | ns |
| HSSD8 | $t_{h(clkH-dV)}$ | Hold time, mmcx_dat[n:0][1] valid after mmcx_clk rising clock edge | 1.7 | | 1.3 | | ns |

(1) In mmcx_dat[n:0], n is equal to 3 for mmc2 and 7 for mmc3.

(2) See Section 4.3.4, *Processor Clocks*.

**Table 6-129. MMC2 and MMC3 Interfaces Switching Characteristics—High-Speed SDIO Mode[2] [5]**

| NO. | PARAMETER | | OPP100 | | OPP50 | | UNIT |
|-----|-----------|-----------|-----|-----|-----|-----|------|
| | | | MIN | MAX | MIN | MAX | |
| HSSD1 | $t_{c(clk)}$ | Frequency[1], output mmcx_clk period | | 48 | | 24 | MHz |
| HSSD2 | $t_{W(clkH)}$ | Typical pulse duration, output mmcx_clk high | 0.5*P[3] | | 0.5*P[3] | | ns |
| HSSD2 | $t_{W(clkL)}$ | Typical pulse duration, output mmcx_clk low | 0.5*P[3] | | 0.5*P[3] | | ns |
| | $t_{dc(clk)}$ | Duty cycle error, output mmcx_clk | −1042 | 1042 | −2083 | 2083 | ps |
| | $t_{J(clk)}$ | Jitter standard deviation[4], output mmcx_clk | −65 | 65 | −65 | 65 | ps |
| HSSD5 | $t_{d(clkL-doV)}$ | Delay time, mmcx_clk rising clock edge to mmcx_cmd transition | 2.6 | 13.8 | 3 | 34.3 | ns |
| HSSD6 | $t_{d(clkL-doV)}$ | Delay time, mmcx_clk rising clock edge to mmcx_dat[n:0][2] transition | 2.6 | 13.8 | 3 | 34.3 | ns |

(1) Related with the output mmcx_clk maximum and minimum frequency.

(2) In mmcx, x = 2 or 3. In mmcx_dat[n:0], n is equal to 3 for mmc2 and 7 for mmc3.

(3) P = output mmcx_clk period in ns.

(4) The jitter probability density can be approximated by a Gaussian function.

(5) See Section 4.3.4, *Processor Clocks*.



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**Figure 6-73. MMC2 and MMC3 Interfaces—High-Speed SDIO Mode—Data/Command Receive[1]**

(1) In mmcx, x = 2 or 3. In mmcx_dat[n:0], n is equal to 3 for mmc2 and 7 for mmc3.
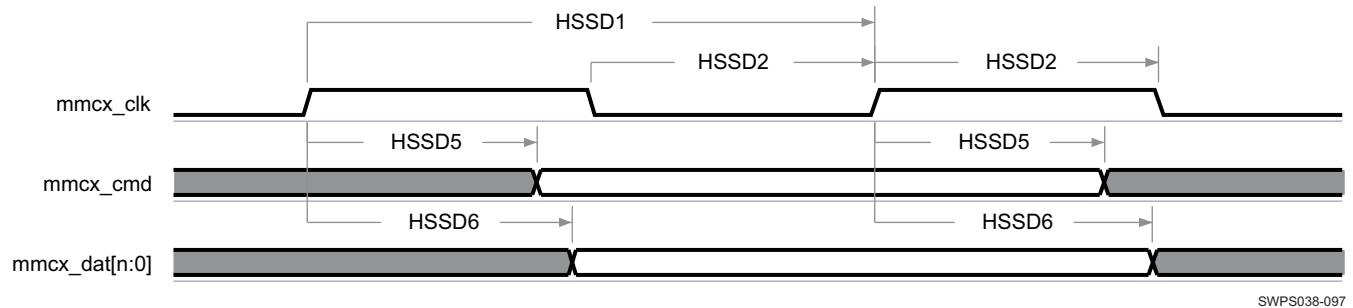
SWPS038-097

**Figure 6-74. MMC2 and MMC3 Interfaces—High-Speed SDIO Mode—Data/Command Transmit[1]**

(1) In mmcx, x = 2 or 3. In mmcx_dat[n:0], n is equal to 3 for mmc2 and 7 for mmc3.

### 6.6.8.1.8 MMC2 and MMC3 Interfaces—Standard SDIO Mode

Table 6-131 and Table 6-132 assume testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 5-89 and Figure 5-90).

**Table 6-130. MMC2 and MMC3 Interfaces Timing Conditions—Standard SDIO Mode**

| TIMING CONDITION PARAMETER | | VALUE | UNIT |
|---|---|---|---|
| **Input Conditions** | | | |
| $t_R$ | Input signal rise time | 10 | ns |
| $t_F$ | Input signal fall time | 10 | ns |
| **Output Condition** | | | |
| $C_{LOAD}$ | Output load capacitance[1] | 5 | pF |

(1) Buffer strength configuration: SPEEDCTRL = 1

**Table 6-131. MMC2 and MMC3 Interfaces Timing Requirements—Standard SDIO Mode[2][3]**

| NO. | PARAMETER | | OPP100 | | OPP50 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| **MMC2 and MMC3 Interface (1.8-V IO)** | | | | | | | |
| SD3 | $t_{su(CMDV\text{-}CLKIH)}$ | Setup time, mmcx_cmd valid before mmcx_clk rising clock edge | 3.3 | | 21.9 | | ns |
| SD4 | $t_{h(CLKIH\text{-}CMDIV)}$ | Hold time, mmcx_cmd valid after mmcx_clk rising clock edge | 18.1 | | 36.7 | | ns |
| SD7 | $t_{su(DATxV\text{-}CLKIH)}$ | Setup time, mmcx_dat[n:0][1] valid before mmcx_clk rising clock edge | 3.3 | | 21.9 | | ns |
| SD8 | $t_{h(CLKIH\text{-}DATxIV)}$ | Hold time, mmcx_dat[n:0][1] valid after mmcx_clk rising clock edge | 18.1 | | 36.7 | | ns |

(1) In mmcx_dat[n:0], n is equal to 3 for MMC2 and 7 for MMC3.

(2) See Section 4.3.4, *Processor Clocks.*

(3) In mmcx, x is equal to 2 or 3.

**Table 6-132. MMC2 and MMC3 Interfaces Switching Characteristics—Standard SDIO Mode[6][7]**

| NO. | PARAMETER | | OPP100 | | OPP50 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| **Standard SDIO Mode** | | | | | | | |
| SD1 | $t_{c(clk)}$ | Frequency[1], output clock period | | 24 | | 12 | MHz |
| SD2 | $t_{W(clkH)}$ | Typical pulse duration, output clock high | X[4] * PO[2] | | X[4] * PO[2] | | ns |
| SD2 | $t_{W(clkL)}$ | Typical pulse duration, output clock low | Y[5] * PO[2] | | Y[5] * PO[2] | | ns |
| | $t_{dc(clk)}$ | Duty cycle error, output clock | | 2083.33 | | 4166.67 | ps |

## Table 6-132. MMC2 and MMC3 Interfaces Switching Characteristics—Standard SDIO Mode[6][7] (continued)

| NO. | | PARAMETER | OPP100 | | OPP50 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| | $t_{J(clk)}$ | Jitter standard deviation[3], output clock | | 200 | | 200 | ps |
| | $t_{R(clk)}$ | Rise time, output clock | | 10 | | 10 | ns |
| | $t_{F(clk)}$ | Fall time, output clock | | 10 | | 10 | ns |
| | $t_{R(data)}$ | Rise time, output data | | 10 | | 10 | ns |
| | $t_{F(data)}$ | Fall time, output data | | 10 | | 10 | ns |
| SD5 | $t_{d(CLKOH-CMD)}$ | Delay time, mmcx_clk rising clock edge to mmcx_cmd transition | 6.13 | 35.53 | 6.3 | 77.03 | ns |
| SD6 | $t_{d(CLKOH-DATx)}$ | Delay time, mmcx_clk rising clock edge to mmcx_dat[n:0][6] transition | 6.13 | 35.53 | 6.3 | 77.03 | ns |

(1) Related to the output mmcx_clk maximum and minimum frequency.

(2) P = output mmcx_clk period in ns

(3) The jitter probability density can be approximated by a Gaussian function.

(4) The X parameter is defined as follows:

| CLKD | X |
|---|---|
| 1 or Even | 0.5 |
| Odd | (trunk[CLKD/2]+1)/CLKD |

All required details about clock division factor CLKD can be found in the *AM/DM37x Multimedia Device Technical Reference Manual* (literature number SPRUGN4).

(5) The Y parameter is defined as follows:

| CLKD | Y |
|---|---|
| 1 or Even | 0.5 |
| Odd | (trunk[CLKD/2])/CLKD |

All required details about clock division factor CLKD can be found in the *AM/DM37x Multimedia Device Technical Reference Manual* (literature number SPRUGN4).

(6) In mmcx, x is equal to 2 or 3. In mmcx_dat[n :0] is equal to 3 for mmc2 and 7 for mmc3.

(7) See Section 4.3.4, *Processor Clocks.*
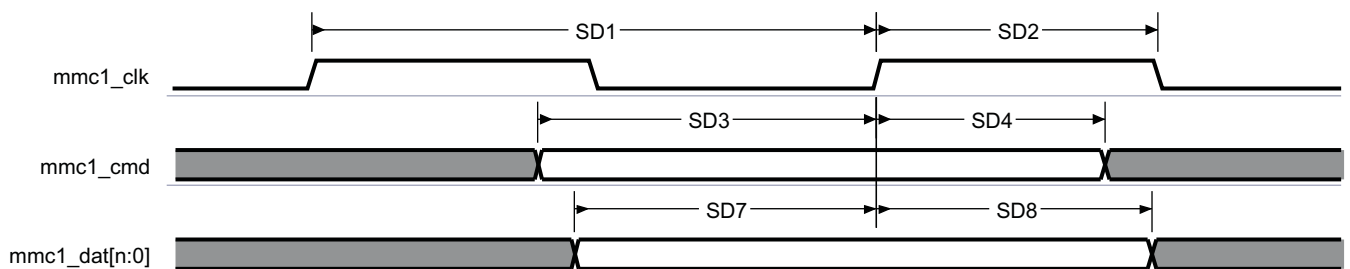


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**Figure 6-75. MMC2 and MMC3 Interfaces—Standard SDIO Mode—Data/Command Receive[1]**

(1) In mmcx, x is equal to 2 or 3. In mmcx_dat[n:0] is equal to 3 for MMC2 and 7 for MMC3.
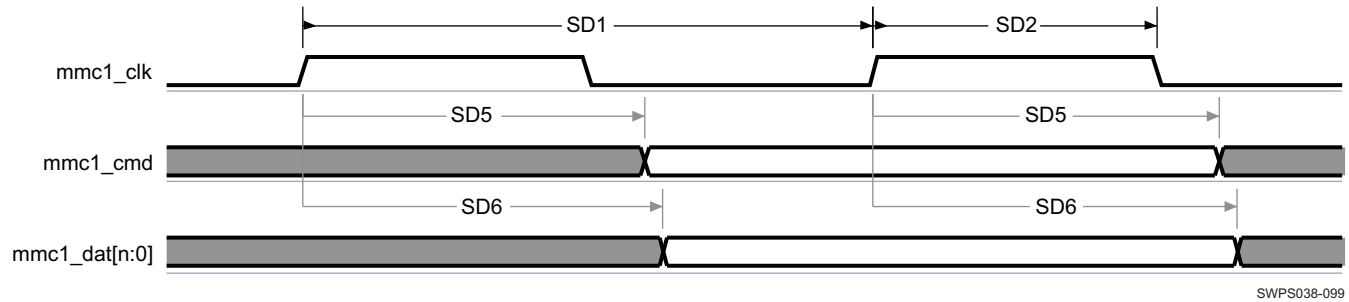
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**Figure 6-76. MMC2 and MMC3 Interfaces—Standard SDIO Mode—Data/Command Transmit[1]**

(1) In mmcx, x is equal to 2 or 3. In mmcx_dat[n:0] is equal to 3 for MMC2 and 7 for MMC3.

### 6.6.8.1.9 MMC2 and MMC3 Interfaces—Embedded Media Interface (eMMC)—High-Speed JC64 Mode

Table 6-134 and Table 6-135 assume testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-77 through Figure 6-78).

**Table 6-133. MMC2 and MMC3 Interfaces Timing Conditions—High-Speed JC64 Mode**

| TIMING CONDITION PARAMETER | | VALUE | | UNIT |
|---|---|---|---|---|
| | | MIN | MAX | |
| **Input Conditions** | | | | |
| $t_R$ | Input signal rise time | 0.38 | 3.82 | ns |
| $t_F$ | Input signal fall time | 0.39 | 3.68 | ns |
| **Output Condition** | | | | |
| $C_{LOAD}$ | Output load capacitance[1] | 14 | | pF |

(1) Buffer strength configuration for MMC3: LB0 = 1.

**Table 6-134. MMC2 and MMC3 Interfaces Timing Requirements—High-Speed JC64 Mode[1]**

| NO. | | PARAMETER | OPP100 | | OPP50 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| MMC3 | $t_{su(cmdV-clkH)}$ | Setup time, input command mmcx_cmd valid before output clock mmcx_clk rising edge | 5.1 | | 25.5 | | ns |
| MMC4 | $t_{h(clkH-cmdIV)}$ | Hold time, input command mmcx_cmd valid after output clock mmcx_clk rising edge | 1.3 | | 0.9 | | ns |
| MMC7 | $t_{su(dV-clkH)}$ | Setup time, input data mmcx_dat[n:0] valid before output clock mmcx_clk rising edge | 5.1 | | 25.5 | | ns |
| MMC8 | $t_{h(clkH-dIV)}$ | Hold time, input data mmcx_dat[n:0] valid after output clock mmcx_clk rising edge | 1.3 | | 0.9 | | ns |

(1) In mmx_dat[n:0], x is equal to 2 or 3 and n is equal to 7.

(2) In mmx_cmd, x is equal to 2 or 3.

(3) In mmx_clk, x is equal to 2 or 3.

**Table 6-135. MMC2 and MMC3 Interfaces Switching Characteristics—High-Speed JC64 Mode[5] [6][7]**

| NO. | | PARAMETER | OPP100 | | OPP50 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| MMC1 | $1/t_{c(clk)}$ | Frequency[1], output mmcx_clk period | | 48 | | 24 | MHz |
| MMC2 | $t_{W(clkH)}$ | Typical pulse duration, output mmcx_clk high | 0.5*P[2] | | 0.5*P[2] | | ns |
| MMC2 | $t_{W(clkL)}$ | Typical pulse duration, output mmcx_clk low | 0.5*P[2] | | 0.5*P[2] | | ns |
| | $t_{dc(clk)}$ | Duty cycle error, output mmcx_clk | −1042 | 1042 | −2083 | 2083 | ps |
| | $t_{J(clk)}$ | Jitter standard deviation[3], output mmcx_clk | −65 | 65 | −65 | 65 | ps |
| | $t_{R(clk)}$ | Rising time, output mmcx_clk | | 2263 | | 2263 | ps |
| | $t_{F(clk)}$ | Falling time, output mmcx_clk | | 2136 | | 2136 | ps |

### Table 6-135. MMC2 and MMC3 Interfaces Switching Characteristics—High-Speed JC64 Mode[5] [6][7] (continued)

| NO. | PARAMETER | | OPP100 | | OPP50 | | UNIT |
|-----|-----------|---|-----|-----|-----|-----|------|
| | | | MIN | MAX | MIN | MAX | |
| MMC5 | $t_{d(clkL-doV)}$ | Delay time, mmcx_clk rising clock edge to mmcx_cmd transition | 3.6 | 16.8 | 4 | 37.2 | ns |
| | $t_{R(do)}$ | Rising time, output mmcx_cmd | | 2263 | | 2263 | ps |
| | $t_{F(do)}$ | Falling time, output mmcx_cmd | | 2136 | | 2136 | ps |
| MMC6 | $t_{d(clkL-doV)}$ | Delay time, mmcx_clk rising clock edge to mmcx_daty transition | 3.6 | 16.8 | 4 | 37.2 | ns |
| | $t_{R(do)}$ | Rising time, output mmcx_dat[n:0][4] | | 2263 | | 2263 | ps |
| | $t_{F(do)}$ | Falling time, output mmcx_dat[n:0][4] | | 2136 | | 2136 | ps |

(1)  Related with the output clock maximum and minimum frequencies programmable in MMC module.

(2)  PO = output clock period in ns

(3)  The jitter probability density can be approximated by a Gaussian function.

(4)  In mmx_dat[n:0], x is equal to 2 or 3 and n is equal to 7.

(5)  See Section 4.3.4, Processor Clocks.

(6)  In mmx_cmd, x is equal to 2 or 3.

(7)  In mmx_clk, x is equal to 2 or 3.
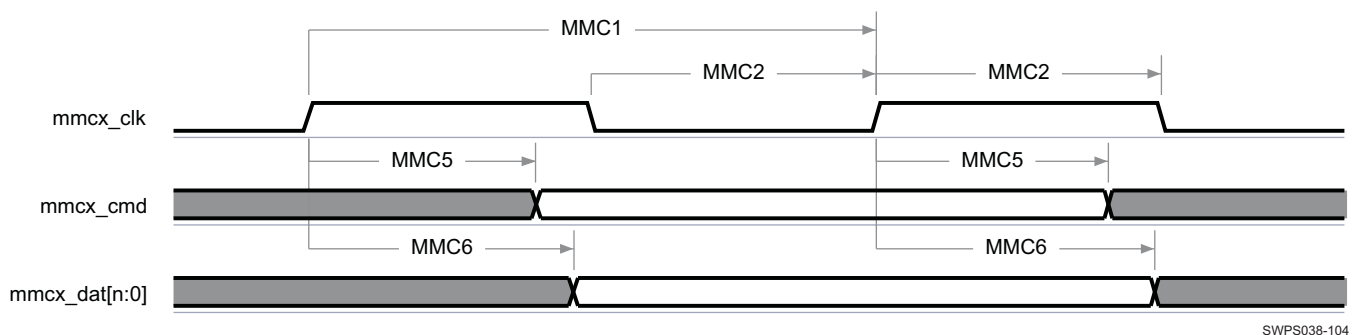


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**Figure 6-77. MMC2 and MMC3 Interfaces—High-Speed JC64 Transmiter Mode[1][2][3]**

(1)  In mmx_dat[n:0], x is equal to 2 or 3 and n is equal to 7.

(2)  In mmx_cmd, x is equal to 2 or 3.

(3)  In mmx_clk, x is equal to 2 or 3.
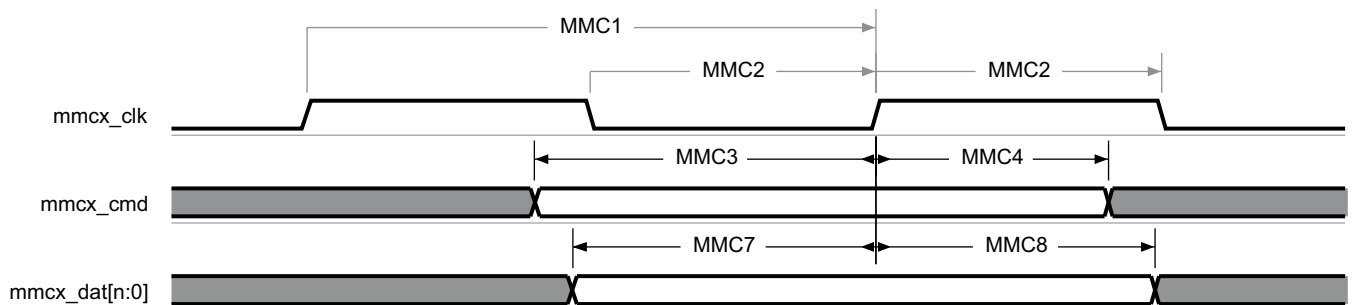


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**Figure 6-78. MMC2 and MMC3 Interfaces—High-Speed JC64 Receiver Mode[1][2][3]**

(1)  In mmx_dat[n:0], x is equal to 2 or 3 and n is equal to 7.

(2)  In mmx_cmd, x is equal to 2 or 3.

(3)  In mmx_clk, x is equal to 2 or 3.

### 6.6.9 Test Interfaces

#### 6.6.9.1 Embedded Trace Macro Interface (ETM)

Table 6-137 assumes testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-79).

**Table 6-136. ETM Timing Conditions—Transmit Mode**

| TIMING CONDITION PARAMETER | | VALUE | | UNIT |
|---|---|---|---|---|
| | | MIN | MAX | |
| **Output Condition** | | | | |
| $C_{LOAD}$ | Output load capacitance[1] | | 10 | pF |

(1) Buffer strength configuration: LB0 = 1.

**Table 6-137. ETM Switching Characteristics—Transmit Mode[4]**

| NO. | PARAMETER | | OPP100 | | OPP50 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| TPIU1 | $1/t_{c(clk)}$ | Frequency[3], output clock etk_clk | | 166 | | 166 | MHz |
| TPIU2 | $t_{w(clkH)}$ | Pulse duration, output clock etk_clk high | 0.5P[1] | | 0.5P[1] | | ns |
| TPIU3 | $t_{w(clkL)}$ | Pulse duration, output clock etk_clk low | 0.5P[1] | | 0.5P[1] | | ns |
| | $t_{dc(clk)}$ | Duty cycle error, output clock etk_clk | −301 | 301 | −301 | 301 | ps |
| | $t_{J(clk)}$ | Jitter standard deviation[2], output clock etk_clk | | 65 | | 65 | ps |
| | $t_{R(clk)}$ | Rise time, output clock etk_clk | | 1.2 | | 1.2 | ns |
| | $t_{F(clk)}$ | Fall time, output clock etk_clk | | 1.2 | | 1.2 | ns |
| TPIU4 | $t_{d(clk-ctl)}$ | Delay time, output clock etk_clk low/high to output control etk_ctl transition | | 0.839 | | 0.839 | ns |
| TPIU5 | $t_{d(clkH-d)}$ | Delay time, output clock etk_clk low/high to output data etk_d[15:0] transition | | 0.839 | | 0.839 | ns |
| | $t_{R(d/ctl)}$ | Rise time, output data etk_d[15:0] and output control etk_ctl | | 1.2 | | 1.2 | ns |
| | $t_{F(d/ctl)}$ | Fall time, output data etk_d[15:0] and output control etk_ctl | | 1.2 | | 1.2 | ns |

(1) P = etk_clk period in ns

(2) The jitter probability density can be approximated by a Gaussian function.

(3) Related with the etm_clk maximum frequency.

(4) See Section 4.3.4, *Processor Clocks*.
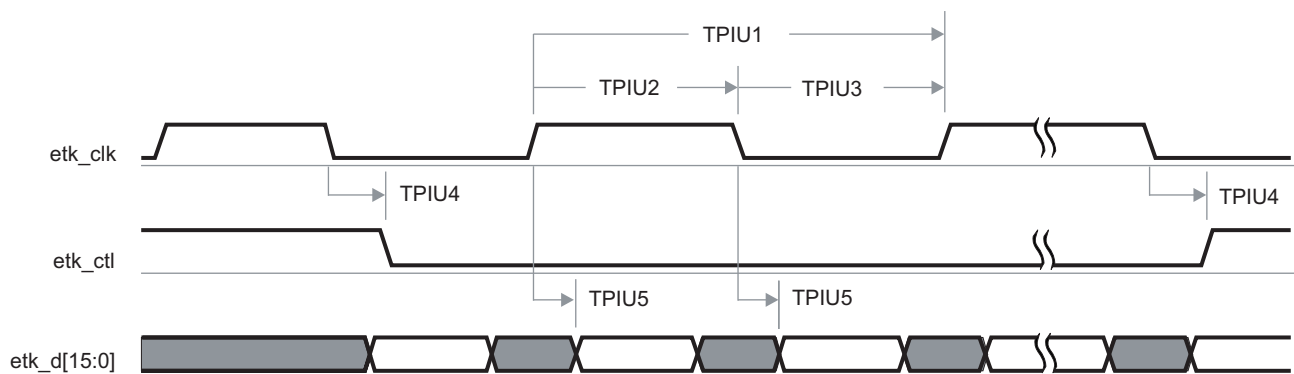


**Figure 6-79. ETM—Transmit Mode**

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Product Folder Link(s): DM3730  DM3725

### 6.6.9.2 System Debug Trace Interface (SDTI)

The System Debug Trace Interface (SDTI) module provides real-time software tracing functionality to the device. The trace interface has four trace data pins and a trace clock pin.

This interface is a dual-edge interface:

- The data are available on rising and falling edge of sdti_clk.
- But can be also configured in single-edge mode where data are available on the falling edge of sdti_clk.

Serial interface operates in clock stop regime: serial clock is not free-running; when there is no trace data, there is no trace clock.

#### 6.6.9.2.1 SDTI—Dual-Edge Mode

Table 6-139 assumes testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-80).

**Table 6-138. SDTI Timing Conditions—Dual-Edge Mode**

| TIMING CONDITION PARAMETER | | VALUE | UNIT |
|---|---|---|---|
| **Output Condition** | | | |
| $C_{LOAD}$ | Output load capacitance[1] | 25 | pF |

(1) Buffer strength configuration: LB0 = 1.

**Table 6-139. SDTI Switching Characteristics—Dual-Edge Mode[2]**

| NO. | PARAMETER | | OPP100 | | OPP50 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| SD1 | $1 / t_{c(clk)}$ | Frequency, output clock sdti_clk | | 34.5 | | 34.5 | MHz |
| SD2 | $t_{w(clk)}$ | Pulse duration, output clock sdti_clk high or low | $0.5P^{(1)} - 1.2$ | $0.5P^{(1)} + 1.2$ | $0.5P^{(1)} - 1.2$ | $0.5P^{(1)} + 1.2$ | ns |
| SD3 | $t_{d(clk-txd)}$ | Delay time, output clock sdti_clk transition to output data sdti_txd[3:0] transition | Multiplexing mode on etk pins | 2.3 | 10.9 | 2.3 | 10.9 | ns |
| | | | Multiplexing mode on jtag_emu pins | 2.3 | 13.9 | 2.3 | 13.9 | |

(1) P = sdti_clk clock period in ns

(2) See Section 4.3.4, *Processor Clocks.*
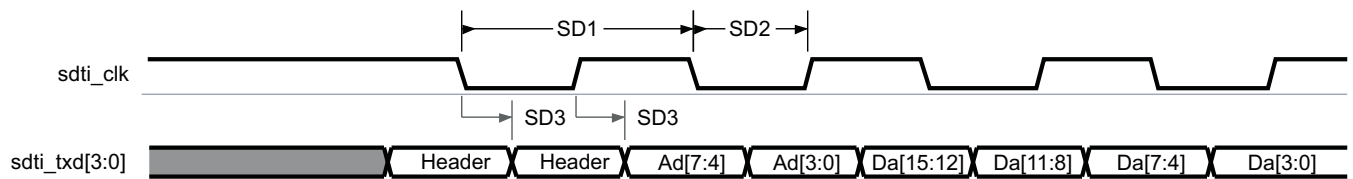


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**Figure 6-80. SDTI—Dual-Edge Mode**

### 6.6.9.2.2 SDTI—Single-Edge Mode

Table 6-141 assumes testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-81).

**Table 6-140. SDTI Timing Conditions—Single-Edge Mode**

| TIMING CONDITION PARAMETER | | VALUE | UNIT |
|---|---|---|---|
| **Output Condition** | | | |
| $C_{LOAD}$ | Output load capacitance[1] | 25 | pF |

(1) Buffer strength configuration: LB0 = 1.

**Table 6-141. SDTI Switching Characteristics—Single-Edge Mode[2]**

| NO. | PARAMETER | | OPP100 | | OPP50 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| SD1 | $1 / t_{c(clk)}$ | Frequency, output clock sdti_clk | | 34.5 | | 34.5 | MHz |
| SD2 | $t_{w(clk)}$ | Pulse duration, output clock sdti_clk high or low | 0.5P[1] – 1.2 | 0.5P[1] + 1.2 | 0.5P[1] – 1.2 | 0.5P[1] + 1.2 | ns |
| SD3 | $t_{d(clk\text{-}txd)}$ | Delay time, output clock sdti_clk transition to output data sdti_txd[3:0] transition | Multiplexing mode on etk pins | 2.3 | 26.5 | 2.3 | 26.5 | ns |
| | | | Multiplexing mode on jtag_emu pins | 2.3 | 33.2 | 2.3 | 33.2 | |

(1) P = sdti_clk clock period in ns

(2) See Section 4.3.4, *Processor Clocks.*



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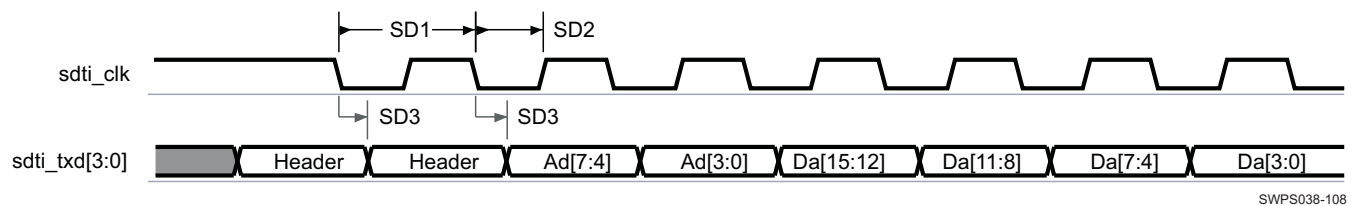
**Figure 6-81. SDTI—Single-Edge Mode**

### 6.6.9.3 JTAG Interface (JTAG)

The JTAG TAP controller handles standard IEEE JTAG interfaces. The following section defines the timing requirements for several tools used to test the device as:

- Free-running clock tool, like XDS560 and XDS510 tools
- Adaptive clock tool, like RealView® ICE tool and Lauterbach™ tool

### 6.6.9.3.1 JTAG—Free-Running Clock Mode

Table 6-143 and Table 6-144 assume testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-82).

**Table 6-142. JTAG Timing Conditions—Free-Running Clock Mode**

| TIMING CONDITION PARAMETER | | VALUE | UNIT |
|---|---|---|---|
| **Input Conditions** | | | |
| $t_R$ | Input signal rise time | 5 | ns |
| $t_F$ | Input signal fall time | 5 | ns |
| **Output Condition** | | | |
| $C_{LOAD}$ | Output load capacitance | 30 | pF |

Submit Documentation Feedback

Product Folder Link(s): DM3730  DM3725

### Table 6-143. JTAG Timing Requirements—Free-Running Clock Mode[5] [6]

| NO. | PARAMETER | | OPP100 | | OPP50 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| JT4 | $1 / t_{c(tck)}$ | Frequency[1], input clock jtag_tck | | 50 | | 50 | MHz |
| JT5 | $t_{w(tckL)}$ | Pulse duration, input clock jtag_tck low | 0.5P[2] | | 0.5P[2] | | ns |
| JT6 | $t_{w(tckH)}$ | Pulse duration, input clock jtag_tck high | 0.5P[2] | | 0.5P[2] | | ns |
| | $t_{dc(tck)}$ | Duty cycle error, input clock jtag_tck | −1250 | 1250 | −1667 | 1667 | ps |
| | $t_{J(tck)}$ | Cycle jitter[3], input clock jtag_tck | −1250 | 1250 | −1667 | 1667 | ps |
| JT7 | $t_{su(tdiV-rtckH)}$ | Setup time, input data jtag_tdi valid before output clock jtag_rtck high | 1.6 | | 1.6 | | ns |
| JT8 | $t_{h(tdiV-rtckH)}$ | Hold time, input data jtag_tdi valid after output clock jtag_rtck high | 0.7 | | 1.0 | | ns |
| JT9 | $t_{su(tmsV-rtckH)}$ | Setup time, input mode select jtag_tms_tmsc valid before output clock jtag_rtck high | 1.6 | | 1.6 | | ns |
| JT10 | $t_{h(tmsV-rtckH)}$ | Hold time, input mode select jtag_tms_tmsc valid after output clock jtag_rtck high | 0.7 | | 1.0 | | ns |
| JT12 | $t_{su(emuxV-rtckH)}$ | Setup time, input emulation jtag_emux[4] valid before output clock jtag_rtck high | 14.4 | | 19.6 | | ns |
| JT13 | $t_{h(emuxV-rtckH)}$ | Hold time, input emulation jtag_emux[4] valid after output clock jtag_rtck high | 2.0 | | 2.7 | | ns |

(1)  Related with the input maximum frequency supported by the JTAG module.

(2)  P = input clock jtag _tck period in ns

(3)  Maximum cycle jitter supported by input clock jtag _tck.

(4)  In jtag_emux, x is equal to 0 or 1.

(5)  The timing requirements are assured for the cycle jitter and duty cycle error conditions specified.

(6)  See Section 4.3.4, *Processor Clocks*.

### Table 6-144. JTAG Switching Characteristics—Free-Running Clock Mode[5]

| NO. | PARAMETER | | OPP100 | | OPP50 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| JT1 | $1 / t_{c(rtck)}$ | Frequency[1], output clock jtag_rtck | | 50 | | 50 | MHz |
| JT2 | $t_{w(rtckL)}$ | Pulse duration, output clock jtag_rtck low | 0.5P[2] | | 0.5P[2] | | ns |
| JT3 | $t_{w(rtckH)}$ | Pulse duration, output clock jtag_rtck high | 0.5P[2] | | 0.5P[2] | | ns |
| | $t_{dc(rtck)}$ | Duty cycle error, output clock jtag_rtck | −1250 | 1250 | −1667 | 1667 | ps |
| | $t_{J(rtck)}$ | Jitter standard deviation[3], output clock jtag_rtck | | 33.3 | | 33.3 | ps |
| | $t_{R(rtck)}$ | Rise time, output clock jtag_rtck | | 0 | | 0 | ns |
| | $t_{F(rtck)}$ | Fall time, output clock jtag_rtck | | 0 | | 0 | ns |
| JT11 | $t_{d(rtckL-tdoV)}$ | Delay time, output clock jtag_rtck low to output data jtag_tdo valid | −5.8 | 5.8 | −7.9 | 7.9 | ns |
| | $t_{R(tdo)}$ | Rise time, output data jtag_tdo | | 0 | | 0 | ns |
| | $t_{F(tdo)}$ | Fall time, output data jtag_tdo | | 0 | | 0 | ns |
| JT14 | $t_{d(rtckH-emuxV)}$ | Delay time, output clock jtag_rtck high to output emulation ,jtag_emux[4] valid | 2.7 | 15.1 | 2.7 | 20.4 | ns |

(1)  Related with the jtag_rtck maximum frequency.

(2)  P = output clock jtag _rtck period in ns

(3)  The jitter probability density can be approximated by a Gaussian function.

(4)  In jtag_emux, x is equal to 0 or 1.

(5)  See Section 4.3.4, *Processor Clocks*.
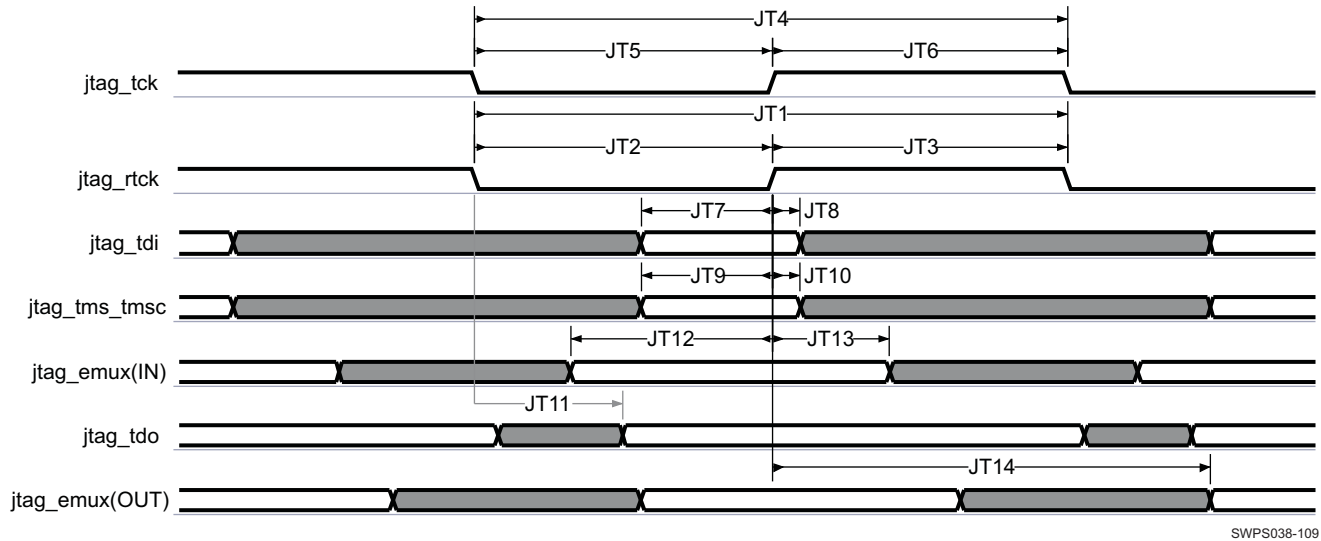
SWPS038-109

(1)  In jtag_emux, x is equal to 0 or 1.

**Figure 6-82. JTAG—Free-Running Clock Mode**

### 6.6.9.3.2 JTAG—Adaptative Clock Mode

Table 6-146 and Table 6-147 assume testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-83).

**Table 6-145. JTAG Timing Conditions—Adaptative Clock Mode**

| TIMING CONDITION PARAMETER | | VALUE | UNIT |
|---|---|---|---|
| **Input Conditions** | | | |
| $t_R$ | Input signal rise time | 5 | ns |
| $t_F$ | Input signal fall time | 5 | ns |
| **Output Condition** | | | |
| $C_{LOAD}$ | Output load capacitance | 30 | pF |

**Table 6-146. JTAG Timing Requirements—Adaptative Clock Mode[4] [5]**

| NO. | PARAMETER | | OPP100 | | OPP50 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| JA4 | $1 / t_{c(tck)}$ | Frequency[1], input clock jtag_tck | | 50 | | 50 | MHz |
| JA5 | $t_{w(tckL)}$ | Pulse duration, input clock jtag_tck low | 0.5P[2] | | 0.5P[2] | | ns |
| JA6 | $t_{w(tckH)}$ | Pulse duration, input clock jtag_tck high | 0.5P[2] | | 0.5P[2] | | ns |
| | $t_{dc(lclk)}$ | Duty cycle error, input clock jtag_tck | −2500 | 2500 | −2500 | 2500 | ps |
| | $t_{J(lclk)}$ | Cycle jitter[3], input clock jtag_tck | −1500 | 1500 | −1500 | 1500 | ps |
| JA7 | $t_{su(tdiV-tckH)}$ | Setup time, input data jtag_tdi valid before input clock jtag_tck high | 13.8 | | 13.8 | | ns |
| JA8 | $t_{h(tdiV-tckH)}$ | Hold time, input data jtag_tdi valid after input clock jtag_tck high | 13.8 | | 13.8 | | ns |
| JA9 | $t_{su(tmsV-tckH)}$ | Setup time, input mode select jtag_tms_tmsc valid before input clock jtag_tck high | 13.8 | | 13.8 | | ns |
| JA10 | $t_{h(tmsV-tckH)}$ | Hold time, input mode select jtag_tms_tmsc valid after input clock jtag_tck high | 13.8 | | 13.8 | | ns |

(1) Related with the input maximum frequency supported by the JTAG module

(2) P = input clock jtag _tck period in ns

(3) Maximum cycle jitter supported by input clock jtag _tck.

(4) The timing requirements are assured for the cycle jitter and duty cycle error conditions specified.

(5) See Section 4.3.4, *Processor Clocks.*

### Table 6-147. JTAG Switching Characteristics—Adaptative Clock Mode[4]

| NO. | PARAMETER | | OPP100 | | OPP50 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| JA1 | $1 / t_{c(rtck)}$ | Frequency[1], output clock jtag_rtck | | 50 | | 50 | MHz |
| JA2 | $t_{w(rtckL)}$ | Pulse duration, output clock jtag_rtck low | 0.5P[2] | | 0.5P[2] | | ns |
| JA3 | $t_{w(rtckH)}$ | Pulse duration, output clock jtag_rtck high | 0.5P[2] | | 0.5P[2] | | ns |
| | $t_{dc(rtck)}$ | Duty cycle error, output clock jtag_rtck | −2500 | 2500 | −2500 | 2500 | ps |
| | $t_{J(rtck)}$ | Jitter standard deviation[3], output clock jtag_rtck | | 33.3 | | 33.3 | ps |
| | $t_{R(rtck)}$ | Rise time, output clock jtag_rtck | | 0 | | 0 | ns |
| | $t_{F(rtck)}$ | Fall time, output clock jtag_rtck | | 0 | | 0 | ns |
| JA11 | $t_{d(rtckL-tdoV)}$ | Delay time, output clock jtag_rtck low to output data jtag_tdo valid | −14.6 | 14.6 | −14.6 | 14.6 | ns |

(1) Related to the jtag _rtck maximum frequency programmable.

(2) P = output clock jtag _rtck period in ns

(3) The jitter probability density can be approximated by a Gaussian function.

(4) See Section 4.3.4, *Processor Clocks.*
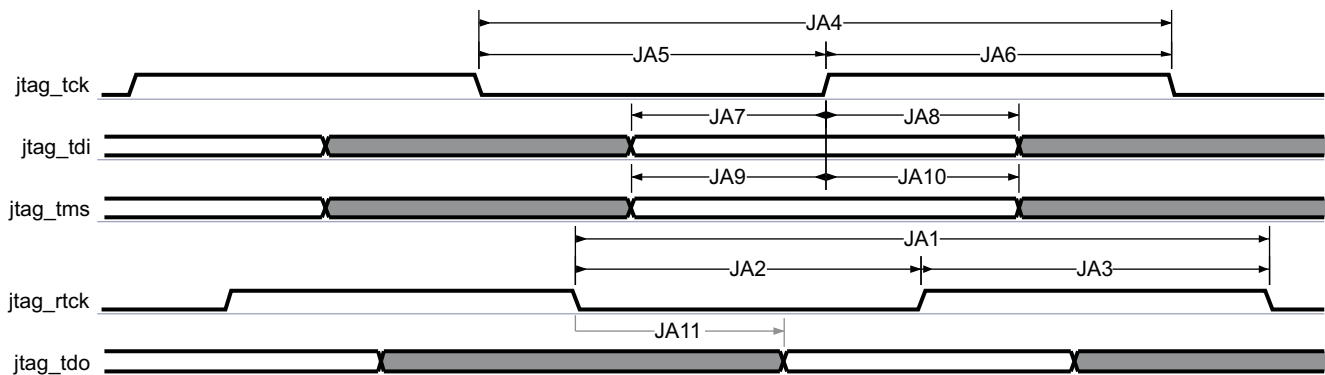


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**Figure 6-83. JTAG—Adaptative Clock Mode**

# 7 Package Characteristics

## 7.1 Package Thermal Characteristics

Table 7-1 and Table 7-2 provide the thermal resistance characteristics for the packages used on this device.

Note: This table provides simulation data and may not represent actual use-case values.

#### Table 7-1. Thermal Resistance Characteristics 800MHz ARM Operation-4Gb DDR + Flash

| PACKAGE | Power (W)[5] | $\theta_{JA}$(°C/W)[2] | $\theta_{JB}$(°C/W)[3] | $\theta_{JC}$(°C/W)[4] | BOARD TYPE |
|---|---|---|---|---|---|
| CBP Package | 1.42 | 20.06 | 6.44 | [6] | 2S2P[1] |
| CBC Package | 1.42 | 19.97 | 7.76 | [6] | 2S2P[1] |
| CUS Package | 1.05 | 24.75 | 11.06 | 7.06 | 2S2P[1] |

(1) The board types are defined by JEDEC (reference JEDEC standard JESD51-9, Test Board for Array Surface Mount Package Thermal Measurements).

(2) $\theta_{JA}$ (Theta-JA) = Thermal Resistance Junction-to-Ambient, °C/W

(3) $\theta_{JB}$ (Theta-JB) = Thermal Resistance Junction-to-Board, °C/W

(4) $\theta_{JC}$ (Theta-JC) = Thermal Resistance Junction-to-Board, °C/W

(5) These power numbers are based on simulation results for DM37x. Power numbers for CBP and CBC packages include the DM37x device and POP memory. CUS package is DM37x only.

(6) Not applicable since these packages have memory package mounted on top.

#### Table 7-2. Thermal Resistance Characteristics 1GHz ARM Operation-8Gb DDR

| PACKAGE | Power (W)[5] | $\theta_{JA}$(°C/W)[2] | $\theta_{JB}$(°C/W)[3] | $\theta_{JC}$(°C/W)[4] | BOARD TYPE |
|---|---|---|---|---|---|
| CBP Package | 2.06 | 19.51 | 6.19 | [6] | 2S2P[1] |
| CBC Package | 2.06 | 20.11 | 8.01 | [6] | 2S2P[1] |
| CUS Package | 1.4 | 24.75 | 11.06 | 7.06 | 2S2P[1] |

(1) The board types are defined by JEDEC (reference JEDEC standard JESD51-9, Test Board for Array Surface Mount Package Thermal Measurements).

(2) $\theta_{JA}$ (Theta-JA) = Thermal Resistance Junction-to-Ambient, °C/W

(3) $\theta_{JB}$ (Theta-JB) = Thermal Resistance Junction-to-Board, °C/W

(4) $\theta_{JC}$ (Theta-JC) = Thermal Resistance Junction-to-Board, °C/W

(5) These power numbers are based on simulation results for DM37x. Power numbers for CBP and CBC packages include the DM37x device and POP memory. CUS package is DM37x only.

(6) Not applicable since these packages have memory package mounted on top.

## 7.2 Device Support

### 7.2.1 Device and Development-Support Tool Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all DM37x processors and support tools. Each device has one of three prefixes: X, P, or null (no prefix). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMDX) through fully qualified production devices/tools (TMDS).

Device development evolutionary flow:

**X**        Experimental device that is not necessarily representative of the final devices electrical specifications and may not use production assembly flow. (TMX definition)

**P**        Prototype device that is not necessarily the final silicon die and may not necessarily meet final electrical specifications. (TMP definition)

**null**      Production version of the silicon die that is fully qualified. (TMS definition)

Support tool development evolutionary flow:

**TMDX**   Development support product that has not yet completed Texas Instruments internal qualification testing.

**TMDS**   Fully qualified development support product.

TMX and TMP devices and TMDX development-support tools are shipped against the following disclaimer:

Developmental product is intended for internal evaluation purposes.

Production devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TIs standard warranty applies.

Predictions show that prototype devices (X or P), have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

For additional description of the device nomenclature markings, see the *Processor Silicon Errata*.
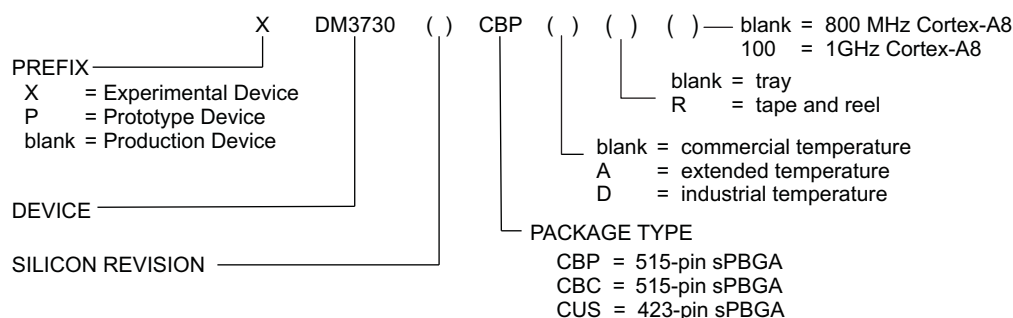


**Figure 7-1. Device Nomenclature**

## 7.2.2 *Documentation Support*

### 7.2.2.1 **Related Documentation from Texas Instruments**

The following documents describe the DM3730/25 Digital Media Processor. Copies of these documents are available on the Internet at www.ti.com. Tip: Enter the literature number in the search box provided at www.ti.com.

The current documentation that describes the DM3730/25 Digital Media Processor, related peripherals, and other technical collateral, is available in the product folder at: www.ti.com.

**SPRUGN4** . Collection of documents providing detailed information on the Sitara™ architecture including power, reset, and clock control, interrupts, memory map, and switch fabric interconnect. Detailed information on the microprocessor unit (MPU) subsystem as well a functional description of the peripherals supported on DM3730/25devices is also included.

#### 7.2.2.1.1 *Community Resources*

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E Community** *TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**TI Embedded Processors Wiki** *Texas Instruments Embedded Processors Wiki.* Established to help developers get started with Embedded Processors from Texas Instruments and to foster innovation and growth of general knowledge about the hardware and software surrounding these devices.

### 7.2.2.2 Related Documentation from Other Sources

The following documents are related to the DM3730, DM3725 Digital Media Processors. Copies of these documents can be obtained directly from the internet or from your Texas Instruments representative.

*Cortex-A8 Technical Reference Manual*. This is the technical reference manual for the Cortex-A8 processor. A copy of this document can be obtained via the internet at http://infocenter.arm.com. Please see the *DM3730, DM3725 Digital Media Processors Silicon Errata* (literature number SPRZ319) to determine the revision of the Cortex-A8 core used on your device.

*ARM Core Cortex^TM-A8 (AT400/AT401) Errata Notice.* Provides a list of advisories for the different revisions of the Cortex-A8 processor. Contact your TI representative for a copy of this document. Please see the *DM3730, DM3725 Digital Media Processors Silicon Errata* (literature number SPRZ319) to determine the revision of the Cortex-A8 core used on your device.

## 7.3 Mechanical Data

![Texas Instruments logo]

7-Feb-2012

## PACKAGING INFORMATION

| Orderable Device | Status [1] | Package Type | Package Drawing | Pins | Package Qty | Eco Plan [2] | Lead/ Ball Finish | MSL Peak Temp [3] | Samples (Requires Login) |
|---|---|---|---|---|---|---|---|---|---|
| DM3725CBC | ACTIVE | POP-FCBGA | CBC | 515 | 119 | Green (RoHS & no Sb/Br) | Call TI | Level-3-260C-168 HR | |
| DM3725CBC100 | ACTIVE | POP-FCBGA | CBC | 515 | 119 | Green (RoHS & no Sb/Br) | Call TI | Level-3-260C-168 HR | |
| DM3725CBCA | ACTIVE | POP-FCBGA | CBC | 515 | 1 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | |
| DM3725CBCD100 | ACTIVE | POP-FCBGA | CBC | 515 | 119 | Green (RoHS & no Sb/Br) | Call TI | Level-3-260C-168 HR | |
| DM3725CBP | ACTIVE | POP-FCBGA | CBP | 515 | 1 | Green (RoHS & no Sb/Br) | Call TI | Level-3-260C-168 HR | |
| DM3725CBP100 | ACTIVE | POP-FCBGA | CBP | 515 | 168 | Green (RoHS & no Sb/Br) | Call TI | Level-3-260C-168 HR | |
| DM3725CBPA | ACTIVE | POP-FCBGA | CBP | 515 | 168 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | |
| DM3725CBPD100 | ACTIVE | POP-FCBGA | CBP | 515 | 1 | Green (RoHS & no Sb/Br) | Call TI | Level-3-260C-168 HR | |
| DM3725CUS | ACTIVE | FCBGA | CUS | 423 | 90 | Green (RoHS & no Sb/Br) | Call TI | Level-3-260C-168 HR | |
| DM3725CUS100 | ACTIVE | FCBGA | CUS | 423 | 90 | Green (RoHS & no Sb/Br) | Call TI | Level-3-260C-168 HR | |
| DM3725CUSA | ACTIVE | FCBGA | CUS | 423 | 1 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | |
| DM3725CUSD100 | ACTIVE | FCBGA | CUS | 423 | 90 | Green (RoHS & no Sb/Br) | Call TI | Level-3-260C-168 HR | |
| DM3730CBC | ACTIVE | POP-FCBGA | CBC | 515 | 119 | Green (RoHS & no Sb/Br) | Call TI | Level-3-260C-168 HR | |
| DM3730CBC100 | ACTIVE | POP-FCBGA | CBC | 515 | 119 | Green (RoHS & no Sb/Br) | Call TI | Level-3-260C-168 HR | |
| DM3730CBCA | ACTIVE | POP-FCBGA | CBC | 515 | 1 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | |
| DM3730CBCD100 | ACTIVE | POP-FCBGA | CBC | 515 | 119 | Green (RoHS & no Sb/Br) | Call TI | Level-3-260C-168 HR | |
| DM3730CBP | ACTIVE | POP-FCBGA | CBP | 515 | 1 | Green (RoHS & no Sb/Br) | Call TI | Level-3-260C-168 HR | |

| Orderable Device | Status [1] | Package Type | Package Drawing | Pins | Package Qty | Eco Plan [2] | Lead/ Ball Finish | MSL Peak Temp [3] | Samples (Requires Login) |
|---|---|---|---|---|---|---|---|---|---|
| DM3730CBP100 | ACTIVE | POP-FCBGA | CBP | 515 | 168 | Green (RoHS & no Sb/Br) | Call TI | Level-3-260C-168 HR | |
| DM3730CBPA | ACTIVE | POP-FCBGA | CBP | 515 | 168 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | |
| DM3730CBPD100 | ACTIVE | POP-FCBGA | CBP | 515 | 168 | Green (RoHS & no Sb/Br) | Call TI | Level-3-260C-168 HR | |
| DM3730CUS | ACTIVE | FCBGA | CUS | 423 | 90 | Green (RoHS & no Sb/Br) | Call TI | Level-3-260C-168 HR | |
| DM3730CUS100 | ACTIVE | FCBGA | CUS | 423 | 90 | Green (RoHS & no Sb/Br) | Call TI | Level-3-260C-168 HR | |
| DM3730CUSA | ACTIVE | FCBGA | CUS | 423 | 90 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | |
| DM3730CUSD100 | ACTIVE | FCBGA | CUS | 423 | 1 | Green (RoHS & no Sb/Br) | Call TI | Level-3-260C-168 HR | |
| XDM3730CBP | OBSOLETE | POP-FCBGA | CBP | 515 | | TBD | Call TI | Call TI | |

[1] The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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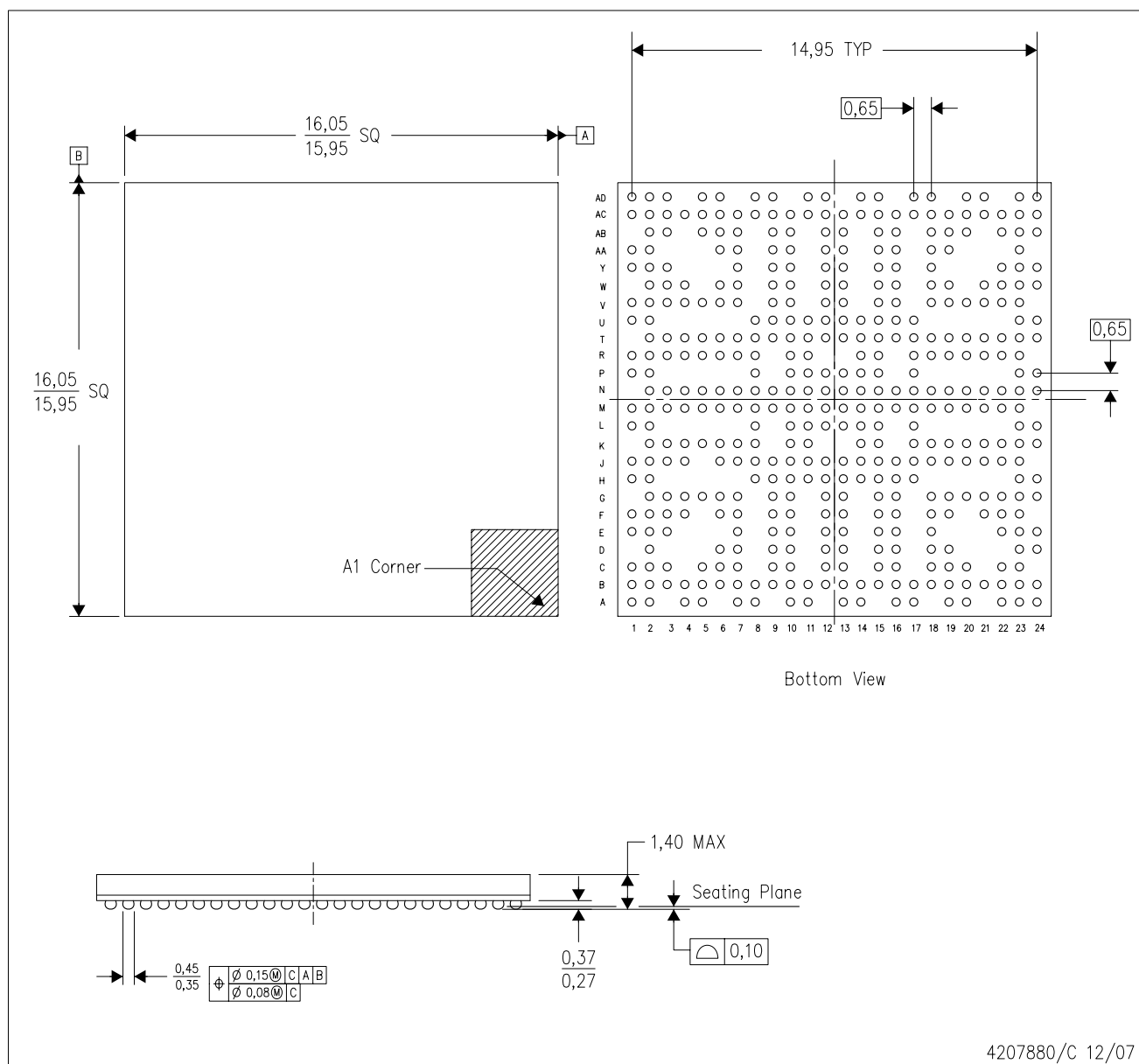
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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

CUS (S−PBGA−N423)                    PLASTIC BALL GRID ARRAY

14,95 TYP

16,05 / 15,95 SQ

16,05 / 15,95 SQ

0,65

0,65

A1 Corner

Bottom View

1,40 MAX

Seating Plane

0,37 / 0,27

0,10

0,45 / 0,35   ⌖ | Ø 0,15 Ⓜ | C | A | B |
              Ø 0,08 Ⓜ | C

4207880/C 12/07

NOTES:    A.    All linear dimensions are in millimeters.
          B.    This drawing is subject to change without notice.
          C.    Flip chip application only.
          D.    Lead−free die bump and solder ball.

CBC (S-PBGA-N515)                    PLASTIC BALL GRID ARRAY
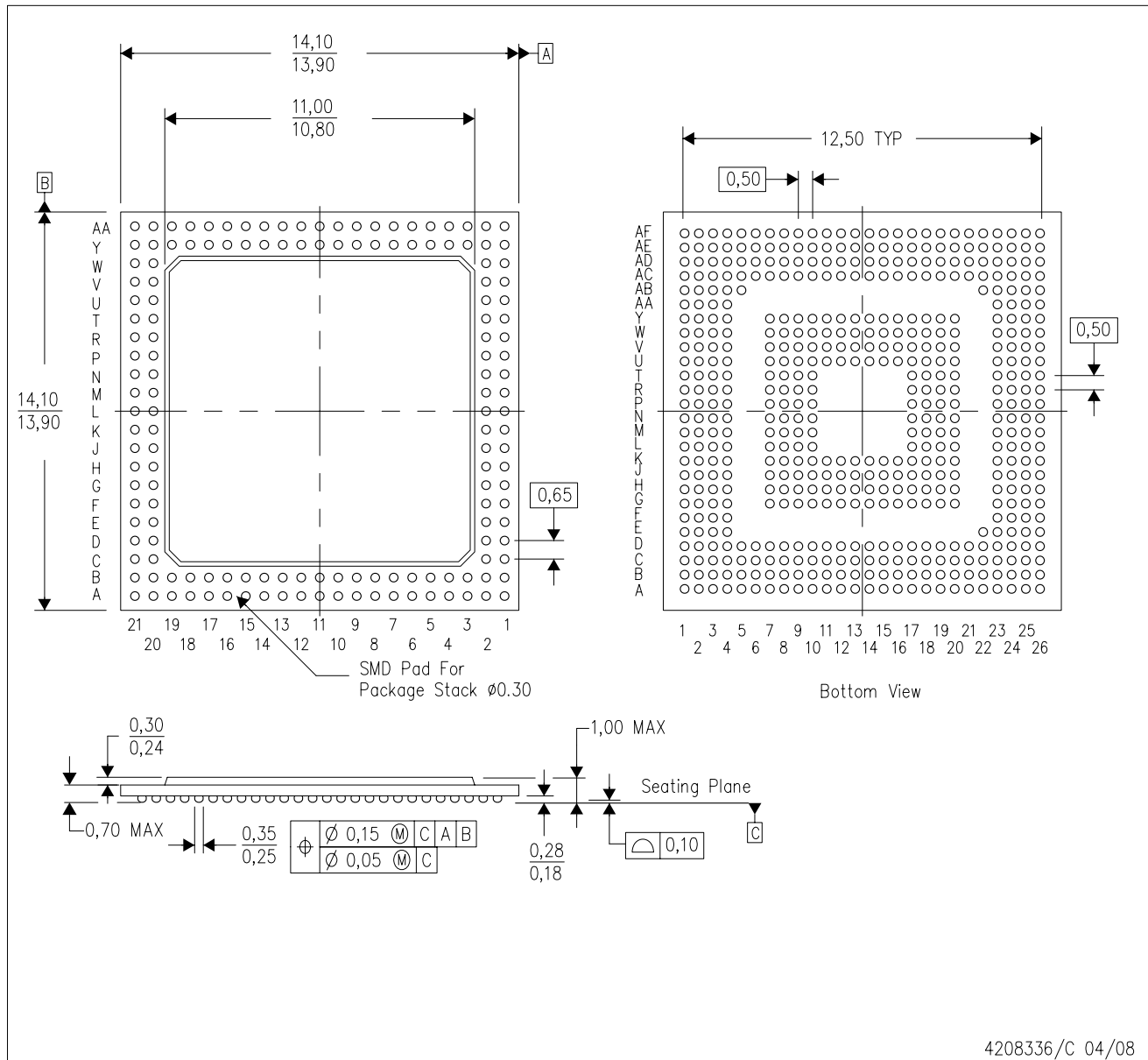
Bottom View

SMD Pad For
Package Stack ∅0.30

Seating Plane

4208336/C 04/08

NOTES:   A.  All linear dimensions are in millimeters.
         B.  This drawing is subject to change without notice.
         C.  Flip chip application only.
         D.  Lead-free die bump and solder ball.

CBP (S−PBGA−N515)                    PLASTIC BALL GRID ARRAY



Bottom View

168 SMD Pads For
Package Stack (∅0,28)

4209888/F 04/10
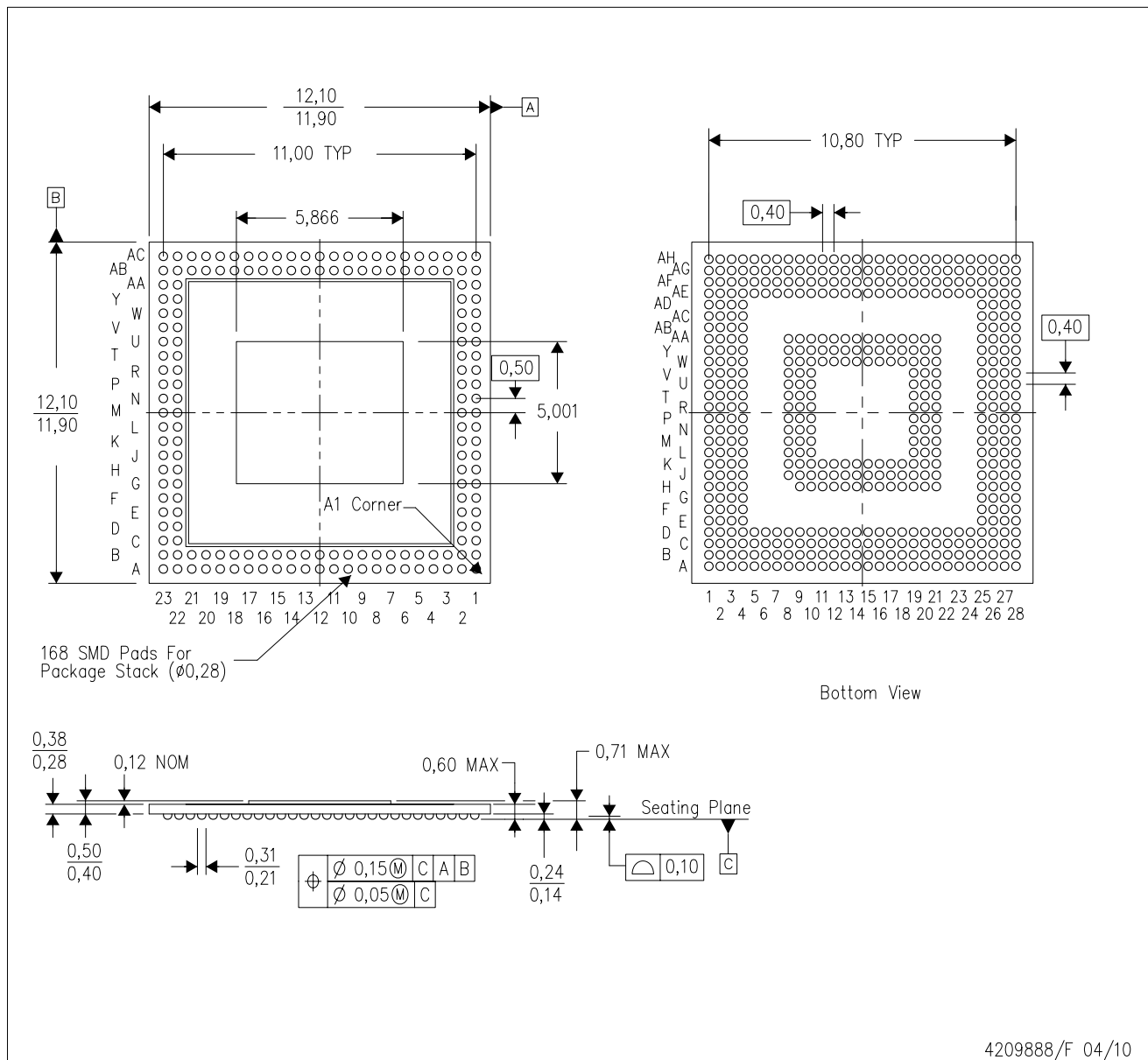
NOTES:   A.  All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
         B.  This drawing is subject to change without notice.
         C.  Flip chip application only.
         D.  Pb−free die bump and solder ball.

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