PLL Modulation

Topic	Student Name	Date	Course Leader
PLL	Wojciech Rościszewski-Wojtanowski (ID: 140062)	26/03/2020	Dr. Inż. Łukasz Matuszewski

This laboratory exercise expands the characteristics of the PLL linear modulation.

Introduction

PLL (else, phase locked loop) is a type of control system that is able to generate a sort of output signal with a phase that is in a way similarly related to the phase of our input signal of course they are not the same. In electronics there are different types of PLL's, one of the most common and simples is an electric circuit that is simply an oscillator of variable frequency and a phase detector that is in the feedback loop therefore whenever the oscillator generates a signal the detector acts and compares to the phase of signal with input in affect it adjusts the oscillator.

Measurements

All measurements for this experiment were simulated using the program LT Spice. Loaded onto the sheet is a modulator and a series of properties as instructed in manual.

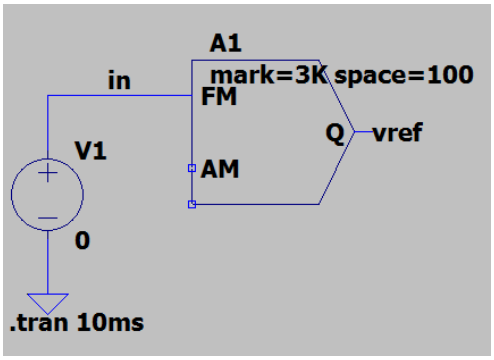

Figure 1.1 Presents EC used for simulation

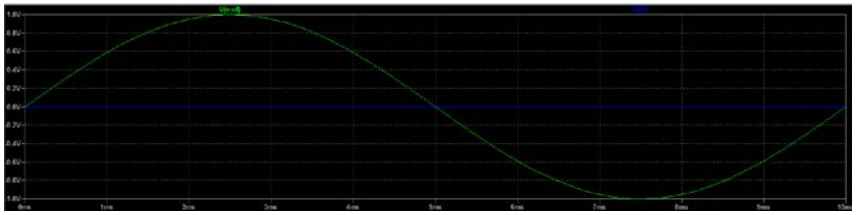

Figure 1.2 Presents EC graph from simulation

Voltage [V]	Frequency [Hz]
0.00	100
0.05	245
0.10	390
0.15	535
0.20	680
0.25	825
0.30	970
0.35	1115
0.40	1300
0.45	1400
0.50	1550
0.55	1700
0.60	1840
0.65	1990
0.70	2140
0.75	2280
0.80	2420
0.85	2560
0.90	2715
0.95	2850
1.00	3000

Figure 1.3 Presents table with given voltage and frequency measurements

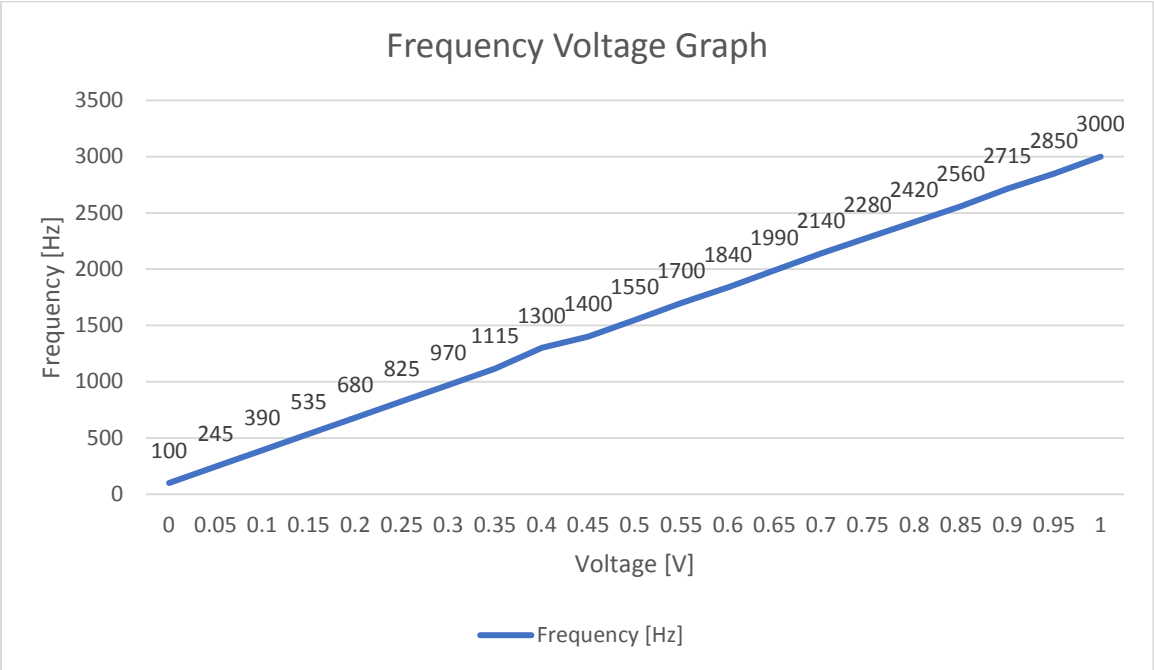

Figure 1.4 Presents a graph with data from figure 1.3

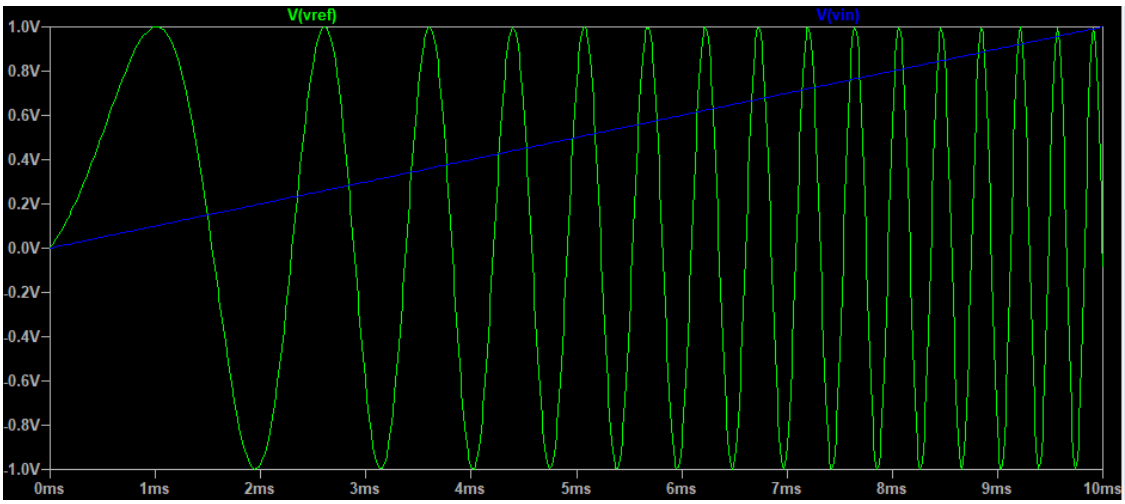

Figure 1.5 Presents graph after I've added PWL as in instruction manual

Once the XOR gate has been constructed with all of the components and values below please find the graphs obtained, please see all descriptions of graph details in figure notation.

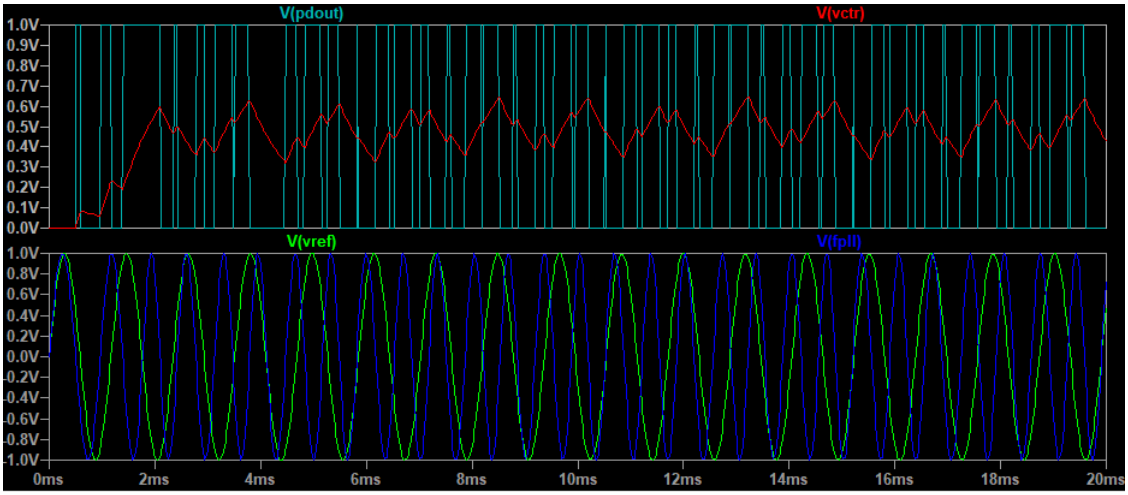

Figure 1.6 Presents synchronous mode graph.

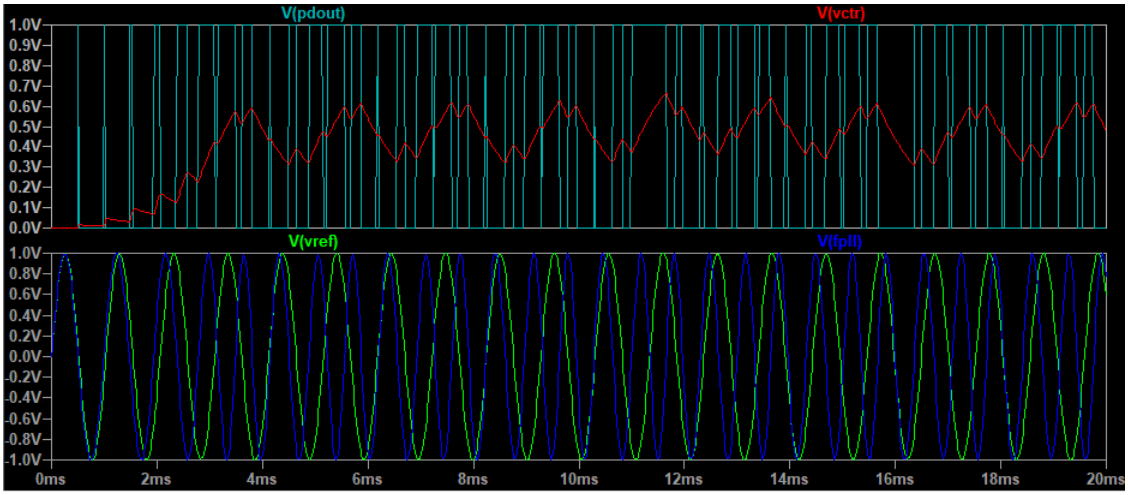

Figure 2.1 Presents the DC level being at 0.3V

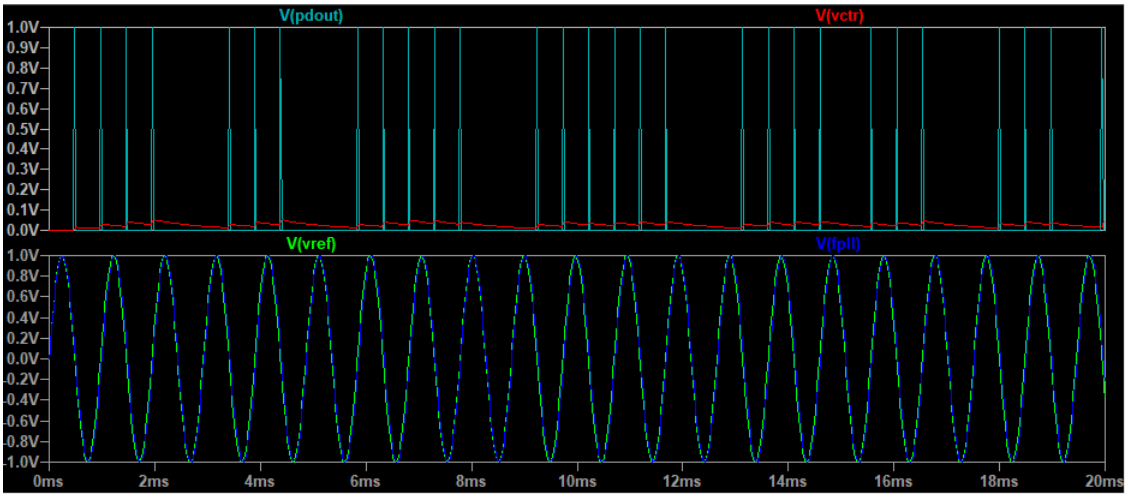

Figure 2.2 Presents the DC level being at est. 0.3V as it enters its synchronous state

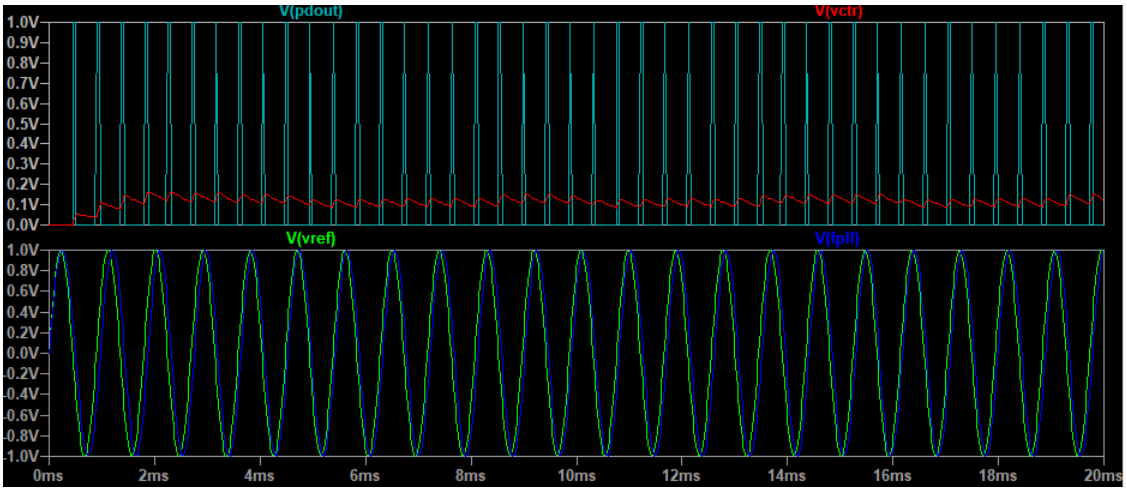

Figure 2.3 Presents the DC level being at est. 0.35V as it enters its synchronous state

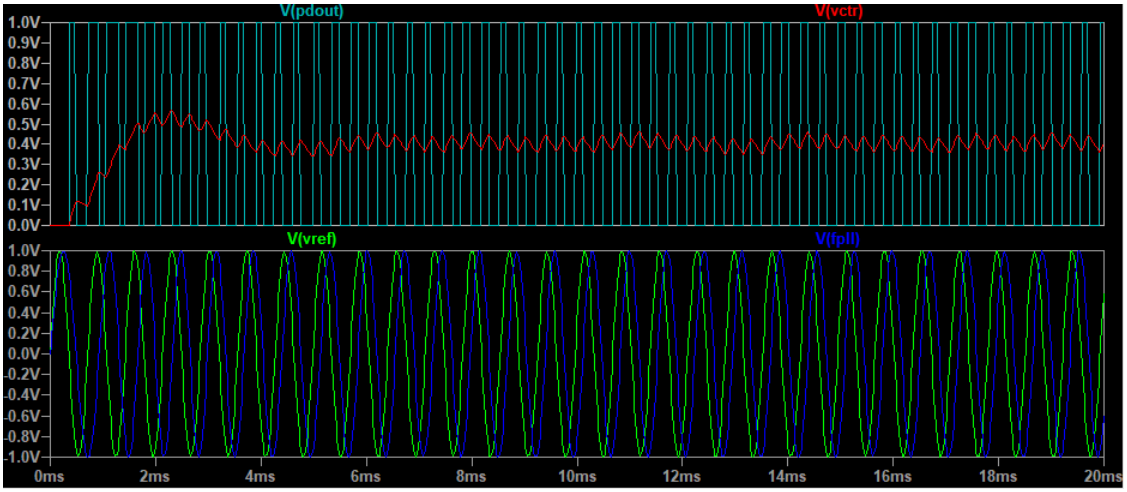

Figure 2.4 Presents the DC level being at est. 0.45 V as it enters its synchronous state

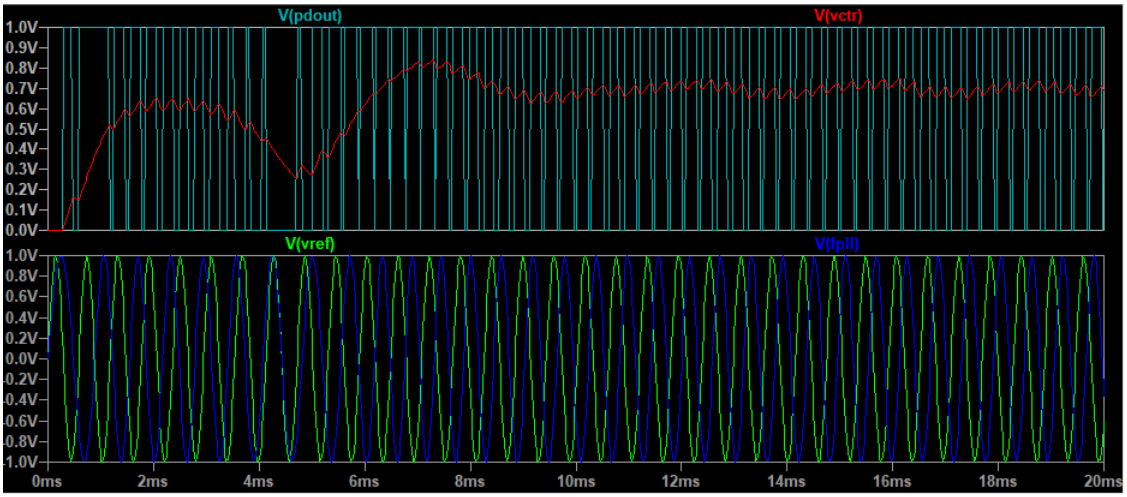

Figure 2.5 Presents the DC level being at est. 0.55V as it enters its synchronous state

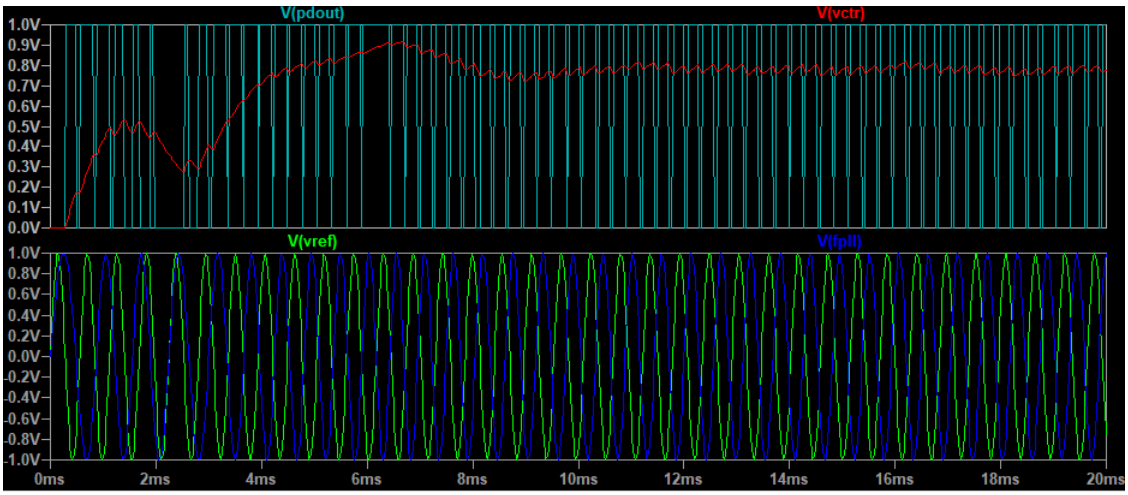

Figure 2.6 Presents the DC level being at est. 0.58V as it leaves its synchronous state

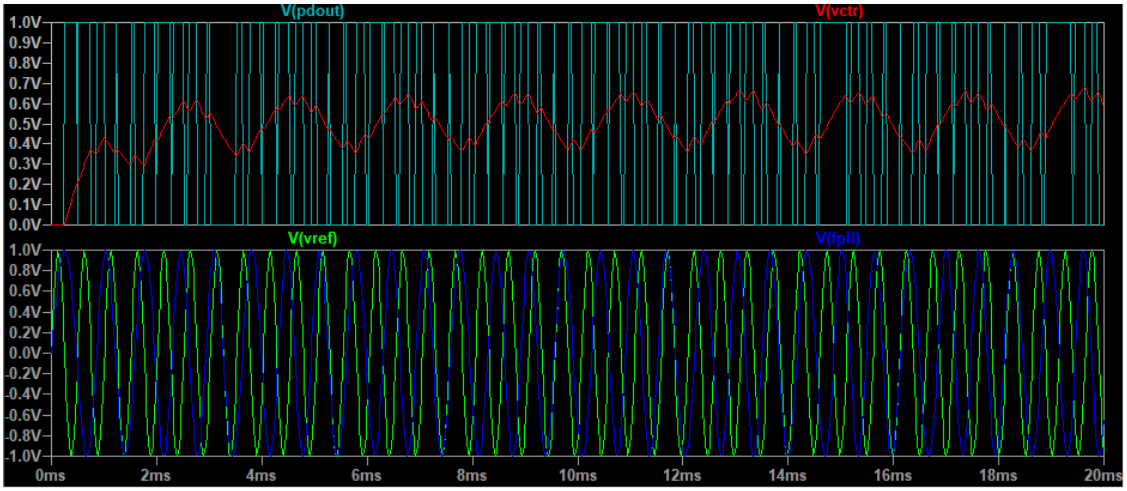

Figure 2.7 Presents the DC level being at est. 0.65V as it exits state

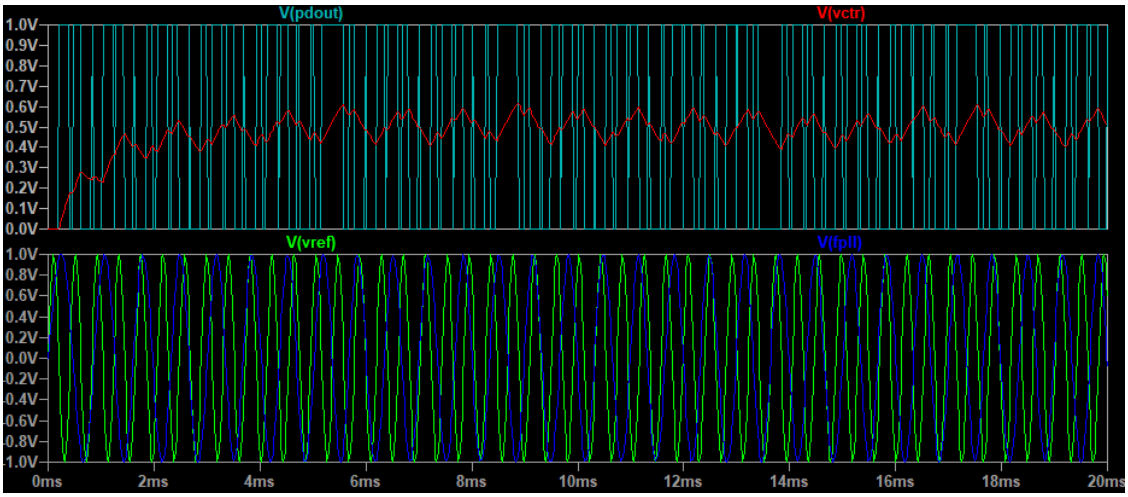

Figure 2.8 Presents the DC level being at est. 0.8V exited of state

Triangular Phase Detector slope characteristic is given below.

$$\varphi = \frac{t_{Vref} - t_{Fpll}}{period} * 2\pi \qquad K_D = \frac{\Delta PDout}{\Delta\varphi} = \frac{PDout_a - PDout_b}{\varphi_a - \varphi_b}$$

We then obtain with use of these formulas:

Φ= (0.0092195722s – 0.0090634456s) / 0.000714796283 * 2*3.14 = 1371. 68459227 rad

KD = 403mV/1371. 68459227 = 0.00029379932

$$K_F = \frac{\Delta PDout}{\Delta Vctr} = \frac{PDout_a - PDout_b}{Vctr_a - Vctr_b}$$

KF=403mV/405mV = 0.99506172839