FM Demodulation

Topic	Student Name	Date	Course Leader
FM Demodulation	Wojciech Rościszewski-Wojtanowski (ID: 140062)	26/05/2020	Dr. Inż. Łukasz Matuszewski

This laboratory exercise expands the characteristics of the FM (frequency modulation) demodulation.

Introduction

Below please find a block diagram of a balanced FM modulator.

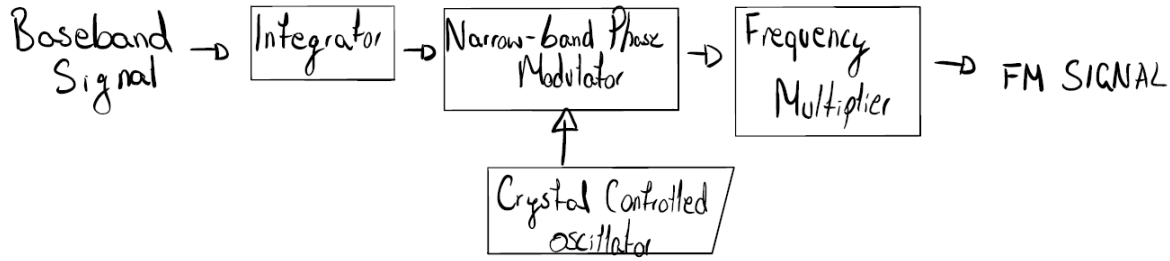

Figure 1 Presents a block diagram of a frequency modulated signal

Measurements

Below please see the circuit that I've constructed in the LTSpice environment.

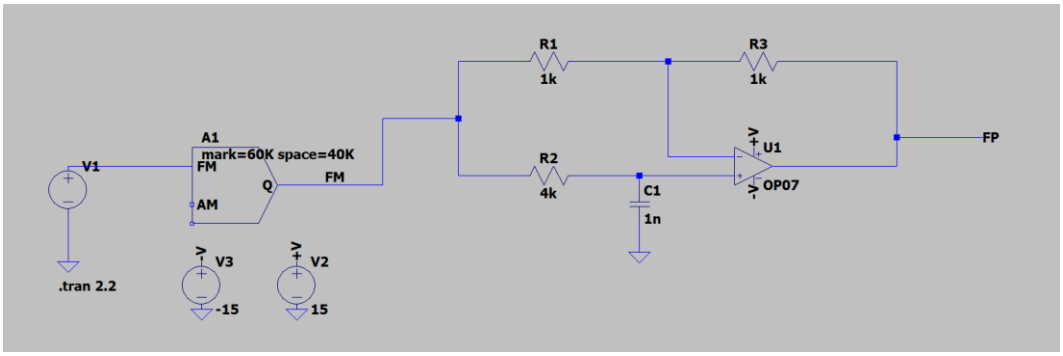

Figure 2 Presents the circuit built from the instruction manual

Below please see the simulation results using the following circuit, as per instruction voltage of source gate has been set to 0v potential.

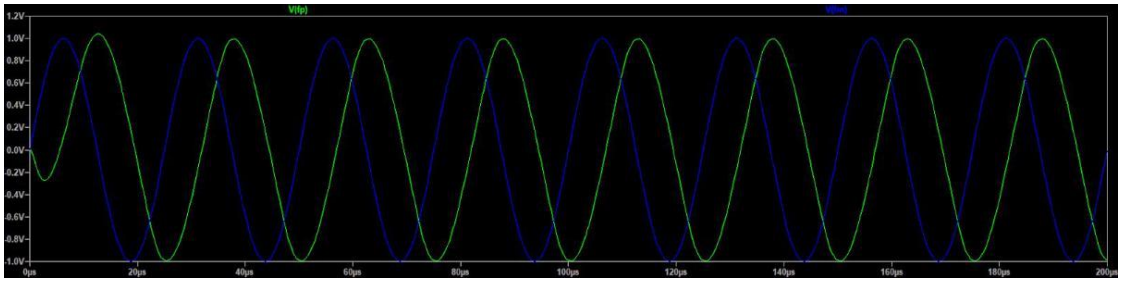

Figure 3 Presents the simulation

As you can see, we see two signals within which one is a FM signal and the other is the FP signal, the phase-shift degree between our two signals presented in the figure above at estimate 96 degrees. Phase shift has been calculated using cursors assuming the time delay of our signals. Therefore, for me to gain the correct phase shift of around 90 degrees I must calculate the values of capacitive and resistive elements of our circuits using the formula 1/2pi*R*C.

With VG set to 1V we receive the following parameters:

- Frequency FM = 60 kHz,
- Frequency FP = 60 kHz,
- Phase-shift = 92 degrees

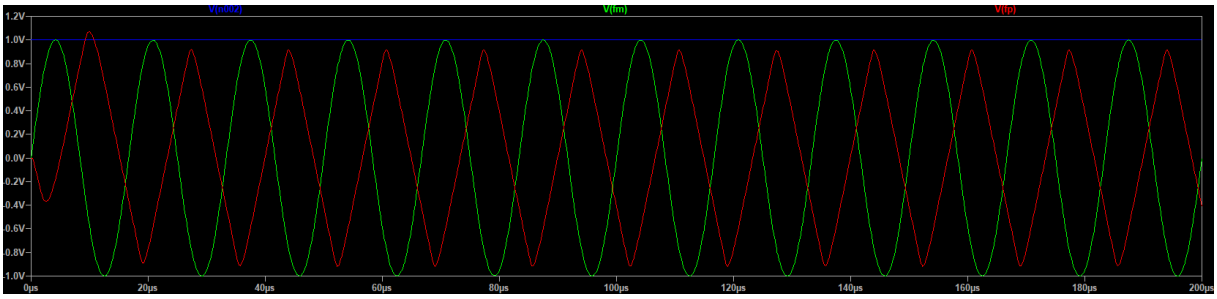

Figure 4 Presents the simulation of new system with VG set to 1V

Below please see a new plot presenting results with the VG set to -1.

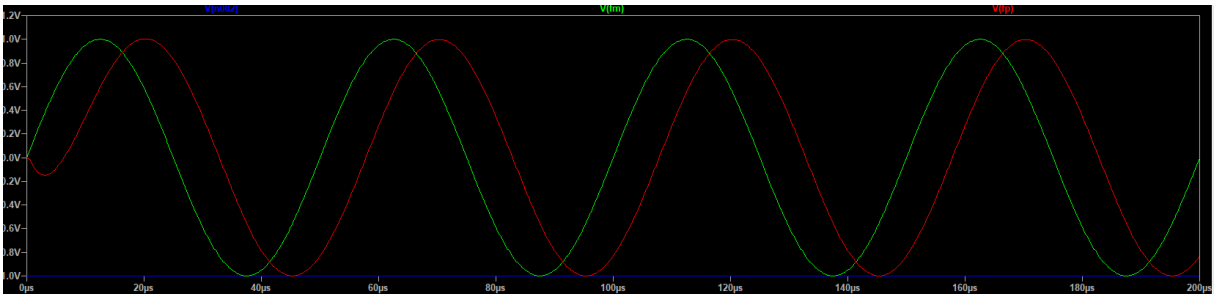

Figure 5 Presents simulation of new system with VG set to -1V

With VG set to 1V we receive the following parameters:

- Frequency FM = 20 kHz,
- Frequency FP = 20 kHz,
- Phase-shift = 92 degrees

To conclude this section/stage of our simulations we can see that by changing the voltage to a value greater than zero the two signals parameters change mostly the frequency increases whilst if the voltage is changed to a value lower than zero then the signal frequency has been decrease as seen in figures 4 and 5.

Below please see a new circuit as per provided instructions in the manual I have constructed the new phase discriminator detector. The message signal of voltage gate 1 VG1 is set with the following parameters as provided in the instruction manual. Sinusoidal wave carrier has been set with an amplitude of 1V and a frequency of 1.5 kHz

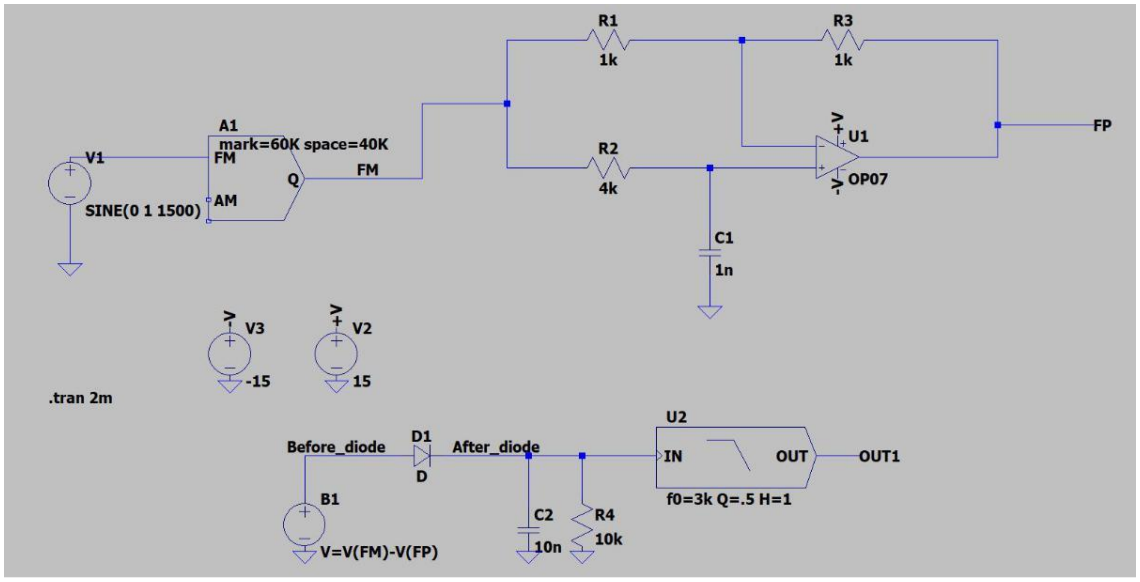

Figure 7 Presents a phase discriminator detector circuit.

The simulation has been ran, below please see the simulation results using all probe output points. As you can see the input of diode we have our modulation of the amplitude, this can be inferred from B1 gate as we are reducing the signal by subtracting the FP signal from FM signal.

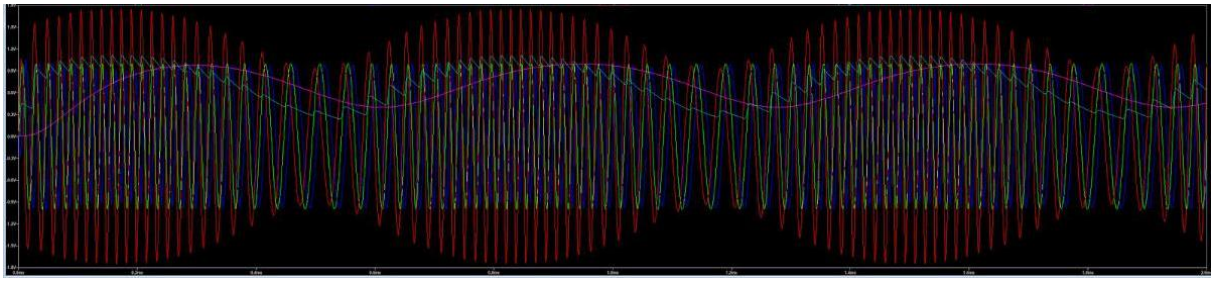

Figure 8 Phase discriminator detector simulation output

Below please see a simulation with the resistor R4 parameter changed to 10kΩ

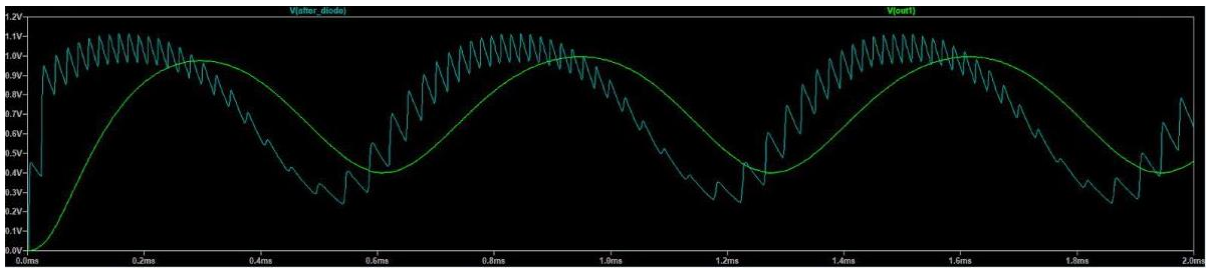

Figure 9 Presents the output signal on output and D1 (after diode)

Below please see a simulation with the resistor R4 parameter changed to 1kΩ

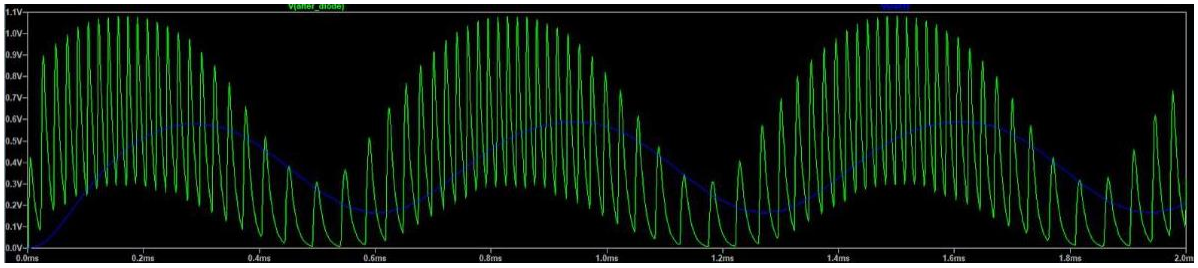

Figure 10 Presents the output signal on output and D1 (after diode)

Below please see a simulation with the resistor R4 parameter changed to 100kΩ

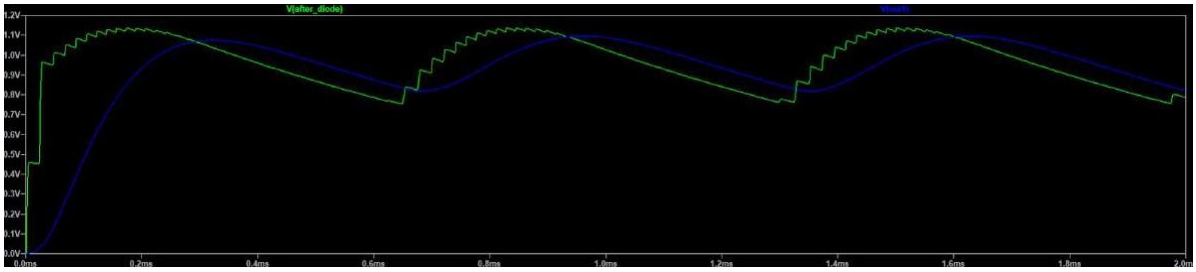

Figure 11 Presents the output signal on output and D1 (after diode)

As you can see in the figures 9 – 11 in the above we see the response of the output signal according to the change of resistance in the resistive element R4. All of this was done under a supplied sinusoidal VG source.
Next step of this task is to set a square wave at the voltage gate, below please see the effects of changing the resistance in resistor R4 for square wave input.

Below please see a simulation with the resistor R4 parameter changed to 10kΩ

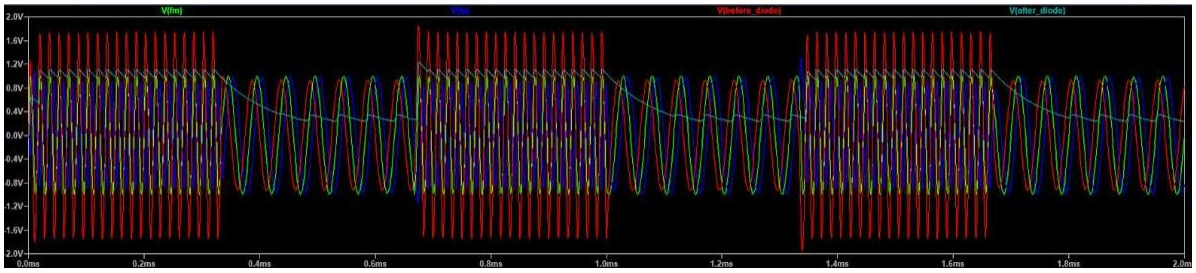

Figure 12 Presents the all signal analysis with R4 parameter changed

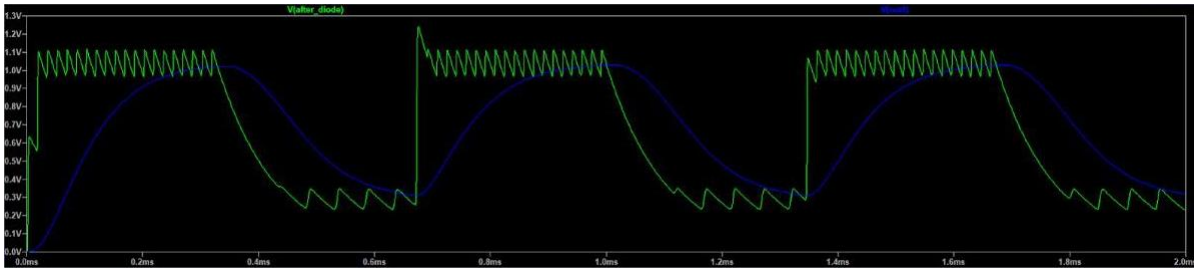

Figure 13 Presents the output signal on output and D1 (after diode) with R4 parameter changed

Below please see a simulation with the resistor R4 parameter changed to 1kΩ

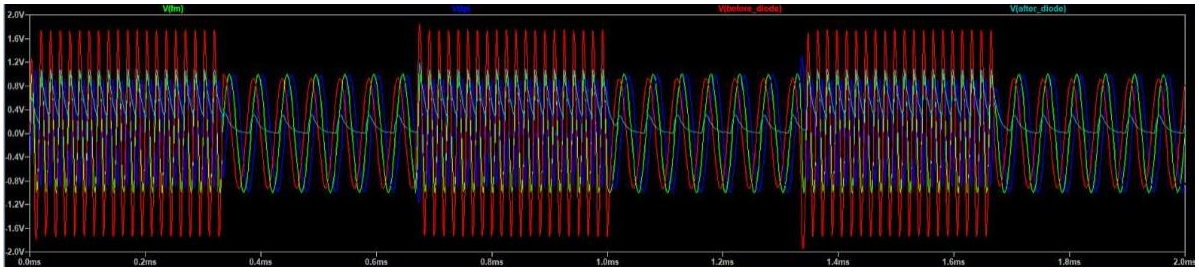

Figure 14 Presents the all signal analysis with R4 parameter changed

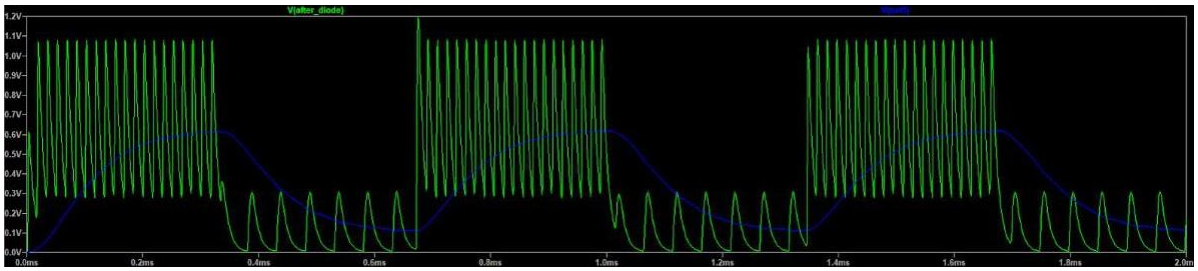

Figure 15 Presents the output signal on output and D1 (after diode) with R4 parameter changed

Below please see a simulation with the resistor R4 parameter changed to 100kΩ

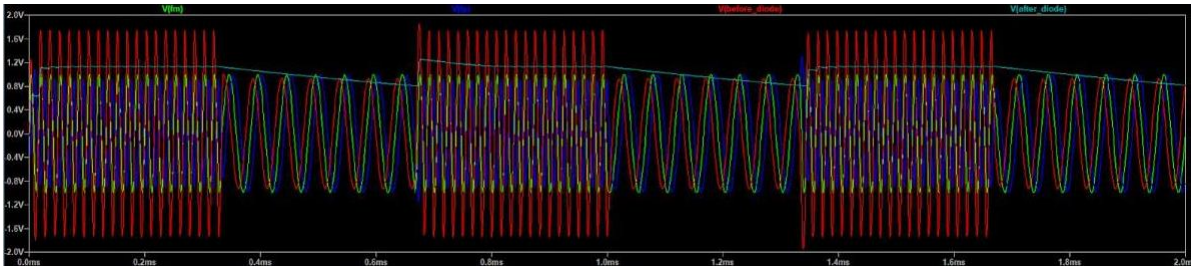

Figure 16 Presents the all signal analysis with R4 parameter changed

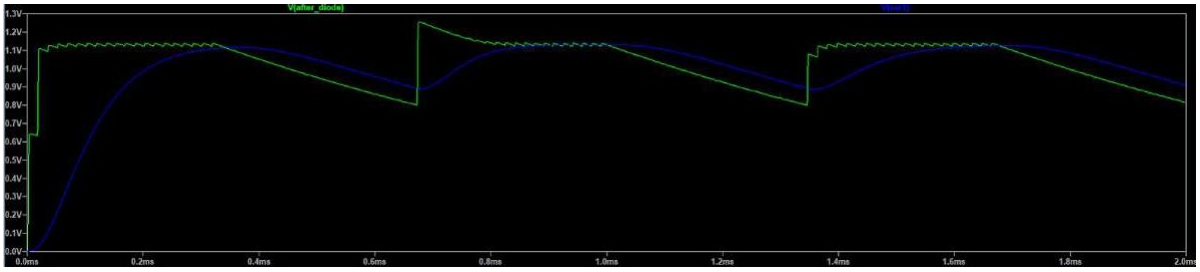

Figure 17 Presents the output signal on output and D1 (after diode) with R4 parameter changed

Next step of this task is to set a triangular wave at the voltage gate, below please see the effects of changing the resistance in resistor R4 for square wave input.

Below please see a simulation with the resistor R4 parameter changed to 10kΩ

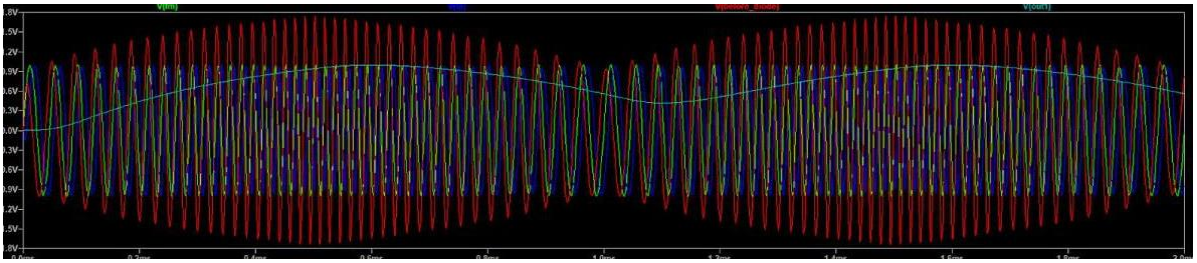

Figure 18 Presents the all signal analysis with R4 parameter changed

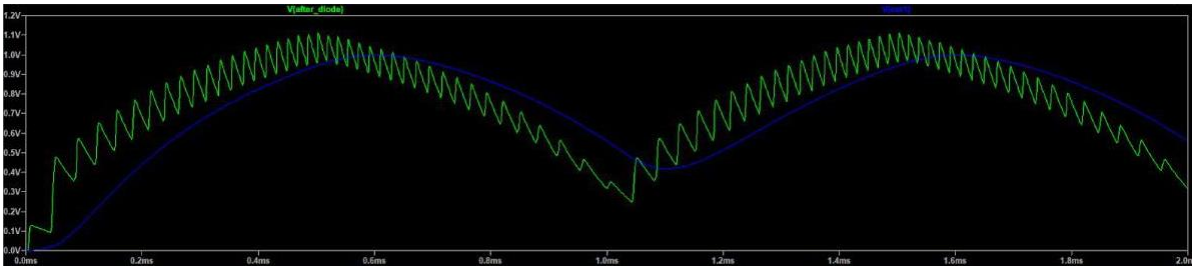

Figure 19 Presents the output signal on output and D1 (after diode) with R4 parameter changed

Below please see a simulation with the resistor R4 parameter changed to 1kΩ

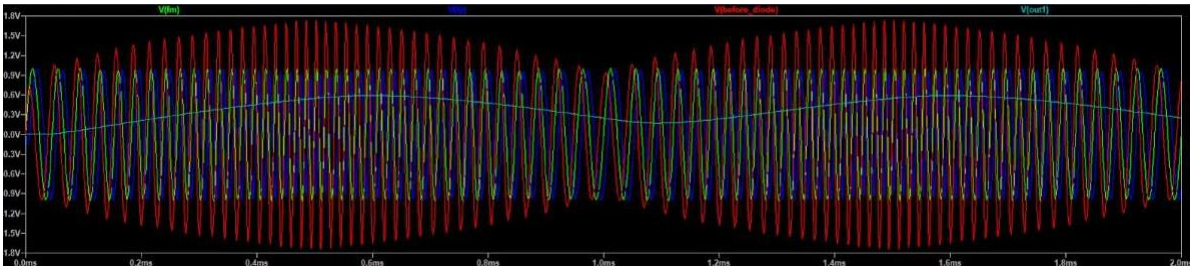

Figure 20 Presents the all signal analysis with R4 parameter changed

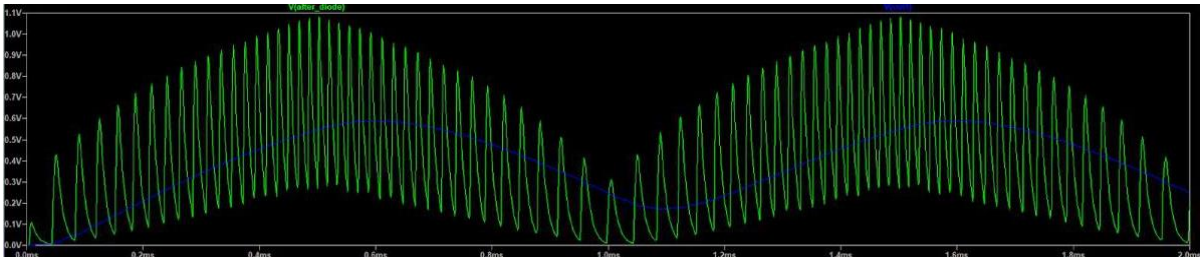

Figure 21 Presents the output signal on output and D1 (after diode) with R4 parameter changed

Below please see a simulation with the resistor R4 parameter changed to 100kΩ

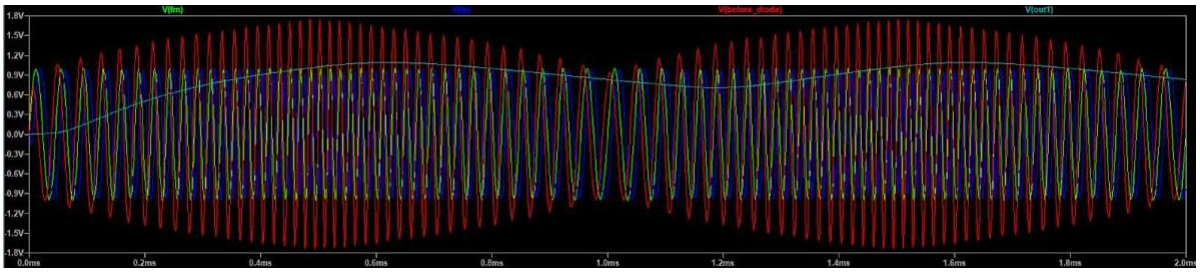

Figure 22 Presents the all signal analysis with R4 parameter changed

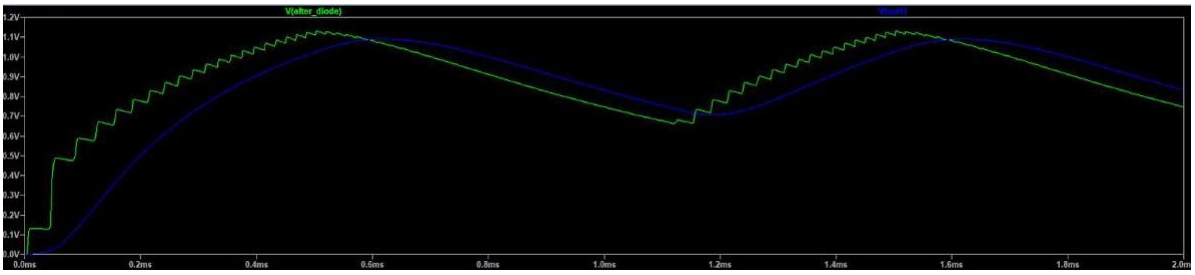

Figure 23 Presents the output signal on output and D1 (after diode) with R4 parameter changed

As seen in the figures in the above we notice that the capacitive and resistive components influence our signal by changing its amplitude as well as frequency - C4 and R4. Please note that this statement only agrees with signals based on the output of the diode as well as the output overall signals.

Below please see the Coincidence detector

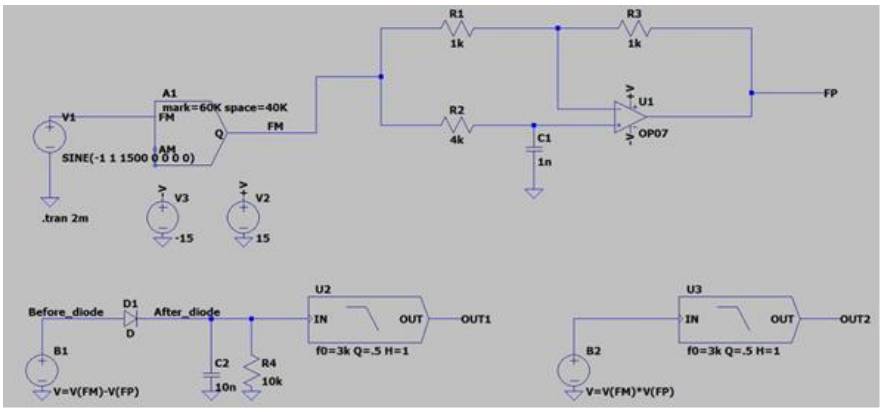

Figure 24 Presents the coincidence detector

As provided in the instruction manual the message signal at voltage gate V1 has been set to the following parameters; input wave is a sinusoidal wave with a frequency of 1.5kHz. The simulation has been ran. Below please find figures 25 and 26 presenting the output resulting signals of said simulation.

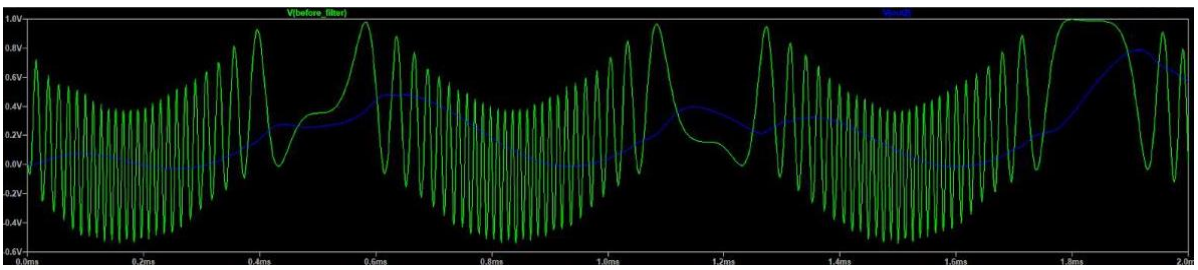

Figure 25 Presents the two signals before and after using the filters

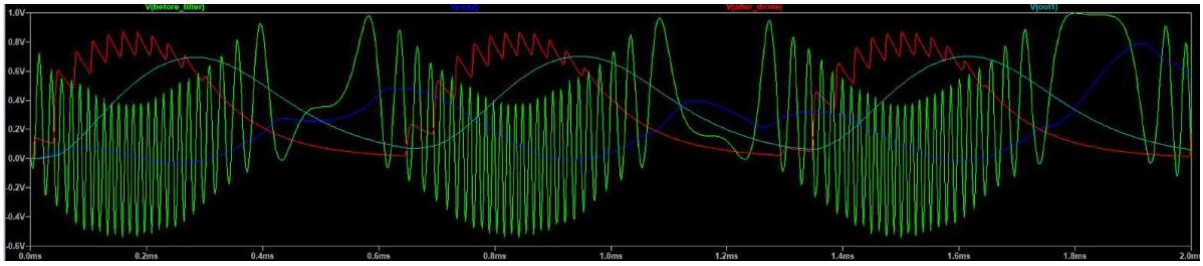

Figure 26 Presents the all signals before and after using the filters (all probe points)

In the above please see figures 25 and 26 presenting the output signals. Firstly we notice that there are less of these fluctuations in figure 25 and more in figure 26. We see that our detector with diode has a low frequency in comparison to the detector without diode, however its amplitude is far more larger. Phase-shift of the signals vary.

Harmonic Number	Frequency [Hz]	Fourier Component	Normalized Component	Phase [degree]	Normalized Phase [deg]
1	1.500e+03	3.134e-01	1.000e+00	-68.45°	0.00°
2	3.000e+03	3.833e-02	1.223e-01	-163.90°	-95.45°
3	4.500e+03	1.107e-02	3.533e-02	-150.08°	-81.63°
4	6.000e+03	3.740e-03	1.193e-02	168.83°	237.28°
5	7.500e+03	1.429e-03	4.560e-03	-178.89°	-110.44°
6	9.000e+03	6.511e-04	2.078e-03	166.77°	235.22°
7	1.050e+04	3.274e-04	1.045e-03	-179.10°	-110.65°
8	1.200e+04	1.672e-04	5.335e-04	176.33°	244.78°
9	1.350e+04	1.062e-04	3.387e-04	-175.34°	-106.90°
10	1.500e+04	7.466e-05	2.382e-04	178.56°	247.01°

Total Harmonic Distortion: 12.796040%(13.152181%)

N-Period=100
Fourier components of V(out2)
DC component:0.241558

Harmonic Number	Frequency [Hz]	Fourier Component	Normalized Component	Phase [degree]	Normalized Phase [deg]
1	1.500e+03	2.425e-01	1.000e+00	125.62°	0.00°
2	3.000e+03	1.542e-02	6.357e-02	1.89°	-123.73°
3	4.500e+03	4.965e-03	2.047e-02	89.51°	-36.11°
4	6.000e+03	2.036e-03	8.394e-03	-167.81°	-293.43°
5	7.500e+03	4.406e-04	1.817e-03	-155.72°	-281.34°
6	9.000e+03	8.610e-04	3.550e-03	170.21°	44.59°
7	1.050e+04	6.923e-04	2.855e-03	-158.01°	-283.63°
8	1.200e+04	3.339e-04	1.377e-03	169.10°	43.48°
9	1.350e+04	6.028e-04	2.486e-03	171.27°	45.65°
10	1.500e+04	4.061e-04	1.674e-03	-165.06°	-290.68°

Total Harmonic Distortion: 6.756555%(56.289981%)

Figure 27 Presents the Total Harmonic Distortion Analysis

As seen in the figure 27, in the above the total distortion is 6.76% (56.3%) for OUT1 probe points whereas for probe point OUT2 the distortion is 12.8%(13.1%). As seen the output which has the lowest distortion has the lowest amount of harmonic distortion in comparison to the second detector.

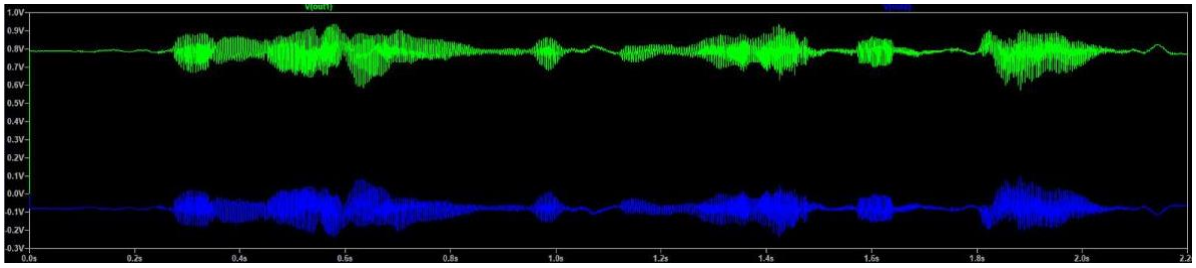

Figure 28 Presents the total harmonic distortion of signals based at probe points OUT 1 & OUT 2

As seen in the figure 28 in the above we see the simulation results or the reconstruction of our signals, we see that the quality is similar between the two signals. However we see certain factors or differences between the two for example the amplitude of the output 2 is far much lower in comparison to the amplitude of output 1. Output 2 is the coincidence detector so it can be said that output 1 phase discriminator detector has a much higher output than the coincidence detector. Thus the sound quality can potentially be more higher in the phase discriminator circuit than the coincidence detector circuit. Another factor is that the design is quite hard and difficult to get around therefore we can say that this is a big drawback hence why the coincidence detector would be the cheapest option.