

MPPG Tool User Guide

V1.2

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Revision History

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1 Introduction

RTK MP PG Tool supports flash programming for RTL87XX series chips.

First, you may refer to [Appendix](#) about EVB connection and pre-settings. There are two modes of downloading image to chip. One is MP Mode, which is for factory mass production; while the other is RD Mode, which is for factory R&D to do some debugs about their image downloading to chip.

In “MP Mode”, tool only accept packed image file which will be packed through “Pack Tool”. In this mode, it provides two methods to modify BT address per chip; provides selection to merge RF parameters and BT address etc. in previous stage (e.g. MP Test); provides selection to modify frequency offset; supports auto-detect serial ports connected.

In “RD Mode”, tool can only accept downloading individual sub-images, also it provides method to modify several configuration parameters. In this mode, detecting and manipulating one or more serial ports is also supported.

2 MP Tool Introduction

2.1 Guide interface



Figure 2-1 Guide interface

Before enter main interface, please select proper “IC Series,” “IC Type” and “Language” (Figure 2-1).

- 1) Click “IC Series” to select IC series you are going to use.
- 2) Then click “IC Type” to select IC type you are going to use. Please make sure correct IC type is selected, or unexpected situation maybe happen in PG procedure.
- 3) Currently two languages are supported: “English” and “Chinese simplified.”
- 4) After IC type and language selection, click “Confirm” to enter main interface of MPPG Tool.

If “Cancel” is clicked, the application terminated and exit.

2.2 Main interface

Figure 2-2 shows the Main interface of MPPG tool.

You can switch “MP mode” or “RD Debug mode” via click Menu “Type”.

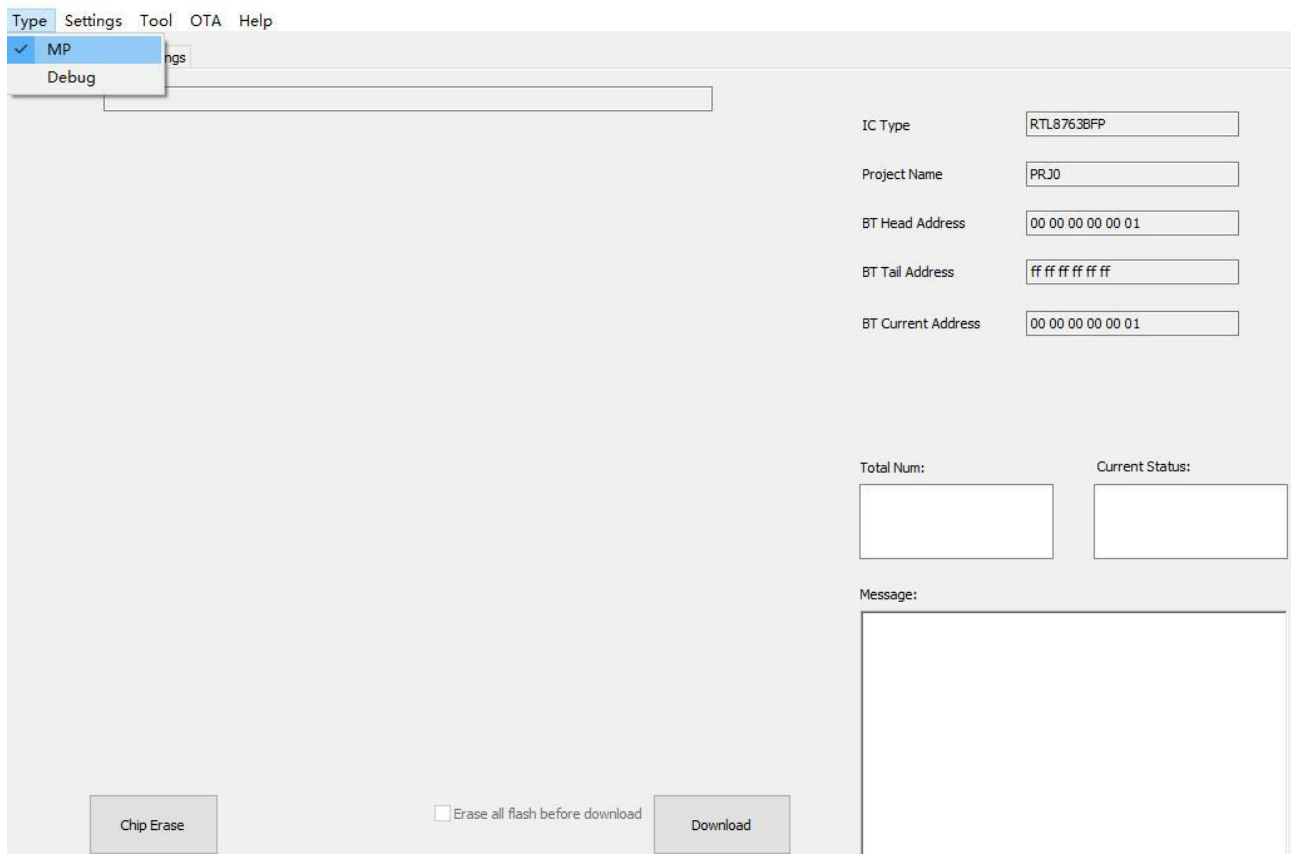


Figure 2-2 Main interface and switch mode

2.3 MP Mode

In MP Mode, MPPG Tool supports functions as follows:

- Chip Erase
- Download with chip erase
- Parallel downloading up to eight ports at a time
- BT address management
- Read back & Merge
- Frequency Offset
- Save & Cancel settings
- Two kinds of BT address setting method
- Some other settings

We will elaborate on these functions in the following chapters.

2.3.1 MP Setting

Before flash programming, you could modify some settings on “MP Setting” page.

2.3.1.1 Lock & Unlock

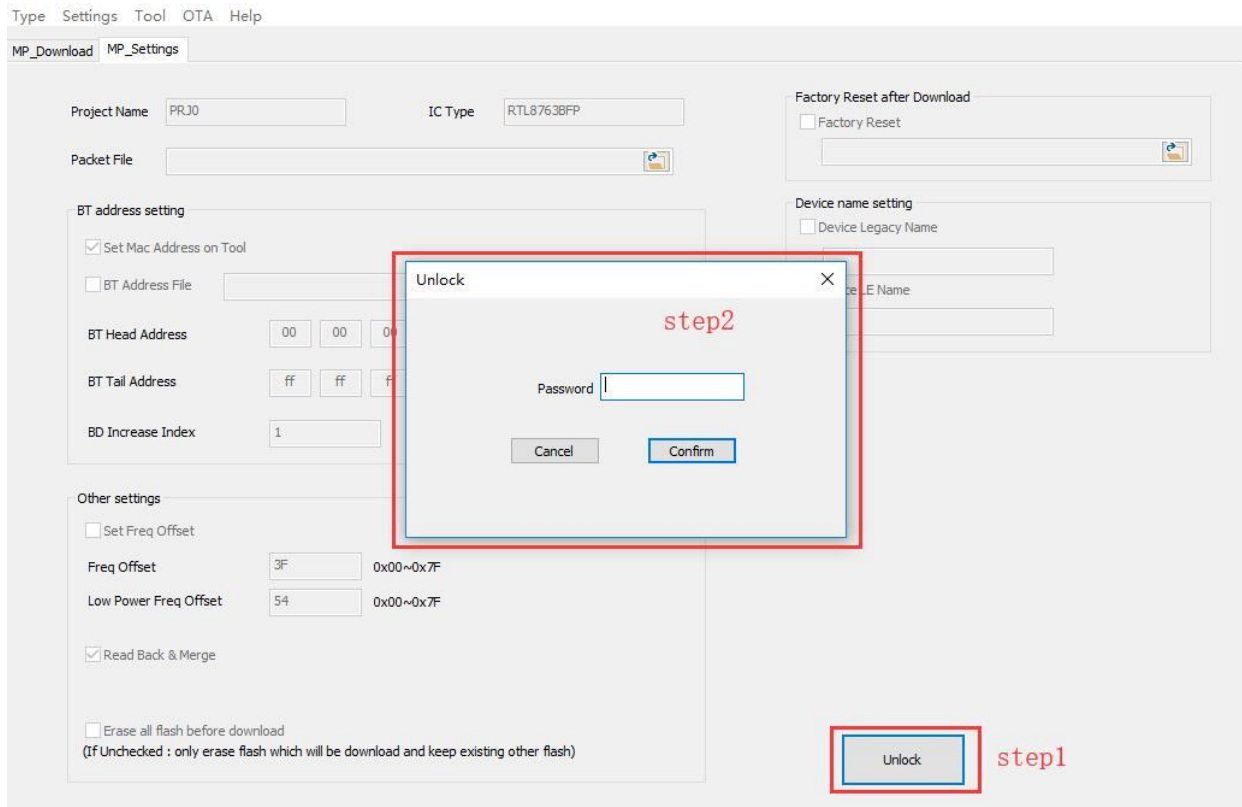


Figure 2-3 Unlock MP Settings

Once entered, this page is always locked to prevent misoperation.

Click “Unlock”, enter password in pop-up dialog and click “Confirm”, then you can set configuration items on the page (Figure 2-3). Usually the initial password is “1”.

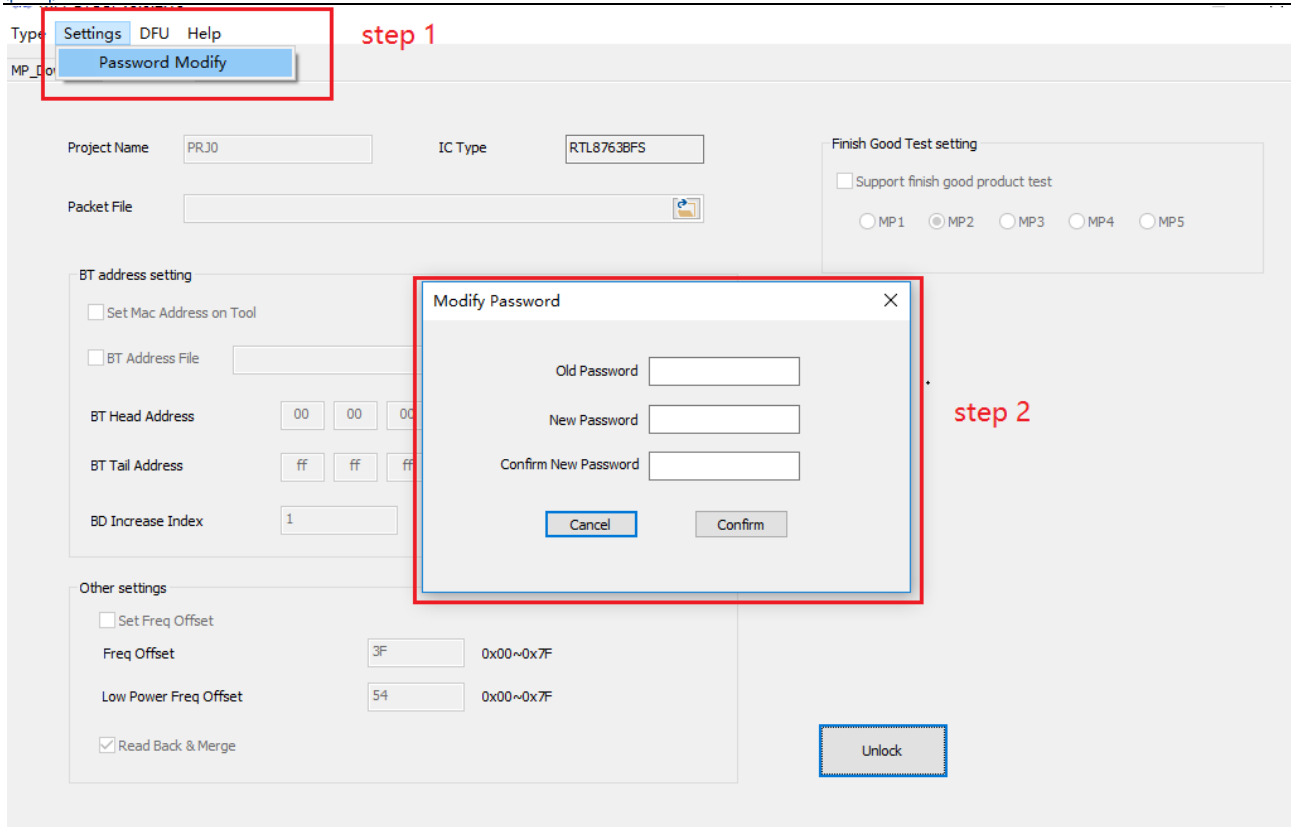


Figure 2-4 Modify Password

You can also modify password of “MP Setting” page via menu by “Settings -> Password Modify” (Figure 2-4).

In “Modify Password” dialog, enter old password, new password, and reenter new password.

Password can be any characters, but empty password is not allowed.

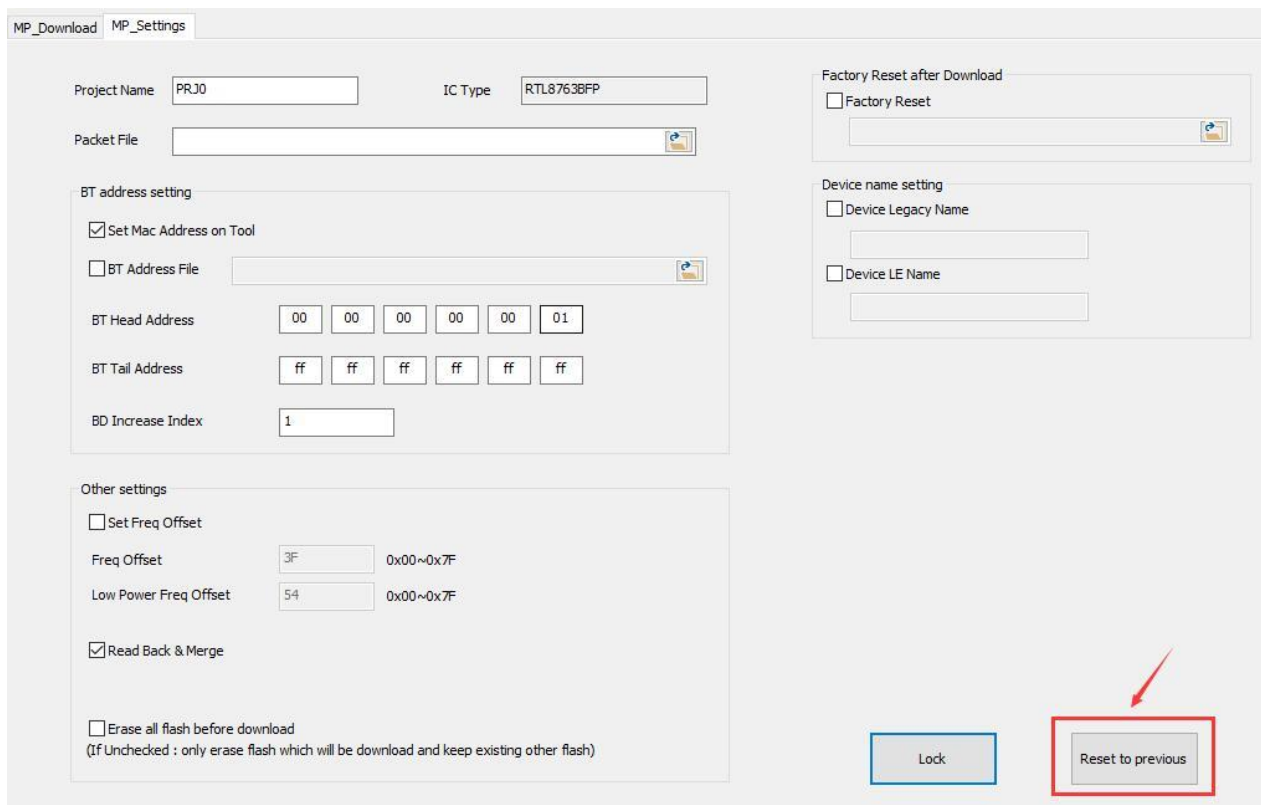


Figure 2-5 Cancel settings

After setting configs on the “MP setting” page, you can choose to save the modification or discard them.

If you don’t want to save them, click “Reset to previous” to discard modification, and parameters on the page will be reversed to previous setting, then click “Lock” to lock the page (Figure 2-5).

If you want to save the configuration, just click “Lock” to save setting modification and lock the page.

2.3.1.2 Configuration Item

In “MP Setting” page you can modify the following settings:

- Project Name
- Packet File
- BT Address Setting
- Frequency Offset
- Merge Back
- Device Name Setting (particular function for specific chips)
- Write RSA Key SHA256(particular function for specific chips)

A) Project Name

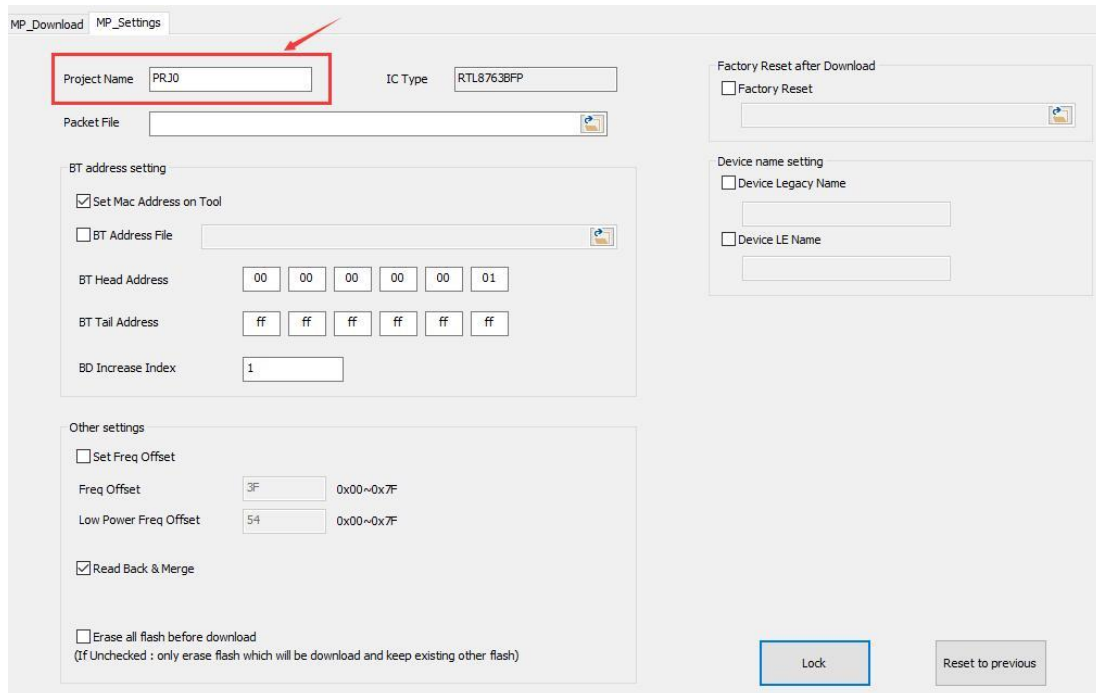


Figure 2-6 Modify Project Name

You can enter a new project name to distinguish from other PG projects, as shown in Figure 2-6.

B) Packet File

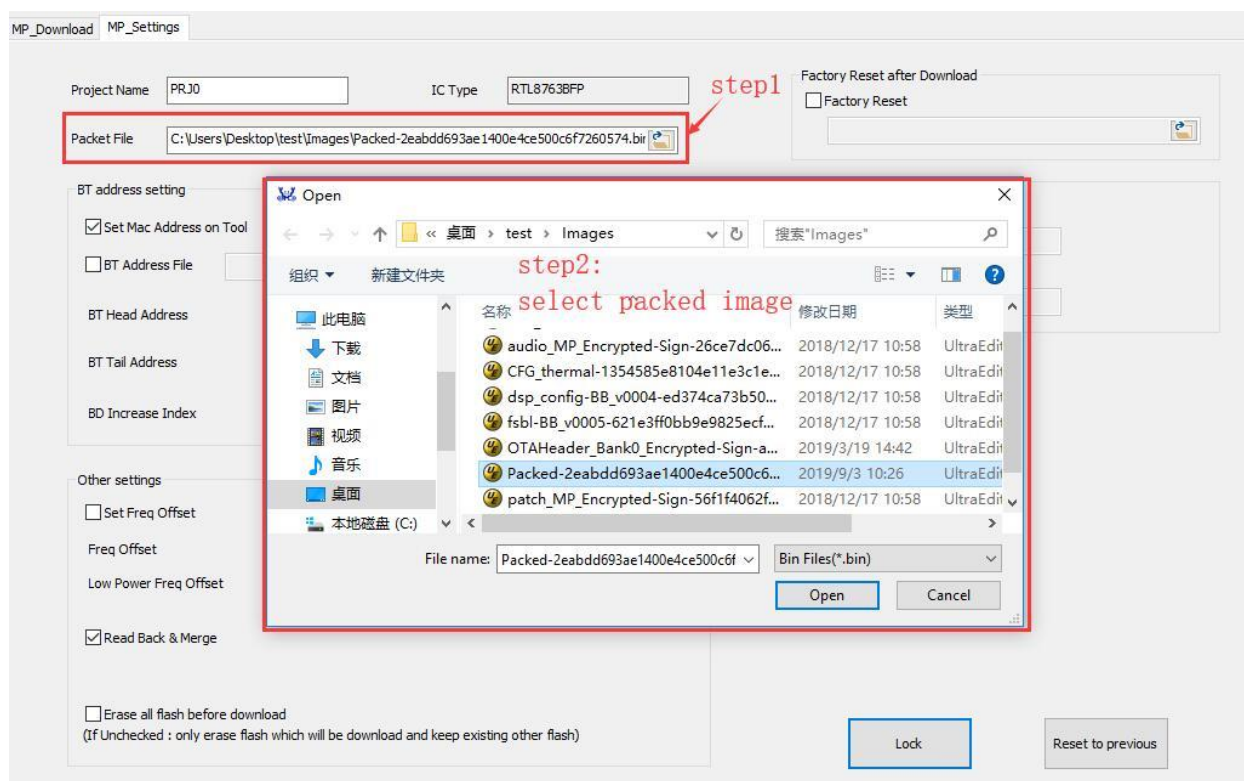
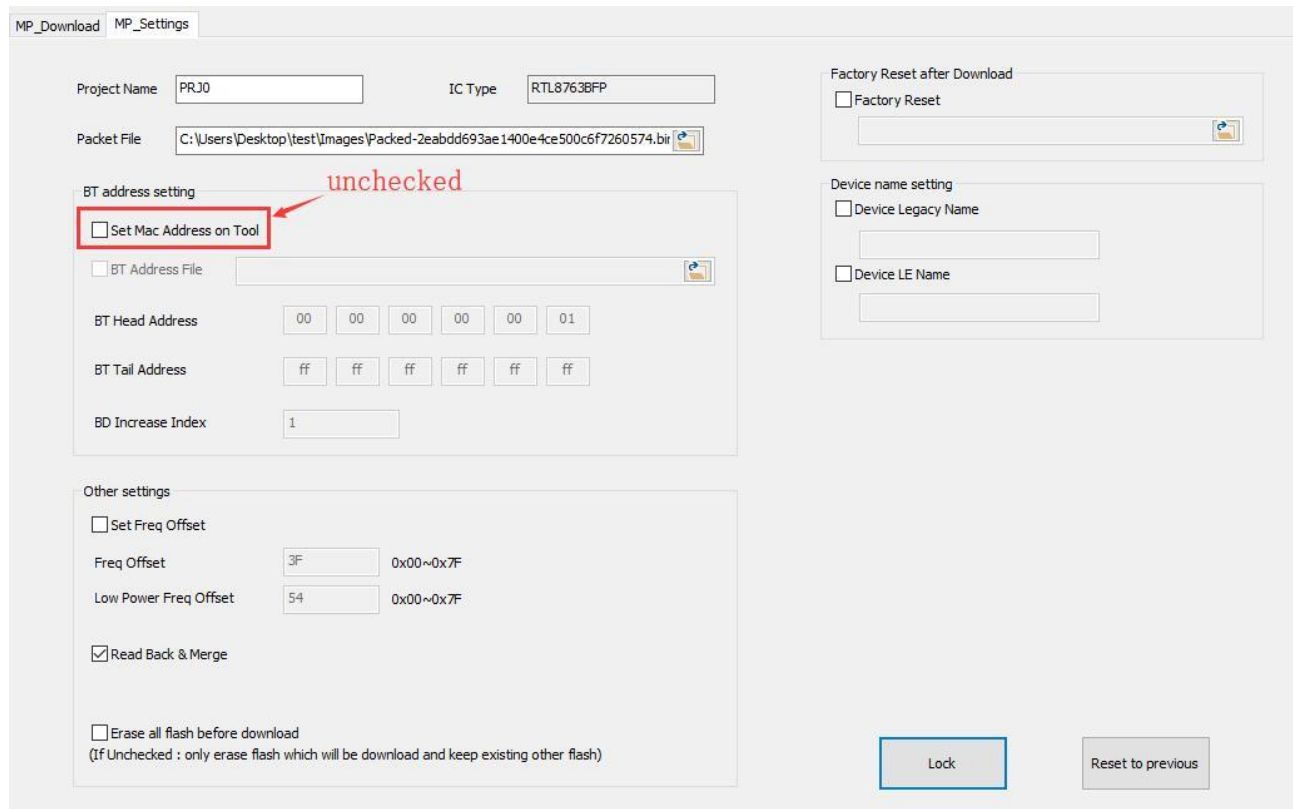


Figure 2-7 Import packet file

There are two ways to select packet file:

- 1) Click the open folder button firstly, an “Open” dialog will pop up. Then select the packet file corresponding to current IC type(Figure 2-7).
- 2) Or you can type in the pack file name directly in the “Packet File” editbox.

C) BT Address Setting



The screenshot shows the 'MP_Settings' tab in the MPPG Tool. The 'BT address setting' section is expanded, showing the 'Set Mac Address on Tool' checkbox is unchecked. A red box highlights this checkbox, and a red arrow points to it with the word 'unchecked' in red text. Other settings include 'Project Name' (PRJ0), 'IC Type' (RTL8763BFP), 'Packet File' (C:\Users\Desktop\test\Images\Packed-2eabdd693ae1400e4ce500c6f7260574.br), 'Factory Reset after Download' (unchecked), 'Device name setting' (unchecked), 'BT Address File' (empty), 'BT Head Address' (00 00 00 00 00 01), 'BT Tail Address' (ff ff ff ff ff ff), 'BD Increase Index' (1), 'Other settings' (Set Freq Offset unchecked, Freq Offset 3F, Low Power Freq Offset 54, Read Back & Merge checked, Erase all flash before download unchecked), and buttons for 'Lock' and 'Reset to previous'.

Figure 2-8 Uncheck “Set Mac Address on Tool”

1. If there is no need to configure BT address per chip in MP download, uncheck “Set Mac Address on Tool” (Figure 2-8).

Attention:

If you want to keep “BT address” configured in previous stage (e.g. MP Tests), just uncheck “Set Mac Address on Tool”, and make sure “Read Back & Merge” is checked.

2. If you want to program “BT address” down to chip in this stage, just check “Set Mac Address on Tool”. There are two ways to configure BT address setting.

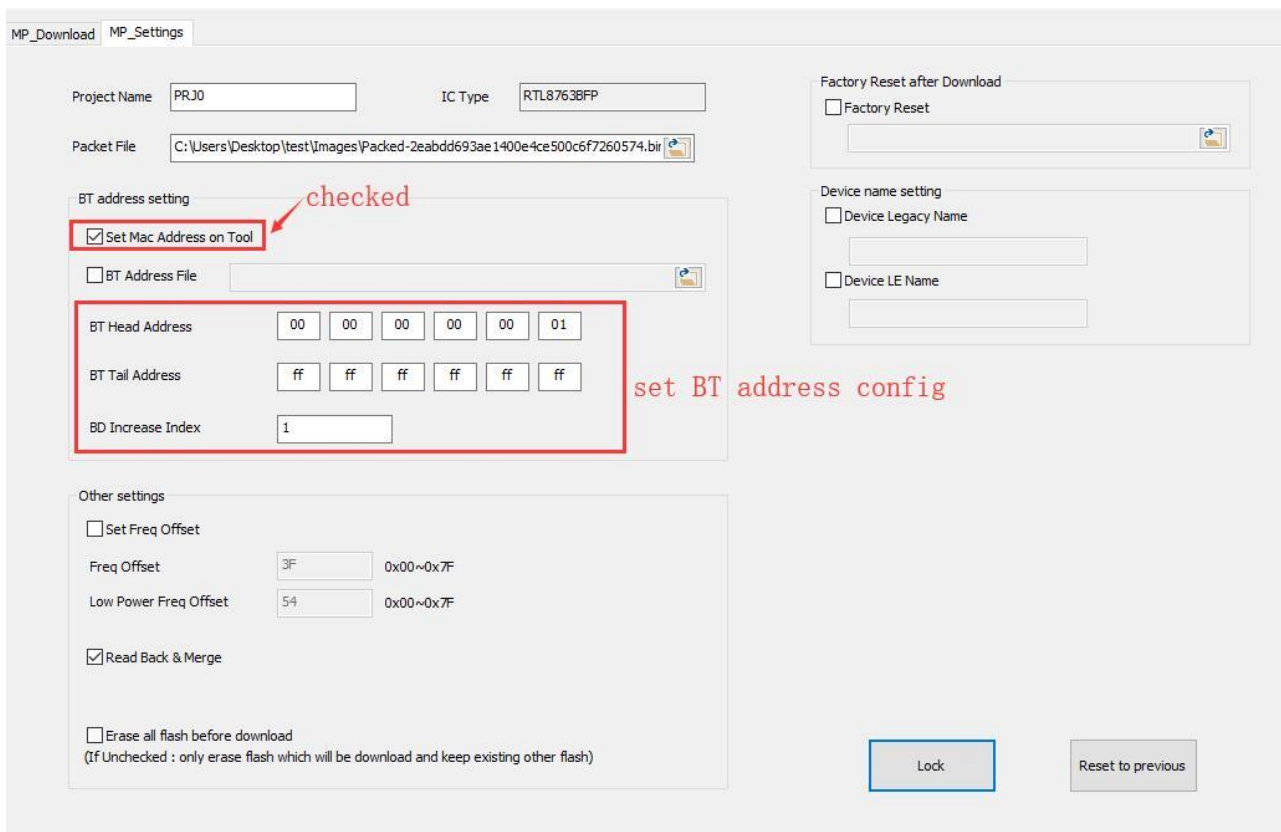


Figure 2-9 Tool manage BT address and use tool set parameter

- 1) Configure by filling addresses on UI, please do the following steps (Figure 2-9):
 - a) Check the “Set Mac Address on Tool”.
 - b) Configure “BT Head address” and “BT Tail Address”, the “BT Tail Address” should be greater than “BT Head Address”.
 - c) Set “BT Increase Index”, the “BT Increase Index” should be in the range from 1 to 99.

If you choose this way, in the following MP Download procedure, BT address per chip will be manipulated from “BT Head Address” to “BT Tail Address”, by the step of “BT Increase index”.
- 2) Configure by providing an imported source file, just check “Set Mac Address on Tool” and “BT Address File”, then select BT Address source file.

If you choose this way, in the following MP Download procedure, BT address per chip will be got from BT imported source file you selected, as shown in Figure 2-10.

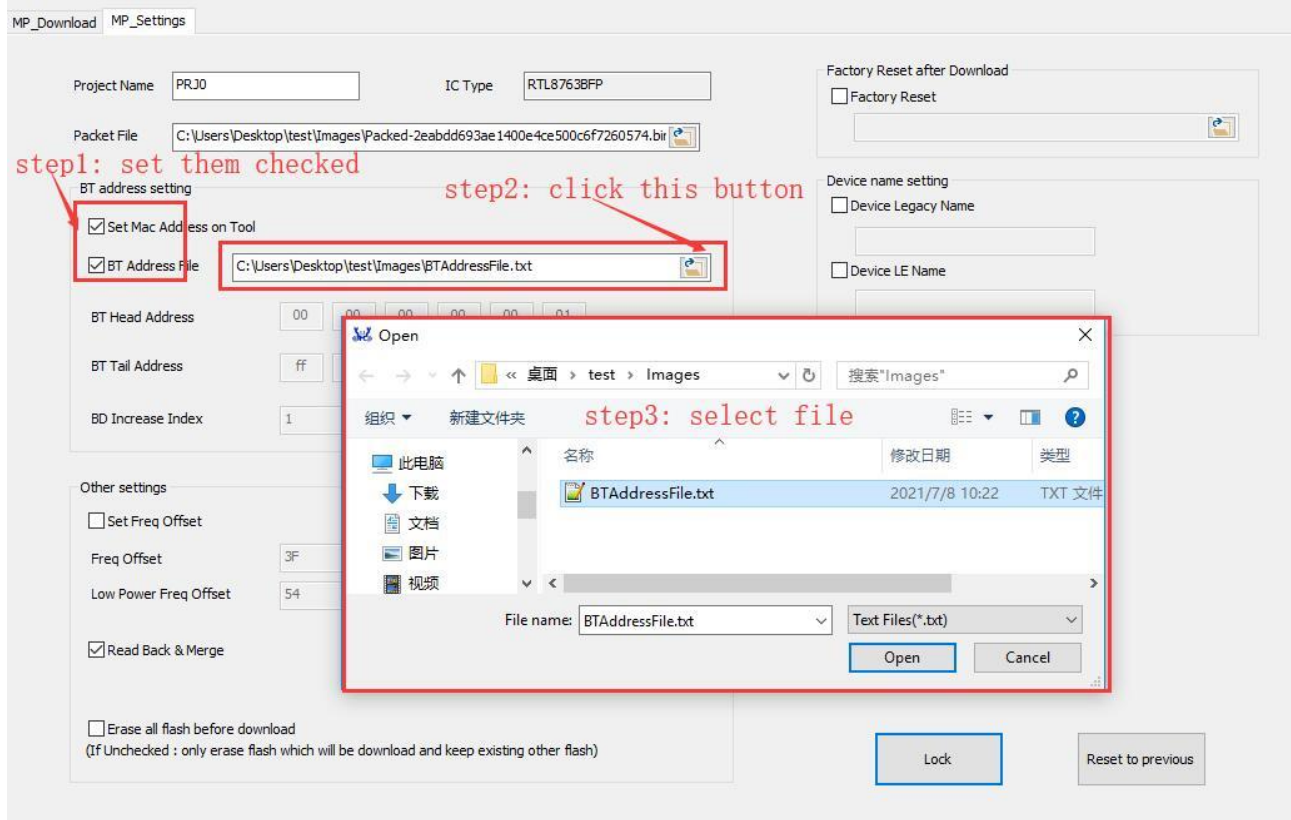


Figure 2-10 Tool manage BT address and use imported txt file

The BT Address source file should be formatted like this:

```

BTAddress.txt - Notepad
File Edit Format View Help
0x112233120040
0x11223312003f
0x11223312003d
0x11223312003c
0x11223312003b
0x11223312003a
0x112233120039
    
```

Figure 2-11 Imported BT address file format

3. Fail address reuse

Some ports' download procedure may fail due to some unexpected errors. The tool will save "fail address" in "BTAddress.txt" in MPPGTool.exe's folder during PG procedure, and reuse "fail address" got from "BTAddress.txt" firstly in the next PG procedure. After the "fail address" got from "BTAddress.txt" is used up, the next BT address acquisition depends on which way you choose to configure BT address setting in previous item 2. BT address manage flow under this scenario is shown below in Figure 2-12.

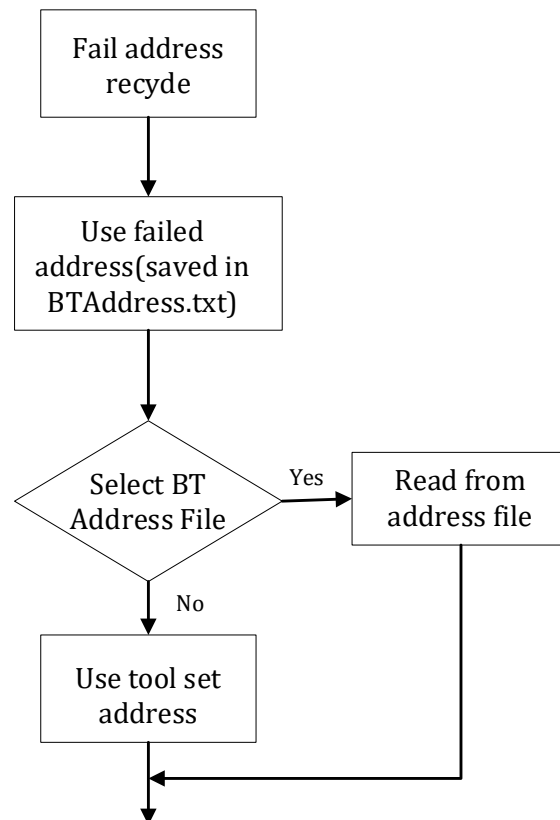
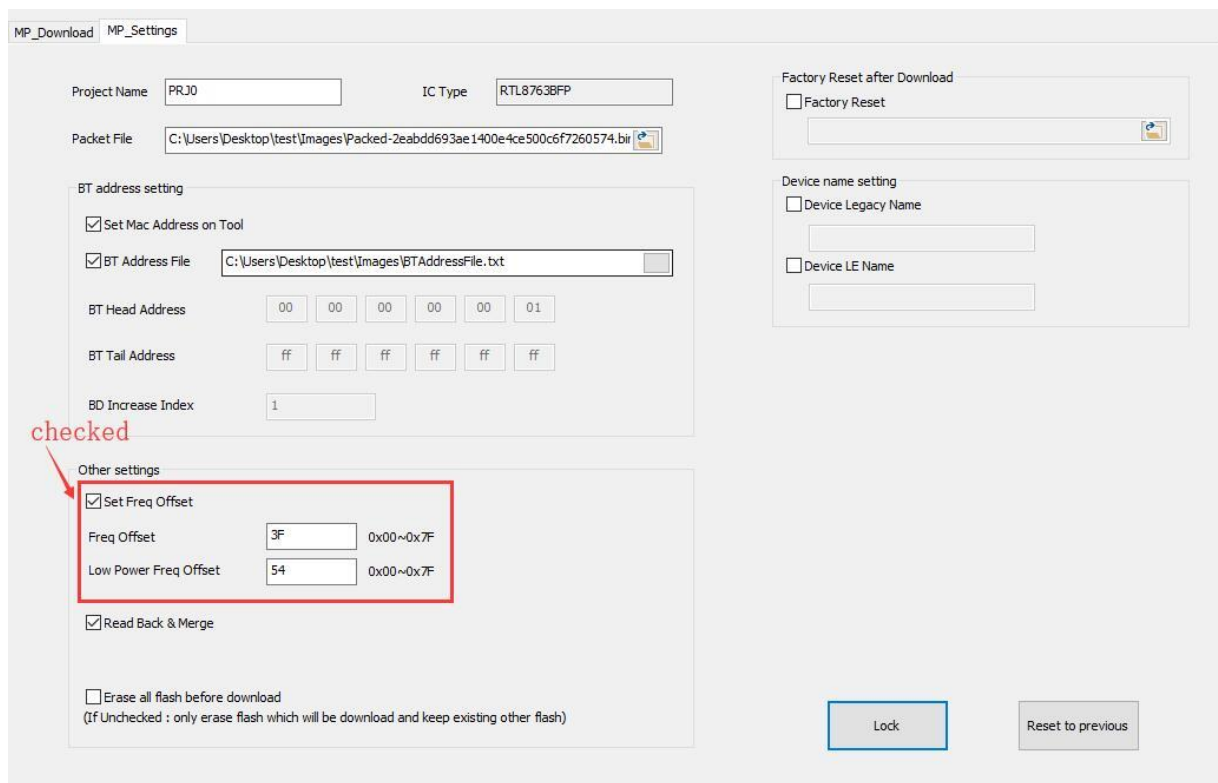


Figure 2-12 BT address manage flow

D) Frequency offset



MP_Download MP_Settings

Project Name: PRJ0 IC Type: RTL8763BFP

Packet File: C:\Users\Desktop\test\Images\Packed-2eabdd693ae1400e4ce500c6f7260574.bir

BT address setting

☒ Set Mac Address on Tool

☒ BT Address File: C:\Users\Desktop\test\Images\BTAddressFile.txt

BT Head Address: 00 00 00 00 00 01

BT Tail Address: ff ff ff ff ff ff

BD Increase Index: 1

Other settings

☒ Set Freq Offset

Freq Offset: 3F 0x00~0x7F

Low Power Freq Offset: 54 0x00~0x7F

☒ Read Back & Merge

☐ Erase all flash before download
(If Unchecked: only erase flash which will be download and keep existing other flash)

Factory Reset after Download

☐ Factory Reset

Device name setting

☐ Device Legacy Name

☐ Device LE Name

Lock Reset to previous

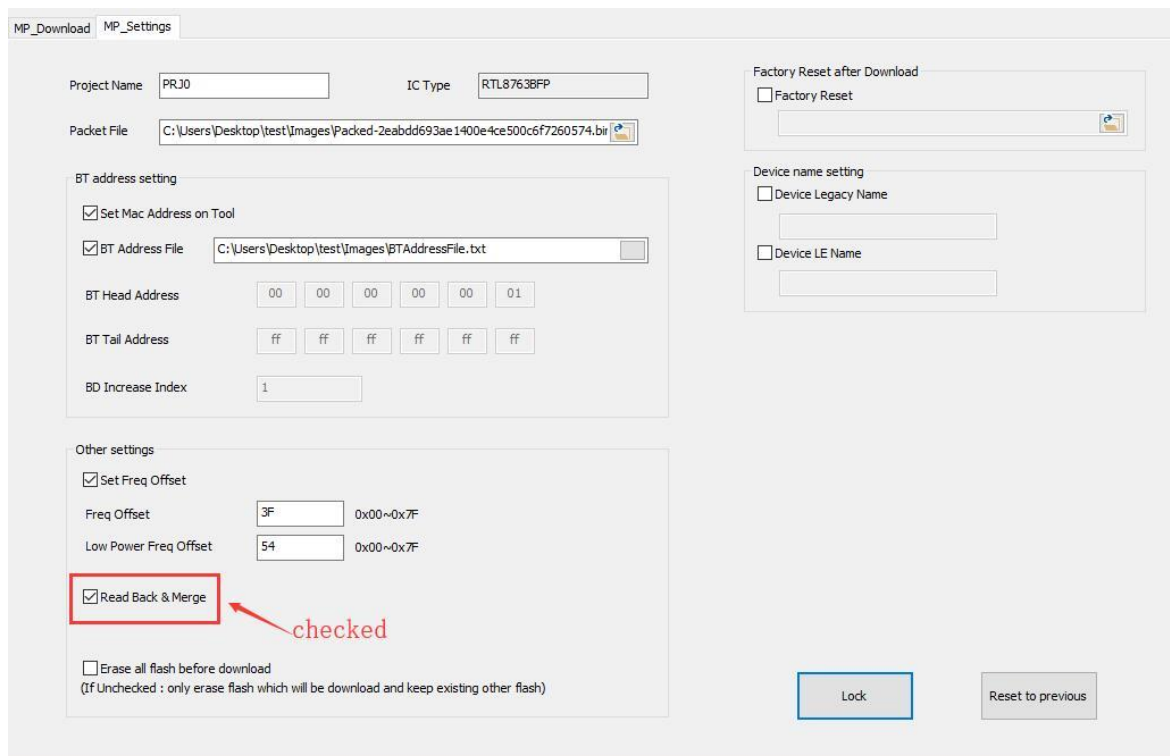
Figure 2-13 Set frequency offset

If you want to set frequency offset, please check the “Set Freq Offset” and input hexadecimal value(range from 0x0 to 0x7F). Out of range input will be limited to maximum or minimum available value (Figure 2-13).

If there is no need to set frequency offset in MP Download procedure, just uncheck “Set Freq offset”.

E) Merge back

If you need to keep parameters (e.g. “BT Address”, “Freq Offset”) configured in previous stage(e.g. MP Tests), check the “Read Back & Merge”, as shown in Figure 2-14.



The screenshot shows the 'MP_Settings' tab in the MPPG Tool. The 'Read Back & Merge' checkbox is checked and highlighted with a red box. A red arrow points to it with the word 'checked' written next to it. Other settings include Project Name (PRJ0), IC Type (RTL8763BFP), and various address fields.

Figure 2-14 Read Back and Merge

Attention:

Assume that “Read Back & Merge” is checked. In “MP Download” tab, you may use “Chip erase” button or set “Erase Entire Chip Before download” checked, it will cause different consequences as below:

- 1) Click “Chip erase” button firstly and then click “Download”, “Read Back & Merge” procedure will not actually take effect, because parameters set in previous stage will be erased firstly.
- 2) Set “Erase Entire Chip Before download” checked and click “Download”, “Read Back & Merge” will take effect.

More detailed instructions will be described in [MP Download](#).

F) Device name setting

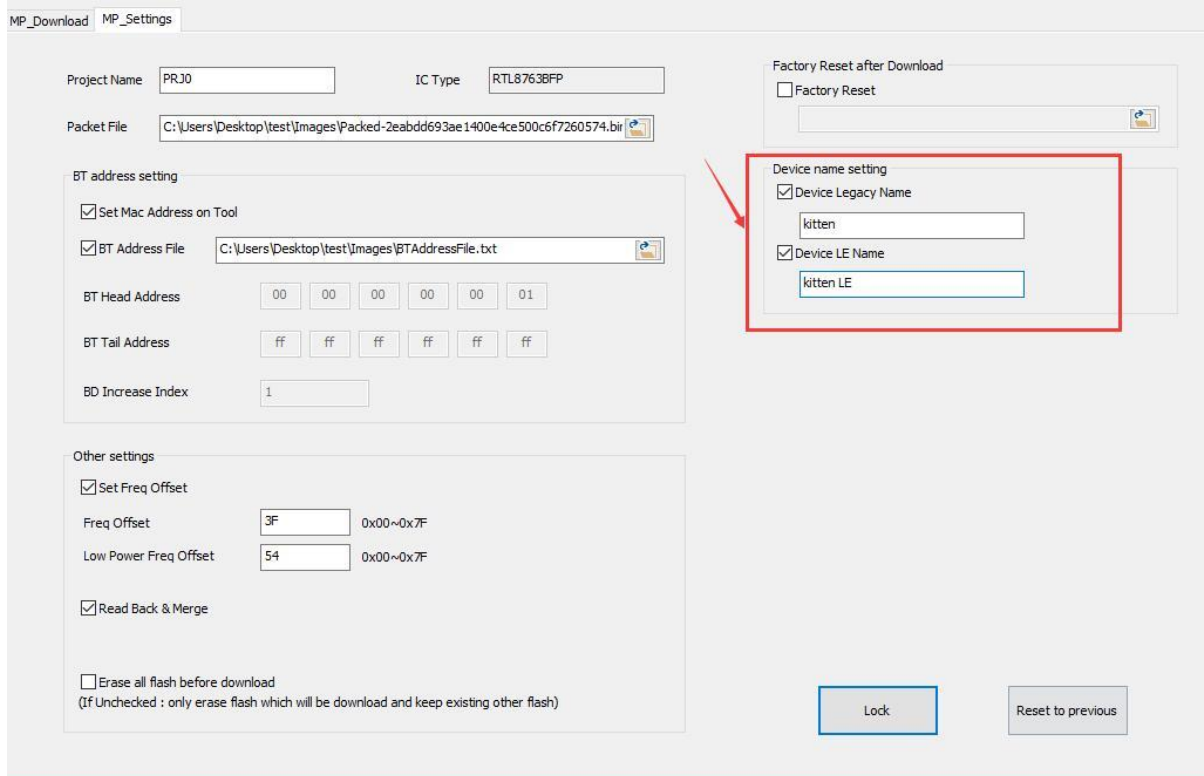


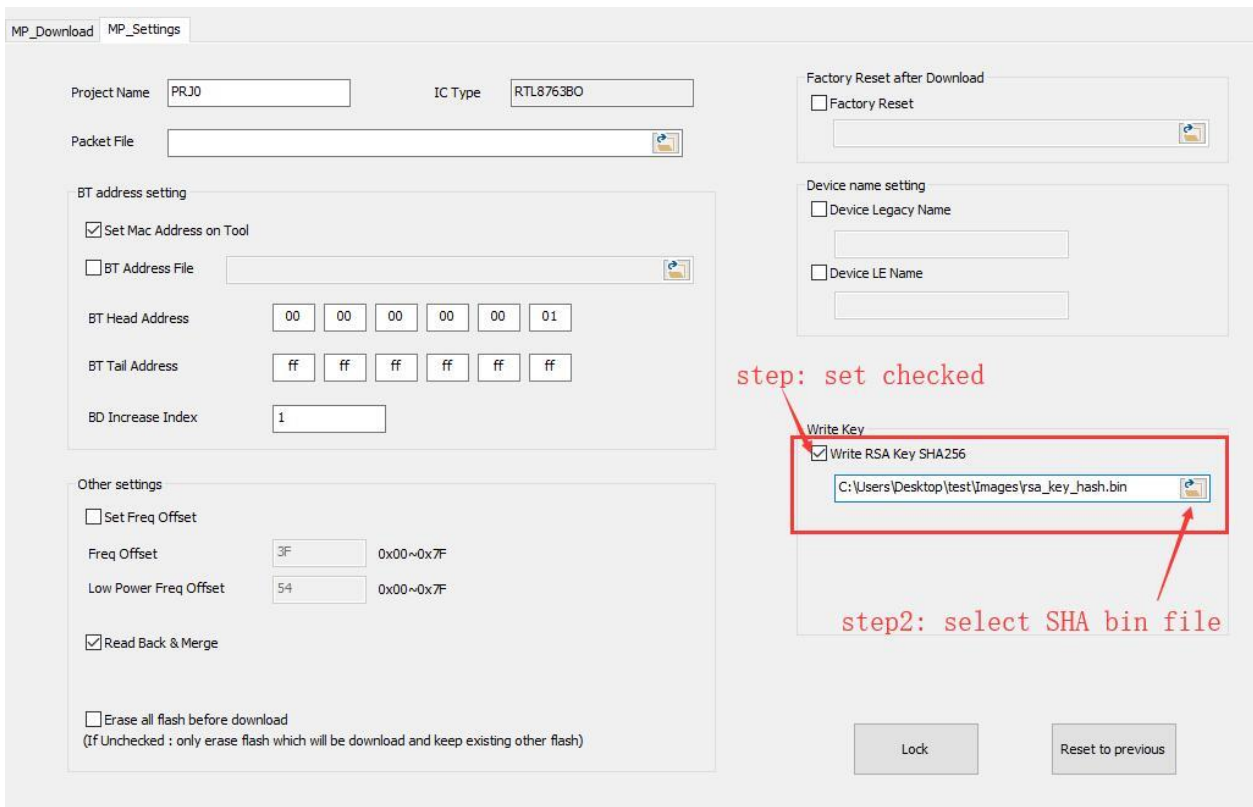
Figure 2-15 Device name setting

The device legacy name and device LE name could be setting in this block, you can only set one, or all of them.

If you want to configure them, check the checkbox and fill in the name (Figure 2-15), otherwise just set unchecked.

G) Write RSA Key SHA256

For some secure chips which need to write RSA Key SHA256 into efuse, the tool provides function of writing RSA Key SHA256 into efuse by importing a valid SHA bin file(Figure 2-16).



The screenshot shows the 'MP_Settings' tab of the MPPG Tool. The 'Project Name' is 'PRJ0' and 'IC Type' is 'RTL8763B0'. The 'BT address setting' section has 'Set Mac Address on Tool' checked. The 'Other settings' section has 'Read Back & Merge' checked. The 'Write Key' section has 'Write RSA Key SHA256' checked, and a file path 'C:\Users\Desktop\test\images\rsa_key_hash.bin' is selected. Red annotations highlight 'step: set checked' and 'step2: select SHA bin file'.

Figure 2-16 Writing RSA Key SHA256

Attention:

- 1) The SHA bin file must be corresponding to the private RSA key which used to re-sign sub-images.
- 2) If one chip is already written RSA Key SHA256 into efuse, don't write different RSA Key SHA256 info into efuse, otherwise the SHA256 field in efuse will be disordered and the chip will never run successfully.
- 3) RTL87X3E chips must use VBAT (battery) power in key write procedure.

If "Write RSA Key SHA256" is checked and import a SHA bin file, in the MP download procedure tool will check SHA information first. SHA information check flow is as follows:

1. Check SHA information from imported bin file

If imported SHA bin file is opened failed or checked invalid, tool will pop up an error message box (Figure 2-17 & Figure 2-18).

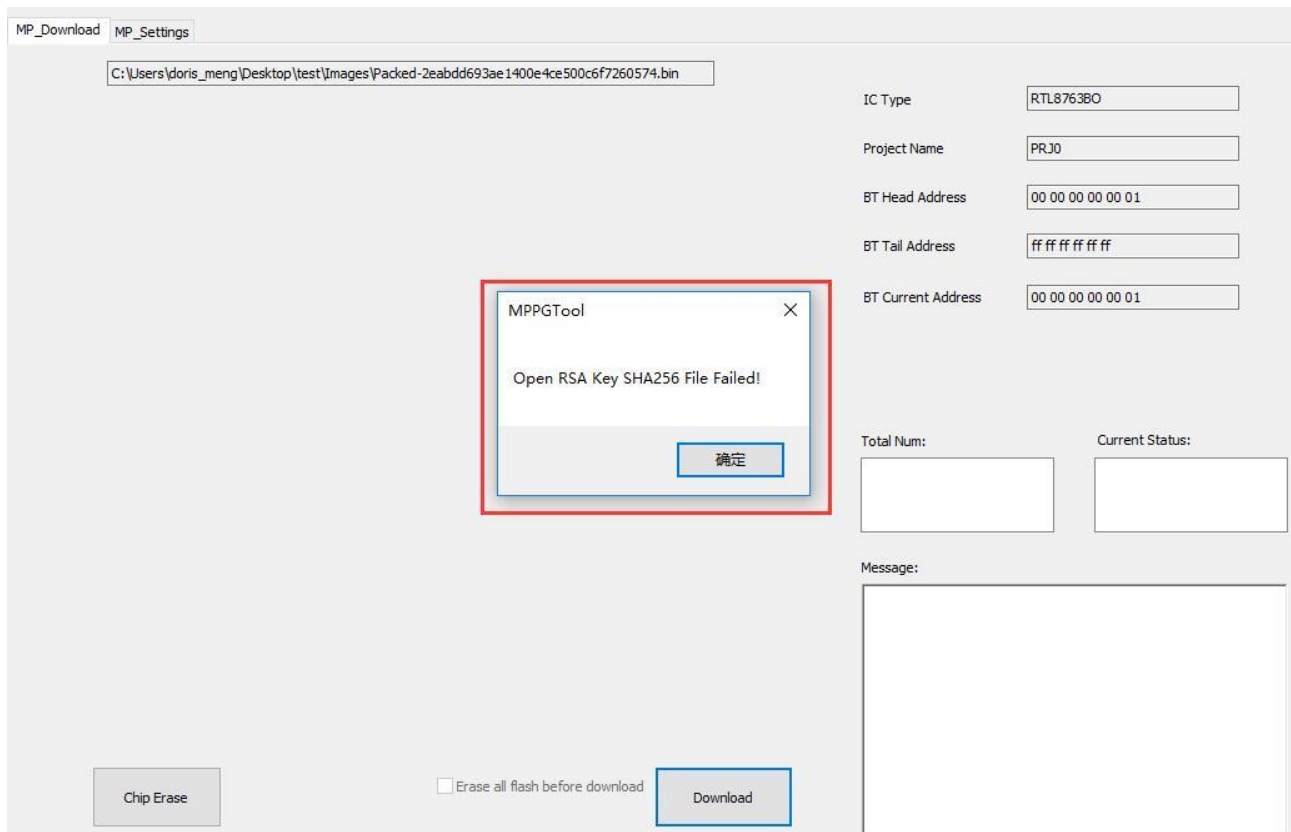


Figure 2-17 SHA bin file open failed

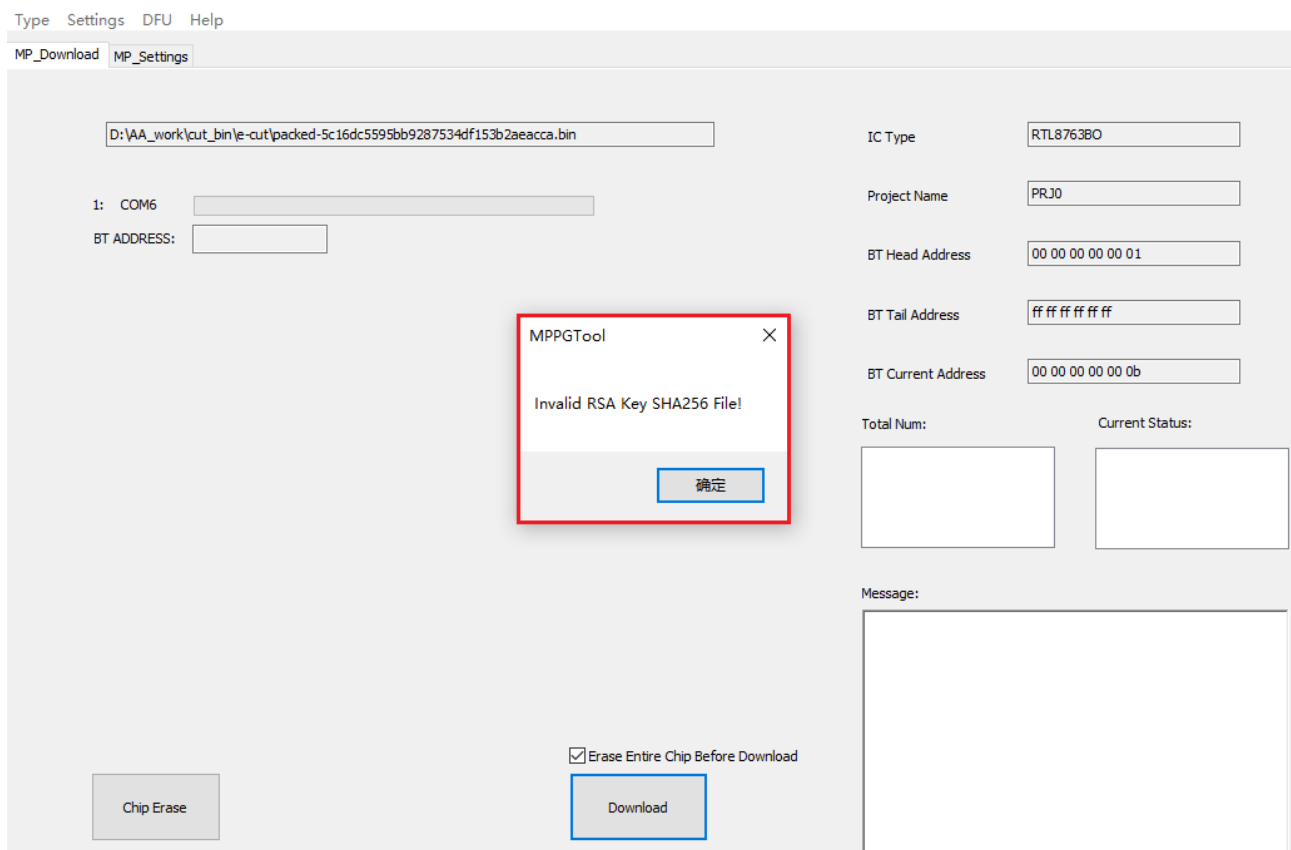


Figure 2-18 SHA bin file invalid

2. Check secure chip enabled

If imported SHA bin file is valid, tool will check whether the chip is secure boot enabled.

If the chip is secure boot disabled, indicate that the chip not allowed to write SHA information into efuse. Tool will print an error message (Figure 2-19).

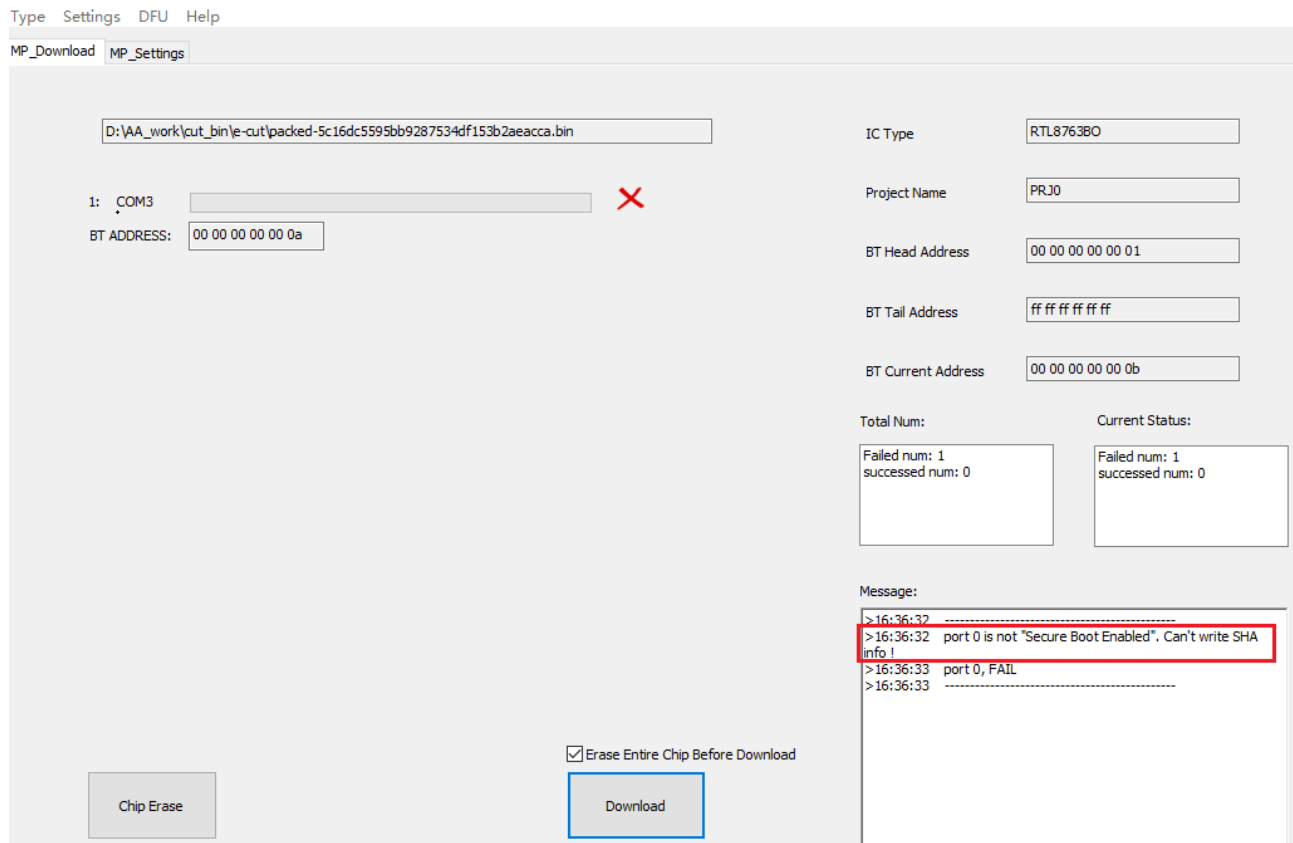


Figure 2-19 Forbid to write SHA info

3. Check SHA information between efuse read back SHA and imported bin file

If imported SHA bin file is valid and chip is secure boot enabled, tool will read back SHA information from efuse and check them with the imported SHA bin file.

- 1) If SHA information read back from efuse is invalid or conflict with the imported SHA bin file, tool will pop up an error message box (Figure 2-20).

Type
Settings
DFU
Help

MP_Download
MP_Settings

D:\AA_work\cut_bin\le-cut\packed-5c16dc5595bb9287534df153b2aeacca.bin

IC Type
RTL8763BO

Project Name
PRJ0

BT Head Address
00 00 00 00 00 01

BT Tail Address
ff ff ff ff ff ff

BT Current Address
00 00 00 00 00 06

Total Num:
Failed num: 1
succeeded num: 0

Current Status:
Failed num: 1
succeeded num: 0

Message:

```

>15:29:48
>15:29:48 port 0, SHA Conflict Error !
>15:29:48 port 0, FAIL
>15:29:48

```

☐ Erase Entire Chip Before Download

Chip Erase
Download

Figure 2-20 Conflict SHA info

- 2) If SHA information read back from efuse is valid and is the same with the imported SHA bin file, tool just enter into PG procedure and skip writing SHA into efuse because the chip is already written the same SHA information.
- 3) If SHA information read back from efuse is empty, indicate that the chip is never written SHA information into efuse before, so tool will enter into formal PG procedure with SHA writing.

Additionally, only write SHA256 bin and bypass download pack bin are supported.

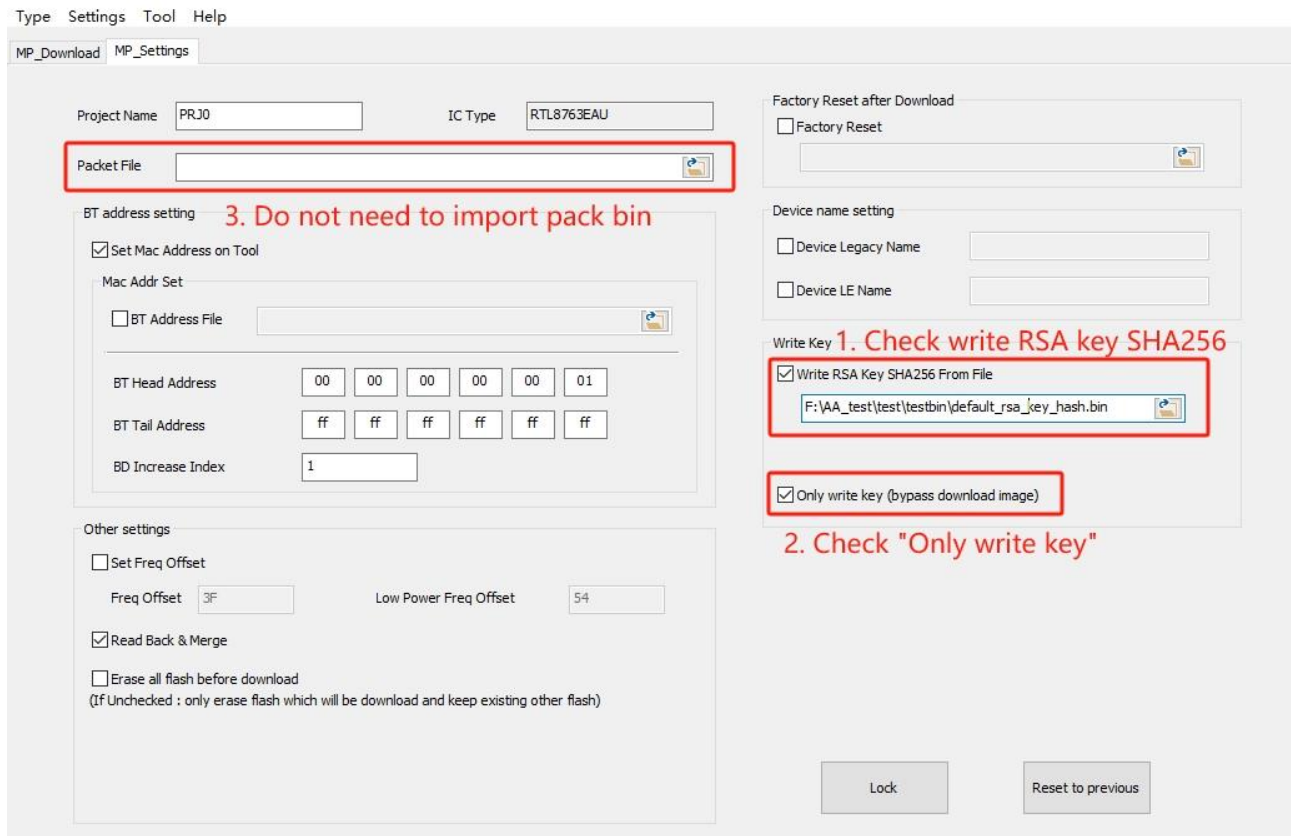


Figure 2-21 Only write RSA key SHA256

H) Enable One Wire Download

Some IC types of the RTL87X3E and RTL8773D series support the one wire download feature.

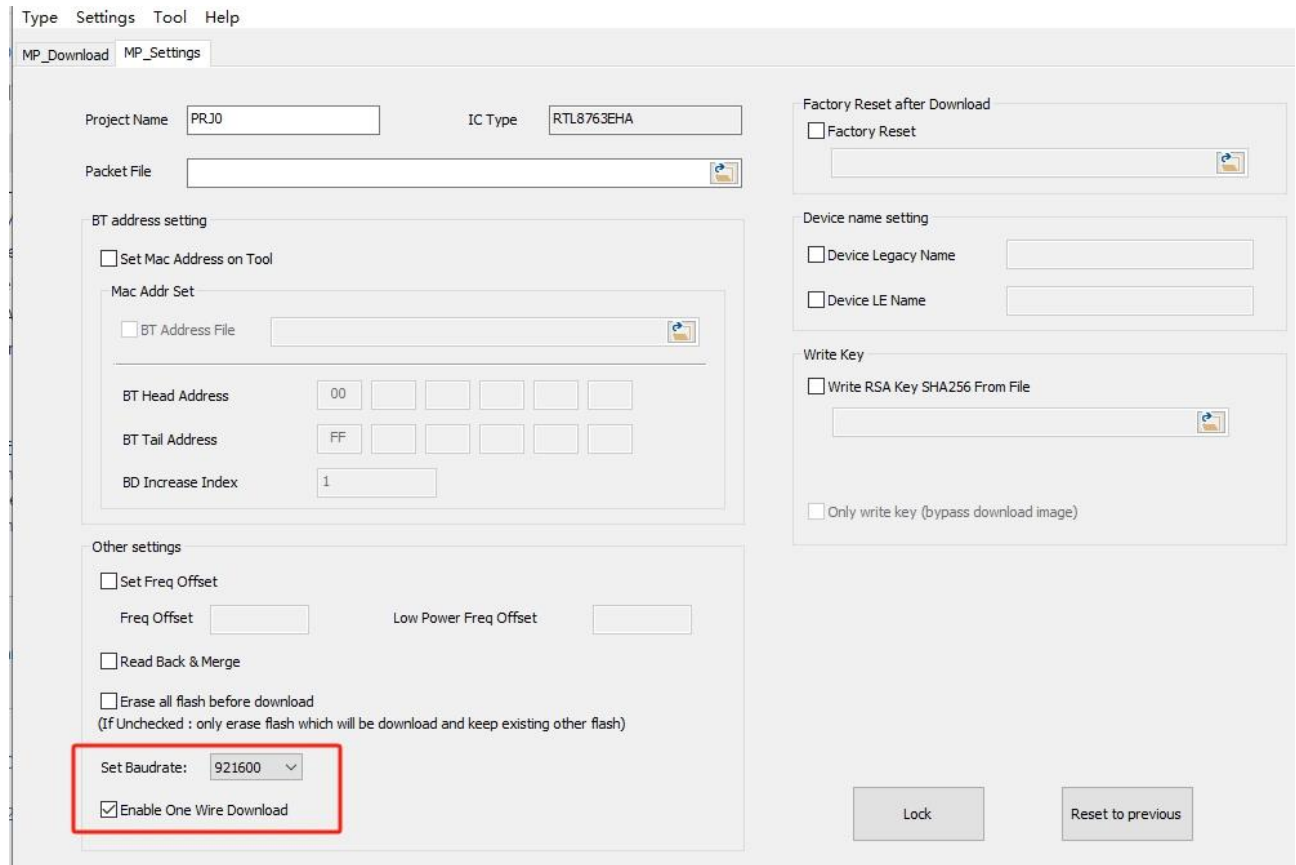
Attention:

- 1) Can't erase and write boot patch image if 'Enable One Wire Download' is checked.
- 2) 'Chip Erase' Button is not allowed to click in MP_Download page if 'Enable One Wire Download' checked in 'MP_Settings' page.
- 3) MPPGTOOL will send app reset command by clicking open button in one wire download mode, which will trigger SOC to reset to access the one wire download program. If the app on the SOC cannot run normally, and it is not in the state of automatic reset constantly, it is necessary to rely on other ways to make the IC reset to access the one wire download program after clicking the open button. After clicking the open button, wait for the SOC to reset to access the one wire download mode, the timeout is set to 20s.
- 4) Recommended to have two bank images burned before switching to one wire download mode.
- 5) The supported baud rates of the chip is dependent on the capacitance. Please choose the chip's supported baud rate.

One wire download flow is as follows:

1. In MP_Settings page, check 'Enable One Wire Download' (Figure 2-22) and configure other required settings.
2. After checking "Enable One Wire Download" checkbox, an option to select the baud rate will be

displayed. Set the appropriate baud rate.



The screenshot shows the 'MP_Settings' tab in the MPPG Tool. The 'Other settings' section contains the 'Enable One Wire Download' checkbox, which is checked and highlighted with a red rectangle. Other visible settings include 'Set Baudrate' set to 921600, 'Factory Reset after Download' (unchecked), 'Device name setting' (unchecked), and 'Write Key' (unchecked). The 'BT address setting' section includes options for 'Set Mac Address on Tool' and 'BT Address File'.

Figure 2-22 Check 'Enable One Wire Download' in MP_Settings page

3. Click the 'Download' button in MP_Download page (Figure 2-23).

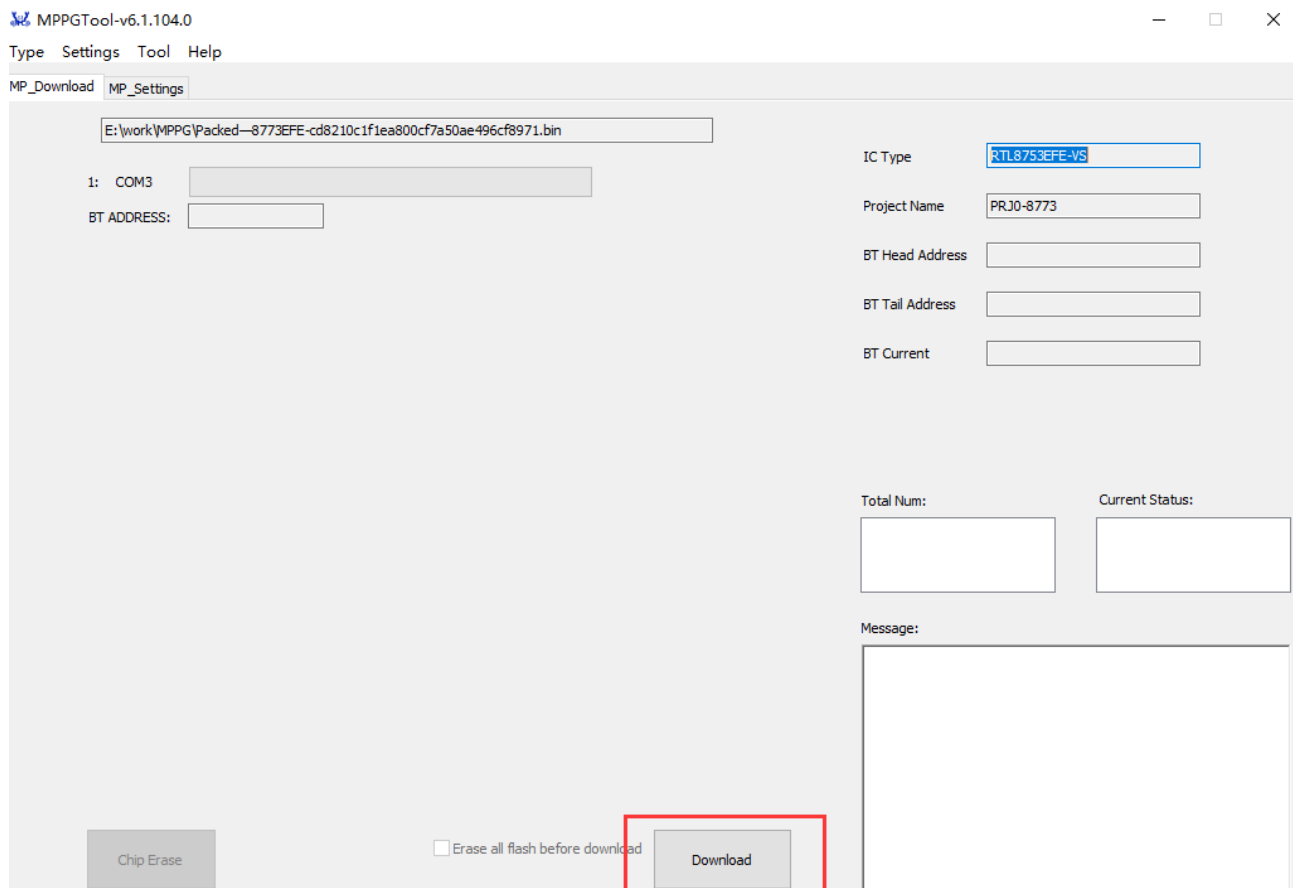


Figure 2-23 Click 'Download' Button in MP_Download page

2.3.2 MP Download

As shown in Figure 2-24, this is the “MP Download” interface.

Before download, make sure proper packet image file is selected on “MP setting” page, or a pop-up message box will telling you “Pack bin does not exists” or other error messages.

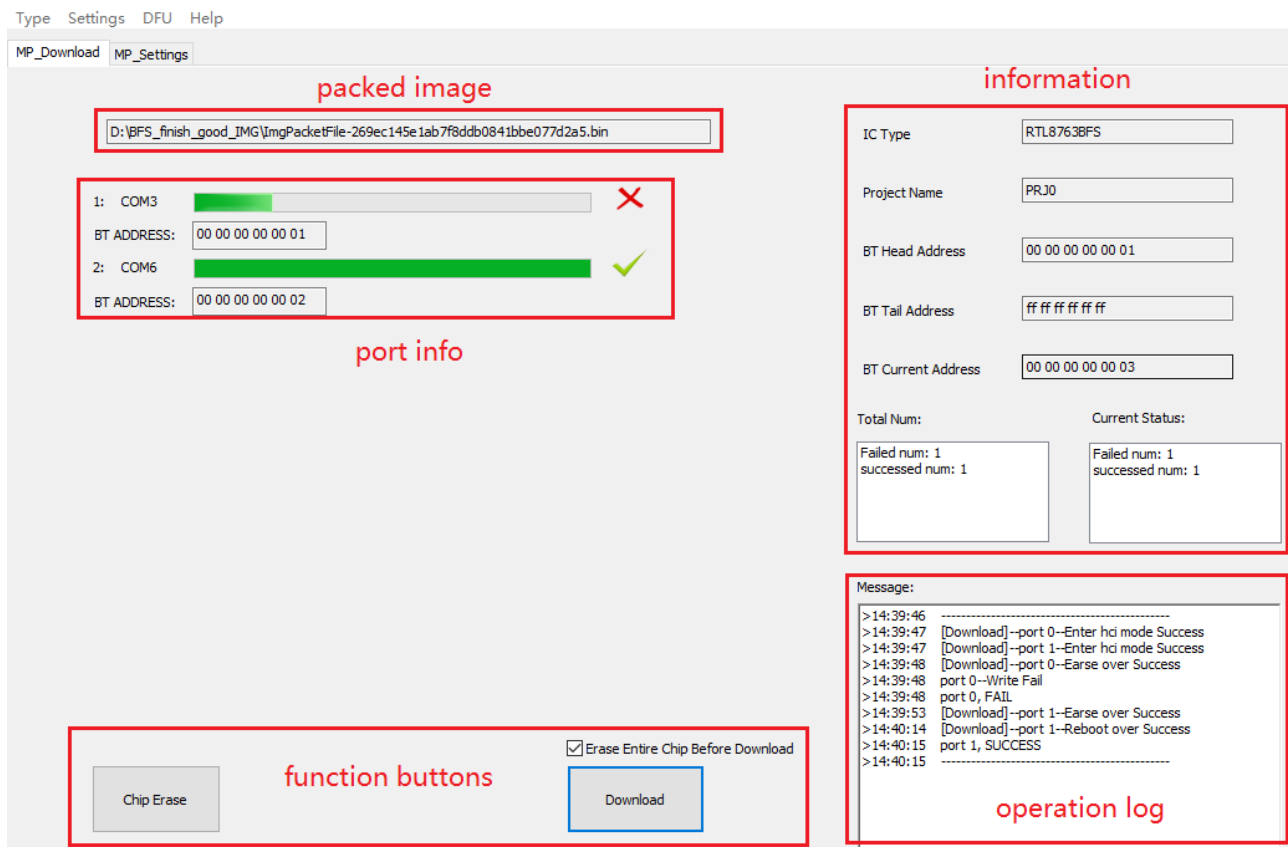


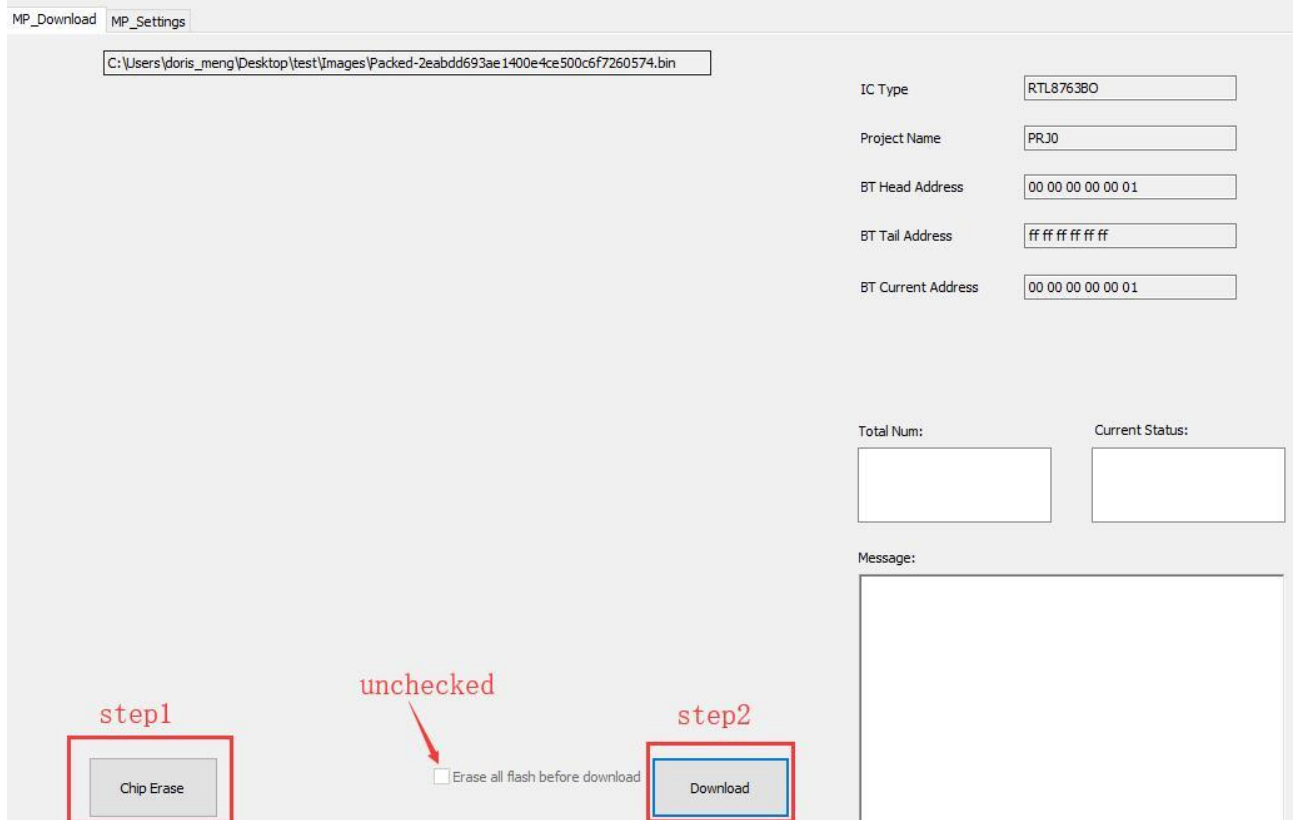
Figure 2-24 MP Download interface

Assume that you've already set some parameters (e.g. "BT Address", "Freq Offset") in previous stage, and you want to read back previous setting, please set "Read Back & Merge" checked on the "MP setting" page.

Under assumption above, if you also want to erase the entire chip, there are two kinds of download procedure, which have different results:

- 1) Click "Chip Erase" button firstly, then click "Download" button (Figure 2-25):
 - a) Click "Chip Erase" button will trigger entire chip erase, so all parameters set in previous stage(ex. parameter set in MP Tests) will be cleared;
 - b) Click "Download" download image to chip, "Read Back & Merge" will not take effect because parameters set in previous stage were already cleared.
- 2) Download with "Erase all flash Before download" checkbox checked (Figure 2-26):
 - a) Read back previous set parameters from flash;
 - b) Erase entire chip;
 - c) Merge flash read back parameters with packet file, then download to chips, "Read Back & Merge" will take effect.

If you do not need "Read Back & Merge" and uncheck it, the above two procedures will get the same result.



MP_Download | MP_Settings

C:\Users\doris_meng\Desktop\test\Images\Packed-2eabdd693ae1400e4ce500c6f7260574.bin

IC Type: RTL8763BO

Project Name: PRJ0

BT Head Address: 00 00 00 00 00 01

BT Tail Address: ff ff ff ff ff ff

BT Current Address: 00 00 00 00 00 01

Total Num:

Current Status:

Message:

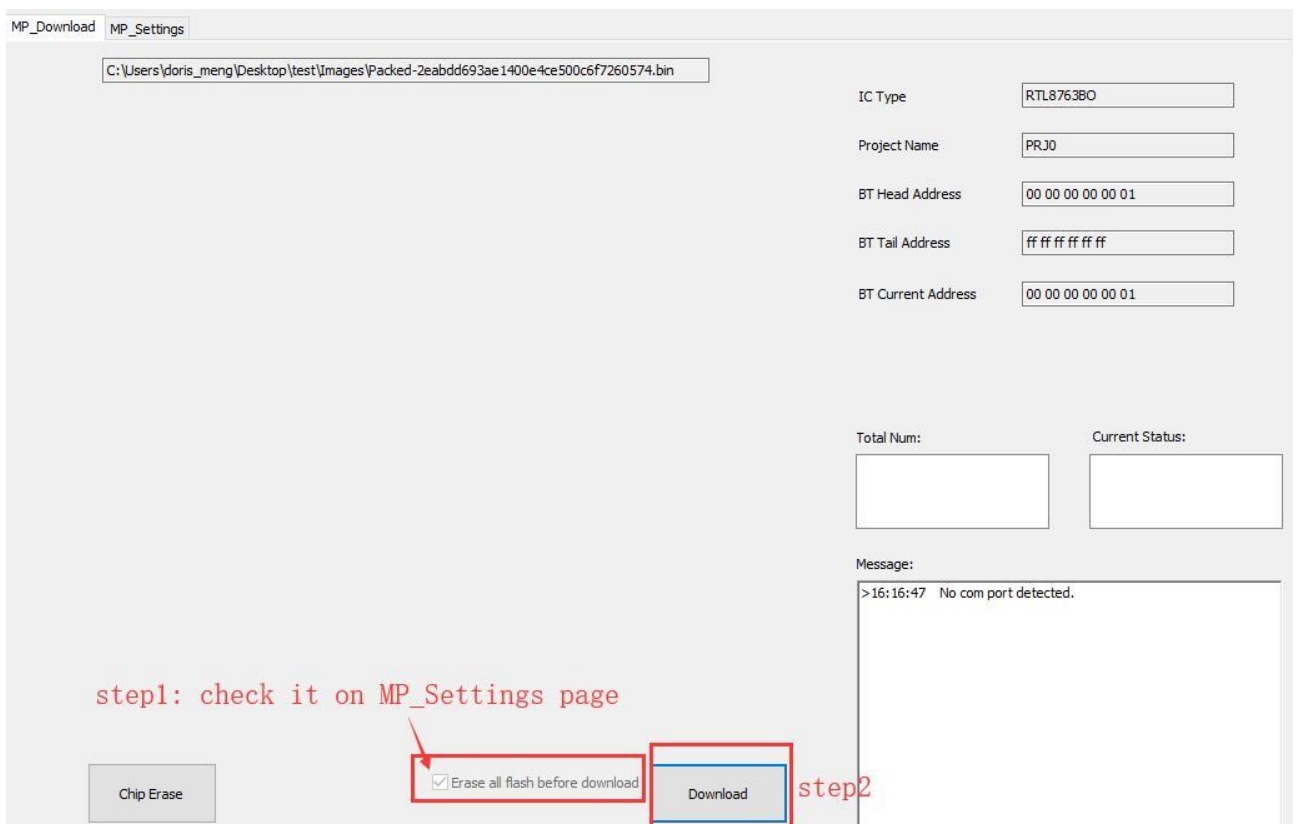
step1:

unchecked: ☐ Erase all flash before download

step2:

Figure 2-25 Chip erase button and Download

“Erase all flash Before download” checkbox is checked on the “MP setting” page.



MP_Download | MP_Settings

C:\Users\doris_meng\Desktop\test\Images\Packed-2eabdd693ae1400e4ce500c6f7260574.bin

IC Type: RTL8763BO

Project Name: PRJ0

BT Head Address: 00 00 00 00 00 01

BT Tail Address: ff ff ff ff ff ff

BT Current Address: 00 00 00 00 00 01

Total Num:

Current Status:

Message:

> 16:16:47 No com port detected.

step1: check it on MP_Settings page: ☒ Erase all flash before download

step2:

Figure 2-26 Erase Entire Chip Before download checkbox and Download

If you check “Set Mac Address on Tool”, it will manipulate BT address by tool itself.

Here are two scenarios:

1) Use “BT Head address”, “BT Tail address” with increase index “BD Increase Index”

As shown in Figure 2-27, on the information area, “BT Head Address”, “BT Tail Address” will show the BT address you set on “MP Setting” page, and “BT Current Address” will show the next BT address which is going to program down to chip.

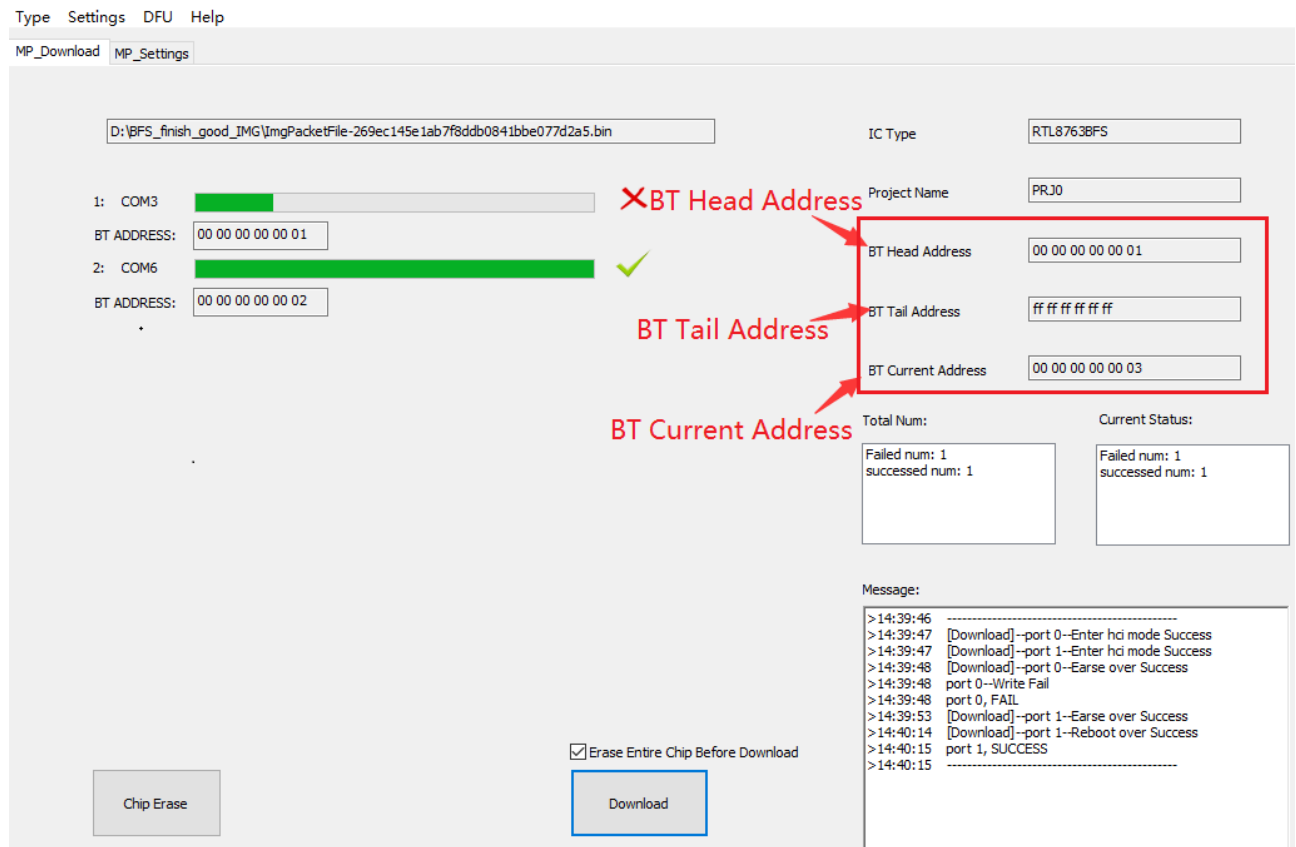


Figure 2-27 BT Address usage logic

Attention:

- 1) During MP Download procedure, “BT Current Address” grow by “BT Increase Index” regardless of downloading fail.
- 2) After MP Download procedure, Tool will save failed address. Then during the next PG procedure, it will reuse failed address. Until all failed addresses are used up, “BT Current Address” will automatically grow by “BT Increase Index” set on “MP Setting” page.

Failed addresses will be saved in “BTAddress.txt” in MPPGTool.exe’s folder as shown in Figure 2-28.

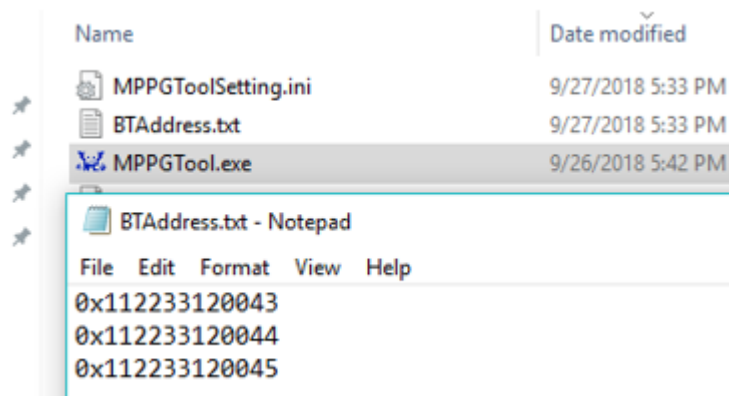


Figure 2-28 BT address file format

2) Use “BT Address File” to set BT address

BT address will automatically be loaded from BT address file, and the information area will not work in this scenario, as shown in Figure 2-29 below.

After PG procedure, the “fail address” and unused addresses will be saved in the same BT address file you imported and at the same time the used addresses will be deleted.

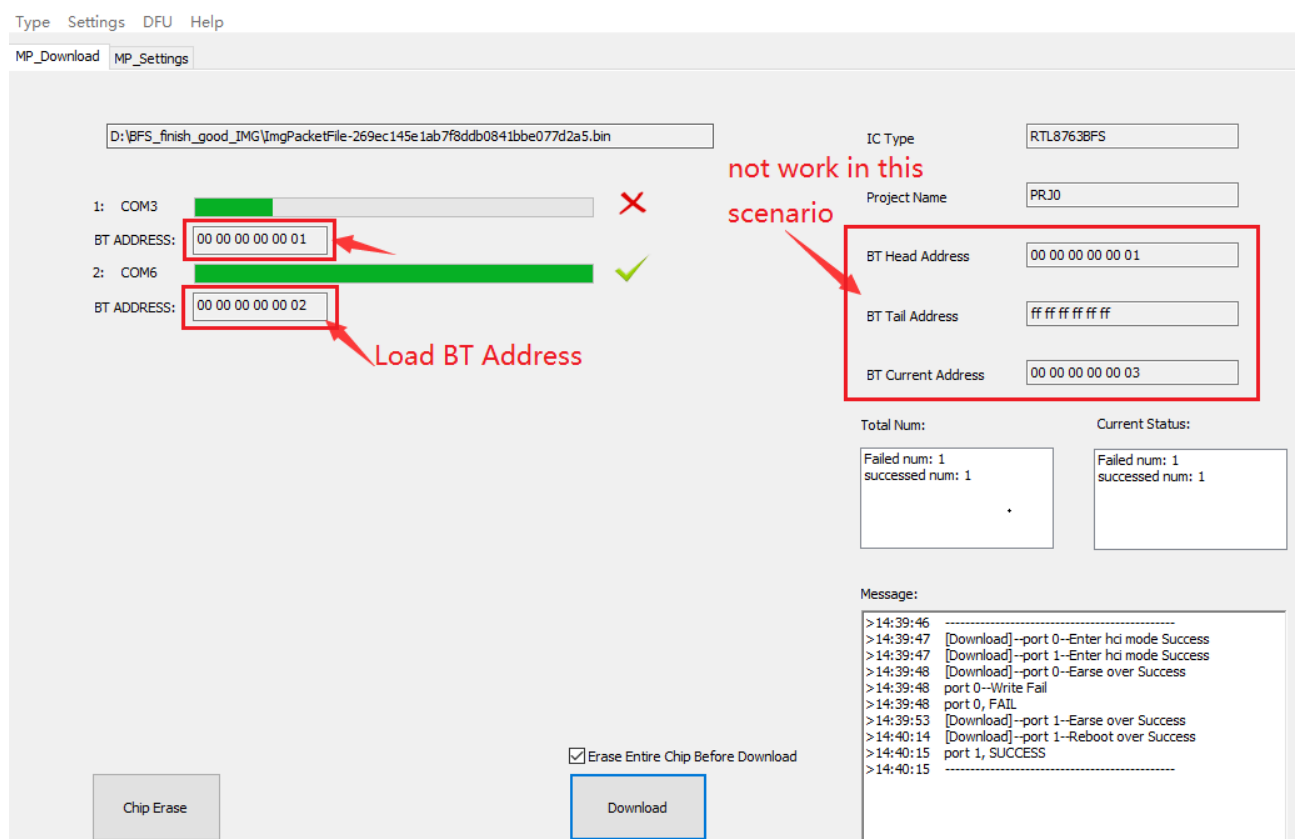


Figure 2-29 Use BT address file

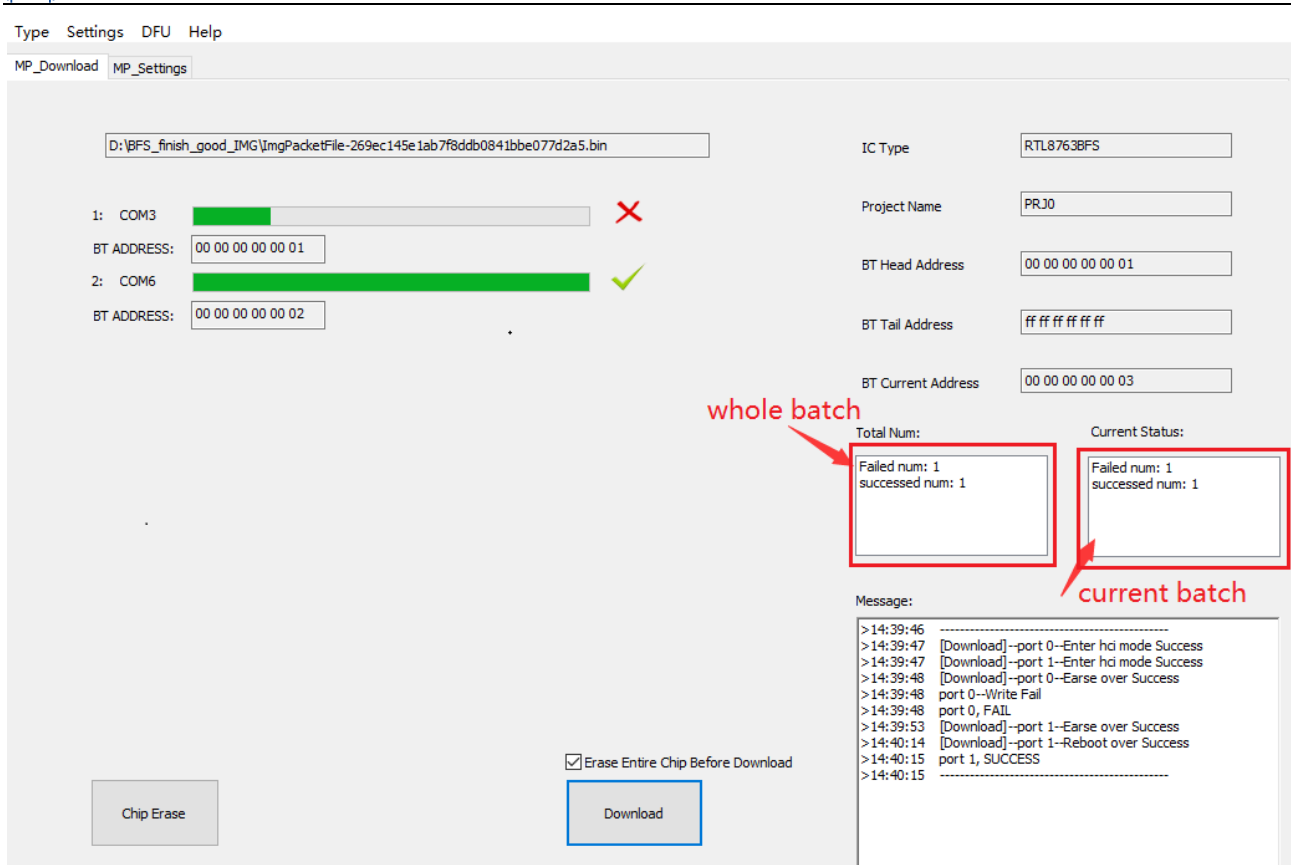


Figure 2-30 Fail and success number after download

In “MP Download” mode, you can know fail numbers of download in a whole batch or in current batch, as shown in Figure 2-30

Also detailed information will be saved in “Log” folder which is in MPPGTool.exe’s folder, it saved in file whose name is formatted like “MPLLogYYYY-MM-DD-HH-mm-ss.txt”. Take Figure 2-31 as an example:

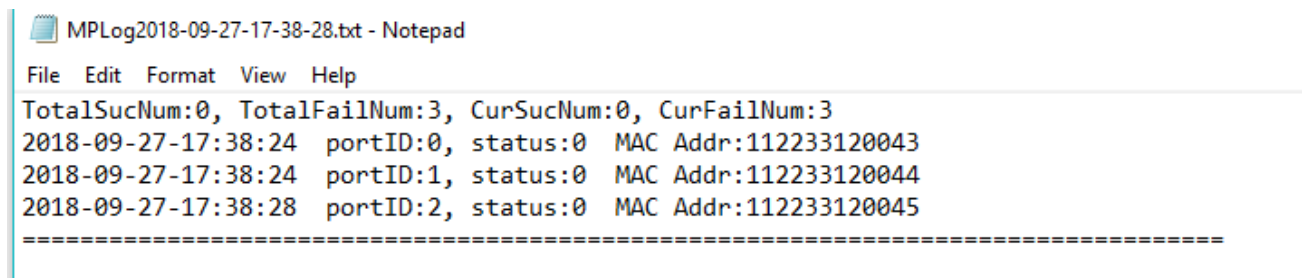


Figure 2-31 MP log format

“TotalSucNum” means success numbers in the whole batch;

“TotalFailNum” means fail numbers in the whole batch;

“CurSucNum” means success numbers in current batch;

“CurFailNum” means fail numbers in current batch.

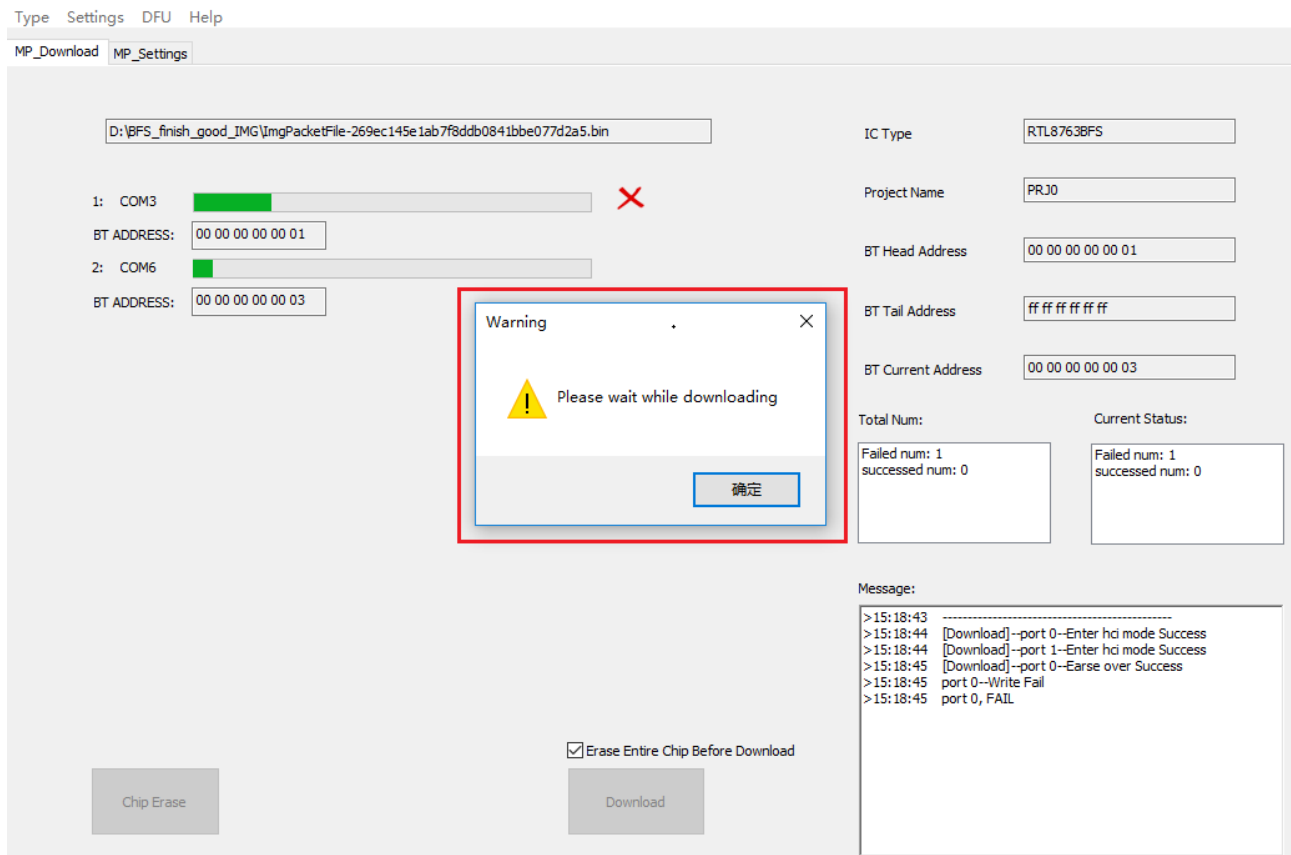


Figure 2-32 Warning message

Please don't try to switch to “Debug mode” or switch to “MP setting” while downloading image or erase entire chip, otherwise a message box shows “Please wait while downloading”, just like Figure 2-32.

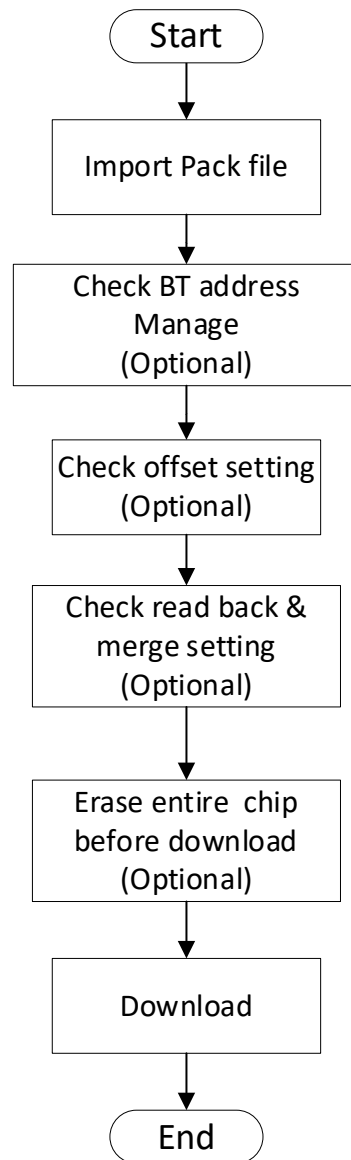


Figure 2-33 Download Selection

The commonly flow of download procedure in MP mode is shown in Figure 2-33.

2.4 RD Mode

In this mode, you can have more authority on operating than in MP mode. RD mode interface is shown in Figure 2-34.

For chips which support configurable flash layout, tool has an additional select box for “flash map.ini” importing, and the select box will not be shown on the RD mode interface.

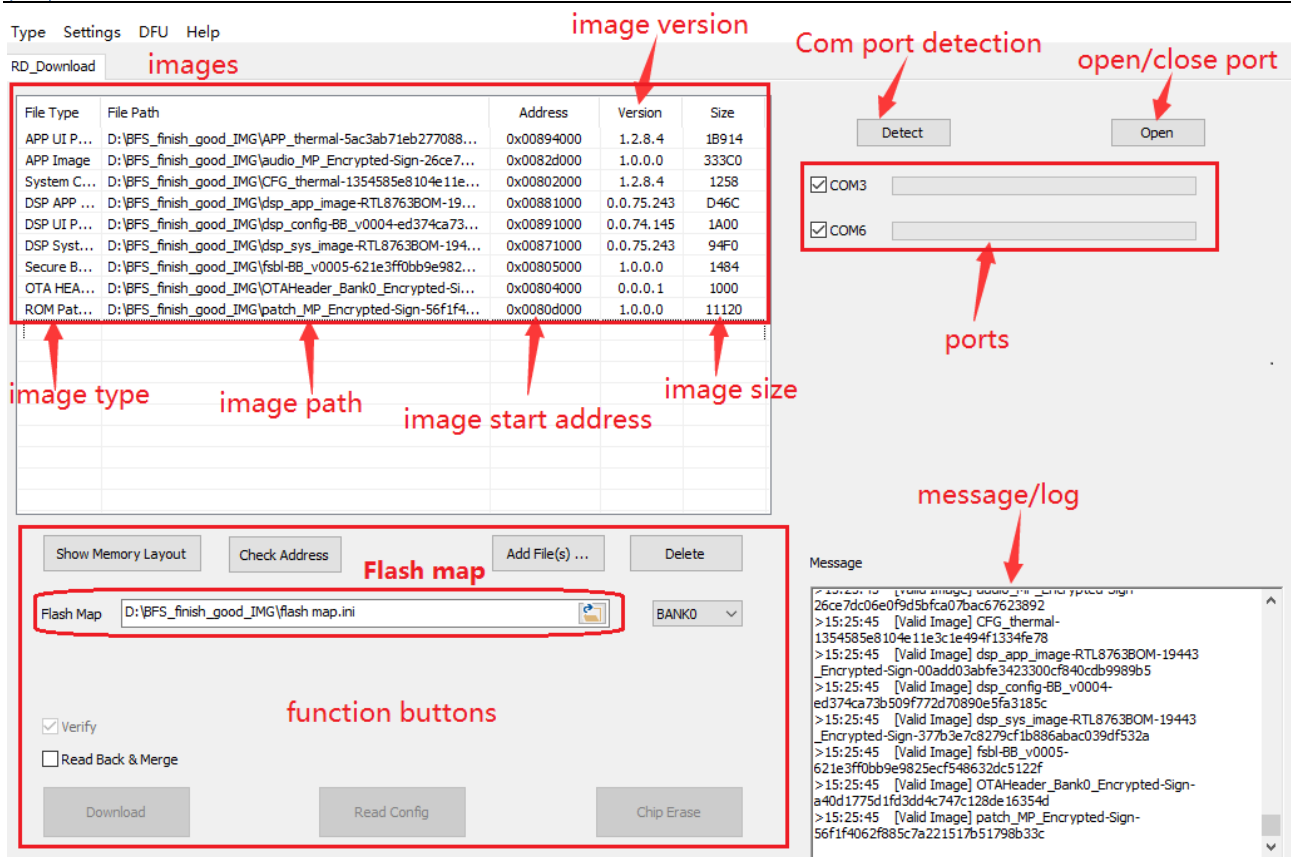


Figure 2-34 RD Download interface

2.4.1 Load image & Check image

A) Add image(s)

There are two methods to add image(s).

- 1) Click "Add File(s)..." as shown in Figure 2-35. An "Open" dialog will pop up and you can select one or several images at one time.
- 2) Double click "File Path" column in each row firstly, a folder icon will show out. You can type in the image path, or click the folder icon to add an image. As shown in Figure 2-36.

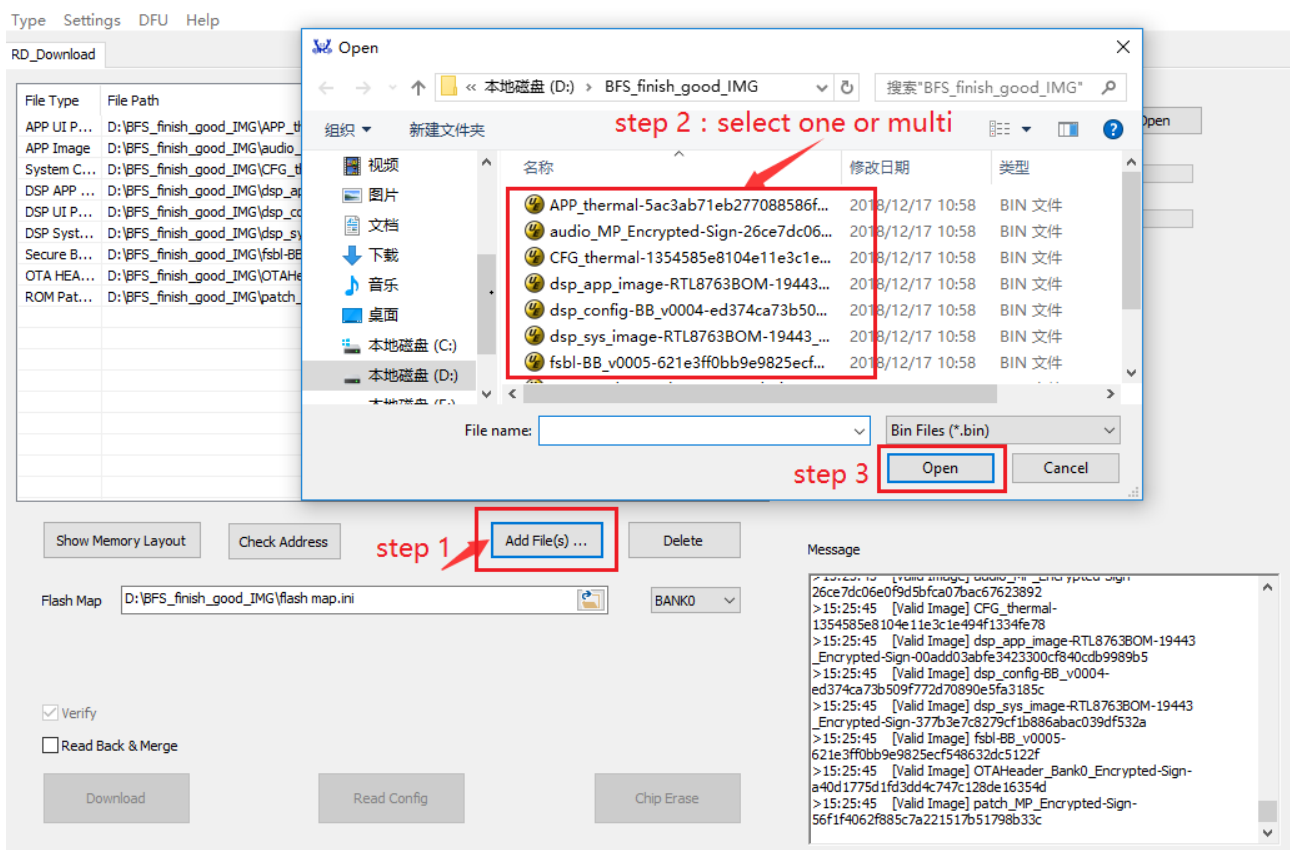


Figure 2-35 Select one or multi bin files

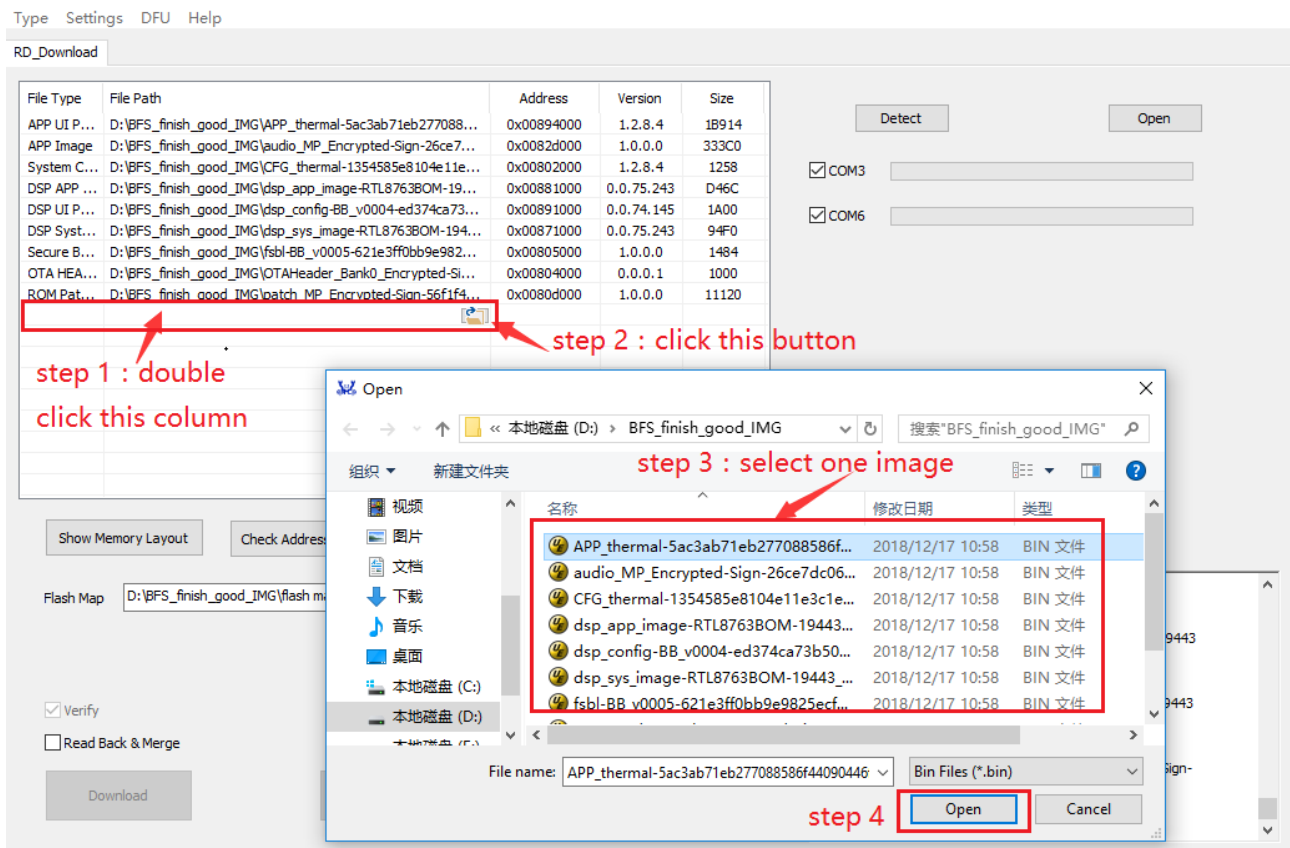


Figure 2-36 Add bin from file path

For chips which support configurable flash layout, it is required to import “flash map.ini” which provides flash address information of sub-images. If “flash map.ini” is not imported, the address info will be marked red in “Address” column.

B) Image validation check

After images is loaded, the application will trigger image validation check and address check automatically. Here are some incorrect situation:

- Inappropriate bin file

Images of inappropriate type will be marked red, and message log will output “Inappropriate bin file” (Figure 2-37).

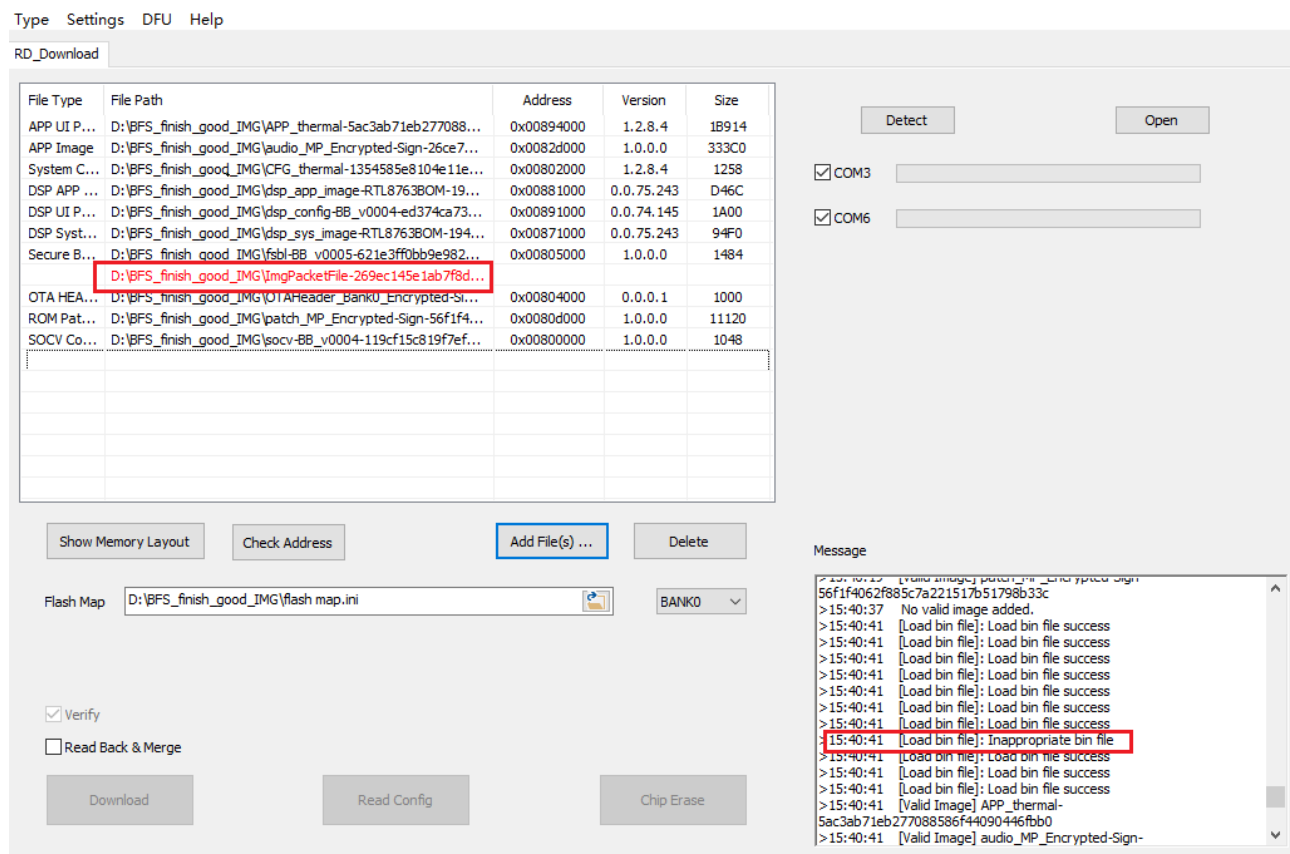


Figure 2-37 Inappropriate bin file

- Duplicated bin type

If the same bin type image has been loaded previously, the image of duplicated bin type will be marked red, and message log will output “Bin file already exist” (Figure 2-38).

- Valid address info

Also, some times in “Address” column, address info is marked red (Figure2-39), if this happens, please check address info or enter address manually and if your entered address is incorrect, some hints will show in the log/message area.

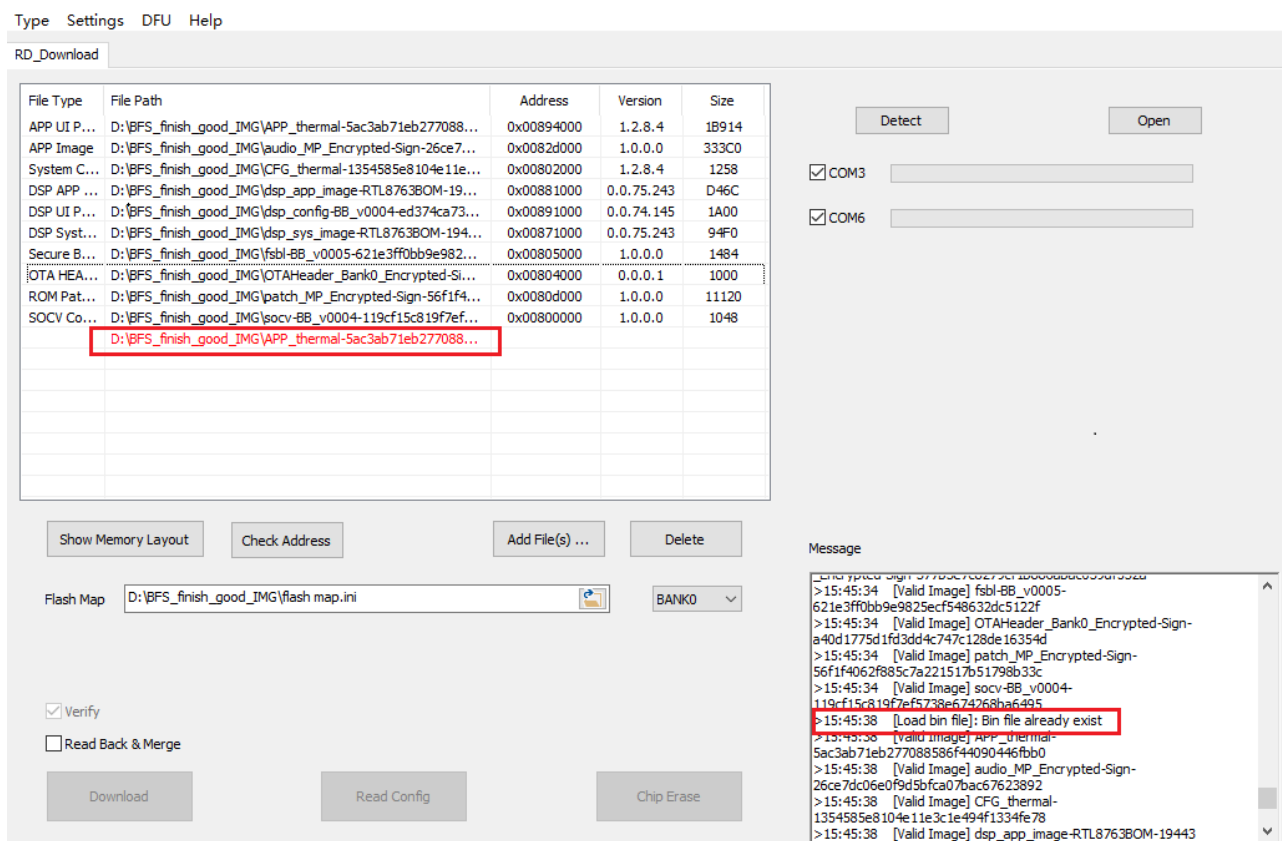


Figure 2-38 Duplicated bin already exist

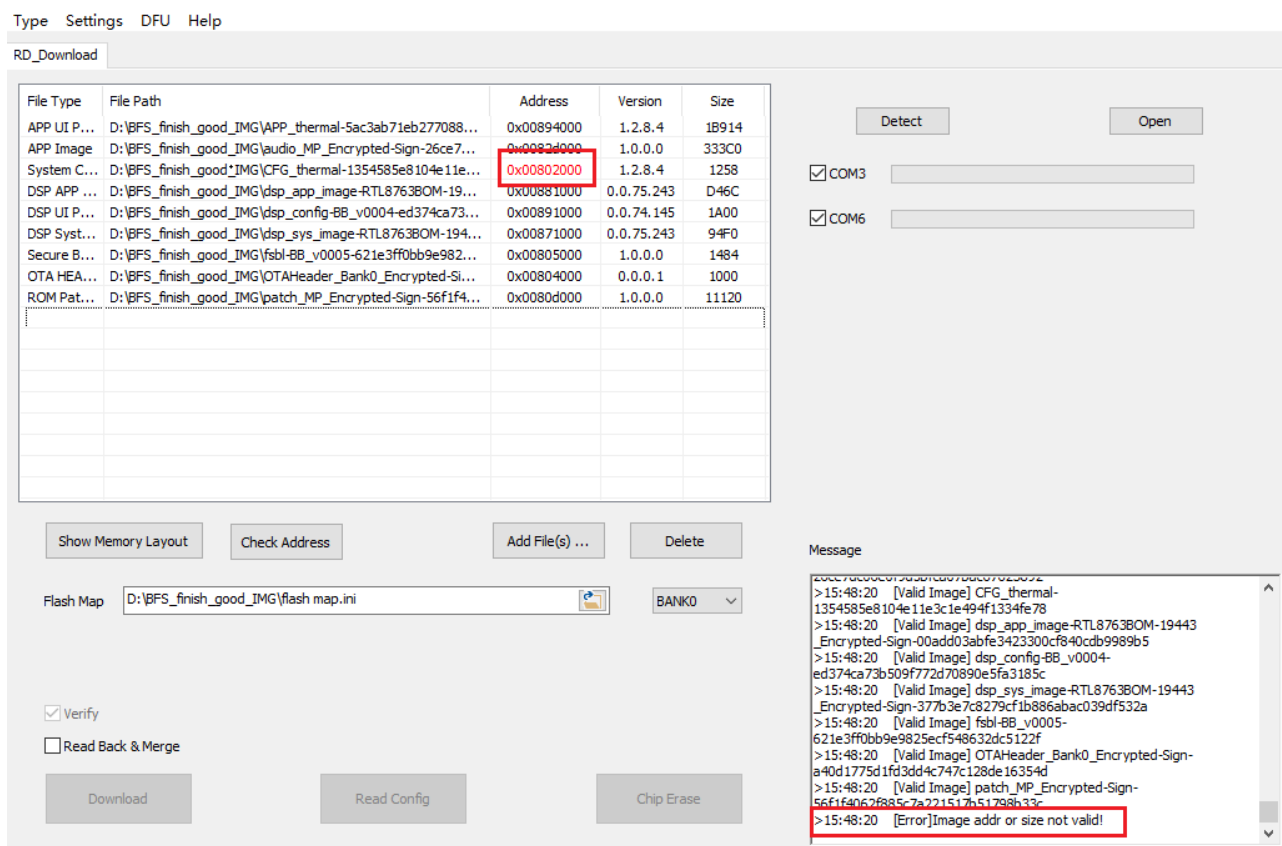


Figure 2-39 Error Address

C) “Flash memory layout” for image validation

Click “Show Memory Layout” to check memory using status, as shown in Figure 2-40.

If there are some conflicts, please delete relevant image files or reload the right image files.

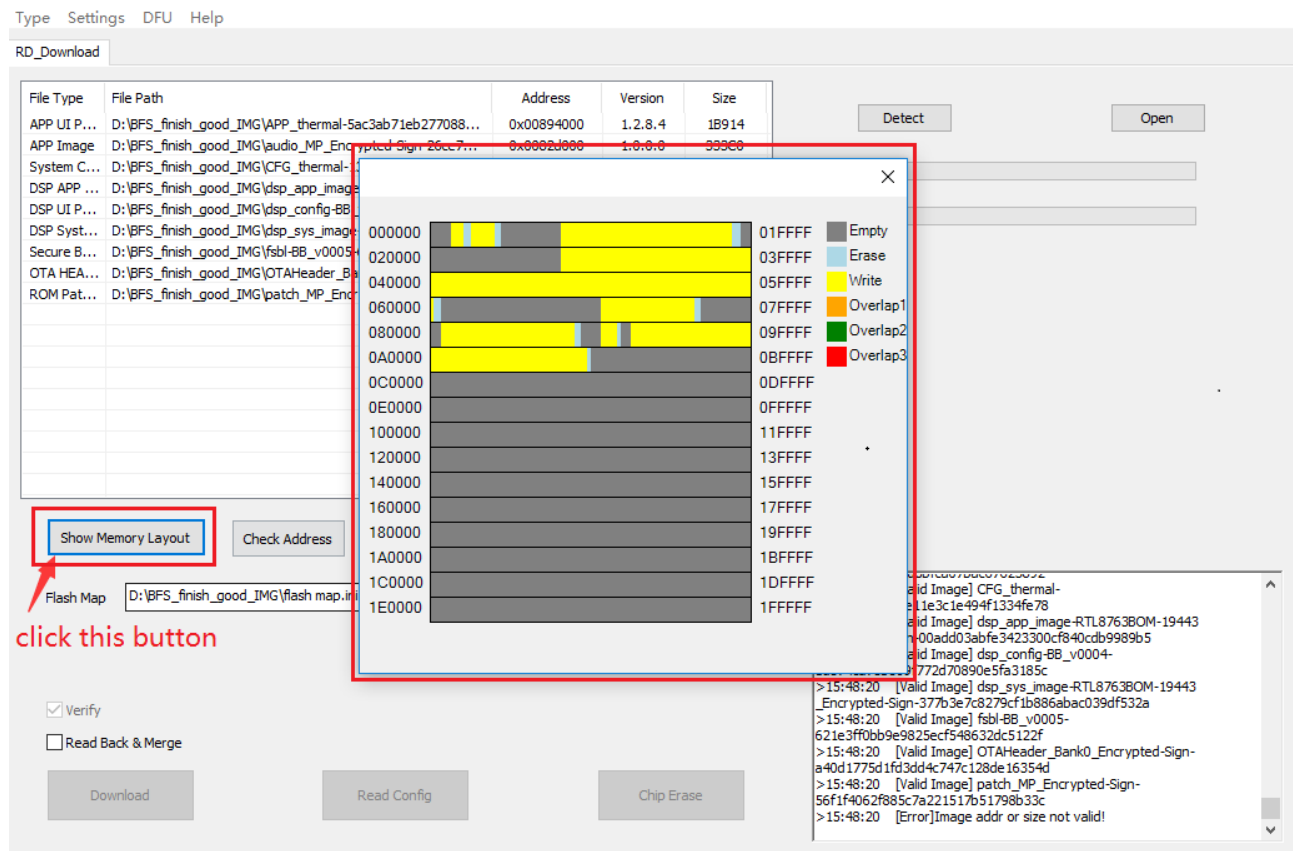


Figure 2-40 Flash memory layout

2.4.2 Detect & Open port

Click “Detect” to detect ports’ number, the number of ports will show after detection, as shown in Figure 2-41, then choose ports you need and click “Open” to make these ports ready for operating.

If one port is good for operate “Download”, “Read Config”, “Chip Erase” etc., an “ok” will show out behind the port, otherwise a “failed” will show.

If one of the chosen ports shows “ok”, then “Download”, “Read Config” and “Chip Erase” will be able to click. As shown in Figure 2-42.

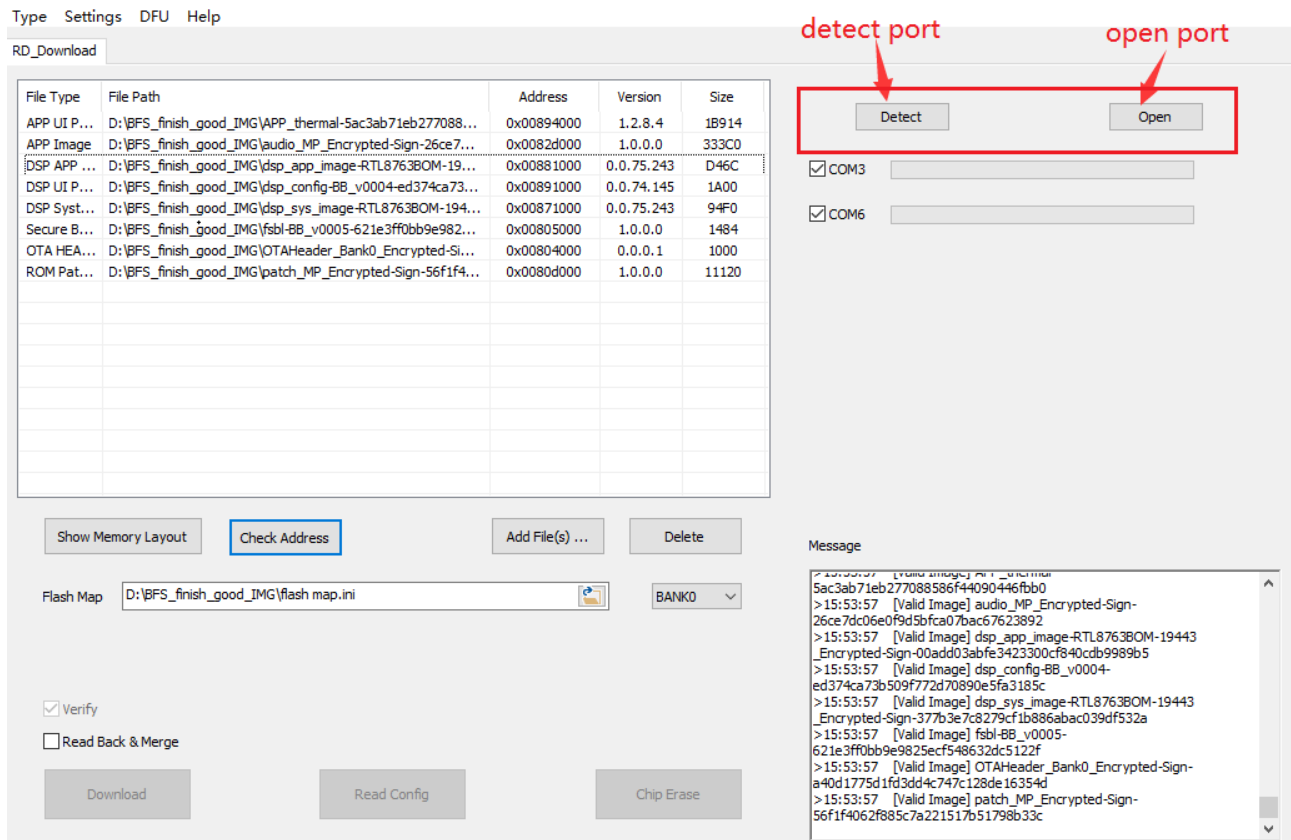


Figure 2-41 Com port detection

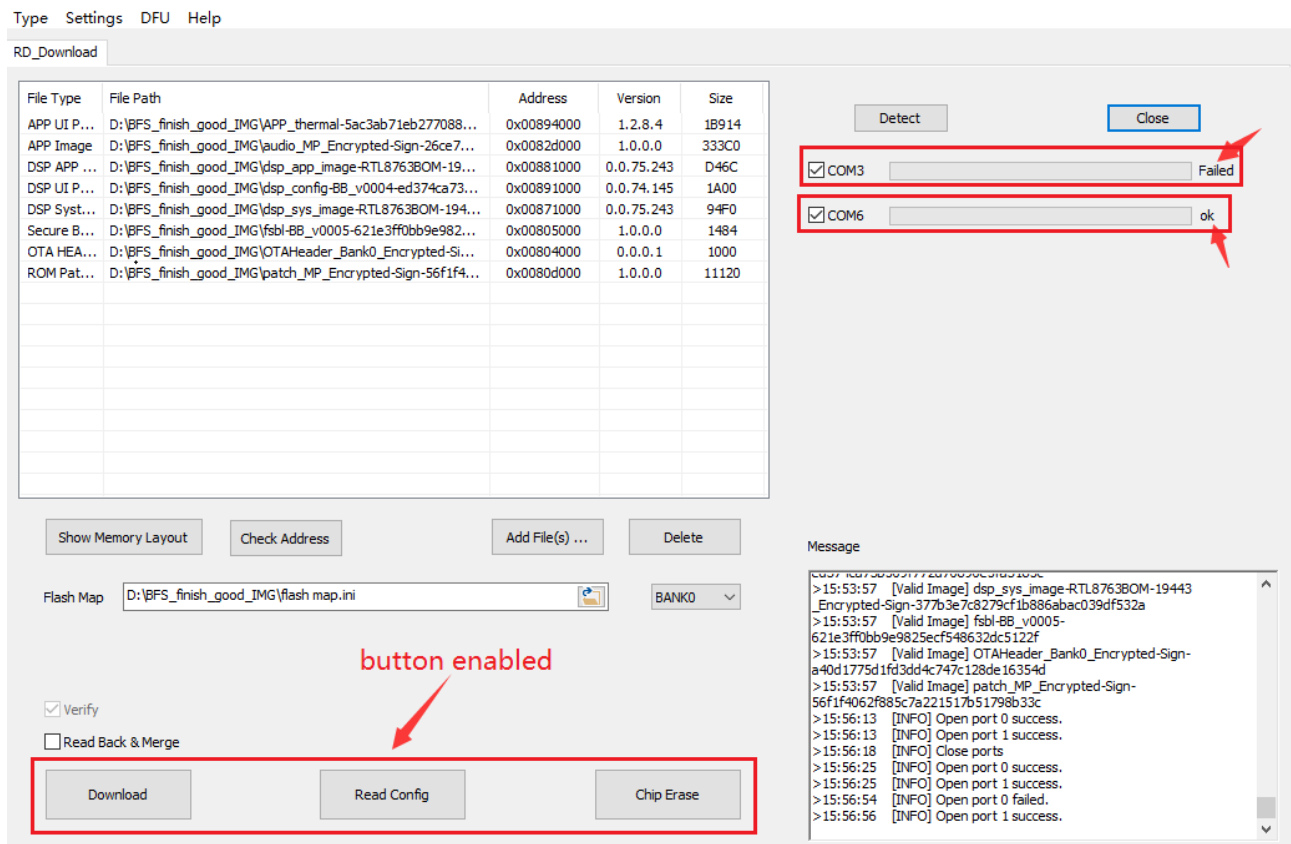


Figure 2-42 Open com port and enable function button

2.4.3 RD Download mode

There is an optional operation for you to choose, “Read Back & Merge”, as shown in Figure 2-43. And there will be two scenarios:

- 1) If “Read Back & Merge” is unchecked, it will erase chip before download. Its procedure will be:
 - a) Erase chip(not the entire chip, only the fields you want to write into)
 - b) Download bin to chip
- 2) If “Read Back & Merge” is set check, it will read back system configuration and merge by imported bin. Its procedure will be:
 - a) Read back parameters and merged with imported bin
 - b) Erase chip(not the entire chip, only the fields you want to write into)
 - c) Download bin to chip

If download procedure succeeds, a “success” will show behind the port. Otherwise, a “failed” will show.

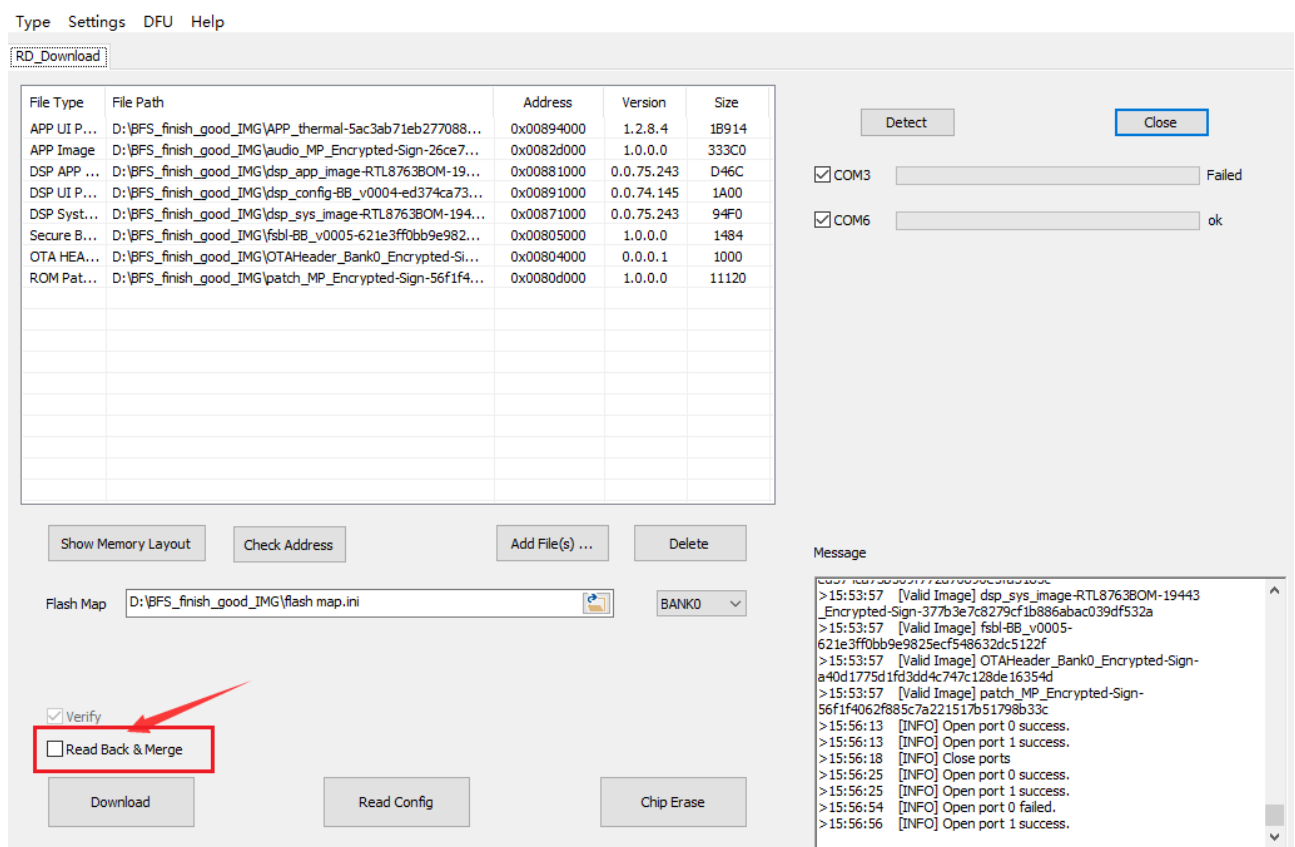


Figure 2-43 RD download mode

2.4.4 Chip Erase

Click “Erase” button to erase the entire chip’s flash area, as shown in Figure 2-44. If chip erase procedure succeeds, a “success” will show behind the port, otherwise it will show a “Failed”.

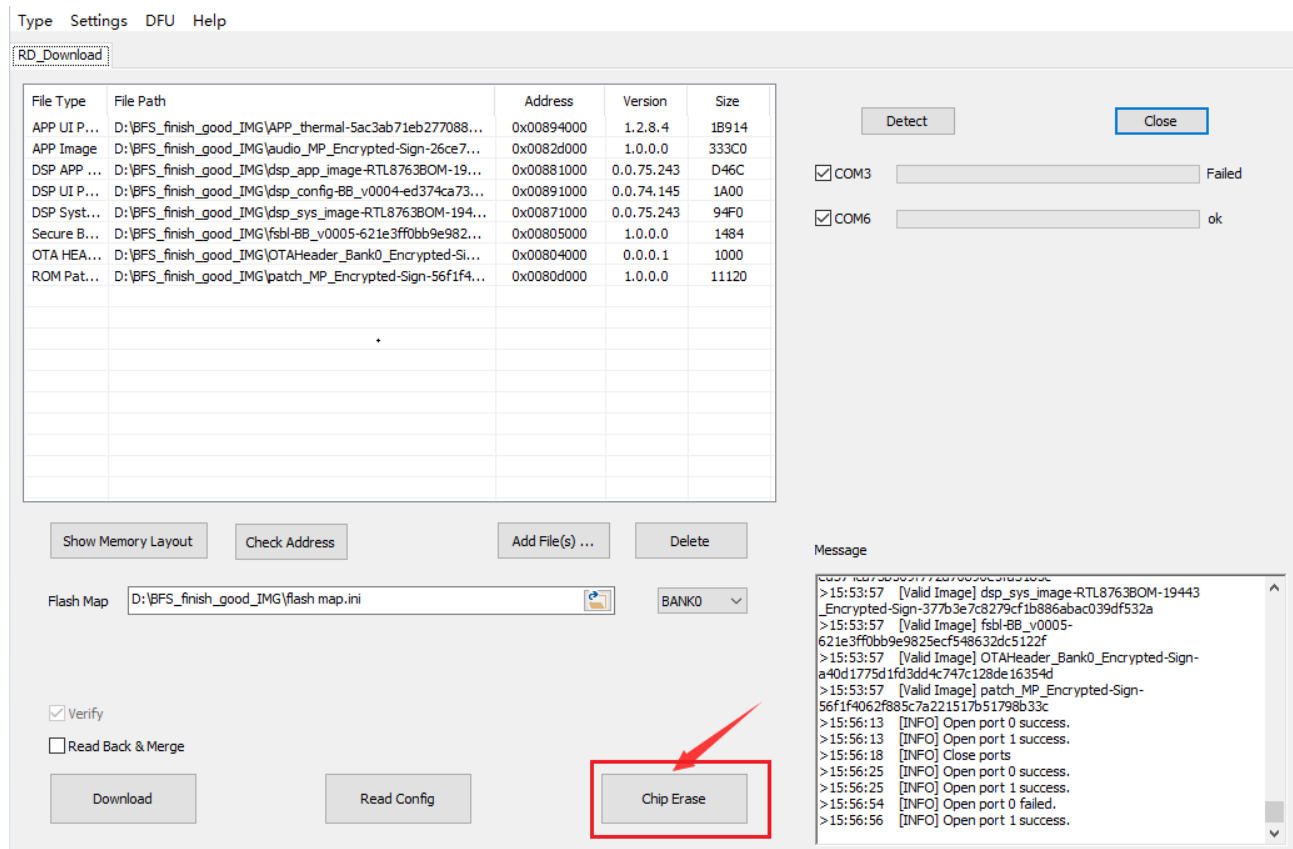


Figure 2-44 Erase entire chip

2.4.5 Read Config

Click “Read Config”, if the chip has not programmed download bin before, “Read Config” progress will fail, as shown in Figure 2-45.

If it has already programmed download bin before, and “Read Config” is successful, it will pop out a “Configuration setting” dialog (Figure 2-46), you can change parameters and check the checkbox you operated before. Then click “Change Setting”, it will program down changes and close the dialog.

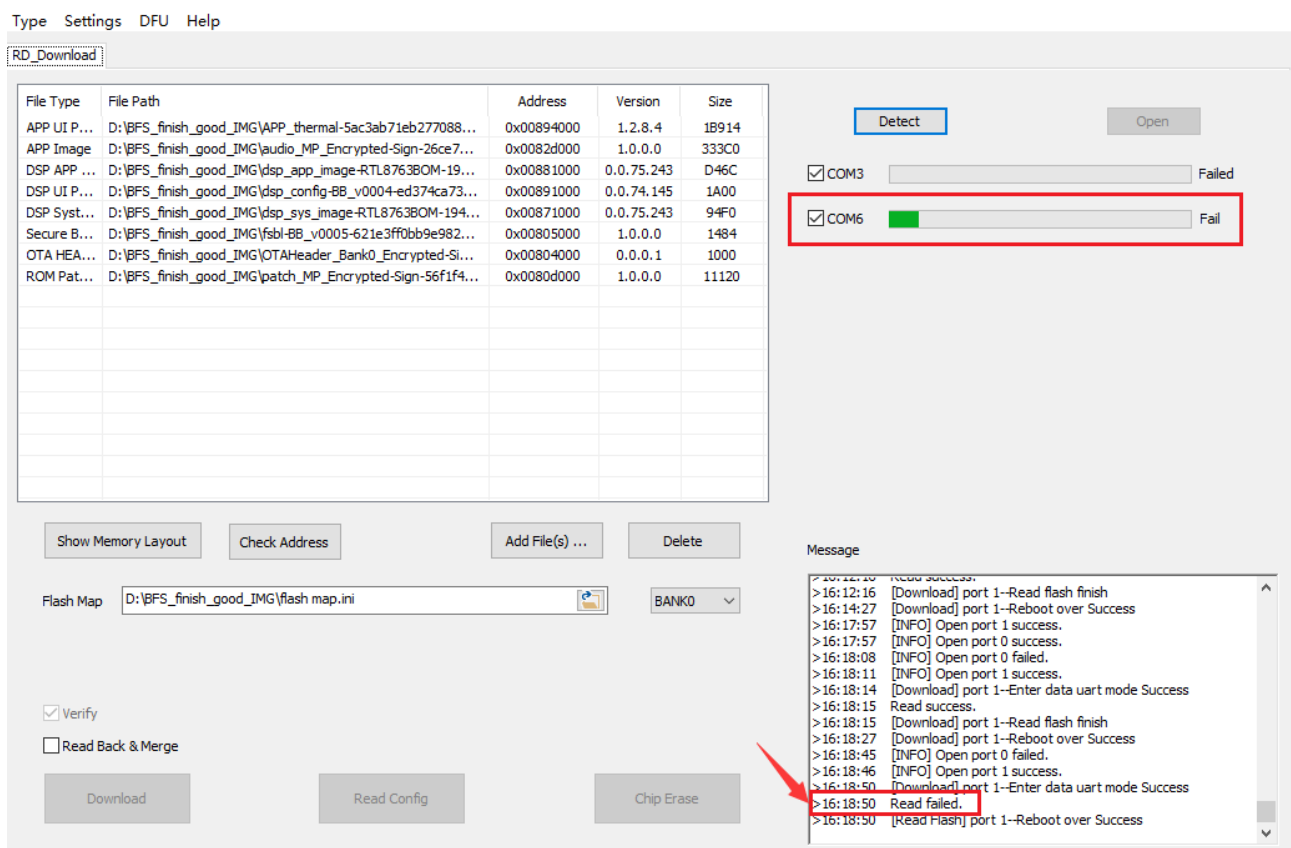


Figure 2-45 Read configuration from chip

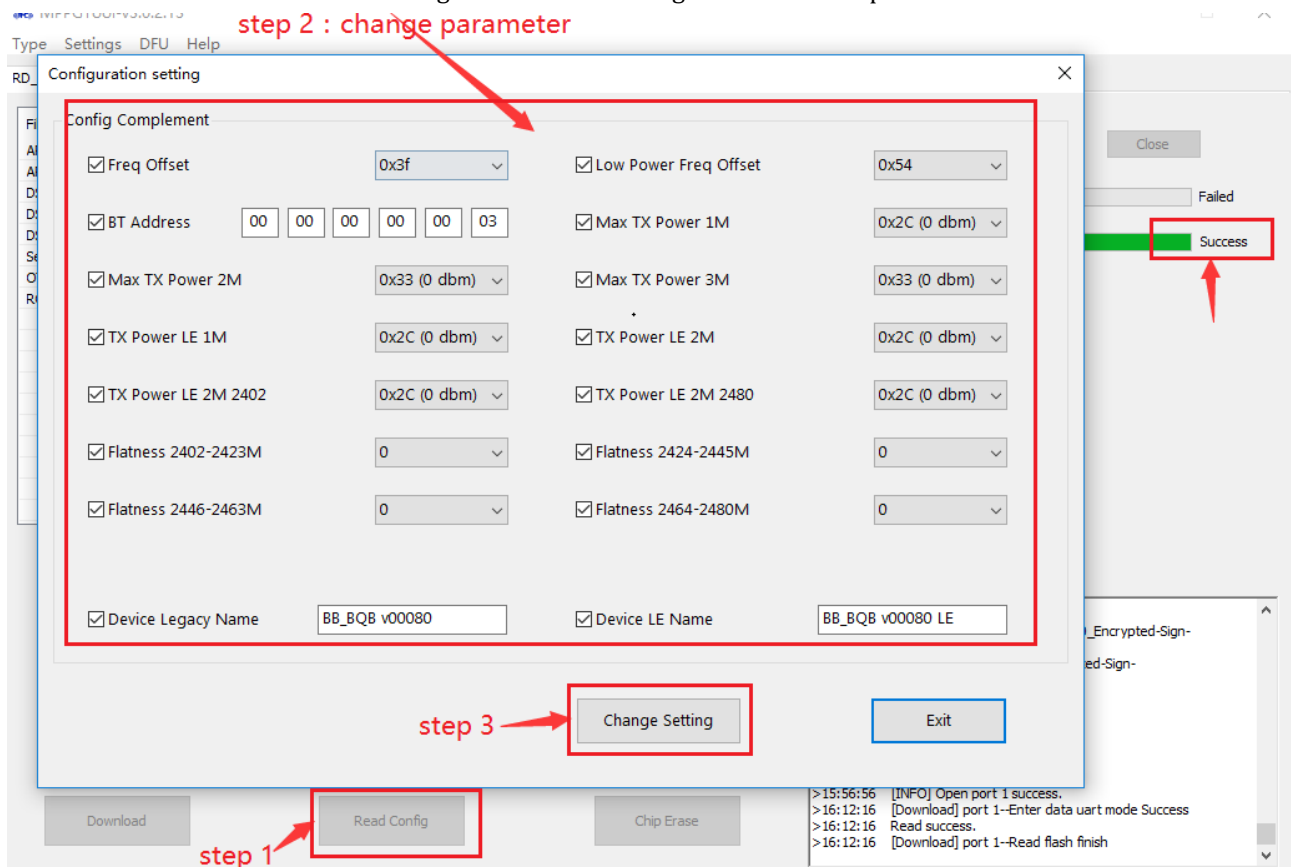


Figure 2-46 Change configuration settings

2.4.6 Efuse SHA check

Efuse SHA information check is a particular function only for some secure chips. It provides functions as follows:

- Check secure boot
- Check SHA information read from efuse

As shown in Figure 2-47, if the IC type you choose at the Guide interface support writing SHA, you will see a “Check Secure Boot” button in the RD mode interface. While choosing other IC types the button will not be shown.

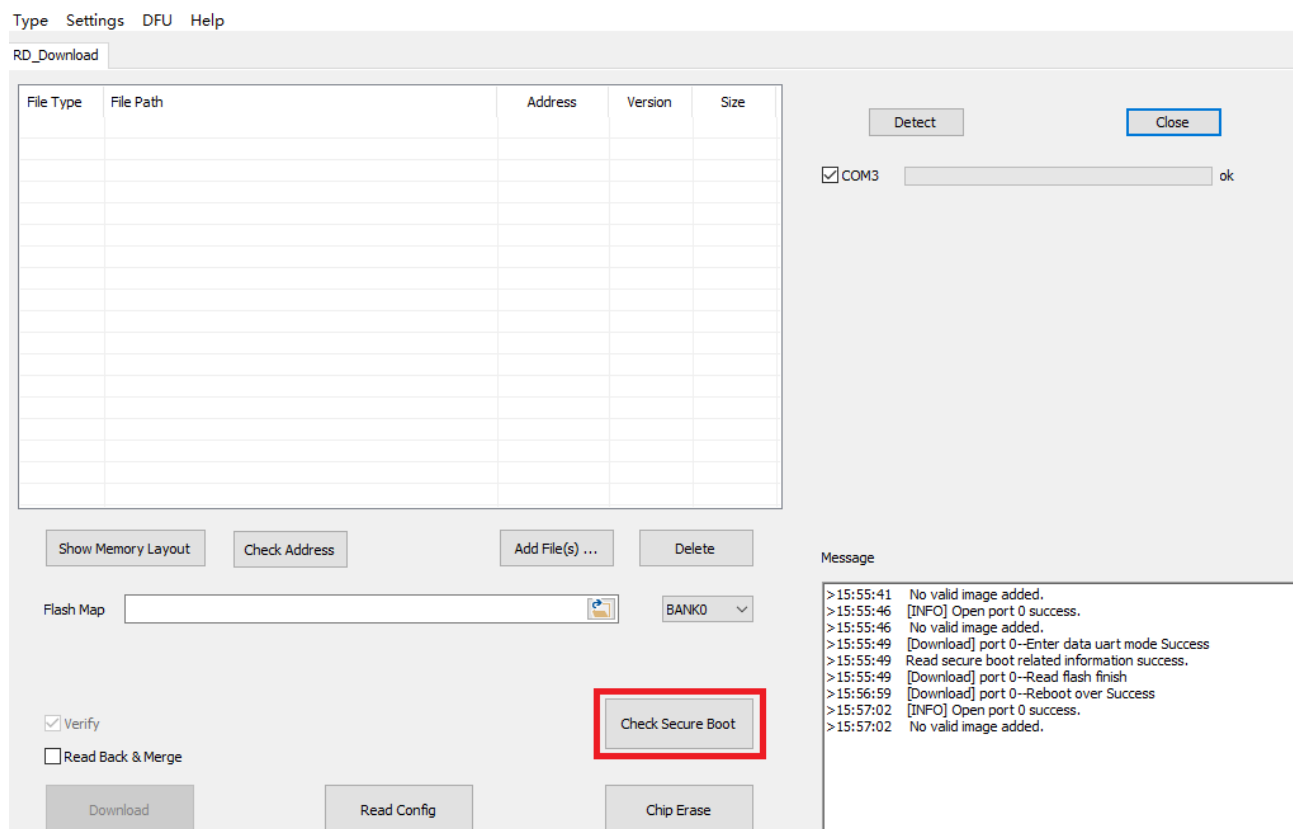


Figure 2-47 Check Secure Boot button

Click “Check Secure Boot” and there will have two results:

1) Secure Boot Disabled

If the chip is not secure boot enabled, the tool will pop up a message box as shown in Figure 2-48.

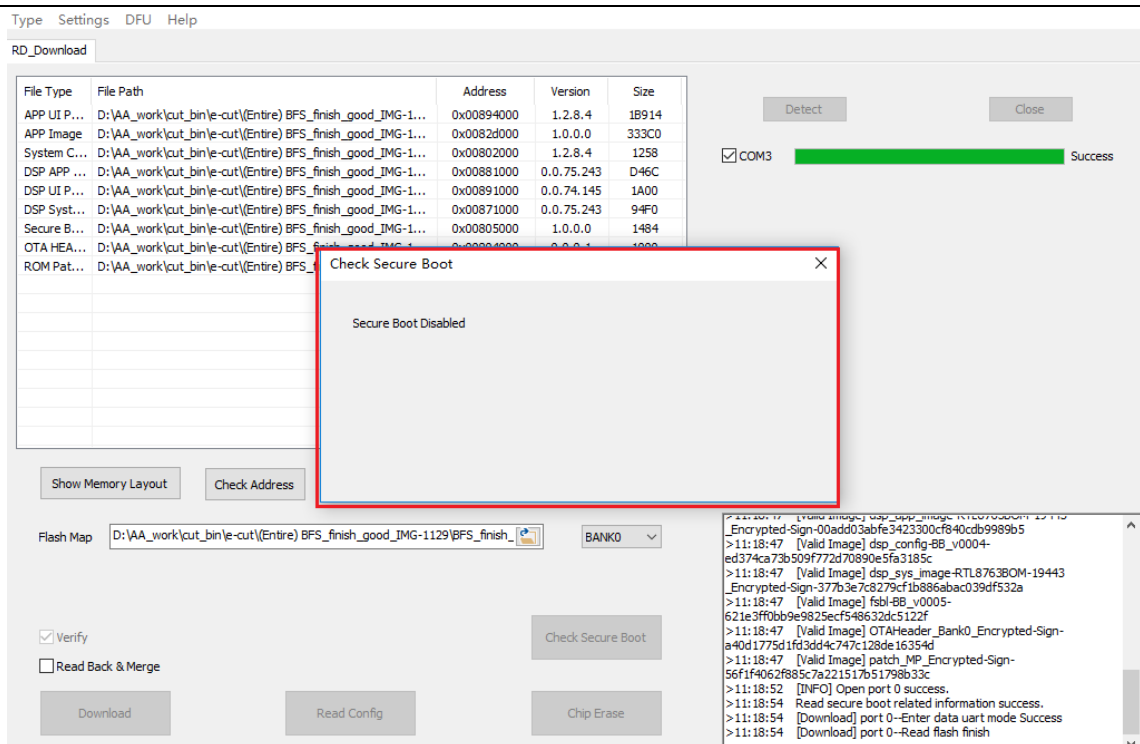


Figure 2-48 Secure Boot Disabled

2) Secure Boot Enabled

If the chip is secure boot enabled, the tool will read back SHA information from efuse and check valid of the SHA information. There are three scenarios:

a) Empty SHA information

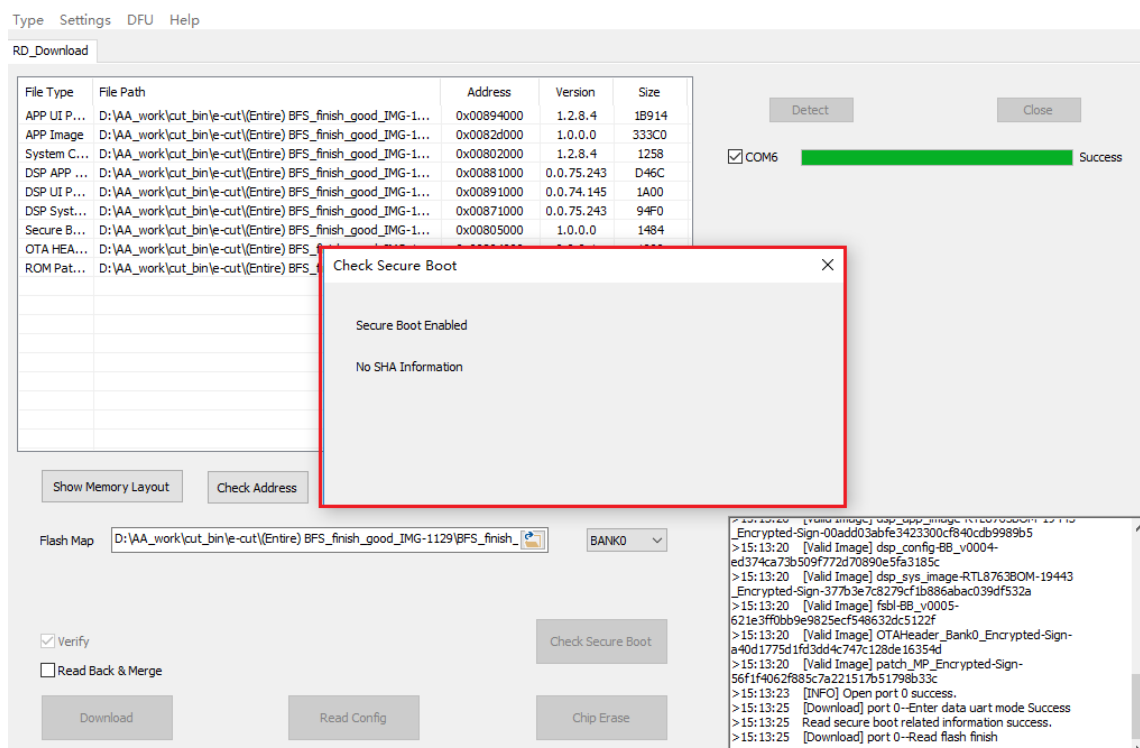


Figure 2-49 Empty SHA information

This scenario indicate that the chip has not be written SHA information into efuse before. The tool will pop up a message box as shown in Figure 2-49.

b) Valid SHA information

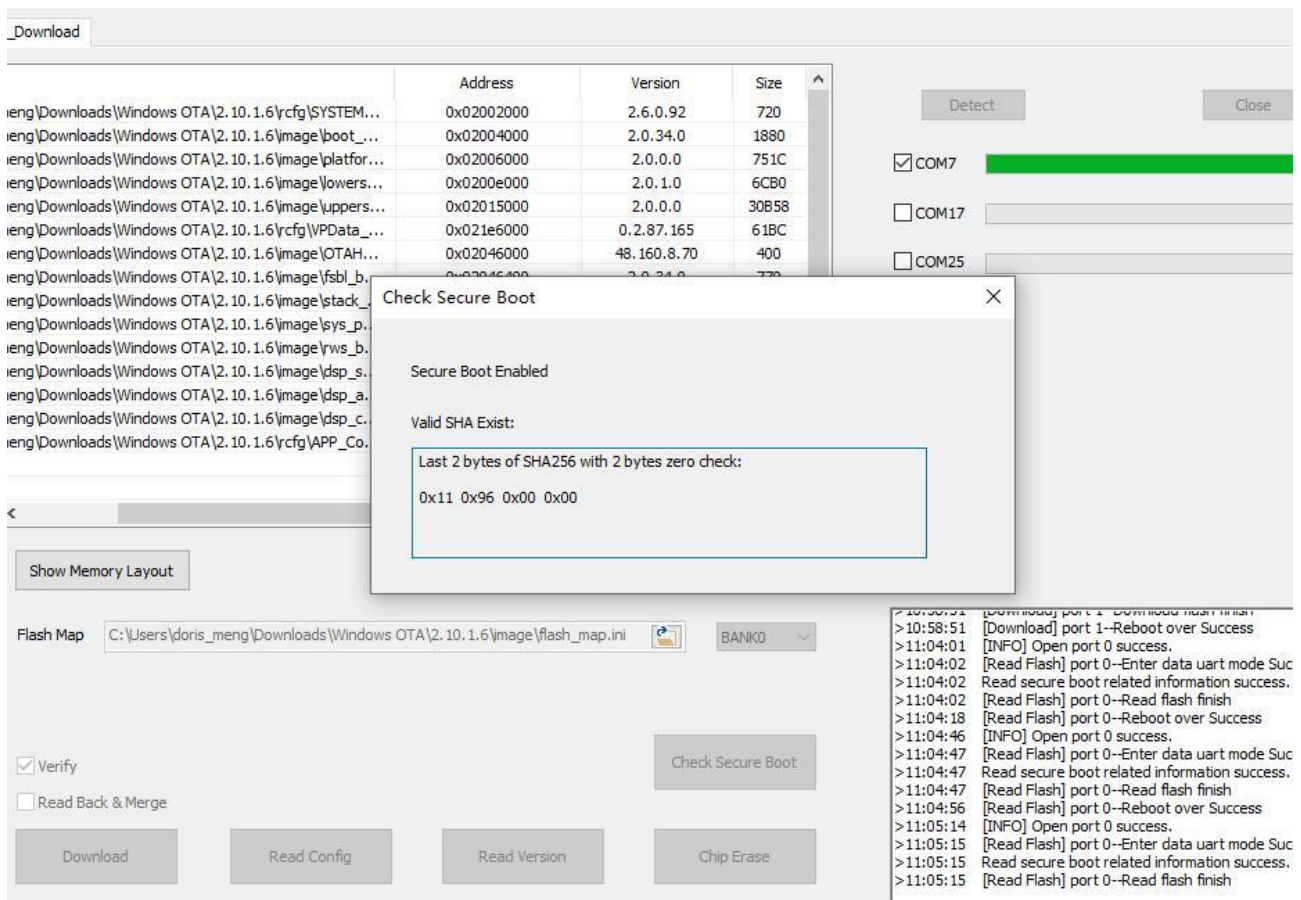


Figure 2-50 Valid SHA information

If the chip has already be written SHA information into efuse before, tool will check validation of the SHA information read from efuse. If the SHA information read from efuse is valid, tool will show part of them on the message box as shown in Figure 2-50.

c) Invalid SHA information

If SHA information read from efuse is not empty and invalid, tool will pop up a message box as shown in Figure 2-51.

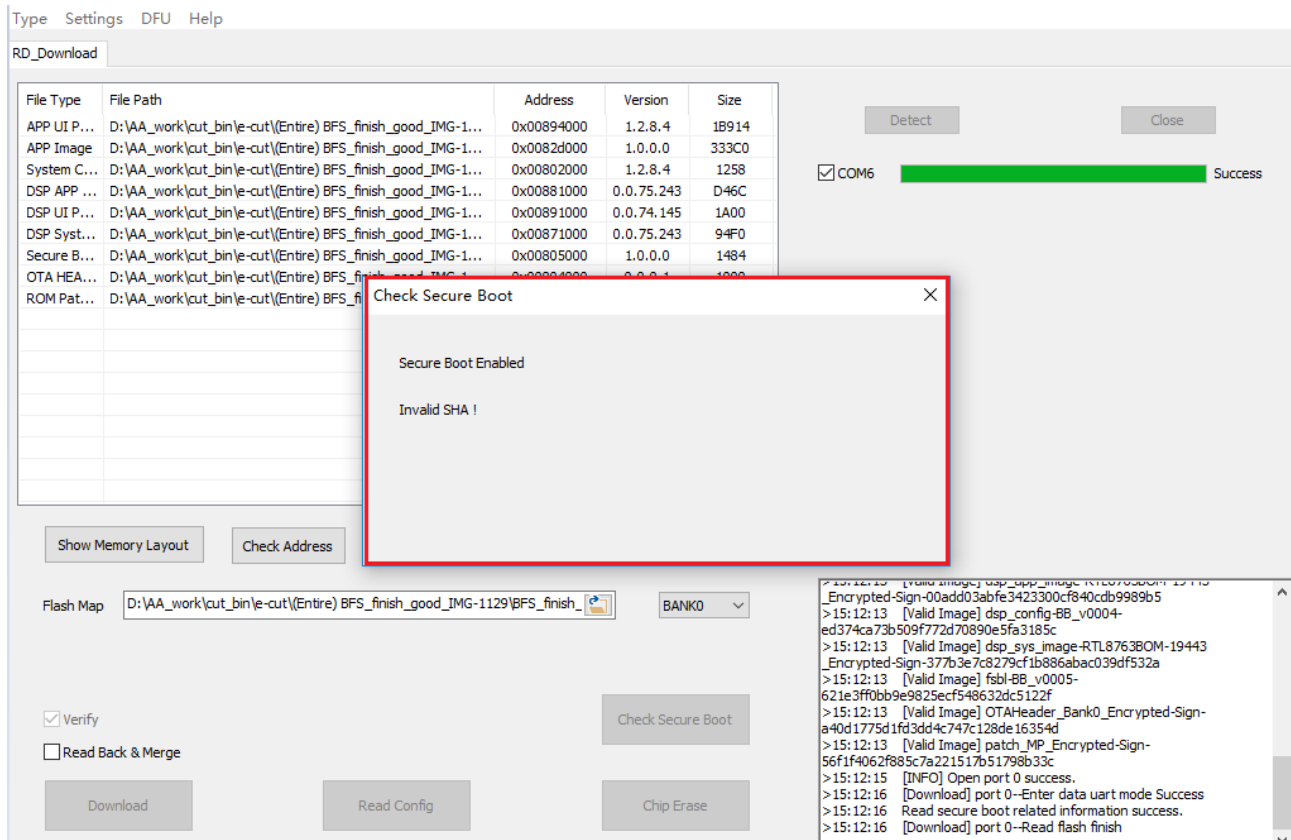


Figure 2-51 Invalid SHA information

2.4.7 Read Version

Click “Read Version”, if the chip has already programmed download bin before, and “Read Version” is successful, it will pop out an “Image Info” dialog (Figure 2-52).

If the chip has not programmed download bin before, “Image Info” dialog will show fail message, as shown in Figure 2-53.

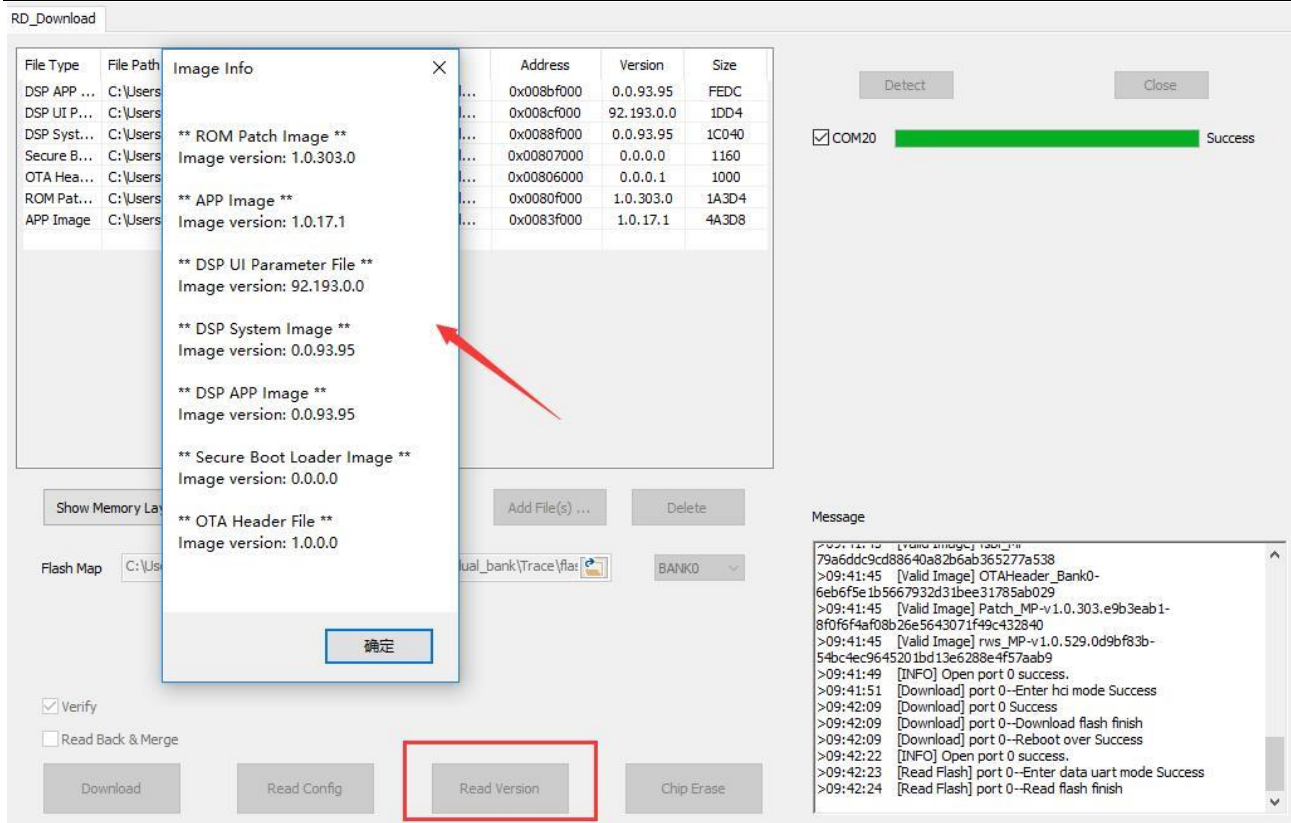


Figure 2-52 Read version success

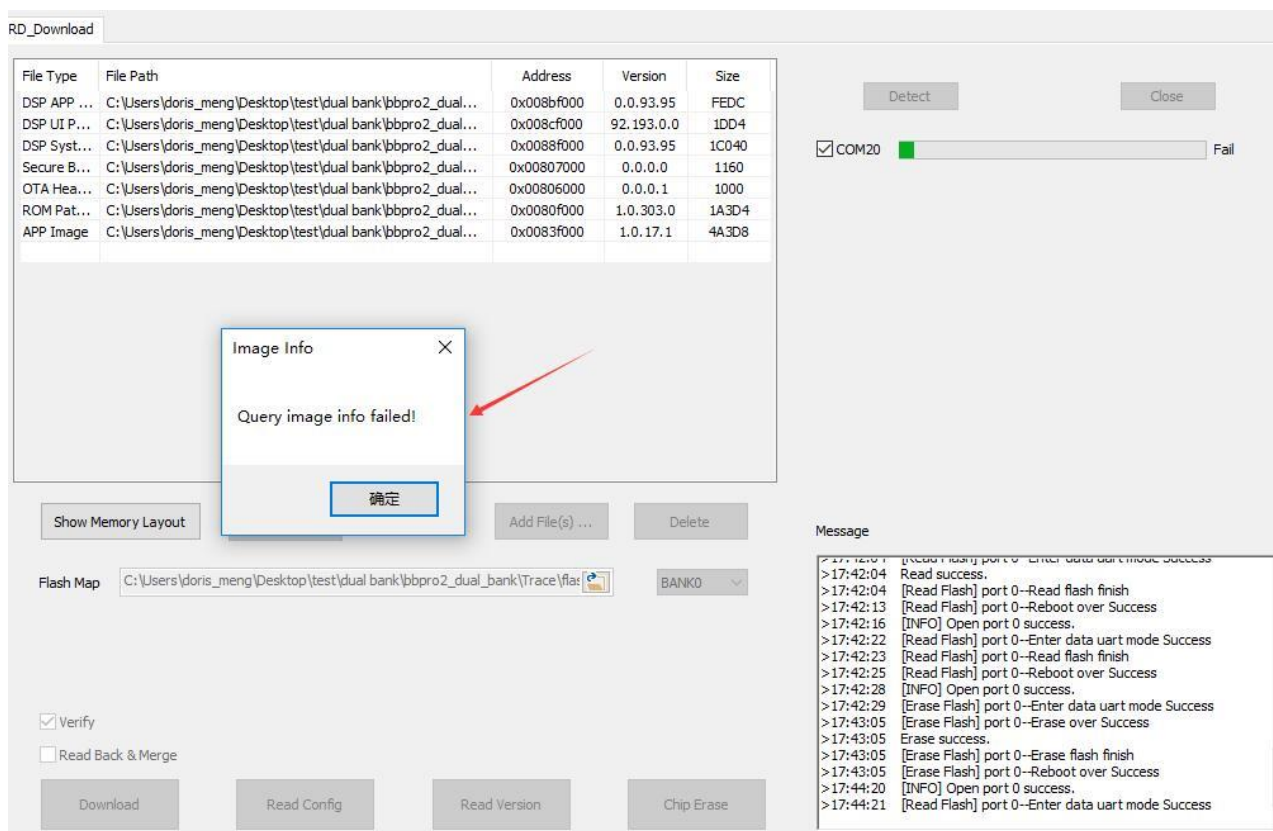


Figure 2-53 Read version fail

2.4.8 One Wire Download

Some IC types of the RTL87X3E and RTL8773D series support the one wire download feature. If this feature is supported, the “Enable One Wire Download” checkbox will be showed on the UI.

1. In RD_Download page, check ‘Enable One Wire Download’ (Figure 2-54), after loading the flash_map.ini and image files.
2. After checking “Enable One Wire Download” checkbox, an option to select the baud rate will be displayed. Set the appropriate baud rate.
3. Click the Detect and Open button to open the port.
4. After the chosen ports shows ‘OK’, click ‘Download’ button to start ‘One Wire Download’.

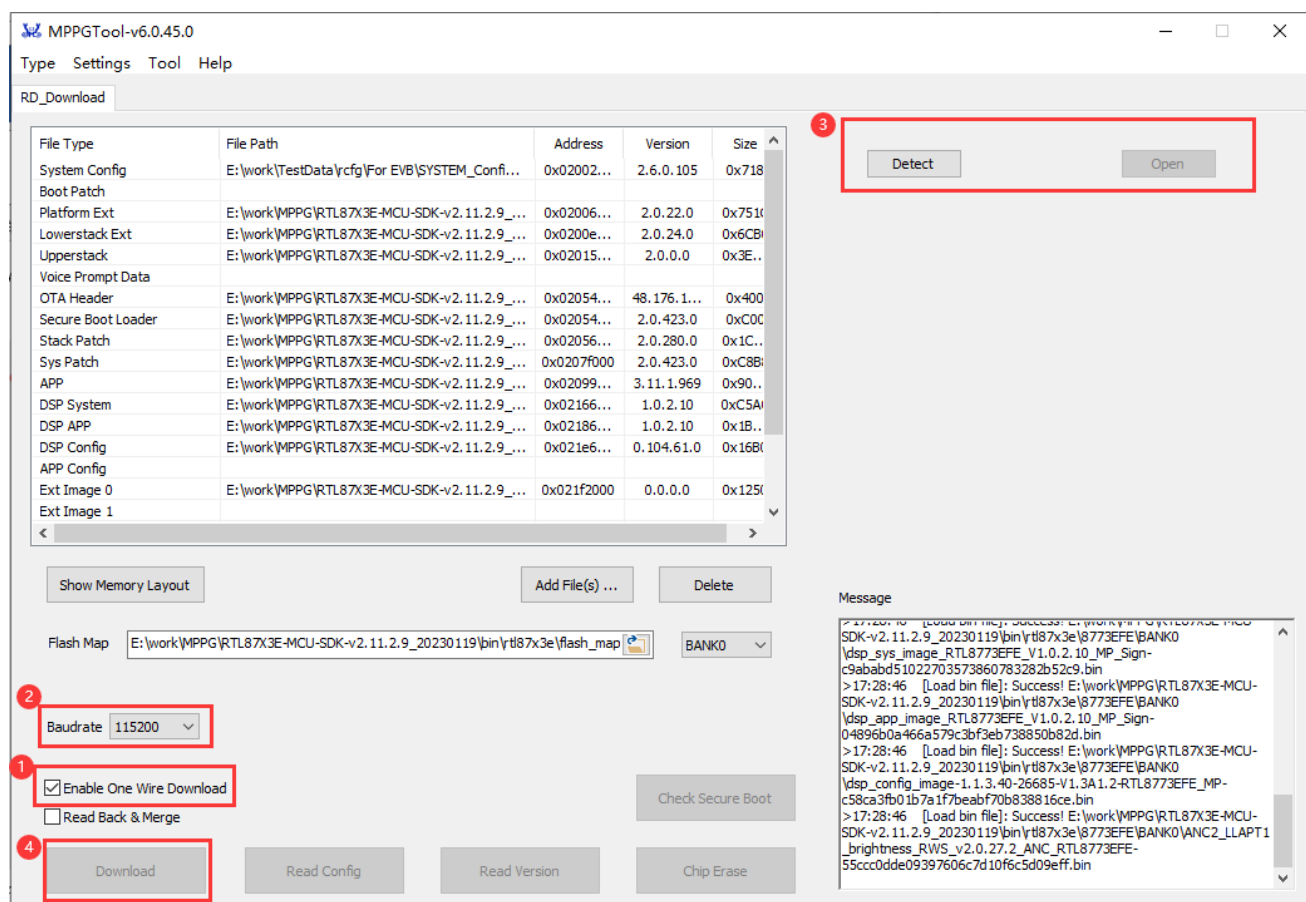


Figure 2-54 Check 'Enable One Wire Download' in RD_Download page

5. EVB wiring of one wire download is as follows:

- a) Connecting one wire Uart adapter
- b) One wire Uart with evb connection

One wire IO of adapter board is connected to VADP on the EVB.

The GND of the adapter board is connected to the GND of the EVB.

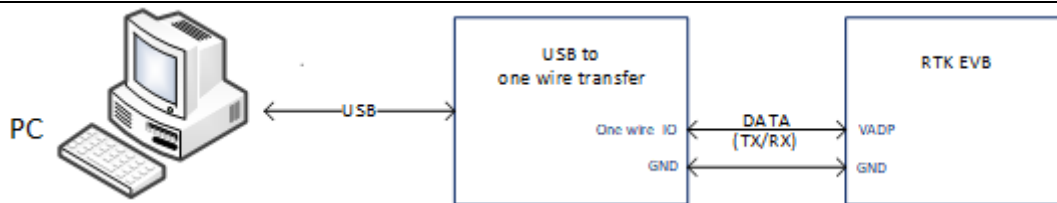


Figure 2-55 One wire Uart with EVB Connection

Attention:

- 1) Can't erase and write boot patch image if 'Enable One Wire Download' checked (Figure 2-56).
- 2) 'Chip Erase' Button is not allowed to click in RD_Download page if 'Enable One Wire Download' has been checked.
- 3) MPPGTOOL will send app reset command by clicking open button in one wire download mode, which will trigger SOC to reset to access the one wire download program. If the app on the SOC cannot run normally, and it is not in the state of automatic reset constantly, it is necessary to rely on other ways to make the IC reset to access the one wire download program after clicking the open button. After clicking the open button, wait for the SOC to reset to access the one wire download mode, the timeout is set to 20s.
- 4) Recommended to have two bank images burned before switching to one wire download mode.
- 5) The supported baud rates of the chip are dependent on the capacitance. Please choose the chip's supported baud rate.

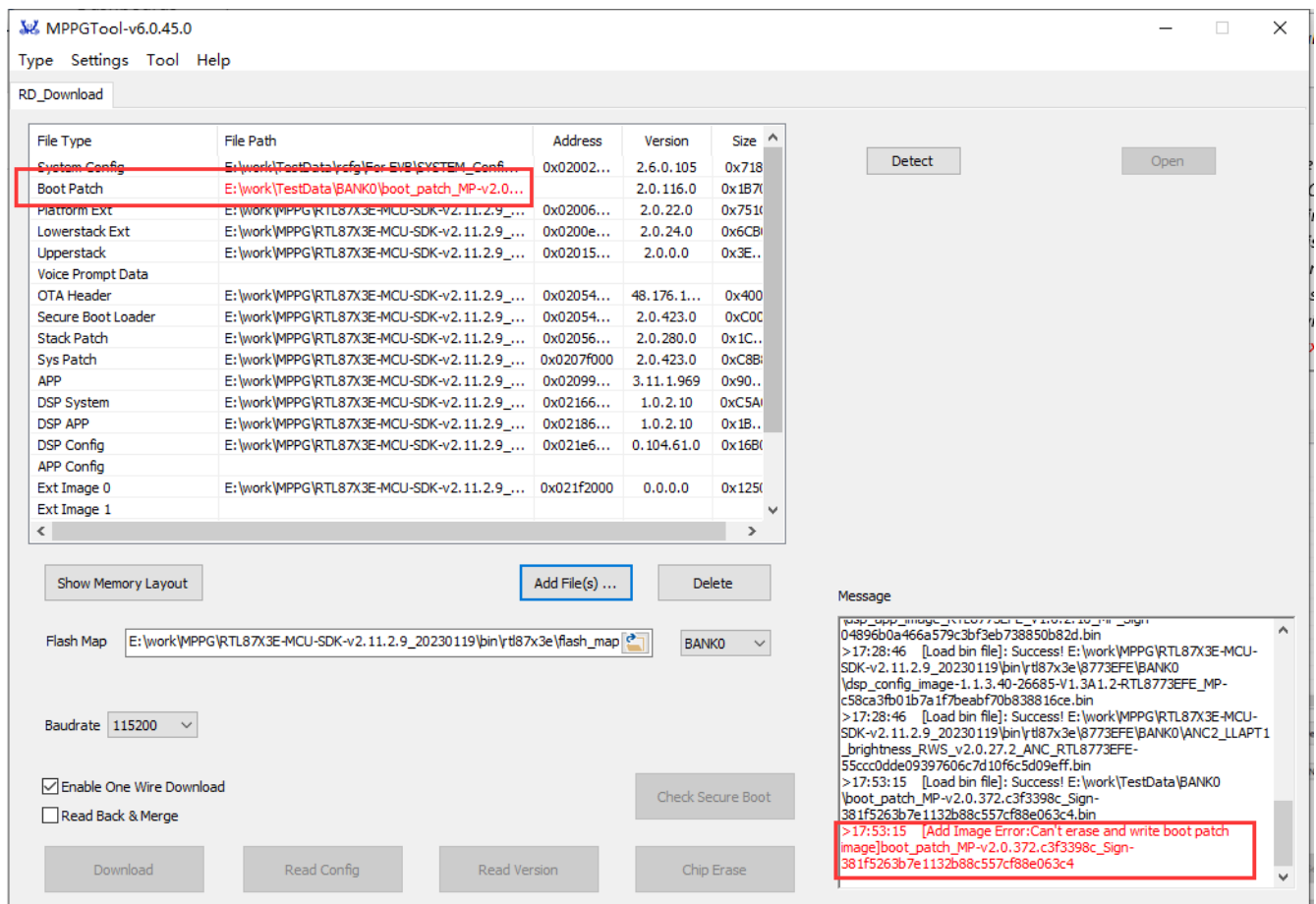


Figure 2-56 Add Boot_patch Image Error

3 Appendix

3.1 System environment

MPPG Tool supports win7 system and win 10 system.

1. MPPG Tool will detect all serial ports in the system. Irrelevant COM ports irrelevant may cause open failure. Please turn off irrelevant ports before mass production.
2. How to turn off irrelevant ports:
 - 1) As shown in Figure 3-1, right click on "Computer" icon, and select "Manage" in menu.

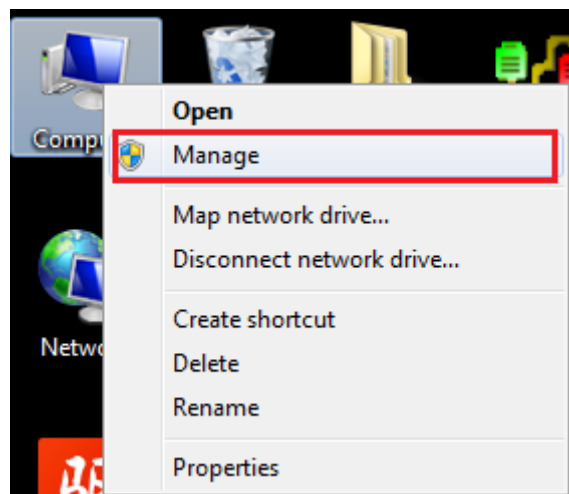


Figure 3-1 Manage Computer

- 2) As shown in Figure 3-2, "Computer management" -> "Device manager" -> "Disable" other irrelevant COM ports in "Ports".

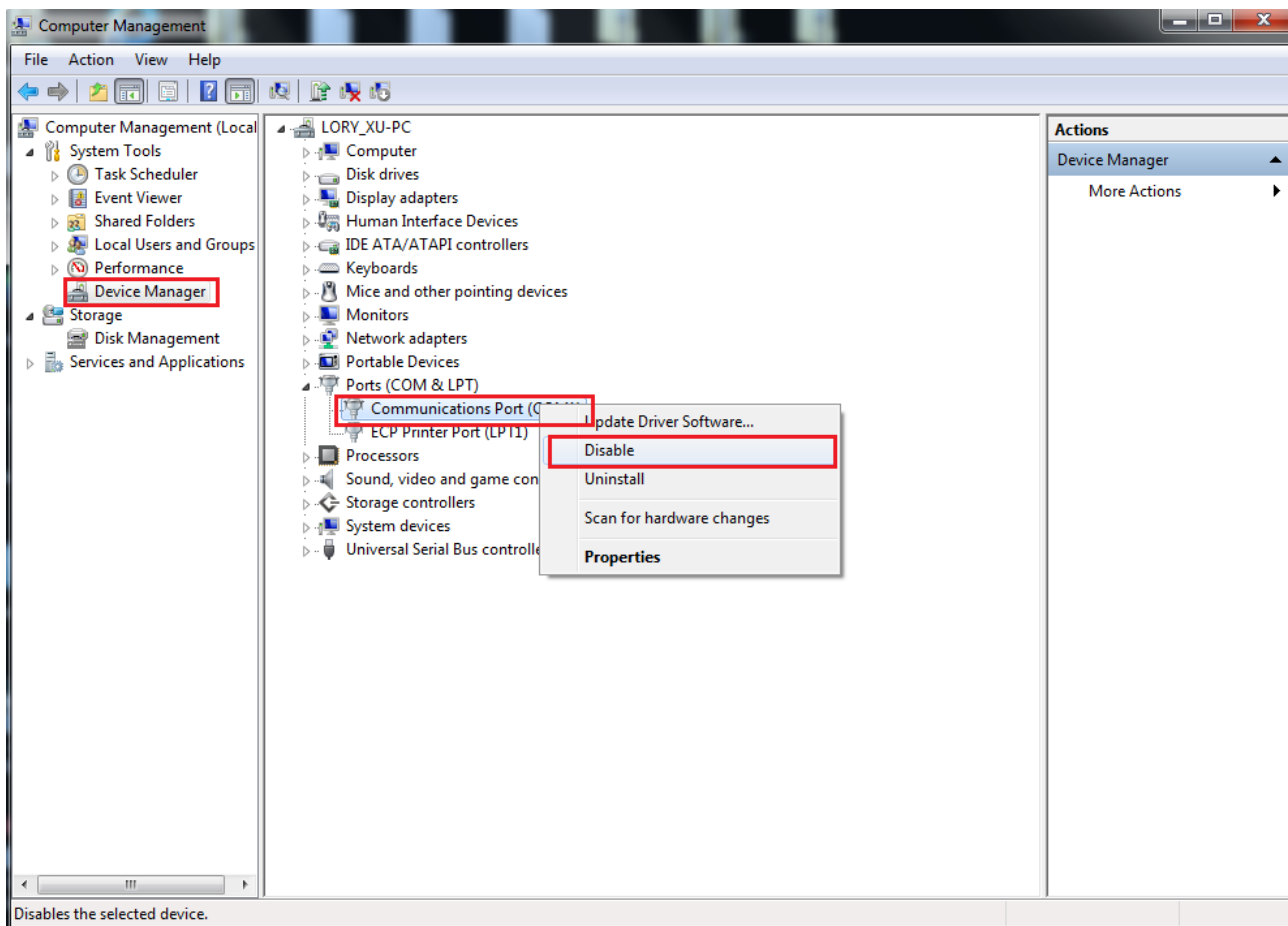


Figure 3-2 Forbid Irrelevant COM

3.2 Connection scenarios

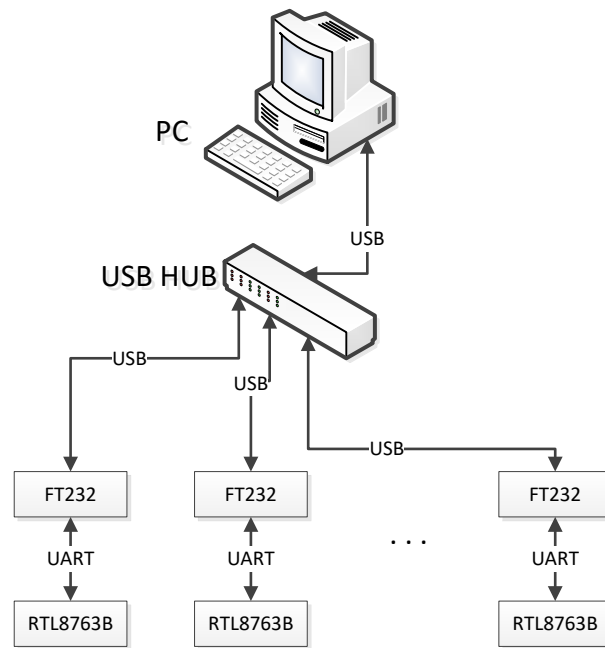


Figure 3-3 One-to-Many Wiring

If downloading through one-to-many way via USB HUB, please make sure sufficient power supply to ensure stable downloading. We strongly suggest to use USB HUB with external power source. (Figure 3-3).

3.3 EVB wiring

1. Make sure the P2_0 is ground connection.
2. Shortening UART_TXD and HCI_RX with jumper cap;
Shortening UART_RXD and HCI_TX with jumper cap.
3. Reset the EVB before PG.

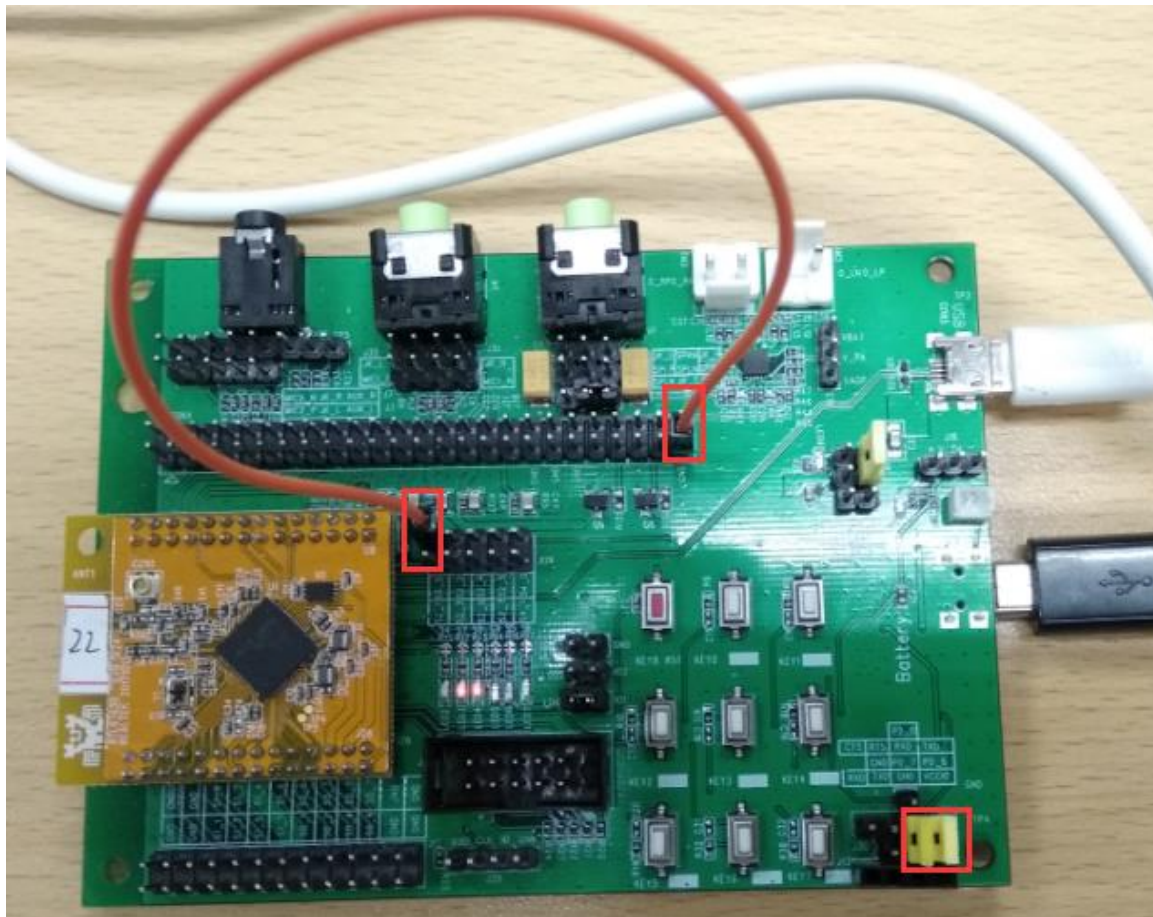


Figure 3-4 EVB wiring

3.4 Suggested flow

The suggested flow is as follows:

Step1 Chip erase.

Attention: *If some parameters need to be maintained (e.g. "BT Address", "Freq Offset" configured in previous stage), skip this step! Simply check "Read Back & Merge" and move on to step2.*

Step2 Download.

Step3 Factory reset.