TI mmWave Sensors IWR14xx/16xx Device Overview

Agenda

- Device Overview
 - TI mmWave sensor portfolio
 - IWR1xx Signal processing chain
 - Example System topologies
- Functional Blocks
 - Device Block Diagram
 - RF and Analog Subsystem
 - Radar Subsystem (aka BSS or BIST Subsystem)
 - Master Subsystem (MSS)
 - DSP Subsystem (DSS: IWR16xx only)
 - Radar Hardware accelerator
- Boot modes
- Software Platform

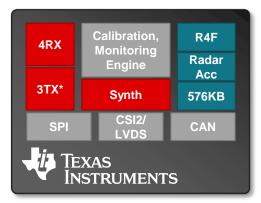


Device Overview



mmWave Sensors – 76-81 GHz Portfolio

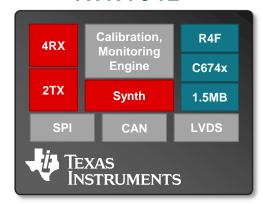
IWR1443



mmWave Sensor + HW Accelerator

- Use Case
 - Satellite Sensor with MCU
 - 4X IWR14 + Central Processor
 - 2X IWR14 + Central Processor
 - Entry-level Single-chip Sensor
 - · Power-optimized applications
 - · HW acceleration for limited processing

IWR1642



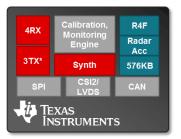
mmWave Sensor + DSP

- Use Cases
 - Full functionality single-chip radar
 - Increased on-board memory for higher range and resolution measurement
 - On-chip DSP for advanced algorithms

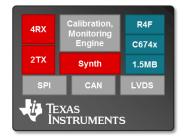
Key Features

- FMCW Radar transceiver with 76-81 GHz operating frequency with 4 GHz chirp bandwidth
- MIMO: Up to three transmitter and four receiver chains
- Programmable, flexible chirp profiles for both long and short range sensing in the same radar frame
- 200MHz ARM Cortex R4F MCU for user application processing
- Radar Hardware accelerator for FFT and CFAR processing (14xx only)
- C674x DSP for FMCW signal processing and advanced tracking, clustering and object classification (I16xx only)
- Continuous monitoring and calibration of Analog/RF through a second dedicated Cortex R4F MCU
- CAN support for ECU Interface
- QSPI Serial Flash support for autonomous boot
- MIBSPI, SPI, I2C, and UART Serial Interfaces Support
- CSI2 (IWR14xx only) and LVDS interfaces for high speed raw data transfer

IWR1443

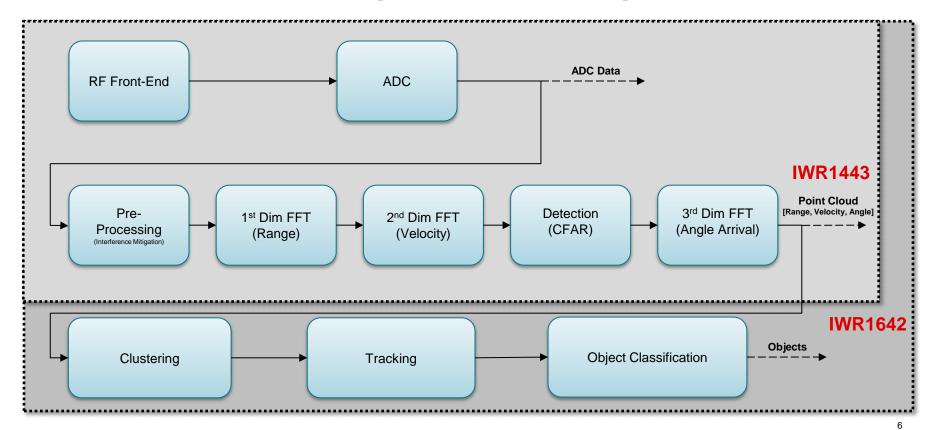


IWR1642

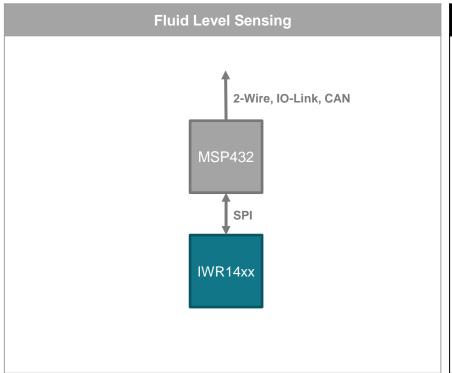


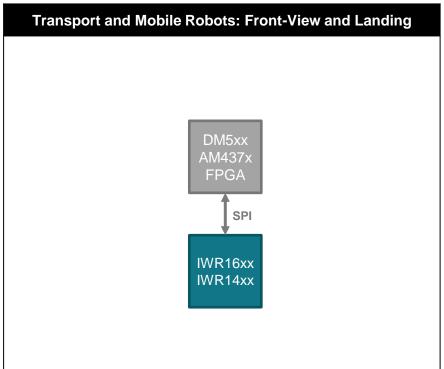


IWR1xxx mmWave Signal Processing

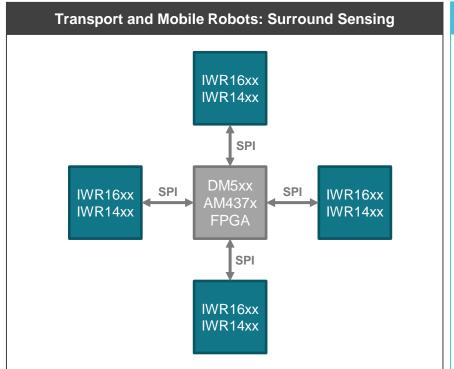


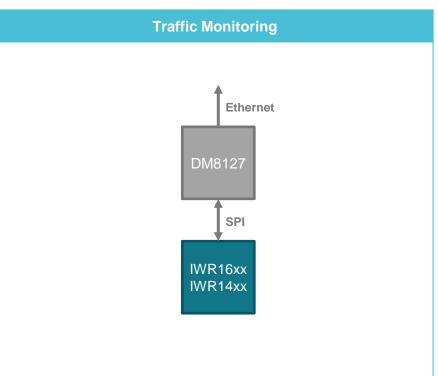
Example System Topologies





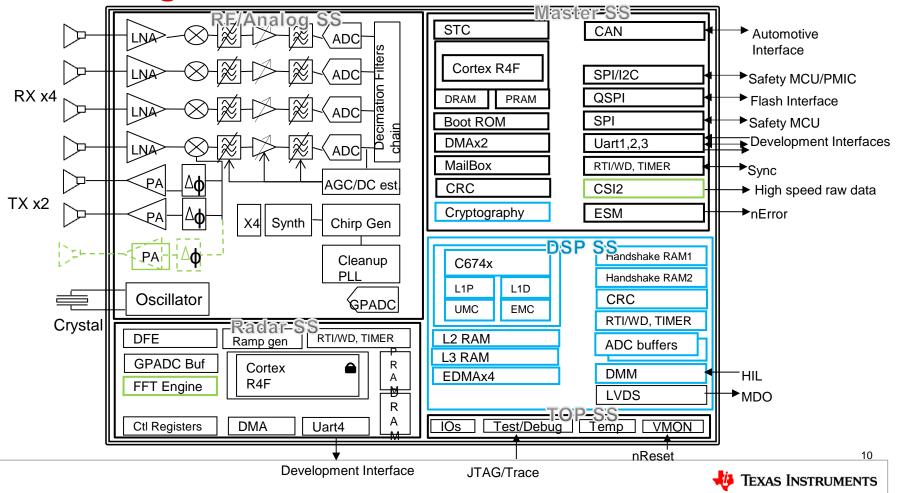
Example System Topologies





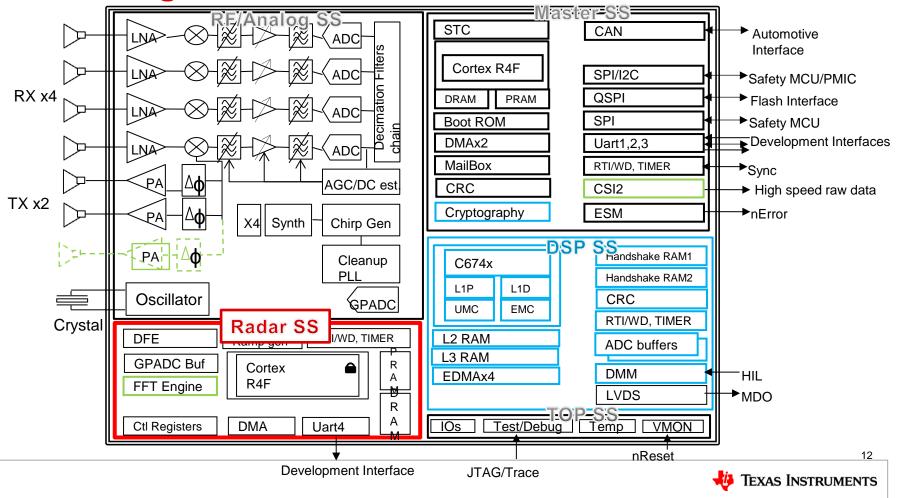
Functional Blocks

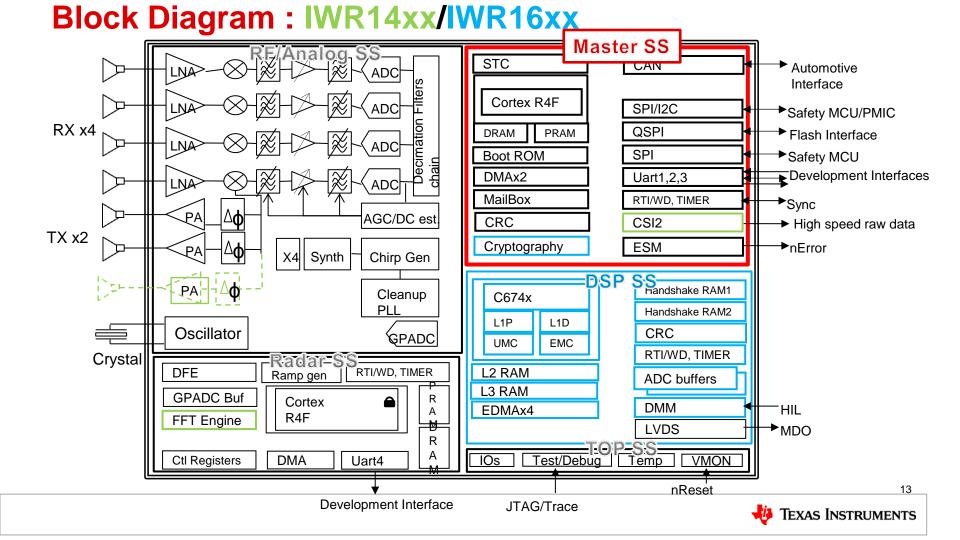
Block Diagram : IWR14xx/IWR16xx



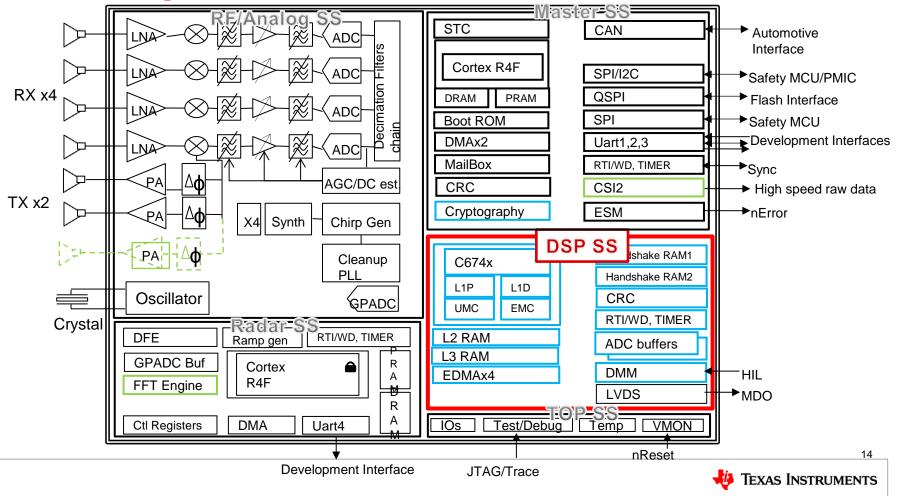
Block Diagram : IWR14xx/IWR16xx RF/Analog SS STC CAN Automotive Decimation Filters Interface Cortex R4F SPI/I2C ◆Safety MCU/PMIC RX x4 **QSPI** DRAM **PRAM** Flash Interface **Boot ROM** SPI ►Safety MCU ▶ Development Interfaces DMAx2 Uart1,2,3 1 MailBox RTI/WD, TIMER **►**Sync $\nabla \Phi$ PΑ AGC/DC est CRC CSI2 High speed raw data TX x2 Cryptography **ESM →**nError JPΑ Synth Chirp Gen SS Handshake RAM1 DSP PA- Δ**Φ** Cleanup C674x PLL Handshake RAM2 L1P L1D Oscillator CRC **GPADC** UMC EMC RTI/WD, TIMER Crystal Radar-SS DFE RTI/WD, TIMER L2 RAM Ramp gen ADC buffers L3 RAM **GPADC Buf** R Cortex DMM EDMAx4 HIL R4F FFT Engine LVDS **►**MDO Ctl Registers DMA IOs Test/Debug VMON Uart4 emp nReset 11 **Development Interface** JTAG/Trace **TEXAS INSTRUMENTS**

Block Diagram : IWR14xx/IWR16xx





Block Diagram : IWR14xx/IWR16xx

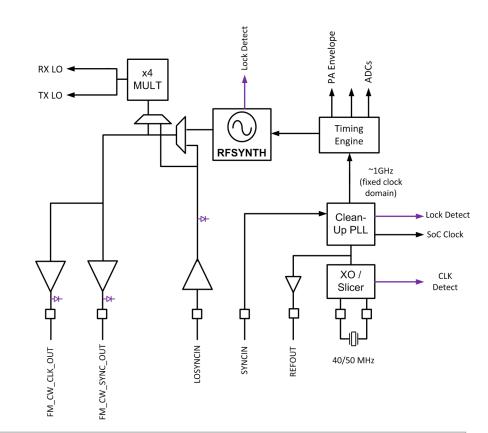


RF and Analog Subsystem

Block Diagram : IWR14xx/IWR16xx RF/Analog SS STC CAN Automotive Decimation Filters Interface Cortex R4F SPI/I2C ◆Safety MCU/PMIC RX x4 **QSPI** DRAM **PRAM** Flash Interface **Boot ROM** SPI Safety MCU ▶ Development Interfaces DMAx2 Uart1,2,3 1 MailBox RTI/WD, TIMER **►**Sync $\nabla \Phi$ PΑ AGC/DC est CRC CSI2 High speed raw data TX x2 Cryptography **ESM →**nError JPΑ Synth Chirp Gen S-S-Handshake RAM1 DSP PA- Δ**Φ** Cleanup C674x PLL Handshake RAM2 L1P L1D Oscillator CRC **GPADC** UMC EMC RTI/WD, TIMER Crystal Radar-SS DFE RTI/WD, TIMER L2 RAM Ramp gen ADC buffers L3 RAM **GPADC Buf** R Cortex DMM EDMAx4 HIL R4F FFT Engine LVDS **►**MDO Ctl Registers DMA IOs Test/Debug VMON Uart4 emp nReset 16 **Development Interface** JTAG/Trace **TEXAS INSTRUMENTS**

RF and Analog: Clock Subsystem

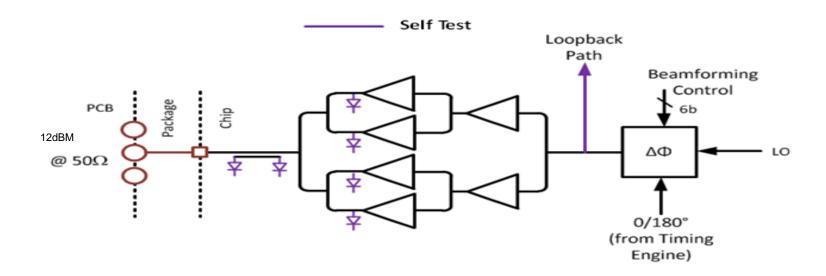
- Supports 40MHz crystal.
- Clean-up PLL provides highfrequency reference for modulated synthesizer and clocks to digital, ADCs.
- FMCW waveforms synthesized in a 19-20.25GHz closed loop frequency synthesizer.





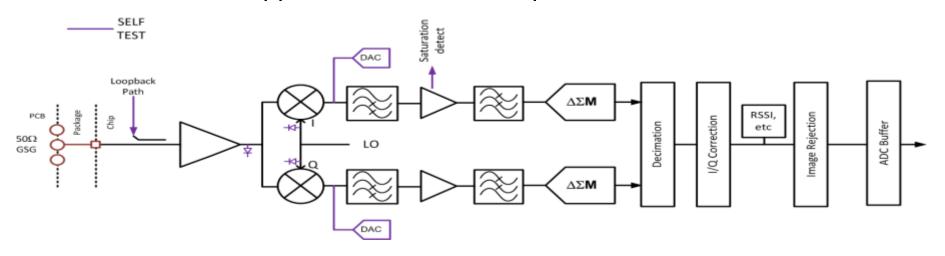
RF and Analog: Transmit Subsystem

- Single-ended antenna interface matched to a 50 ohm GCPW on the PCB at the edge of the package.
- Power/impedance monitors at the edge of the die.
- Binary (0/180) phase modulation for MIMO radar and interference mitigation.



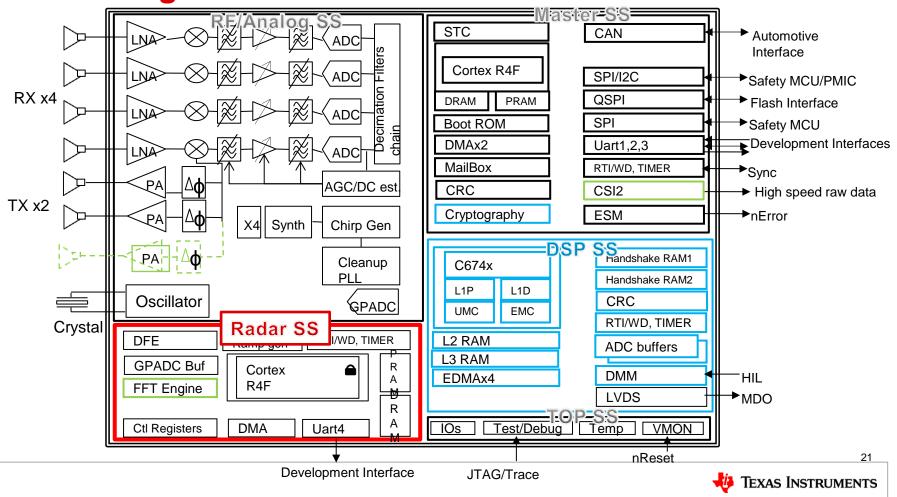
RF and Analog: Receive Subsystem

- Complex (I/Q) baseband.
- Programmable high pass filters to compensate for channel loss.
- CTSDM ADC supports IF bandwidths up to 15MHz.



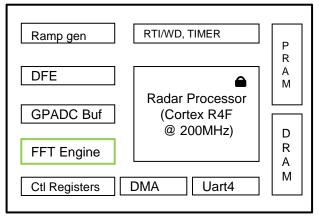
Radar Subsystem (aka BSS)

Block Diagram : IWR14xx/IWR16xx



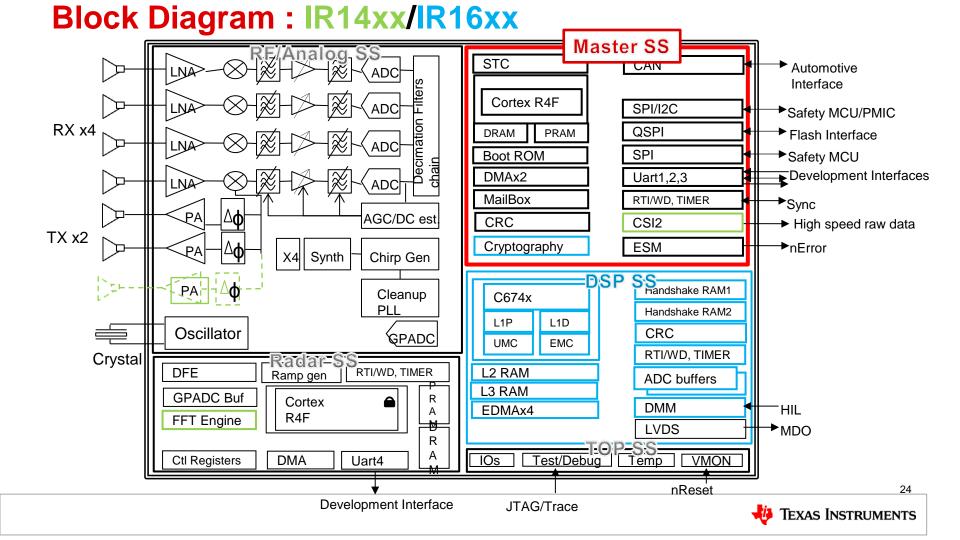
Radar Subsystem (BSS)

- Also known as the BSS, includes the DFE (digital front-end) and Ramp Generator
- Also includes a dedicated Cortex R4F MCU for configuration, monitoring, and calibration of the low-level RF/Analog components
- Access to the Radar subsystem provided through hardware mailboxes and a well defined API



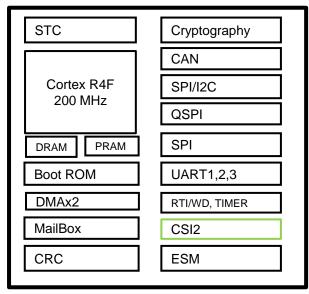
Radar Subsystem

Master Subsystem (MSS)



Master (Control) Subsystem

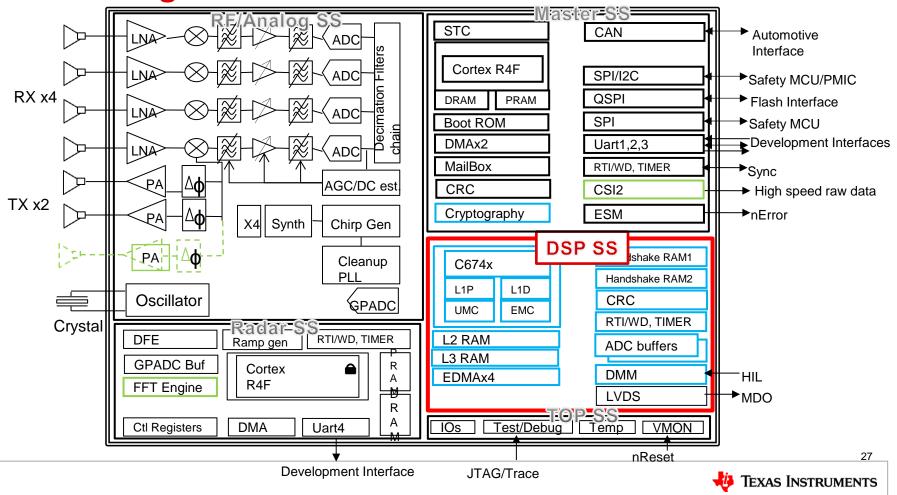
- The MSS includes an ARM Cortex R4F processor clocked at 200 MHz for running application code.
- User application running on MSS controls overall operation of the device, including Radar subsystem (BSS) control via well-defined API messages and perform radar signal processing.
- This subsystem also includes the various external interfaces available on the 14 or 16xx devices.



Master Subsystem

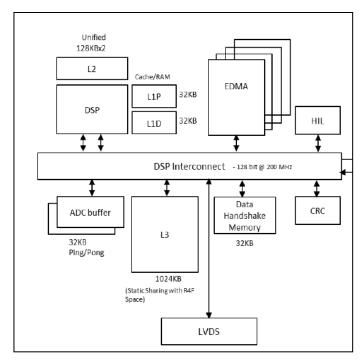
DSP Subsystem (DSS)

Block Diagram : IWR14xx/IWR16xx



DSP Subsystem (DSS): IWR16xx only

- C674x DSP clocked at 600 MHz for advanced Radar signal processing
- High bandwidth interconnect for high performance (128-bit, 200MHz)
- 256 KB L2 and 1 MB of L3 memory
- Four DMAs for data transfer, LVDS interface for Measurement data output, ADC buffers, CRC engine and data handshake memory

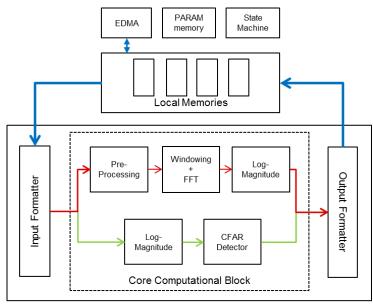


DSP Subsystem (DSS)

Radar Hardware Accelerator

Radar Hardware Accelerator

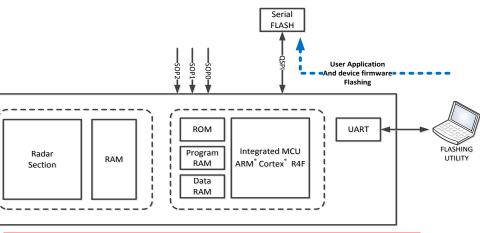
- Accelerates FFT and CFAR detection operations
- Simple pre-FFT processing and Magnitude and Log-Magnitude computation capability
- Flexible data flow and data sample arrangement to support efficient multi-dimensional FFT operations and transpose accesses
- Chaining and Looping mechanism to sequence accelerator operations with minimal intervention from the main processor
- CFAR-CA detector support (linear and logarithmic)



Radar Hardware Accelerator

Boot Modes

Boot Modes

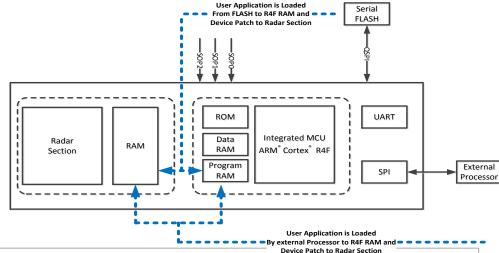


Flashing Mode:

- Bootloader enables the UART driver
- Expects a data stream comprising of User Application (Binary Image)
- Loads data to appropriate sections of the serial FLASH

Functional Mode:

- Bootloader looks for a valid image in the serial flash memory, interfaced over the QSPI port.
- Bootloader transfers the same to Master System's memory sub-system





Software Platform

mmWave Software

Simplified evaluation and development

mmWave SDK

Includes:

- TI RTOS
- Drivers
 - SPI
 - CAN
 - · LVDS / CSI-2
 - EDMA
 - UART
 - I2C
 - GPIO
 - Timers
 - FFT HW
- Signal Processing Library
 - On DSP
 - · On HW Accelerator
- mmWaveAPI
- mmWaveLink
- mmWaveLib

mmWave Examples

- · TI Designs:
 - Power-Optimized Field Transmitter
 - · Traffic monitoring
- Examples:
 - mmWaveDemo (OOB)
- Labs:
 - Water Vs Ground Lab
 - Vital Sign Lab

mmWave Studio

Includes:

- System Estimator define chirp configuration through abstracted parameters like max range, minimum range, etc
- Capture capture raw ADC data from capture HW onto the PC



Simplified mmWave sensor configuration

 Generate mmWave sensor chirp configurations through system-level parameters to control [Range, Velocity, Angle] output

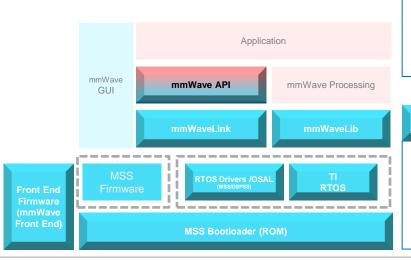
Internal RF Chirn

mmWave OOB GUI for visualization of the output

		I	Configuration
Customer Inputs			Range FFT Size
Maximum Range	Minimum Object Size	mmWave Studio	Doppler FFT Size
Minimum Range / Resolution	Frame Rate		Chirp Duration & Ramp Slope
Maximum Velocity	Sensitivity		Chirp Bandwidth
Minimum Velocity / Resolution	Field of View		Chirp Ramp Slope
Device (IWR14x vs IWR16x)	Frequency Band		+40 other parameters

mmWave SDK – The TI components

Modular design Well defined APIs Documentation – doxygen, release notes, user guide MISRA-C compatibility for all foundational components Applicable for IWR1443/IWR1642



RTOS Drivers

- Encapsulate the functionality of the hardware IPs in the SOC.
- Provide a well defined API to the higher layers.
- OS-agnostic via the OSAL layer

OSAI

- An abstraction layer for some of the common OS services. (Semaphore, Interrupts, Clock)
- Sample TI RTOS based port in mmWaveSDK
- Customers can port the OSAL for their custom OS, as per their requirements

BSS Firmware

- ROM Firmware for mmWave Front End
- Provides well defined APIs to configure, start and monitor mmWaye Front End
- Communicates with MSS via Mailbox and proprietary protocol

mmWaveLink

- Low level control for mmWave Front End
- Communicates over Mailbox to BSS (front end)
- Implements the communication protocol between the BIST subsystem and Master subsystem

mmWave API

- Simple APIs for application to perform the task of radar sensing
- High level control for mmWave Front End and DSS
- Runs on top of mmWaveLink/IPC and Drivers.

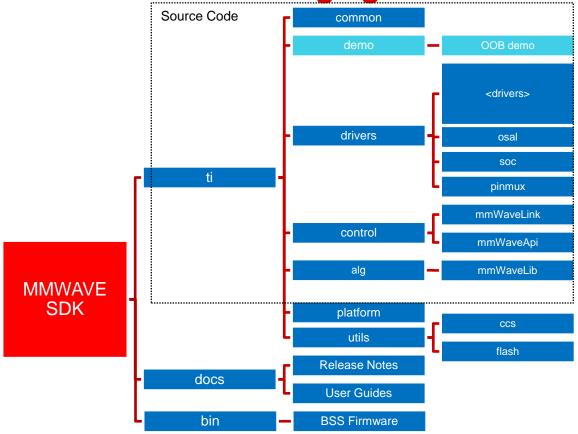
mmWayel ib

- Provides functions for elements or sub functions of typical radar processing chain
- Optimized for C674x
- Accelerate customer code development and reduce SW effort to achieve a working radar processing chain

3



mmWave SDK - Packaging



- Uses TI compiler tools (Cortex-R4F, C674X) provided as part of CCS
- Demo built over TI RTOS
- Simple makefile based build system

Learn more about Industrial mmWave Sensors

- Learn more about IWR1x devices, please visit the product pages
 - IWR1443: http://www.ti.com/product/IWR1443
 - IWR1642: http://www.ti.com/product/IWR1642
- Get started evaluating the platform with IWR1x EVMs, purchase EVM at
 - IWR1443 EVM: http://www.ti.com/tool/IWR1443BOOST
 - IWR1642 EVM: http://www.ti.com/tool/IWR1642BOOST
- Download mmWave SDK @ http://www.ti.com/tool/MMWAVE-SDK
- Ask question on TI's E2E forum @ http://e2e.ti.com



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