

D7	D6	D5	D4	D3	D2	D1	D0	Q2	Q1	Q0
X	X	X	X	X	X	X	1	0	0	0
X	X	X	X	X	X	1	0	0	0	1
X	X	X	X	X	1	0	0	0	1	0
X	X	X	X	1	0	0	0	0	1	1
X	X	X	1	0	0	0	0	1	0	0
X	X	1	0	0	0	0	0	1	0	1
X	1	0	0	0	0	0	0	1	1	0
1	0	0	0	0	0	0	0	1	1	1

第一种 CASE 的写法

6.8.1 Register

```

module encoder
  (D0, D1, D2, D3, D4, D5, D6, D7,
   Q2Q1Q0);
  input [7:0] D0, D1, D2, D3, D4, D5, D6, D7;
  output [2:0] Q2Q1Q0;
  reg [2:0] Q2Q1Q0;

  always @(*)
    begin
      Q2Q1Q0 = 3'b000;
      case (1'b1)
        D0: Q2Q1Q0 = 3'b000;
        D1: Q2Q1Q0 = 3'b001;
        D2: Q2Q1Q0 = 3'b010;
        D3: Q2Q1Q0 = 3'b011;
        D4: Q2Q1Q0 = 3'b100;
        D5: Q2Q1Q0 = 3'b101;
        D6: Q2Q1Q0 = 3'b110;
        D7: Q2Q1Q0 = 3'b111;
      endcase
    end
  endmodule

```

6.8.2 Digital Design – Building Blocks

Priority Encoder Verilog RTL

```

module priority_encoder
  (D0, D1, D2, D3, D4, D5, D6, D7,
   Q2Q1Q0);
  input [7:0] D0, D1, D2, D3, D4, D5, D6, D7;
  output [2:0] Q2Q1Q0;
  reg [2:0] Q2Q1Q0;

  always @(*)
    begin
      Q2Q1Q0 = 3'b000;
      if (D0) Q2Q1Q0 = 3'b000;
      else if(D1) Q2Q1Q0 = 3'b001;
      else if(D2) Q2Q1Q0 = 3'b010;
      else if(D3) Q2Q1Q0 = 3'b011;
      else if(D4) Q2Q1Q0 = 3'b100;
      else if(D5) Q2Q1Q0 = 3'b101;
      else if(D6) Q2Q1Q0 = 3'b110;
      else if(D7) Q2Q1Q0 = 3'b111;
    end
  endmodule

```

第二种 IF – ELSE 的写法