Agilent Technologies

Ground Bounce Basics and Best Practices

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Introduction:

Most electronic circuit designers are now familiar with ground bounce problems internal to integrated circuits and the ground bounce that can occur between an IC and the PC board. However, many PC board designers and board test developers are unfamiliar with ground bounce problems related to test. Ground bounce, whether at the IC, PC board, or system level is a transient voltage difference between the ground reference points in two parts of a circuit. In all cases the cause is a transient current (generally due to switching) flowing through the ground path impedance between the two portions of the circuit. As with the familiar ground bounce internal to an IC, ground bounce during board test can result in unexpected, and sometimes intermittent, behavior of the circuit being tested.[1]

This article begins with a description of the physical properties that result in ground bounce during board test, and some real-world examples. Following is a discussion of common circuit design, fixture construction, test system, and test technique related features that often combine to cause ground bounce problems during board test. There is a discussion of best practices for the board designer and the test engineer to minimize the likelihood of ground bounce induced test problems. A short description of boundary scan testing and ground bounce relationships completes the discussion.

The author first encountered board test ground bounce in the early 1990's when advanced CMOS logic parts became prevalent. These first experiences mostly involved library tests on large ASIC devices, though the phenomenon could even be found in the tests of smaller SSI parts. Today, the most commonly encountered board test ground bounce problems involve boundary scan tests. With boundary scan tests becoming increasingly common, it is important to be familiar with the causes of ground bounce and techniques used to control it.

Understanding Ground Bounce:

Board test ground bounce is a transient voltage differential between the test system ground and the device-under-test (DUT) ground. The mechanism for this, and how ground bounce impacts board test, are described below with reference to the included drawings. The first drawing illustrates the most common situation for ground bounce, while the second illustrates another situation that increases the likelihood of ground bounce related test problems.

Reference Figure 1: Basic Ground Bounce

The most common, and basic, form of ground bounce occurs when the DUT board has multiple output pins change state simultaneously due to some stimulus. This is common when performing boundary scan tests. During a boundary scan test serial signal data is shifted into the DUT, and at the time of the update command all of the outputs in the chain assume their new state. It is common for a boundary scan chain to have hundreds or even thousands of pins involved in a test. For the frames (or vectors) that have a substantially equal number of pins transitioning from a "0" to a "1" as transition from a "1" to a "0" the probability of ground bounce problems is reduced. This is the case for several of the frames in a typical boundary scan interconnect test,

[1] Fairchild Semiconductor application note 640 "*Understanding and Minimizing Ground Bounce*" gives excellent descriptions of ground bounce at the IC level. Another excellect reference is "*High-Speed Digital Design: A Handbook of Black Magic*" by Howard Johnson and Martin Graham © 1993 Prentic Hall – section 2.4.1 specifically covers ground bounce at the IC level.

especially when the number of pins involved in the test is nearly equal to a power of two. However, there are frames in every boundary scan test where a substantial portion of the pins will transition in the same direction.

As the DUT output pins transition, current Ircv flows through the fixture wiring to charge the input capacitance of the receiver in the board tester. (In this simplified diagram Crcv is a combination of the fixture wiring capacitance, the capacitance of the receiver circuit itself, and any trace and relay capacitance in the tester.) This current then returns from the tester to the DUT through the ground wires in the fixture. The current needed to charge the capacitance on the pin card of the tester is proportional to the edge speed of the output of the DUT as:

$$I = C\frac{dV}{dt}$$

The impedance of the wire in the fixture limits this current somewhat. This impedance is generally dominated by the inductance of the wire, so we will ignore the resistance. The voltage developed across the inductance (Lrcv) is given by:

$$V = L\frac{dI}{dt}$$

If the circuit consisted of ideal components, the DUT source would switch in zero time and the full voltage would appear across the inductor because the voltage across a capacitor and the current through an inductor cannot change instantaneously. There would then be a pure exponential settling of the capacitor voltage to the source voltage, and the inductor current to zero. Since the components are not ideal, a capacitor current and an inductor voltage with a sharp rise time and a long exponential decay approximate the actual situation.

The return current flowing in the ground path between the tester and the DUT causes a similar transient voltage to appear across the inductance of the ground path. This voltage is known as ground bounce. Usually (but not always) the inductance of the ground path is smaller than the inductance of the receiver connection, and the ground bounce voltage will be less than the voltage across the receiver wire inductance.

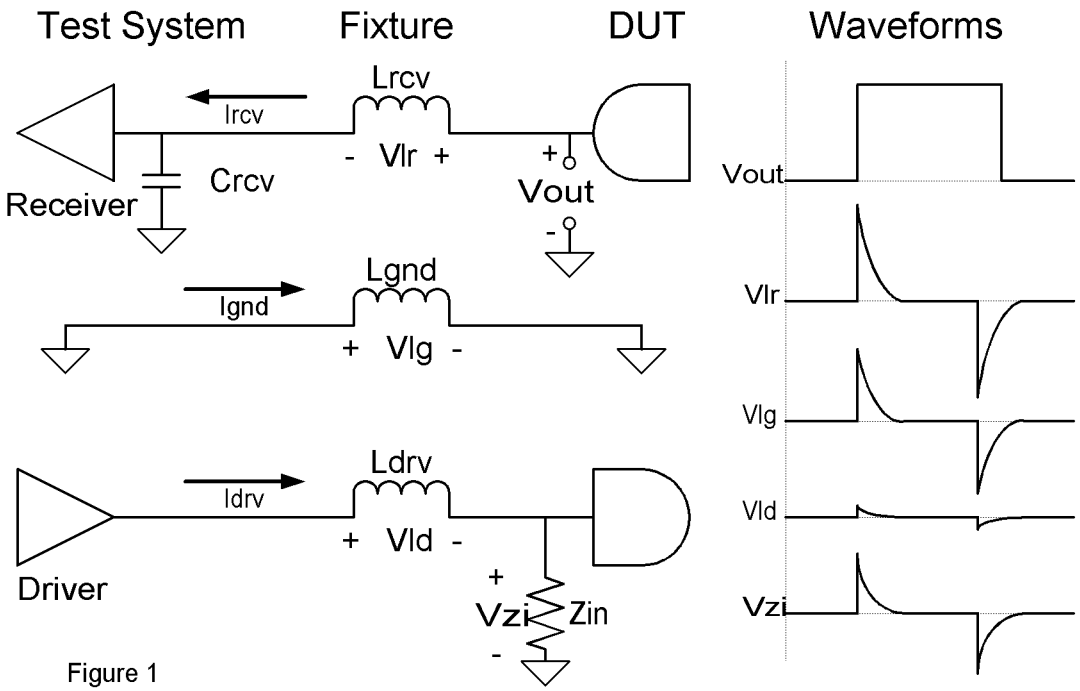


Figure 1

If the only components in the circuit are the DUT and the receivers on the tester, this ground bounce voltage will not cause any problems; unfortunately, this is rarely the case. There are usually some signals provided by the tester to stimulate and control the DUT in order to perform the test. The driver at the bottom of Figure 1 is an example of one of these lines. Assuming that

this driver is static at this point in the test, its output voltage is fixed with respect to the tester ground and the driver impedance is usually quite low (<1 ohm). Since the driver state is static, the input to the DUT should also be static at this point in the test; however, there is a voltage between the DUT ground and the tester ground. A potential equal to the ground bounce voltage must appear somewhere in the driver path. If the input impedance of the DUT, Zin, is small (<10 ohms) most of the voltage will drop across the fixture wire inductance, Ldrv. If Zin is not small, most of the ground bounce voltage will appear across Zin and will be seen by the input of the DUT. If the transient voltage at the input of the DUT is sufficiently large to cross the logic switching threshold, and lasts a sufficient time, the output of the gate will switch causing a transient pulse. Herein lies the problem with ground bounce!

When the driver signal is connected to a signal that is an input of a sequential circuit this added pulse will change the expected state of the DUT circuit, resulting in non-predicted (and generally failing) activity. Examples of state determining (or edge-sensitive) lines in sequential circuits are the clock and reset lines of state machines. The most common example in terms of board test problems today are the TCK and TRST lines of boundary scan chains. It is important to note that non-state determining signal lines, for example address lines for a memory device, are not susceptible to ground bounce (unless a related state determining line is also affected). This is because their behavior will settle before the tester captures the down-stream output state of the circuit.

It is rare for the Zin of an edge-sensitive line to be low. This will occur when there is a signal on the DUT also driving that signal (such as an on-board clock), or when the normal use of the line allows for a slow response (such as a reset line that is de-bounced with a capacitor). In either of these cases the signal will be unlikely to respond to ground bounce events.

The actual ground bounce voltage between the DUT ground and tester ground is almost impossible to measure directly because of the distances between the two points and the high speed transient nature of the signal. The consequences of ground bounce are much easier to measure. With a static driver signal connected to a high impedance input node on the DUT it is easy to measure the resulting disturbance that results at the DUT input (relative to DUT ground). This is how ground bounce is most commonly, and correctly, measured in the board test environment.

Reference Figure 2: Ground Bounce with Overdrive

Figure 2 illustrates an extension of the circuit in Figure 1 that exacerbates ground bounce problems. In this case pin drivers in the tester are being used to overdrive[2] an output on the DUT. At points in the test where the pin drivers change state there is usually not a serious problem with ground bounce, even though there are large currents flowing. This is because the pin drivers in the tester intentionally have slow edge transition (slew) rates.

The problem in this case occurs at points in the test where the drivers are placed in a high impedance state (also called tri-state™ [3]). The pin drivers, of necessity, enter the high impedance state very rapidly, allowing the DUT outputs to assume their normal state at a slew rate limited only by the output speed of the DUT device. How is this worse than the case where the DUT outputs switch normally? Consider the state of the circuit just prior to the drivers entering tri-state™, and then shortly after. In the initial state the driver is sourcing a large current to force the output of the DUT to a logic high while the DUT output would normally be low. Therefore Ipe is a large negative current. This current must return from the DUT to the tester through the ground wires in the fixture, resulting in a similar large negative Ignd. Because the circuit has achieved steady state there will be no voltages across the inductors and no current flowing in Cpe. A small voltage will exist between the DUT ground and the tester ground due to

[2] Overdrive is a test technique where a low impedance driver in the tester is used to temporarily force an output pin on a DUT device to a specific logic state, even if the device would normally be in the opposite state. This is done to apply known input patterns to another device being tested "downstream" of the device being overdriven.
[3] National Semiconductor

the resistance in the ground wires. After the pin drivers achieve the high impedance state there will be a transient current flow from the DUT device to charge Cpe to the logic low state, similar to the current charging Crcv in Figure 1. During the short time between these two states dramatic changes are taking place. The voltage that develops across Lpe will be large because the change in Ipe is large. Ignd also changes from a large negative value to a small (transient) positive value resulting in a large voltage, Vlg, developing between the DUT ground and the tester ground. Cpe being the parallel combination of the receiver input capacitance and the driver tri-state™ capacitance further exacerbates this.

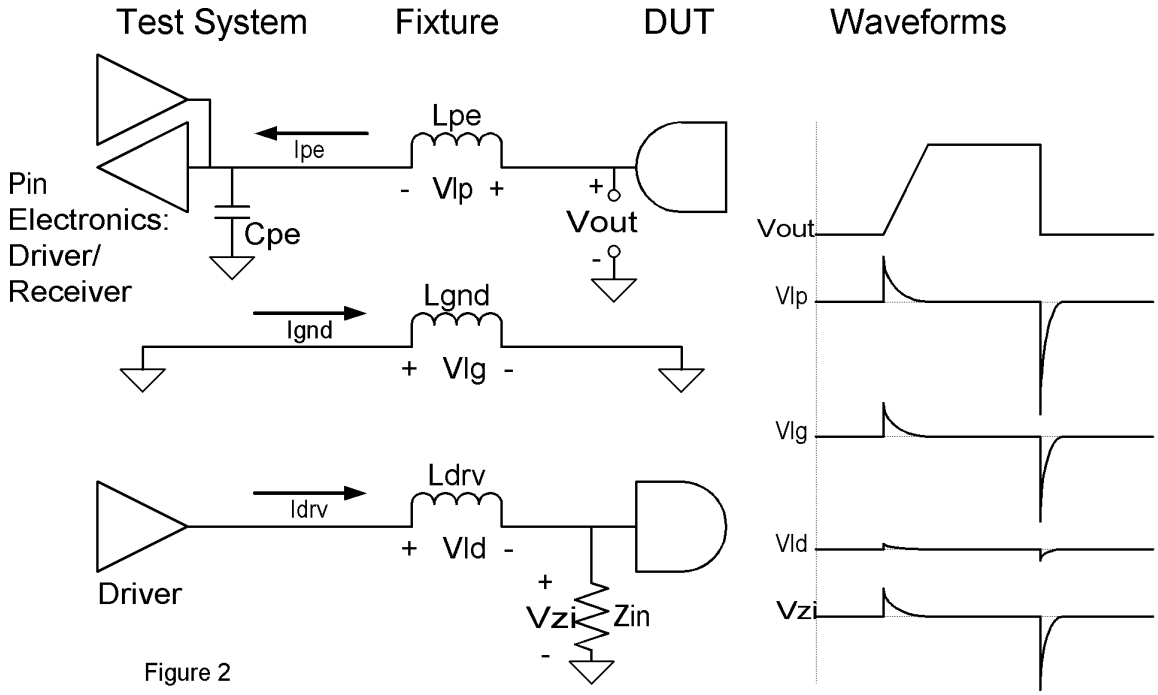
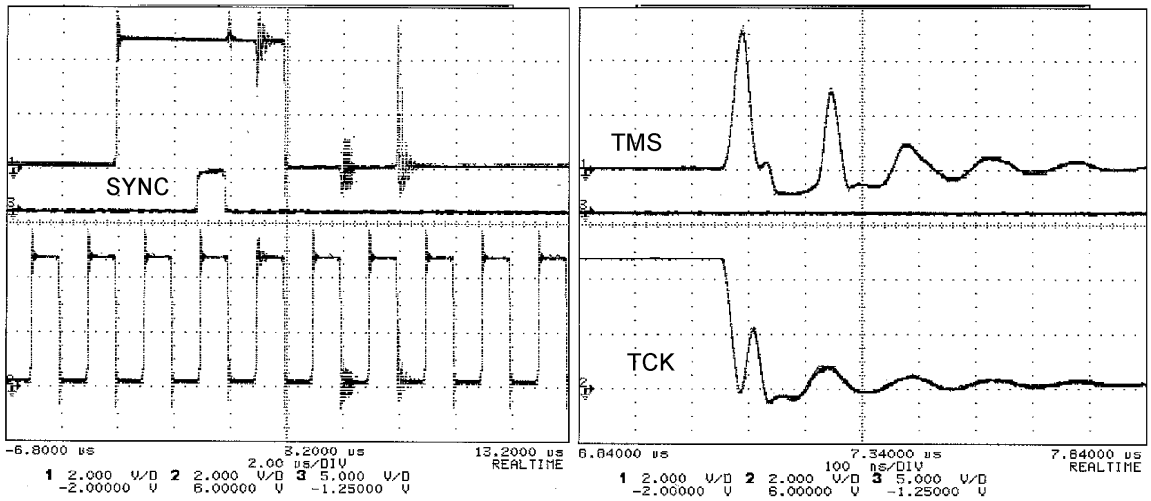


Figure 2

This sequence of events can result in dramatic ground bounce voltages. This used to happen occasionally with library tests of large parts when the "up-stream" devices could not be disabled by placing their output pins in a high impedance state. Today this occurs occasionally when large numbers of pins must be overdriven in order to test the input pins of boundary scan devices during connect tests. This particular situation can be avoided by providing ways to disable the up-stream devices so that they do not have to be overdriven.

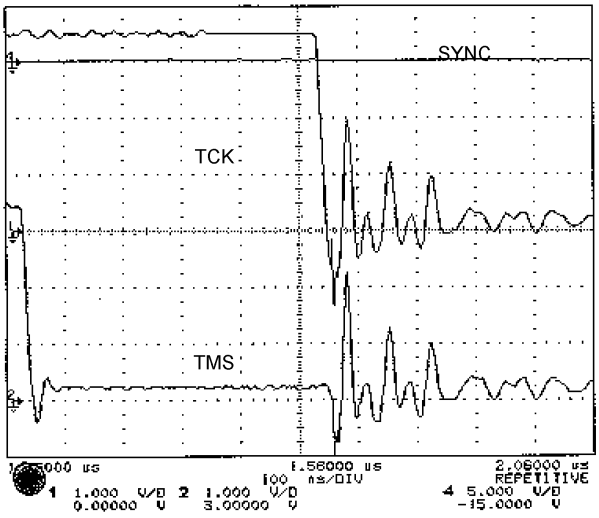
Examples of Actual Ground Bounce Signals:

The oscilloscope pictures, shown below in Example 1, illustrate the ground bounce occurring during the boundary scan connect test of a telecom rack card. At this point in the test, 155 device pins are being tested – of these, 87 are input pins which must be overdriven because the up-stream device cannot be disabled. At the falling edge of TCK, shown in the expanded view on the right side, the test system drivers are placed in tri-state™. The ground bounce, as measured on TMS, is in excess of five volts. The ground bounce affecting TCK is slightly more than two volts. (The differences are due to the impedances of the two signals on the DUT, and localized differences in ground path impedance between the two signals and their respective pin cards in the test system.) Normally a spike on TMS (a non edge-sensitive signal) would not be a problem. Since TCK also has a spike exceeding the device threshold, the logic "1" on TMS causes the boundary scan state machine within the DUT to advance to an unexpected state. This results in a failing test. The root cause of this test failure is ground access probe points that are not near the signal probe access points. It is possible to correct the problem by breaking up the test.



Example 1

Example 2 illustrates a similar situation existing during the boundary scan interconnect test on a small VXI card. The board has three relatively small CPLD parts tested with boundary scan. The interconnect test does not involve a large number of nodes with probes on them, but the ground access to the board is very poor. The board design allows only eleven ground probe access points, and seven of them are required for power supply connections. This leaves only four ground probes available to connect to pin card grounds on the test system. This results in a consistently failing test which is difficult to debug.



Example 2

Variables Affecting Ground Bounce:

Many of the major factors affecting the level of ground bounce can be easily seen from the examples discussed around figures 1 & 2. A few additional factors are not so obvious until further study is made of ground bounce. The most important of both of these are discussed in the following paragraphs.

The load of the test system on the DUT affects ground bounce directly. The larger the capacitance of the test system, the larger ground bounce will be. There is little the designer or test developer can do to change this, since the test platform is usually beyond their control. Lumped loads, such as those at the test system, have a larger affect on the ground bounce level than an equivalent distributed load (see the Fairchild paper referenced in footnote 1).

Higher speeds make ground bounce worse. Here the concern is not MHz, but the output characteristics of the DUT devices. Outputs that switch rapidly (large dV/dt) and can provide large output currents (large dI/dt) will cause greater ground bounce. The push for faster system speeds (MHz) drives logic families to higher switching speeds (dV/dt). Board designers can reduce test related ground bounce problems by using the slowest logic family (dV/dt) that will allow them to achieve their required system speed (MHz). It is important to note that the lower supply voltages used in many new systems help with this by reducing the voltage swing and therefore the dV portion of the dV/dt – however the noise margin is also reduced. Another area where designers can help, especially when using programmable logic devices, is to choose output cells with lower drive currents.

Tests with large numbers of outputs switching simultaneously exacerbate ground bounce problems because there is a larger transient current in the ground return. This can sometimes be mitigated for large library tests by selecting test patterns that limit the number of pins switching at one time, or test patterns that balance the numbers of rising and falling edges. Large boundary scan tests are particularly susceptible to ground bounce problems, because the test patterns involve large numbers of pins changing state simultaneously. Some board test systems, such as the Agilent 3070, provide tools to break up large boundary scan connect tests to control ground bounce without adversely affecting test coverage.

Pattern sensitivity and DUT sensitivity are both common with ground bounce. If the victim signal on the DUT has its threshold very near the peak of the ground bounce signal intermittent failures are common. In this event making small changes in the test can result in the test consistently passing or failing. The difference between two DUT boards can easily result in different behavior since one may have slightly stronger output drive or a lower threshold voltage (still well within the normal device fabrication limits) and this DUT will be more prone to failing the test. Also small changes in the test pattern, such as may occur if devices are re-ordered in a boundary scan test, or during an ECO, can result in a formerly stable test becoming intermittent. It is not possible to totally avoid this, but following good design for test (DFT) procedures will reduce the number of these incidents.

Modern designs that employ multiple logic families and multiple logic power supply voltages are particularly at risk for ground bounce. Consider for example a board that uses 3.3 volt logic for I/O and peripheral functions, and has a processor core that is operating at 1.8 volts. Because of the larger swings the 3.3 volt parts are likely to have a higher output slew rate (dV/dt) than the 1.8 volt parts, even thought the 1.8 volt core may be capable of operating at higher system clock rates. If a boundary scan test were to involve parts from both logic families (a common occurrence) any edge-sensitive inputs on the 1.8 volt devices will be much more susceptible to ground bounce than edge-sensitive inputs on the 3.3 volt devices because of the lower noise margin. If there is a choice during the design or test development between selecting an edge-sensitive input connection to the test system, it should be made to the logic family that has the largest noise immunity. It is important to note that this noise immunity has two major parts. The first is how far away the switching threshold is from the normal logic levels. The second is related to the maximum clock rate, or minimum propagation delay of the part – faster parts will respond to a narrow glitch that a slower part would ignore.

Selecting the probe access point on the DUT can be a tricky trade-off for either the board designer or the board test developer. Connecting test system receivers as far as possible from the driving point in the DUT circuit will reduce ground bounce (though generally only slightly). For the best signal fidelity when the test system is driving a net, the probe point should be taken at the output pin of the source on the DUT. Bi-directional pins obviously complicate this! Overall, if there is probe location choice during either design or test development, it is best to choose the location at the driving point for uni-directional nets.

The IEEE 1149.1 standard for boundary scan requires that all output pins on a device be able to transition simultaneously. For many real world parts this is far outside of their normal operating region, especially for parts in high pin count packages. During test development it is important to review the data sheets of all parts to determine if there is a limit on the number of pins that can be allowed to transition simultaneously. This is a common specification for programmable logic

devices in large packages. Some form of boundary scan test break up should be used if the device specifications recommend against having all of the output pins (as defined for the application) transition simultaneously.

Ground bounce in ICs is generally mirrored by power supply bounce. Supply bounce is often less of a problem in ICs than is ground bounce because many logic families have more noise margin on the high side than on the low side. This is less common with the lower voltage families that are mostly symmetrical. Supply bounce is much less pronounced in board test because the DUT power supplies are rarely referenced directly to the pin cards where digital measurements are made. The added loop distance in the power supply return to the pin cards greatly reduces the effects of power supply bounce.

Ground Bounce Best Practices:

The following paragraphs describe best practice, or design for test, techniques. Some of these are described above, and many are applications of the principles described earlier in the section on understanding ground bounce. These techniques fall into three areas: things that are mainly under the control of the board designer, things that are mainly under the control of the board test developer, and things that they can both influence in cooperation. These techniques are relatively easy and low cost if included in the up front planning of the board designer and the board test programmer – trying to retrofit them after a problem is found can range from difficult or impractical to nearly impossible.

Board Designer Domain:

When developing new parts for a board, including ASICs and programmable logic parts, it is helpful for the designer to choose the lowest current drive output cells that are consistent with good operation in the part's native application. This reduces the amount of current available to rapidly charge the system capacitance, directly reducing ground bounce. This also applies to the selection of the logic family for smaller SSI and MSI functions such as bus drivers. In addition to the test benefits, this can reduce noise problems on the DUT operating in its normal environment and will reduce overall power dissipation.

A technique frequently applied to reducing ground bounce problems within ICs and at the board level is to stagger the timing of output pins on a device. Spreading the switching time of a large number of outputs over a period of hundreds of picoseconds to a few nanoseconds can substantially reduce ground bounce at the IC level. This works well when the round trip time for the incident wave to reach its destination, and return through the ground path, is less than or equal to the switching time spread. As an example, for edges spread over a 2 nanosecond period the distance between the source and destination should be less than about six inches (15 cm) with a solid ground plane as the return path. The round trip time, as shown in the example waveforms, for board test ground bounce is much larger than a few nanoseconds. With sufficient edge dispersion this technique would work for board test related ground bounce, but this would seriously compromise normal performance.

Many boards provide buffers for at least some of the boundary scan ports because of the large fan-out of the TCK, TMS, and TRST signals. Properly implemented, this can be effective in reducing ground bounce problems. It is critical to remember during PC board layout that, while these signals may not operate at a high clock frequency, they require careful transmission line consideration because the edge rate of the buffer parts is generally very fast and these lines (especially TCK and TRST) are sensitive to edge anomalies. When possible, the board designer should choose a relatively slow (and low drive current) part for this buffer. This will reduce signal fidelity problems, as will using multiple buffers for each signal to keep routes short. Additional benefit can be gained by having the board designer work with the board test developer to implement a clean path from the test system for the boundary scan signals. Depending on the characteristics of the test system, this may involve controlled impedance connections between the tester and the DUT, or adding some loading at the DUT on these signals to lower the input impedance, reducing sensitivity to ground bounce.

Joint Board Designer and Board Test Developer Domain:

Ground bounce disturbances of a specific edge-sensitive signal on the DUT can be reduced by routing the edge-sensitive signal between the DUT and the test system pin card through a controlled impedance line (such as twisted pair or coax). The controlled impedance line must connect to ground close to the signal connections at both ends of the line. This requires a ground probe point near the edge-sensitive signal probe point on the DUT. By supplying additional ground probe points near edge-sensitive signals the board designer provides the test developer with a powerful tool.

Well distributed access to ground probe points on the DUT is one of the most important factors in reducing overall ground bounce. The density of ground probe access points in any area of the board should reflect the signal probe access density in that area. This can run counter to efforts to reduce the probe force per unit area on the DUT, and both of these needs must be considered. Some of the very worst ground bounce problems the author has seen were on boards that had a reasonable number of ground probe access points relative to the number of signal probe access points, but with the ground and signal access points widely separated on the board. One particular telecom rack card (see Example 1 earlier) had a boundary scan test for a series of BGA parts all located along one edge of the board with signal access provided at the BGA pad vias. All of the ground access to the card was located on the connector along the opposite edge of the card. Ground bounce was a serious (though recoverable) problem despite a numerically sufficient number of ground pins. A useful metric for ground access is to overlay the board with a grid of squares roughly 1.4 inches (3.5 cm) on a side – then count the signal and ground probe access points in each square. There should be roughly one ground probe point for every five signal probe points in each square.

Whenever possible, devices should be provided with a method for disabling their output pins. This reduces the need to overdrive during testing, and this translates into fewer opportunities for ground bounce problems. The designer can influence this by providing disable capability in ASIC parts and programmable logic parts, and by using a resistor to bias enable pins rather than tying them directly to supplies. The board test programmer then must utilize this disable capability to best advantage. In addition to reduced ground bounce, these efforts usually result in improved test coverage and better diagnostics.

Board Test Developer Domain:

It is important to make use of as many ground pins on the test system pin cards as is possible. This is the dual of providing good ground access to the DUT. In general, if there are a sufficient number of ground access points on the DUT, the test system fixture design software will make good use of the ground pins on the pin cards. When there are an insufficient number of ground access points on the DUT, the ground connectivity to the pin cards may be severely compromised as well.

The addition of a ground plane to the fixture can be a significant factor in reducing the potential for ground bounce. This is most effective in those situations where the other grounding rules have been followed. When there is good to excellent ground access to the DUT, and there are no access problems to the ground pins on the test system pin cards, a ground plane can noticeably reduce the ground return path impedance, and the observed ground bounce. In cases where there is poor ground access to the DUT, a ground plane will generally provide little advantage. The addition of a ground plane to a fixture is not a trivial matter – however, for boards that are difficult to test, this may be the difference between success and failure. If experience indicates a high risk of ground bounce problems for a new DUT, the savings in debug time may easily justify the added cost of a ground plane. A ground plane is also advantageous in fixtures with large wire volumes, as it nearly eliminates ground wires in the fixture.

There is a way to get some advantage from a ground plane on boards that have poor ground probe access, especially if it is in a limited area of a generally accessible board. If the fixture ground plane is very close to the DUT ground or power plane the capacitance between the fixture plane and the DUT plane can help reduce the ground path impedance. If this is done, it is best to

use an auxiliary ground plane near the DUT in addition to a ground plane inside the fixture. This is recommended only as a method of last resort, rather than a design plan to lower the required ground access to the DUT board.

Large boundary scan connect tests can be successfully split into several smaller tests. The Agilent 3070 provides tools to do this automatically. These smaller tests will have fewer pins switching simultaneously, reducing ground bounce. This is very effective and can be used after the fact as a technique to salvage a failing or unstable test.

Dual stage fixturing, that provides connections only to a limited set of nodes, will reduce the likelihood of ground bounce problems with large boundary scan interconnect tests. By reducing the number of signals coupling to the test system the ground path current is reduced. This can be very difficult and expensive to implement with vacuum and pneumatic fixtures, but is easily accomplished when using a mechanical press. The minimum set of pins to access would be the power pins and the boundary scan chain pins. Nodes needed for device disable (and any functional test nodes) should also be included in the nodes available in the raised position.

Sidebar on Boundary Scan Tests:

There are several different types of tests that fall under the umbrella of boundary scan. These are briefly described here, along with the level of ground bounce risk for the different test types. Boundary scan tests can only be performed on devices that provide special facilities for these tests. These consist of four (or sometimes five) control and access pins on the device, along with special cells at each digital (for IEEE 1149.1 testing) I/O pin. In recent years these have become much more common as device pin counts have increased and the area required for the I/O pin cells has dropped. (It is now common for the boundary scan register cells to be implemented in the space under the bonding pads, effectively taking no real estate on the device.)

Tap Integrity Test:
The tap integrity test verifies that the boundary scan path from the tester, through the DUT board, and back to the test system is functional. The only device pins tested are the boundary scan access port pins. This test is generally run as the first part of all other tests, and may not be available as a stand-alone test. There is little risk of a tap integrity test failing due to ground bounce because there are few pins transitioning during this test. (When tap integrity tests do exhibit ground bounce problems, it usually occurs when the DUT switches from native mode to boundary scan mode.)

Connect Test:
Connect tests are a form of in-circuit test used in conjunction with the boundary scan chain. These tests are performed on one device (IC) at a time. The other devices are either disabled or set to a “safe” state. It is common to use the by-pass register on devices when they are not the device being tested. Connect tests only test those device pins connected to nodes that have probe access points on them. These tests are performed to verify that there are no opens between the test device I/O pins and the test system access probes. No testing is done for shorts, because they would have been previously found during normal in-circuit, unpowered shorts testing. Only two patterns are applied, all “0” and all “1”. Connect tests, because of the large number of pins transitioning (due to both large devices and the test pattern), are prone to serious ground bounce failures. This can be aggravated if devices “up-stream” of the tested device must be overdriven to test inputs on the tested device.

Interconnect Test:
Interconnect tests are performed on DUT board nets that connect at least two boundary scan pins together. (Actually, they can also be performed on sets as small as one pin, provided the pin has self-monitoring capability). These tests are performed to test for shorts between these nodes, and they are capable of finding opens on some of the device pins (when multiple boundary scan pins are connected to a net, they may not all be tested for opens). The patterns applied include a counter pattern (consisting of several frames), all “1”, all “0”, and an anti-aliasing pattern consisting of the 1’s complement of the lowest order three vectors (or frames) of the counter pattern. This test may be partly redundant with testing performed during the connect test.

Interconnect tests are performed on all devices in a boundary scan chain simultaneously. It is possible for interconnect tests to suffer ground bounce problems because of the large number of pins involved and the patterns applied. (Note that the test system resources are only connected to a small number of pins during this test; however, the system will still provide capacitive coupling to each probed node on the order of a few to a few tens of picofarads because of the test system disconnect capacitance.)

Bus Wire Test:
Bus wire tests are an extension of interconnect tests and they are used to fill out the opens testing that may not have been completed during the interconnect tests. This test is not always a separate test – this test may be automatically run as a part of the interconnect test. Bus wire tests usually involve a sub-set of the interconnect test pin set, and are therefore less likely to suffer from ground bounce problems.

Powered Shorts:
Powered shorts tests are used to locate potential shorts missed during interconnect tests and in-circuit, unpowered shorts testing. These potential shorts will be between boundary scan accessible nets that have no probe access points, and other nets that do have probe access points but no boundary scan access. This testing is generally limited to testing for shorts between proximal pins on a device. While there is some risk of ground bounce problems, these tests are usually less troublesome than connect tests and interconnect tests.

Silicon Nails:
Silicon nails tests are an extension of boundary scan used to test clusters of non-boundary scan parts that interconnect boundary scan parts. These tests are similar in nature to interconnect and bus wire tests.

Summary:

Ground bounce, a transient disturbance between the DUT and the test system grounds, is an increasingly common problem in board tests. It is observed most often during large boundary scan tests, and occasionally during large library tests. By understanding the problem it is possible to significantly reduce the risk of failing tests through the use of preventive measures. Techniques to be used both during board design and during test implementation have been presented. The most successful approach involves a partnership between the board designer and the board test developer. By understanding each other's problems and needs it is possible to develop boards that present little risk of ground bounce failures in production. This co-operation reduces time-to-market and the cost of test.