



ATtiny804/1604

ATtiny804/1604 Silicon Errata and Data Sheet Clarification

The ATtiny804/1604 devices you have received conform functionally to the current device data sheet ([DS40002028](#)), except for the anomalies described in this document. The erratas described in this document will likely be addressed in future revisions of the ATtiny804/1604 devices.

Note:

- This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current.
- Refer to the Device/Revision ID section in the current device data sheet ([DS40002028](#)) for more detailed information on Device Identification and Revision IDs for your specific device, or contact your local Microchip sales office for assistance.

1. Silicon Issue Summary

Legend

- Erratum is not applicable.
- X** Erratum is applicable.
- * This silicon revision was never released to production.

Peripheral	Short Description	Valid for Silicon Revision
		Rev. A
ADC	2.2.1 One Extra Measurement Performed After Disabling ADC Free-Running Mode	X
	2.2.2 Pending Event Stuck When Disabling the ADC	X
	2.2.3 ADC Functionality Cannot be Ensured with CLKADC Above 1.5 MHz and a Setting of 25% Duty Cycle	X
	2.2.4 ADC Performance Degrades with CLKADC Above 1.5 MHz and VDD < 2.7V	X
CCL	2.3.1 Connecting LUTs in Linked Mode Require OUTEN Set to '1'	X
	2.3.2 D-latch is Not Functional	X
RTC	2.4.1 Any Write to the RTC.CTRLA Register Resets the RTC and PIT Prescaler	X
	2.4.2 Disabling the RTC Stops the PIT	X
TCB	2.5.1 Minimum Event Duration Must Exceed the Selected Clock Period	X
	2.5.2 The TCA Restart Command Does Not Force a Restart of TCB	X
USART	2.6.1 TXD Pin Override Not Released When Disabling the Transmitter	X

2. Silicon Errata Issues

2.1 Errata Details

- Erratum is not applicable.
- X** Erratum is applicable.
- * This silicon revision was never released to production.

2.2 ADC - Analog-to-Digital Converter

2.2.1 One Extra Measurement Performed After Disabling ADC Free-Running Mode

The ADC may perform one additional measurement after clearing ADCn.CTRLA.FREERUN.

Work around

Write ADCn.CTRLA.ENABLE to '0' to stop the Free-Running mode immediately.

Affected Silicon Revisions

Rev. A							
X							

2.2.2 Pending Event Stuck When Disabling the ADC

If the ADC is disabled during an event-triggered conversion, the event will not be cleared.

Work around

Clear ADC.EVCTRL.STARTEI and wait for the conversion to complete before disabling the ADC.

Affected Silicon Revisions

Rev. A							
X							

2.2.3 ADC Functionality Cannot be Ensured with CLK_{ADC} Above 1.5 MHz and a Setting of 25% Duty Cycle

The ADC functionality cannot be ensured if CLK_{ADC} > 1.5 MHz with ADCn.CALIB.DUTYCYC set to '1'.

Work around

If ADC is operated with CLK_{ADC} > 1.5 MHz, ADCn.CALIB.DUTYCYC must be set to '0' (50% duty cycle).

Affected Silicon Revisions

Rev. A							
X							

2.2.4 ADC Performance Degrades with CLK_{ADC} Above 1.5 MHz and VDD < 2.7V

The ADC INL performance degrades if CLK_{ADC} > 1.5 MHz and ADCn.CALIB.DUTYCYC set to '0' for VDD < 2.7V.

Work around

None.

Affected Silicon Revisions

Rev. A							
X							

2.3 CCL - Configurable Custom Logic**2.3.1 Connecting LUTs in Linked Mode Require OUTEN Set to '1'**

Connecting the LUTs in linked mode require LUTnCTRLA.OUTEN set to '1' for the LUT providing the input source.

Work around

Use an event channel to link the LUTs or do not use the corresponding I/O pin for other purposes.

Affected Silicon Revisions

Rev. A							
X							

2.3.2 D-latch is Not Functional

The CCL D-latch is not functional.

Work around

None.

Affected Silicon Revisions

Rev. A							
X							

2.4 RTC - Real-Time Counter**2.4.1 Any Write to the RTC.CTRLA Register Resets the RTC and PIT Prescaler**

Any write to the RTC.CTRLA register resets the RTC and PIT prescaler.

Work around

None.

Affected Silicon Revisions

Rev. A							
X							

2.4.2 Disabling the RTC Stops the PIT

Writing RTC.CTRLA.RTCEN to '0' will stop the PIT.

Writing RTC.PITCTRLA.PITEN to '0' will stop the RTC.

Work around

Do not disable the RTC or the PIT if any of the modules are used.

Affected Silicon Revisions

Rev. A							
X							

2.5 TCB - Timer/Counter B

2.5.1 Minimum Event Duration Must Exceed the Selected Clock Period

Event detection will fail if TCBn receives an input event with a high/low period shorter than the period of the selected clock source (CLKSEL in TCBn.CTRLA). This applies to the TCB modes (CNTMODE in TCBn.CTRLB) *Time-Out Check* and *Input Capture Frequency and Pulse-Width Measurement* mode.

Work around

Ensure that the high/low period of input events is equal to or longer than the period of the selected clock source (CLKSEL in TCBn.CTRLA).

Affected Silicon Revisions

Rev. A							
X							

2.5.2 The TCA Restart Command Does Not Force a Restart of TCB

The TCA restart command does not force a restart of the TCB when TCB is running in SYNCUPD mode. TCB is only restarted after a TCA OVF.

Work around

None.

Affected Silicon Revisions

Rev. A							
X							

2.6 USART - Universal Synchronous and Asynchronous Receiver and Transmitter

2.6.1 TXD Pin Override Not Released When Disabling the Transmitter

The USART will not release the TXD pin override if:

- The USART transmitter is disabled by writing the TXEN bit in USART.CTRLB to '0' while the USART receiver is disabled (RXEN in USART.CTRLB is '0')
- Both the USART transmitter and receiver are disabled at the same time by writing the TXEN and RXEN bits in USART.CTRLB to '0'

Work around

There are two possible work arounds:

- Make sure the receiver is enabled (RXEN in USART.CTRLB is '1') while disabling the transmitter (writing TXEN in USART.CTRLB to '0')

- Writing to any register in the USART after disabling the transmitter will start the USART for long enough to release the pin override of the TXD pin

Affected Silicon Revisions

Rev. A							
X							

3. Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet ([DS40002028](#)):

Note: Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

3.1 Electrical Characteristics

3.1.1 ADC

A clarification has been made to the electrical characteristics for the ADC peripheral:

- Added a note for 50% duty cycle

Table 3-1. Clock and Timing Characteristics

Symbol	Description	Conditions	Min.	Typ.	Max.	Unit
f_{ADC}	Sample rate	$1.1\text{V} \leq V_{\text{REF}}$	15	-	115	ksps
		$1.1\text{V} \leq V_{\text{REF}}$ (8-bit resolution)	15	-	150	
		$V_{\text{REF}}=0.55\text{V}$ (10-bit)	7.5	-	20	
CLK_{ADC}	Clock frequency	$V_{\text{REF}}=0.55\text{V}$ (10-bit)	100	-	260	kHz
		$1.1\text{V} \leq V_{\text{REF}}$ (10-bit)	200	-	1500	
		$1.1\text{V} \leq V_{\text{REF}}$ (8-bit resolution)	200	-	2000 ⁽¹⁾	
T_{s}	Sampling time		2	2	33	CLK_{ADC} cycles
T_{CONV}	Conversion time (latency)	Sampling time = 2CLK_{ADC}	8.7	-	50	μs
T_{START}	Start-up time	Internal V_{REF}	-	22	-	μs

Note:

1. **50% duty cycle is required for clock frequencies above 1500 kHz.**

4. Document Revision History

Note: The data sheet clarification document revision is independent of the die revision and the device variant (last letter of the ordering number).

4.1 Revision History

Doc Rev.	Date	Comments
B	10/2019	<ul style="list-style-type: none">Updated document template.The ADC errata, ADC Functionality Cannot be Ensured with ADCCLK Above 1.5 MHz for All Conditions, has been split into two separate erratas and rewritten.Added clarification for ADC electrical characteristics.
A	06/2019	<ul style="list-style-type: none">Initial document release.

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ISBN: 978-1-5224-5151-8

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