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Ph. D. dissertation

*DIGITALLY-ASSISTED ANALOG CIRCUITS FOR HYBRID
PIXEL X-RAY DETECTORS*

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*WSPOMAGANE CYFROWO UKŁADY ANALOGOWE DLA
POTRZEB HYBRYDOWYCH DETEKTORÓW
PIKSELOWYCH PROMIENIOWANIA X*

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ABSTRACT

The dissertation describes the theoretical studies and experimental tests of the multichannel readout circuits for hybrid X-ray detectors, addressing aspects of the design of integrated circuits which contain both analog circuitry as well as digital logic integrated on the same silicon substrate. Combining more and more functionality inside a pixel is a trend observed in nowadays readout integrated circuits. However, integration of several blocks of diverse functionality in each readout channel and implementation of inter-pixel communication impose new challenges in the process of simulation, design, implementation and verification of the integrated mixed-mode systems.

Scientific problems addressed by this dissertation aim at improving design process of mixed-mode readout integrated circuits, in particular, with the algorithms dealing with charge sharing implemented inside a chip. To achieve this goal, the basic concepts of X-ray detector systems and their limitations are studied. Then, the algorithms implemented in mixed-mode integrated circuits for dealing with charge sharing and selected solutions from the literature are discussed. The C8P1 algorithm, developed by the ASIC group from the AGH University of Science and Technology, is a subject of detailed conceptual analyses and simulations as a known solution to the charge sharing problem. The simulation approach to this algorithm and implementation of realistic models, including practical aspects, for example non-ideal comparators, noise or analog parameters spread is presented. The influence of analog parameters spread on the detector registration is analysed. The simulations are conducted in static and dynamic modes.

The target of the experimental part of the thesis is to confirm the conclusions obtained through the simulations. Firstly, the architecture and design aspects of the multichannel readout integrated circuit named Chase Jr. chip with the C8P1 algorithm are presented. The operation and configuration of the chip with an emphasis on analog path reconfiguration for the purpose of testing and trimming is revealed. The dedicated measurement environment implemented for the Chase Jr. tests and the practical realisation of the testing procedures for the Chase Jr. chip are described. The measurement results for the Chase Jr. chip bonded to a silicon sensor are shown. Three types of experiments are conducted: the preliminary integrated circuit tests without X-ray radiation performed for calibration purposes, the experiments using an X-ray tube and the experiments using specialised synchrotron source, used mainly for the assessment of the algorithm dealing with charge sharing in this work. The experiments include the tests of signal reconstruction in the case of charge sharing, the tests of registration at pixel borders, the tests of influence of correction on the C8P1 algorithm and the high count rate tests.

The results of the simulations and measurements lead to the conclusions that the integrated circuit with the C8P1 algorithm switched on allows reconstruction of the total photon energy from fractional signals in the case of charge sharing between two or four pixels, and thus, the photons

can be detected even at pixel borders, where the standard approach fails. This proves that the charge sharing effect occurring in hybrid pixel detectors can be compensated by mixed analog-digital circuits implemented inside the readout electronics using inter-pixel communication strategies. However, increasing pixel-to-pixel gain spread, DC offset spread and noise, result in the significant degradation of the detection efficiency in the C8P1 mode. Therefore, there is a need for dedicated correction circuits to minimise the analog parameters spread between channels and assure the proper operation of the detector. The results of the tests of the Chase Jr. chip prove in practice, that it is possible to overcome technology limitations regarding analog parameters spread of the multichannel integrated circuits for hybrid pixel detectors with inter-pixel communication, using digitally assisted correction blocks.

ABSTRAKT

Niniejsza rozprawa przedstawia rozważania teoretyczne, wyniki symulacji oraz pomiarów wielokanałowych układów odczytowych dla hybrydowych detektorów promieniowania X. Układy takie zawierają zarówno część analogową jak i cyfrową, zintegrowane w jednym układzie scalonym. Widocznym trendem w projektowaniu tych układów jest zwiększanie funkcjonalności pojedynczego kanału, co stawia nowe wyzwania w procesie symulacji, projektowania i testowania zintegrowanych systemów analogowo-cyfrowych.

Podjęte w ramach tej pracy rozważania naukowe mają na celu optymalizację procesu projektowania analogowo-cyfrowych scalonych układów odczytowych, w szczególności zawierających algorytmy do minimalizacji efektów związanych ze zjawiskiem podziału ładunku. We wstępnie wprowadzono podstawowe pojęcia, opisano zjawiska i rozwiązania dedykowane detekcji promieniowania X. Następnie, przedstawiono algorytmy i implementacje układowe podejmujące próby rozwiązania problemu podziału ładunku w detektorach pracujących w trybie pojedynczego zliczania fotonów opisane w literaturze. Przedmiotem szerszych badań koncepcyjnych i symulacyjnych stał się algorytm C8P1, zaproponowany przez grupę projektowania układów scalonych z Katedry Metrologii i Elektroniki, Akademii Górnictwo-Hutniczej. W pracy zaproponowano statyczne i dynamiczne modele układu odczytowego uwzględniające m.in. rozrzuty parametrów analogowych pomiędzy kanałami, wynikające z efektów niedopasowania technologicznego oraz szumy.

W eksperimentalnej części pracy zaprezentowano architekturę, zasadę działania oraz konfigurację układu scalonego Chase Jr. z zaimplementowanym algorytmem C8P1. W celu przeprowadzenia zautomatyzowanych testów samego układu oraz detektora składającego się z układu Chase Jr. zbondowanego do krzemowego czujnika, zaprojektowano oraz zaimplementowano dedykowane środowisko testowe. Przeprowadzono trzy rodzaje eksperymentów: wstępne testy układu scalonego bez promieniowania X w celach kalibracyjnych, testy z użyciem lampy rentgenowskiej oraz testy synchrotronowe. Przedmiotem szerszej analizy były procedury korekcyjne i wpływ korekcji na poprawność detekcji, rekonstrukcja sygnału w detektorze w przypadku podziału ładunku oraz działanie detektora w warunkach promieniowania o dużym natężeniu.

Zarówno wyniki symulacji jak i pomiarów pokazują, że układ scalony z zaimplementowanym algorytmem C8P1 pozwala na odtworzenie pierwotnej energii padającego fotonu w przypadku podziału ładunku pomiędzy dwa lub cztery piksele, zatem foton mogą zostać zarejestrowane nawet na krawędziach pomiędzy pikselami. Oznacza to, że podział ładunku może zostać skompensowany przy wykorzystaniu

układów analogowych wspomaganych cyfrowo wykorzystujących komunikację międzypikselową. Jednakże, zaobserwowano i udowodniono, że znaczący wpływ na jakość detekcji mają szумy elektroniki odczytu oraz rozrzut parametrów analogowych układu, takich jak offset DC na wejściu dyskryminatora czy wzmacnienie. Wskazano na konieczność stosowania dedykowanych układów i procedur korekcyjnych do minimalizacji rozrzutów pomiędzy kanałami, co jest warunkiem poprawnej pracy detektora. Wyniki uzyskane w testach układu Chase Jr. bezpośrednio udowadniają, że możliwe jest pokonanie ograniczeń technologicznych dotyczących rozrzutów parametrów analogowych w hybrydowych pikselowych detektorach promieniowania X, wykorzystując cyfrowe wspomaganie bloków analogowych.

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LIST OF ABBREVIATIONS AND ACRONYMS

ADC –Analog-to-Digital Converter

API – Application Programming Interface

AGH – Akademia Górnictwo-Hutnicza

APS – Advanced Photon Source

ASIC – Application Specific Integrated Circuit

CSA – Charge Sensitive Amplifier

CT – Computed Tomography

DAC – Digital-to-Analog Converter

DISCR - DISCRiminator

ENC – Equivalent Noise Charge

FNAL – Fermi National Accelerator Laboratory

KB mirrors – Kirkpatrick-Baez mirrors

LVDS – Low-Voltage Differential Signalling

NMOS – n-Channel Metal-Oxide-Semiconductor

PMOS – p-Channel Metal-Oxide-Semiconductor

SPC – Single Photon Counting

SH FAST – SHaper FAST

SH SLOW – SHaper SLOW

SNR – Signal-to-Noise Ratio

SRH – Signal Rebuild Hub

THR – THreshold

TDC – Time-to-Digital Conversion

ToT – Time-over-Threshold

PCB – Printed Circuit Board

ROI – Region of Interest

XPCS – X-Ray Photon Correlation Spectroscopy

1 INTRODUCTION

1.1 Work thesis

The dissertation treats on the subject of integrated circuits for reading out pixelated sensors which can handle registration of X-ray photons while charge generated by these photons is shared among several pixels. These integrated circuits contain both analog circuitry and digital logic integrated on the same silicon substrate. The coexistence of analog-digital parts on one chip is a common trend in recent methodologies of the integrated circuit designing, since it responds to technological imperfections in decanometre fabrication processes. It allows compensating for these imperfections; it increases the design flexibility; it offers extensions above traditional modes of control of functional chains and it allows efficient storing of results digitally. However, integration of several blocks of diverse functionalities in each readout channel and implementation of inter-pixel communication impose new challenges in the process of simulation, design, implementation and verification of the integrated mixed-mode systems.

Scientific problems addressed by this dissertation aim at improving the design process of mixed-mode readout integrated circuits, in particular, realizing the algorithms dealing with charge sharing implemented inside a chip. In complex circuits, comprising even several thousands of transistors per channel, new methods of assessment of the algorithms dealing with charge sharing on the simulation level need to be introduced to optimise the simulation time and accuracy. Therefore, possible improvements on the simulation and experimental level are investigated and new directions in the process of an integrated circuits implementation are determined.

This work describes a broader context of studies conducted in Kraków by the ASIC group at the AGH University of Science and Technology, the Department of Measurement and Electronics. The Chase Jr. chip was developed in the design team of the ASIC group. The simulations were performed for a generalized readout channel of an integrated circuit dealing with charge sharing, while the Chase Jr. chip was used for the experiments supporting findings of this work.

The manuscript is divided into 7 chapters. Chapter 1 introduces the basic concepts of X-ray detector systems and their limitations, leading to the formulation of the work theses. Chapter 2 describes the known algorithms implemented in mixed-mode integrated circuits for dealing with charge sharing

and selected solutions that were given in the literature so far. Chapter 3 is dedicated to the simulation approach applied to these algorithms and to the implementation of realistic models, including practical aspects of the circuits, for example, non-ideal comparators, noise or analog parameters spread. Chapter 4 describes the architecture and design guidelines for the multichannel readout Chase Jr. chip. Chapter 5 presents the dedicated measurement environment developed for the tests and the practical realisation of the testing procedures for the Chase Jr. chip. The measurement results from the tests of the Chase Jr. chip bonded to a silicon sensor are presented in Chapter 6. Chapter 7 concludes the work and shows the prospects for the future developments of readout integrated circuits for X-ray hybrid pixel detectors, in particular, with solutions dealing with charge sharing implemented inside a chip.

During the preliminary phase of the research, the following set of theses, which motivated the further research presented in this dissertation, was formulated:

1.1 Thesis 1 (focus on goals):

The charge sharing effect occurring in hybrid pixel detectors may be compensated by mixed analog-digital circuits using inter-pixel communication and digital assistance strategies, and such an approach allows registering photons irrespectively of the interaction position on the detector and avoiding counting extra photons or loosing photons hitting pixel borders.

1.2 Thesis 2 (focus on methods):

Readout integrated circuits for hybrid pixel X-ray detectors with inter-pixel communication implemented for dealing with charge sharing require adequately modified methods of the readout channel parameters estimation, such as gain, DC offsets or noise, with respect to classical solutions working in the single photon counting mode.

1.3 Thesis 3 (focus on simulation solution):

It is possible to build a model of a mixed-mode circuit of a hybrid X-ray detector readout channel with inter-pixel communication using behavioural representations of functional blocks, to improve the process of the design and assessment of the inter-pixel algorithms for dealing with charge sharing, optimising the simulation time and allowing validation of the system behaviour on the higher level of abstraction.

1.4 Thesis 4 (focus on hardware solution):

It is possible to overcome technological limitations regarding analog parameters spread of the multichannel integrated circuits for hybrid pixel detectors with inter-pixel communication by using multistage digitally assisted correction mechanisms, which are achievable for implementations in $100 \mu\text{m} \times 100 \mu\text{m}$ pixel and smaller, and the use of digital blocks is necessary for proper energy measurements and proper hits allocations in the case of algorithms for charge sharing compensation implemented inside a chip.

1.2 X-ray generation

X-rays were discovered in 1895 by Wilhelm Röntgen while experimenting with vacuum tubes, when the fluorescent effect was unexpectedly observed. The effect could only be produced by passing light and the tube was covered with a shield so that no light should escape from the tube. Thus, Röntgen concluded that it might only be explained by the existence of a new kind of rays, which he termed X-rays 'for the sake of brevity'[1]. From the physical point of view, X-ray radiation is electromagnetic radiation with a wavelength within the range from 5 pm to 10 nm. Mentioning just a few most important features of X-rays, they are invisible to the human eye, propagating with the speed of light and unaffected by magnetic and electrical fields. Similarly to visible light, X-rays can be diffracted, reflected, refracted and polarized.

1.2.1 X-ray tube

X-ray radiation can be generated in a laboratory environment in several ways, employing: X-ray tubes, linear accelerators or synchrotron radiation sources. X-ray tubes are most commonly used due to their availability and low cost. In a typical X-ray tube, X-rays are produced when high-speed electrons from a heated cathode decelerate and lose their energy passing through an anode. Radiation is emitted as a consequence of two mechanisms, i.e. bremsstrahlung (braking radiation) and characteristic radiation. Braking radiation is emitted when an electron loses its kinetic energy in the Coulomb field of an atomic nucleus of an anode. The energy of a braking electron is mainly changed into heat (99%) and the rest goes into X-rays (1%). The radiation intensity is proportional to the atomic number of the anode material and the radiation has a continuous energy spectrum.

Characteristic radiation can be produced by interaction of an incident electron with a K-shell electron. The energy of the incident electron has to be higher than the binding energy of the inner shell electron. In this case, an electron in the K-shell is ejected and the created vacancy is filled by electrons from the upper L or M shell. In this process, X-rays are emitted. Their energy is equivalent to the difference between binding energy levels of the outer and inner shell electrons. Thus, the emitted radiation has discrete energy values, and the energy depends on the anode material and its atomic number – Z, for example photon energies are equal to 5.4 keV, 8.0 keV and 17.4 keV for anodes made of Cr, Cu and Mo, respectively.

Therefore, a radiation spectrum of an X-ray tube contains both, the characteristic X-rays peaks produced at particular photon energies, as well as the bremsstrahlung spectrum, characterised by a continuous distribution [2]. An example of an X-ray tube spectrum is presented in Fig. 1.1. The endpoint

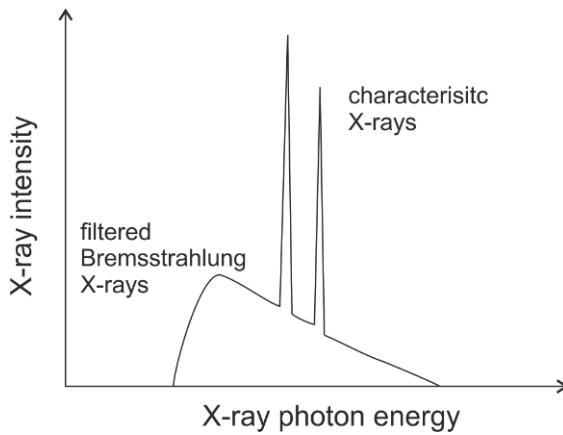


Fig. 1.1 A typical X-ray spectrum for an X-ray tube.

photon energy corresponds to the energy of the incident electron, thus, it is determined by the voltage applied to the X-ray tube.

The main problem concerning generating X-rays with a tube is the inefficiency of the process, resulting in conversion of most of the kinetic energy of electrons into heat. Therefore, cooling needs to be used to prevent the anode from melting and heat dissipation requires special attention in equipment design and manufacturing. Moreover, the photons are radiated in different directions and the beam is not collimated [3]. Last, but not least, the beam is never monochromatic, so monochromators need to be used to extract only a selected energy of photons. Taking the aforementioned features into account, the final photon beam has low intensity, and only a part of the generated X-rays can be finally absorbed by the detector. The main advantage of a synchrotron radiation source over an X-ray tube is the capability of generating high-flux and coherent beams.

1.2.2 Synchrotron radiation source

A general diagram of a synchrotron (from the resources of the APS – the Advanced Photon Source, at Argonne National Laboratory [4], where the experiments described in Chapter 6 were carried out) is presented in Fig. 1.2. Synchrotron radiation is produced when high-speed electrons circulate in a magnetic field of a storage ring. The magnetic field is controlled with bending magnets. Special insertion devices, called wigglers and undulators, are placed in straight sections of a storage ring. When passing through an alternating magnetic field of an insertion device, the particles experience oscillations, which stimulates the emission of synchrotron radiation. A wiggler is an insertion device with a longer period and a higher field. As a consequence, radiation produced in consecutive periods exhibits a lack of phase

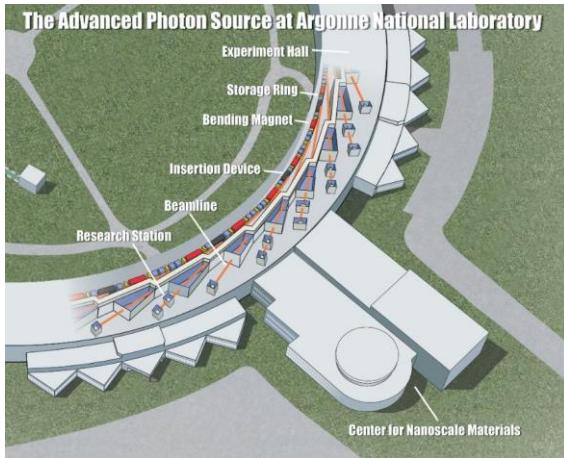


Fig. 1.2 A cutaway of the APS experiment hall, with storage ring components, insertion devices, beamlines, first-optics enclosures, research stations, a typical lab/office module (figure from [7]).

coherence and larger angular excursion [5]. An undulator is a multi-period wiggler which concentrates the radiation into a narrow cone [5]. The radiation spectrum is not continuous but nearly monochromatic, as it comprises a narrow spectral line at a well-defined frequency and its higher odd harmonics [6].

The emitted light is transported to the beamlines, where the photon beam can be optically tuned for a particular application using mirrors and focusing devices [16]. The synchrotron light has a continuous spectrum from infrared to soft and hard X-rays [15], however, most commonly, the beam is restricted to a narrow energy band using monochromators. Finally, the tuned beam reaches a research station hutch with the instrumentation dedicated to a particular measurement.

According to [7], there are more than 50 synchrotron light sources in operation in the world serving the scientific and industrial research in the fields of materials science, physics, biological science, innovative X-ray instrumentation, chemistry, environmental and geophysical science [4]. Over the years, a steady increase in the brightness of synchrotron radiation sources has been observed, reaching a factor of 10^{20} - 10^{21} photons/s/ 0.1% bw/mm 2 /mrad 2 in the 3rd generation synchrotrons like the European Synchrotron Radiation Facility, Grenoble, France; Spring8, Harima, Japan or the Advanced Photon Source at Argonne National Laboratory, and striving towards 10^{22} photons/s/ 0.1% bw/mm 2 /mrad 2 in the 4th generation synchrotrons. The tendency in the next generation sources is to boost brightness and produce radiation with a coherent flux, approaching the diffraction limit. The higher brightness is needed for imaging with a nanometre resolution to allow mapping atoms positions in a wide field of view. Coherence will enable

Table 1.1 The APS at Argonne National Laboratory [6] radiation characteristics.

Parameter	Value	Unit
Storage ring beam energy	7	GeV
Beam current [mA]	100	mA
Number of bunches	24-324	
Available energy range	0.25-170	keV
Horizontal Beam Size (rms)	274	μm
Horizontal Divergence (rms)	11.3	μrad
Vertical Beam Size (rms)	10.8	μm
Vertical Divergence (rms)	3.7	μrad
Brilliance at 20 keV	0.6	photons/s/0.1%bw/mm ² /mrad ²

high spatial resolution, even if the material is non-periodic, thus it will allow visualization of defects or disorders of an atom scale and measuring the atomic-scale dynamic processes in a sample with a nanosecond resolution. The synchrotron beam parameters of the APS at Argonne National Laboratory are given in Table 1.1.

1.2.3 X-ray sources in tests of 2D position sensitive devices

From the viewpoint of testing and calibration of a 2D position sensitive device, testing environment plays an important role. Two, different in requirements, types of experiments can be distinguished, namely flat field illumination and pencil beam tests. The concept of a flat field illumination experiment is presented schematically in Fig. 1.3a. In this experiment, the whole area of a detecting device must be illuminated and the most important aspect is maintaining uniformity in X-rays intensity on the large detection area. Clearly, the higher the intensity, the better, since it reduces tests duration. Bearing these requirements in mind, high-power X-ray tubes are used for flat field illumination tests. It is due to the fact that beam sizes achieved from a synchrotron, as presented in Table 1.1, are on the order of 0.1 mm, while dimensions of detectors can reach 25 mm x 30 mm [8].

In the case of pencil beam tests, only a small spot on a detector is illuminated. To achieve a small-diameter X-ray beam, focusing optics can be used. The Kirkpatrick-Baez mirrors (KB mirrors) are typically

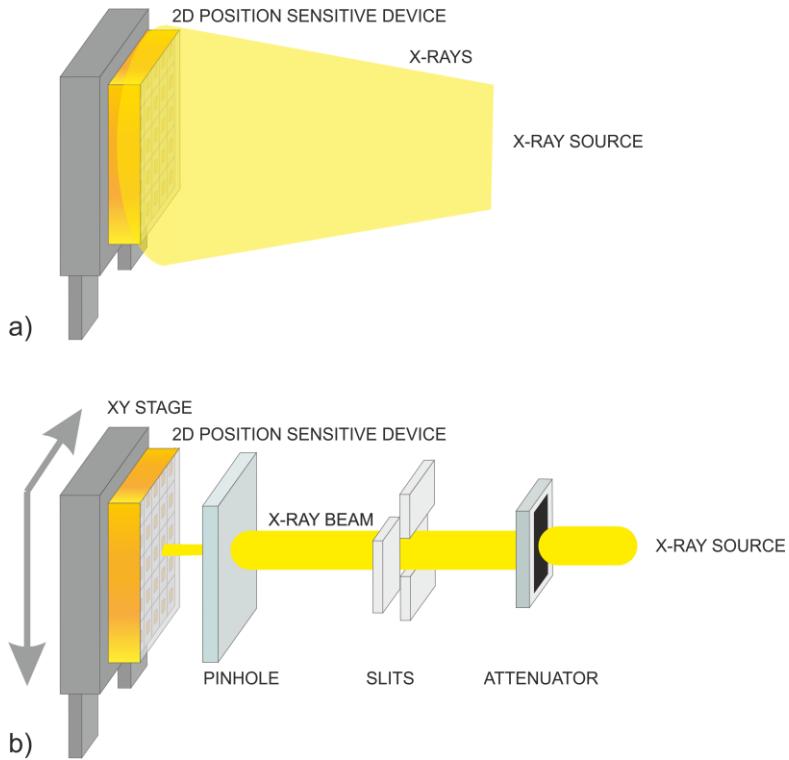


Fig. 1.3 a) A concept of a flat field illumination test. b) A concept of a pencil beam test.

used instrumentation pieces containing two glancing-angle mirrors, which enable focusing a beam in alternate planes with the minimal loss of intensity. The short focal length optics allows achieving nanoscale beams of a sub-100 nm level focusing on 64 m long beamlines at third generation synchrotron sources [9]. The perfectly smooth (surface roughness less than a few angstroms) and parabolic shaped (with an error below a few tenths of microradians) mirrors allow focusing a collimated X-ray beam to a 100 nm diameter spot without significant scattering [9]. However, the instrumentation is very prone to temperature fluctuations, which, as well as stray molecules in imperfect vacuum, deflect the focal point [10]. Therefore, adjusting the KB instrumentation and the detector position, can be inconvenient in the case of testing position sensitive devices. Another aspect which becomes important, especially for thicker detectors, is that the beam is focused at a constant distance, which may lead to the parallax effect.

An alternative solution, presented in Fig. 1.3b uses a simple pinhole of a diameter equal to the desired beam diameter. A pinhole is placed in front of a detecting device, perpendicularly to the beam. In this case, the positioning of the pinhole and the detector is not complicated, and the environmental conditions, like temperature, do not influence the parameters of an X-ray beam after crossing a pinhole. However, it should be noted that an additional effect of X-ray scattering on the pinhole walls is unavoidable

in this solution. To reduce the area of registration of scattered photons, the pinhole must be positioned as close to the detector as possible.

For pencil beam tests, a synchrotron facility is used, rather than an X-ray tube. In order to justify this choice, two experimental set-ups for the pencil beam tests are considered. The first one is a synchrotron facility and the other one is an X-ray tube. In pencil beam tests, described in the following chapters, performed at the APS, a flux of 20 kphotons/s after a 3.5 μm -diameter-pinhole was measured. The tests of the detector using flat field illumination with an X-ray tube were also performed, and the maximum photon fluxes between 100 kphotons/s and 1Mphotons/s per a 100 $\mu\text{m} \times 100 \mu\text{m}$ pixel were measured. This means, that the maximum flux that can be registered with the X-ray tube, if the 3.5 μm -diameter pinhole was placed in front of the device, would be at most 1 kphotons/s. Typically, a monochromator is used both for an X-ray tube and a synchrotron to transmit only a narrow energy band radiation and to avoid ambiguity in interpretations of registered spectra, which are influenced simultaneously by the effect of charge sharing and multienergy photon beam. Nevertheless, the flux is significantly decreased, in the case of an X-ray tube. Therefore, if these two experimental environments were compared, regarding the pencil beam tests of a hybrid pixel detector, the same experiment would last at least 20 times longer with a tube, making an application of an X-ray tube for this experiment impractical.

The tests for extracting detector parameters, estimating the maximum photon count rate, as well as investigating effects, occurring when photons interact with a sensor in particular detector areas, such as on the edges between readout channels, require registration of high photon statistics by a detector. Therefore, intensity is the key feature of an X-ray beam in the experiments described in this thesis, aiming at testing a 2D position sensitive X-ray detector. This aspect provided motivation for the synchrotron studies of the detector described in the following sections.

1.3 X-ray interaction with matter

1.3.1 Dominant mechanisms of interaction of X-ray photons with atoms

When an X-ray photon traverses through matter, it may interact with atoms in several possible processes, which, depending on the X-ray energy range, mainly include photoelectric effect, coherent scattering, incoherent scattering and electron–positron pair production.

In the photoelectric absorption, depicted in Fig. 1.4a, an incident photon is absorbed and an atomic electron is liberated. The energy E of the incident photon is given by Eq. 1.1, as the Planck–Einstein relation.

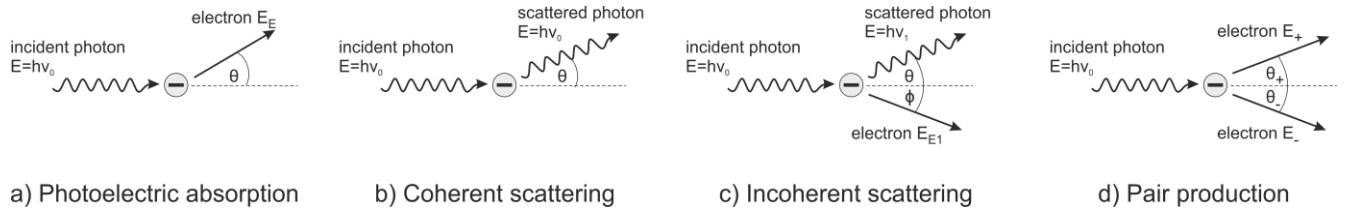


Fig. 1.4 The mechanisms of an X-ray photon interaction with matter.

$$E = h\nu_0$$

Eq. 1.1

where h is the Planck's constant ($6.626 \cdot 10^{-34}$ Js), ν_0 is the initial frequency of the electromagnetic radiation.

The resulting kinetic energy E_E of the electron is equal to the energy E decreased by the electron binding energy E_{BINDING} according to Eq. 1.2:

$$h\nu_0 = E_E + E_{\text{BINDING}}$$

Eq. 1.2

Consequently, the absorption occurs only if the photon energy is higher than the binding energy. The liberated electron leaves a vacancy, so the excited atom needs to return to the basic state in one of the two competitive processes: fluorescent photon emission or emission of an electron from the same atom, called Auger effect. However, for typical X-ray detector materials, the fluorescence quantum yield is low enough (for example 3.6% for the K shell in silicon [11]) to neglect this effect, and the Auger electron emission is dominant, which is important regarding detector design. The emitted Auger electron ionizes the material producing electron-hole pairs in the case of semiconductor.

In scattering processes, a secondary photon is emitted. The direction of this new photon is changed from the trajectory of the incident photon. In the case of Rayleigh elastic scattering, also called the coherent scattering, the incident photon is absorbed by the target atom and another scattered photon is emitted, without excitation of the target atom, as presented in Fig. 1.4b. Thus, the energy of both incident and scattered photons remains the same [12].

Inelastic Compton scattering, also called the incoherent scattering, is presented in Fig. 1.4c. In this instance, an incident photon is absorbed and a scattered photon of lower energy is emitted with a direction altered by an angle θ . A part of the incident photon energy is transferred to the electron ejected from an outer shell at an angle ϕ , which is given by the equation Eq. 1.3.

$$h\nu_0 = E_{E1} + h\nu_1$$

Eq. 1.3

where $h\nu_0$ is the energy of the incident photon, E_{E1} is the kinetic energy of the electron, $h\nu_1$ is the energy of the secondary photon. From the relativistic theory and the law of conservation of momentum, the energies of the secondary photon (Eq. 1.4) and the electron (Eq. 1.5) can be derived [11]:

$$h\nu_1 = \frac{h\nu_0}{1+\alpha(1-\cos\theta)} \quad \text{Eq. 1.4}$$

$$E_{E1} = \frac{h\nu_0 \cdot 2\alpha \cos^2 \phi}{(1+\alpha)^2 - (\alpha^2 \cos^2 \phi)} \quad \text{Eq. 1.5}$$

where $\alpha = \frac{h\nu_1}{mc^2}$, θ is the photon scattering angle, and ϕ is the electron ejection angle. Both, the secondary photon and the electron may cause further ionization in the material.

If the energy of an X-ray photon exceeds 1.02 MeV, an electron – positron pair can be created, which is shown in Fig. 1.4d. An incident photon releases the energy to create a pair, while the rest of the energy is changed into the kinetic energy of the positron and the electron.

Each interaction mechanism can be characterised by the cross-section parameter, which determines the probability of the energy transfer from the incident photon for each process. This parameter, expressed in cm^2/g , is highly dependent on the material atomic number Z and photon energy. The cross-sections for silicon (Si) and cadmium telluride (CdTe), typically used as sensor materials, for the following processes: the coherent scattering, the incoherent scattering, the photoelectric absorption, and the pair production in the field of the atomic nucleus according to [13] are presented in Fig. 1.5. The total cross-section is defined by the sum of the partial cross-sections of the four different described interactions.

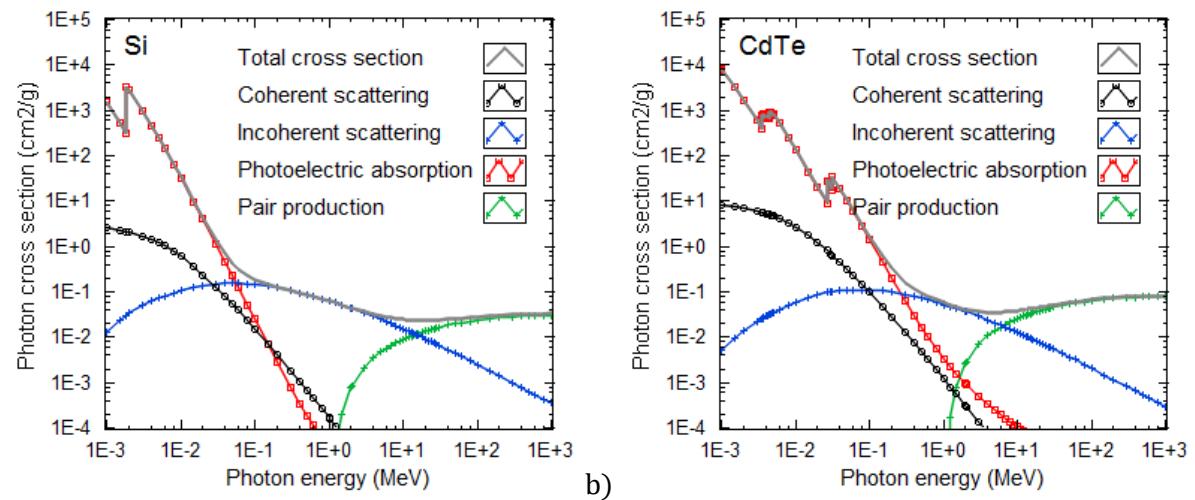


Fig. 1.5 The photon cross-section a) for Si and b) for CdTe.

It can be observed that photoelectric absorption is the dominant process for the lower energies in both materials. For silicon, for the photon energies between 100 keV and 10 MeV, the incoherent scattering contributes to most of the attenuation, whereas for the high energy photons above 10 MeV, pair production plays the dominant role. For cadmium telluride, the cross-section characteristics are shifted towards higher energies, so the photoelectric absorption is dominant up to the photon energy of 250 keV.

Therefore, for example 300 μm thick silicon is used for photon detection up to energies of about 30 keV. Since photoelectric absorption is the ideal process for the detector operation, and the cross-section for photoelectric absorption for a material of atomic number Z is proportional to Z^n , where $4 < n < 5.2$ [14], other semiconductor compound materials with higher Z, like CdTe or CdZnTe (CZT) are used for detection of photons of higher energies of 40-200 keV.

1.3.2 Electron - hole pairs generation in semiconductor sensor materials

As a consequence of all the aforementioned processes, a certain number of electron – hole pairs is generated in an interaction of a photon with a given material. Since for the lower energies (for example less than 100 keV for Si and less than 250 keV for CdTe), photoelectric absorption is the dominant process, in which electron-hole pairs are generated, it can be assumed that a number of generated electron-hole pairs is proportional to the photon energy. This relation is used as a basis of the X-ray photon detection concept in X-ray photon counting detectors. An average number N of electron - hole pairs, generated by a single photon of the energy E is given by Eq. 1.6:

$$N = \frac{E}{E_{EH}} \quad \text{Eq. 1.6}$$

where E_{EH} is the energy required to create an electron - hole pair. For instance, $E_{EH} = 3.6 \text{ eV}$ in Si, $E_{EH} = 4.4 \text{ eV}$ in CdTe or $E_{EH} = 4.6 \text{ eV}$ in CZT [15]. Thus, for example, an X-ray photon of 8 keV generates about 2179 electron-hole pairs when an interaction takes place in Si. The energy E_{EH} is larger than the band gap (for example in silicon it is three times larger), and the difference between the two energies is dissipated as thermal energy, since, during the excitation, the momentum is changed into lattice vibration [16]. However, the number of resulting electron-hole pairs is also subject to fluctuations, with the variance σ_N^2 given by the Fano relation (Eq. 1.7) according to [17]:

$$\sigma_N^2 = FN \quad \text{Eq. 1.7}$$

where F is the Fano factor. For Si and most other semiconductors, the value F is on the order of 0.1 [12].

1.3.3 Beam attenuation and filtration

When an X-ray beam traverses through matter, the photons are subject to absorption and scattering. Therefore, a monochromatic beam does not change its energy but the flux of photons is attenuated. The absorption law is given by Eq. 1.8.

$$I(x) = I_0 \exp(-\mu x) \quad \text{Eq. 1.8}$$

where I is the beam intensity after passing through a material of the thickness x , I_0 is the intensity of an incident beam, and μ is the linear attenuation coefficient. Absorption and scattering contribute to the total attenuation of a beam, thus the linear attenuation coefficient can be described by the sum of μ_{abs} - the linear absorption coefficient and μ_{scatt} – the linear scattering coefficient as in Eq. 1.9 [16].

$$\mu = \mu_{\text{abs}} + \mu_{\text{scatt}} \quad \text{Eq. 1.9}$$

Both μ_{abs} and μ_{scatt} are the properties of an absorber material, dependent on its density, the atomic number Z , and the photon energy. To express the attenuation coefficient independently of the material density, the mass attenuation coefficient, described by Eq. 1.10, expressed in cm^2/g , is commonly used.

$$\mu_m = \sigma \frac{N_A}{A} \quad \text{Eq. 1.10}$$

where σ is the total cross-section, N_A is the Avogadro's constant, A is the atomic mass. Thus, as already described for the photon cross-section (see Fig. 1.4), the absorption contributes to the most of the attenuation, in the lower photon energy range, whereas Compton scattering becomes significant in the higher photon energy range.

Different properties of materials in terms of absorption coefficients are useful for filtration for example in X-ray medical imaging. A typical X-ray tube spectrum, as presented in Fig. 1.1, consists of a large peak of 'soft' lower-energy X-rays which are not valuable for imaging, however, they are absorbed by patient's tissues. These photons can be removed from the beam before passing through a patient by using a low-Z metal filter (for example aluminium) that attenuates majority of the photons of energies below 15 keV, which significantly reduces the patient dose [15].

1.4 X-ray imaging in applications

X-ray imaging is a technique used to register properties of the electromagnetic radiation, such as: intensity, energy, timing properties, polarization, etc., typically visualized using a projection on a 2D plane. The first imaging techniques were developed very early. Just one year after Röntgen's discovery, the X-ray department was set up at the Glasgow Royal Infirmary, the first medical diagnosis using X-rays was made, the inner structures of animals and mummies were investigated, the mechanics of the frog limb

was recorded and manufacturers started producing and selling first X-ray equipment [3]. Since then, X-rays have been widely spread in medical applications, diagnostic techniques (like radiography, computed tomography) and radiotherapy. Another vast field of application is material science and life science, employing the techniques including: X-ray spectrometry, X-ray diffraction and X-ray scattering. X-ray radiation finds its application also in such areas as luggage scanning, criminology or drug development. In the following sections selected techniques are described.

1.4.1 X-ray radiography

Since X-rays are absorbed differently while passing through materials or tissues of a different structure, density or thickness, they are widely used in medical diagnostics. Nevertheless, it is well known that the irradiation of the tissues results in biological reactions, such as damaging living cells or genetic mutations [2]. Transmission radiography, the most popular technique, is based on the measurement of attenuation of the radiation passing through an object (for example luggage) or a tissue. Many forms of transmission radiography have been developed, such as Computed Tomography (CT), where the large number of 2D X-ray images is taken at different angles in order to reconstruct computationally a 3D image, or microscopy, where an X-ray beam is focused to a point on a sample, and the sample is scanned across it [18]. Typical photon energy values for medical diagnostic applications, including dental imaging, mammography or chest imaging, are from the range of 20 keV to 140 keV, depending on the organ under examination. Thus, X-ray tubes with rhodium, molybdenum or tungsten targets are used [19]. For baggage screening, higher energy photons are required, even up to 9 MeV, and either a tungsten-target tube or linear accelerators can be used [19].

1.4.2 X-ray spectroscopy

Another technique, gaining increasing attention, is X-ray spectroscopy which is popularly called ‘colour X-ray imaging’. Just like in transmission radiography, the attenuation of the beam is measured by a detector. However, the additional information about the energy of photons is obtained. To apply that method, several images need to be measured at different energy thresholds, however, it would be required to obtain multi-energy information by classifying the photons as they arrive, within a single exposure. This is crucial, especially in medical applications to reduce artifacts for example coming from breathing, as well as to reduce patient dose. The information carried by different wavelength X-rays can be used to distinguish materials, on the basis of the fact that X-ray attenuation is material and energy dependent. This opens new possibilities in identifying tissue types, presence of illegal substances in a luggage or strain distributions in industrial components [20]. Spectroscopic imaging is also used in selective medical imaging

to discriminate between a high Z contrast agent (often composed of gadolinium or iodine) and body tissues (built from materials with $Z < 20$), used in such diagnostic methods as differential angiography. Other techniques profiting from spectroscopy are K-edge imaging [21] or photon weighting [22].

1.4.3 X-ray diffraction and scattering

X-ray diffraction and scattering experiments, including X-ray diffraction and small- and wide-angle scattering, rely on the measurement of intensity patterns of X-rays which passed through a sample as a function of a photon energy, scattering angle and polarization. In diffraction experiments, a crystal lattice diffracts an X-ray beam according to the Bragg's law. The measured positions and intensities of diffracted X-rays are related to the crystal lattice arrangement by the inverse Fourier transform. Therefore, X-ray diffraction is the basic method of crystallography, in which the 3D structure of molecules at near atomic resolution is determined. If additionally, an X-ray beam is highly coherent, which can be achieved with 4th generation synchrotrons, non-crystalline samples can be also analysed.

Diffraction and scattering experiments are similar in principles. The difference between them arises from performing measurements of crystals (in diffraction) or of non-crystalline molecules (in scattering). In scattering experiments, photons interact with electrons of different atoms. Some of the photons from the initial beam are scattered, while the rest do not interact. The registered scattered pattern, when separated from the unscattered beam, is used to calculate the molecules arrangement.

Both techniques are widely used in structural biology, which reveals for example, new aspects of DNA and RNA, hormones, which regulate physiological and behavioral activities of the body, or enzymes, which catalyse the reactions in the cells. Therefore, these techniques play an important role in pharmaceutical industry, medicine or biotechnology [18]. For scattering and diffraction experiments, generally, a monochromatic beam of high intensity is required, thus synchrotrons and free electron lasers are widely used, and several laboratory small angle and diffractometer devices are also available on the market.

1.4.4 Time-resolved X-ray experiments

Time-resolved X-ray experiments aim at investigation of both, the structural and dynamic properties of a given sample. The experiments often involve X-ray diffraction, scattering and spectroscopic techniques, while the time range of the experiments varies from femtoseconds to hours. For instance, enzymatic experiments focus on the steps lasting from femto- to nanoseconds, whereas, processes of ligand binding and signal transduction are observed on the millisecond scale [23]. The time resolution of the measurement is strictly related to the time of diffraction exposures, being limited by the pulse length

of an X-ray source. The source needs to deliver an adequate amount of photons to a detector in order to obtain a signal with good signal-to-noise ratio [24]. Thus, a specialised X-ray source of high brilliance and, preferably, high coherence is needed for time-resolved X-ray experiments. Laser plasma sources, third generation synchrotron sources and free electron lasers can provide X-ray photons in pulses of the picoseconds duration and the resulting photon flux is sufficient to perform time-resolved experiments [23]. Time-resolved experiments allow following evolutions of chemical, physical and biological processes on the atomic scale, for example giving an insight into the translation process in ribosome or photosynthesis.

All of the aforementioned techniques require, often application specific, X-ray position sensitive detectors. The requirements for medical detectors are: reducing patient dose, enhancing image contrast and resolution, while maintaining low intensity. In contrast to medical applications, duration of the experiment is a crucial aspect, while the radiation dose is not a considerable limit in material science. Therefore, detectors are designed to operate in high-flux conditions, and the readout channel sizes are reduced to obtain better resolution and additionally, to increase the operational speed of the detector. The types, principles of operation and limitations of detector devices are the subject of the next chapters.

1.5 Operation of hybrid semiconductor position sensitive detector for X-ray-imaging

A position sensitive detector is a device that measures localisation of an incoming particle, which could, in particular, be an X-ray photon. Typically, it is built from 1D or 2D arrays of sensor segments and readout electronics. In general, X-ray detection systems can be divided into two groups; indirect and direct detectors. In indirect detectors, detection is a two-step process. A scintillator converts X-ray radiation into visible light, which is then detected by means of a photodiode or a photomultiplier tube. A direct detector is a more efficient solution, since X-ray photons are absorbed and directly converted into electron-hole pairs. Typically, a bias voltage is applied to drift and ultimately collect charge carriers, for processing by the readout electronics. A sensor is a system of reverse biased diodes and a high-resistivity pure layer is used to provide detection with low leakage current. Diodes can be designed in varied geometries, and, according to the diode shapes, detectors can be divided into strip or pixel devices. Although, the principle of operation is common for both solutions, pixel detectors deliver spatial resolution in two dimensions in comparison to single sided strip detectors. Additionally, multiple photon detections at the same time are possible in pixel detectors, since, unlike in double sided strip detectors, all of the channels operate independently.

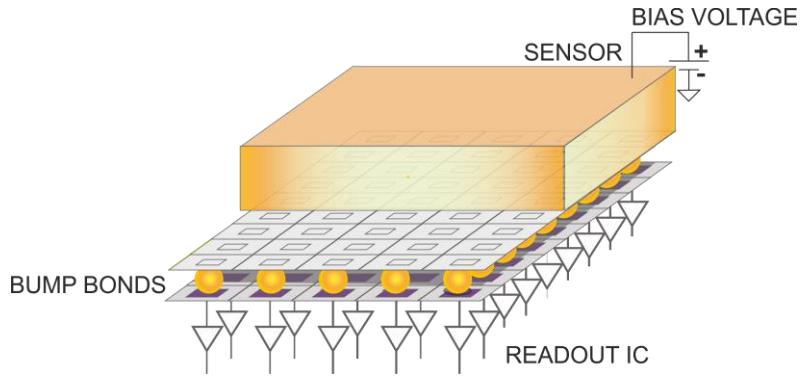


Fig. 1.6 A semiconductor hybrid pixel detector.

Detectors can be further classified as integrating or single photon counting systems. The most common solution nowadays for medical and non-destructive material science applications is a detector working in an integrating mode [25]. In this mode, signals induced by the incoming photons are integrated over a given time exposure, amplified and digitized, and used to estimate the photon flux [26]. This method was initially proposed to cope with high intensities, however, it typically possesses a limited dynamic range and yields a low signal-to-noise ratio due to integration of the noise. In recent years, single photon counting (SPC) devices have been a subject of an intensive research. High count rates can be achieved due to the channel size minimisation and the optimisation of readout electronics. Moreover, this solution allows noise reduction, enhanced spatial resolution and high dynamic range. In an SPC device, each photon is processed individually and generally both the interaction position and photon energy can be measured. A hybrid pixel detector, working in the SPC mode, consists of a segmented sensor connected to an array of electronic readout channels, which is presented in Fig. 1.6. A sensor and an Application Specific Integrated Circuit (ASIC) for readout are electrically and mechanically connected, using bump-bonding. This thesis focuses on single photon counting hybrid pixel detectors, thus this type of devices is described in more details.

1.5.1 Charge transport in sensor - drift and diffusion

When an X-ray photon interacts with a sensor, it deposits energy in a semiconductor material. The electron-hole pairs are created in the mechanism described in section 1.3.1. The generated charge carriers drift in the opposite directions towards the electrodes due to a bias voltage applied. The carriers velocity is expressed by Eq. 1.11 and Eq. 1.12

$$v_H = \mu_H E \quad \text{Eq. 1.11}$$

$$v_E = -\mu_E E \quad \text{Eq. 1.12}$$

where v_H and v_E are the drift velocities, μ_H and μ_E are the mobilities of holes and electrons, respectively, E is the electric field. The time needed for the charge carriers to reach electrodes is called collection time. It depends on the interaction depth, detector thickness and applied voltage bias. While charge clouds drift to the electrodes, they increase their sizes due to diffusion. The diffusion current has the opposite direction to the concentration gradient. By solving a diffusion equation [27] and using Einstein's relation for calculating the diffusion coefficient D [28], the effective σ_{cloud} – the width (rms) of the charge cloud distribution can be calculated [29], which is given by Eq. 1.13.

$$\sigma_{\text{cloud}} = \sqrt{\frac{2kT d^2}{qV}} = \sqrt{2Dt} \quad \text{Eq. 1.13}$$

where $k = 1.38 \cdot 10^{-23} \text{ J} \cdot \text{K}^{-1}$ is the Boltzmann constant, T is the absolute temperature, d is the drift distance, q is the unit charge, V is the bias voltage, t is the collection time.

1.5.2 Charge sharing effect

A charge cloud spread may result in the charge collection by more than one electrode, and this phenomenon is called charge sharing. This effect is presented conceptually in Fig. 1.7. When a photon A interacts with a sensor, the whole charge cloud is collected by one electrode and the signal is processed by one readout channel. In the case of another photon B, the interaction occurs in the corner between four channels. The charge carriers are collected by the neighbouring electrodes and the signal is processed by four readout channels. In this situation, if no circuit dealing with charge sharing problem is implemented, a detector may register four simultaneous events related to the photons of lower energies instead of one. Therefore, charge sharing may significantly impair the energy resolution, as well as it may result in missing some of the interaction events or counting extra events, affecting consequently the statistical features of the measurements, for example, statistical distributions of the measured photon fluxes.

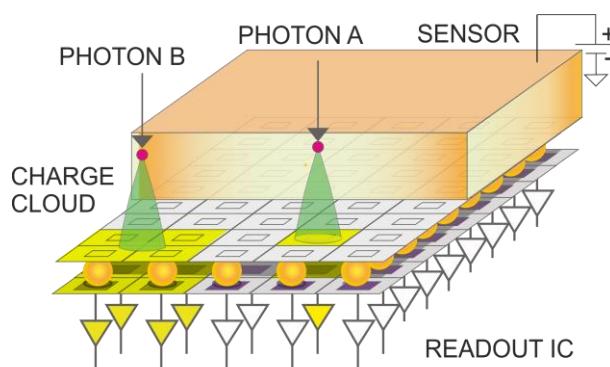


Fig. 1.7 The operation of a semiconductor hybrid pixel detector in case of charge sharing.

An impact of the charge sharing effect enlarges with shrinking of the channel sizes and with an increase of the collection time, according to Eq. 1.13. The collection time can be reduced by applying a high bias voltage and reducing the detector thickness. However, the latter is at the cost of the detection efficiency. The small channel size is a desired feature of novel hybrid X-ray detectors, as it allows better spatial resolution and helps overcoming the processing speed related issues by accepting more photons per the unit area. Thus, the charge sharing effect becomes more significant in novel detectors and must be dealt with by a readout integrated circuit or in off-chip processing.

To illustrate the impact of the charge sharing effect on a sample detector, simulations of the charge cloud spread due to diffusion were performed for a pixelated Si sensor of the thickness $d=300 \mu\text{m}$, and for the bias voltage applied $V=100 \text{ V}$. The Gaussian charge cloud model, given by the equation 1.14 [30] was assumed:

$$f(x, y) = A \exp \left(- \left(\frac{(x-x_0)^2}{2\sigma^2} + \frac{(y-y_0)^2}{2\sigma^2} \right) \right) \quad \text{Eq. 1.14}$$

where, f is the function of charge distribution, A is the photon energy dependent amplitude coefficient, x_0, y_0 are the positions representing the pixel edge, σ is the standard deviation assuming the symmetrical shape of a charge cloud. The percentage of photon interaction events affected by the charge sharing effect as a function of a detector channel size is presented in Fig. 1.8. An event is defined as not affected by the charge sharing effect if at least 99.7% of the charge carriers are collected by one electrode. The plot shows that charge sharing has a significant impact even on detectors with large pixel pitches, affecting more than 35% of the pixel area for pixels with the dimensions $200 \mu\text{m} \times 200 \mu\text{m}$. Scaling down a detector pitch, results in acquiring a size comparable to pixel dimensions by a charge cloud, hence, finally, all of the events are affected by charge sharing.

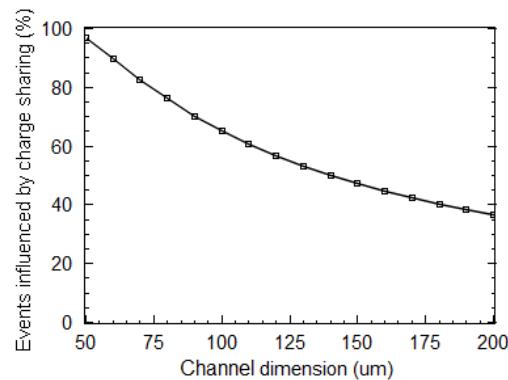


Fig. 1.8 The percentage of events affected by the charge sharing effect as a function of the detector channel size for a silicon sensor of the thickness $d=300 \mu\text{m}$, and for the bias voltage applied $V=100 \text{ V}$.

1.5.3 Other effects degrading performance of photon counting detectors

Except of charge sharing, there are other physical factors that lead to performance degradation of photon counting detectors. They are K-escape, Compton scattering and charge trapping [31]. K-escape is the effect of a discrete energy loss caused by the emission of a secondary fluorescent photon in the photoelectric absorption process. Such a photon may be absorbed by the same pixel as a primary photon or ‘escape’ from the pixel. In the latter case, it is either registered by an adjacent electrode as a photon of an energy reduced by the K-shell energy or is not registered by a detector at all.

Although, Compton scattering is not the dominant interaction mechanism, it can also influence the detector performance. If a photon loses its energy, it deposits the energy at the interaction site. Thus, partial signals may be observed in adjacent channels. Contrary to K-escape X-rays, the energy loss in Compton scattering depends on the scattering angle, therefore, scattered X-rays have a continuous spectrum.

Another effect which needs to be mentioned is charge trapping in a semiconductor material. Defects or impurities in the sensor volume can trap the charges while drifting to the electrodes, which results in reduction of the signal induced and the delayed collection of the trapped carriers. The impact of this effect can be diminished by reducing a sensor thickness, increasing a bias voltage or choosing a sensor material with higher carrier mobilities.

In conclusion, all of the abovementioned factors may lead to degradations in both: the number of the recorded events and the quality of the measured energy or timing spectra. The resolution of a detector is influenced by the multiple factors, including the spreading of charge cloud, secondary photons and electrons emission, efficiency in generation of electron-hole pairs [26]. Thus, the detector performance is strongly dependent on the sensor material parameters in each application.

1.5.4 Common sensor materials

Typical sensor materials include Si, GaAs, CdTe and CdZnTe (CZT). Selected properties of the most popular sensor materials are collected in Table 1.2 according to [11], [32], [15]. Silicon can be grown as a highly homogenous and pure substrate, resulting in the long charge carrier lifetime about 100 μ s, the industrial fabrication of silicon is relatively cheap and has matured over the years. Taking these facts into consideration, silicon has been most commonly used as a sensor material. In this thesis, a silicon sensor bump-bonded to a readout integrated circuit was used. However, when specific requirements, for example for medical imaging, need to be taken into account, other sensor materials gain in importance [16]. High Z semiconductor compound materials, like gallium arsenide (GaAs), cadmium telluride (CdTe) or cadmium

Table 1.2. The properties of the most popular sensor materials at 300 K.

Material	Si	GaAs	CdTe	CZT
Atomic Number	14	31/33	48/52	48/30/52
Density [g/cm ³]	2.33	5.32	6.2	5.9
Band gap [ev]	1.12	1.43	1.5	1.6
Electron – hole pair creation energy (E_{EH}) [eV]	3.62	4.2	4.43	4.6
Electron mobility [cm ² /Vs]	1450	8000	1150	1350
Hole mobility [cm ² /Vs]	450	400	110	50
Electron lifetime [s]	10 ⁻⁴	10 ⁻⁸	10 ⁻⁶	10 ⁻⁶
Hole lifetime [s]	10 ⁻⁴	10 ⁻⁸	10 ⁻⁶	10 ⁻⁶

zinc telluride (CZT) have become particularly attractive in high energy physics and medical applications due to their high photoelectric absorption cross-section for high photon energies in comparison with silicon. Compared to Si sensors, CZT and CdTe sensors can be massive despite of low thickness and provide high stopping power for the higher energy X-rays [26]. As far as GaAs is concerned, being a direct semiconductor with high electron mobility, it is widely used in the high speed electronics. However, the short carrier lifetime entails incomplete charge collection due to charge trapping [16].

A hybrid approach in semiconductor position sensitive detectors enables choosing a sensor made of the optimum material, determined by the requirements of a specific application.

1.5.5 Readout integrated circuit

The motion of charge carriers in the sensor volume induces electrical currents on the electrodes. A readout integrated circuit for a hybrid pixel semiconductor X-ray detector consists of dedicated electronic channels, one for each sensor pixel. A general task for a readout integrated circuit in a single photon counting device is to register each photon-sensor interaction event and assign it to one of the sensor channels. Each readout channel is designed to amplify and process the induced signal, therefore a typical readout channel architecture comprises a preamplifier, a pulse shaper, and a digital circuit which determines the final system response [33], [34], [35]. The standard readout architecture is presented in Fig.

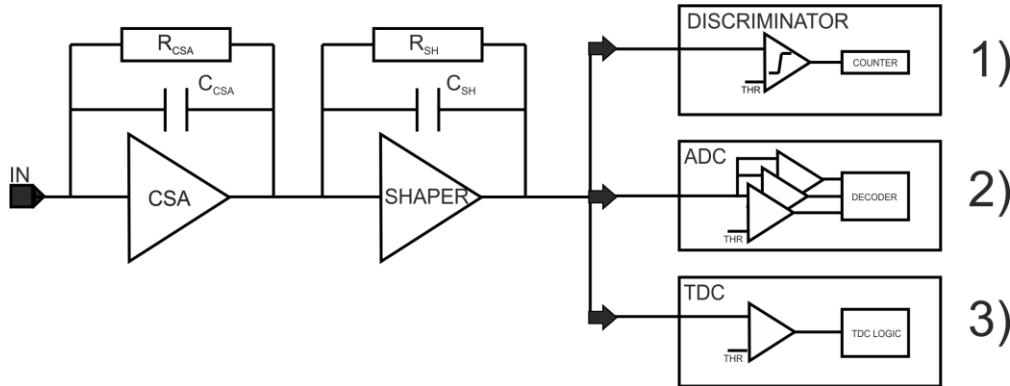


Fig. 1.9 A standard architecture of a readout channel of a hybrid pixel detector with the alternative methods of digitization.

1.9. A charge sensitive preamplifier (CSA) integrates a current signal, resulting in a voltage step with an amplitude proportional to the charge detected. Then, the signal is amplified and filtered according to the SNR and timing requirements by a block which is called a shaper. Finally, a digital circuit determines the system response based on the analog information, stores the result locally and transmits to the data acquisition system. There are several methods of digitising an analog signal and the most common ones include: binary readout (option 1), employing one or more discriminators and a counter, an on-pixel ADC (option 2) [36][37][38], and finally Time-to-Digital conversion TDC (option 3) [39]. The popular method of amplitude spectroscopy is the time measurement when the signal is above a threshold, which is called Time-over-Threshold ToT [40][41][42].

The standard approach to the implementation of a readout channel cannot respond to the problem of the impact of charge sharing on the detector performance. To address this problem, the readout channel should be equipped with some additional inter-pixel circuitry for dealing with charge sharing. This aspect is described in Section 2 in detail.

It should be noted that the hybrid pixel detector performance suffers not only from the sensor-based effects but also from the integrated circuit-based limitations, since the readout integrated circuit design process involves trade-offs between contradictory design constraints. These limitations and their impact on the integrated circuit design are described in Section 1.6.

1.5.6 Methods of estimation of analog chain parameters

The analog chain parameters, such as gain or noise are typically optimised during a design process. However, due to the process mismatch, described in Section 1.6.1, the parameters vary from channel

to channel. There is a need of extracting the analog chain parameters of all channels to evaluate the detector performance and to allow trimming of the system parameters. In this section, typical methods of measurement and estimation of DC offset at the discriminator input, gain and noise, expressed in terms of equivalent noise charge (ENC), are described.

The following conditions are assumed: linearity of the detector with the standard architecture of a channel and a binary readout, no charge sharing and a Gaussian distribution of the signal amplitude at the shaper output corresponding to a given photon energy. Then the probability that the pulse amplitude is higher than the energy threshold value is given by Eq. 1.15.

$$p = \frac{1}{2} \left(1 - \operatorname{erf} \left(\frac{E_{th} - E_0}{\sigma_E \sqrt{2}} \right) \right) \quad \text{Eq. 1.15}$$

where erf is the error function [43], E_{th} is the energy threshold, E_0 is the photon energy, σ_E is the cumulative factor representing Fano fluctuations and electronic noise.

Therefore, the mean number n of the registered photons above the threshold value expressed in terms of the threshold voltage V_{th} , can be given by Eq. 1.16.

$$n(V_{th}) = \frac{1}{2} N_0 \left(1 - \operatorname{erf} \left(\frac{V_{th} - V_0}{\sigma_t \sqrt{2}} \right) \right) \quad \text{Eq. 1.16}$$

where N_0 is the number of photons interacting with a sensor, V_0 is the threshold voltage corresponding to the photon energy E_0 , σ_t is the cumulative factor corresponding to σ_E .

If the charge sharing phenomenon is taken into account, the formula contains an additional linear factor and is given by Eq. 1.17 [44].

$$n(V_{th}) = \frac{1}{2} N_0 \left(1 - \operatorname{erf} \left(\frac{V_{th} - V_0}{\sigma_t \sqrt{2}} \right) \right) \left(1 - \frac{2\Delta l}{x_0} \left(\frac{V_{th}}{V_0} - \frac{1}{2} \right) \right) \quad \text{Eq. 1.17}$$

where $2\Delta l$ is the width of the pixel area affected by charge sharing, x_0 is the pixel dimension.

A plot of the $n(V_{th})$ function is called an integral energy spectrum. If the $n(V_{th})$ function is differentiated, the obtained plot is called a differential energy spectrum or a pulse height spectrum. A common technique to measure an integral spectrum is monotonic scanning with the threshold voltage at the discriminator input and plotting numbers of events registered by the counter within a given duration of a time frame. Thus, the integral spectrum can be also called a ‘threshold scan’ due to the method of measurement. A sample threshold scan is presented in Fig. 1.10.

To measure a DC offset at the discriminator input, threshold scans are performed without X-ray radiation, since measuring a noise peak is enough to determine the offset. The DC offset can be estimated

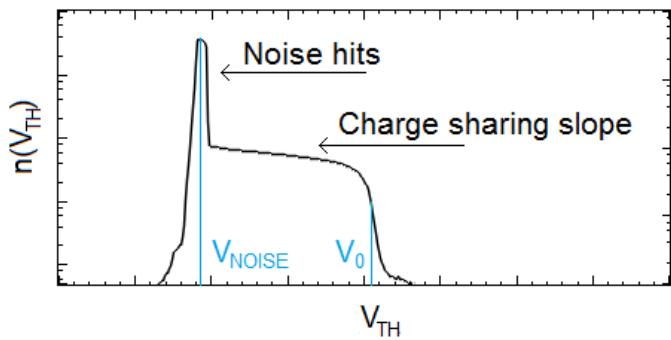


Fig. 1.10 A sample threshold scan plot with the threshold voltages V_{noise}, V_0 marked.

as a shift from the expected threshold level V_{noise} equal to a mean value for the Gaussian model of a noise peak. To measure gain, a threshold scan for all the pixels is performed. Typically, to ensure uniform experiment conditions, the scans are measured in a flat field illumination test. The gain k_V value for a readout channel can be calculated using Eq. 1.18.

$$k_V = \frac{V_0 - V_{\text{noise}}}{Q_0} \quad \text{Eq. 1.18}$$

where Q_0 is the total charge deposited in a sensor by a photon of the energy E_0 . Furthermore, the equivalent noise charge (ENC) value can be calculated using Eq. 1.19

$$\text{ENC} = \frac{\sigma_t}{k_V} \quad \text{Eq. 1.19}$$

In the literature, the ENC for a readout channel is commonly used as a figure of merit for detector characterisation and is related to the system response to an input charge of 1e- [25], [45], [46], [47]. Therefore, to express noise in electrons, the ENC given by Eq. 1.18 is divided by a unit charge $q = 1.602 \cdot 10^{-19} \text{ C}$. Analogously, k_V can be expressed in [V/e-].

1.6 Limitations in readout electronics

A readout integrated circuit for a hybrid pixel detector, working in a single photon counting mode, should meet various, often contradictory requirements, including:

- low power consumption (in the range of several μW per channel) to prevent a multichannel integrated circuit from overheating and damage,
- low noise of readout electronics to maintain large signal-to-noise ratio (SNR), and consequently high detection efficiency,

- fast processing which allows operating with high frequencies of the input pulses, so that two subsequent pulses with the arrival time difference in the sub- μ s range can be distinguished,
- small occupied silicon area, as a layout of the electronic readout must fit to the sensor layout with the pixel pitch in the submillimetre range; by decreasing pixel size, the spatial resolution and the detector maximum count rate per area can be improved.

The design optimisation becomes more difficult due to the limiting factors, which, in real detection systems, cause degradation of the energy resolution and the count rate. These factors include, among others, mismatch of circuit components due to the process variations, electronic noise, pulse pile-up and crosstalk.

1.6.1 Mismatch

On the one hand, a small occupied silicon area is a requirement for novel readout integrated circuit designs. On the other hand, more complicated functions of a readout channel, for example involving anti-charge-sharing algorithms are needed. To fit more components in a smaller available space, transistors of smaller dimensions are used in the design. The access to the new deep submicrometre technologies (180nm, 130nm, 40nm etc.) allows scaling down single channel sizes, maintaining the desired functionality. However, even in the newest technologies, the analog parameters are subject to random variations. This happens due to process mismatch resulting in fluctuations of the gate oxide thickness, doping concentrations, components geometry and systematic global variations, for example due to the voltage drop along pixel columns or oxide thickness gradients over the chip [16]. These variations translate into DC offset and gain mismatches, which reduce the overall system performance. The impact on the performance is even more significant in the case of integrated circuits with implemented complex inter-pixel communication. An example of such case is an integrated circuit with algorithms dealing with charge sharing.

To give an insight into how the mismatch of the parameters of a single transistor affects the analog parameters of a readout channel, calculations of standard deviations of the threshold voltages, according to the Pelgrom's model [48] are performed for two technology nodes. Variations of the threshold voltages are directly translated into the variations of DC offsets at the discriminator input.

The threshold voltage V_T and the current factor β are the dominant sources of gate-source voltage or the drain-source current mismatch for two matched MOS transistors [49]. The current factor β is defined by Eq. 1.20.

$$\beta = \mu C_{\text{ox}} \frac{W}{L} \quad \text{Eq. 1.20}$$

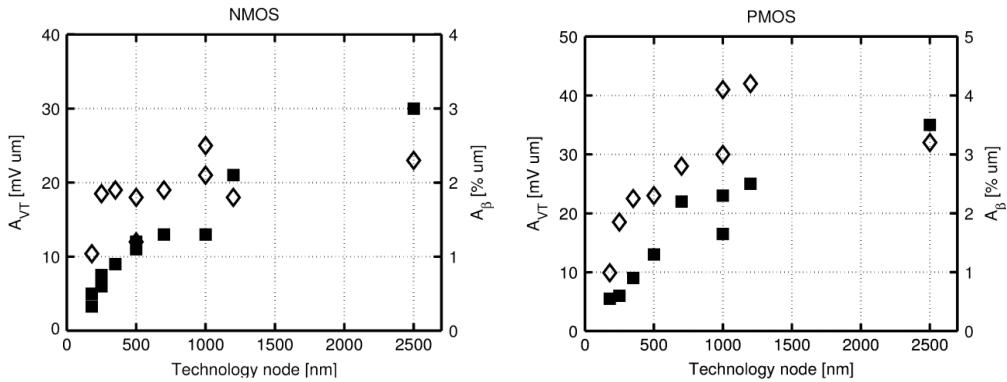


Fig. 1.11 The technology dependent constants A_{VT} represented with black squares, and A_β represented with diamonds for a) NMOS and b) PMOS devices (figures from [49]).

where μ is the carrier mobility, C_{ox} is the gate oxide capacitance, W is the gate width, L is the gate length. According to the Pelgrom model, these random differences have a normal distribution with zero mean and a variance inversely proportional to the transistor area WL , given by Eq. 1.21 and Eq. 1.22 [49] for two closely spaced transistors with sizes not too close to minimal.

$$\sigma^2(\Delta V_T) = \frac{A_{VT}^2}{WL} \quad \text{Eq. 1.21}$$

$$\left(\frac{\sigma(\Delta\beta)}{\beta} \right)^2 = \frac{A_\beta^2}{WL} \quad \text{Eq. 1.22}$$

where V_T is the threshold voltage, β is the current factor, A_{VT} and A_β are the technology dependent constants. The experimentally calculated constants A_{VT} and A_β for selected technology nodes are presented in Fig. 1.11 for NMOS and PMOS transistors.

Considering, for example, an NMOS device in a 250 nm process with $A_{VT} = 7.5 \text{ mV}\mu\text{m}$ and in a 180 nm process with $A_{VT} = 3.3 \text{ mV}\mu\text{m}$ [50], the threshold voltage dispersion $\sigma(V_T)$, calculated from Eq. 1.21 for two transistors of the sizes $W = L = 0.5 \mu\text{m}$ and $W = L = 5 \mu\text{m}$ are given in Table 1.3. Increasing device dimensions and technology scaling indeed reduces the threshold voltage dispersion. Mismatch

Table 1.3. The threshold voltage dispersion $\sigma(V_T)$ for selected two technology nodes and two transistor sizes.

	$W = L = 0.5 \mu\text{m}$	$W = L = 5 \mu\text{m}$
Technology node 250nm	15 mV	1.5 mV
Technology node 180nm	6.6 mV	0.66 mV

can also be reduced to some extent by using the component matching techniques in layout design, such as avoiding minimum transistor sizes allowed by a technological process, using common-centroid geometries, using the same device orientation etc. [51]. However, trimming circuits are usually necessary in multichannel integrated circuits with pixels of small dimensions to mitigate the impact of device mismatch on the system performance. The readout channel scheme with additional trimming features is presented in Fig. 1.12. The main parameters which can be trimmed are DC offsets at the discriminator input and gains of the charge sensitive amplifier (CSA) or the shaper, since variations of these parameters may result in an increased noise hit rate or decreased sensitivity of a detector.

Dynamic storing of an analog correction voltage on a capacitor and static trimming DACs are the two techniques typically used for DC offsets trimming [16]. The first method provides good precision, at the cost of the need of periodic refreshing of the stored quantities. Therefore, it is useful for a synchronous circuit operation or for the applications with short exposure times [52]. The second method, not requiring any refreshing, is commonly used with usually 3-bit up to 8-bit DACs. The monotonicity and linearity of the DAC significantly improves the correction procedure performance, however, such DACs with monotonic and linear characteristics occupy more space in silicon. More detailed investigation of the monotonic DAC design for a hybrid pixel detector can be found in [53].

Gain correction techniques usually involve implementing an amplifier circuit with an adjustable value of the feedback capacitance (C_{CSA} or C_{SH}). The capacitors of different values, connected in parallel, can be switched on as required with a programmed value stored in a register. This allows setting the amplifier feedback capacitance independently in each channel for adjusting the gain in order to minimise the pixel-to-pixel gain spread in the whole pixel matrix. In further chapters pixel-to-pixel gain spread is called gain spread, for the sake of simplicity.

In the following chapters, the trimming procedures definitions and the impact of correction techniques are investigated, both on the simulated and experimental level.

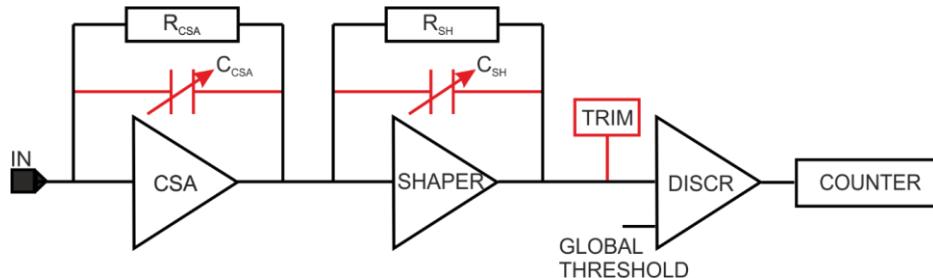


Fig. 1.12 The standard architecture of a readout channel for a hybrid pixel detector with added DC offset and gain trimming features.

1.6.2 Electronic noise

Electronic noise is usually expressed in terms of ENC. The ENC value is defined as an amount of input charge, for which the signal-to-noise ratio at the shaper output equals 1. The lower the noise, the better the performance of the detector is, since it improves timing and energy resolution. For example, to distinguish photons of lower energies, large ENC makes setting a threshold difficult or impossible. ENC for a detector with a capacitive sensor and processing electronics with a band pass filter can be expressed by Eq. 1.23 [54], [55].

$$ENC^2 = ENC_i^2 + ENC_v^2 + ENC_f^2 \quad \text{Eq. 1.23}$$

where ENC_i is the current parallel component of the equivalent noise charge, ENC_v is the voltage series component of the equivalent noise charge, ENC_f is the voltage flicker noise component of the equivalent noise charge. These components can be further expressed by Eq. 1.24, Eq. 1.25, Eq. 1.25

$$ENC_i^2 = F_i \tau_s \alpha \quad \text{Eq. 1.24}$$

$$ENC_v^2 = F_v \frac{(C_{CSA} + C_{in})^2}{\tau_s} \beta \quad \text{Eq. 1.25}$$

$$ENC_f^2 = F_f (C_{CSA} + C_{in})^2 A_F \quad \text{Eq. 1.26}$$

where F_i, F_v, F_f are the constants for the semi-Gaussian shapers determined by the filter type (for example for a CR-RC filter $F_i=F_v=0.92, F_f=3.70$ [56]), C_{CSA} is the feedback capacitance, C_{in} is the input capacitance, including the detector capacitance, τ_s is the shaper peaking time, and α, β, A_F are the parameters related to the power spectral density of the current and the power spectral density of voltage noise and are given by Eq. 1.27, Eq. 1.28.

$$\frac{dI_n^2}{df} = 2qI_{DET} + \frac{4kT}{R_{BIAS}} + \frac{4kT}{R_{CSA}} = \alpha \quad \text{Eq. 1.27}$$

$$\frac{dV_n^2}{df} = \frac{4kT\gamma_n}{g_m} + \frac{K_f}{C_{ox}^2 W L_f} = \beta + \frac{A_F}{f} \quad \text{Eq. 1.28}$$

where $\frac{dI_n^2}{df}$ is the power spectral density of the parallel current noise sources, q is the elementary charge, I_{DET} is the detector leakage current, k is the Boltzman constant, T is the temperature, R_{BIAS} is the detector bias resistance, R_{CSA} is the CSA feedback resistance, $\frac{dV_n^2}{df}$ is the power spectral density of the voltage noise of the input transistor, γ_n is the coefficient dependent on the transistor channel length (in the range between $\frac{1}{2}$ and $\frac{2}{3}$), g_m is the input transistor transconductance, C_{ox} is the input transistor gate oxide

Table 1.4. A sample detector parameters assumed for ENC calculations based on [56], [66].

Parameter	Value	Unit	Parameter	Value	Unit	Parameter	Value	Unit
F_i	0.92		C_{CSA}	10	fF	K_f	10^{-28}	C^2/m^2
F_v	0.92		C_{in}	500	fF	C_{ox}	1.75	fF/ μm^2
F_f	3.70		R_{BIAS}	∞	Ω	W	18	μm
k	$1.38 \cdot 10^{-23}$	J/K	R_{CSA}	150	M Ω	L	0.2	μm
T	298	K	I_{DET}	1	pA	γ_n	2/3	
q	$1.602 \cdot 10^{-19}$	C				g_m	100	$\mu A/V$

capacitance, W is the transistor width, L is the transistor length, K_f is the coefficient associated with flicker noise, f is the frequency.

Thus, in general, three factors, namely, current white noise, voltage white noise and flicker noise ($1/f$) contribute to the total ENC. The dependency of these factors on the shaper peaking time τ_s for a sample detector, is illustrated in Fig. 1.13. The parameters of a sample detector assumed for the sake of the ENC analysis are listed in Table 1.4.

It can be concluded that the flicker noise component is independent on the shaper peaking time and is dependent on the input capacitance, thus it can be optimised by choosing low noise elements and technology process. Voltage white noise decreases with the shaper peaking time increase, and is proportional to the sum of the input and the feedback capacitances. However, long shaper peaking time limits the speed of the detector. The current white noise increases with the shaper peaking time increase, nonetheless, it can be reduced by minimising the detector leakage current and lowering the operation temperature. Additionally, from the viewpoint of the noise optimisation, the values of the R_{BIAS} and R_{CSA} resistors should be large, yet, large R_{CSA} negatively influences the high count rate performance.

ENC can be minimised by the input stage and shaping filter optimisations [57], [58], [59]. Although it is possible to optimise the detector parameters to find the minimum ENC value, choosing an optimal value of the shaper peaking time, the shaper architecture, and the input capacitance is a trade off between the contradictory noise and speed requirements. For example, in the chip design described in Chapter 4, the maximum detector count rate was increased at the cost of ENC, so the lower shaper peaking time values were chosen to meet the high count rate requirements.

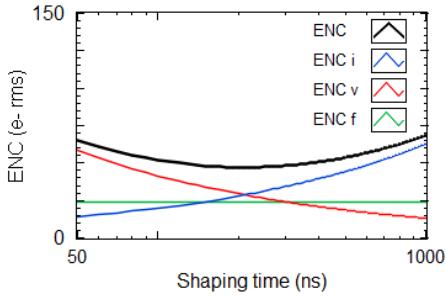


Fig. 1.13 The ENC components versus shaper peaking time τ_s .

1.6.3 Pulse pile-up

The pulse pile-up is an overlap of signals generated by arrivals of two consecutive photons closely spaced in time. If the second pulse occurs too fast, the signal at the shaper output does not switch the discriminator because the signal amplitude remains higher than a threshold during both pulses processing. In general, the pile-ups occur when a signal at the amplifier output does not return to the baseline before a new pulse arrives. The arrival may happen either when the signal is above the baseline or on the negative undershoot. The first type of pile-up happens when the signal has not crossed the baseline yet before the next pulse arrives and leads to a positive DC voltage shift. The latter is a consequence of non-ideal integration and shaping and results in a negative DC voltage shift. The shifts and the pulses overlap degrade energy resolution of the detector and for high count rates lead to missing the events occurring too fast one after another.

A natural way to reduce the event loss is to accelerate processing in the system. The speed can be improved by optimising the filter design, choosing the proper filter type and order, and, in particular, by minimisation of the filter peaking time. However, what was shown in Section 1.6.2, with a decrease of the peaking time, contribution of voltage white noise increases, increasing the total ENC. Other solutions improving detector speed, which are used in circuit designs, are pole-zero cancellation circuits and base-line restorers. A pole-zero cancellation circuit compensates the unwanted pole of the CSA by introducing a zero to a channel transfer function [56]. As a consequence, it deals with the signal undershoot at the shaper output. A simple base-line restorer consists of a memory capacitor and a switched resistance, which is switched off when a pulse arrives [56]. This allows minimisation of the base-line shifts for unipolar pulses.

A detector system responds to an event with a physical process which takes a certain amount of time. This time, in which the detector is non-responsive, is called ‘dead time’. The two approaches to detector modelling, namely paralysable and non-paralysable model, are usually used. In both models

a detector stays non-responsive for a period of time, after each pulse detection. However, in a paralysable model the subsequent pulse extends the non-responsive period, which results in the total blockage of registration for high fluxes, whereas a subsequent pulse is ignored in a non-paralysable model. The paralysable model represents well the full readout channel behaviour, thus, it is commonly used to describe detectors. However, other, more complex models are also introduced [60], [61]. The paralysable detector model, is given by Eq. 1.29.

$$N_{\text{out}} = N_{\text{in}} e^{-\tau N_{\text{in}}} \quad \text{Eq. 1.29}$$

where N_{out} is the output count rate (counts/pixel/s), N_{in} is the input count rate (counts/pixel/s), τ is the dead time.

To illustrate the behaviour of a typical detector response for a high photon flux, simulations were performed. The generation of X-ray photons by an X-ray tube or by a radiation source is a random in nature process. The number of photons detected in a time window follows the Poisson statistics [62]. Let X be a random variable that describes a number of photons hitting a detector within a specific time interval T . X is a Poisson distributed random variable with a parameter λ ($X \sim \text{Poisson}(\lambda)$), where λ is the average number of events expected to occur within a specific time interval. For comparison, a model assuming synchronised pulses of the count rate equal to λ is examined. The time $\tau = 100$ ns needed for the pulse processing by a readout channel is assumed. In the standard channel architecture, the dead time τ is mainly determined by the shaper peaking time and can be defined as the time during which the discriminator signal stays high.

The simulated Poisson distributed pulse train is shown in Fig. 1.14. The trivial case of the uniformly synchronised pulse train is not presented. A pile-up can be observed in the case b) and c), when the subsequent pulses overlap. The output count rates N_{out} were calculated for increasing values of the input count rates N_{in} up to 10 Mcounts/s and the simulation results are presented in Fig. 1.15. Since in real devices, arriving photons are Poisson distributed, in contrast to synchronised photons, the total blockage of the detector system due to a pile-up occurs for count rates higher than 10M counts/s. However, the detector response is degraded with the 10% counts loss for the input count rate equal to 2.6M counts/s, assuming $\tau = 100$ ns.

In conclusion, a pile-up is an undesired, but an inevitable effect, which degrades the detector high count rate performance. However, several techniques including filter optimisation and additional circuitry implementation can reduce the dead time and improve the detector speed [63], [64], [65].

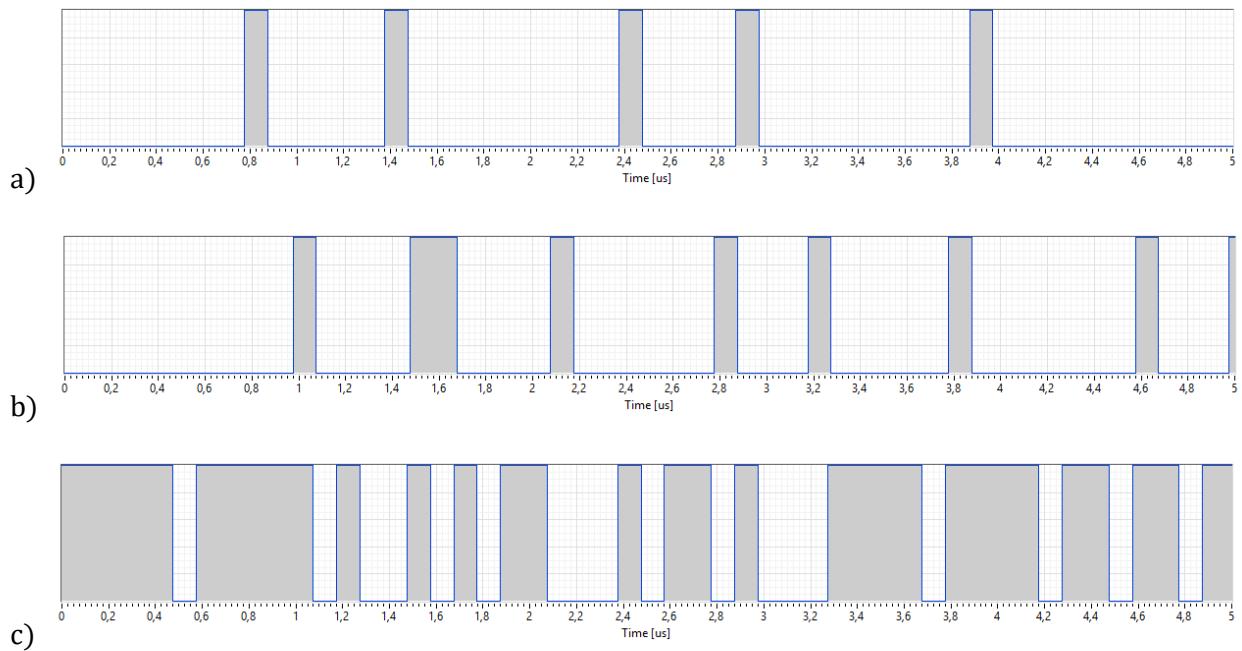


Fig. 1.14 The Poisson distributed pulse trains for $\tau = 100$ ns, $T = 1 \mu\text{s}$ and a) $\lambda = 1$, b) $\lambda = 2$, c) $\lambda = 10$.

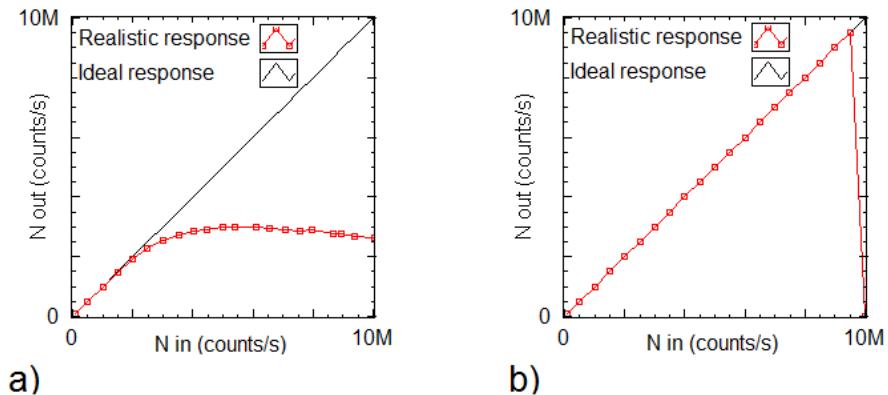


Fig. 1.15 The output count rates as a function of input count rates for a) Poisson distributed pulses, b) synchronised pulses.

1.6.4 Crosstalk

Crosstalk, defined as an undesired interaction between different circuits on the same die, is a common problem in mixed-mode integrated circuits containing high performance analog circuits and fast digital blocks. Fast switching signals of the digital part of the readout integrated circuit may introduce errors in the sensitive analog circuits, which leads to degradation of the pulse processing,

and consequently, to the poorer photon registration. There are several techniques used to minimise cross-talk, including reduction of generated switching noise, increasing the insensitivity of analog blocks and providing proper isolation between digital and analog parts. A study of the cross-talk minimisation is presented in [66].

1.6.5 Conclusions on integrated circuit limitations

Designing multichannel readout integrated circuits for hybrid pixel detectors involves balancing between contradictory constraints put on the maximum available silicon space, power dissipation, electronic noise and speed of pulse processing. Additionally, the spread of the analog parameters between channels and minimisation of crosstalk should be taken into account. For example, achieving high rates of circuit operation, desired from the viewpoint of the detector speed, may introduce a crosstalk effect. Some circuit architectures used for crosstalk minimisation, may increase noise, though [56]. Low noise, as well as better mismatch can be easier achieved in larger pixels, however, from the viewpoint of the spatial resolution and detector maximum count rate, minimisation of channel sizes is required.

Moreover, with a decreasing pixel size, detector systems suffer more significantly from charge sharing and the standard approach to the implementation of a readout channel cannot solve the problem of the impact of charge sharing on the detector performance. When photon interactions occur close to a pixel corner, each of the four neighbouring pixels registers a signal of a reduced amplitude. Consequently, the system detects more than one parallel event, each initiated by a lower energy photon. In this case, both the hit position as well as the photon energy are improperly recorded. What is more important, some of the events may not be registered at all when a fractional signal in none of the neighbouring pixels exceeds a given threshold.

To conclude, the design and implementation of the integrated circuits for X-ray hybrid pixel detectors is a complex process and requires specialised tools and methods of optimisation. All the solutions, implemented inside a chip, need detailed research and assessment on the simulation level. The simulations and system verification become even more challenging if inter-pixel communication is implemented inside a chip, for example for dealing with the charge sharing effect.

2 DEALING WITH CHARGE SHARING – ALGORITHM CONCEPTS, SELECTED ASICs AND OWN PROTOTYPE SOLUTION

To overcome problems related to the charge sharing effect, various hardware algorithms have been proposed and some of them were implemented in silicon [8], [67]–[70]. In some applications, an off-chip correction of detection data is also possible [40], [71], [45]. The aim of this chapter is to present general requirements, which an algorithm dealing with charge sharing needs to meet. Moreover, the selected solutions, whose operation is assisted by digital blocks, presented in the literature, are discussed. Finally, the prototype implementation of the algorithm, called C8P1, which will be the subject of the simulations presented in the next chapter, is introduced.

2.1 Algorithm concepts for dealing with charge sharing

The common aim of algorithms dealing with charge sharing is to reconstruct the signal as if the total charge deposited by a single photon would be processed in a single channel. It is also necessary to assign an event to a pixel in a group, preferentially to the one with the largest charge deposition. The first task can be realised by summing signals from the pixels which contribute to the photon detection. The second one usually involves designing a decision logic which compares information from the pixels in a formed group, while the process of a group formation is defined by the algorithm. Performing these two simultaneous tasks requires development of an extensive inter-pixel communication system, since neighbouring pixels firstly, need to be ‘aware’ of each other’s existence and secondly, they trigger each other to perform the allocation process at the right moment.

There are several challenges for on-chip algorithms dealing with charge sharing, mainly caused by the fact that the pixels need to work in parallel in an asynchronous system. One of the challenges is defining the size of the pixel group considered by the algorithm and defining how the information

is shared among these pixels. A size of a charge cloud in the sensor when charge reaches the collection electrodes depends on the combination of parameters such as sensor material and thickness, pixel pitch, radiation nature and photon energy. However, most commonly the charge is assumed to be shared between maximum four pixels. Thus, four pixels sharing a corner are, by definition, in the pixel cluster taken into account by the algorithm and used to determine a winner (these pixels for simplicity will be called ‘activated’). However, a larger pixel array needs to be typically involved in the process of hit allocation. For example, more pixels can be activated to check if the charge deposited is the highest among the neighbours by the means of simple comparison. Moreover, the group of activated pixels dynamically changes, in particular, it shrinks in time when some of the signals are too low to be considered by the algorithm as the pixels with the highest charge deposition. In fact, the size of the group of activated pixels is algorithm specific, but it is desired to have this group as small as possible due to several reasons. First of all, implementing physical connections and communication between the pixels on a chip occupies space. Secondly, the pixels in a group are disabled from registration of new hits for some time. Moreover, assuring unambiguity is a challenge when a group is larger.

The other challenge that should be considered is the availability of the information shared between the pixels. The communication between pixels should take long enough for the pixels to be aware of the registration process and to fully exchange the required information about the collected charge. However, it cannot be too long, since all the pixels in the activated group are inhibited from registration of another event while they still contribute to the allocation process. That is why, the question arises how to determine the moment of latching the result. The solution is not obvious since there is no clock. Thus, it is not possible to assure the synchronicity between the pixels. The group of activated pixels can dynamically change, and a change of state has to be communicated to all the pixels in the group.

There is no universal solution, which can address all the aforementioned issues, because every algorithm always suffers from trade-offs between speed, accuracy, resistance to noise and complexity of the design. In the next section, several examples of the designs are presented, however, it should be noted, that due to insufficient and selective information available in the literature, not all the implementation details are described.

2.2 Selected ASICs

There are several solutions dealing with charge sharing already implemented and tested on a chip. The examples of integrated circuits with such algorithms are listed in Table 2.1. Parameters in Table 2.1 are given, provided that they are available in publications. However, descriptions of implementations of the algorithms are often ambiguous or incomplete. There is also no common vocabulary for the basic

concepts and implementation of the algorithms. That is why before presenting the selected ASIC solutions, the systemized vocabulary used in the algorithm descriptions is introduced, so that the algorithms can be more easily understood and compared.

The key terms, often used interchangeably:

- Hit, event – photon interaction with a sensor,
- Fractional charge – charge collected by a single pixel,
- Charge reconstruction, charge summing – a process of adding fractional signals corresponding to charges from the adjacent pixels,
- Adding node, summing node, signal rebuild hub (SRH), reconstruction node – a circuit responsible for signal reconstruction typically from four pixels sharing a corner, realised, depending on a specific solution, in the voltage or current mode,
- Adjacent, neighbouring pixels – a group of pixels sharing an edge or a corner with a given pixel in a square layout,
- Neighbourhood, local neighbourhood, pixel cluster – activated group of pixels,
- Event allocation, hit allocation, charge assignment – process of assigning an event to the pixel in the neighbourhood with the largest charge deposition,
- Winning pixel, winner, chosen pixel – the pixel in the neighbourhood which gets a hit assigned.

The next sections are dedicated to the general descriptions of each of the solutions from Table 2.1 to a degree permitted by the level of details found in the literature.

2.2.1 Pixirad Pixie III

In PIXIE III [8], configured to deal with the charge sharing effects, the signals of four adjacent pixels are added to evaluate the total energy of a photon in the case of charge sharing between up to four pixels. To avoid multiple counts, the algorithm assumes also that only one counter in one pixel per event is allowed to count. This is implemented using the Time-Over-Threshold technique on the discriminator output pulse. If an event is registered in several pixels, the algorithm allocates the hit to the pixel with the highest charge fraction.

Table 2.1 The ASICs with charge reconstruction algorithms, according to [10], [19], [22], [24], [34]

ASIC	CMOS process	Pixel array node	Pixel Size (μm^2)	No. of transistors per pixel	Algorithm name	Charge reconstruction technique	Dead time (μs)
Large scale ASICs							
Pixirad III [8]	Pixie 160	512x402	62x62	1.5k	Pixel summing mode	Current ToT mode	0.2
X-Counter [70]	180	128x256	100x100	2.3k	Charge sharing correction feature	-	0.12
Medipix3 [73], [101]	130	256x256	55x55	1.6k	Charge summing algorithm	Current ToT mode	7
Medipix3RX [75]	130	128x128	110x110	1.8k	Charge summing algorithm	Current ToT mode	2.02
Prototypes							
Chase Jr. [67], [78]	40	18x24	100x100	4.5k	C8P1	Voltage Amplitude mode comparison	1.01
miniVIPIC [68]	130	32x32	100x100	4k	C8P1	Voltage Amplitude mode comparison	-

2.2.2 X-Counter

According to [70], the algorithm assumes that if pulses from two or more nearest neighbours coincide in time, such a case is regarded as one event and the total charge is attributed to the pixel with the highest charge among neighbours. Dealing with a trade-off between the energy resolution and the maximum count rate, the algorithm takes into account only the closest neighbours instead of a larger pixel cluster, since the issue of the maximum counting speed is the priority.

2.2.3 Medipix 3/3RX

A version of the ‘charge summing algorithm’ for a sensor with the hexagonal pixels was introduced in [72]. However, there is no further information, whether it has ever been implemented in a chip. The algorithm assumes that charge may be shared between all the adjacent pixels, so a cluster of seven pixels is created. The proposed detector layout and the pixel architecture are presented in Fig. 2.1. Each pixel contains a discriminator and its output pulse is sent to its neighbours. This pulse length is proportional to the charge collected by the pixel, so by comparing the pulse duration of all seven pixels in a cluster, the pixel with the highest charge deposited is elected as a pixel in which an interaction occurs. The total energy reconstruction is reported to be achieved by adding up the discriminator pulses or the preamplified signals of the adjacent pixels. The system registers a hit if a pixel collects most of the charge and the signal from a seven-pixel-cluster exceeds a globally set threshold.

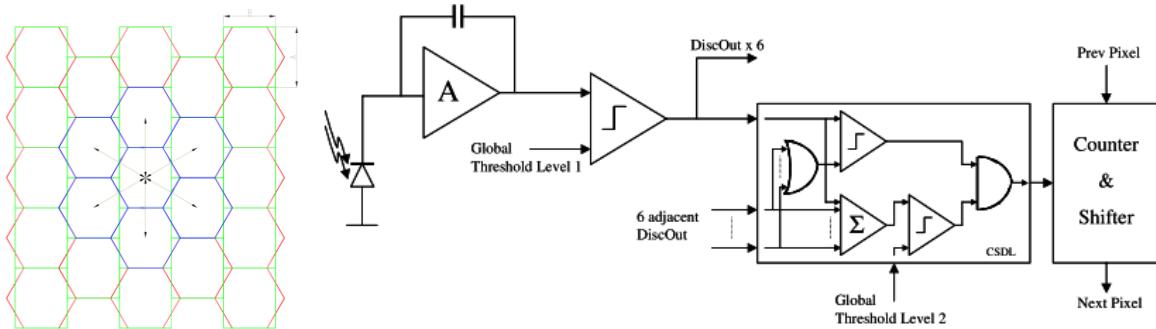


Fig. 2.1 The proposed hexagonal-pixel-detector layout (left) and a pixel architecture (right) revealed as an announcement of future developments for Medipix2, according to [72].

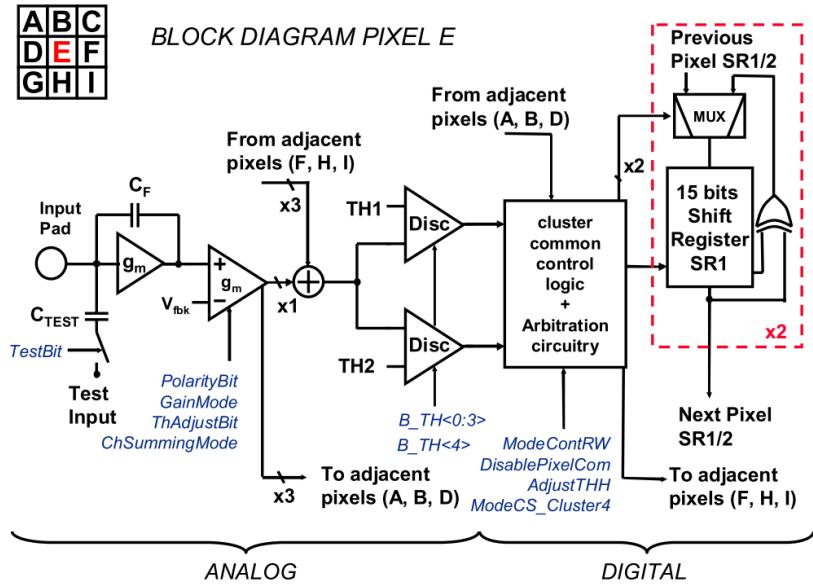


Fig. 2.2 A schematic diagram of the readout channel architecture of Medipix3 according to [73].

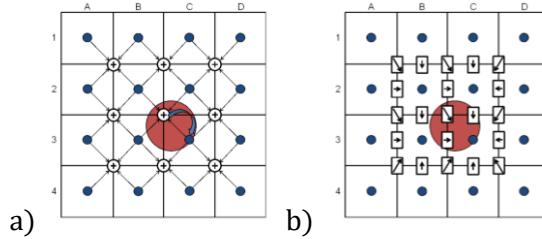


Fig. 2.3 An illustration of the Charge Summing Algorithm according to [75]. a) The local signal is compared with a threshold. The arbitration network determines which pixel receives the largest charge. b) The reconstructed summed signal from four pixels is compared with a threshold.

The next version of the ‘charge summing algorithm’ was introduced for the Medipix3 prototype ASIC [73]. As far as the implementation details are concerned, both an ASIC and a sensor are divided into square pixels, so in this case, each pixel has eight direct neighbours. Each readout channel, presented in Fig. 2.2, consists of a charge sensitive amplifier, a shaper and two discriminators. An inter-pixel communication is implemented by sending currents from the shaper’s outputs to the adding nodes common to four adjacent pixels. The added signals are discriminated and the added signal is assigned to the summing node with the largest sum by a system of arbitrators based on modified RS flip-flops (Seitz’s arbiters [74]). When a pixel wins the arbitration decision, its counter is incremented.

The latest version of the Charge Summing Algorithm is implemented in the Medipix3RX ASIC [75]. The algorithm is based on the two parallel processes, namely, the hit allocation and the charge reconstruction, which are schematically presented in Fig. 2.3. The readout channel of the Medipix3RX ASIC is presented in Fig. 2.4. It can be noticed that readout channels in both Medipix3 versions consists of a charge sensitive amplifier, a shaper, an adding node, discriminators and an arbitration circuitry (see Fig. 2.2 and Fig. 2.4). In Medipix3RX the arbitration decision is based on the comparison of the local pixel charges with the charges collected by its neighbours, whereas in the previous solution, the total charge in one adding node is compared to the adjacent adding nodes. In Medipix3RX during the hit allocation process, the arbitration logic compares the output discriminators signals from a local pixel and its eight neighbours. The decision relies on the timing properties of the discriminator output signal. The Counter0 is incremented, when the largest charge is detected in the local pixel. At the same time the arbitration logic inhibits the Counter0 of the neighbouring pixels, in order not to count the same photon twice. In the charge reconstruction process, the charge from four neighbours is added by a summing circuit. The Counter1 is incremented if two conditions are met: the arbitration logic allocates a hit to this pixel and any of the surrounding summing nodes exceeds a given threshold.

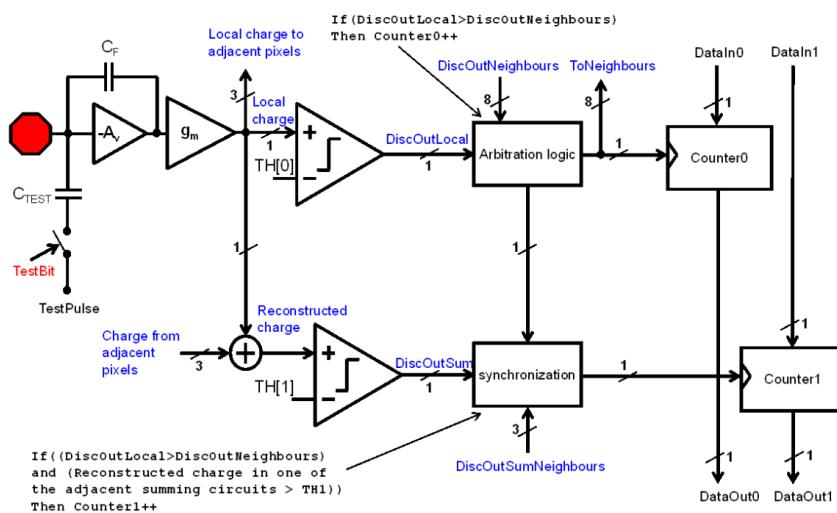


Fig. 2.4 A schematic diagram of the readout channel architecture of Medipix3RX according to [75].

2.3 Prototype solution - C8P1 in miniVIPC and Chase Jr. chip

2.3.1 C8P1 algorithm concept

The algorithm called C8P1 was proposed by the AGH – Fermilab group in 2011[76] as an answer to the solutions presented at that time which struggled with the problems of improper hit allocation and charge reconstruction. Then, the characteristics and parameters of the C8P1 algorithm became the subject of this research aiming at the algorithm performance evaluation and optimisation.

The C8P1 algorithm [77], implemented in the miniVIPC [68] and Chase Jr. chips [67], [78], performs simultaneously two tasks: reconstruction of the total charge deposited by a single photon in a pixel cluster and event allocation to the pixel (among the pixels inside a cluster) with the largest charge deposition. The first problem is solved by summing the signals from four pixels sharing a corner in the voltage mode. If the amplitude of the summed signal is above a predefined threshold, all pixels contributing to the summed signal are activated to compare their own signals with eight pixels adjacent to them. The hit is allocated to a given pixel if the signal amplitude is the highest among its neighbours. Thus, the name of the algorithm comes from the two conditions which have to be met to register a hit: eight comparators point to the pixel and one summed signal in a pixel has to be above a threshold. The idea of the C8P1 algorithm is schematically presented in Fig. 2.5. Each pixel corner has a signal rebuild hub (SRH) marked with a circle. Eight voltage comparators (marked with the grey arrows) are used to allocate the total charge to the pixel with the largest charge deposition.

The readout channel architecture implementing the abovementioned functionality is presented in Fig. 2.6a. When a single photon deposits the charge in one or more pixels, only some fractional charge is collected by a single channel, which is shown in Fig. 2.6b. The signal in a CSA is transformed from a current pulse to a voltage step. The amplitude of the signal is proportional to the deposited charge. Then the signal is processed independently in two paths: a fast path for the total charge reconstruction, and a slow path for the hit allocation.

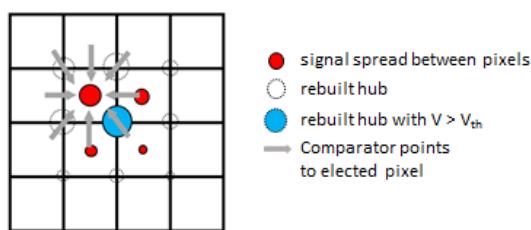


Fig. 2.5 The C8P1 algorithm: reconstruction of the total charge. Figure from [67].

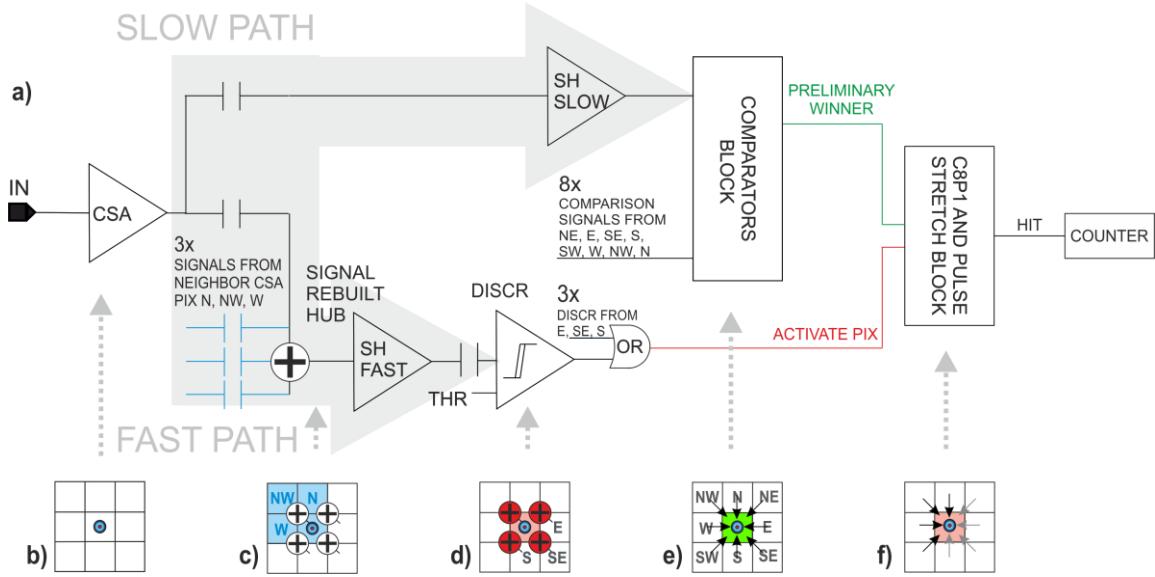


Fig. 2.6 A schematic diagram of the readout channel architecture with the C8P1 algorithm.

In the fast path, the fractional signals from a cluster of 2×2 pixels are added by a SRH presented in Fig. 2.6c. The reconstructed signal is filtered by the shaper-fast (SH FAST). If any of four-neighbour-reconstructed signals exceeds a predefined threshold (a signal from one pixel contributes to four SRHs) the ‘activate pix’ signal is set, what is shown in Fig. 2.6d.

In the slow path, the fractional signal is filtered by a shaper-slow (SH SLOW) and compared with the corresponding signals from the eight adjacent pixels. When the comparators block (containing eight comparators and an AND gate) determines that the signal amplitude is the highest in the entire pixel cluster, the ‘preliminary winner’ signal is set, as presented in Fig. 2.6e. Most of the solutions presented in the literature use the ToT technique to compare signals. However, in noisy conditions, it may introduce uncertainties in time measurements of the discriminator signals. It is due to the fact that the threshold must be set low enough for the system to distinguish the fractional signal corresponding to the $\frac{1}{4}$ of the target energy. Assuming the low threshold setting and taking into account a typical form of a semi-Gaussian CR-RCⁿ waveform at the shaper output, it should be noted that the moment when the signal falls below the threshold is detected on a low slope of the signal, and consequently, in this area the time measurement is more susceptible to noise. As a result, the smaller-amplitude signal may be incorrectly considered as being of the larger amplitude. In such case, the hit can be improperly allocated [77]. That is why,

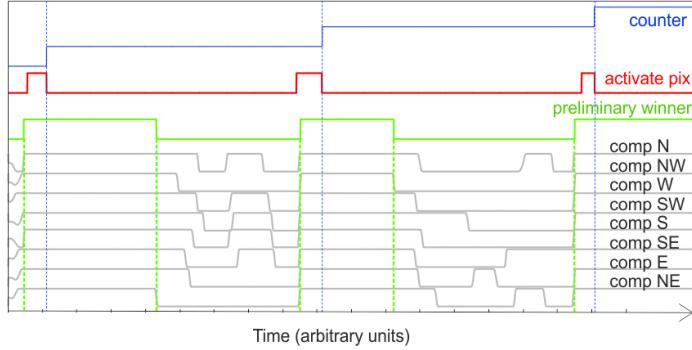


Fig. 2.7 The logic signals used by the C8P1 block to determine if the hit counter in the pixel should be incremented.

in the C8P1 algorithm, the comparison of the shapers' slow signals is realised through comparing of the signal amplitudes.

On the basis of the output signals from the two paths: the fast one ('activate pix') and the slow one ('preliminary winner'), the C8P1 digital block assesses if a pixel should register an event, which is presented in Fig. 2.6f. The final decision to increment a hit counter is taken on the negative edge of the 'activate pix' signal. If at that time, the 'preliminary winner' signal is set (all eight comparators point to the pixel), this pixel is latched as the winner. The signals used by the C8P1 block are presented in Fig. 2.7. Eight logic comparator signals (marked as comp N, comp NW, comp W, comp SW, comp S, comp SE, comp E, comp NE), after logically ANDing them together, result in the 'preliminary winner' signal. The 'result latch' time marks in Fig. 2.7 represent three consecutive moments of evaluations on the negative edges of 'activate pix'. At each pointer marked by the 'result latch', all eight comparators point to the pixel to be the winner and as a result, the counter in this pixel is incremented. In between the moments of 'result latch', the comparators may change their states.

2.3.2 Two implementations of C8P1 algorithm

The C8P1 algorithm is used in two chips: Chase Jr. and miniVIPC. These two implementations slightly differ in terms of the C8P1 block realization. Moreover, in the Chase Jr chip additional discriminator is added, which allows setting a double threshold and register the photons in a given energy window. The two simplified schematic readout channel architectures of the miniVIPIC and the Chase Jr. chips are presented in Fig. 2.8 and Fig. 2.9 respectively. In the Chase Jr. solution, in the C8P1 operation mode, the fast path is equipped with two discriminators, called 'low' and 'high'. Each discriminator is followed by a counter. The thresholds are controlled externally, allowing setting two different energy thresholds

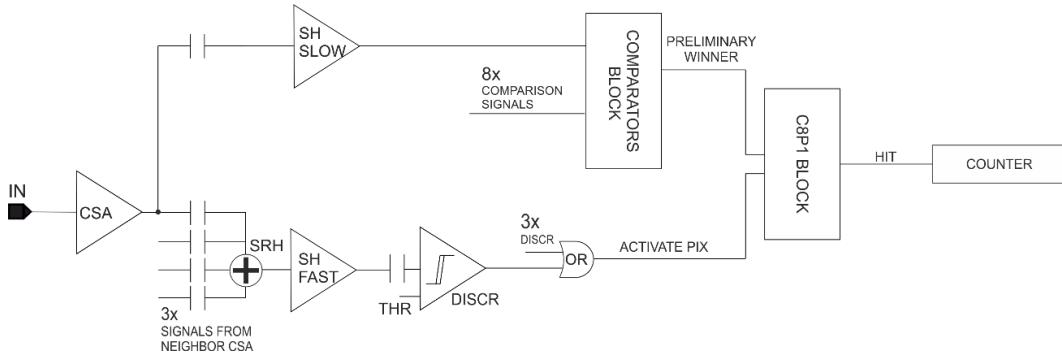


Fig. 2.8 A Schematic diagram of the readout channel architecture of the miniVIPIC chip.

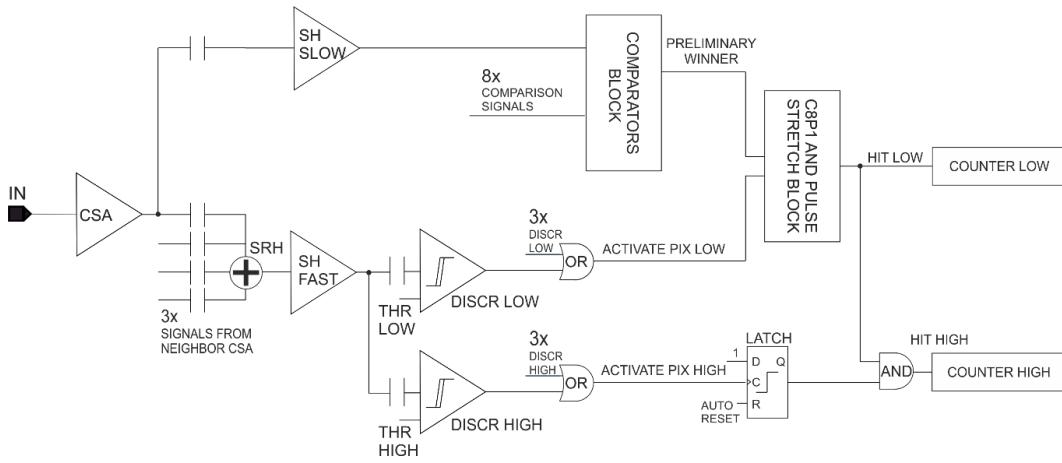


Fig. 2.9 A schematic diagram of the readout channel architecture of the Chase Jr. chip.

for each path – low and high. The ‘activate pix low’ and ‘preliminary winner’ signals are used by the C8P1 block to determine if the hit counter low should be incremented (as previously presented in Fig. 2.7). The counter high is incremented if two conditions are met: the hit is registered using the C8P1 logic and the signal from the shaper-fast exceeds the energy threshold high. This functionality allows counting photons in two overlapping energy bins: photons of the energy higher than the threshold low and higher than the threshold high. By subtracting the numbers of photons in these two bins, the number of photons in an energy window (THR LOW, THR HIGH) can be obtained. The timing diagram of the shaper-fast signal and digital signals ‘activate pix’ and ‘hit’ for two different threshold high settings are presented in Fig. 2.10. If the threshold high is set below the photon energy level (THR HIGH 1 in Fig. 2.10a), both counters low and high are incremented, since the ‘hit low’ and ‘hit high 1’ signals are set, as presented in Fig. 2.10b. In the case of the threshold high set above photon energy level (THR HIGH 2), only the counter low is incremented.

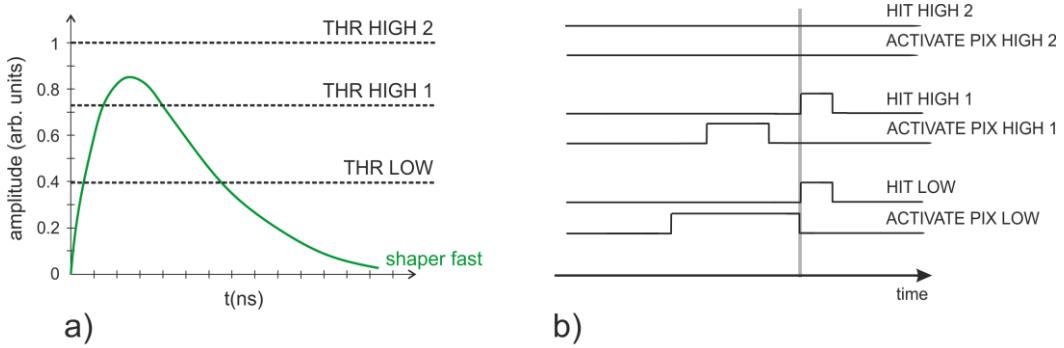


Fig. 2.10 a) A timing diagram of a shaper fast signal and sample threshold settings. b) A timing diagram of the resulting ‘activate pix’ and ‘hit’ signals for given thresholds.

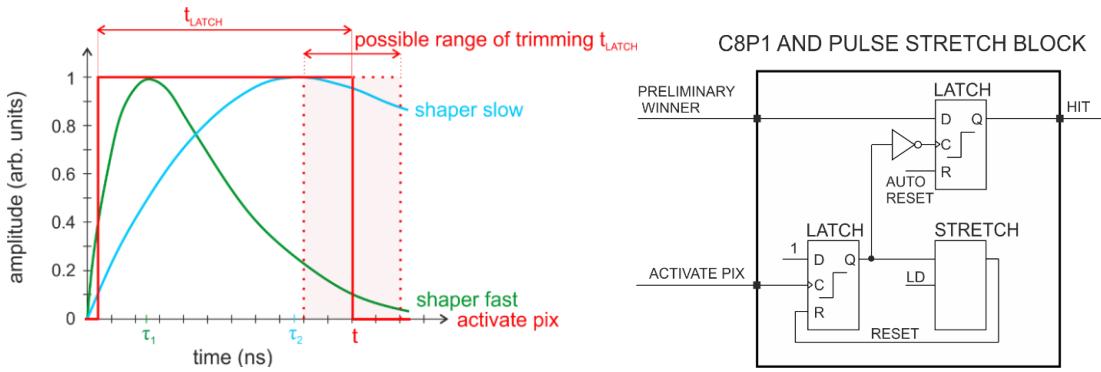


Fig. 2.11 a) A timing diagram of the signals used to determine the C8P1 algorithm result. b) A schematic diagram of the ‘C8P1 and pulse stretching block’.

Another difference between the two implementations of the C8P1 algorithm is the realisation of the C8P1 block. A timing diagram is presented in Fig. 2.11a to illustrate the signal processing in both the slow and fast paths. Parameters τ_1 and τ_2 represent the peaking time of the shaper-fast and the shaper-slow, respectively. The signal at the shaper-fast output is discriminated. Then, the discriminator outputs of the four adjacent pixels are logically ORed to create the ‘activate pix’ signal, which determines the time of comparison of the shapers’ slow signals. Preferably, the comparisons should occur at the shaper-slow amplitude peak. This can be realised using a peak detector to stretch the signals and to compare them effectively as DC signals. Another solution, used in miniVIPIC, is defining the time of comparison based on the shaper peaking time of the shaper fast and mutual relation of the peaking time of the shaper fast and slow. In the Chase Jr. solution, the exact moment of latching the comparison result is defined by the negative edges of ‘activate pix’ signals, however, the time can be adjusted within a predefined range. The duration of the ‘activate pix’ signal is marked as t_{LATCH} in

Fig. 2.11 Fig. 2.11a; the possible range of trimming is coloured. The implementation of this functionality is realised in the 'C8P1 and pulse stretch block' presented in Fig. 2.11b. It allows stretching of the signal 'activate pix', controlled with the register called 'Latch Delay' (LD). The resulting 'activate pix' signal determines the time t_{LATCH} at which the 'preliminary winner' signal is latched.

2.3.3 Example cases of signal processing in C8P1 algorithm

The signal processing has been presented so far from the viewpoint of a single readout channel. Now, the three examples of the signals processing in the pixel matrix are described, to better illustrate the C8P1 functioning. The scenarios when a photon hits the detector in the pixel centre (Fig. 2.12), in between two pixels (Fig. 2.13) and in between four pixels (Fig. 2.14), are described and analysed. The threshold is assumed to be set to the half of the photon energy. In all three cases, the interaction takes place in the pixel P22 and this pixel should be pointed to register this hit by the algorithm. All three figures show the C8P1 decision process in the same order, and the following sections of the figures present:

- a) the position of the photon interaction with the detector (the red dot) and the charge cloud (the blue circle). The state of the pixel matrix at time t_0 – when the charge cloud arrives at the electrodes.
- b) the fast path: the SRHs ('+' sign). The coloured SRHs represent those in which the shaper-fast signals exceed the threshold. Those marked with dark red colour register 100% charge, other register only fractional charge. If the shaper-fast signal in any of four surrounding rebuild hubs exceeds the given threshold, this pixel has 'activate pix' signal set (marked in red). The state of the pixel matrix at time t_1 – at the shaper-fast signal of the pixel P22 amplitude peak.
- c) the fast path: the signals 'activate pix' of 9 pixels – P11, P12, P13, P21, P22, P23, P31, P32, P33.
- d) the slow path: the state of the comparators at the borders between the pixels (the grey arrows). If all eight comparators at the borders of one pixel point to this pixel (the black arrows), the 'preliminary winner' signal is set in this pixel (the pixel marked in green). The state of the pixel matrix at time t_{LATCH} – when the result is latched on the negative slope of 'active pix'.
- e) the slow path: the signals 'preliminary winner' of 9 pixels – P11, P12, P13, P21, P22, P23, P31, P32, P33.

It should be noted that all signals are presented illustratively to introduce the concept, and delays or timing properties of the comparators and discriminators are not considered. The section dedicated to the simulation deals with more realistic models, though.

In the case presented in Fig. 2.12, all the charge is collected by one pixel P22. Therefore, in the fast path, four signal rebuild hubs, surrounding the P22 pixel, fully reconstruct the total amplitude, and the total signals in those hubs exceed the threshold. By definition, nine pixels P11, P12, P13, P21, P22, P23, P31, P32, P33 have ‘activate pixel’ signal set, since they contribute to one of these four signal rebuild hubs. It is worth noticing, that all those nine pixels are activated due to the signal received by only one pixel P22. In the slow path, the comparators continuously track the signals from the adjacent pixels, comparing their temporary amplitudes. Before the registration on the falling edge of the ‘activate pix’ signal occurs, the pixels can have the ‘preliminary winner’ signal changing even multiple times, for example, due to noise. However, the hit is not registered in this case, since the noisy input signal is of a low amplitude and it does not exceed the threshold. The result is latched on the negative edge of the ‘activate pix’ signal, and in this case, the ‘preliminary winner’ signal is set for the P22 pixel, which increments its counter.

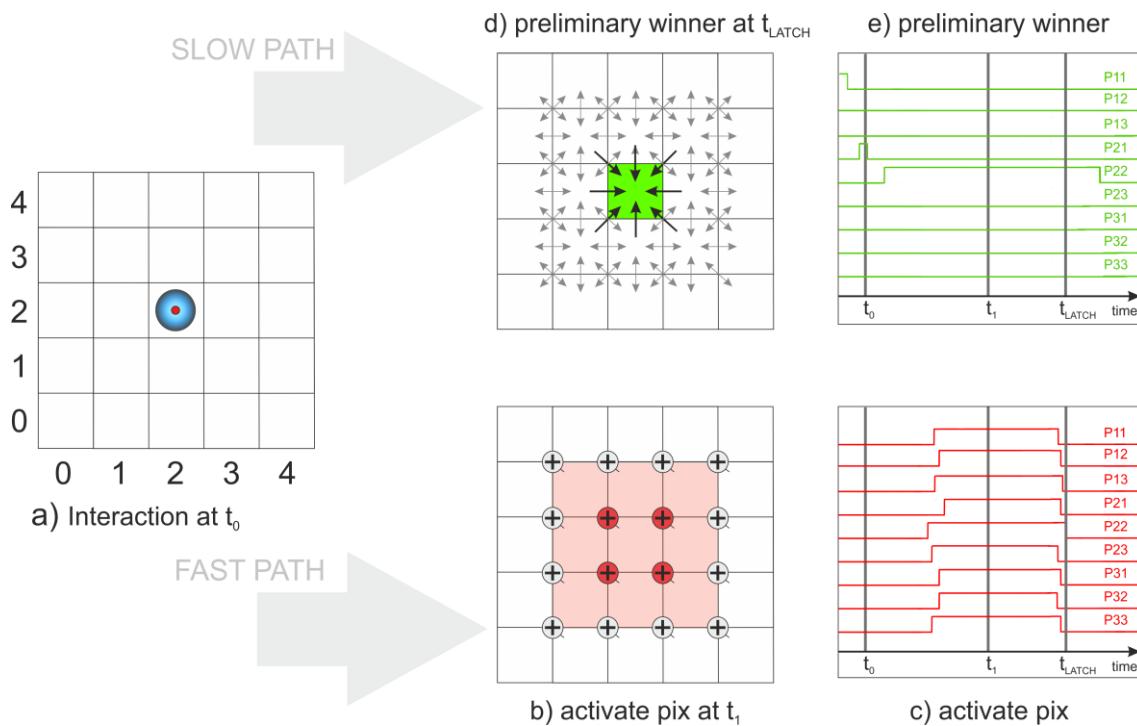


Fig. 2.12 The C8P1 concept when a photon hits the detector in the pixel centre. 100% electrons collected by the pixel P22.

In the case presented in Fig. 2.13, the charge is not evenly shared between pixels P22 and P32. Since the charge division is nearly equal, it is possible that more than nine pixels are activated, in the presence of noise and discriminator offsets, because the signals in the signal rebuild hubs constructed of the pixels P41, P42, P31, P32 and P42, P43, P32, P32 might also exceed the threshold. Most probably, the activated cluster would be the same as in Fig. 2.12, but in the worst case, twelve pixels are activated. The ‘activate pix’ signal is set for a longer period of time in pixels – P21, P22, P23, P31, P32, P33. However, only two signal rebuild hubs (marked in dark red in Fig. 2.13b) reconstruct fully the amplitude. As far as the slow path is concerned, the comparators may change their states before latching of the result, pointing even interchangeably at P22 or P32. Thus, if there is only a slight difference between the amount of collected charge, the algorithm most likely allocates the hit properly, however, due to the noise issues and = the comparator offsets it may allocate the hit to the neighbour pixel, but what is crucial, the event will not be missed.

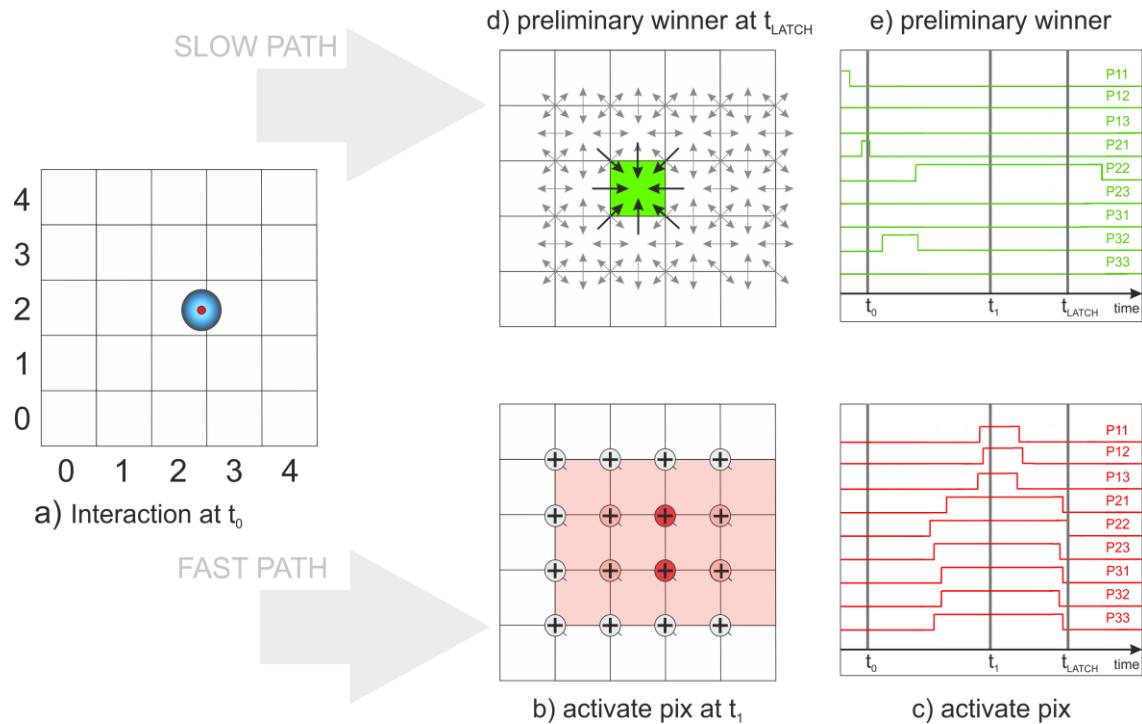


Fig. 2.13 The C8P1 concept when a photon hits the detector in between two pixels, and 70% and 30% of electrons are collected by the pixel P22 and P32, respectively.

In the case presented in Fig. 2.14, the charge is shared between pixels P22, P23, P32, P33. Most of the charge is collected by the pixel P22, therefore, only four surrounding P22 signal rebuild hubs receive the signal of the amplitude exceeding the threshold. The ‘activate pix’ signal is set for nine P11, P12, P13, P21, P22, P23, P31, P32, P33 pixels. However, it is set for the longer period of time only in four pixels P22, P23, P32, P33, since only one signal rebuild hub fully reconstructs the total amplitude (marked in dark red in Fig. 2.14b). When most of the charge is collected by one pixel, comparators indicate properly the preliminary winner pixel, even in presence of noise or offsets. The result indicating the pixel P22 to be a winner is latched on the negative edge of the ‘activate pix’ signal.

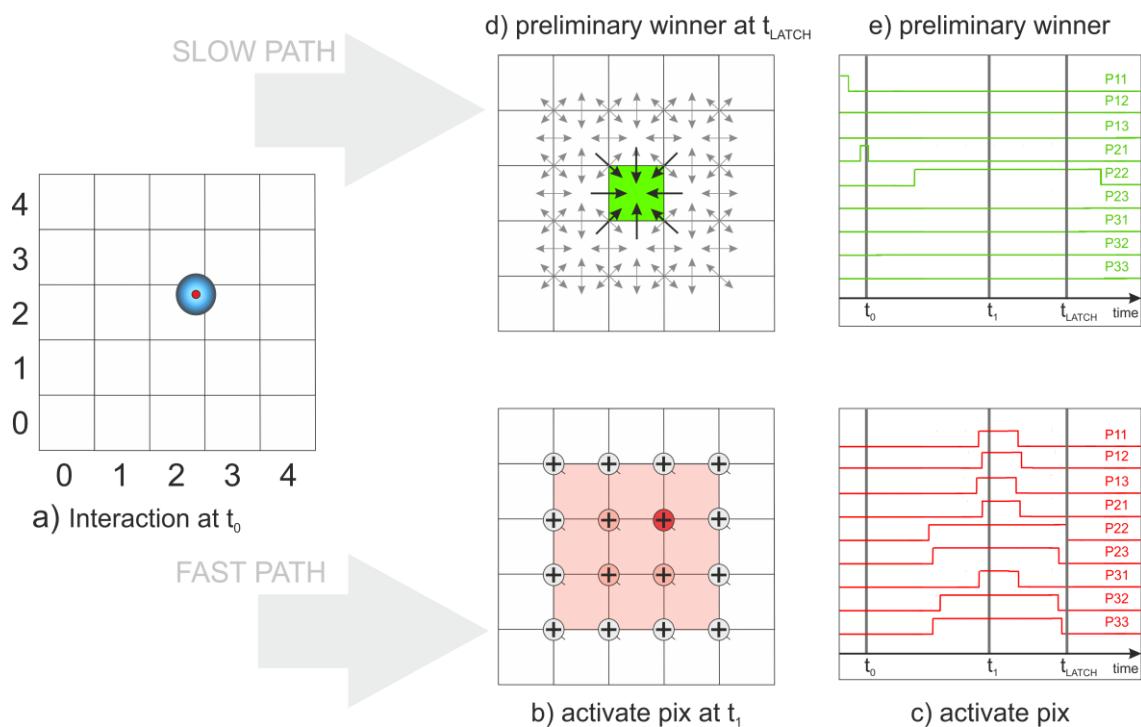


Fig. 2.14 The C8P1 concept when a photon hits the detector in between four pixels. 70%, 13%, 12% and 5% of electrons collected by the pixel P22, P32, P23 and P33 respectively.

2.4 Comparison of C8P1 and other existing solutions

In conclusion, comparing the C8P1 algorithm to the solutions presented by other researchers, the main differences are listed below:

- The signals are added in a signal rebuild hub in the voltage (not current) mode, this is preferred because duplication of currents requires current mirrors, necessary to feed signal rebuild hubs, which are the cause of additional mismatch (refer to Section 1.6.1 Mismatch)
- The comparison in the comparators block is performed exploiting the shaper-slow signals amplitudes, whereas in the other solutions, the comparison is based on exploiting the timing properties of the discriminator output signals, using the ToT technique. It was decided to compare amplitudes of the signals since such technique shows better performance [77], taking into account noise conditions.
- When a hit is registered, other pixels in the neighbourhood are not inhibited from registering another hit. The decision is made on the negative edge of the ‘activate pix’ signal, thus, it is important to provide the optimal size of a pixel neighbourhood cluster to avoid multiple hit registration for one photon interaction.

The aim of the research was to perform studies of algorithms dealing with charge sharing which can be implemented on a chip. Achieving this goal has been intended through simulations based on models of increasing fidelity with respect to the actual possible in-hardware implementations. However, on the basis of the literature descriptions of the aforementioned solutions, it has not been possible to determine how exactly the inter-pixel communication is realised and how and when the exchange of information between pixels is done in other solutions than the C8P1 algorithm. The C8P1 algorithm, developed as a proprietary solution by the AGH – Fermilab research collaboration, allowed building fully functional models and perform the detailed analysis. Thus, the next chapter is dedicated to the C8P1 simulations, specifically. However, general models prepared for simulations are believed to be easily adjustable to describe other solutions, if the details of such solutions are known.

3 SIMULATION APPROACH TO CHARGE SHARING COMPENSATION ALGORITHMS

One of the goals of this thesis is to develop and implement a systematic approach to simulations of a readout integrated circuit with an inter-pixel communication for an algorithm dealing with charge sharing. The execution time of the simulations on the transistor level for the whole matrix of pixels communicating with each other is often not acceptable. Therefore, the simulations on a high abstraction level are proposed, including static and dynamic modelling. The first technique allows verification of the algorithm concept, including tests of hit allocation and verification of detection efficiency. The solution is optimised for the simulation speed and does not take into account timing properties of the analog blocks. The next technique introduces the parameterised behavioural models of analog and digital blocks and takes into consideration signals changing in the time domain. It allows testing of the algorithm taking into account timing properties of the signals and noise analysis.

The aim of the simulations was to determine the differences in the number of hits detected in the SPC and C8P1 modes in the case of charge sharing and the influence of the analog parameters mismatch between channels and random noise on the detection performance. The next task was to optimise the threshold setting in the SPC and C8P1 modes taking into consideration the gain spread, the DC offset at the discriminator spread and the electronic noise. If the analog parameters spread and noise are minimised to the satisfactory level, the simulations are performed to prove that the total photon energy can be reconstructed from the fractional signals in the C8P1 mode in the case of charge sharing.

This chapter is dedicated to the development of the verification environment which allows testing the algorithm concept and guiding the ASIC implementation process through the parameter optimisation. The motivation, the tools and the implementation of readout channel models are introduced. The simulations allowed prediction of the detection system behaviour in the case of charge sharing and comparison of a detector with and without the C8P1 algorithm.

3.1 Analytical approach towards modelling of readout channel

The analytical approach in modelling the noise registrations in physical devices has been already introduced by Rice in 1944 [79]. In Rice's work, the noise due to the shot effect is studied for the linear physical devices, for which mean and standard deviations are given by Campbell's theorem. The models dedicated in particular to a single photon counting pixel system have also been a subject of research. To evaluate the implications of small pixel dimensions in detector systems, models introducing charge sharing are studied for example in [80], [81].

From the viewpoint of the detector performance, an interesting question is raised: how the real detector behaves taking into account the analog parameters mismatch and the random noise. The signals in the pixel matrix for the detector working in the SPC mode are subject to the DC offset spread, gains spread and random electronic noise. These factors can be taken into account by introducing the additive and multiplicative noise sources to a readout channel model presented schematically in Fig. 3.1. In the simplest approach, namely, in static modelling, timing properties of the analog blocks are neglected, thus, the signals analysis is reduced to the analysis of signal magnitudes. In this approach, the algorithm output is determined considering only 'snapshots' of the signals, meaning the frozen temporary state of the input parameters. Then, noise sources can be treated mathematically as random variables. On the basis of the experimental results as well as on the literature research, the variables can be treated as normally distributed, which can be denoted by Eq. 3.1-3.3.

$$X_i \sim N(0, \sigma_{Xi}) \quad \text{Eq. 3.1}$$

$$Y_i \sim N(\mu_{Yi}, \sigma_{Yi}) \quad \text{Eq. 3.2}$$

$$Z_i \sim N(\mu_{Zi}, \sigma_{Zi}) \quad \text{Eq. 3.3}$$

where, X_i is the random variable representing the electronic noise in i -th pixel with zero mean and σ_{Xi} standard deviation, Y_i is the random variable representing the readout channel gain in i -th pixel with μ_{Yi} mean and σ_{Yi} standard deviation, Z_i is the random variable representing the DC offset at the discriminator

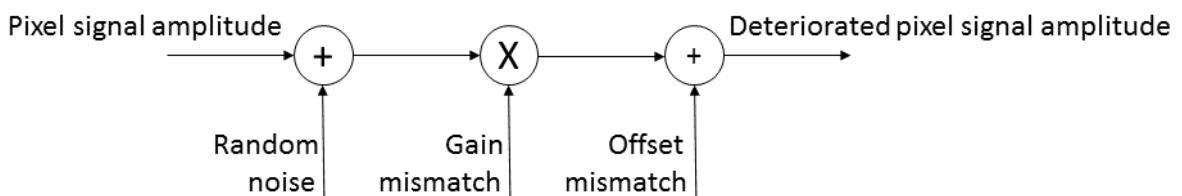


Fig. 3.1 A schematic diagram introducing noise sources in the static model.

in i-th pixel with μ_{zi} mean and σ_{zi} standard deviation. It should be noted that if the assumption is made that for each temporal signal sample, X has a normal distribution with a zero mean, the noise signal is treated as Gaussian white noise.

Eq. 1.17 describes the number of counts measured by the detector as a function of the threshold voltage. If all of the parameters N_0 , V_0 , $2\Delta l$, x_0 , and σ_t were known, it would be possible to predict the optimal threshold for the detector operation. The N_0 , V_0 , $2\Delta l$, x_0 values can be extracted from the detector model, however, in the known publications [44], [80], the σ_t is typically treated as a cumulative fluctuation factor including the Fano factor, noise and DC offset dispersion. To solve the problem of threshold setting analytically, with regard to gain and offset dispersion and noise, the contribution of each aforementioned factor to a cumulative factor representing each readout channel signal distortions should be considered.

The signal induced in a detector in the static model can be treated as a one-dimensional variable dependent on the photon energy. The signal distortions related to Fano factor for a considered silicon sensor are negligible in comparison to the mismatch and noise, therefore they were not considered in the model. To calculate the joint distribution of the three random variables X_i , Y_i , Z_i , the sum of the random variable Z_i , and product of the two Y_i, X_i , random variables need to be calculated. Firstly, only a single channel is considered, thus, for the simplicity of the notation, the random variables are denoted without 'i' index. In mathematical terms, the joint distribution is to be found. Following the formula from [82], the distribution of the product of the two independent Gaussian random variables Y and X is given by Eq. 3.4.

$$f_{YX}(x) = \exp\left(-\frac{\mu_Y^2}{2\sigma_Y^2} - \frac{\mu_X^2}{2\sigma_X^2}\right) \times \sum_{n=0}^{\infty} \sum_{m=0}^{2n} \left(\frac{2n}{m}\right) \frac{\mu_Y^m \mu_X^{2n-m} x^{2n-m} |x|^{m-n}}{\pi(2n)! \sigma_Y^{n+m+1} \sigma_X^{3n-m+1}} K_{m-n}\left(\frac{|x|}{\sigma_X \sigma_Y}\right) \quad \text{Eq. 3.4}$$

Where $K_v(\cdot)$ is the modified Bessel function of the second kind and order v, given by Eq. 3.5 [83].

$$K_v(z) = \frac{\pi}{2} \frac{I_{-v}(z) - I_v(z)}{\sin(v\pi)} \quad \text{Eq. 3.5}$$

Where $I_v(\cdot)$ is the modified Bessel function of the first kind and order v, and can be computed with Eq. 3.6.

$$I_v(z) = \left(\frac{1}{2}z\right)^v \sum_{k=0}^{\infty} \frac{\left(\frac{1}{4}z^2\right)^k}{k! \Gamma(v+k+1)} \quad \text{Eq. 3.6}$$

Where $\Gamma(\cdot)$ is the gamma function given by Eq. 3.7.

$$\Gamma(n) = (n-1)! \quad \text{Eq. 3.7}$$

Assuming that the electronic noise is white Gaussian noise, $\mu_X = 0$ can be substituted into Eq. 3.4. The formula can be simplified to Eq. 3.8, noticing that, in the sum, only the terms for which $m = 2n$ remain.

$$f_{YX}(x) = \exp\left(-\frac{\mu_Y^2}{2\sigma_Y^2}\right) \times \sum_{n=0}^{\infty} \frac{\mu_Y^{2n} |x|^n}{\pi(2n)! \sigma_Y^{n+1} \sigma_X^{n+1}} K_n\left(\frac{|x|}{\sigma_X \sigma_Y}\right) \quad \text{Eq. 3.8}$$

Even after simplification, based on Eq. 3.8, it can be shown that there is no analytical expression for the probability density function of the product of two normal random variables Y and X [84]. Thus, if it is needed, the probability density functions should be calculated numerically in this case. Calculating the joint distribution of the Y and X random variables was the first step to estimate the parameters of the joint distribution taking into account the gain and offset dispersion and the noise. However, the resulting distribution is neither normal, nor it can be derived analytically.

The problem is impossible to be solved analytically, because many coupled degrees of freedom coexist in the signal processing path and moreover, the inter-pixel communication is implemented which additionally complicates the signal processing. Therefore, Monte Carlo methods are considered as a good alternative to study the effects of mismatches of analog parameters in the readout channels. It is important to simplify the transistor models at a higher abstraction level to optimise the simulation speed. Maintaining the desired precision and the desired level of detail, is equally important. Therefore, two behavioural macro-models used in Monte Carlo simulations to verify the C8P1 algorithm are presented in the following sections.

3.2 Static model of detector

3.2.1 Model implementation for Monte Carlo simulations

The static model of a readout channels matrix introduces the simplified idea of the C8P1 algorithm shown in Fig. 2.6. LabVIEW is used as the calculation environment. The simulation procedure can be broken down into the steps presented in Fig. 3.2. Firstly, the input simulation parameters, such as a sensor thickness and material, a bias voltage, a pixel matrix size and a simulation resolution, are defined. Secondly, a charge cloud is numerically represented according to the Gaussian model introduced in Section 1.5.2 for a photon of a given energy. Then, the simulation steps are repeated for different photon interaction

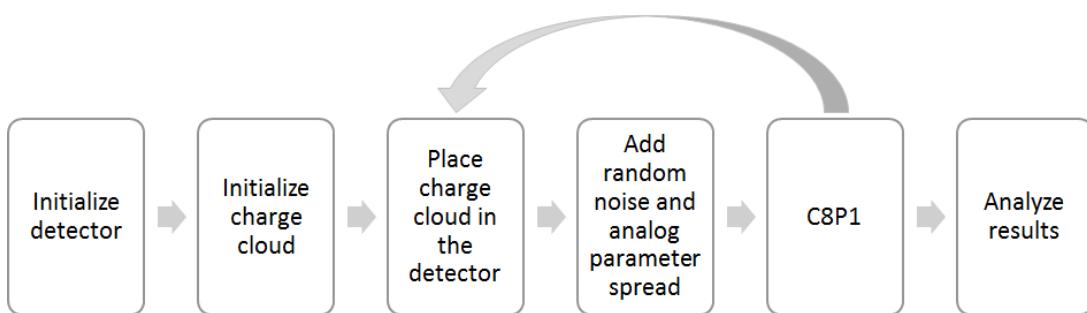


Fig. 3.2 The static simulation steps.

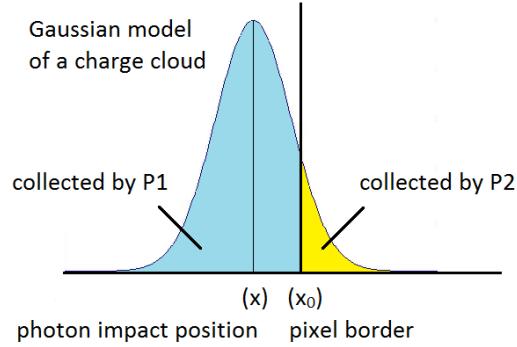


Fig. 3.3 The concept of charge collection by neighbouring pixels implemented in simulations.

locations, that vary randomly or according to a specific pattern. Placing the charge cloud in the detector is realized by integrating the two dimensional Gaussian function on 2D space intervals determined by pixel sizes. This idea in the one dimensional case is presented in Fig. 3.3. In this example, the photon impact position $x < x_0$, which means that the interaction occurs in the pixel P1 and the pixel P1 collects most of the charge.

The implementation of the C8P1 algorithm in this approach is simplified to operation on the maximum amplitudes of the signals from the slow and the fast paths. The algorithm in its nutshell covers summing fractional values from four neighbouring pixels, sum discrimination and comparison between each pixel with its eight neighbours. No timing properties of the analog blocks are considered. The same procedure can be repeated as a parametric scan. Noise, analog parameters spread, interaction position or threshold value can be defined as variables.

The simulations allow verification of the following issues, both in the SPC and C8P1 modes for the certain photon interaction position, the analog parameters spread, the noise and the threshold settings:

- is a hit allocated to the proper pixel where the photon interaction takes place?
- how many hits are detected, how many hits are missed and how many extra hits are counted?

3.2.2 Simulation results

One of the first goals of the simulations was to compare the detection efficiency for the standard readout channel parameters in the SPC and C8P1 modes. To perform simulations as close as possible to the physical representation of the detector, the parameters of a typical detector system, presented in Table 3.1, were set. The pixel pitch, the photon energy and the charge cloud σ were chosen to reflect the parameters of the detection set-up consisting of the Chase Jr. chip working under the nominal

conditions. The region of interest (ROI) size was chosen to include borders between the pixels to observe the detector behaviour in the case of charge sharing.

The pixel matrix size was set to 6 x 6 pixels of the size of 100 μm x 100 μm , out of which the region of interest, covering the area of 250 μm x 250 μm was chosen in the middle of the pixel matrix to avoid border effects. The charge cloud was simulated with $\sigma_{\text{cloud}} = 10 \mu\text{m}$. The σ_{cloud} can be found from Eq. 1.13 or estimated from the experimental results. The charge cloud spread estimated from the analytical approach for $T = 300 \text{ K}$, detector thickness $d = 320 \mu\text{m}$, bias voltage $V = 120 \text{ V}$ and $kt/q = 0.02586 \text{ V}$ resulted in $\sigma_{\text{cloud}} = 6.6 \mu\text{m}$. The estimation was consistent with the experimental results, where the entire region affected by charge sharing was measured to be about 20 μm wide [85]. Assuming Gaussian charge distribution and the fact that there is no charge sharing between channels if more than 99.7% of charge is collected by one channel, the estimated $\sigma_{\text{cloud}} \approx 20/3 \mu\text{m}$. For thicker sensors that can be used for higher X-Ray detection efficiency, the charge sharing affects larger areas, since the σ_{cloud} is larger, therefore, the $\sigma_{\text{cloud}} = 10 \mu\text{m}$ is considered in the model as a good average value.

The readout channel parameters spread was included in the first model (Test variant 1), reflecting the values measured in the experiments. The gain spread, defined as the standard deviation to the mean gain ratio was set to 5%, the electronic noise $\text{ENC} = 100 \text{ e}$, the DC offset spread at the discriminators was set to $\sigma = 40 \text{ e}$. Typically, for detection systems working in the SPC mode, the global threshold is set in the middle between the average noise level \bar{V}_{noise} and \bar{V}_0 . The \bar{V}_0 value is the mean threshold voltage corresponding to the total photon energy. Therefore for 8 keV photons, the threshold was initially set to 4 keV.

To explore the charge sharing effect dependency on the photon impact position, the charge cloud was simulated in the locations in the detector which were restricted to the chosen ROI. For each location, 1,000 hits were simulated. The areas of pixel edges were scanned with a 1 μm resolution at the pixel borders and with a 4 μm resolution in the central pixel areas to optimise the execution time of the simulations. The total number of counts registered in each location by the simulated detector was plotted as a function of the photon position, resulting in a map of counts. This idea of the ROI scan was a simulation of the pencil beam test, carried out on the real detector later.

The first simulation results presented in Fig. 3.4a and b show the maps of counts for the detector working in the SPC and C8P1 modes, respectively. In the C8P1 mode, the border between pixels cannot be recognised, which means that the detector counts photons properly even in the case of charge sharing. For the SPC mode, though, the errors in registration on the pixel edges are clearly visible. There are additional counts registered at the border between two pixels and counts are lost in the pixel corners.

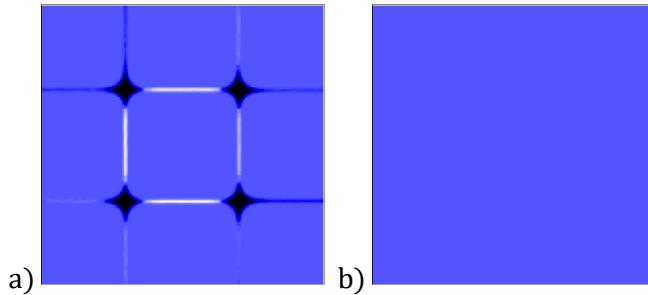


Fig. 3.4 The map of counts for the scan of the $250 \mu\text{m} \times 250 \mu\text{m}$ ROI obtained in simulations of a detector working a) in the SPC mode b) in the C8P1 mode for the 8 keV photon energy and the 4 keV threshold setting.

The mean number of detected hits in the SPC mode is $n = 1,002.03$, $\sigma = 11.36$, while, in the C8P1 mode, it is $n = 1,000.66$, $\sigma = 0.89$. These numbers are rather close for both operation modes. Therefore, another figure of merit should be defined to compare quantitatively the two maps of counts. The definition of the proposed quality factor Q is given by Eq. 3.9.

$$Q = \begin{cases} 0, & \text{for } n = 0 \\ \frac{|n-\sigma|}{n} \cdot \frac{p}{p_{\text{tot}}}, & \text{otherwise} \end{cases} \quad \text{Eq. 3.9}$$

where n is the mean number of detected hits, σ is the standard deviation of the number of detected hits, p is the number of pixels in which the number of counts falls in the range [900; 1100], p_{tot} is the total number of pixels in the ROI. The quality of the imaging is defined by the absence of the pixel border effects and by the uniform registration in all the pixels. The pixel border effects influence mostly the $\frac{p}{p_{\text{tot}}}$ factor, which decreases for extra or lost counts. If pixels register different number of hits, for example due to the gain or offset spread, the $\frac{|n-\sigma|}{n}$ is deteriorated by the larger σ . In the ideal detector, 1,000 hits are registered irrespectively of an interaction position and $Q = 1$. The Q factor is used to evaluate the simulated detector performance in the presence of random noise and analog parameters spread. The quality factor Q , calculated for the typical maps presented in Fig. 3.4, equals $Q = 0.866$ and $Q = 0.999$, for the SPC and C8P1 modes respectively. It suggests that C8P1 allows nearly ideal registration for typical detector parameters and the threshold set to a half of the photon energy.

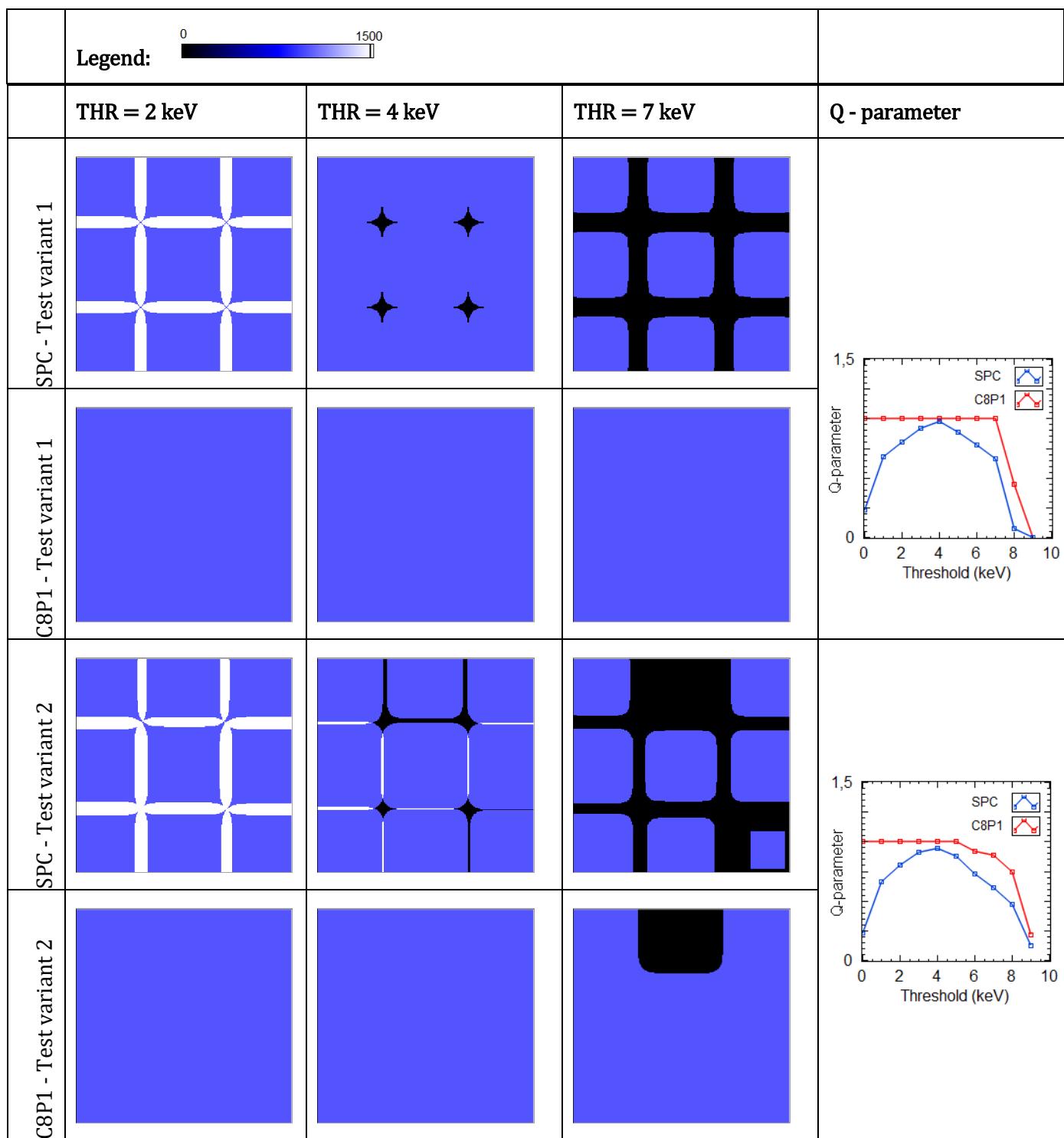
The presented model involves typical DC offset spread, gain spread and random noise. To study how the analog parameters mismatch between the channels and the random noise influence the detection performance, and especially, to discover how these parameters affect the registration at the pixel borders, the models with the parameters listed in Table 3.1 were used in simulations. For each set of the readout channel parameters, threshold was changed within a range [0; 9] keV with the 1 keV step.

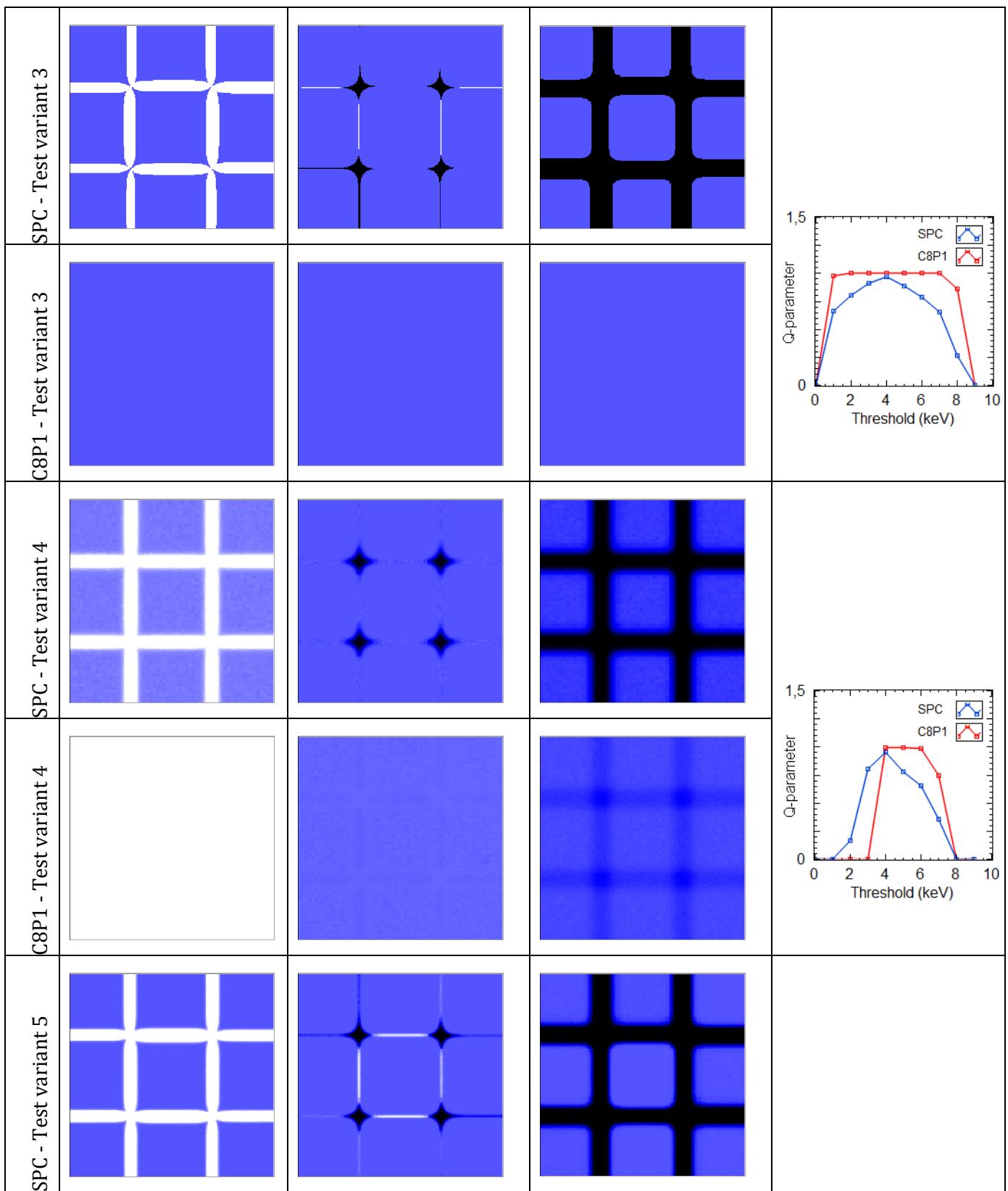
The simulation results, including the maps of counts and plots of the Q-parameter dependencies on the threshold setting for all the test variants listed in Table 3.1, are presented in Fig. 3.5. The test variant 1 refers to the ideal detector with no mismatch and noise. The test variants from 2 to 4 show the detector behaviours for which only one of the parameters: gain, DC offsets or noise was randomly deteriorated to observe the individual parameter contribution to the registration quality. In the test variant 5 and the test variant 6 a model of the typical detector and the detector with large gain and DC offset spread and noise are simulated to verify the need of the detector parameter optimisation in order to improve detection efficiency.

Table 3.1. Input parameters for the static detector model.

Sensor type	Photon energy	Charge cloud σ	Pixel array	Pixel pitch	ROI size
Si	8 keV	10 μm	6 x 6	100 x 100 μm^2	250 x 250 μm^2

Test variant	Threshold	Gain spread	DC offset	ENC
1	0-9 keV	0	0	0
2	0-9 keV	20%	0	0
3	0-9 keV	0	100 e ⁻	0
4	0-9 keV	0	0	200 e ⁻
5	0-9 keV	5%	40 e ⁻	100 e ⁻
6	0-9 keV	20%	100 e ⁻	200 e ⁻





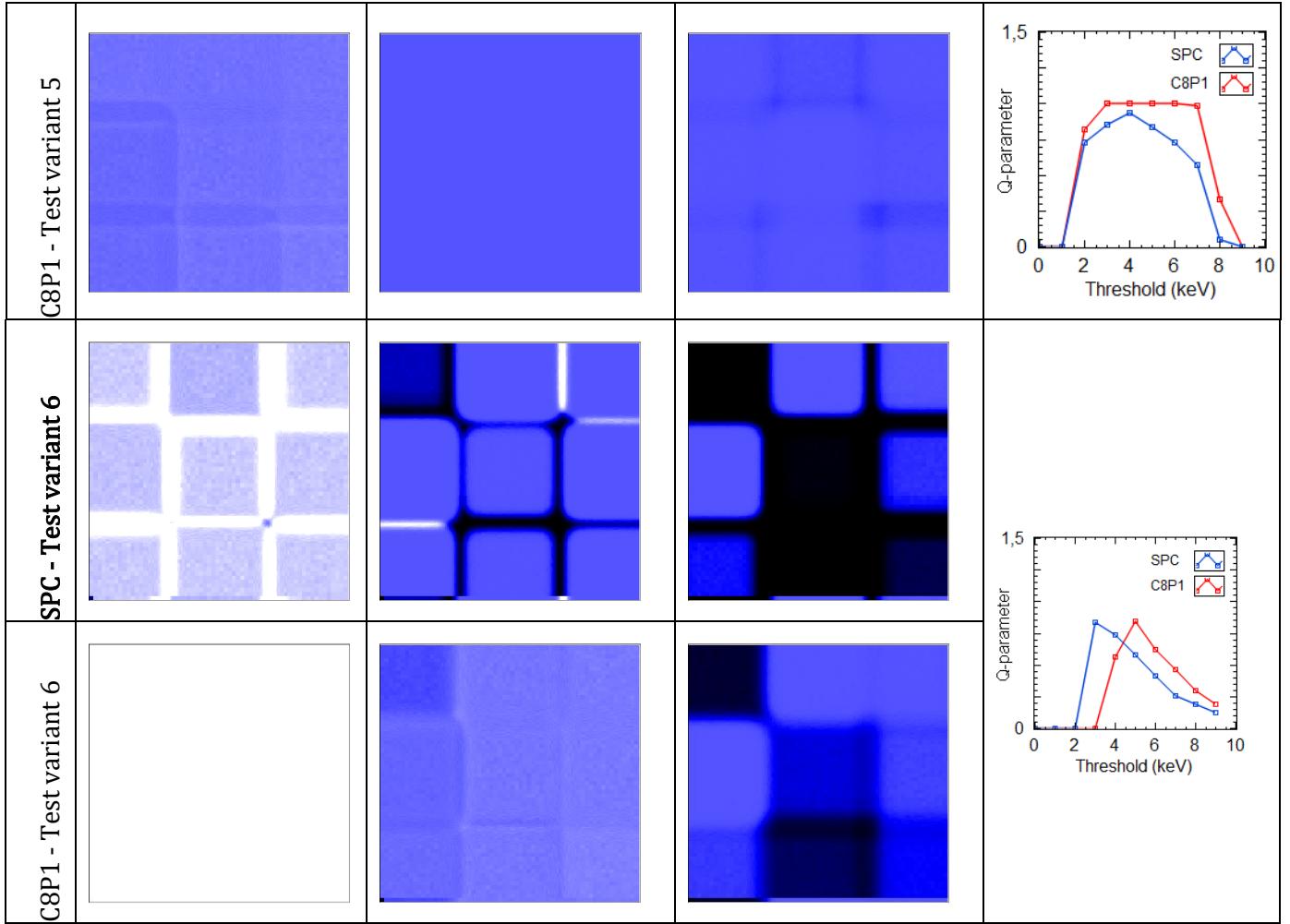


Fig. 3.5 The maps of counts for the scan of the $250 \mu\text{m} \times 250 \mu\text{m}$ ROI for the test variants listed in Table 3.1.

The first conclusion based on the Q-parameter plots is that the threshold equal to 4 keV is the optimal setting for the detector working in the SPC mode. It should be noted however, that even for the optimal threshold setting and the ideal detector model tested in ‘Test variant 1’, the parameter Q is always less than 1. It means that errors in the number of counts due to charge sharing are inevitable in the SPC approach, whereas $Q \approx 1$ is obtained in a noticeably wider threshold range for the detector working in the C8P1 mode. The exact optimal threshold range is dependent on the gain spread, DC offset spread and noise.

The general observation from all the simulation results is that for the threshold values lower than the half of the photon energy, the additional counts are registered at the pixel borders in the SPC mode, which are marked as the white borders. It is due to the fact that the charge is shared between pixels and two events instead of one are counted in the neighbouring pixels. A detector working in the C8P1 mode is not a subject to this problem, since the fractional signals are added. For the threshold values higher than

the half of the photon energy, the counts are lost at the pixel borders in the SPC mode, which is marked as black areas. This happens because the fractional signals do not exceed the threshold in the case of charge sharing. In the C8P1 mode, the hits are not lost below the 7 keV threshold unless the pixel exhibits extremely low offset, low gain or large ENC. For instance, the middle pixel in the upper row in ‘Test variant 2’ has its gain 30% lower than the nominal gain value. In the C8P1 mode, this pixel contributes to the sum in the SRH, degrading the total signal amplitude. The analogous behaviour can be seen for the low DC offset values. However, in ‘Test variant 3’, it is not present for the 7 keV threshold, since randomly chosen offset values for each pixel in the ROI resulted in the initial signal decreased by not more than 5%.

The noise deteriorates the detector performance in a similar manner in the SPC and C8P1 mode, which is visible in ‘Test variant 4’. It affects both pixel edges and pixel centres, resulting in a variation of the total number of counts. The Q parameter never reaches 1 in both operation modes, however, for the thresholds set to the half of the photon energy and above, Q is higher for the C8P1 mode. Interestingly, for low threshold values, a detector with the C8P1 algorithm registers additional counts irrespectively of the photon position. This can be explained by the fact that the signal with the noise is added from four neighbouring pixels in the C8P1 algorithm. Therefore, the signal on which the discrimination is performed has a larger standard deviation in the C8P1 mode than in the SPC case.

The comparison of the two tests variants, 5 and 6, of a detector with the typical and large parameter spread, shows that, even though the perfect registration with $Q = 1$ is not possible in the presence of noise for any threshold, the noise and parameter spread optimisation is a crucial issue in the detector design. A 20% gain spread, 5% DC offset spread, and signal to noise ratio at the level of 11 result in the significant degradation of the detection efficiency and the maximum quality factor obtained is $Q = 0.84$ for the C8P1 mode. This suggests that the dedicated correction circuits should be implemented in order to minimise the analog parameters spread between the channels for the proper operation of the detector.

The simulations were performed only for several threshold settings to observe the trend and to optimise the simulations time. Another test, using the static modelling approach, was performed for the typical detector settings to study the fractional signal reconstruction. The threshold was varied from 1 to 15 keV, and interaction locations, denoted as (x,y) , where x were changed within the range from $-50 \mu\text{m}$ to $50 \mu\text{m}$ with a $0.5 \mu\text{m}$ step, while y was kept constant, to emulate a pencil beam moving from one pixel to its neighbour. The simulation idea of an X-ray beam movement from the pixel P1 to the pixel P2 along the axis parallel to the pixels’ edge, is presented in Fig. 3.6. For each position threshold scans were calculated.

The simulation results are presented in Fig. 3.7a and b, in the SPC and the C8P1 mode, respectively. When the photon impact position is close to the pixel border, denoted as $x \approx 0$, the charge is divided between pixels P1 and P2. The blue counts are those measured by the P1 pixel, and the orange ones by the P2 pixel. In the SPC mode both pixels P1 and P2 register 10,000 counts for the pixel border and for low threshold values about 1.2 V. However, for the higher threshold values above 4 keV, the number of counts drops down to 0 in both pixels. Thus, if a hit occurs near the pixel border, either both or none of the pixels may register such an event, depending on the threshold setting. As it is shown in the previous simulations, the threshold equal to 4 keV is the optimal setting for the SPC mode at the pixel border, to minimise extra and lost counts. In the C8P1 mode, the orange and the blue surfaces do not overlap, which means that each hit is assigned to only one pixel each time by the C8P1 algorithm. When the pulse amplitudes in the SPC mode are compared with the pulse amplitudes in the C8P1 mode for $x_0 = -50 \mu\text{m}$ or $x_0 = 50 \mu\text{m}$, it can be also

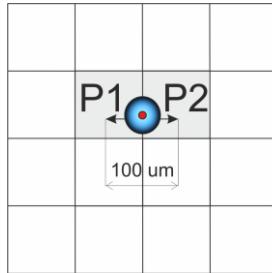


Fig. 3.6 The measurement conditions when the pulse injection circuitry injects two different calibration pulses into neighbouring pixels P1 and P2 emulating X-ray beam movement along the horizontal axis.

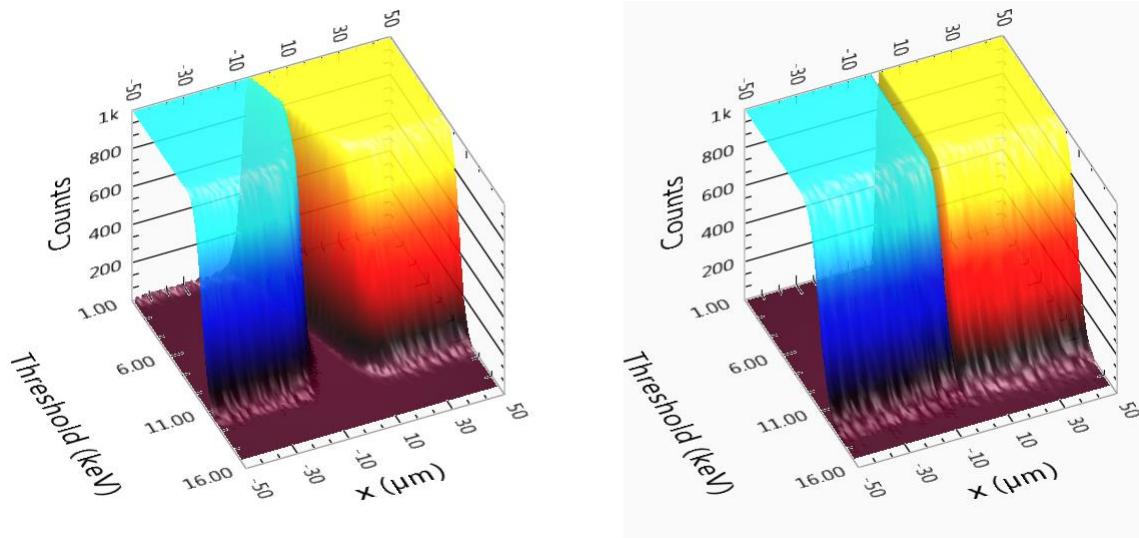


Fig. 3.7 The number of counts versus threshold and distance from the pixel border in a) the SPC mode b) the C8P1 mode. Pixel P1 is represented with blue and P2 with orange colour.

observed that the total signal amplitude is recovered in the C8P1 mode, irrespectively of the simulated beam position.

The analysis using a static model can be extended to study the dependency of potential mistakes in registration, such as counting extra hits or not registering counts, on the photon energy. Simulation was performed for the detector parameters given in ‘Test variant 5’, the photon energy varied from 4 to 12 keV and the photon interaction position was randomly chosen. If more than one hit was counted in the detector, the rest of the hits were treated as extra hits, whereas, if no hit was detected, it was treated as a count loss. The results presented in Fig. 3.8a and b present a number of errors that occurred for 10,000 simulated random interactions, in the SPC and C8P1 modes, respectively. The extra hits counted are marked in yellow, and the hits lost are marked in blue.

The results show that the optimal threshold (marked dark) for the SPC mode changes from 2 keV to 6 keV for the photon energies varying from 4 keV to 12 keV. However, finding the optimal threshold does not guarantee an errorless registration. In fact, the yellow and blue plots overlap, which suggests that some counts will be lost or counted multiple times in any case. In the C8P1 mode, the optimum threshold is not restricted to a single point, and the higher the photon energy, the wider the range of optimal threshold setting. For instance, if the photon energy is equal to 6 keV, the optimal threshold range for which no more than 0.1% mistakes occur is 1 keV wide, while for a 12 keV photon it is 6 keV wide.

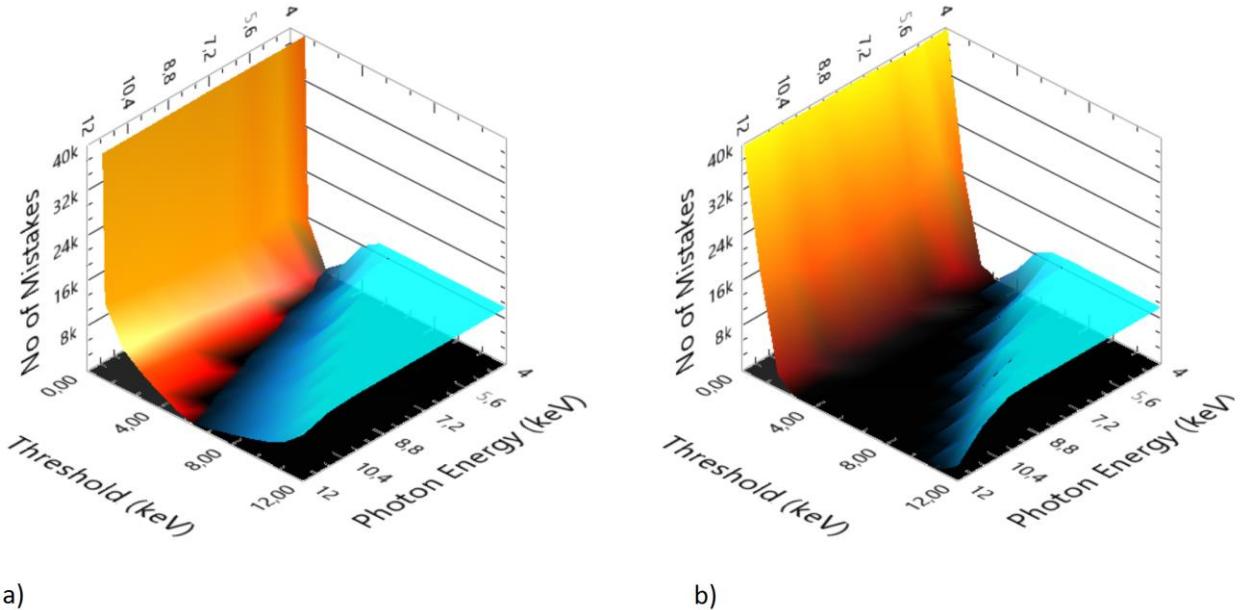


Fig. 3.8 The number of mistakes, namely, the extra hits counted marked in yellow, and the hits lost marked in blue in the a) SPC mode, b) C8P1 mode.

The conclusion from all the static simulations is that the exact range of proper threshold setting cannot be calculated analytically. Prediction of the optimal threshold requires simulations for typical detector parameters to obtain, first, a rough estimation and, then, performing experimental analysis is needed to increase the accuracy. For each detector module, the threshold scans can be performed to determine the pixel with the lowest extracted energy peak V_0 and the highest noise peak V_{noise} . Then, the values of $V_{noise} + k\sigma_{noise}$ and $V_0 - k\sigma_{noise}$ can be treated as the optimal threshold range for the chip operating in the C8P1 mode, where $k = 3$ up to $k = 5$ is used in practice [56].

In the case of large mismatch and noise, lossless registration cannot be achieved even in the C8P1 mode. There are two types of errors identified in these simulations occurring for a detector working in the C8P1 mode. Namely, there are the additionally counted hits (due to noise) and counts loss (due to low pixel gain or DC offset, or large noise). Therefore, there is a need for implementation of correction circuits and development of procedures in order to compensate for the readout channel analog parameter mismatch.

3.3 Dynamic model of readout channel

3.3.1 Model implementation

The static simulations did not take into account timing properties of the readout channel. Therefore, revealing time-related aspects, the dynamic simulation should be performed to study the algorithm more extensively. The behavioural model of the readout channel for dynamic simulations was implemented in the Cadence® Virtuoso® environment to study in particular the C8P1 algorithm. Nevertheless, the model was built with the parameterised functional blocks, to allow easy adjustments to other versions of the charge sharing compensation algorithms. Building the model on the high abstraction level served for the optimisation of the simulation execution time. However, it should be noted, that the execution time is significantly longer in the dynamic approach. For instance, a single threshold scan takes 100,000 times longer in the dynamic approach than in the static one. Therefore, the dynamic approach is used only to study time-related issues that cannot be modelled in the static approach.

The readout channel was modelled with the circuit shown in Fig. 3.9. Both SH SLOW and SH FAST were implemented as the second order quasi-Gaussian CR-RC filters. The transfer functions of the shapers and the CSA were calculated to reflect the parameters of the common blocks used in the standard readout channel architecture. The realistic models of comparators and discriminators, implemented in Verilog-A were used. The C8P1 block was implemented in the System Verilog. The input noise sources were represented as a parallel noise current source $\overline{I_n^2}$ and a serial noise voltage source $\overline{V_n^2}$ according to [33].

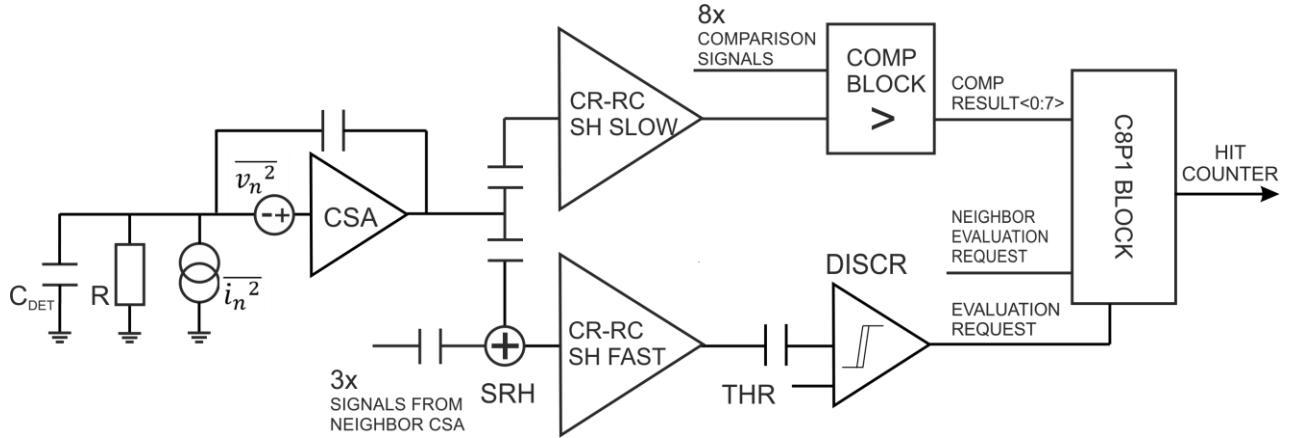


Fig. 3.9 The simplified readout channel architecture with the C8P1 algorithm for dynamic simulations.

The noise sources were effectively lumped noise contributions and they were chosen to reflect a typically expected signal-to-noise ratio at the output. The contribution of the feedback resistor in the CSA was neglected.

3.3.2 Simulation results

The pixel matrix size was set to 7 x 7 pixels, no gain spread and no DC offset spread was assumed. A signal corresponding to the charge generated in a photon interaction can be injected to each pixel, emulating charge sharing. If no signal is injected to the pixels, and a parametric analysis is performed with varying threshold, noise peaks can be observed in threshold scans. When the front-end output is connected to the discriminator, and the threshold is set to the voltage equivalent to the front-end baseline, the frequency of the baseline crossing can be described by the Rice formula [79] in mathematical terms. Another important result given by Rice is the dependency of the frequency of the noise hits on the threshold voltage, shown in Eq. 3.10.

$$f_n = \frac{1}{2} f_{n0} \exp\left(\frac{-V_{th}^2}{2V_{noise}^2}\right) \quad \text{Eq. 3.10}$$

where f_n is the frequency of the noise hits, f_{n0} is the frequency of the baseline crossing, V_{th} is the threshold voltage, V_{noise} is the threshold given in the reference to the baseline. For the purpose of parameters extraction, described in Section 1.5.6, a noise peak can be approximated with a Gaussian function. The simulated noise peaks obtained for the SPC and C8P1 modes are presented in Fig. 3.10. It can be observed that the noise peak in the C8P1 mode is shifted with respect to the SPC mode. Moreover, the noise peak sigma is larger and the maximum number of counts is lower for the C8P1 mode. The larger noise peak sigma is caused by the fact that the discrimination is performed on the added signals from four individual

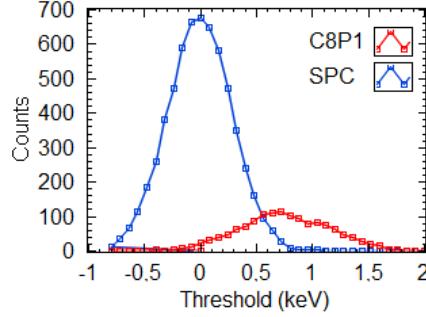


Fig. 3.10 The noise peaks registered in dynamic simulations in the SPC and C8P1 modes.

channels. The noise peak shift towards higher energies and the lower number of counts are also related to the principle of operation of the C8P1 algorithm. Firstly, only one pixel in a group of activated pixels can register a hit during one evaluation phase and all other pixels are blocked from registration additional noise counts in the C8P1 mode. Moreover, not only the threshold has to be exceeded by the signal, but also eight comparators have to indicate the pixel as a winner. If V_{th} is set to the baseline value, obviously the maximum number of counts is obtained in the SPC mode, since the signal is Gaussian white noise with zero mean. However, in the C8P1 mode, if a SRH signal sample is slightly above zero threshold, even if the condition of the zero-crossing is fulfilled, it is not likely that the individual pixel signal exceeds the eight neighbouring signals at the moment of comparison. That is why the noise peak is shifted and less events are counted. The conclusion from these observations is that the noise peak measured in the C8P1 mode cannot be used to estimate the parameters such as the readout channel gain. The parameters estimation for each readout channel should be performed when the detector operates in the SPC mode.

To assess the simulation model, the simulations were performed for the two scenarios presented in Fig. 3.11 a) the photons hitting a detector in the central pixel area and b) the photons hitting a detector at the border between two pixels. The results of the simulations for the dynamic model, correspond to the results for the static model (refer to Fig. 3.7). However, due to the long execution time of the dynamic simulations, the simulations were performed only for the two chosen photon interaction positions, which were identified in the static simulations as potentially prone to errors. In Fig. 3.11, the noise peak shift is visible, as expected. The signal amplitudes in both modes (calculated for the C8P1 mode, using the noise peak estimation from the SPC mode) are comparable. In the case of the charge sharing presented in Fig. 3.11b, the total signal is recovered from fractional signals in the C8P1 mode, and only one pixel P1 registers a hit. In the SPC mode, the fractional signals are visible.

The dynamic simulations allow studying the timing properties of analog blocks. For instance, the comparators switching can be observed. It was shown in Section 3.2 that the errors in photon

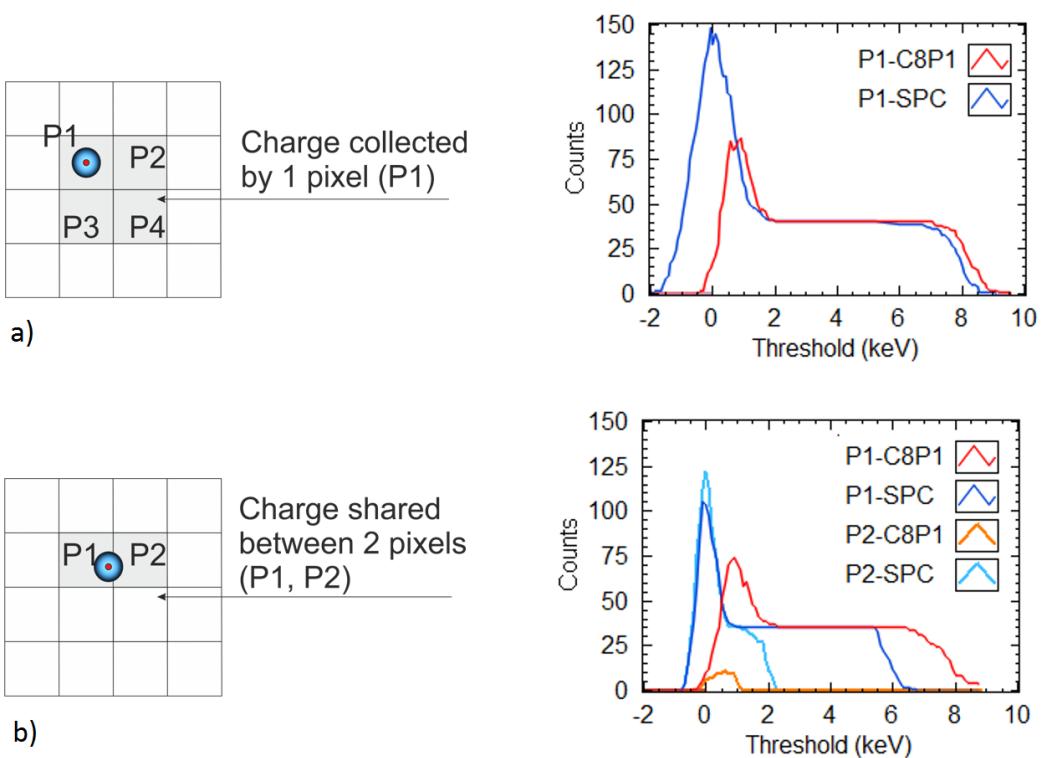


Fig. 3.11 The test scenarios and threshold scans registered in the dynamic simulations in the SPC and C8P1 modes for photon interactions a) in the central pixel area, b) at the border between two pixels.

registration may occur in the C8P1 mode at the pixel borders, due to noise or large analog parameters spread between channels. The question rises whether there are any other time related mechanisms causing errors which cannot be revealed in the static simulations. In the scenario when the charge is equally shared between two pixels, in the most common case, the events are registered interchangeably by pixels P1 and P2 in the C8P1 mode due to noise. This is the expected behaviour which corresponds with the results from the static model. However, an alternative scenario, is also possible. On the negative edge of ‘activate pix’ signal, the event is latched in P1 and just after, the ‘activate pix’ signal in P2 results in latching the preliminary winner again. If the comparator between these two pixels returns to the initial state and switches its state between two events latching, two pixels register the events caused by one photon interaction. This mechanism may cause multiple counts registration at the pixel borders.

3.4 Conclusions on static and dynamic modelling

Monte Carlo methods were used to study the effects of noise and mismatches of the analog parameters in the readout channels. The readout channel model was simplified to the static and dynamic models to assess the C8P1 performance. The static approach has an advantage of significantly better time performance, therefore, the tests requiring performing multiple threshold scans can be performed using

this model. However, to study the effects of the timing properties of the readout channel analog blocks, the dynamic model was introduced. The simulation approaches were described also in [78], [85].

It was observed that optimal registration is obtained in the SPC mode for the threshold equal to the half of the photon energy. However, additional counts are registered or the counts are lost at the pixel borders in the SPC mode, irrespectively of the threshold settings. The C8P1 mode solves this problem, since fractional signals are added, and it allows proper registration, even on the pixel edges. The range of the proper threshold setting was calculated for the typical detector parameters and it was shown that the range of the possible threshold setting increases in the C8P1 mode with the increase of the photon energy.

Noise and analog parameters mismatches deteriorate the detector performance, resulting in a variation of the number of counts which are registered. Therefore, noise and parameter spread optimisation is identified as the most crucial aspect of the detector design. The types of errors caused by the noise, gain and DC offset spread and timing issues, were identified for a detector working in the C8P1 mode. The additional hits were counted due to noise and comparator switching and the counts were lost due to the low pixel gain or DC offset.

The simulations show also that the noise peak in the C8P1 mode is shifted with regard to the SPC mode, and therefore it cannot be used for the readout channel parameter extraction. To estimate the pixel gain, for instance, the threshold scan characteristics should be measured in the SPC mode. Thus, the design needs to allow this option.

4 INTEGRATED CIRCUIT DEALING WITH CHARGE SHARING

As described in Chapter 2.3 the first studies done by the AGH and FNAL groups on the full charge reconstruction algorithms, introducing the C8P1 algorithm, were presented in 2011. The C8P1 algorithm was implemented in two integrated circuits, namely MiniVIPIC and Chase Jr. The latter was a subject of the theoretical studies and the tests, which are described in the following Chapters. Therefore, the Chase Jr. chip's design and manufacturing aspects are described in more details in this Chapter in order to introduce the main integrated circuit features allowing for the evaluation and latter tests of the C8P1 algorithm performance and explain trimming of the analog parameters.

4.1 Main aspects of Chase Jr. chip and detector module design

Chase Jr. is a small scale prototype chip, designed in a CMOS 40nm process, dedicated for soft X-ray detectors. The target applications for the detector are XPCS experiments, thus it was designed for and tested with the photon energy of 8 keV. The chip and detector design were widely described in [67], [86]. The photo of the single chip is presented in Fig. 4.1a. The chip bump-bonded to a 320 μm thick silicon sensor is presented in Fig. 4.1b. The layout of the chip is presented in Fig. 4.1c. The prototype chip occupies 2 mm x 4.5 mm of the silicon area. It contains a matrix of 18×24 pixels and peripheral blocks responsible for the communication with the chip and the configuration control. To allow wire bonding, only a part of the pixel matrix (of the dimensions 18 x 18 pixels) was bump-bonded to a sensor. The communication with the chip, implemented according to the Low-Voltage Differential Signaling standard (LVDS), uses seven LVDS transmitters and two LVDS receivers [87]. The analog and digital pads provide power supply, reference voltages and digital control signals. The additional pads on the pixel matrix sides are used for the connection of a sensor guard-rings. The test pads, located in the upper part of the chip, are used for monitoring selected chip voltages during different integrated circuit operations. The Chase Jr. pixel size

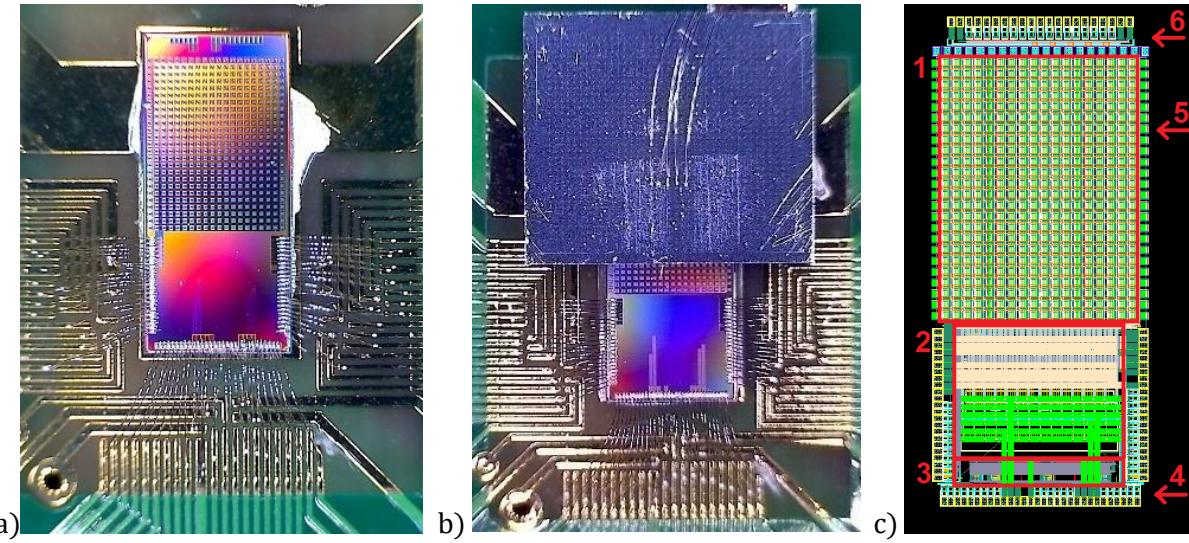


Fig. 4.1 The photo of the Chase Jr. chip a) single, b) with the bump-bonded silicon detector, c) the layout of the Chase Jr. chip. 1 - pixel matrix, 2 – decoupling capacitors and analog references block, 3 – LVDS transceivers, 4 – analog and digital pads, 5 – detector guard ring, 6 – tests structures.

of $100 \mu\text{m} \times 100 \mu\text{m}$ was chosen to match the sensor pixel pitch. The analog front-end occupies 55% of the pixel area. It consists of a CSA, two shapers, two discriminators and a comparator block. The digital back-end occupies 18% of the pixel area. It contains the C8P1 block, two 24-bit counters, and a register. The analog path and the C8P1 block was described in Section 2.3. The counter permits storing numbers of photons detected in the given channel, while the register controls the analog block configuration. The rest of the pixel area is dedicated to the power supply decoupling and the signal routing. During the readout from the pixel matrix the data from the counters in a pixel column are shifted bit by bit into the global shift register. The chip contains a global 18-bit shift register which allows shifting in the chip configuration values to the configuration register and reading the data from 18 pixel columns through two outputs.

4.2 Testability features of Chase Jr. chip

The chip readout channel architecture for the C8P1 algorithm has been already described in Section 2.3. However, the exact implementation of the readout channel is more complex in order to enable, on the one hand, the trimming of the analog parameters (refer to Section 1.6.1) and, on the other hand, evaluation of the prototype C8P1 algorithm performance. Since the chip was built as a prototype, the readout channel was implemented with bearing in mind extensive testability of the individual blocks and processing paths. The Chase Jr. readout channel architecture with all the testability and trimming features is presented in Fig. 4.2, while the description of the configuration bits used for testing and trimming

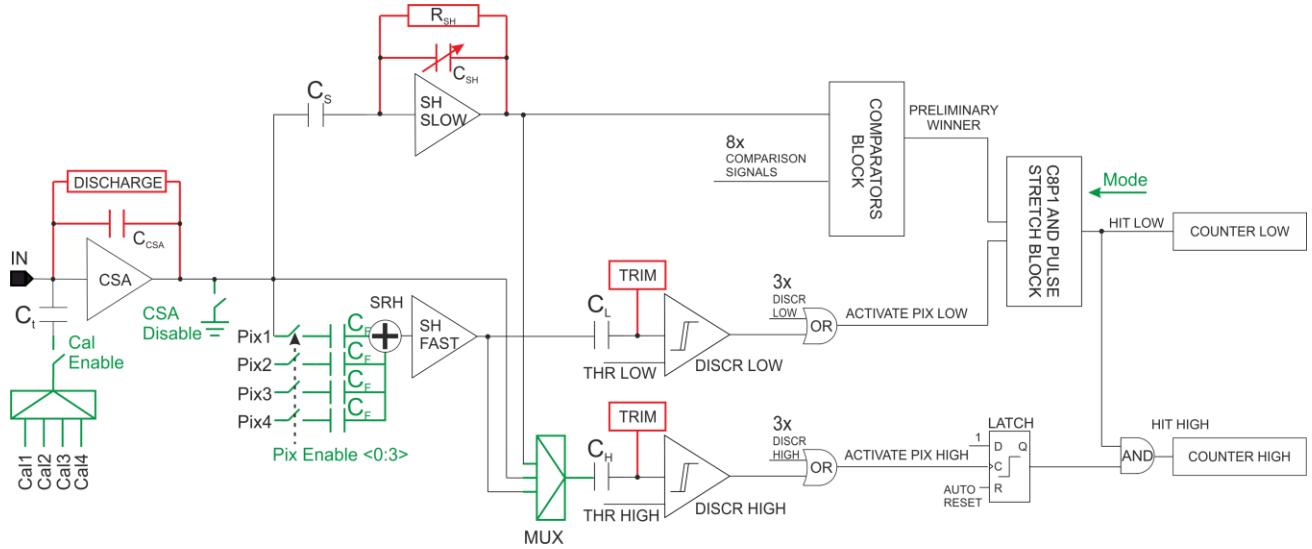


Fig. 4.2 The single readout channel architecture of the Chase Jr. chip with the testability features marked in green and the trimming features marked in red.

of Chase Jr. is presented in Table 4.1. Apart from the functionality already described in Sections 2.3.1 and 2.3.2, the readout channel was additionally equipped with the following testability features:

- The CSA_DISABLE switch,
- The Calibration circuit with the CAL_ENABLE switch,
- The signal rebuild hub with four PIX_ENABLE switches,
- The choice of the operation modes implemented in the C8P1 block,
- The multiplexer MUX,

and the following trimming features:

- The two trimming DACs for DC offsets trimming at the discriminator input,
- The gain switching in the shaper slow feedback,
- The gain switching in the CSA feedback.

Table 4.1 The list of the Chase Jr. configuration bits used for testing and trimming purposes.

Name	Description	Bits No.
TRIM_HIGH	DAC control for THR HIGH trimming	7
TRIM_LOW	DAC control for THR LOW trimming	6
BM	Control of MUX configuration	2
BSF	BSF<4> - control of 2 gain modes of SH FAST BSF<0:3> - control of switches connecting a pixel CSA output to SRH	1 4
BSL	Control of SH SLOW gain	3
BCSA	Control of CSA gain	3
CSA_DISABLE	Control of CSA_DISABLE switch	1
BX	Choice of calibration line (Cal1, Cal2, Cal3, Cal4)	2
CAL_ENABLE	Control of CAL_ENABLE switch	1
LD	Control of comparison latch delay	5
MODE	Choice of operation mode – SPC or C8P1	1

4.2.1 Individual pixels contribution into summing

The first testability feature is the CSA_DISABLE switch, which enables shortening the CSA output to ground. It is useful in the evaluation of the C8P1 performance, as a restricted group of pixels can be chosen to process signals. It allows testing a single pixel both with and without the influence of its neighbours. Each pixel contains also the calibration pulse injection circuitry for verification of the C8P1 algorithm without X-ray radiation and without a sensor bonded to a chip. An internal pulse generation block allows injection of four different current pulses (Cal1, Cal2, Cal3, Cal4) to a pixel if the CAL_ENABLE switch is on. Four voltage steps, feeding the test capacitance $C_t = 4.8 \text{ fF}$, are set globally for the whole pixel matrix, but they can be selected in each pixel with two configuration bits. Thus, the charge sharing effect can be emulated by the injection of different current pulses to four neighbouring pixels at the same time.

The SRH allows the reconstruction of the total signal from fractional signals of four neighbouring pixels. Testability features are used to verify this summing circuit operation, and thus, to control the photon energy reconstruction by the C8P1 algorithm. Not only, the calibration pulse amplitude can be set independently in each pixel using the calibration circuit, but also the pixels contributing to the summing node can be chosen with the PIX_ENABLE <0:3> switches. This functionality admits of verification of the neighbouring pixels contribution to the resolved signal. When all the PIX_ENABLE <0:3> switches are on, the chip operates in the summing mode. By switching off three out of four PIX_ENABLE <0:3> switches, only the signal from one pixel is processed, as if there was no SRH.

4.2.2 Standard and C8P1 mode of operation

The ‘Pix Enable’ switching, together with the choice of the operation mode implemented in the C8P1 block, allows the comparison of the two modes of operation, i.e. the C8P1 mode and the SPC mode. If all the PIX_ENABLE <0:3> switches are on, and the C8P1 mode is chosen at the input of the C8P1 block, the signals from four CSAs of the pixels sharing one corner are added and the digital C8P1 block defines if the counters should be incremented. In the following chapters, this will be referred to as the C8P1 chip configuration or the C8P1 mode. The simplified scheme of the C8P1 configuration without the testability and trimming features included was already presented in Fig. 2.6. If only the PIX_ENABLE <0> switch is on, and the SPC mode is chosen at the input of the C8P1 block, then, no inter-pixel communication is enabled and the C8P1 algorithm is not involved in the hit assignment process. Thus, the counters are incremented on the negative edge of the signals at the discriminators output. This will be referred to as the SPC chip configuration or the SPC mode.

4.2.3 Analog path reconfiguration for purpose of testing and trimming

The multiplexer MUX provides a choice of signals feeding the discriminator high. The signals from the CSA output, the shaper fast output, the shaper slow output can be connected to the discriminator high. Therefore, the MUX is used for testing the CSA and the shapers blocks, and allows setting a configuration needed for the DC offsets, CSA and the SH SLOW gains correction. During trimming, an integrated circuit operates in the SPC mode, so that the parameters of each pixel can be adjusted independently without the neighbouring pixels contribution.

4.3 Circuits for trimming of analog chain parameters

As stated in Section 1.6.1 and Section 3.2.2, the uniformity of the analog parameters between the readout channels is the crucial issue, especially for an integrated circuit with the complex architecture

with algorithms using inter-pixel communication implemented. A Large DC offset spread makes setting of a global threshold for all channels impossible. If an assumption is made that one of the pixels is taken as a reference, and its DC offset equals 0, then a threshold can be set for this pixel in between V_{NOISE} and V_0 (refer to Fig. 1.10). The rest of the pixels with a positive DC offset are more susceptible to count noise hits, whereas the pixels with a negative DC offset may not count hits.

The gain spread alters signals amplitudes, which are directly related to the charge collected by the pixels. This leads to a decrease in the number of properly chosen pixels which collected most of the charge by the algorithm. In the Chase Jr. chip, a large spread of the analog parameters affects the signal reconstruction in the SRH and the signals comparison in the COMPARISON BLOCK. As a consequence, errors in photon energy and a hit position detection may occur.

A large parameter spread caused by a manufacturing process can be compensated by correction circuits [52], [88], [89]. Since the main parameters which affect the performance of the C8P1 algorithm are gain and offsets, the dedicated circuits are implemented for the correction of the CSA gains, the SH SLOW gains and the DC offsets at the discriminators input. Two DACs in each pixel are implemented at the DISCR LOW and DISCR HIGH inputs in the Chase Jr. chip for DC offset correction [53]. Correction DACs are implemented only for the discriminators, while the comparators use the auto-zero method to reduce offsets. The feedback capacitors connected in parallel, which can be switched independently in each pixel within the range of 4-11 fF with the 1 fF resolution, provide the gain control of the CSA. The same mechanism is implemented for the gain control of the SH SLOW, with the feedback capacitance set in the range of 14-28 fF with the 2 fF resolution. The states of the switches are controlled with the registers that can be set independently for each pixel.

4.4 Correction procedures

The correction procedures are based on the extraction of the analog parameters such as offsets, and gains (refer to Section 1.5.6). The first step of the trimming process involves the DC offsets at the discriminator inputs correction. Then the CSA gains are trimmed, and finally, the SH SLOW gains undergo a similar correction procedure.

4.4.1 DC offsets trimming

The idea for the DC offset correction procedure is to choose the right DAC value for each pixel which results in the lowest DC offset spread in the whole pixel matrix. Therefore, a target DC offset must be chosen as a reference for all the pixels. Then, for each pixel a trim DAC correction value for which

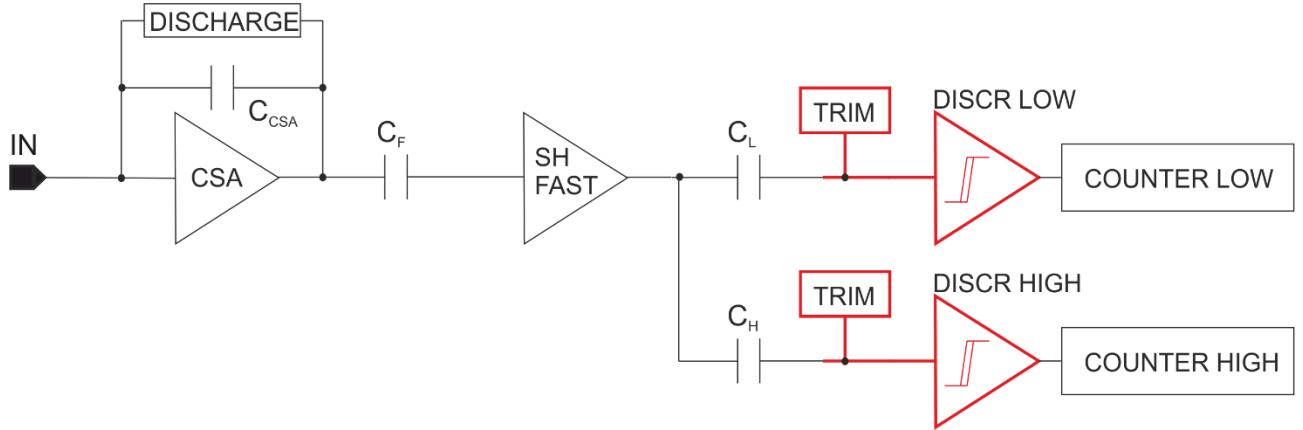


Fig. 4.3 The analog chain configuration for the purpose of the DC offsets trimming.

the distance between the DC offset and the target DC offset reaches the minimum is chosen. There are several possible techniques of correction, including the threshold scan based method and the trim DAC scan based method. However, irrespectively of the method chosen, the analog path is configured as shown in Fig. 4.3.

In the first method, called the standard correction, the threshold scans without any input signal (CSA_DISABLE switch is on) are performed for all the possible codes of the trimming DACs for all the pixels. The Gaussian model is fitted to the obtained noise counts characteristics to extract the DC offset values for each pixel. A sample trim DAC characteristics for Chase Jr. representing the extracted DC offsets plotted versus the DAC values for all the pixels are presented in Fig. 4.4a. As shown in Fig. 4.4b, the DC offset spread after trimming is dependent on the target DC offset chosen. For the too low and too high target DC offset values, the spread increases, since the target DC offset is inaccessible for a significant fraction of pixels. Therefore, the target DC offset is chosen as a mean value from DC offsets for all the pixels obtained for the centre code of the DAC. As a consequence, it is possible to minimise a DC offset spread. Fig. 4.4c shows sample results of the trimming. The offset spread before trimming for the mean DAC value was reduced nearly 10 times by applying this correction procedure.

The disadvantage of the described procedure is its significant time consumption, since the threshold scans must be performed for all the DAC values. For Chase Jr., the whole procedure took about 2 hours. Another trimming technique which is more time efficient is based on so called the trim DAC scan [88], [90]. In this method, called for simplicity hereafter the fast correction, the number of the counts

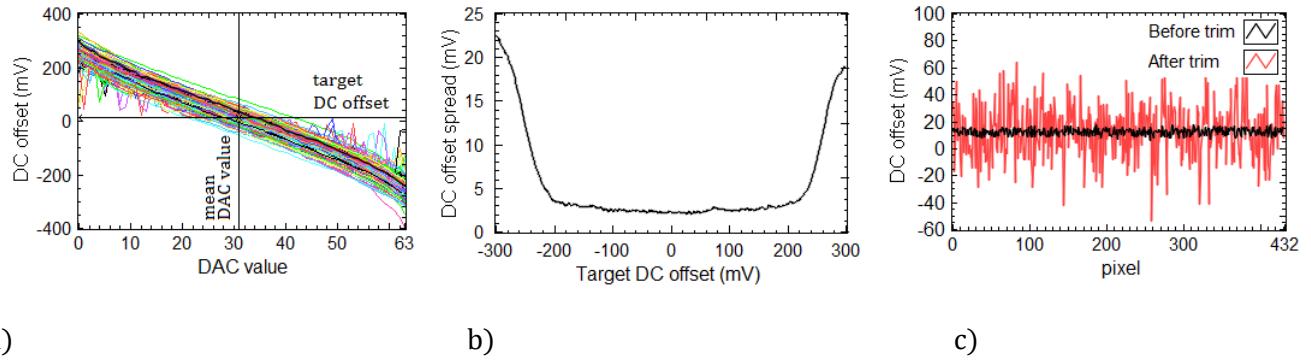


Fig. 4.4 a) The trim DAC characteristics. b) The DC offset spread ($\sigma(V_T)$) as a function of the target DC offset. c) The DC offset spread before and after trimming.

is measured with one set threshold for all the trimming DAC values. Then, the trim DAC values for which the maximum number of counts is achieved in each pixel are chosen as the correction values.

Moreover, the correction procedures, can be further accelerated if the DACs characteristics are monotonic or linear. In this case, a DAC range can be measured first and the optimisation algorithms can be incorporated, in order to reduce the total number of the tested DAC codes.

4.4.2 Gains trimming

The second step of trimming involves the CSA gains trimming, which equalizes the response of the fast processing paths. The analog path is configured as shown in Fig. 4.5, so the CSA output is connected via the multiplexer directly to the discriminator input. The threshold scans are performed when a detector is either uniformly illuminated with monochromatic X-ray radiation of the known energy or the calibration circuit is used to inject the same calibration pulses to each pixel in the matrix. The advantage of performing trimming using calibration pulses is the possibility of trimming a chip before bonding it to a sensor. However, any mismatch of the calibration circuits parameters impacts the correction

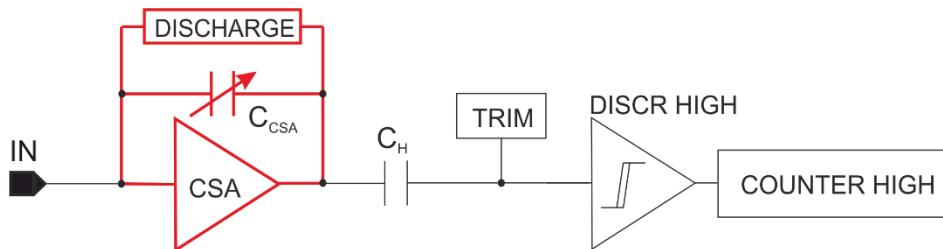


Fig. 4.5 The analog chain configuration for the purpose of CSA gains trimming.

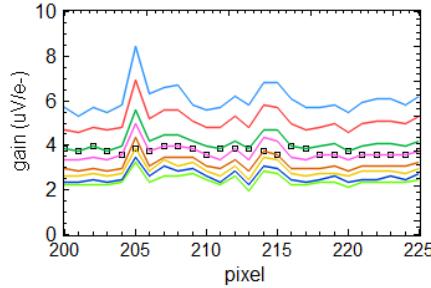


Fig. 4.6 The CSA gain values for all BCSA parameter configurations for selected pixels.

precision. Therefore, the gain can be calculated more precisely from the measurements with X-ray radiation. The gain values are extracted for all eight possible gain settings. The register values resulting in each CSA gain closest to the mean gain are chosen for each pixel. A sample plot given in Fig. 4.6, showing all the measured gains for selected pixels, illustrates the gain correction idea. The black squares represent the resulting gain values chosen in the correction procedure. The gain spread from before trimming was reduced nearly 2 times by applying this correction procedure.

The last step is the SH SLOW gains trimming, performed in the same manner as the CSA gains trimming with the readout channel configured as shown in Fig. 4.7. The trimming procedures should be performed in the aforementioned order. The DC offset correction allows performing threshold scans for the gains trimming procedures in a narrow threshold range, which improves the trimming procedure speed. The CSA gains are trimmed in the next step, as they contribute to the total gains of the fast and slow paths. Once the CSA gains are trimmed, the SH SLOW gains can be trimmed to ensure the proper performance of the hit assignment process by the COMPARATORS BLOCK. The SH FAST gains are not trimmed in the Chase Jr. chip, since this shaper is used only for triggering the process of hit assignment by the C8P1 block. Therefore, only two gain modes (i.e. the high gain mode and the low gain mode) are provided in the design. Although the SH FAST gains trimming turned out to be not critical

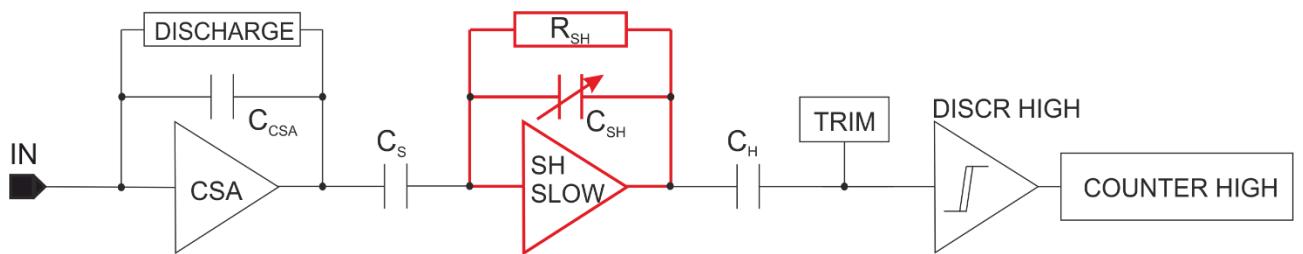


Fig. 4.7 The analog chain configuration for the purpose of SH SLOW gains trimming.

for the C8P1 algorithm operation in the prototype chip (refer to Chapter 6), it will grow in importance in future designs operating with several energy thresholds.

Due to the fact that trimming procedures significantly improve the detector performance, especially with the implemented algorithm dealing with charge sharing, the trimming procedures described in this Chapter were performed for each tested module of the Chase Jr. chip. The results of trimming are described in Chapter 6. More details concerning the circuitry allowing extensive tests of the different chip blocks and functionality can be found in [91].

5 DEDICATED MEASUREMENT ENVIRONMENT FOR INTEGRATED CIRCUIT FOR HYBRID PIXEL DETECTOR

To verify the simulation results obtained during the design phase of the chip, the fabricated device must undergo a series of tests, preceded by the correction procedures described in Section 4.4. Since the same tests need to be applied for all the modules produced, a dedicated software is the solution optimised for automation and minimisation of the tests duration. Therefore, such a testing platform was implemented for the tests of the Chase Jr. chip.

The requirements for a testing environment include easy automation, design modularity and flexibility, and possibility of handling parallel processes using several different hardware instruments. The solution should be modular and scalable to ensure that both the core application and particular functions can be reused for the next generation of tests with either new versions of the chip or using different measurement equipment. In this Chapter the requirements for the testing platform, the measurement set-up for a hybrid pixel X-ray detector and the software implementation are described.

5.1 Requirements for measurement environment

An integrated circuit for a hybrid pixel detector ought to be tested in various environments, both with and without a sensor bonded. In general, the core of the system is a detector module attached to a dedicated PCB. The measurement set-up consists of a control module and hardware instruments for biasing of the chip and communication. Additional test-dependent peripheral devices, like an X-ray tube, a wafer probing machine or an XY stage motion controller should be also considered. A general view of a measurement set-up arrangement with aforementioned modules is presented in Fig. 5.1.

The requirements for the measurement system for the Chase Jr. chip are listed below:

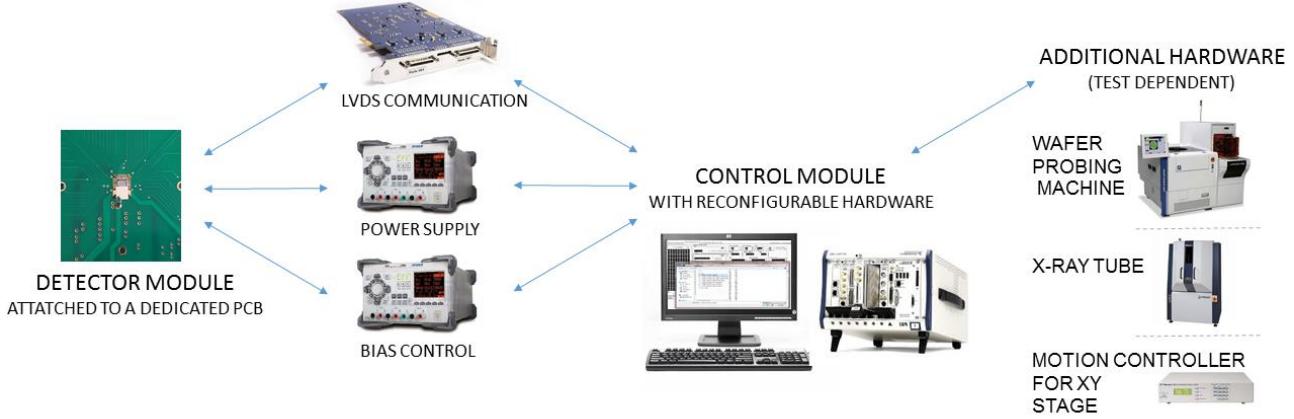


Fig. 5.1 The setup required for the ASIC tests.

- The system should support a high speed digital input/output communication with the chip in the LVDS standard.
- The system should admit of control and measurement of such analog parameters like bias and power supply voltages and currents with low-noise instruments.
- The system should allow easy reconfiguration of the chip by setting configuration bits.
- The system should support task synchronization by handling parallel processes of communication, instruments control, data acquisition, data online presentation, data analysis and data logging.
- The system should allow automation of the tests and correction procedures.
- The solution should allow to adjust the system easily to any new instruments or testing procedures that can be developed in future.
- The software architecture should be divided in separate modules performing particular tasks, it should be easily scalable to adjust to new versions of the chip and also to allow new types of tests for example using different instrumentation.

5.2 Test procedures

The choice of testing procedures for hybrid pixel detectors is determined by specific functionality and applications of a module to be tested. In general, a testing platform should allow performing several procedures which cover setting integrated circuit and control instruments configuration, performing simple digital tests, executing correction procedures and performing single or parametrised threshold scans. The tests can be divided in general into two cases, namely, with or without X-ray radiation. Since bonding a chip to a sensor is an expensive process, in the first stage, the chips on the wafer [92] or already

mounted to a PCB board but without a sensor undergo a series of tests. Due to the calibration internal pulse generation block, X-ray radiation can be emulated, and parameters and functionalities of the chip can be characterised. After these preliminary tests, a chip is bonded to a sensor and further tests with X-ray radiation are performed. In the following sections, testing procedures are described.

5.2.1 Preliminary tests without X-ray radiation

The first step of the Chase Jr. verification is testing a chip mounted to a PCB board without a sensor bonded. A set of bench tests is designed for that purpose covering the power consumption check, verification of the ASIC bias currents, communication tests and tests of the chip functionality using an internally generated calibration pulse. It allows test modules without X-ray radiation. The standard tests procedures are listed in Table 5.1.

The first test covers the bias currents and power consumption comparison with previously simulated values in order to reveal any possible issues with power supply and references globally set for all the pixels. The following test steps provide a digital verification of the chip. To verify the communication with the chip, the shift register's test and the counters' test are performed. During the shift register's test random values are written to the global shift register and they are read out and checked whether they were not altered or corrupted in any other way. The counter test verifies not only the global register, but also the readout from the whole pixel matrix. In this case, random values are shifted to the global shift register, then written to the counters and read out from the counters using the global shift register. The result of the comparison with the input sequence verifies the communication with each pixel in the matrix.

After the digital verification, the analog parameters for the pixel matrix are extracted. The chip undergoes the fast correction procedure described in Section 4.4.1. Since the chip is equipped with the calibration pulse injection circuit, the tests without the sensor connected can be performed, emulating the registration of photons by the readout channel. Using this functionality the gain correction procedures described in Section 4.4.2 can be carried out. The analog parameters spread between the channels can be estimated before and after correction. However, it should be noticed that the final correction results obtained for the tests with X-ray radiation can be different due to the capacitance spread in the calibration pulse injection circuitry among the channels. Nevertheless, these tests are important to estimate if there

Table 5.1 Standard test procedures for the ASICs before bonding to the sensor.

No.	Tests type
1	Bias currents measurement
2	Power consumption measurement
3	Shift registers test
4	Counter test
5	DC offset fast correction
6	Gain correction
7	Tests with calibration pulses

are no bad pixels in the matrix and if the analog parameters in each pixel can be trimmed so that the analog parameters spread would be within the acceptable ranges.

The calibration pulse injection circuit allows also further tests without X-rays, which aim at the verification of the algorithms for dealing with charge sharing. The functionality of the test pulse injection circuit allows setting four different global voltage steps feeding the calibration capacitance in each pixel. Thus, one out of four values can be selected using the configuration bits. This emulates the division of charge generated in the detector between 4 pixels. Additionally, calibration can be switched on and off separately in each pixel. Therefore, various dedicated neighbourhoods can be tested.

5.2.2 Tests with X-ray radiation

After bonding a chip to a sensor, the standard test procedures listed in Table 5.1 are executed, except of the tests with a calibration pulse. Depending on the X-ray source used, different types of tests can be performed, namely flat field illumination experiments or pencil beam experiments (refer to Section 1.2.3). The first type of the experiment, aims at checking the uniformity of the detection system parameters and, their correction, while the latter aims specifically at the assessment of the C8P1 algorithm. The particular tests are described in Chapter 6, presenting the measurements results, and the software allowing performing such tests is described in the next section.

5.3 Measurement set-up

Bearing in mind that the environment should allow easy automation, design modularity and flexibility, and handling parallel processes using several different hardware instruments, the LabVIEW graphical programming environment was employed to implement the software. It allows implementing of the application core, the communication with the chip and the control of the hardware instruments on one platform. National Instruments modular devices, which can be easily programmed with LabVIEW environment, were chosen. The list covering the devices used to build a measurement set-up is presented in Table 5.2.

The core of the system consists of a detector module attached to a dedicated PCB and a PXI control module equipped with the reconfigurable hardware. The communication and biasing of the chip is provided using the dedicated National Instruments hardware. A high speed digital waveform generator and an analyser are used for digital communication using the LVDS standard. The analog output modules are used for analog blocks biasing. The modular instruments in the control module chassis can be exchanged with other devices, as needed. For example, depending on the laboratory equipment availability, either a dedicated low-noise source measurement unit or Rigol power supply was used for biasing integrated circuit analog and digital blocks. The control module is also responsible for communication with the programmable external devices, such as a wafer probing machine, an X-ray tube or a motion controller. Controlling such devices within one platform allows synchronising and automating of test procedures.

Table 5.2 A list of measurement setup devices chosen for the Chase Jr. tests.

	DEVICE	MANUFACTURER	ABBREVIATION
1	Controller NI PXIe-1062Q	National Instruments	Control module
2	Multifunction DAQ NI 6733, NI 6259	National Instruments	Bias control
3	NI PXI 6562 HSDIO LVDS Interface NI	National Instruments	Digital interface
4	Rigol DP832	Rigol	Power Supply
5	Chase Jr. readout chip	TSMC	Chase Jr.

5.4 Software functionality for testing procedures

After the basic procedures of bias currents measurements, power consumption measurements, shift registers tests and counter tests, the next steps, involving integrated circuit correction and threshold scan tests, can be performed. These tests require a proper chip configuration. Especially, for testing the C8P1 algorithm in Chase Jr., setting the control bit configuration (refer to Table 4.1) for each pixel to cover different test scenarios remains an important aspect. The configuration bits in the Chase Jr. chip can be set independently in each pixel. By changing the configuration, a user can perform tests with or without a calibration pulse or choose the pixel neighbourhood for tests. The functionality of the complex algorithm for the elimination of the charge sharing effects can be decomposed and tested stage after stage by setting a chip in the SPC configuration or the C8P1 configuration. Therefore, a convenient panel allowing changing and reloading the chip configuration, was implemented. It is shown in Fig. 5.2. The application allows changing each bit separately for each pixel, using predefined configurations, loading the configurations created as a result of correction procedures or loading the configurations from the previous tests from a file.

Once a bit configuration is loaded, the correction and test of the chip can be performed. The panel, presented in Fig. 5.3, allows performing a threshold scan, which is the most often used test for integrated

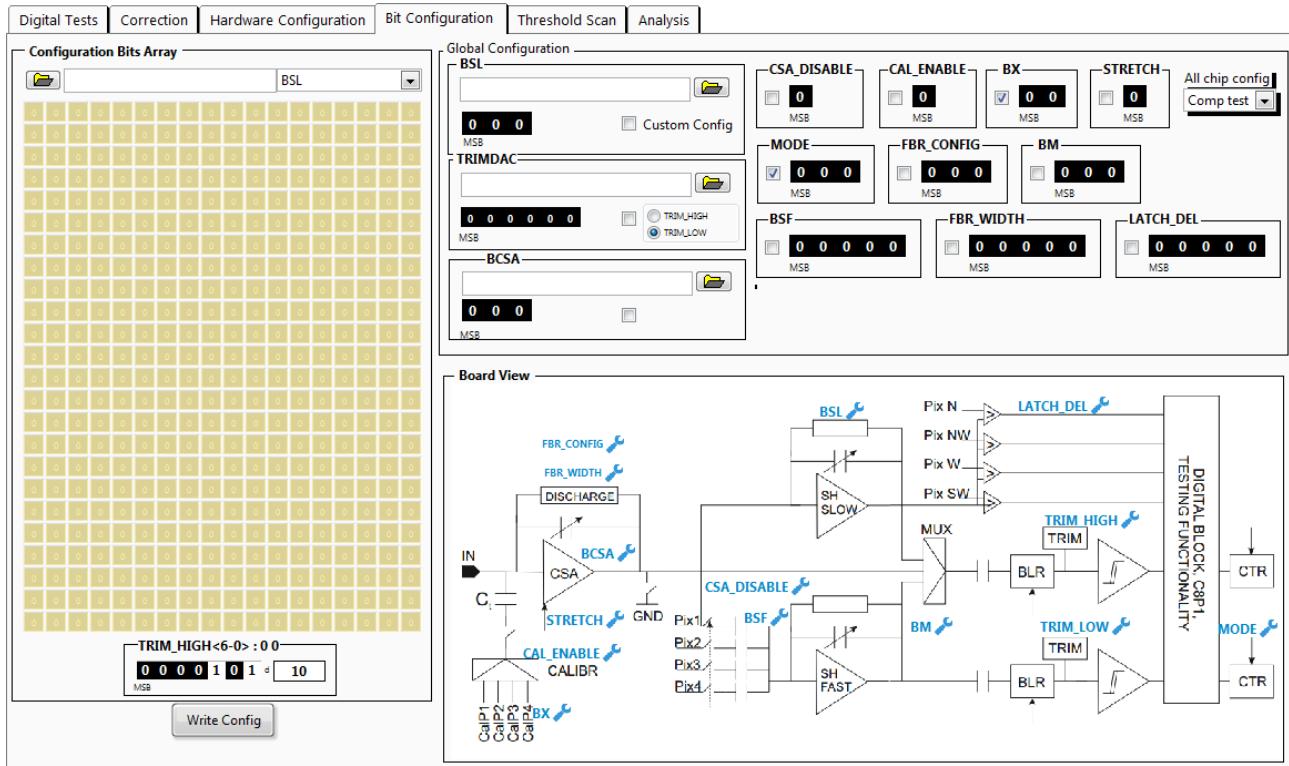


Fig. 5.2 The user interface panel allowing setting the chip configuration.

circuit validation. Firstly, the test parameters need to be defined. A user can define a single threshold scan test, enqueue a set of tests with different configurations, or define a parameter scan in which the chip configuration bits or external device parameters can be changed within a range. Secondly, the parameter threshold scans allow performing automated correction procedures, since, as explained in Section 4.4, the threshold scan for all the DAC or register values need to be done to start these correction procedures.

The application architecture is multithread. It supports performing multiple tests together with data analysis and defining another test at the same time. The test results can be observed online and are plotted on two graphs, namely the ‘Threshold Scan’ and ‘Pixel Matrix’ graphs. The ‘Threshold Scan’ plot represents the number of counts versus the threshold value for a pixel chosen by a user. The ‘Pixel Matrix’ is an intensity plot representing the current number of counts in the whole pixel matrix for a selected threshold. The shortcut keys copy the visual data from the plots to the clipboard, supporting quick report creation. The final results, together with the chip and the hardware configuration are saved to a file defined by a user.

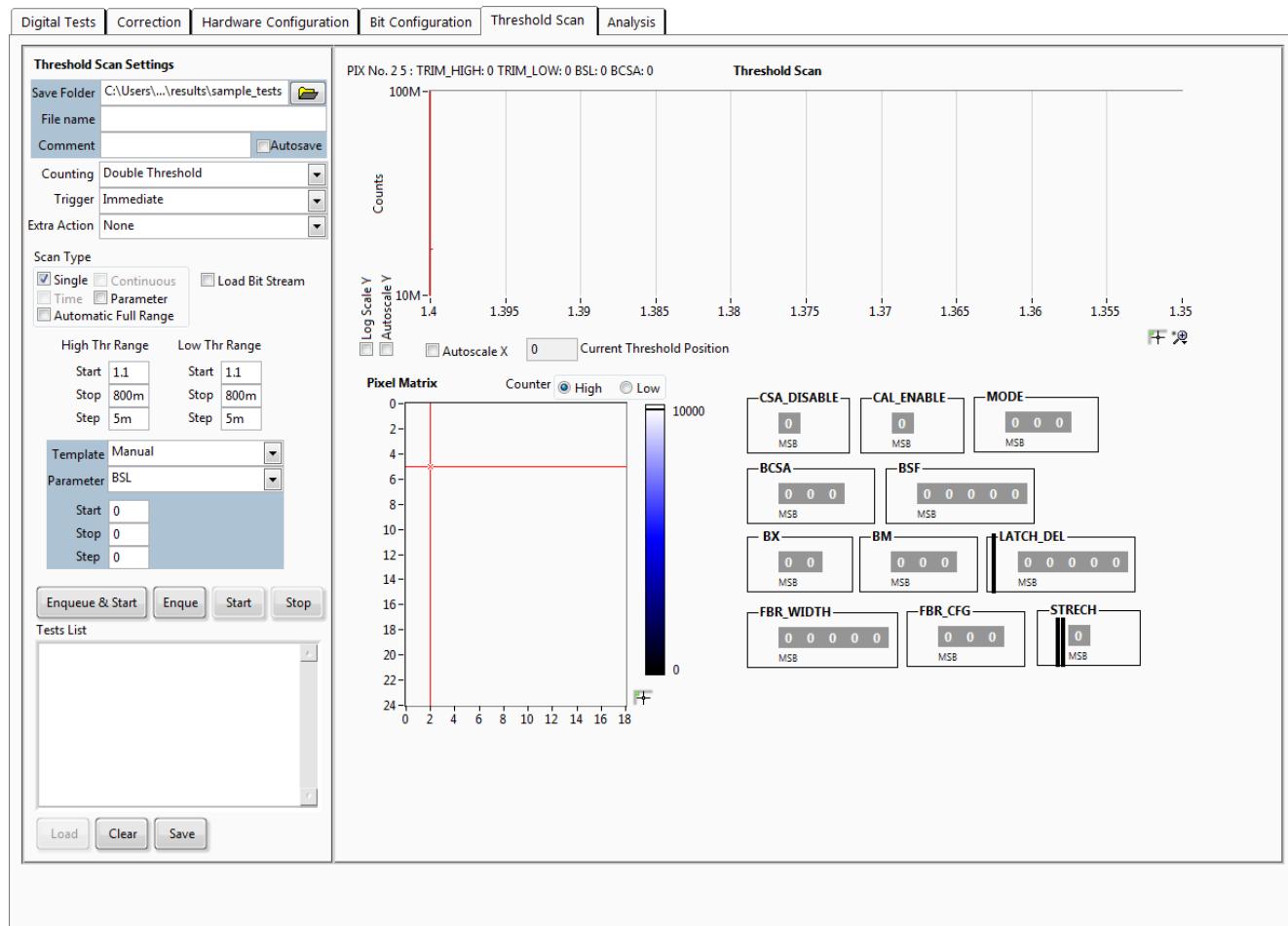


Fig. 5.3 The user interface panel for the threshold scan tests.

5.5 Software architecture and implementation

To implement the aforementioned functionalities, a multi-thread application was designed. The modules building the application are schematically presented in Fig. 5.4. A core application is divided into six modules, each implemented as a separate state machine. The USER INTERFACE module is implemented as an event-driven state machine [93], since its role is to react to user's actions. The rest of the modules are implemented as queued state machines [93]. This architecture supports multitasking. At the same time, a user can configure the tests on the user interface, the offline analysis can be done. The analysis does not affect the THRESHOLD SCAN thread, the thread with the highest priority, which is responsible for communication and readout from the chip. The communication between the modules is realized via queues, represented in Fig. 5.4 with blue 'Q' sign. For the communication from the MAIN CONTROL thread to the USER INTERFACE thread, a user event mechanism is used, represented with the orange 'UE' sign [93]. Each thread has its own data structure implemented as the 'Type Definition Cluster'.

The dedicated API (application programming interface) for the queue communication was implemented, wrapping the queues functions in the Functional Global Variable architecture. It supports readability of the code and allows calling the same queue function with arguments defining the action (such as 'Dequeue', 'Enqueue', 'Flush', etc.), the command to be executed by the receiver (implemented as 'Enum' and 'Variant Control') and the sender's ID. The state machine template designed for a purpose of implementation of all the threads in this application is presented in Fig. 5.5.

Since the main tasks are defined in separate threads, they can work independently, optimising the tests time and yielding flexibility. Application modularity and low coupling allows maintaining

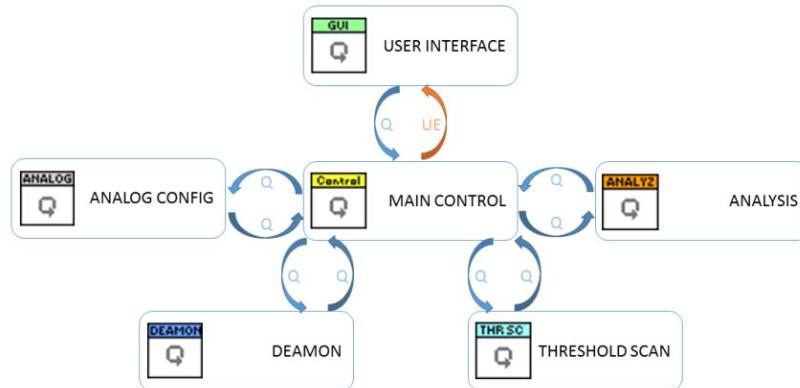


Fig. 5.4 The application architecture diagram.

the application easily and should any of the instruments need replacement, only one of the modules is changed, while the application core structure remains unchanged. Moreover, the application can be easily adapted to other devices under tests and other hardware used for biasing and controlling the chip due to the low-level API. All these aspects provide testing environment, which can be reused for future chip and set-up designs.

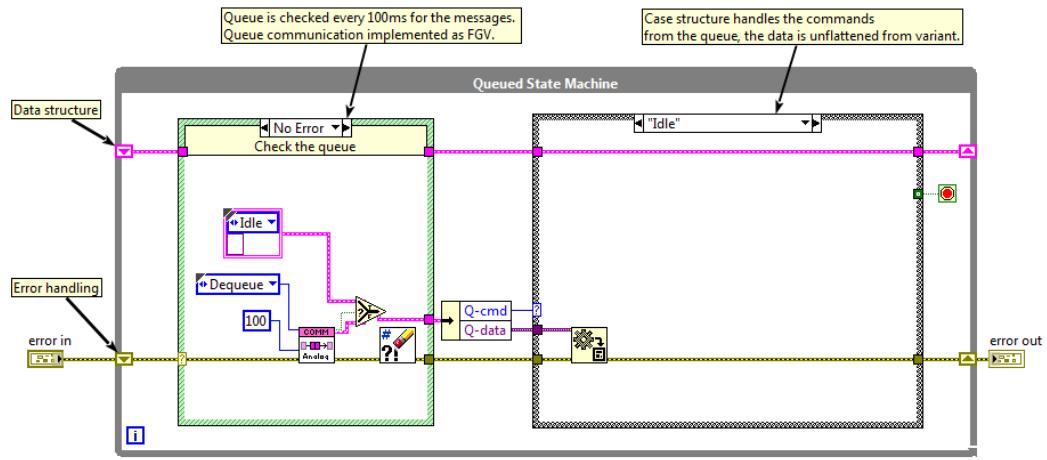


Fig. 5.5 The queued state machine concept implemented in LabVIEW.

6 MEASUREMENTS RESULTS

The aim of the experiments is, on the one hand, to develop general methods of evaluation of an inter-pixel algorithm dealing with charge sharing, and, on the other hand, to introduce these methods to the evaluation of the performance of the C8P1 algorithm. The experiments are designed so that the detection efficiency could be quantified in the case of charge sharing. Detection efficiency refers to counting each photon which hits a detector and to allocation each event to a proper pixel. Two approaches how to achieve this goal are addressed in this Chapter. The first approach involves testing a chip without X-ray radiation, using calibration pulse injection circuits and it is described in Section 6.2. It allows preliminary tests of the chip, even without a sensor bonded. Moreover, using different pulse amplitudes injected to the neighbouring pixels, the photon interactions at known positions and thus, charge sharing, can be emulated. The second approach, presented in Section 6.3, involves tests with X-ray radiation. The pencil beam tests allow positioning the photon flux at the pixel border to study charge sharing, in particular, for rare cases when the charge is shared nearly equally between two or four pixels. Moreover, the chip's sensitivity to the analog parameters spread and mitigation of the performance degradation achieved with the digital correction blocks are studied. Finally, the tests targeting estimation of the maximum count rate that can be handled by the device operating in the SPC and C8P1 modes are addressed.

6.1 Correction results

The correction procedures were performed in the order described in Section 4.4 to compensate the effects of the analog parameters spread. At first, trimming of the DC offsets at the discriminator inputs was performed and the correction results are presented in Section 6.1.1. Then, the CSA and the SH SLOW gains were equalized. The results of this procedure are given in Section 6.1.2. The correction results provided in Section 6.1 were measured for a sample Chase Jr. module with a sensor bonded, that was used in the experiments with X-ray radiation introduced in Section 6.3. The same correction procedures were performed for all the modules.

6.1.1 DC offset correction

In the first step of correction, addressed in Section 4.4.1, the spread of DC offsets at the discriminators was reduced by applying DAC codes calculated in the DC offsets trimming procedure for a 7-bit trimming DAC. The threshold scans without an input signal performed before and after correction, as well as histograms of the DC offsets values before and after the correction are presented in Fig. 6.1. The fast correction allowed the reduction of the spread of the DC threshold offsets from $\sigma = 15.13$ mV to $\sigma = 0.75$ mV.

The standard correction method effectively led to the same results, however, the execution time was significantly shorter for the fast correction method. The procedure duration can be calculated from the formula Eq. 6.1:

$$t_{proc} = (t_{step} + t_{set}) \cdot n + t_{valid} \quad \text{Eq. 6.1}$$

where t_{proc} is the total procedure time, t_{step} is the time needed to execute each measurement step (in case of the standard correction it is a threshold scan, in case of the fast correction it is a single measurement for one threshold value), t_{set} is the time needed for changing the settings between the steps, n is the number of steps (for both procedures, it is the number of possible DAC codes), t_{valid} is the time needed for the correction validation (for both procedures, it includes performing the final validation threshold scan for the corrected pixel matrix).

Assuming that threshold scans are performed for the 0.5 V threshold range with the 1 mV threshold step, it can be calculated that the measurement steps are 500 times more time consuming in the standard correction procedure to ensure that the whole trim DAC range is covered and the precision of estimation of the Gaussian noise peak is maintained at the satisfactory level. The procedure durations, including additional operations, such as model fitting, saving to a file and performing validation scans, are measured to be approximately 40 seconds and 2 hours for the fast and standard correction, respectively.

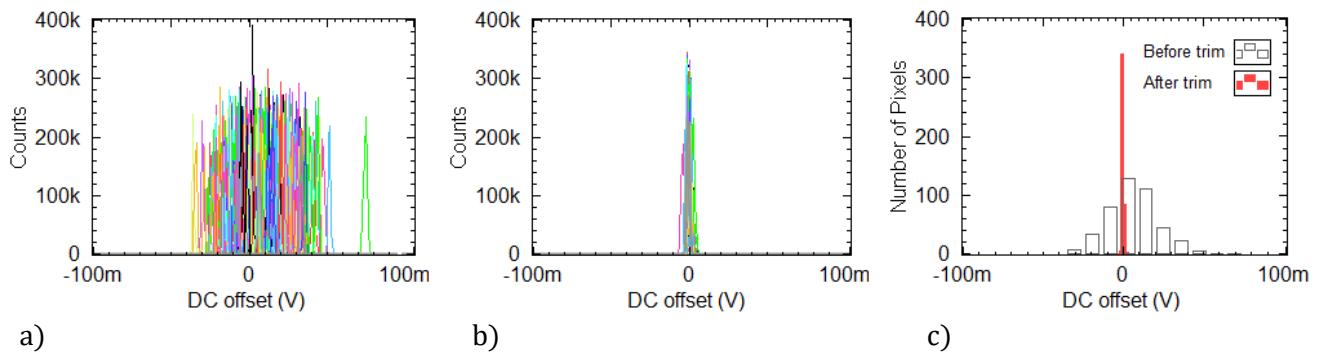


Fig. 6.1 Threshold scans for 432 pixels a) before and b) after DC offsets correction. c) Histograms of the DC offsets of the discriminator thresholds for 432 pixels before and after correction.

The fast correction procedure can be also further improved in terms of time consumption. Assuming the linearity of the trim DAC characteristics, the trim DAC scan steps can be spaced more widely, i.e. taking every second or every fourth trim DAC value. Then, the interpolation can be used to pick the trim DAC value for which the DC offset would be closest to the target value.

Considering the spread of the DC threshold offsets before and after the correction, the spread decreased during the correction by more than 20 times. If the higher precision of the DC offset correction is needed, the trim DAC current, controlled with an external bias, can be adjusted, entailing the trim DAC characteristics slope adjustment. For the optimal trim DAC current, two requirements should be met. The first is that the trim DAC range covers the target DC offset value for all the pixels. It guarantees that all, even the outlying pixels can be corrected. At the same time, the trim DAC characteristics slope should be as low as possible, to provide the highest possible resolution. Therefore, theoretically, the results of the correction with a 7-bit DAC can be further improved by the order of 4, provided that there are no outlying pixels. However, bearing in mind that the offset spread is less than 1 mV, which corresponds to less than 36 e⁻, and the noise ENC = 117 e⁻ rms, it was assumed that for the purpose of the experiments, the DC offset spread was at the satisfactory level allowing proper global threshold setting.

6.1.2 Gain correction

After the DC offsets correction, the gains corrections procedures, introduced in Section 6.1.2, were performed. The gain was extracted using the methods of the analog parameter estimation given in Section 1.5.6.

The sample results for the module, addressed further in Section 6.3, are presented. The correction results are restricted to those pixels connected to a sensor which registered the incoming photons. The upper part of the pixel matrix was not stud bump-bonded to a sensor in order to allow wire-bonding of the chip. Both CSA and SH SLOW gain correction procedures require performing eight threshold scans and then model fitting, which takes about 10 minutes altogether.

The gains extracted from the threshold scans before and after trimming for the chip configured for the purpose of the CSA gains trimming (see Fig. 4.5) are presented in Fig. 6.2a and the histogram of the gains is shown in Fig. 6.2b. The gain spread, calculated as the standard deviation to mean gain ratio, achieved after correction was 3.8%. The results of the SH SLOW trimming are presented in Fig. 6.3a and the corresponding histogram of gains is shown in Fig. 6.3b. The gains are the total gains of the slow path, since the analog chain configured for the purpose of the SH SLOW gains trimming consists of the CSA and the SH SLOW (see Fig. 4.7). The gain spread, calculated as the standard deviation to mean gain ratio,

achieved after correction is 2.3%. The mean gains and the gain spread are summarised in Table 6.1. The CSA gain correction procedure decreased the gain spread about three times and the SH SLOW gain correction decreased the gain spread more than four times. Taking into account the nominal gain of the fast signal processing path, including CSA and SH FAST, estimated as $27.6 \mu\text{V/e-}$, the threshold dispersion after correction, expressed in electrons, equals $\sigma = 27 \text{ e-}$. The noise, calculated for a module with a sensor bonded,

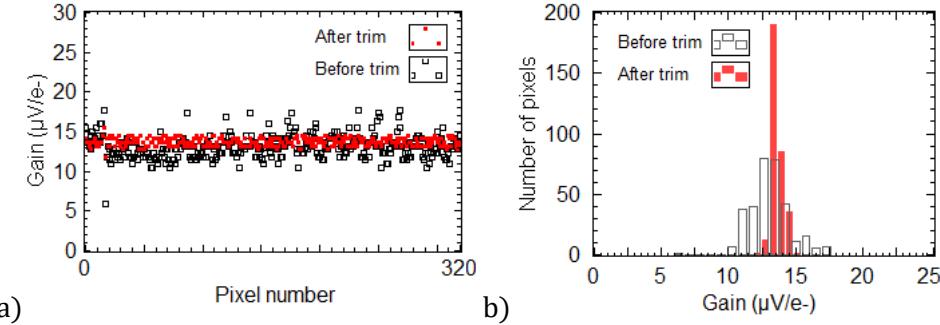


Fig. 6.2 The CSA gains before and after correction. a) Gain values for all the pixels, b) Gains histogram.

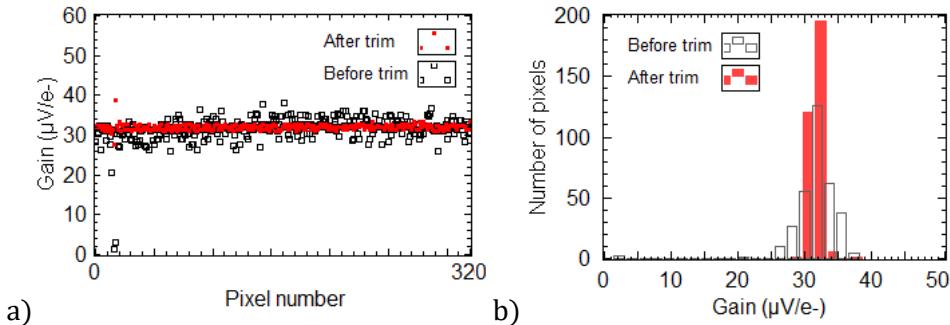


Fig. 6.3 The slow path gains before and after correction. a) Gain values for all the pixels, b) Gains histogram.

Table 6.1 The gain correction results.

	CSA		SH SLOW	
	Before correction	After correction	Before correction	After correction
mean k_V ($\mu\text{V/e-}$)	13.1	13.7	31.5	31.9
σ_{k_V} ($\mu\text{V/e-}$)	1.51	0.52	3.28	0.73
$\frac{\sigma_{k_V}}{\text{mean } k_V}$ (%)	11.5	3.8	10.4	2.3

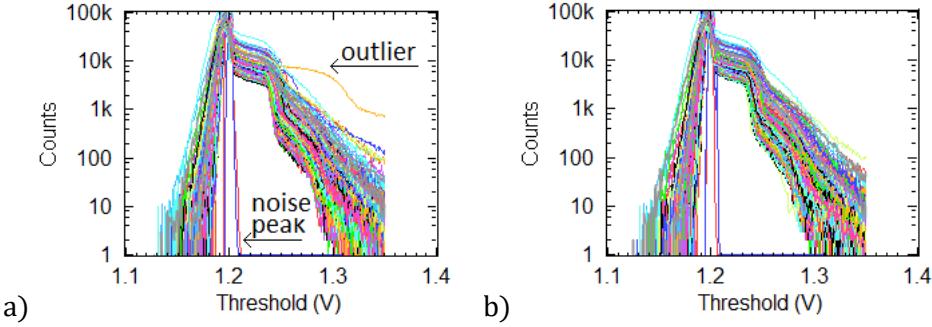


Fig. 6.4 Threshold scans for the detector illuminated with X-rays a) before and b) after CSA correction.

equals $\text{ENC} = 117 \text{ e}^-$. Considering the DC offset spread reduction, the CSA gains spread reduction and noise performance, it is possible to set a global threshold for all the pixels, being only electronic noise limited.

Similarly to the DC offsets trimming, one of the main goals of the gains trimming is to adjust the outlying pixels. The outlying pixels are those rare cases with an extremely large or low gains. The detector works properly only if the whole pixel matrix is uniform. Therefore, if the correction range is high enough, the outlying pixel can be trimmed. A sample set of threshold scans before and after correction for another module, which contained an outlier is presented in Fig. 6.4a and Fig. 6.4b, respectively. It can be observed that for some of the pixels, which were not bonded to the sensor, only Gaussian noise peak was registered. The correction performed by digitally assisted analog blocks allowed trimming the outlying pixel with the high CSA gain and made a global threshold setting possible.

To conclude, the CSA gains uniformity is important for the C8P1 algorithm triggering in the fast processing path, whereas, the SH SLOW gains uniformity improves the signals comparison between the pixels. The influence of the correction on the algorithm is studied in the next chapters. In the following chapters, it is assumed that all the correction procedures were performed in advance, unless it is stated otherwise.

6.2 Experimental results of tests without X-ray radiation

The calibration pulse injection circuitry, introduced in Section 4.2, allows verification of the C8P1 algorithm without X-ray radiation and a sensor bonded to the chip. The charge sharing effect can be emulated using the calibration circuit by injecting different current pulses to four neighbouring pixels. When the Chase Jr. chip without a sensor bonded is tested, the gains trimming using the calibration pulses is used. The mismatch of the parameters of the calibration circuits, especially of the capacitors, influences the signal amplitudes at the input of the C8P1 algorithm. Therefore, the correction procedures

are performed before the tests. It should be noted that due to the calibration capacitances spread, the calibration circuit contributes to the gain spread. However, passing over the cause of the gain spread, the gains can be corrected using a calibration circuit, to achieve the calibration pulses of the amplitudes corresponding to the wanted fractional signals. The correction with the calibration circuits exhibits a translinear approach, meaning that despite the capacitances spread, the uniform and proportional signals can be achieved at the inputs of the C8P1 algorithm for preliminary testing purposes. When a complete detector with a sensor was tested, the trimming was performed one more time using X-ray radiation.

The following sections are dedicated to the preliminary tests performed using the calibration pulse injection circuitry, including the tests of the pixel contribution into summing, the influence of the correction on the C8P1 performance and the tests emulating charge sharing, when hits occur at the pixel border.

6.2.1 Linearity of calibration circuit

The preliminary tests of the Chase Jr. chip were performed without X-ray radiation. The calibration pulse injection circuit was used for the gain correction. The linearity of the calibration pulse injection circuit was measured first, before any tests of summing of signals from the neighbouring pixels by the SRH block and before the C8P1 tests, were performed. The calibration circuit response was measured by performing the threshold scans with the calibration amplitude varying within the range of 20-270 mV. The discriminator pulses were counted and the pulse amplitude $V_0 - V_{\text{noise}}$ was estimated following the method given in Section 1.5.6. Fig. 6.5a presents the raw data and Fig. 6.5b shows the linear models fitted to the measured pulse amplitudes for 432 pixels. The average slope for the linear fitting models was estimated as $a = 0.78$, with $\sigma = 0.04$ and the intercept $b = 3.47$ mV with $\sigma = 4.11$ mV. Within the range between 20 mV and 270 mV, the calibration pulse injection circuits are assumed to be linear for the majority of pixels. However, one of the pixels exhibits a nonlinear behaviour for the low calibration amplitudes, which can be traced down to the problems with error function fitting due to the larger noise measured

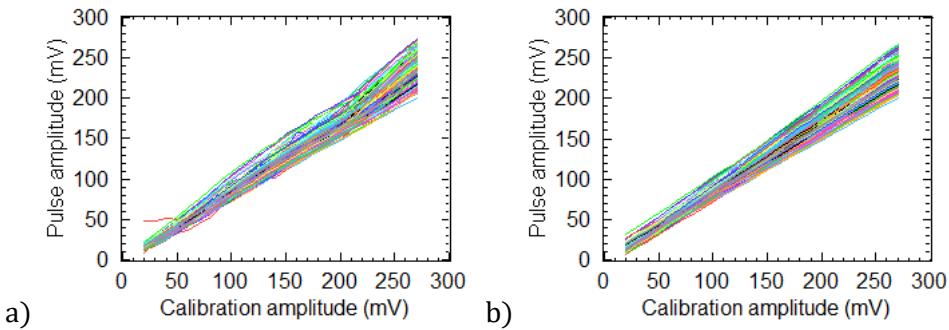


Fig. 6.5 The output pulse amplitude measured for 432 pixels versus impulse calibration amplitude, a) raw data, b) linear fitting models.

in this pixel. Thus, the calibration amplitudes chosen for the SRH tests are not lower than 40 mV to avoid ambiguity in the gain extraction.

The calibration amplitudes of 50 mV, 60 mV, 70 mV and 90 mV are used in the summing and the C8P1 tests. The pulse amplitude spread between the channels needs to be taken into account, since it contributes to the errors in the summing and signals comparison. The spread of the pulse amplitudes between the channels calculated as a standard deviation, equals 2.4 mV, 2.7 mV, 3.0 mV and 3.4 mV, for 50 mV, 60 mV, 70 mV and 90 mV, respectively. The sum of the four abovementioned pulse amplitudes equals 270 mV, with expected spread $\sigma = 6$ mV, assuming that the pulse amplitudes in the channels can be treated as uncorrelated quantities.

The experiments regarding the pixel contribution into summing, addressed in the next section, were performed selecting clusters of 2 x 2 pixels in the pixel matrix. The signals amplitudes were measured for each pixel in the SPC mode, then the summing in the SRH block was activated by changing the control bits BSF. The arithmetic sum of the measured pulses in the SPC mode was compared with the hardware summation by the SRH block in each cluster to prove the proper operation of the SRH block. However, taking into consideration the expected sum spread $\sigma = 6$ mV, the sum of the pulse amplitudes of four individual pixels working in the SCP mode is expected to differ from cluster to cluster.

6.2.2 Tests of pixels contribution into summing in C8P1 algorithm

The calibration pulse injection circuit was used to test summing of signals in the SRH block and the C8P1 performance. Four different current pulses were injected 10,000 times in the chosen clusters of four pixels sharing a corner to reflect the effect of charge sharing. Fig. 6.6a presents a test scenario for one of the clusters, where the charge is divided between four pixels. Since the following calibration pulse

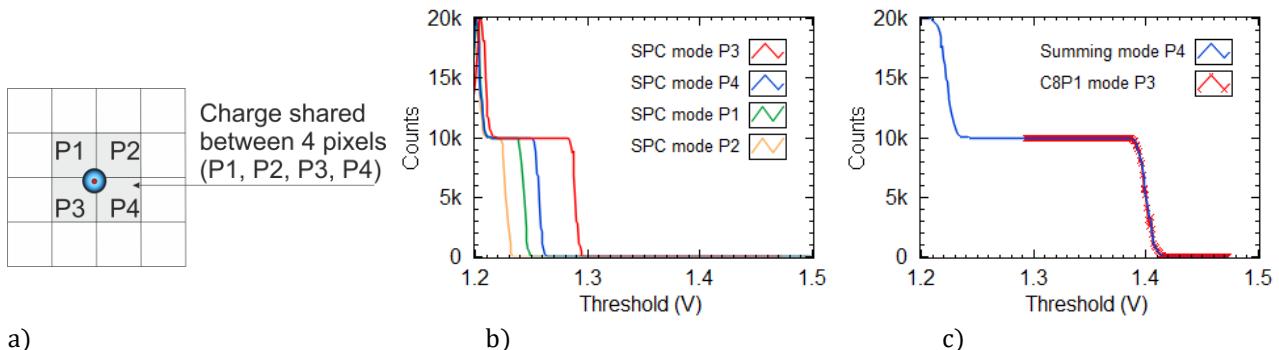


Fig. 6.6 a) The measurement conditions, where pulse injection circuitry injects four different calibration pulses into neighbouring pixels P1, P2, P3, P4, reflecting charge sharing between four pixels. b) Threshold scans in the SPC mode. c) Threshold scans in the summing and the C8P1 modes.

amplitudes were chosen: 90 mV, 70 mV, 60 mV, 50 mV, the pixels received 33%, 26%, 22%, and 19% of the total charge, respectively. To exclude the neighbourhood of the P1-P4 cluster from the analysis, the pixels surrounding the cluster had the CSA_DISABLE switched on (refer to Section 4.2.1).

Firstly, the chip was tested in the SPC mode. The threshold scans for four sample pixels, operating in the SPC mode, are presented in Fig. 6.6b. The pulse amplitudes measured in the pixels P3, P4, P1, P2 equal 86 mV, 57 mV, 41 mV, 29 mV, respectively. Secondly, the summing in the SRH was tested by performing the threshold scans in the summing mode. Finally, the threshold scans were measured in the C8P1 mode. The results for these two modes are presented in Fig. 6.6c. The SRH is physically implemented in the way that it belongs to the left bottom corner pixel of each 4-pixel cluster. Therefore, the highest sum of the signals is observed in the pixel P4 and the C8P1 algorithm assigns the reconstructed summed signal to the pixel with the highest amplitude. Thus, the fully reconstructed signal is allocated to the pixel P3, which received the 90 mV calibration amplitude. The pulse amplitude calculated for the summing mode equals 213 mV. The relative error between the pulse amplitude in the summing mode and the summing individual P1, P2, P3, P4 pixels amplitudes in the SPC mode is 0.1% for the case shown in Fig. 6.6c.

The 18×24 pixel matrix was divided into 2×2 separate pixel clusters, resulting in the 48 pixel clusters. The tests presented in Fig. 6.6 were performed for all the clusters, marked in the counts map with the white squares, to obtain the statistical information on how well the total signal is reconstructed by the SRH and the C8P1 algorithm. The tests of the selected 4-pixels clusters show that the total signal amplitude is reconstructed by the summing block with 2.9% calculated as a mean relative error. The clusters with invalid signals were excluded from the analysis.

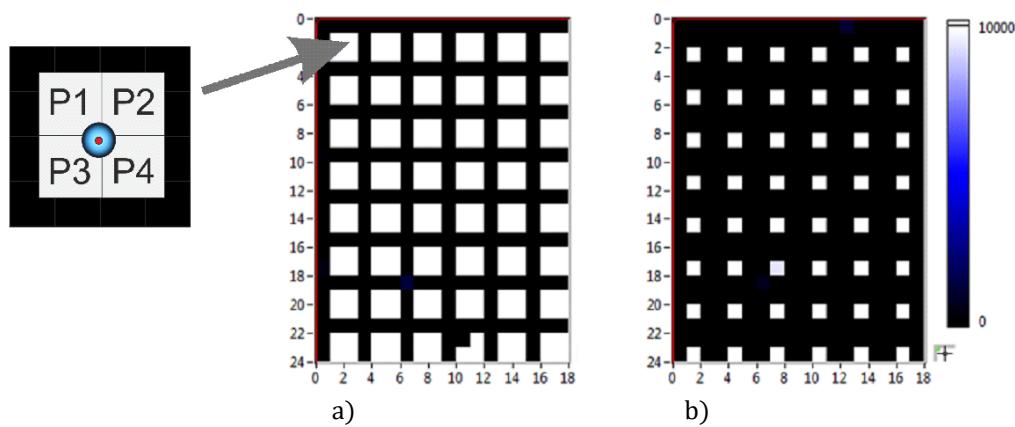


Fig. 6.7 Four different calibration pulses are injected in the clusters of the neighboring pixels. Number of counts measured in the pixel matrix when the chip operates in a) the SPC mode, b) the C8P1 mode.

The map of the number of counts in the pixel matrix, when four different calibration pulses are injected in the 48 clusters of neighbouring pixels, is presented in Fig. 6.7. In the experiment in Fig. 6.7a, the threshold is set just above the noise level and all the pixels with the pulse injected, except of one dead pixel in the last row, counted 10,000 events. If the average values \bar{V}_0 and \bar{V}_{noise} were calculated for all the pixels in the matrix, and the global threshold was set to $(\frac{\bar{V}_0 - \bar{V}_{\text{noise}}}{2})$, none of the pixels would register the events in the SPC mode, because fractional signals amplitudes were too small.

In contrast, Fig. 6.7b shows that the pixel P3 with the highest signal amplitude was properly chosen by the C8P1 algorithm as the ‘winner’ in all of the examined clusters, while the rest of the pixels did not register any signal. It can be concluded that the C8P1 algorithm, preceded by the correction of the chip, allows reconstructing the total amplitude by summing the individual pixel pulses. The analogous tests for the uncorrected pixel matrix and the influence of correction on the C8P1 algorithm is discussed in the following chapters.

In this Section, the tests with clearly distinguishable pulse amplitudes were presented. The purpose of these tests was to reflect the most common case in which the photon interaction occurs inside a pixel. The hits were allocated by the algorithm to the pixels which received the highest amplitude pulse. The case of the equally divided charge reflects the rare case of photon interaction exactly at the pixel border or in the pixel corner. Although rare, these cases should be studied, since they may introduce specific conditions for the C8P1 algorithm.

6.2.3 Influence of correction on C8P1 results

As shown in the previous chapter, the C8P1 algorithm leads to the reconstruction of the total signal amplitude and allocates events to pixels with the highest fractional amplitudes. However, this is possible only when the uniformity of the analog readout channels parameters is assured in the pixel matrix. Referring to the studies of the correction results presented in Section 6.1, the large DC offset spread and gains spread make setting a global threshold for the proper operation of the C8P1 impossible. Moreover, large gains spread results in errors in hit allocations. Therefore, the qualitative analysis of the influence of the correction on the C8P1 results was performed.

The number of counts in the pixel matrix in the C8P1 mode was examined for three cases: before DC offsets and gains correction, after only DC offsets correction, and after DC offsets and gains correction. The same experiment conditions, as described in the previous chapter, were maintained. The results are presented in Fig. 6.8. As shown in Fig. 6.8a, the C8P1 algorithm fails for the not corrected pixel matrix. Some of the pixels which should be ‘winners’ 10,000 times, counted less than 10,000 events, some counted

more than 10,000 events and some did not register any counts. In Fig. 6.8b, the chip is already corrected for the DC offset spread. All of 48 clusters register the hits, however, there are a few clusters in which the winning pixels are not properly assigned or the number of registered events is less than 10,000. The last graph in Fig. 6.8c shows the proper execution of the C8P1 algorithm when all the correction procedures were performed before the tests.

The errors in the number of counts registered in the case of a large DC offset spread are a consequence of the problems with setting a global threshold for all the pixels. To illustrate this mechanism, three threshold scans in the case of a large DC offset spread are shown in Fig. 6.9. The global threshold is properly set for the pixel P2. However, the DC offset shifts the threshold scan characteristics for the pixels P1 and P3. As a result, no counts are registered by P1 and the additional noise counts are registered by P3.

In the case of large gains spread, two types of errors occurred, namely, wrong hit allocations or counting less events. The reason of choosing a wrong winning pixel is the non-uniformity of the gains

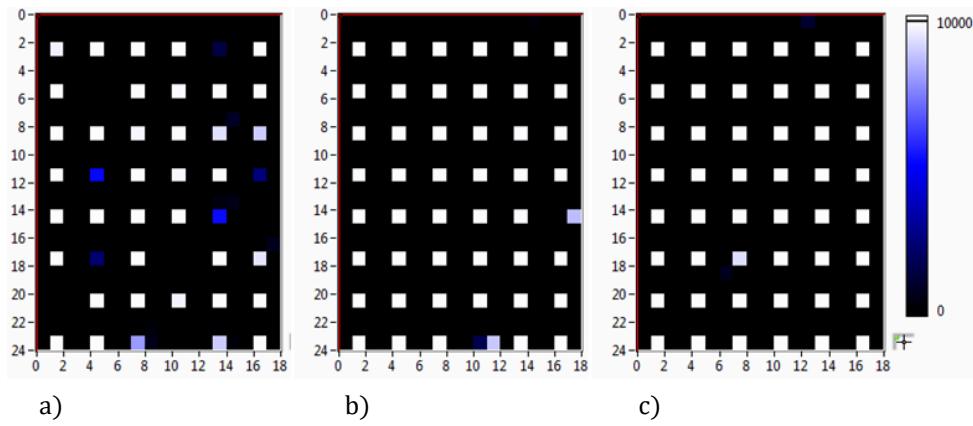


Fig. 6.8 The number of counts measured in the pixel matrix when the chip operates in the C8P1 mode a) before correction, b) after DC offsets correction, c) after DC offsets and gains correction.

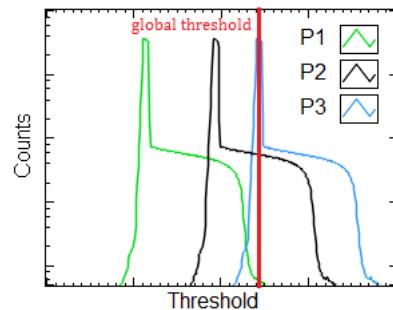


Fig. 6.9 Schematically presented threshold scans for three pixels P1, P2, P3 in the case of the large DC offset spread.

in the pixel matrix, causing the wrong comparison results. The smaller number of counts can be registered due to two reasons. The first one is a low signal amplitude at the SRH, resulting in the V_0 value close to the global threshold. The second is such gain spread among four pixels in a cluster that resulting pulse amplitudes are very similar. Then, the C8P1 algorithm may not choose any of the pixels. This observation was a motivation for further studies of the C8P1 performance in the pencil beam tests using synchrotron radiation.

6.2.4 Emulation of pencil beam test using calibration circuit

The aim of a pencil beam test is to observe the detector response and evaluate the C8P1 performance, when photons hit a detector at known locations at the border between pixels. The experiment environments for the pencil beam tests are described in Section 1.2.3. However, before the tests at the synchrotron facility are performed, the calibration circuit can be used to emulate the conditions of the pencil beam test.

An X-ray beam movement from the pixel P1 to the pixel P2 along the axis parallel to the pixels' edge, which is presented in Fig. 6.10, was emulated by injecting different values of the calibration pulses to the pixels P1 and P2. The idea of the tests was similar to the simulations described in Section 3.2.1. The calibration pulse values for each simulated beam position were calculated assuming the Gaussian model of the charge cloud, introduced in Section 1.5.2. The charge collected by each pixel is defined as an integral on an interval determined by the pixel sizes. When the photon impact position denoted as x is close to the pixel border x_0 , the charge is divided between the pixels P1 and P2.

The parameters of the charge cloud model were calculated for the 320 μm thick silicon sensor, working under the nominal bias conditions. The amplitude coefficient depending on the photon energy was set to 4,500 e $^-$, while the spread of the charge cloud was set to $\sigma = 20 \mu\text{m}/3$. From the photon impact position, denoted as (x,y) , x was varied within the range of $-50 \mu\text{m}$ to $50 \mu\text{m}$ with the $0.5 \mu\text{m}$ step, while y was kept constant. For each step, the threshold scans were measured.

The resulting threshold scans for 200 measurement steps are shown in Fig. 6.11a and Fig. 6.11b, for the chip operating in the SPC and the C8P1 mode, respectively. The blue counts are those measured by the pixel P1, and the orange ones by the pixel P2. In the SPC mode for the $x \approx 0$ position corresponding to the pixel border and for low threshold values of about 1.2 V, both pixels P1 and P2 register 10,000 counts. However, for the higher threshold values of about 1.3 V, the number of counts drops down to 0 in both pixels. Thus, if a hit occurs near the pixel border, either both or none of the pixels may register such an event, depending on the threshold setting. In the C8P1 mode, the orange and the blue surfaces do not overlap,

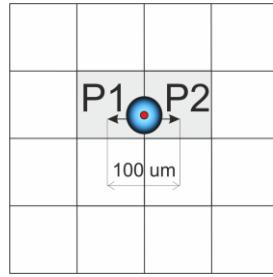


Fig. 6.10 The measurement conditions when the pulse injection circuitry injects two different calibration pulses into the neighbouring pixels P1 and P2 emulating X-ray beam movement along the axis.

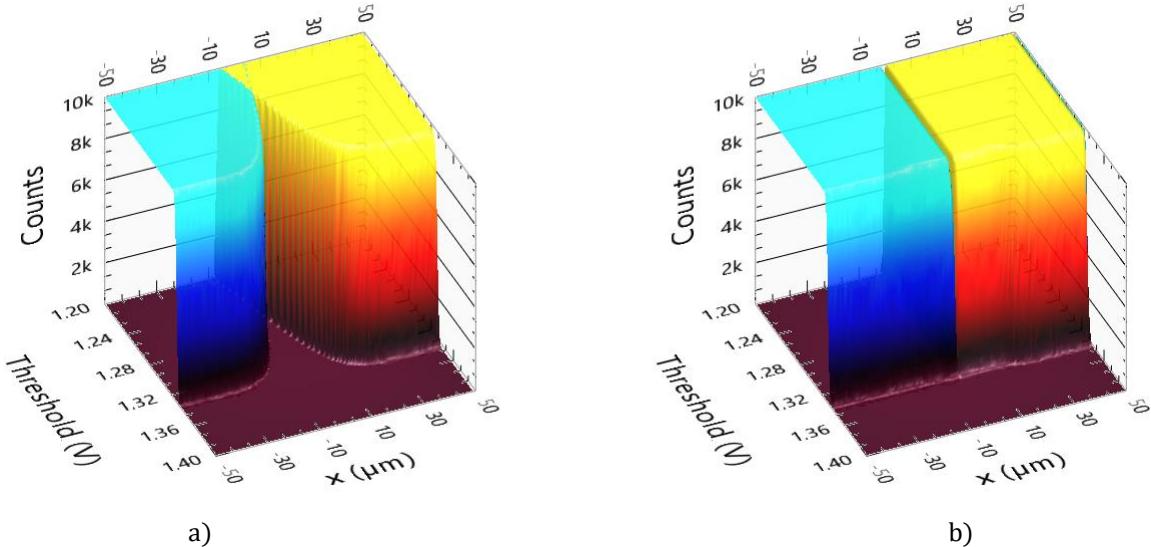


Fig. 6.11 a) The number of counts versus threshold and distance from the pixel border in a) the SPC mode b) the C8P1 mode. The pixel P1 is represented with blue and P2 with orange colour.

which means that each hit is assigned to only one pixel every time by the C8P1 algorithm. When the pulse amplitudes in the SPC mode are compared with the pulse amplitudes in the C8P1 mode for $x_0 = -50 \mu\text{m}$ or $x_0 = 50 \mu\text{m}$, it can be also observed that the total signal amplitude is recovered in the C8P1 mode, irrespectively of the simulated beam position.

6.3 Experimental results of tests with X-ray radiation

The XPCS experiments are the planned application for the detector equipped with the readout integrated circuit, like the Chase Jr. chip. Typically, photons of the energy in the range from 7 keV to 10 keV are used for these types of experiments [94]. Therefore, the 8 keV sources were chosen for the detector tests. The X-ray sources used for the tests and the test set-up are described in Section 6.3.1.

Experiments with 8 keV photons are challenging for photon counting detectors. It is due to the fact that fractional signals induced in the neighbouring pixels may be comparable to the noise and the magnitude of the analog parameters spread, while charge is shared. Nevertheless, the correction procedures performed before the tests allowed registering the incoming photons despite their low energy of 8 keV.

The tests of the detector included the pencil beam experiments for the C8P1 algorithm assessment and the flat field illumination experiments for the detector examination under the high-flux conditions. The first type of tests served for answering the question if the photon energy is properly reconstructed when charge is shared between the pixels. Moreover, the tests verified whether the incoming photons are not missed in the case of nearly evenly shared charge and whether the C8P1 algorithm allocates the events to one of the neighbouring pixels each time. The measurement results are discussed in Sections 6.3.2 and 6.3.3. The influence of the correction on the C8P1 performance is also studied.

The high count rate capabilities of the detector were examined in the flat field illumination tests, and are addressed in Section 6.3.5. An implementation of an algorithm with inter-pixel communication contributes to the dead time, since the neighbouring pixels are blocked from further registrations during each allocation process. In order to gain an insight into the phenomena, the detector responses for a high photon flux were quantified and compared between the SPC and C8P1 modes.

6.3.1 Experiment set-ups

6.3.1.1 Pencil beam tests with synchrotron radiation

The tests were performed with an 8 keV photon beam generated at the Advanced Photon Source at Argonne National Laboratory. The experiment was set up on the 1BM-B beam line. The synchrotron facility was introduced in Section 1.2.2 and the idea of the pencil beam tests was presented in Section 1.2.3. To obtain a pencil X-ray beam with a narrow wavelength distribution and collimated to a small cross-section, a silicon crystal monochromator and a platinum-iridium pinhole collimator with a nominal diameter of 3.5 μm were used. The beam intensity allowed registering on the order of 10-30 kphotons/s after the pinhole. This was checked with a reference photodiode by measuring its photocurrent. The module was located perpendicularly to the beam and the movement of the detector was provided by the ESP301 motion controller connected to the Newport CM25A X-Y stages. The experiment set-up is presented in Fig. 6.12.

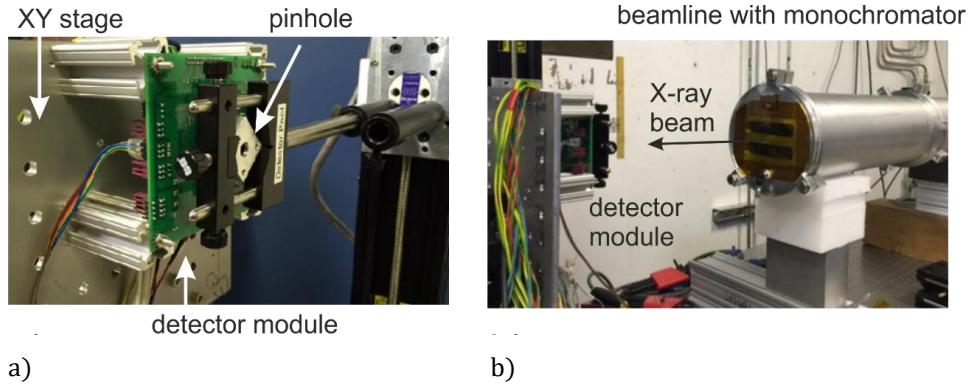


Fig. 6.12 The experiment set-up for the tests with synchrotron radiation at the APS facility.

In the experiment, the position of the detector in front of the beam was changed, while the detector settings were maintained. During the measurement results analysis, a steady beam intensity decrease was revealed for the entire allocated beam time. The number of counts registered by the detector plotted as a function of time during a part of the allocated beam time is presented in Fig. 6.13a and Fig. 6.13b. For example, during Test 3, which lasted about 160 minutes, the average number of registered events decreased by almost 9%. The reason for the decrease of the number of counts was identified as cooling off of the crystal monochromator, which was heated by other research station users in the preceding experiment. Since the aim of the tests was to analyse the numbers of counts obtained in the measurements performed within several hours, there was a need for adjusting the monochromator angle several times during the tests to obtain the desired higher beam intensity. The changes in the intensity, which were discovered during the data analysis, were identified as a factor that would adversely affect the analysis, leading possibly to wrong conclusions from the comparison of the experimental results. Therefore, the post-processing compensation for the intensity loss was considered and introduced.

The sudden drops of the numbers of the counts in Test 2, and Test 4 visible in Fig. 6.13a and Fig. 6.13b, happen during the pixel border crossing by the beam when the chip operated in the C8P1 mode with uncorrected gains, and in the SPC mode, respectively. They are not present in Test 3, since the chip operated in the C8P1 mode with the corrected gains. Since these sudden drops are not caused by the external conditions, the measurements taken at the pixel border were excluded from the intensity correction analysis.

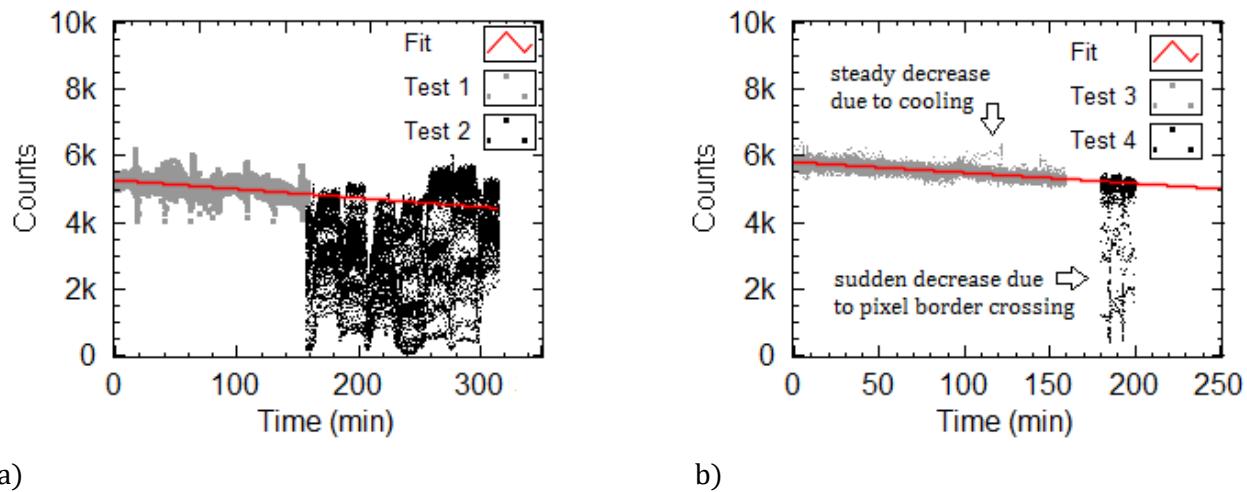


Fig. 6.13 The number of counts measured during the experiments a) Test 1, Test 2, b) Test 3, Test 4 with a visible steady counts decrease due to the monochromator cooling off.

Both, the monochromator cooling off process and the dependency of the beam intensity on the temperature of the monochromator crystal, are of unknown time dependence and may be non-linear. However, since the temperature was decreasing slowly, the measurement results could be approximated with a linear function within the experiment time range. The linear model fitted to the measurement data is marked in red in Fig. 6.13a and Fig. 6.13b. The calculated slope equals -2.7 counts/min for Test 1, and -3.22 counts/min for Test 3. After Test 2, and before Test 3, the monochromator settings were adjusted to obtain again higher beam intensity at the detector. The results presented in the following chapters are corrected for the intensity with the calculated factors, unless stated otherwise.

6.3.1.2 Flat field illumination tests

The flat field illumination tests of the Chase Jr. chip addressed in the further sections were performed using the Rigaku X-ray generators equipped with a Cu anode, emitting 8.0 keV photons. The idea of the flat field illumination tests was described in Section 1.2.3. The photographs of the measurement environment are presented in Fig. 6.14. It consists of the Rigaku X-ray tube, the X-ray detector module with the Chase Jr. chip and the control module, which has been already described in Section 5.3. The detector module was positioned so that all the detector area was uniformly illuminated with the photons.

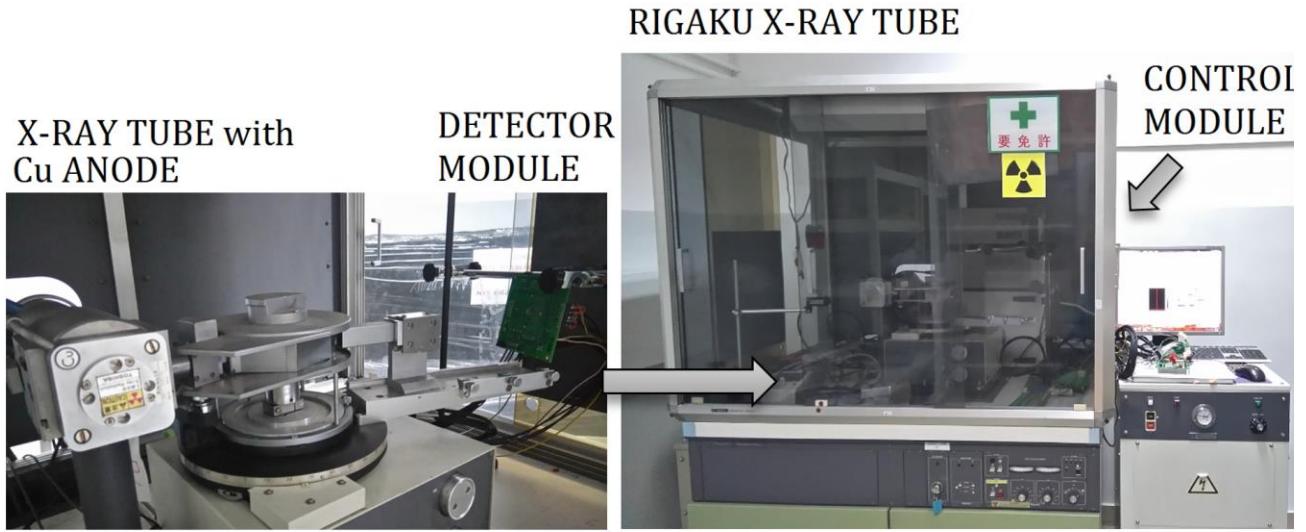


Fig. 6.14 The photographs of the measurement set-up used for the flat field illumination tests of a detector with the Chase Jr. chip.

6.3.2 Tests of signal reconstruction in the case of charge sharing

The measurements with synchrotron radiation are needed to assess the detector and the C8P1 performance, in particular, for the events occurring at the pixel borders. To verify if the photon energy is reconstructed by the C8P1 algorithm, similar tests to those described in Section 6.2.2 were performed with 8 keV X-ray radiation. The pencil beam was positioned close to the pixel borders of some pixels in the matrix. The threshold scans in the SPC and C8P1 modes were measured for two cases, specifically, when the photon interactions occurred close to the borders between two pixels and close to the corner between four pixels.

6.3.2.1 Charge sharing between two pixels

The pencil beam position and the measurement results for the photon interactions occurring close to the pixel border between the pixels P1 and P2, which were arbitrarily chosen, are presented in Fig. 6.15. When the charge is shared not evenly between the two pixels, which is schematically shown in Fig. 6.15a, the pixels P1 and P2 register the signals of different amplitudes in the SPC mode. This is represented with the blue plots in Fig. 6.15b. Both signal amplitudes are lower than the level corresponding to the photon energy of 8 keV. Moreover, due to the beam position shifted towards the pixel P1, the signal amplitude measured in P1 is 3.5 times higher than in P2. The red plots in Fig. 6.15b represent the number of counts measured in the C8P1 mode. As described in Section 2.3.2, two discriminators, ‘high’ and ‘low’ are used in

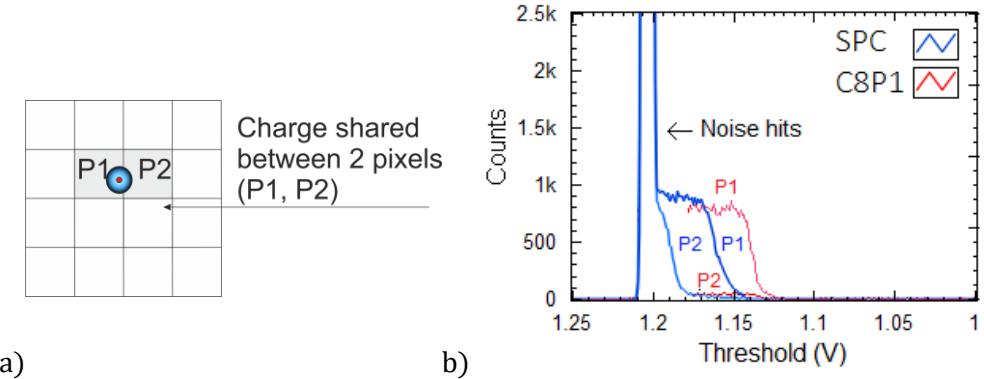


Fig. 6.15 The measurement assumptions: the photon interactions occur close to the border between neighbouring pixels P1, P2. Charge is shared between these two pixels. b) Threshold scans for the pixels P1, P2 in the SPC mode (blue plots) and in the C8P1 mode (red plots).

the design of the Chase Jr. chip. The discriminator ‘low’ threshold used for triggering was set to the value of 4 keV, therefore, the tests were restricted to registration of the events exceeding the 4 keV energy threshold in the C8P1 mode. This is the reason why ‘noise peak’ is not visible in the C8P1 mode.

When the chip operates in the C8P1 mode, the total photon energy is reconstructed in the summing process. The algorithm allocates 95.5% of the hits to the pixel P1, and the rest to the pixel P2. The allocation of some of the hits to the pixel P2 can be caused by noise for the cases of charge shared more evenly. It should be noted that the exact hit position is unknown and it varies within the range limited by the pinhole.

6.3.2.2 Charge sharing between four pixels

The pencil beam position and the results of the test, when the events occur close to the corner between four neighbouring pixels P1-P4 are presented in Fig. 6.16. The charge corresponding to the 8 keV energy of photons is divided nearly equally between the pixels, which is depicted in Fig. 6.16a. The signals registered in the SPC mode are represented in Fig. 6.16b with blue curves. The signals are of such low amplitudes, that they are not distinguishable from the noise. To conclude, it is impossible to set the threshold properly in the SPC mode to register 8 keV photons, when the interactions occur in the pixel corner.

However, when the chip operates in the C8P1 mode, unlike in the SPC mode, the signal corresponding to the total energy of 8 keV is recovered. The red plots in Fig. 6.16b represent the signals measured in the pixels P1-P4 in the C8P1 mode. Since charge is shared nearly evenly, the algorithm allocates the hits to the pixel P1, P2, P3, P4 in 32.8 %, 5.4%, 43% and 18.8% of the total number of cases, respectively due to noise and variability of exact photon impact positions.

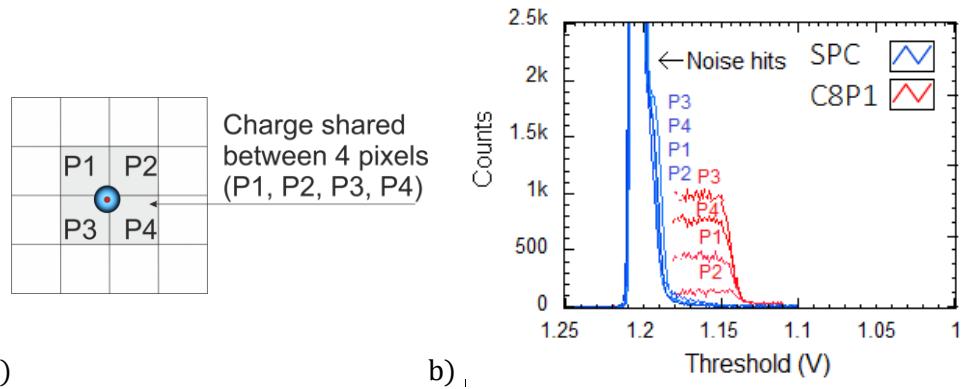


Fig. 6.16 a) The measurement assumptions: the photon interactions occur close to the corner between the neighbouring pixels P1, P2, P3, P4. Charge is shared between four pixels. b) Threshold scans for the pixels P1, P2, P3, P4 in the SPC mode (blue plots) and the C8P1 mode (red plots).

The experiments prove that the total signal corresponding to the photon energy of 8 keV can be recovered when the chip operates in the C8P1 mode, even for the events occurring in the pixel corner. The allocation of the hits depends on the exact hit position, and, consequently, on the proportions of the charge divided between the neighbouring pixels. Noise contributes also to the allocation process.

6.3.3 Tests of registration at pixel borders

In the experiments described in the previous section, it was shown that the signal amplitude can be reconstructed by the C8P1 algorithm, which allows setting a threshold to register events occurring even for the beam set at the pixel borders. However, to fully evaluate the C8P1 performance, it should be verified if all of the incoming photons are detected and if there are no losses in the number of the registered counts in the C8P1 mode, when interactions occur close to a pixel border with respect to the registered counts when the beam is in the centre of a pixel. Therefore, the tests of chosen ROIs on the detector were performed to verify if each time, when a photon interacts with a sensor, a hit is allocated to a pixel. Since the initial number of photons in the beam is unknown, the test results for the central and border pixel areas in the SPC and the C8P1 mode were compared to achieve the targeted goal.

During the tests, the pencil beam location on the detector was changed along the X and Y axes, scanning the ROIs of $250 \mu\text{m} \times 250 \mu\text{m}$ and $700 \mu\text{m} \times 700 \mu\text{m}$ sizes with the $5 \mu\text{m}$ step. The idea of a ROI scan is presented in Fig. 6.17. The detector was scanned line by line along an axis parallel to a pixel edge by a beam. In each location, the total number of counts registered by the detector was measured in a 100 ms time exposure window, chosen to prevent the counter from overflowing. The average values \bar{V}_0 and \bar{V}_{noise}

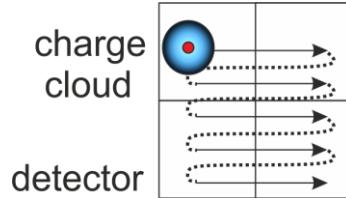


Fig. 6.17 The idea of the ROI scan with a pencil beam.

were calculated for all the pixels in the matrix, and the global threshold was set to $\left(\frac{\bar{V}_0 - \bar{V}_{\text{noise}}}{2}\right)$. The total number of counts was plotted as a function of the beam location on the detector.

The intensity correction introduced in Section 6.3.1.1 was applied. The results of the correction are presented in Fig. 6.18. The intensity plots in Fig. 6.18a and Fig. 6.18b show the number of counts as a function of the beam position before and after the intensity correction, respectively. The correction compensated the slope profile which is visible on the cross-section along the Y axis in Fig. 6.18c. The cross-sections after the correction do not show any profile in Fig. 6.18d. After the correction, the number of counts measured by the detector can be compared between the SPC and the C8P1 mode.

The chip configuration was set to optimise the C8P1 performance. The time of latching the comparison result between the pixels, controlled with the ‘Latch Delay’ (LD) registers was chosen to minimise the errors in registrations at the pixel borders. The sample results of scans for LD = 0, corresponding to the minimum programmable delay, and LD = 15 are presented in Fig. 6.19a and Fig. 6.19b. Too short delays result in errors in counting the events at the pixel borders. This can be related to the timing properties of the discriminators, and latching result too early. For large LD values the signals might be of the amplitude in the range of noise or analog parameters spread when the comparison result is latched, or even, the signals might be compared on the overshoot of the analog response. Therefore, LD = 15, for which no pixel border effects were observed, was chosen for the further tests.

The results of the measurements of a 250 $\mu\text{m} \times 250 \mu\text{m}$ ROI in the C8P1 mode and in the SPC mode are presented in Fig. 6.20. In the C8P1 mode in Fig. 6.20a, the pixel borders are nearly not distinguishable, which can be also examined on the cross-sections plotted for the Y=60 μm and Y = 85 μm positions for the C8P1 mode presented in Fig. 6.20d. In the SPC mode, the borders between the pixels can be recognised on the counts map presented in Fig. 6.20b. The decrease in the number of counts from 6,000 even down to 1,000 for the pixel borders can be observed on the cross-section for the Y=60 μm and Y = 85 μm positions, presented in Fig. 6.20e. The counts map in the C8P1 mode and the estimation of the charge cloud size from Section 6.2.4 allowed dividing the ROI into two areas, namely,

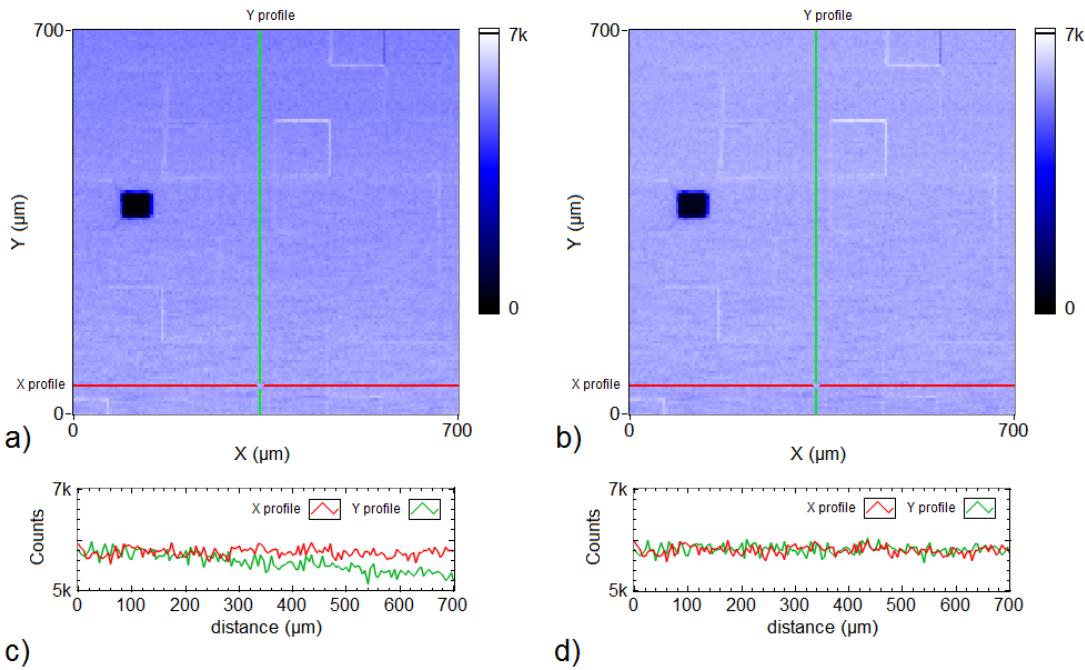


Fig. 6.18 The map of counts for the scan of the 700 μm x 700 μm ROI in the C8P1 mode a) before and b) after the intensity correction. The cross-sections parallel to X and Y axes c) before and d) after the intensity correction.

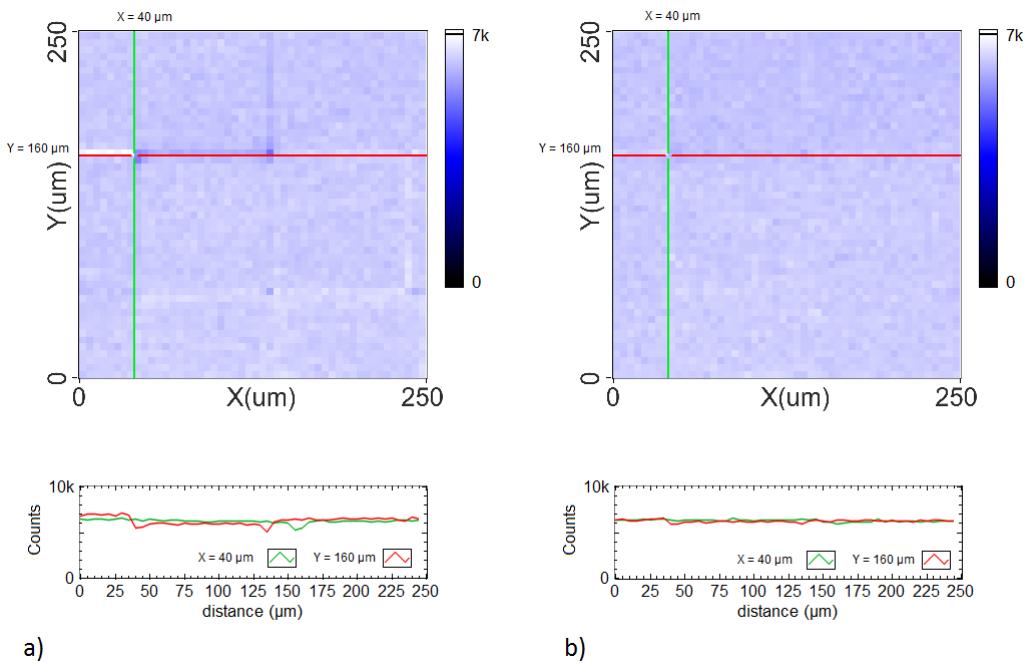


Fig. 6.19 The map of counts for the scan of the 250 μm x 250 μm ROI in the C8P1 mode a) with LD = 0, b) LD = 15.

the pixel borders and the pixel central areas. To define the pixel border areas, the matrix in the SPC mode was scanned and the beam positions in which at least 10% decrease in the counts in the SPC mode was observed, were flagged as potential borders. Then, the column (m) in which all the points are flagged together with the columns ($m-1$) and ($m+1$) were added to the pixel border areas. The analogous operation was performed on the rows, which resulted in the constructed pixel border width of 15 μm . It means that, theoretically, if a photon hits the detector outside of the pixel border area, one pixel collects at least 98% charge. The selection of the pixel border areas and the pixel central areas for 250 $\mu\text{m} \times 250 \mu\text{m}$ ROI is marked in Fig. 6.20c.

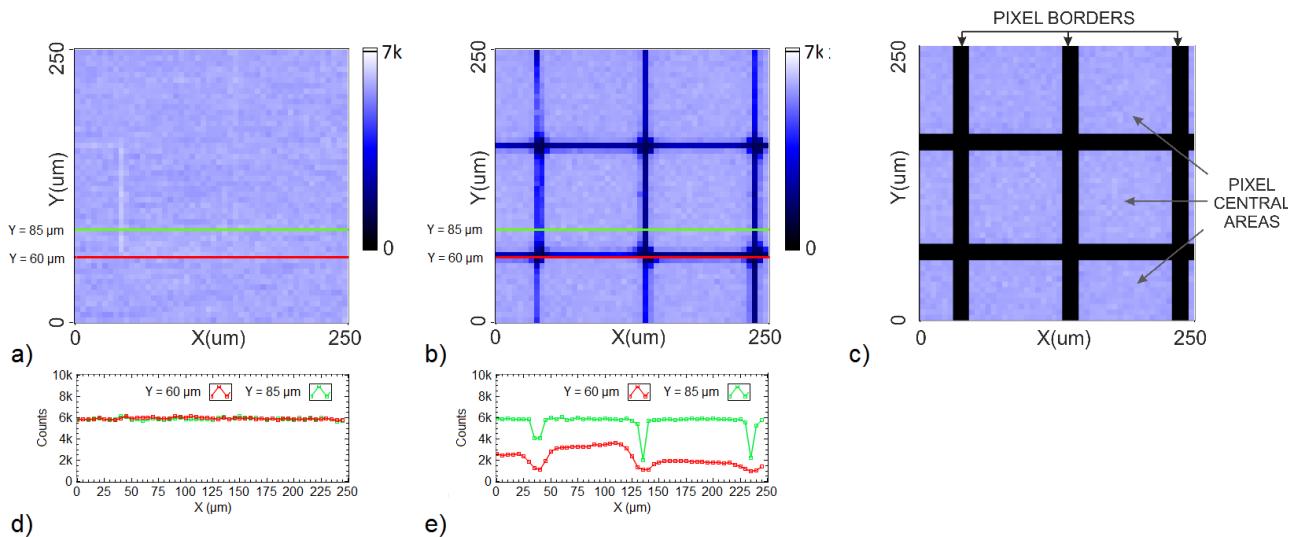


Fig. 6.20 The map of counts for the scan of the 250 $\mu\text{m} \times 250 \mu\text{m}$ ROI a) in the C8P1 mode b) in the SPC mode. c) ROI division into two areas, namely, the pixel borders and the central pixel area. The cross-section parallel to X axis for Y=60 μm and Y=85 μm for d) the C8P1 mode and e) the SPC mode.

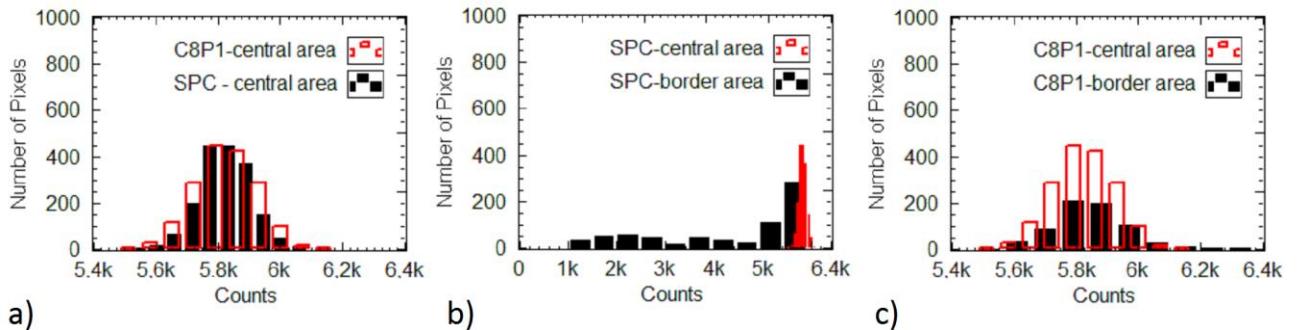


Fig. 6.21 The histograms comparing the numbers of counts in a) the central pixels areas for the C8P1 and the SPC mode, b) the central pixels areas and the border areas for the SPC mode, c) the central pixels areas and the border areas for the C8P1 mode.

Firstly, it was verified whether the number of counts is the same for the SPC and the C8P1 mode, when all the charge is collected by one pixel, meaning that no charge sharing occurs. The aim of the test was to ensure that the C8P1 algorithm does not degrade the detection efficiency. Therefore, the number of counts in the central pixel areas in the SPC and the C8P1 modes were compared. Fig. 6.21a shows the number of counts measured in the detector for the pixel central areas in the C8P1 and the SPC mode. The mean values and standard deviations equal $5819+/-101$ and $5822+/-83$ for the C8P1 mode and the SPC mode, respectively. The difference between the two means is not significant, thus, it can be concluded that there is no decrease in the detection efficiency for the C8P1 mode.

Secondly, it was studied whether the registration efficiency decreases in the pixel border areas. Therefore, the number of counts was compared for the pixel borders and pixel central areas in the SPC and in the C8P1 mode. Fig. 6.21b presents the histogram of the numbers of counts measured in the detector central pixels areas and the border areas for the SPC mode. The average values and the standard deviations equal $5822+/-83$ and $4332+/-1522$ for the central pixels areas and the borders, respectively. It means that there is a significant count number decrease, for the events registered at the borders in the SPC mode. Fig. 6.21c shows the analogous histogram for the C8P1 mode. The average values and the standard deviations equal $5819+/-101$ and $5845+/-122$ for the central pixels areas and the borders, respectively. It means that there is no significant count number decrease, for the events registered at the borders in the C8P1 mode.

In conclusion, comparing the experimental results measured in the C8P1 and in the SPC mode, it can be deduced that the events are not lost in the C8P1 mode, regardless of the photon interaction location, which was the goal of this part of work.

6.3.4 Influence of correction on C8P1 performance

The measurements with low energy photons introduce a challenge to a photon counting detector, especially in the case of charge sharing. It was already shown in Section 6.2.3, that a large analog parameters spread degrades the detection efficiency, since it makes setting a global threshold impossible. Moreover, in the case of the C8P1 algorithm, it has an impact on the comparison of the signals in the slow path. To study the influence of the gains correction on the C8P1 performance, the scans of a $700\text{ }\mu\text{m} \times 700$ ROI were performed for two cases of an uncorrected pixel matrix. The DC offset correction procedure was performed and the first scan was measured for the non-equalized CSA gains and the SH gains. The second scan was measured for the equalized CSA gains but the non-equalized SH SLOW gains.

In the first case, the BCSA registers were set to 5 for all the pixels, resulting in the average gain equal to $10.89 \mu\text{V/e-}$ in the ROI, while the average gain for the corrected matrix equals $13.06 \mu\text{V/e-}$. The results of the scan, in which the total number of counts registered by the detector is measured with respect to the beam position, is presented in Fig. 6.22a. The gains spread in the pixel matrix and the lower average gain resulted in a degradation of the detector performance. The total number of counts in the whole matrix decreased. The number of counts is different for each pixel and the borders between pixels are distinguishable, which can be observed also on the cross-section in Fig. 6.22b. The main mechanism responsible for these issues degrading the detector performance is that when the pixels with the lower gains contributes to the sum in the SRH, the sum from four pixels do not satisfy the condition of exceeding the triggering threshold. It should be noted that one pixel with the lower gain affects four SRHs to which it is connected.

During the second test, the CSA gains were equalized and the SH SLOW gains remained uncorrected. The resulting map of counts and the cross-sections are presented in Fig. 6.22c and Fig. 6.22d, respectively. The number of counts is stable in the entire pixel matrix, only slight variations of the number of counts are visible at the pixel borders. The large gain spread in the slow processing path does not influence the activation of the algorithm in the fast path. Therefore, the events are registered by the detector. However, wrong allocations of hits might happen, when a pixel which collected less charge, wins the comparison. It might occur when due to a larger gain, the pixel has larger signal amplitude at the SH SLOW output. Such a case was also investigated in Section 6.2.3.

In conclusion, since the CSA gain affects both the fast and the slow signal processing paths, its equalization is crucial for the detector performance. The large CSA gain spread, and the low gain for some pixels result in a lack of activation of the C8P1 algorithm and, consequently, it results in a lack of registration of some of the incoming photons. The large SH SLOW gains spread does not affect the activation of the algorithm, thus, the events can be registered, although the allocation of the hit might be incorrect due to the errors in comparisons. Since the exact photon position at the detector in this experiment is unknown and the scans present the total number of counts in the detector, the correctness of allocation cannot be determined in this test. The pencil beam tests served for the investigation of a possible count loss, whereas, the tests with the calibration circuit allowed studying the hit allocation. The results of these tests, both with and without X-ray radiation, prove that the C8P1 allows the reconstruction of total photon energy and the registration of correct numbers of events only if the correction procedures are performed to the satisfactory level before the tests.

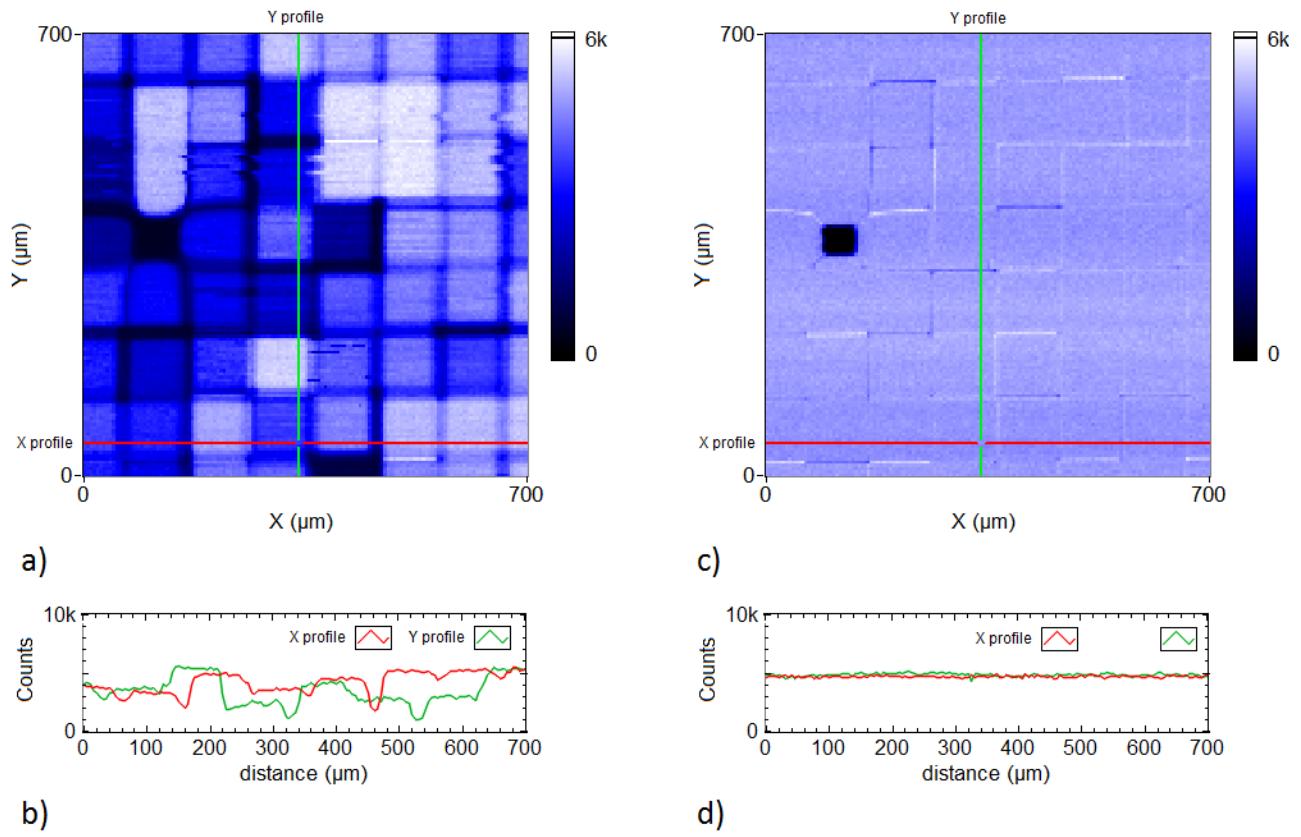


Fig. 6.22. a) The map of counts for the scan of the 700 μm x 700 μm ROI in the C8P1 mode for uncorrected both CSA gains and SH SLOW gains and b) a corresponding cross-section. c) The map of counts for corrected CSA gains and uncorrected SH SLOW gains and d) a corresponding cross-section.

6.3.5 High count rate tests

An algorithm with the inter-pixel communication is expected to contribute to the dead time, since the neighbouring pixels are blocked from the registration during each ongoing allocation process. Therefore, the detector responses for a high photon flux were quantified and compared between the SPC and C8P1 modes. The measurements were performed using the set-up presented in Section 6.3.1.2. The tube current was changed within the range 10-200 mA, and the tube voltage was set to 40 kV. The Chase Jr. chip underwent the correction procedures and the default settings were applied. The number of counts was measured for increasing photon fluxes and the measurement results are presented in Fig. 6.23a and 6.23b, for the chip operating in the SPC mode and in the C8P1 mode, respectively. The paralysable detector

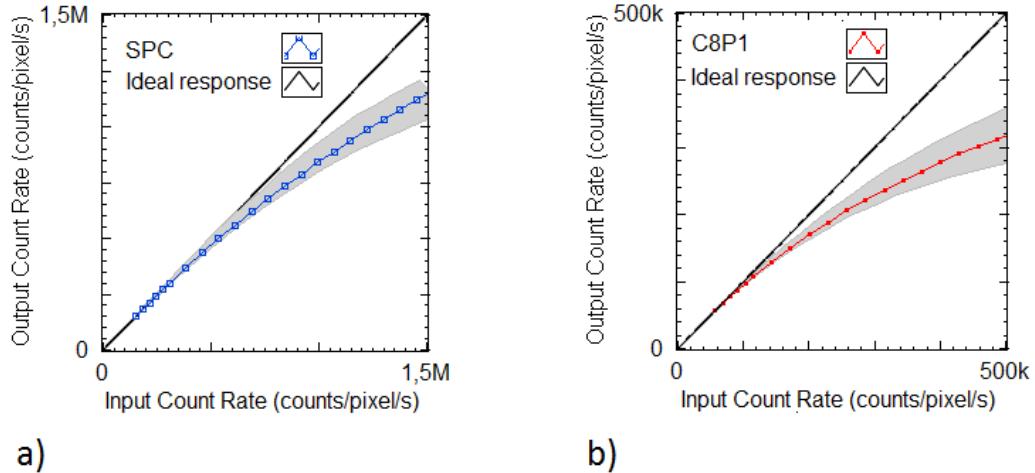


Fig. 6.23. The output count rates plotted as a function of the input count rates fitted to the paralysable model for the chip operating in a) the SPC mode and b) the C8P1 mode.

model, given by Eq. 1.28, was used to extract the dead times for both cases. The average dead time was estimated $\tau = 0.21 \mu\text{s}$ for the SPC mode, and $\tau = 1.01 \mu\text{s}$ for the C8P1 mode. As a reference, the results available from the recent linearity test of Medipix3RX show that the dead time in the charge summing mode is not lower than $\tau = 2.02 \mu\text{s}$ [95]. The 10% loss input rate calculated using the paralysable dead time model equals $1.02 \times 10^7 \text{ photons/mm}^2\text{s}$ for the C8P1 mode.

It can be concluded, that the Chase Jr. chip operating in the C8P1 mode can work under the high-flux conditions, however, the estimated dead time is around five times larger than the value calculated for the chip operating in the SPC mode.

6.4 Conclusions on measurement methods and C8P1 algorithm performance

In Chapter 6 the methods of evaluation of an inter-pixel algorithm dealing with charge sharing were introduced. The verification procedures developed during the research involved the preliminary tests with the calibration pulse injection circuit. The proposed tests allowed injecting different pulse amplitudes to the neighbouring pixels, reflecting the signals induced in the case of charge sharing. Moreover, the injection of pulses to many clusters at the same time allowed the validation of the whole matrix in terms of the amplitude reconstruction by the C8P1 algorithm. Analogous tests with X-rays take longer, since the beam must be positioned in each location, separately. Finally, the test emulating the pencil beam movement at the detector can be performed in the laboratory before the tests at the synchrotron facility. Tests with the calibration circuit were also described in [30], [67], [86].

The tests with X-ray radiation were designed to study the detector behaviour in the case of charge sharing, in particular, for rare cases when the charge is shared nearly equally between the neighbouring pixels. The measurement results prove that the digitally-assisted analog circuit with the C8P1 algorithm implemented allowed for cancelation of the effects related to charge sharing in the hybrid pixel detector. The C8P1 algorithm enabled reconstruction of the total signal corresponding even to the low energy photons, such as 8 keV. The allocation of the events depended on the exact hit position, and, consequently, on the proportions in which the charge was divided between the neighbouring pixels. However, it was proved in the pencil beam tests that, contrary to the SPC mode, all the photon-detector interactions, regardless of the photon interaction location, were registered by the detector in the C8P1 mode. Tests with X-ray radiation were also described in [67], [91], [96].

The digitally controlled blocks, such as DC offsets and gains correction blocks allowed trimming the analog parameters spread which is crucial for the performance of the algorithm dealing with charge sharing. The large DC offset and CSA gain spread were identified as the main cause of errors in a number of counts registered by the detector due to a lack of triggering the algorithm in the fast signal processing path. The large SH slow gains spread was responsible for the wrong hit allocation due to the errors in comparison in the slow processing path. It was shown that the algorithm works properly only if the correction procedures are applied in advance.

Moreover, the future improvements for the correction procedures were proposed, including interpolation in the DC offsets correction. This approach allows maintaining the same correction precision. If higher precision of the DC offset correction is needed, the trim DAC current, controlled with an external bias, can be adjusted, entailing the trim DAC characteristics slope adjustment.

Finally, the high count rate performance of the Chase Jr. chip was evaluated. It was measured that the estimated dead time is about five times larger in the C8P1 mode than in the SPC mode, which was expected. The dead time obtained in the C8P1 mode is $\tau = 1.01 \mu\text{s}$, and the parameter can be further improved in the next generation of Chase Jr. by using the solution of the digitally assisted CSA described in the following publications [97]–[99].

7 CONCLUSIONS AND PROSPECTS

The theoretical analyses, simulations and measurement results for mixed-mode circuits of a readout channel of an integrated circuit for hybrid X-ray detector are presented in this thesis. The readout channel comprises of digitally-assisted analog circuits. Digital assistance refers to readout integrated circuit components, in particular, to digital support of the algorithms dealing with charge sharing, digital to analog converters which are used in the circuits realizing multistage corrections and to digital control of the settings that support reconfiguration mechanisms of the channel functionalities. Such digitally-assisted analog circuits are studied, simulated and tested aiming at the optimisation of the detector performance, especially in the presence of charge sharing.

First, the basic concepts of X-ray detector systems i.e. X-ray generation, X-ray interaction with matter, signal formation in hybrid pixel detector and limitations of readout systems, including charge sharing, were studied. Then, to tackle with aforementioned challenges the information about available solutions was collected and analysed. Known hardware algorithms proposed in the literature, i.e. Pixirad Pixie III, X-Counter, Medipix3/3RX were investigated aiming at understanding their range of correct operating conditions and their limitations. These solutions were compared to the prototype solution, namely the C8P1 algorithm, which was developed proprietarily by the ASIC groups from the AGH and FNAL and built into the Chase Jr. chip and miniVIPIC chip. The C8P1 algorithm became the subject of detailed conceptual analyses and simulations as a known solution to the charge sharing problem. The simulations were conducted in static and dynamic modes in the LabVIEW and Cadence environments. Realistic models, including practical aspects of the circuits, for example non-ideal comparators, noise or analog parameters spread were conceived. The influence of analog parameters spreads on the detector registration efficacy and efficiency was analysed. Required degree of digitally assisted correction was studied in detail in order to obtain satisfactory detection performance. Next, the architecture and design guidelines for the multichannel readout the Chase Jr. chip were described. The operation and configuration of the Chase Jr. chip with an emphasis on analog path reconfiguration for the purpose of testing and trimming was revealed. The target was to experimentally confirm the conclusions obtained through the simulations. For each individual test, the analog path reconfiguration, using available digital resources,

was proposed and test scenarios were designed at this stage. To meet the testing requirements, a dedicated testing system architecture was designed by the author. The system was built from the basic concept, through hardware, to entire software environment combining all the required functionalities under one hood. The compact testing system was implemented in LabVIEW environment, using NI FlexRIO modules. The automated test sequences were programmed and served for validation of the solution dealing with charge sharing implemented inside the Chase Jr. chip, for investigation of the influence of noise and analog parameter spread on the detector performance, and for validation of the digitally-assisted correction procedures. Modularity and reconfigurability of the system, supporting incorporation of different hardware instruments, allowed using the system in different experiment environments, including an X-ray tube and a synchrotron facility. The testing environment could be also reused for the next generation of tests with either new versions of the chip or different measurement equipment. The construction of this test set-up crucially contributed to this thesis goals. A distinguishing feature of the system was the first assembly implementation of the sequence of the correction procedures which were optimised for low time allotment applied in tests of a chip built in a 40 nm process. A silicon sensor was bonded to the Chase Jr. chip and the detector module was tested. Three types of experiments were conducted: the preliminary integrated circuit tests without X-ray radiation performed for calibration purposes, experiments using an X-ray tube and experiments using an X-ray beam at a synchrotron facility. The tests were performed by the author at the Advanced Photon Source at Argonne National Laboratory, Lemont, USA and Rigaku Co., Tokio, Japan. The experiments included tests of signal reconstruction in the case of charge sharing, tests of registration at pixel borders, tests of influence of correction on the C8P1 algorithm and high count rate tests. The aim of the test program was to verify the hardware solution dealing with charge sharing and to provide material supporting the theses of the work. The target application for the detector are XPCS experiments. In the XPCS experiments, it is important to register correct number of photons and calculate timing properties of photon impact and time correlations between impacts in order to study structural dynamics of an investigated sample. In such experiments, typically low energy photons are used, and this is why the simulations and experiments were carried out for 8 keV energy photons.

All of the simulations and experiments were the subject of the research and they resulted in the consistent set of publications [30], [53], [67], [78], [85], [86], [96], [98]. The conducted research was part of a broader study program on the hybrid pixel detectors dealing with charge sharing [68], [100], [101], and the issues of the sensitivity of the algorithms to analog parameters spread was also a subject in the publications [8], [68], [69].

The research for this thesis was held in the international research collaboration, including the Fermi National Accelerator Laboratory, USA and Rigaku Co., Japan. The experiments were conducted at the Advanced Photon Source at Argonne National Laboratory, USA and Rigaku Co., Japan. The work was supported by the Polish National Science Center under Contract UMO-2013/09/B/ST7/01627 and Contract DEC-2014/13/B/ST7/01168.

7.1 Conclusions from simulation results

The analyses of a readout channel were conducted using the analytical and simulation approach. Firstly, it was proven that a model of a readout channel could not be given analytically due to the complexity of the system. The signals originate from multiple sources, are merged and are subject of nonlinear operations. Then, the lack of analytical solutions motivated numerical studies of a readout channel and led to the development of the dedicated simulation environment. The execution time of simulations on the transistor level was not acceptable. Thus, the simulations on a high abstraction level, incorporating behavioural models of the functional blocks, were proposed. The simulation approaches followed the proposed division into static and dynamic strategies.

The simulations based on the static strategy did not take into account changing of signals in the time domain and timing properties of the analog blocks. However, they allowed verification of the algorithm concept, including the tests of the hit allocation procedure and verification of the detection efficiency. To analyse the results of the static simulations, a quality factor Q was introduced, providing information on a degree of the uniformity of registration of photons by a detector. The number of photons of the energy of 8 keV registered in a chosen region of interest of the detector in the SPC and C8P1 modes were compared quantitatively.

The results of the static simulations lead to the following conclusions:

- Assuming typical mean values and their variations of the detector parameters, $Q_{\text{SPC}} = 0.866$ and $Q_{\text{C8P1}} = 0.999$ are obtained, which shows that registration is deteriorated at the pixels borders for the detector with the algorithm dealing with charge sharing switched off, while the C8P1 algorithm allows almost uniform registration.
- Increasing the gain spread, DC offset spread and noise, collectively and individually to the values exceeding the typical levels from two to four times, results in the significant degradation of the Q factor, i.e. to the value of $Q = 0.84$, and thus, translating to the degradation of the detection efficiency in the C8P1 mode.

The photon interaction positions identified in static simulations as prone to registration errors were further investigated in the dynamic approach. In the dynamic simulations, parametrised behavioural models of analog and digital blocks, taking into consideration signals changing in the time domain, were used. Threshold scans were simulated without and with an input signal to perform noise analyses and to investigate a readout channel in the case of charge sharing between two and four pixels.

The results of the dynamic simulations lead to the following conclusions:

- The integrated circuit with the C8P1 algorithm switched on allow reconstruction of the total photon energy from fractional signals in the case of charge sharing between two or four pixels, and thus, the photons can be detected even at pixel borders, where the SPC approach fails.
- The position of the noise peak in the C8P1 mode is found shifted with respect to the SPC mode due to the neighbouring pixel blockage, which impacts also the statistical distribution of the registered hits, leading to the larger noise peak spread and lower maximum number of noise counts registered in the C8P1 mode comparing to the SPC mode.
- The total number of noise hits, defined as the integral number of counts, is more than four times larger in the SPC mode than in the C8P1 mode.

To summarize, two functional models, namely the static and dynamic model, of a mixed-mode circuit of a readout channel of a hybrid X-ray detector with inter-pixel communication were designed. The static approach allowed performing fast simulations for the chosen region of interest of the detector, which involved solving 1,000 events for each of about 14,000 photon impact positions. Then, dynamic simulations, better approximating real operation of the circuit, were performed. The static and dynamic simulations show that the charge sharing effect occurring in hybrid pixel detectors can be compensated by mixed analog-digital circuits implemented inside the readout electronics using inter-pixel communication strategies, which support ‘Thesis 1’ from Chapter 1.1. In the case of charge sharing between up to four readout channels, the signal can be fully reconstructed from the fractional signals. In the case of charge sharing between more than four readout channels, even though the energy cannot be fully reconstructed, the event can be allocated to the proper pixel.

The noise analysis shows that the noise peak obtained in the C8P1 mode cannot be used for the readout channel parameter extraction. For instance, the alternative readout channel gain estimation technique for the detectors with the C8P1 algorithm implemented is proposed. The second parameter differentiating between the C8P1 and SPC modes is the population of the noise peak. Both arguments support ‘Thesis 2’ from Chapter 1.1.

The simulations based on the static and dynamic models show that without trimming the analog parameters, the circuit realizing the C8P1 algorithm cannot perform to the desired degree. There is a need for dedicated correction circuits to minimise the analog parameters spread between channels and assure the proper operation of the detector. This lead to the conclusion that for typical detector parameters, digital correction circuits ought to be implemented to compensate for the analog parameters spread, which fulfils the claim given in ‘Thesis 3’ from Chapter 1.1.

7.2 Conclusions from experimental results

The discussed Chase Jr. chip occupied 2 mm x 4.5 mm of the silicon area and contained a matrix of 18×24 pixels, each of size $100 \mu\text{m} \times 100 \mu\text{m}$. A detector module, consisting of the Chase Jr. chip with the C8P1 algorithm implemented and a silicon 320 μm thick sensor was tested using a dedicated test environment developed as a part of this thesis. The integrated circuit was initially tested without X-ray radiation, using the on-a-chip calibration pulse injection circuits. Preliminary tests consisted of exposures to an X-ray tube for correction purposes. After the preliminary tests, the whole detector was tested at the synchrotron with low energy X-rays.

The results of the experiments lead to the following conclusions:

- The analog circuits in the Chase Jr. chip with the parameters corrected with digital assistance to the values of: the DC offset down to 36 e-, the CSA gain down to 3.8%, the SH SLOW gain down to 2.3% calculated as the standard deviation to mean gain ratios, and with the input-referred noise floor of 117 e- allow operation of the system as if the effects related to charge sharing were not present.
- The allocation of the events to a particular pixel depends on the exact hit position, and, consequently, on the proportions in which the charge is divided between the neighbouring pixels.
- All the photon-detector interactions, regardless of the photon interaction location, are registered by the detector in the C8P1 mode in the pencil beam tests, whereas, events losses are observed in the SPC mode. The number of events registered in the central pixel areas in the C8P1 and SPC modes show that there is no count decrease in the C8P1 algorithm. The number of counts registered in the pixel central areas is equal to $5819+/-101$ and $5822+/-83$, for the C8P1 mode and the SPC mode, respectively. The number of events registered at pixel borders in the C8P1 and SPC modes show that events are not lost in the C8P1 mode, while there is a significant count number decrease in the SPC mode. The total number of counts is equal to $5822+/-83$ and $4332+/-1522$, for the C8P1

mode and for the SPC mode, respectively. The detector with the C8P1 mode switched on registers photons uniformly without events losses.

- While the analog parameters are not trimmed, the large DC offset and CSA gain spreads are recognised as the main causes of errors in the numbers of counts registered by the detector due to a lack of triggering of the algorithm in the fast signal processing path.
- Digitally controlled blocks, such as DC offsets and gains correction circuits allow trimming the analog parameters spread, which is identified to be crucial for the performance of the chip with the C8P1 algorithm at the simulation stage. It is shown that the algorithm works properly only if the correction procedures are applied in advance.
- The average dead times estimated using the paralysable detector model from the measurements under flat field illumination is equal to $\tau = 0.21 \mu\text{s}$ for the SPC mode, and $\tau = 1.01 \mu\text{s}$ for the C8P1 mode, which corresponds well to the simulation results. It is found that these values correspond to the proportions of the populations of the noise peaks in the SPC and C8P1 modes.

To summarise, the measurement results also show that the charge sharing between up to four channels present in hybrid pixel detectors may be compensated by mixed analog-digital circuits realizing algorithms dealing with charge sharing, leading to full energy reconstruction. As it is predicted in simulations and proved in measurements, it is possible to overcome technology limitations regarding analog parameters spread of the multichannel integrated circuits for hybrid pixel detectors with inter-pixel communication, using digitally assisted correction blocks. The correction of the DC offsets at the discriminators, amplifier and shaper gains allow proper energy measurement and proper hit allocation in the case of algorithms for charge sharing compensation implemented inside a chip, which proves ‘Thesis 4’ from Chapter 1.1. The integrated circuit with the pixel sizes of $100 \mu\text{m} \times 100 \mu\text{m}$ was tested. However, it is possible to scale down the pixel dimensions, since additional testing structures are implemented inside each pixel in the chip studied in this work.

7.3 Prospects

The conclusions from simulations and experiments lead to better understanding of dependencies among the signals processed by the circuits embedding complex algorithms in the real implementations. The research on the algorithms dealing with charge sharing implemented in integrated circuits for hybrid pixel detectors shows that the development of a full scale circuit, a successor of the Chase Jr. chip or miniVIPIC, with the algorithm dealing with charge sharing is possible. Both, the results of this work and the conclusions from the experiments presented in the literature [8], [69] show that the full scale chips

suffer from the analog parameters spread and require digital assistance for gain and DC offsets trimming. This work provides guidelines where the trimming is essential and how to conduct it.

It is true that the full energy reconstruction is possible for the charge shared between no more than 2×2 pixels. However, the studies of the C8P1 algorithm show that the same idea of the C8P1 algorithm could be extended to the cases of charge sharing between more than four pixels, since the algorithm always chooses the pixel with the highest signal amplitude among the neighbours. This is an important aspect for thicker sensors and for scaling down the pixel sizes. C8P1-like algorithms optimised for dealing with charge sharing can be also adapted to multi-energy measurements, which means that the technology of hybrid pixel detectors with algorithms dealing with charge sharing can also be attractive for medical X-ray imaging applications.

The estimated dead times for the detectors working in the C8P1 mode are found to be about five times lower than in the SPC mode as a result of this work. In parallel to that, the noise peak analysis in this thesis reveals differences in the population of the noise peaks measured in the threshold scans in the C8P1 and the SPC mode. The correlation between the maximum count rate and the noise peak population is observed. The derivation of the maximum count rate from the noise peak parameters could be an interesting study. However, this is beyond the scope of this thesis and formulates an interesting subject for carrying over this work in a future project.

Deep understanding of the processes inside the C8P1 algorithm, given by this work, stimulate the research towards the algorithms eliminating individual signals comparisons between pixels. Motivation for this future work is reduction of the channel electronics and therefore, smaller power dissipation and smaller real estate occupancy [102]. Entirely unresolved subject in the charge sharing compensation research is how to deal with charge sharing in a multi-modules detector at the border between the chips.

The results achieved throughout the study for this thesis lead to new research perspectives, concerning hybrid pixel detectors applied in medical diagnosis. A new research program has been already established (2016/21/B/ST7/02228) to develop new solutions to dedicated integrated circuits in nanometre technologies for colour imaging. The research concentrates on hybrid pixel detectors with algorithm dealing with charge sharing implemented on a chip. Medical applications require usually operation with high intensities of X-ray fluxes, with several discriminator levels and with large range of photon energies. Thus, sensor materials other than silicon, like CdTe, CZT are also to be considered.

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OŚWIADCZENIE

Oświadczam, świadoma odpowiedzialności karnej za poświadczenie nieprawdy, że niniejszą pracę doktorską wykonałam osobiście i samodzielnie i że nie korzystałam ze źródeł innych niż wymienione w pracy.